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The feasability of implementing a face recognition system based on Gabor filter and nearst nighbour techniques in an FPGA device for door control systems

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Abstract

Door access control systems based on face recognition are geared towards simplifying difficult face recognition problems in uncontrolled environments. Such systems are able to control illumination, offer neutral pose and improve the poor performance of many face recognition algorithms. Door access control systems control illumination and pose in order to overcome face recognition problems. While there have been significant improvements in the algorithms with increasing recognition accuracy, very little research has been conducted on implementing these in hardware devices. Most of the previous studies focused on implementing a simple principal component analysis in hardware with low recognition accuracy. In contrast, the use of a Gabor filter for feature extraction and the nearest neighbour method for classification were found to be better alternatives. Dramatic developments in field programmable gate arrays (FPGAs) have allowed designers to select various resources and functions to implement many complex designs. The aim of this paper is to present the feasibility of implementing Gabor filter and nearest neighbour face recognition algorithms in an FPGA device for face recognition. Our simulation using Xilinx FPGA platforms verified the feasibility of such a system with minimum hardware requirements.

Keywords

door, device, recognition, fpga, face, techniques, nighbour, nearst, filter, gabor, system, feasability, implementing, systems, control

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The Feasibility of Implementing a Face Recognition System Based on a Gabor Filter and Nearest Neighbor Techniques in an FPGA Device for Door Control Systems

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Abstract: Door access control systems based on face recognition are geared towards simplifying difficult face recognition problems in uncontrolled environments. Such systems are able to control illumination, offer neutral pose and improve the poor performance of many face recognition algorithms. Door access control systems control illumination and pose in order to overcome face recognition problems. While there have been significant improvements in the algorithms with increasing recognition accuracy, very little research has been conducted on implementing these in hardware devices. Most of the previous studies focused on implementing a simple principal component analysis in hardware with low recognition accuracy. In contrast, the use of a Gabor filter for feature extraction and the nearest neighbour method for classification were found to be better alternatives. Dramatic developments in field programmable gate arrays (FPGAs) have allowed designers to select various resources and functions to implement many complex designs. The aim of this paper is to present the feasibility of implementing Gabor filter and nearest neighbour face recognition algorithms in an FPGA device for face recognition. Our simulation using Xilinx FPGA platforms verified the feasibility of such a system with minimum hardware requirements.

Key words: Access control, face recognition, field programmable gate array.

1. Introduction

Face recognition has become an important research area because of its usefulness in numerous applications. Such a recognition system can be used to allow access to computers, to control entry into restricted areas and to search for a face in databases for identification. Many organisations such as the Roads and Maritime Services in Australia and the Australian Department of Immigration create large face image databases for face identification or verification purposes[1], [2]. The general idea of face recognition is to extract certain data from the region of interest in a human facial image and to compare them to stored data for identification. The feature extraction stage represents the backbone of face recognition systems because of the direct dependency of the accuracy of any face recognition system on the accuracy of the extracted facial features. The task of feature extraction is very difficult because of certain environmental issues. The following paragraphs outline these environmental problems which have the main influences on the accuracy of any face recognition system.

The ambient light or artificial illumination affects the accuracy of face recognition systems. This is because the basic idea of capturing an image depends on the reflection of the light off an object and the higher the amount of illumination, the higher the recognition accuracy.

Another difficulty which prevents face recognition (FR) systems from achieving good recognition

accuracy is the camera angle (pose). The closer the image pose is to the front view, the more accurate the recognition. For face recognition, changes in facial expression are also problematic because they alter details such as the distance between the eyebrows and the iris in case of anger or surprise or change the size of the mouth in the case of happiness. Simple non-permanent cosmetic alterations are also a common problem in obtaining good recognition accuracy. One example of such cosmetic alterations is make-up which tends to slightly modify the features. These alterations can interfere with contouring techniques used to perceive facial shape and alter the perceived nose size and shape or mouth size. Other colour enhancements and eye alterations can convey misinformation such as the location of eyebrows, eye contrast and cancelling the dark area under the eyes leading to potential change in the appearance of a person.

Although wearing eye-glasses is necessary for many human vision problems and the certain healthy people also wear them for cosmetic reasons but wearing glasses hides the eyes which contain the greatest amount of distinctive information. It also changes the holistic facial appearance of a person.

In order to overcome these problems, a considerable research has been undertaken to improve the face recognition algorithms. However, these algorithms still struggle to overcome problems of background, illumination and pose variations.

Other research has been focused on controlling these imaging environments by using a controlling system such as door access control systems. Door access control systems can simplify these problems by controlling many of such variations. However, the existing door access control systems are limited to implement a very basic face recognition approaches which is the Principle Component Analysis technique (PCA). In this study, we focus on studying the feasibility of implementing an alternative face recognition algorithm in an FPGA device. The rest of this article is organized as follows: Section 2 presents the related previous work. Section 3 introduces an FPGA device. Section 4 outlines the key points of the proposed face recognition system. Section 5 presents the feature extraction stage using a distributive arithmetic finite impulse response (FIR) filter. Section 6 presents the simulation design of the distributed arithmetic FIR filter. Section 7 presents the hardware implementation of the nearest neighbor classifier (NNC). Section 8 presents the results of the hardware simulations. Section 9 concludes the study and suggests future research.

2. Review of the Literature

Face recognition is very important in many applications such as security verification and people identification in cash machines and employee attendance systems. The existing face recognition designs suffer from many environmental problems such as illumination, pose and expression changes. In order to overcome these problems, some research has outlined the necessity for a pre-processing stage in order to make use of valid facial images which are unadulterated with the use of make-up, wigs, facial hair or glasses. The pre-processing stages of illumination normalization and histogram equalization techniques have been developed to enhance or retrieve the input image [3]-[7]. However, these techniques do not solve the problems of pose and expression changes. Other research has focused on improving the feature extraction or classification techniques. Techniques such as Principle Component Analysis (PCA) [8], [9], Independent Component Analysis (ICA) [10] and Linear Discriminative Analysis (LDA) [11], [12] are related to holistic facial appearance while others, such as the Gabor filter [13] and Local Feature Analysis (LFA) [14] are based on identifying individual features. These methods, however, require the use of much pre-processing of the input image in order to solve the problems associated with illumination, pose and expression changes. Using a door access control system, however, can produce more robust input data for face recognition. The typical door access control system consists of a camera, an illumination source, an electronic door lock and the system control which connects all components using a human-machine control interface. Door access

control systems work on controlling the distance between the camera and the person to control the background, and by fixing the lighting refresh rate and the camera angle (pose) and requiring the person of interest to pose for a frontal view with a neutral expression, as shown in Fig. 1. These properties of a door access control system result in high recognition accuracy. However, existing door access control systems are limited to the traditional Principle Component Analysis (PCA) feature extraction technique [15]. This if because of its simplicity and dimensionality reduction as it works on selecting a number of eigenvectors from the database as the image information space and the best match is found by projecting the eigenvectors of the input image into that space.

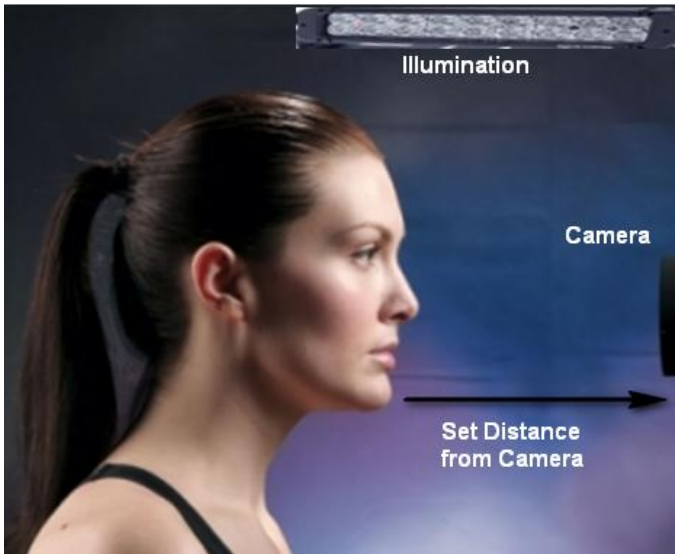

Fig. 1. Example of controlling the set distance, lighting, background and the pose of a facial image[16].

However, This naturally leads to missing certain information by selecting only part of the eigenvectors of the database images that result in mismatch [17]. In contrast, a face recognition system based on a hybrid feature extraction and nearest neighbor for classification was found to obtain higher recognition accuracy [17]. In [18], a hybrid feature extraction was designed based on a combination of local features extracted using a Gabor filter applied on three holistic regions: the eye, the nose and the mouth. These three regions are extracted and convolved with the Gabor filters and the maximum intensity of each Gabor representation of these three regions is computed to produce the required feature vector. This vector is passed through the classification stage using the nearest neighbor classifier based on the City Block distance metric. This system is found to be more accurate than a PCA-based algorithm for face recognition.

In addition to the selectivity of the face recognition algorithm, the hardware device is also important in improving the performance of a door access control system which is exploiting a sort of systems that need to be small in size, have lower power consumption, high performance and embedded architecture. Embedded system is one system that has computer hardware with software embedded in a device that is implemented for a particular purpose [17]. According to the number of hardware resources, the amount of power consumption and the number of programming tools, embedded systems can be classified as small scale, medium scale and large scale systems. The selection of each one of these types is related to the design requirements. For example, systems that require a large number of hardware resources usually use sophisticated embedded systems. Improvements on these systems allow designers to achieve complex design with highly economical processing and elevated performance [15]. There exist many types of sophisticated embedded systems such as complex programmable logical devices (CPLD), application specific integrated circuits (ASIC) and field programmable gate arrays (FPGA). FPGAs are found to be an

ideal platform for an embedded computer running a high-performance control system [17], [19].

3. Field Programmable Gate Array (FPGA)

The selection of an appropriate hardware device for the proposed door access control system is important in order to achieve higher recognition accuracy and high performance. FPGA is superior to the other hardware platforms in terms of its field reprogramming ability, logic flexibility and dynamic reconfiguration [17]. Many field programmable gate array devices (FPGA) have been developed to be used in a wide range of real-time applications. One of the most important of these is door access control systems based on face recognition. An FPGA can be defined as a programmable semiconductor device that surround a matrix of Configurable Logic Blocks (CLBs) and is connected via programmable interconnections. It consists of three components: logic blocks, I/O blocks and programmable routing [19]. The CLB of an FPGA has up to four slices which contain logic cells. These logic cells consist of look-up tables (LUT) for memory purposes, a register for holding internal data , clock-set and clock-enable for timing, a set and reset signal (S/R) for control and a multiply and accumulate unit (MAC) to do all mathematical operations. The CLB of an FPGA device can be configured so that its internal logical components serve certain tasks. For example the flip-flops can be used to do a parallel data storage and the LUT can be used to store the results of the required design during the internal process. This enhances the FPGA device's abilities in a range of features to support various complex designs. In general, the main features of an FPGA device for any design are: memory for storing data, control units (microcontrollers), mathematical and logical functions (adders/subtracters, multipliers, MAC and DSP48) and input/output units. FPGAs offer more logical flexibility, are more sophisticated, and provide more opportunities for dynamic reconfiguration of the system. In particular, they have some powerful help tools which can simplify the design process even for people who do not have much experience in hardware implementation. The Xilinx Company, for instance, provides printout documents containing the procedure for operating a Xilinx system generator, an ISE project navigator and the compilers and other helpful design tools such as a product data sheet and a user guide [20].

4. Face Recognition System

The hardware implementation of face recognition algorithms is important for a wide variety of real- time applications, particularly in door access control systems. According to the findings of our previous research [17], FPGA devices are very suitable for a number of complex tasks, and in particular, for face-recognition algorithm implementation. Analyzing the performance results of many face recognition algorithms and their architecture in [17], shows that a hybrid technique that combines both the holistic approach as well as local feature analysis will improve overall recognition accuracy. Gabor filters stand out as a technique which is unique yet robust against subtle changes of an individual over the years, one which can be used as a valid discriminant. Gabor representation of any input image has 40 different filters with different orientation and scales which have the benefit of allow for finer discrimination between images. Another important advantage is that it can be implemented on an FPGA as opposed to a desktop or a network computer. Such situations demand simplicity as well as reliability in producing image comparisons for face recognition. The key points of the proposed face-recognition system based on hybrid feature extraction (the local Gabor filter and the holistic three segment facial regions) and the nearest neighbor technique for classification can be described as follows:

4.1. Three Regions Extraction

The procedure of extracting the three regions of interest is important because these regions have the most discriminative data for any facial image. In this step, it is supposed that, the size of the input image is

rescaled to (112×92 pixels) in addition to the gray scale transformation. This is important as different images have varying image sizes especially when using different image databases for testing purposes. The process of region extraction in MATLAB is performed using the script shown in Fig. 2.

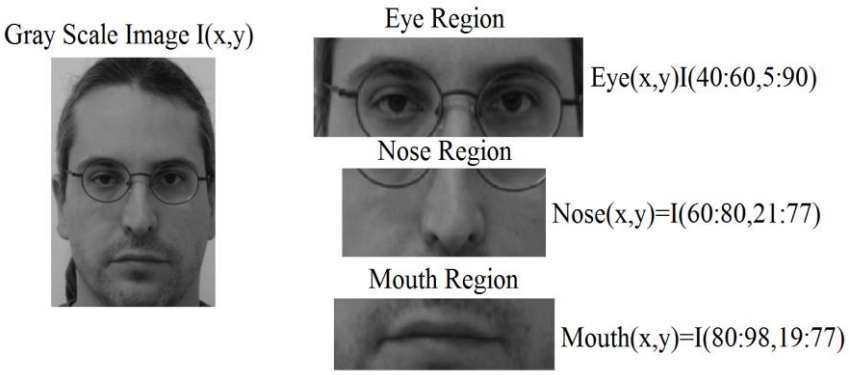

Fig. 2. Three region extraction

where I is the input gray scale resized image and the Eye(x, y), Nose(x, y) and Mouth(x, y) are the eye, nose and mouth regions respectively.

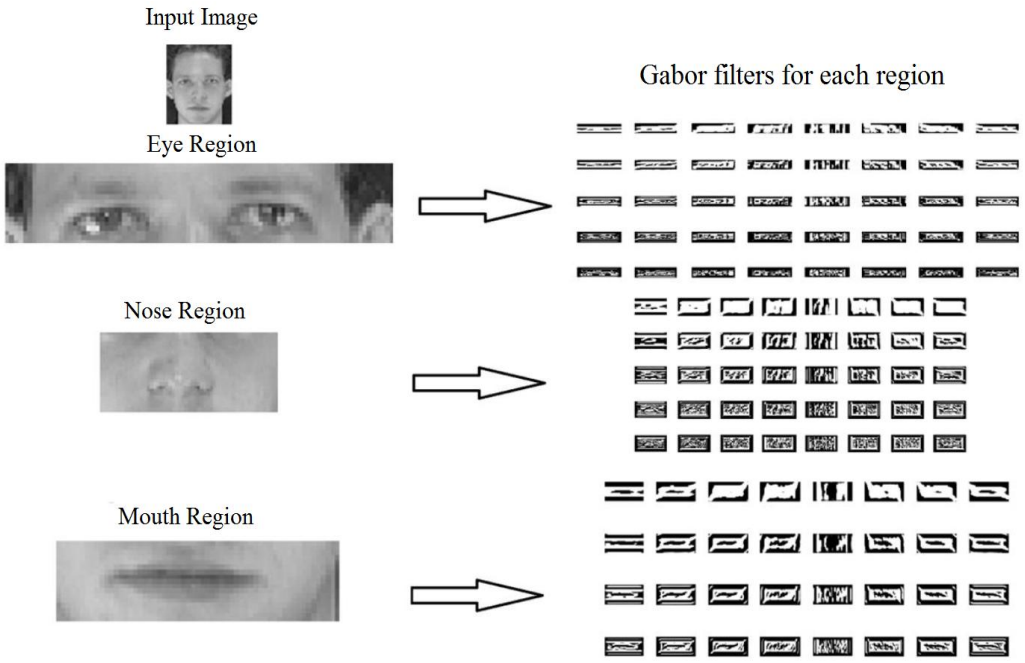

Fig. 3. The feature extraction stage of the proposed face recognition system.

4.2. Gabor Transformation

Each extracted region is passed through a Gabor filter to produce 40 hybrid representations of the input image as shown in Fig. 3. These 40 representations are reduced to 40 values containing only the maximum intensity. Then the resulting 40 values represent the feature vector of the input region. The nearest neighbor technique based on the City Block distance metric is then used to find the best match for the resulting vector among the stored vectors in the database. In order to study the feasibility of implementing these steps in an FPGA device, it is assumed that the input image has already been transformed into gray scale and three regions have been extracted. This enables us to pay more attention to the hardware implementation of the Gabor filter and the nearest neighbor techniques.

5. Feature Extraction by the Gabor Filter Using a Distributive Arithmetic FIR Filter

Face representation using Gabor filters has been used in various pattern recognition applications. The Gabor filter is an important local feature extraction technique as it provides robustness against varying brightness and contrast in the image [21]. The selection of the filter parameters is very important in designing a Gabor filter for face recognition. Gabor filters with multi-orientations and scales are created to obtain the required features from a given image. The common Gabor filters for feature extraction have 5 scales and 8 orientations, i.e., u=0, 1... p–1 and v=0, 1... r–1, where p=5 and r=8. Another representation of the Gabor filter is shown in Eq. 1. This representation has been proven by many studies to achieve an optimal resolution in the spatial and frequency domains

$$GK(n,m,s,o)=\frac{1}{\delta^2}k^2*\beta*(\omega-\exp[\frac{-\delta^2}{2}]) \tag{1}$$

$$\beta=\exp[\frac{-(k/\delta^2)^2*(n^2+m^2)}{2\delta^2}] \tag{2}$$

$$\omega=\exp\left[-k^2*(n,m)\right] \tag{3}$$

$$k=\left|\frac{k_{\max}*e^{\frac{j\pi s}{8}}}{f^2}\right| \tag{4}$$

where the parameters (n, m) are the kernel window dimensions $s\in\{0,1,2,3,4\}$ and $o\in\{0,1,2,3,4,5,6,7\}$ are the scales and the orientations of the Gabor kernel, ($k_{\max}$) is the maximum frequency, f is spatial frequency between the frequency domain kernels and δ is the standard deviation of the Gaussian in the kernel window. In this study these parameter values are chosen to be: $k_{\max}=\pi/2$, $f=\sqrt{2}$, $\delta=\pi$. The core problem of Gabor filter hardware implementation is that it requires many hardware resources to implement the functions of sine, cosine and calculating powers of complex exponentials. This problem becomes more complex in extracting facial features with large dimensionality as the input image must be convolved with 40 Gabor filters with different scales and orientations. Transforming a Gabor filter into a matrix with fixed coefficients can tackle this difficult problem using MATLAB. The representation of the Gabor coefficient requires 64-bit signed double floating points in MATLAB. Based on Eq. 5, the required memory size (S) for the Gabor filter coefficients is 327.68kB.

$$S=n.t.x \tag{5}$$

where n=32×32 bit is the image dimensions, t=64 bit is the required number of bits to manipulate a signed double floating points value and x=40 is the number of Gabor filters.

The next step is to convolve these 40 Gabor filters with the input image. The convolution is the sum of multiplying each kernel value with the pixel value underneath it. This operation has to be repeated for the entire input image after shifting the Gabor kernel over the image pixels to find the corresponding convolution values. This means that the convolution computation using the traditional addition and multiplication is quite complex. FPGA can be used to implement operations in parallel and hence used to implement large filter banks with minimum delays. The FIR filter is one of the most powerful FPGA applications that is used for convolution operations.

Gabor magnitude responses for the entire filter bank of the 40 Gabor filters are commonly computed first using a convolution operation of an FIR filter. An FIR filter hardware implementation was designed using a Xilinx Virtex-4 FPGA kit in [22] and using Xilinx Virtex-2 devices in [23] with the following equation:

$$f[n] = \sum_{k=0}^{N-1} h[k]x[n-k] \tag{6}$$

where $f[n]$ is the filter output, $x[n\text{-}k]$ is the input data and h[k] is the filter coefficients.

The hardware implementation of FIR filter design using Eq. (6) was found to be highly computationally expensive. In contrast, distributed arithmetic presents a better solution for an FIR filter implementation in an FPGA. This is because of its high flexibility which permits serial to full-parallel arrangements. In order to implement the required convolution operations, a distributed arithmetic FIR filter is used. The Gabor filter coefficients are stored in the FIR filters and the 40 FIR filters are executed in parallel.

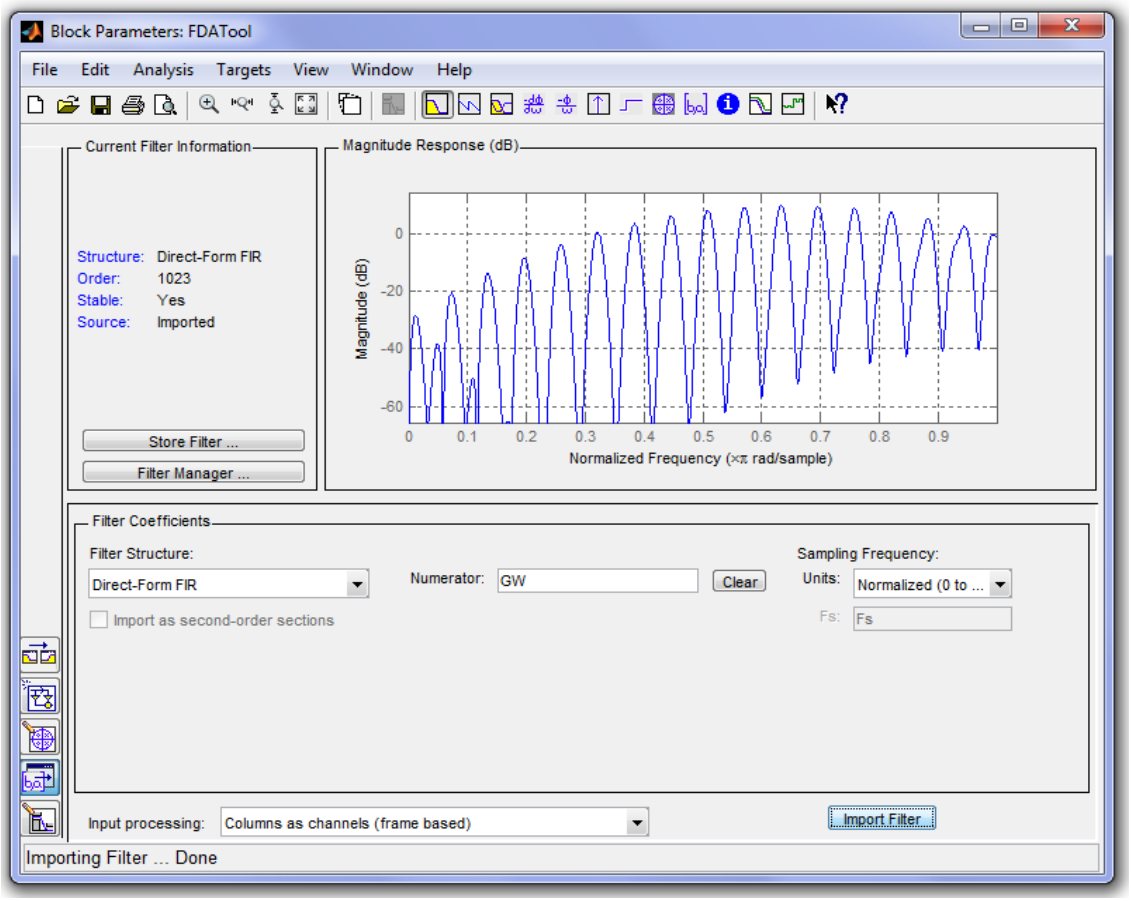

Fig. 4. FDATool Block parameter.

6. Distributed Arithmetic FIR Filter Simulation Design

In order to describe the feasibility of designing a distributed arithmetic FIR filter, the Xilinx block set and system generator tools are used. The Xilinx block set is compatible with the MATLAB simulink and this allows designers to select the appropriate block for the design. In this study, a FIR.5.0 filter is exploited. The FIR.5.0 block is a simulation block provided with the Xilinx block set tools. FIR.5.0 can be used to simulate a Distributed Arithmetic FIR filter. Such a block is used in this research to develop the simulation of the distribution arithmetic FIR filter in order to obtain the convolution between the input image and the Gabor filter coefficients. The simulation design of this filter consists of an input unit, an output unit and the FIR.5.0 blocks, as shown in Fig. 5. The input data for this simulation design is one of the three region images which are already loaded onto the MATLAB work space and stored as matrices. This data is entered into the simulation using gate-in block which makes the input data compatible with the Xilinx environment. A FIR.5.0 block is used in this simulation to obtain an FIR filter. This block allows the structure of the FIR filter

to be selected. The coefficients of one Gabor filter (1 from 40 Gabor filters) are loaded onto the FIR.5.0 block using an FDA tool. This tool allows uploading the coefficient vector from the work space by specifying the filter structure as direct FIR form and the vector name in the FDA tool block parameter as shown in Fig. 4.

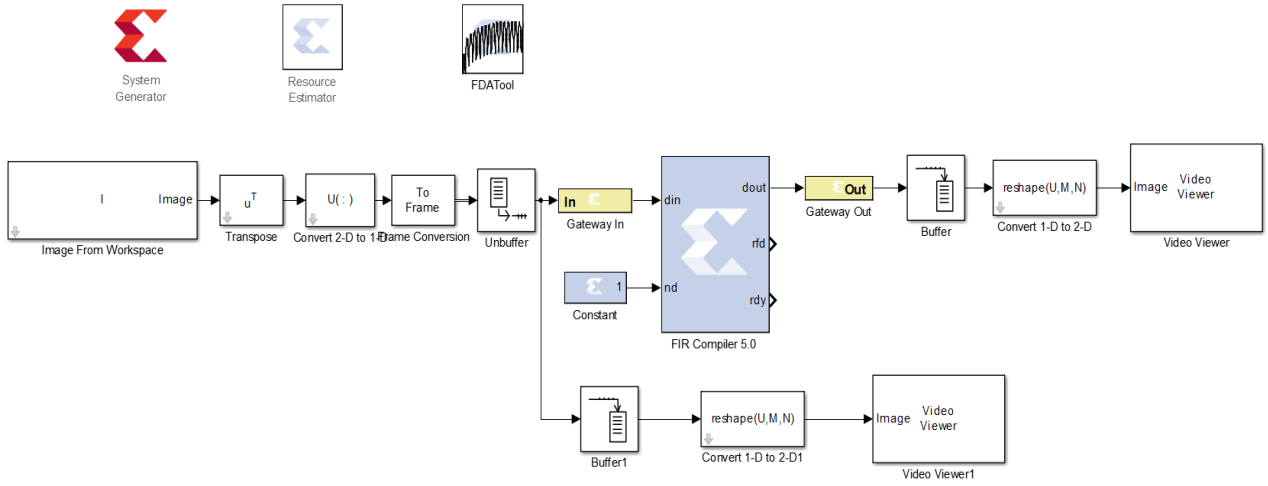

Fig. 5. The simulation design of an FIR filter.

After running the simulation design (Fig. 5), the system will compute the required FIR filtering (convolution) between one set of Gabor filter coefficients which are loaded to the FIR.5.0 by the FDA tool and the input image. The output of the system represents the Gabor features of the input image. Since the feature extraction stage in the proposed face recognition system consists of 40 Gabor filters, 40 FIR filters (40 paths) are connected in parallel to compute 40 Gabor representations of an input image, as shown in Fig. 5.

The resulting vector from each FIR filter (each path) has the same size as the input image (the input region). This will produce a very high dimension feature vector. To overcome this problem, the maximum intensity of each Gabor representation is computed to produce one value only. The simulation design in Fig. 6 is run using an M-code block provided with a Xilinx block set. This design is useful for doing comparison operations (maximum computations). It can be used to implement the required comparator operation on the output of each FIR filter resulting in 40 values which represent the facial feature vectors as shown in Fig. 7, where $V \in \{v_1, v_2, v_3, ..., v_{40}\}$ is the output vector which consists of the 40 maximum intensities of the 40 Gabor representations of the input image.

7. Nearest Neighbor Classifier Hardware Implementation

The resulting feature vector of the FIR (Gabor) filters, which are the facial feature vectors, must be classified according to the nearest neighbor technique to find the best match using the City Block distance metric. The required number of neighbors in this research is one (K=1) because each filter path will produce one value. The city block distance is given by:

$$dc(x,y) = \sum_{i=1}^{i=N} |x_i - y_i| \tag{7}$$

where $x \in x_1, x_2, x_3, x_4 ....., x_f$ is the testing vector and $y = y_1, y_2, y_3, ...y_n$ are the training vectors where n is the number of the stored features vectors in the database and f is the length of the input testing vector. The City Block distance equation can be written as:

$$dc(x,y1) = (x_1 - y_{11}) + (x_2 - y_{12}) + (x_3 - y_{13}) + (x_4 - y_{14}) + ...(x_f - y_{1f})\ dc(x,y2) = (x_1 - y_{21}) + (x_2 - y_{22}) + (x_3 - y_{23}) + (x_4 - y_{24}) + ...(x_f - y_{2f})$$
$$dc(x,yn) = (x_1 - y_{n1}) + (x_2 - y_{n2}) + (x_3 - y_{n3}) + (x_4 - y_{n4}) + ...(x_f - y_{nf}) \tag{8}$$

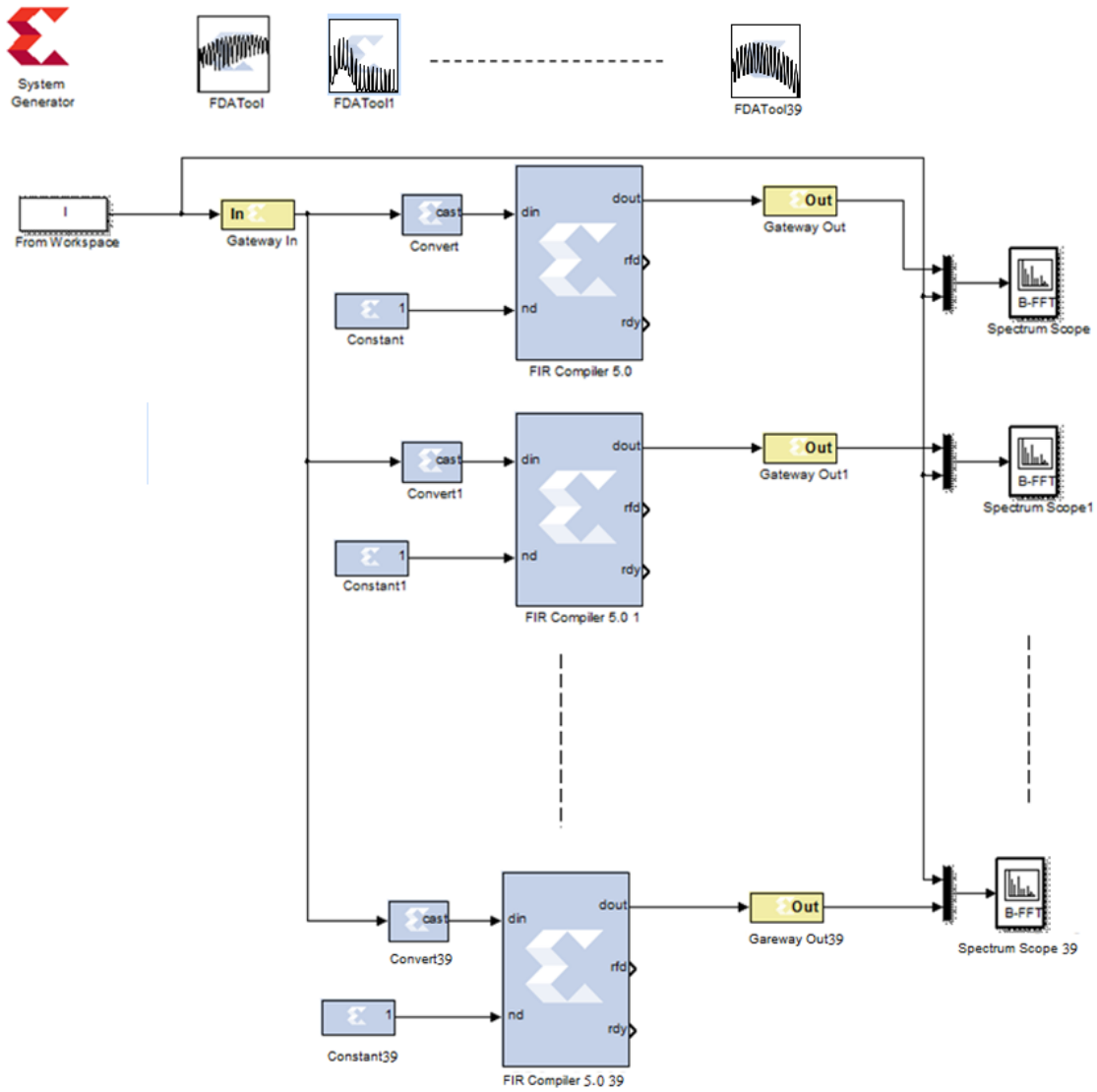

Fig. 6. The simulation design of 40 FIR filters connected in parallel.

The City Block metric is used to find the minimum distance in nearest neighbor classification for matching vectors. The hardware implementation of the required addition and subtraction steps can be obtained using an FPGA device exploiting its parallelism characteristic. Each value of the unknown vector is subtracted from the corresponding value of the f training vector and the results are added to each other producing one distance value. This step can be achieved using Xilinx system generator simulation. The simulation of one of the required paths of computing the City Block distance is shown in Fig. 8. The input for this simulation is one training vector and the test vector. The parallelism characteristic of FPGA devices can be used to calculate the City Block distance by assigning a similar simulation design to each training vector as shown in Fig. 9. The vector $d \in \{d_1, d_2, ..., d_n\}$ consists of the City Block distances between each feature vector in the training set and the feature vector of the input image, where n is the number of the training feature vectors. The size of the database varies between one system and another depending on the number of images that are used in that database. Supposing that the number of images is 100 (x=100), the value of the required memory to store the feature vectors of these 100 images using Eq. 5 is equal to 32kB as the image size here is n=40, which is the number of the maximum intensities of the resulting convolution values between each image and 40 Gabor filters. The next step is to find the minimum value of the resulting City Block distances. This is done using the following simulation design, as shown in Fig. 10. In this

simulation design, an M-code block from the Xilinx block set is also used to fetch the required MATLAB function. This function computes the minimum distance from the input distance vector in order to determine the nearest neighbor which is the best match for the test candidate.

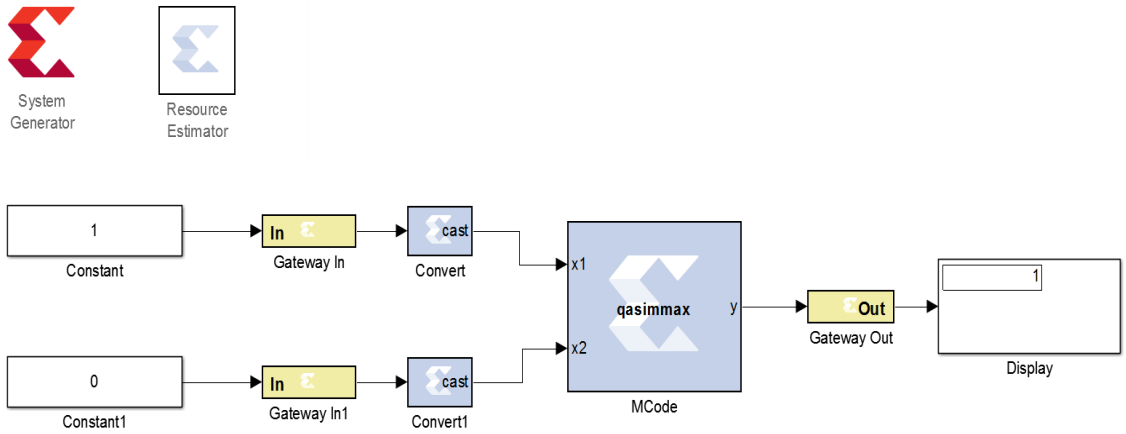

Fig. 7. The simulation design of the maximum comparator.

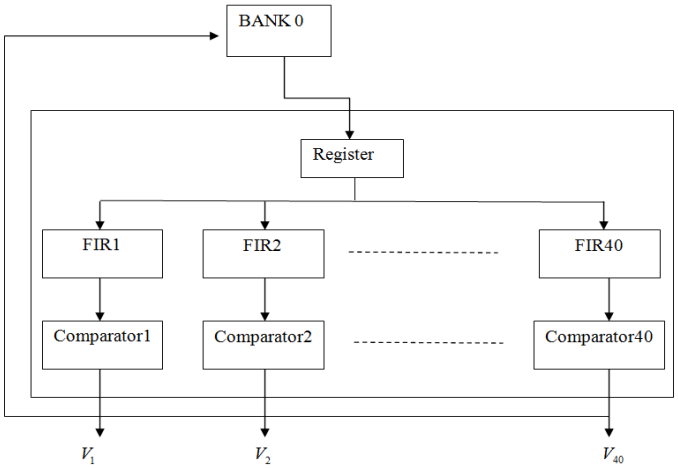

Fig. 8. Forty FIR filters connected in parallel to perform a convolution of Gabor filters.

8. Hardware Simulations Results

In this study, the simulation design of the proposed face recognition system is implemented using the Xilinx platform. The reason for selecting this platform is its simplicity and efficiency in doing the whole design steps using the MATLAB simulink tool box. The design of the system passes through four simulation models: convolution computation, maximum intensity calculation, City Block calculation and the minimum calculation. In the first model, the simulation design of the distributed FIR filter is built using the Xilinx system generator blockset for simulink. In this simulation, a resources estimator is used to determine the required hardware resources for implementing such a filter in an FPGA device. The hardware resources of the simulation are 263 slices, 938 flip flops and 900 LUTs. The ISE project navigator is used then to complete the required implementation of this simulation. The results in Table 1 are for one path (one FIR filter) and the total number of paths is 40. This is necessary for performing the required convolution processes between the input image and the 40 Gabor filters. Therefore, the total hardware resources can be estimated by multiplying each component by 40. In the second model, the simulation design is performed using a MATLAB function which computes the maximum intensity of the FIR filter output sequence. The MATLAB function is fetched in the simulation model by the M-block from Xilinx block set. This design is

applied on the output of each FIR filter to derive a feature vector of forty values. The hardware resources and the utilization of one simulation of the second model are presented in Table 1.

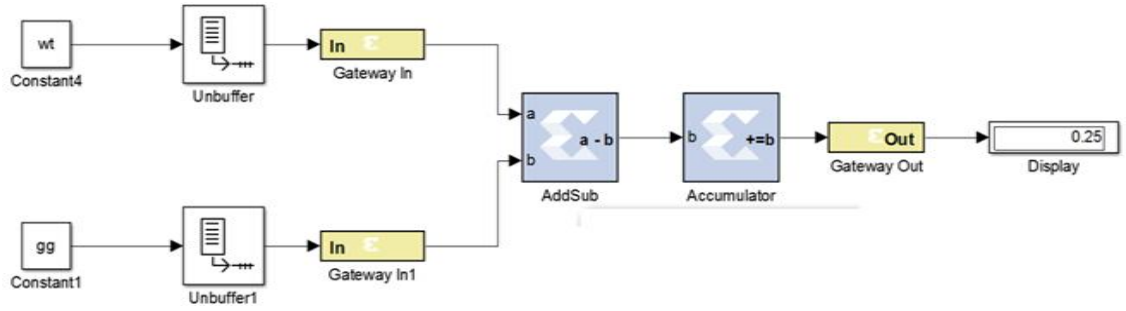

Fig. 9. The simulation design of one path of the city block distances.

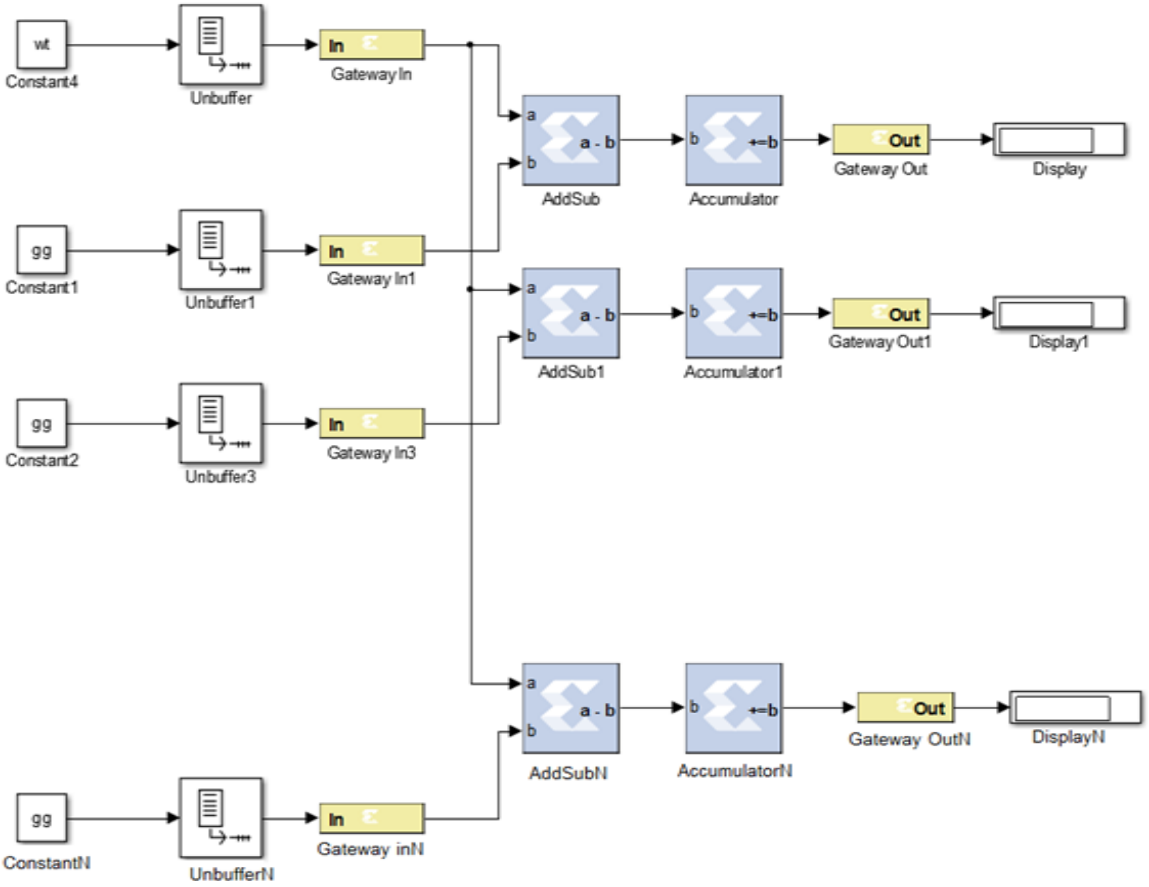

Fig. 10. The simulation design of commuting the City Block values between the testing vector and N training paths.

The resulting vector of the maximum intensity of the 40 FIR filters represents the feature vector of the input image. This vector then enters the classification stage to find the best match for the input image from existing vectors in a database. The third simulation is designed to achieve the nearest neighbour by computing the City Block distance between the testing feature vector and one of the trained vectors. The simulation design of one path of the required City Block distance requires 36 slices, 17 flip flops and 68 LUTs. The total number of the required paths (the third simulation design) in this stage depends on the number of stored vectors in the database. This is because the nearest neighbor technique works based on finding the nearest City Block distance between the input vector and the stored vectors in the database. Finally, a simulation is designed using a MATLAB function to find the minimum City Block distance of the

resulting vector. The resource utilization of this simulation design is shown in Table 2.

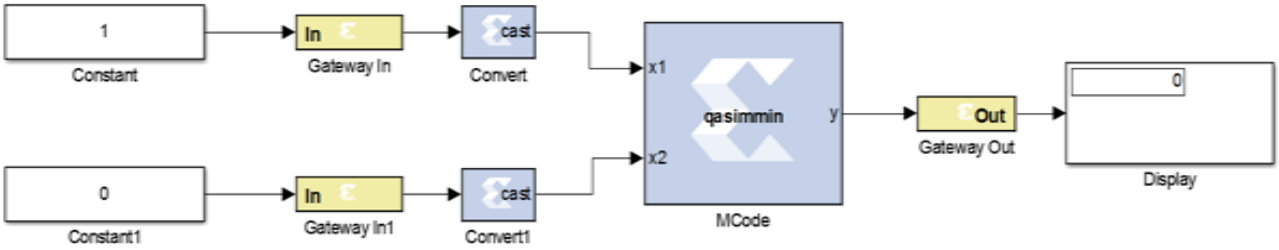

Fig. 11. A comparator simulation design.

Table 1. The Utilization of the Comparator Design Using Vertix5-FPGA

Slice Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	16	203,800	1%
Number used as logic	16	203,800	1%
Number of occupied Slices	8	50,950	1%
Number with an unused Flip Flop	16	16	100%
Number of bonded IOBs	48	400	12%

Table 2. The Resources Utilization of the Comparator Simulation Design Using Vertix5-FPGA

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1	407,600	0%
Number of Slice LUTs	31	203,800	1%
Number used as logic	16	203,800	1%
Number of occupied Slices	8	50,950	1%
Number of bonded IOBs	49	400	12%

The best match is then the facial image corresponding to the minimum City Block distance. All of the above simulations confirm the ability of the Xilinx system generator and ISE project navigator to complete the required steps of the hardware implementation. This is because the Xilinx platform has a one-to-one correspondence to the hardware implementation. The results of these simulations confirm the feasibility of implementing the proposed face recognition system in an FPGA device in terms of hardware resources and data storage ability.

In comparison to the hardware implementation of Gabor filter in [24] it can be stated that the hardware device in [24] was not reprogrammable and a full utilization was required for achieving the face recognition system. This implementation utilizes a 100% of the hardware device resources which is detrimental to its longevity. In contrast in our design, lower than 10% of the full hardware resources were utilized and the FPGA device is a reprogrammable device which allows further system upgrades for a real door access control system. However, in terms of real-time applications such as door access control systems, the first simulation model, which is the FIR filter, is found to be time consuming as the filter evaluates point by point operations to calculate the required convolutions between the input image and the Gabor filter coefficients. To overcome this problem, the image divider stage must be used to divide the input image into sub-images and the number of these sub-images depends on the available hardware resources in the FPGA device. The FIR filter is then applied on these sub-images in parallel, which can significantly speed up the processing time.

9. Conclusion

The feasibility of implementing a face recognition system in an FPGA device based on Gabor filters for

feature extraction and the nearest neighbor technique for classification have been investigated. The resulting face-recognition design can be used in a door access control system. In this study, a Xilinx system generator and an ISE project navigator were used to design the required simulation and to produce the hardware implementation reports. The distributive arithmetic FIR filter was used in the feature extraction stage to compute the convolution operation between the input image (three region images) and each of the 40 Gabor matrices (filter coefficients). In the classification stage, the simulation design of the nearest neighbor technique was attempted based on the City Block distance. The results obtained using the simulations confirmed the feasibility of implementing a face recognition system on an FPGA device with minimum hardware. The process of converting the MATLAB code of Gabor filters into 40 fixed matrices can reduce the hardware resources to only one 8.192KB RAM for each filter. Since the Xilinx simulation provides a one-to-one realistic correspondence between simulation and real implementation, this validates our research and will soon be implemented on a Xilinx FPGA device. This research will serve as the foundation for future studies and further improvement in both system reliability and face recognition accuracy, leading to the design of a door access control system based on face recognition. The required time processing and the critical path delay of the FPGA device will be discussed in future research when the hardware implementation and camera modeling are completed. Future work will focus on reducing the processing time delay by either reducing the number of the selected Gabor filter orientations and scales or by dividing the resulting Gabor matrix into sub-matrices and applying these sub-matrices to the system in parallel at the same time by increasing the hardware utilization of the FPGA device.

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References

[1] RMS. (2014). Facial Recognition system in the roads and maritime services. *Transportation*.

[2] DIAC. (2013). Department of Immigration and Border Protection, Annual Report for 2012-2013.

[3] Cao, X. S., Yu, Wang, W., L., *et al.* (2012). Illumination invariant extraction for face recognition using neighboring wavelet coefficients. *Pattern Recognition, 45,* pp. 1299-1305.

[4] Hu, H. (2011). Variable lighting face recognition using discrete wavelet transform. *Pattern Recognition Letters, 32*, pp. 1526-1534.

[5] Abbas, A. K., Abdel-Hay, M. I., & Fahmy, H. M. S. (2008). Expression and illumination invariant preprocessing technique for Face Recognition. *Proceedings of International Conference on Computer Engineering & Systems* (pp. 59-64).

[6] Hardeep, K., & Amandeep K. (2013). Illumination invariant face recognition. *International Journal of Computer Applications, 64*.

[7] Bairagi, B. K. D., Chatterjee, S. C., & Tudu, A. B. (2012). Expressions invariant face recognition using SURF and Gabor features. *Proceedings of Third International Conference on Emerging Applications of Information Technology* (pp. 170-173).

[8] Saurabh, P. B., & Chaudhari D. S. (2012). Principal component analysis for face recognition. *International Journal of Engineering and Advanced Technology, 1,* pp. 91-94.

[9] Prakash S. M., & Kalpna, C. J. (2011). Face Recognition Using PCA. *International Journal of Artificial Intelligence & Knowledge Discovery, 1,* 25-28.

[10] Shen, M. C., Li, P., *et al.* (2012). "Independent component analysis for face recognition based on two dimension symmetrical image matrix," *Proceedings of 24th Chinese Conference on Control and Decision*

(pp. 4145-4149).
[11] Bansal, A. M., & Arora, S. K. (2012). Face Recognition Using PCA and LDA Algorithm. *Proceedings of Second International Conference on Advanced Computing & Communication Technologies* (pp. 251-254).
[12] Razzak, M. I. K., Alghathbar, M. K., & Yousaf, R. K. (2011). Face recognition using layered linear discriminant analysis and small subspace. *Proceedings of IEEE 10th International Conference on,Computer and Information Technology* (pp. 1407-1412).
[13] Muhammad, S. A., Khalid, M., Raza, & S. M. (2011). Face recognition using gabor filters. *Journal of Applied Computer Science & Mathematics, 5*, pp. 53-57.
[14] Ehsan F.-E. J., Zelek, S., & John, T. (2007). Robust face recognition through local graph matching. *Journal of Multimedia, 2,* 31-37.
[15] Ibrahim, R., & Zin, Z. M. (2011). Study of automated face recognition system for office door access control application. *IEEE 3rd International Conference on Communication Software and Networks* (pp. 132-136).
[16] Sint, S. (2011). *Posing the Face*. From http://stevesint.com/blog/
[17] Al-Shebani, Q., *et al.* (2013). Embedded door access control systems based on face recognition: A survey. *Proceedings of 7th International Conference on Signal Processing and Communication Systems* (pp. 1-7).
[18] Alshebani, Q., *et al.* (2014). A hybrid feature extraction technique for face recognition. *International Proceedings of Computer Science and Information Technology*, 166-170.
[19] MacLean, W. J. (2005). An evaluation of the suitability of fpgas for embedded vision systems. *Proceedings of IEEE Computer Society Conference on Computer Vision and Pattern Recognition* (pp. 131-131).
[20] Xilinx. (August 2013). *UG479 7 Series DSP48E1 Slice, User Guide.* From http://www.xilinx.com
[21] Ki-Chung,C. S.-C., & Kee, S.-R. K. (1999). Face recognition using principal component analysis of Gabor filter responses. *Proceedings of International Workshop on Recognition, Analysis, and Tracking of Faces and Gestures in Real-Time Systems* (pp. 53-57).
[22] Anurag, A., *et al.*, (2013). FIR filter designing using Xilinx system generator. *International Journal of Computer Applications*, 68.
[23] Mirzaei, S., *et al.*, (2006). FPGA implementation of high speed FIR filters using add and shift method. *Proceedings of International Conference on Computer Design* (pp. 308-313).
[24] Shimin, W., & Jihua, Y., Research and implementation of embedded face recognition system based on ARM9. *Proceedings of International Conference on Mechanic Automation and Control Engineering* (pp. 2618-2621).

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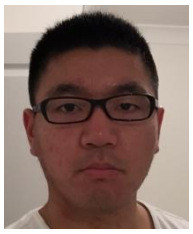

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