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Abstract

Enhanced performance was observed for dye-sensitized solar cells (DSSCs) utilizing counter electrodes based on Pt electrodeposits compared to counter electrodes based on sputtered Pt. Scanning electron microscopy of Pt electrodeposits revealed that the use of an initial cathodic overpotential pulse followed by steady electrodeposition at a mild cathodic potential yielded ~40nm particles, compared to ~600nm particles when no such pulse was used. Cyclic voltammetry and electrochemical impedance spectroscopy (EIS) of electrode materials suggested that Pt electrodeposits would give enhanced performance as DSSC counter electrodes compared to sputtered Pt, and this was confirmed by device testing. EIS characterization of DSSCs under illumination revealed that Pt electrodeposit counter electrodes were found to be more catalytically stable compared to sputtered Pt. The best counter electrode was based on Pt electrodeposited using an initial cathodic overpotential pulse and demonstrated charge-transfer resistance [RCT(Pt)] values of 0.6 and 0.7Ωcm² within a symmetrical Pt/I⁻³/I⁻/Pt cell and within a DSSC, respectively.

Keywords

Enhanced, performance, dye, sensitized, solar, cells, utilizing, platinum, electrodeposit, counter, electrodes

Disciplines

Life Sciences | Physical Sciences and Mathematics | Social and Behavioral Sciences

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Enhanced Performance of Dye Sensitized Solar Cells Utilizing Platinum Electrodeposit Counter Electrodes

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Enhanced performance was observed for dye-sensitized solar cells (DSSCs) utilizing counter electrodes based on Pt electrodeposits compared to counter electrodes based on sputtered Pt. Scanning electron microscopy of Pt electrodeposits revealed that the use of an initial cathodic overpotential pulse followed by steady electrodeposition at a mild cathodic potential yielded ~40 nm particles, compared to ~600 nm particles when no such pulse was used. Cyclic voltammetry and electrochemical impedance spectroscopy (EIS) of electrode materials suggested that Pt electrodeposits would give enhanced performance as DSSC counter electrodes compared to sputtered Pt, and this was confirmed by device testing. EIS characterization of DSSCs under illumination revealed that Pt electrodeposit counter electrodes were found to be more catalytically stable compared to sputtered Pt. The best counter electrode was based on Pt electrodeposited using an initial cathodic overpotential pulse and demonstrated charge-transfer resistance [$R_{CT}(Pt)$] values of 0.6 and 0.7 $\Omega \text{ cm}^2$ within a symmetrical Pt/I₃⁻/I⁻/Pt cell and within a DSSC, respectively.
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Dye-sensitized solar cells (DSSCs) based on nanoporous TiO₂ thin films have been intensively investigated ever since the report of the first such devices.¹ The operation of DSSCs involves electron injection into TiO₂ from a bound photoexcited dye, regeneration of the resulting photo-oxidized dye through the donation of an electron from I⁻, and diffusion of the resultant I₃⁻ species through the electrolyte to the counter electrode where I⁻ is regenerated. While development of the dye-sensitized nanoporous TiO₂ photoanode is of primary importance for raising device efficiencies, development of the counter electrode is significant in terms of minimizing device internal resistance and lowering the cost of device production.

The best performing material for DSSC counter electrodes is Pt, which shows excellent catalytic activity for the reduction of I₃⁻ at film thicknesses of only a few nanometers. Alternative materials include various forms of carbon, including graphite,^{2,3} carbon black,²⁻⁴ carbon powder,⁵ and carbon nanotubes,⁶ and the conducting polymer poly(3,4-ethylenedioxythiophene).⁷⁻¹⁰ However, the catalytic activity of such alternative materials only approaches that of Pt when films with thicknesses on the order of micrometers are used. The best DSSC counter electrode is thermal Pt on fluorine-doped tin oxide (FTO) glass, prepared by the decomposition of H₂PtCl₆ to Pt at temperatures approaching 400°C, and demonstrating $R_{CT}(Pt)$ values as low as 0.07 $\Omega \text{ cm}^2$.¹¹ However, this method is not suitable for flexible plastic substrates, and the high temperature would add to DSSC production costs. Alternative methods of Pt deposition that avoid the high temperatures of the thermal method include sputtering,^{6,7,9,12-14} chemical reduction,^{15,16} and electrodeposition.^{6,11,17-19}

The majority of previous studies considering Pt electrodeposition for DSSC counter electrodes have only used this technique as an aside to other focuses, with some even raising questions regarding the stability of Pt electrodeposits within DSSCs.^{6,11} To our knowledge, only one previous study has set out with the aim of optimizing the Pt electrodeposition process for DSSC counter electrodes. Kim et al.¹⁸ compared direct and pulsed current Pt electrodeposition for glass and plastic-based DSSCs. The authors used cyclic voltammetry (CV) and electrochemical impedance spectroscopy (EIS) to show that the pulsed current technique gave catalytically superior Pt compared to the direct current technique, achieved through control of the morphology. Considerably higher DSSC efficiencies were achieved when using counter electrodes prepared via pulsed current compared to direct current. We have now built upon the studies by Kim et al. to determine charge-transfer resistance [$R_{CT}(Pt)$] values corrected

for area, a comparison of Pt deposited by other techniques (e.g., sputtering), and measurement of the $R_{CT}(Pt)$ associated with counter electrodes incorporated within DSSCs under operation.

The following considers DSSC counter electrodes based on Pt electrodeposited by constant potential (CE) with and without the use of an initial cathodic overpotential pulse, and comparison with sputtered Pt. Electrode materials were characterized by scanning electron microscopy (SEM) and CV, and were also fabricated into symmetrical Pt/I₃⁻/I⁻/Pt cells and characterized periodically over time using EIS. DSSCs utilizing such electrode materials as counter electrodes were fabricated and their current-voltage (*I-V*) and EIS characteristics also periodically measured over time. The stability of DSSC counter electrodes based on electrodeposited and sputtered Pt is considered within symmetrical Pt/I₃⁻/I⁻/Pt cells and within DSSCs.

Experimental

Counter electrode preparation.— Pt was electrodeposited from an aqueous solution containing 10 mM H₂PtCl₆ and 0.5 M Na₂SO₄ in a three-electrode cell with indium tin oxide (ITO) glass (Delta Technologies, 10 Ω/\square) working electrode, Pt mesh auxiliary electrode, and Ag/AgCl reference electrode.

Two sets of optimized conditions were used to electrodeposit Pt onto ITO glass. The first involved application of a CE of -0.4 V up to a charge density of 100 mC cm⁻², hereafter referred to as "CE." The CE of -0.4 V represented a limit beyond which H₂(g) evolution interfered with the electrodeposition of Pt, resulting in nonuniform coatings. The second involved application of an initial -0.6 V pulse for 2 s followed by CE electrodeposition at -0.4 V up to a charge density of 100 mC cm⁻², hereafter referred to as "p + CE." The aim of the pulse was to create nucleation sites across the ITO glass substrate for subsequent Pt electrodeposition. Assuming complete reduction of H₂PtCl₆ to Pt⁰ on the ITO glass working electrode surface and 100% electrochemical efficiency, the charge density of 100 mC cm⁻² used to prepare Pt electrodeposits would have corresponded to a Pt loading of ~50 $\mu\text{g cm}^{-2}$, although the actual loading (not measured) was likely less than this.

For comparison, counter electrodes were also prepared by sputter coating of Pt onto the same ITO glass substrate as above. A Dynavac Magnetron SC100MS sputter coater was used to sputter an 8 nm coating using 50 mA sputter current, 2×10^{-3} mbar Ar pressure, and 40 s sputtering time. Counter electrodes prepared by sputter coating are hereafter referred to as "sputtered." The 8 nm coating thickness corresponded to a Pt loading of ~20 $\mu\text{g cm}^{-2}$.

Counter electrode characterization.— SEMs of electrodeposited and sputtered Pt coatings on ITO glass were recorded on a Hitachi

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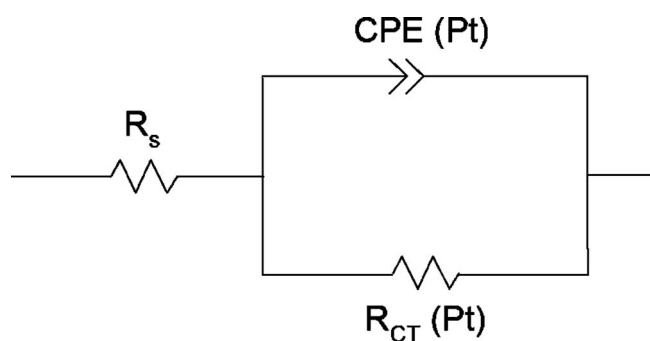


Figure 1. Equivalent circuit used to fit the highest frequency arc observed in Nyquist plots of symmetrical Pt/I₃⁻/I⁻/Pt cells and DSSCs in order to obtain $R_{CT}(Pt)$.

S4500 field emission scanning electron microscope. CVs of candidate DSSC counter electrodes were carried out in a three-electrode cell with Pt-coated ITO glass working electrode, Pt mesh auxiliary electrode, and Ag/Ag⁺ reference electrode. The electrolyte was made up of 1 mM I₂, 20 mM tetrapropylammonium iodide (TPAI), and 0.2 M tetrabutylammonium perchlorate (TBAP) in acetonitrile (ACN).

Sealed symmetrical Pt/I₃⁻/I⁻/Pt cells consisting of identical Pt-coated ITO glass electrodes were fabricated using a 60 μm hot-melt spacer and a liquid electrolyte containing 0.6 M 2,3-dimethyl-1-propylimidazolium iodide (DMPII) and 0.03 M I₂ in 85:15 ACN:valeronitrile (VN). The liquid electrolyte was introduced through a small predrilled hole in one of the electrodes by vacuum backfill. Sealing was achieved by covering the hole with a piece of 60 μm hot-melt and a glass slide.

EIS of symmetrical Pt/I₃⁻/I⁻/Pt cells was carried out periodically over 21 days using a Solartron SI 1287 electrochemical interface and Solartron SI 1260 impedance/gain-phase analyzer. Characterization was carried out at open circuit using an ac perturbation of 10 mV and a frequency range 100 kHz to 0.1 Hz. Spectra were analyzed using ZView version 2.90 software (Scribner Associates, Inc.). $R_{CT}(Pt)$ was obtained by fitting the arc observed at highest frequency in Nyquist plots¹¹ to the equivalent circuit shown in Fig. 1, which contained the elements series resistance (R_s), and constant phase element [CPE(Pt)] and $R_{CT}(Pt)$ associated with the counter electrode/electrolyte interface. The use of a CPE instead of a capacitor reflected the textured, heterogeneous surface of Pt-coated ITO glass electrodes.

DSSC fabrication and testing.—Solaronix Ti-nanoxide T-paste was screen-printed on Asahi FTO glass (8 Ω/□) to 8 × 8 mm and to three layers, giving films with thickness ~18 μm. Layers were allowed to “flow” at room temperature for ~5 min and then dried at ~120°C for ~10 min prior to the printing of subsequent layers. TiO₂ films were sintered using a maximum temperature of 500°C. Sintered, transparent films at ~120°C were placed in 0.3 mM N719 Ru dye solution in 1:1 ACN:*t*-butyl alcohol and left to sensitize for 24 h. Sealed DSSCs were fabricated using a 60 μm hot-melt spacer. The liquid electrolyte contained 0.6 M DMPII, 0.03 M I₂, 0.1 M guanidine thiocyanate (GT), and 0.5 M *t*-butyl pyridine (TBP) in 85:15 ACN:VN. Sputtered, CE, or p + CE type counter electrodes were used and had a small hole drilled to allow for introduction of the liquid electrolyte via vacuum backfill. Devices were sealed by covering the hole in the counter electrode with a piece of 60 μm hot-melt and a glass slide. A mask of slightly larger size than the active area was also used. *I*-*V* curves of DSSCs were measured periodically over 21 days on a Newport Solar Simulator under AM1.5 and 100 mW cm⁻² illumination intensity, which was set using a calibrated Si diode (PECCELL), whose incident photon to

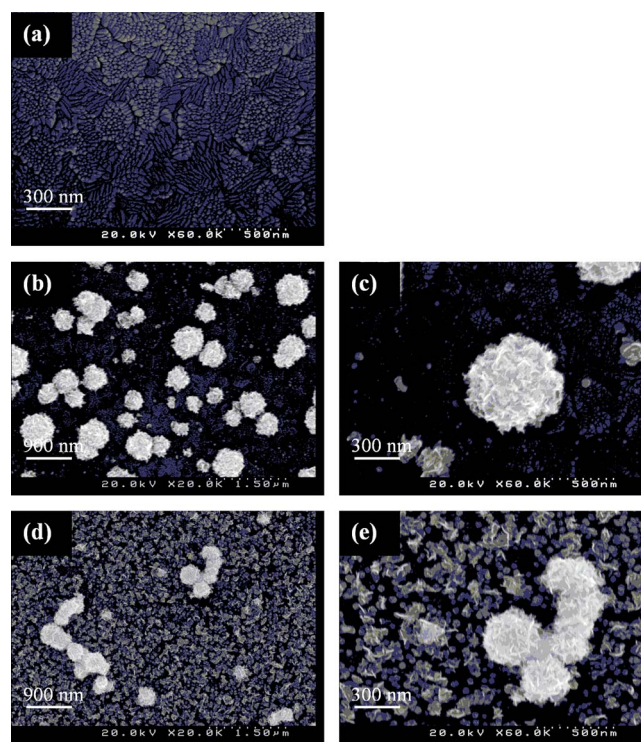


Figure 2. (Color online) SEMs of different Pt-coated ITO glass electrodes (a) sputtered, (b, c) CE, and (d, e) p + CE.

current efficiency spectrum had been adjusted to match an N719-sensitized solar cell. Devices were kept in a drawer in the dark between measurements.

EIS characterization of DSSCs commenced with monitoring of the open-circuit voltage (V_{oc}) of devices under AM1.5, 100 mW cm⁻² illumination until stable within ~±2 mV (typically reached within ~2 min of illumination). This stable value for V_{oc} was then applied as the dc bias for EIS experiments, over which an ac perturbation of 10 mV was applied over the frequency range 100 kHz to 0.1 Hz. $R_{CT}(Pt)$ was obtained by fitting the arc observed at highest frequency in Nyquist plots²⁰ to the equivalent circuit shown in Fig. 1.

Results and Discussion

Counter electrode characterization.—SEMs of sputtered, CE deposited, and pulse/constant potential (p + CE) deposited Pt-coated ITO glass electrodes are shown in Fig. 2.

The sputtered-type Pt coating was conformal and reflected the morphology of the underlying ITO glass substrate. This morphology consisted of a considerably textured surface including elongated features of size ~70 × 20 nm. The CE-type electrode was characterized by a surface sparsely covered with rounded, textured particles of size ~600 nm. The use of an initial pulse of overpotential in the case of the p + CE type electrode led to a very different morphology compared to the CE-type electrode, characterized largely by particles of size ~40 nm and intermittently by the presence of rounded, textured agglomerates of size ~350 nm. The effect on morphology when using an electrochemical pulse here was similar to previous studies.^{18,21} It was expected that the changes to Pt electrode morphology with and without an initial pulse of overpotential would influence performance within DSSCs. Specifically, the apparent higher surface area of p + CE type electrode in particular was expected to result in enhanced DSSC performance.

Figure 3 shows overlaid CVs recorded for sputtered, CE, and p + CE type electrodes in I₃⁻/I⁻ electrolyte, while Table I summarizes the peak cathodic current (I_{pc}) and peak cathodic potential

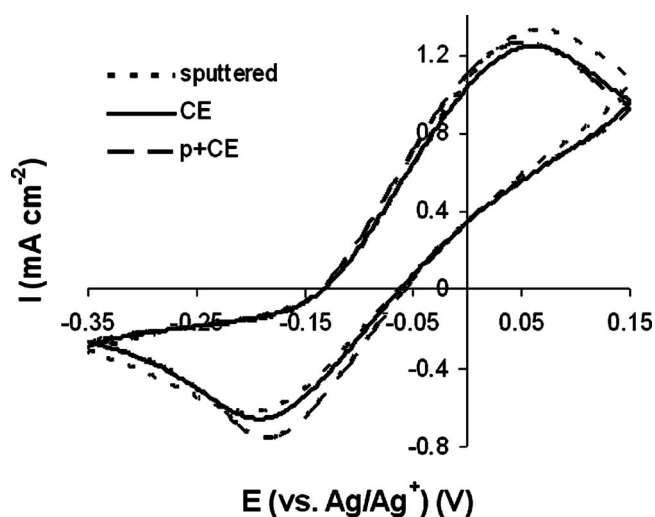


Figure 3. CVs of sputtered, CE, and p + CE type electrodes. Electrolyte: 1 mM I_2 , 20 mM TPAI, and 0.2 M TBAP in ACN. $\nu = 10 \text{ mV s}^{-1}$.

(E_{pc}) data related to I_3^- reduction. CVs obtained for electrodeposited Pt (CE and p + CE) demonstrated higher absolute I_{pc} values compared to sputtered Pt. Consistent with the trend in I_{pc} , electrodeposited Pt demonstrated lower absolute E_{pc} values compared to sputtered electrodes. These results suggest an electrochemical activity series p + CE > CE > sputtered. In turn, this electrochemical activity series would predict that electrodes obtained by the p + CE method would give the best performance within DSSCs, followed by those obtained using the CE method and finally sputtered Pt. To confirm the apparent advantage of Pt electrodeposit electrodes over the sputtered electrode, EIS characterization of sealed symmetrical Pt/ I_3^-/I^- /Pt cells was carried out.

Figure 4 illustrates Nyquist plots recorded on the day of fabrication of representative symmetrical Pt/ I_3^-/I^- /Pt cells based on sputtered, CE, and p + CE type electrodes, while $R_{CT}(Pt)$ results averaged over four cells as a function of time are shown in Fig. 5. The error associated with measured $R_{CT}(Pt)$ values was $\pm 8.5\%$. All electrode types showed good stability over time, especially in the case of p + CE type electrode. Consistent with results of CV characterization above, sputtered and CE-type electrodes showed similar $R_{CT}(Pt)$ values of 1.1 and 1.2 $\Omega \text{ cm}^2$, respectively. Impressively, the p + CE type electrode showed a substantially lower $R_{CT}(Pt)$ value of 0.6 $\Omega \text{ cm}^2$. To our knowledge this is the lowest $R_{CT}(Pt)$ value reported for a Pt electrodeposit electrode to date.

Utilization of Pt electrodeposit counter electrodes in DSSCs.— Trends in I - V curve performance parameters over time for DSSCs utilizing counter electrodes based on sputtered, CE, and p + CE type electrodes were obtained (Fig. 6). Each data point presented is the average of four experimental values, and the error associated with overall efficiency (η) values was $\pm 3.6\%$. Short circuit current (I_{sc}) and V_{oc} were largely unaffected by counter electrode type and both decreased over time, indicative of an increase in recombination at the photoanode/electrolyte interface.^{22,23} The influence of the

Table I. Summary of I_{pc} and E_{pc} data related to I_3^- reduction on sputtered, CE, and p + CE type electrodes taken from CVs in Fig. 2.

Electrode type	I_{pc} (mA cm^{-2})	E_{pc} (vs Ag/Ag ⁺) (V)
Sputtered	-0.48	-0.202
CE	-0.51	-0.192
p + CE	-0.62	-0.186

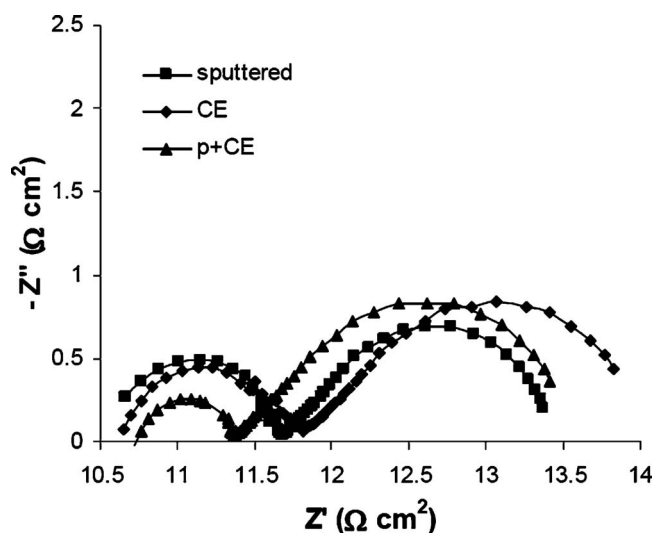


Figure 4. Nyquist plots recorded on day of fabrication of symmetrical Pt/ I_3^-/I^- /Pt cells based on sputtered, CE, and p + CE type electrodes. Electrolyte: 0.6 M DMPII and 0.03 M I_2 in 85:15 ACN:VN.

counter electrode used was most evident when considering the fill factor (FF) obtained. Devices utilizing electrodeposited Pt counter electrodes showed significantly higher FF values compared to devices utilizing sputtered Pt counter electrode. This was due to the lower $R_{CT}(Pt)$ measured within DSSCs for Pt electrodeposits compared to sputtered Pt, which is discussed below in relation to the EIS characterization of devices. Interestingly, the FF of all devices increased slightly with time; however, this was likely the result of the fall in resistive losses due to falling I_{sc} with time and not an improvement in the performance of counter electrodes. The significantly higher FF values achieved for DSSCs based on Pt electrodeposit counter electrodes translated into $\sim 5\%$ relative improvement in η values compared to DSSCs based on sputtered Pt counter electrode.

Nyquist plots were recorded on the day of fabrication for representative DSSCs utilizing sputtered Pt or electrodeposited Pt counter electrodes (Fig. 7). The variation of $R_{CT}(Pt)$ values obtained over time are shown in Fig. 8, where each data point was the average of four experimental values, while the associated error was $\pm 11.9\%$. For any given point in time, DSSCs based on Pt electrodeposit counter electrodes demonstrated $R_{CT}(Pt)$ values that were $\sim 1/2$

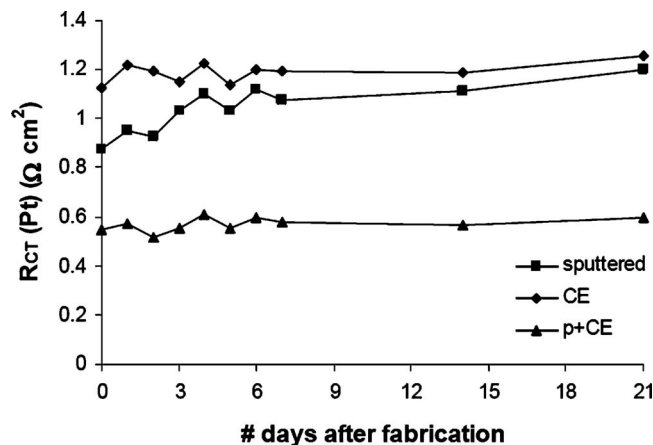


Figure 5. $R_{CT}(Pt)$ results from EIS characterization of Pt/ I_3^-/I^- /Pt cells based on sputtered, CE, and p + CE electrode types over time. Electrolyte: 0.6 M DMPII and 0.03 M I_2 in 85:15 ACN:VN.

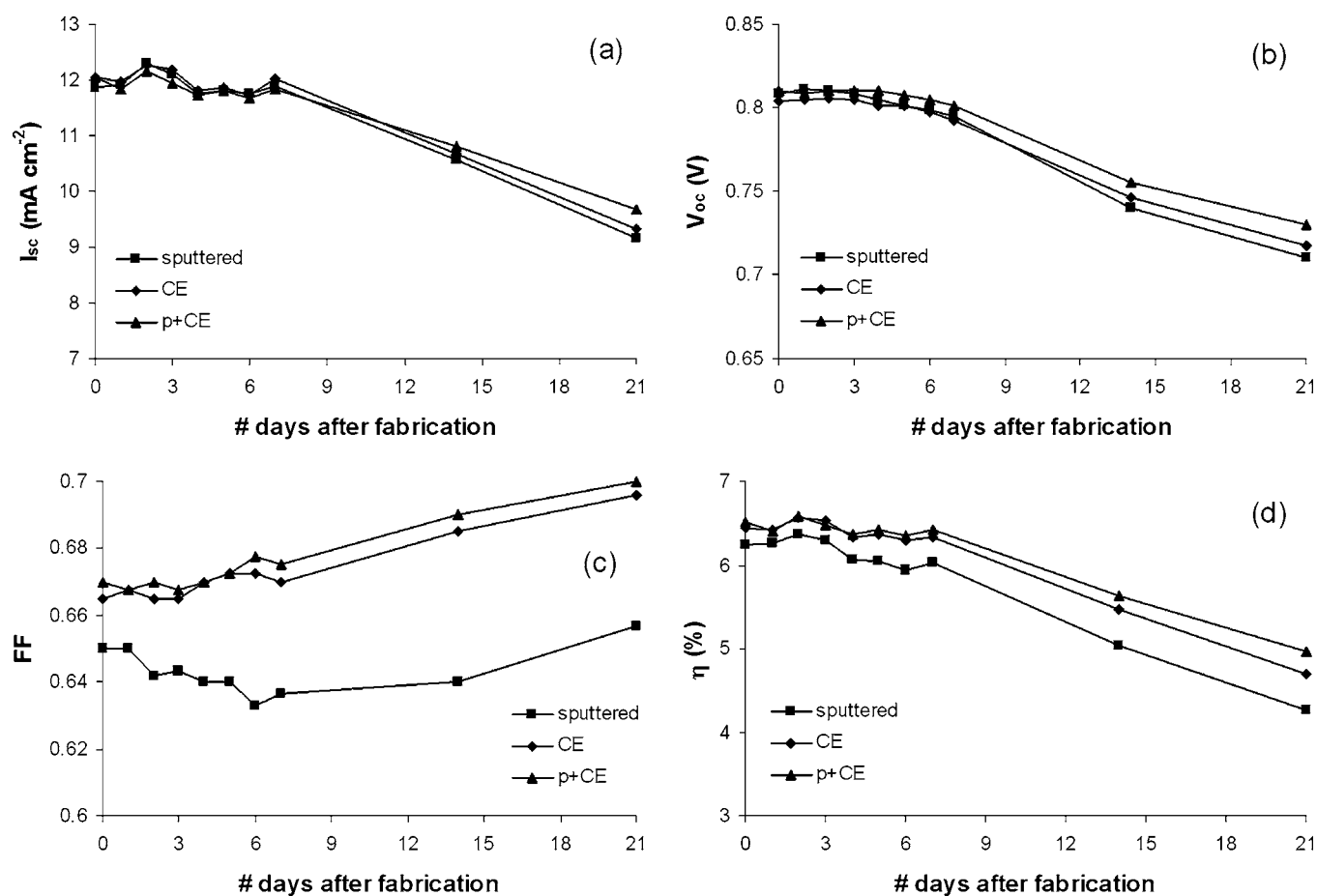


Figure 6. Trends in I - V curve performance parameters over time for DSSCs utilizing counter electrodes based on sputtered, CE, and p + CE electrode types (a) I_{sc} , (b) V_{oc} , (c) FF, and (d) η at AM1.5, 100 mW cm^{-2} illumination. Electrolyte: 0.6 M DMPII, 0.03 M I_2 , 0.1 M GT, and 0.5 M TBP in 85:15 ACN:VN.

those of DSSCs based on sputtered Pt counter electrode. The lower $R_{CT}(\text{Pt})$ values of devices based on Pt electrodeposited counter electrodes meant that the overall internal resistance of such devices was also lower, leading to the significantly higher FF values observed in Fig. 6. $R_{CT}(\text{Pt})$ values increased with time for all counter electrode types, in contrast to the stable $R_{CT}(\text{Pt})$ values observed for the EIS characterization of Pt/ I_3^-/I^- /Pt cells (Fig. 5). This may be attributed to the flow of photocurrent through devices during I - V testing. The minimal increase in $R_{CT}(\text{Pt})$ with time for devices based on electrodeposited Pt counter electrodes was much less compared to devices based on sputtered Pt counter electrode, demonstrating the higher catalytic stability of Pt electrodeposits. On the day of fabrication, devices based on sputtered, CE, and p + CE type counter

electrodes demonstrated $R_{CT}(\text{Pt})$ values of 1.6, 0.8, and $0.7 \Omega \text{ cm}^2$, respectively. These values were slightly higher (with the exception of CE-type counter electrode) compared to the $R_{CT}(\text{Pt})$ values obtained from the EIS characterization of Pt/ I_3^-/I^- /Pt cells (Fig. 5). This may be attributed to the additives GT and TBP used in the liquid electrolyte of DSSCs, which were not used in the liquid electrolyte for Pt/ I_3^-/I^- /Pt cells. Moreover, the different operation of illuminated DSSCs and the symmetrical Pt/ I_3^-/I^- /Pt devices at open-circuit condition may contribute to this slight difference.

Conclusions

Sputtered and electrodeposited Pt coatings on ITO glass were compared as counter electrodes in DSSCs. SEM of Pt electrodepos-

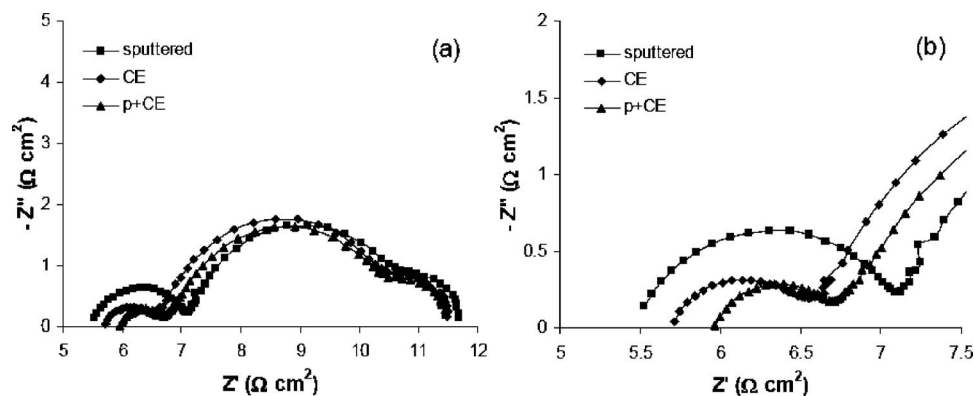


Figure 7. Nyquist plots recorded on day of fabrication for DSSCs based on sputtered, CE and p + CE type counter electrodes (a) showing complete EIS spectra and (b) zoom of high-frequency arcs related to counter electrode/electrolyte interface. Electrolyte: 0.6 M DMPII, 0.03 M I_2 , 0.1 M GT, and 0.5 M TBP in 85:15 ACN:VN.

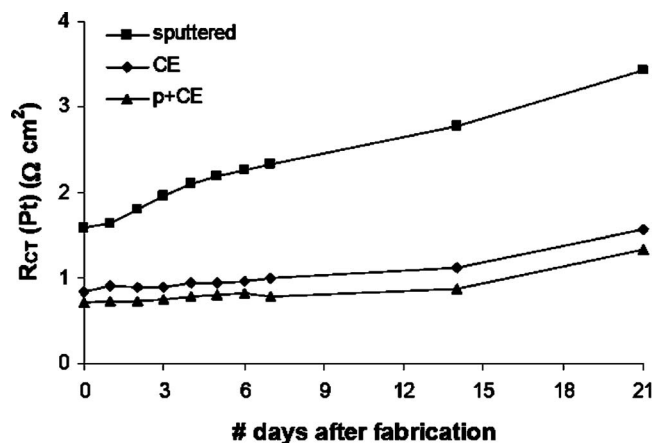


Figure 8. $R_{CT}(Pt)$ results from EIS characterization of DSSCs utilizing counter electrodes based on sputtered, CE, and p + CE electrode types over time. Electrolyte: 0.6 M DMPII, 0.03 M I_2 , 0.1 M GT, and 0.5 M TBP in 85:15 ACN:VN.

its revealed that the use of an initial cathodic overpotential pulse of -0.6 V followed by growth at -0.4 V greatly influenced morphology compared to when no such pulse was used. CV of sputtered, CE, and p + CE type electrodes, and EIS of symmetrical $Pt/I_3^-/I^-/Pt$ cells based on such electrodes, suggested that Pt electrodeposits would in general give enhanced performance as counter electrodes within DSSCs. This was confirmed by $I-V$ testing of DSSCs, which demonstrated $\sim 5\%$ relative improvement in overall η when Pt electrodeposit counter electrodes were used in place of a sputtered Pt counter electrode. In addition to superior outright performance, Pt electrodeposit counter electrodes were also found to be more catalytically stable compared to a sputtered Pt counter electrode. The best counter electrode was the p + CE type, which showed $R_{CT}(Pt)$ values of 0.6 and 0.7 $\Omega\text{ cm}^2$ within a symmetrical $Pt/I_3^-/I^-/Pt$ cell and a DSSC, respectively.

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