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Enhancing Transient Stability of PLL-Synchronized Converters by Introducing Voltage Normalization Control

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***Abstract*— This paper presents a novel phase-locked loop (PLL) structure for improving the transient stability of grid-connected converters by introducing voltage normalization control (VNC) in the conventional PLL. First, the underlying mechanism of losing synchronization during a grid fault is analyzed, and it is revealed that the key factor is the significant decrease of voltage magnitude at the point of common coupling (PCC). In order to avoid the decrease of damping ratio due to the voltage dips, a voltage normalization control method is introduced by controlling the *d*-axis voltage magnitude to the rated value even during grid faults. To this end, the transient stability can be improved during grid faults. Phase portraits when using a conventional PLL and the PLL+VNC are both visualized for validating the effectiveness of the proposed structure. The performance of adding the additional voltage normalization control is analyzed through both small-signal and large-signal models. Finally, the experimental results are presented to verify the effectiveness of improved PLL structure for enhancing the transient stability.**

***Index Terms*— phase-locked loop, transient stability, grid faults, voltage normalization control, voltage-source converters**

I. INTRODUCTION

Recently, with the high penetration of power converter-based renewable energy integrated into the grid, stability issues of grid-connected converters have received more and more attention. Generally, stability issues can be divided into two categories: small-signal stability and large-signal stability [1]-[4]. The small-signal stability analysis is based on a steady operation point and then linearizing the non-linear part in the control structure. The precondition of the small-signal analysis is that there exists a steady-state operation point. However, under large-signal disturbances such as grid faults, the operating point may not exist or can not be achieved. This kind of stability issue is defined as large-signal stability. One common large-signal stability issue of grid-connected converters is synchronization stability. The PLL is widely employed for grid synchronization of power converters [5], and large-signal synchronization stability describes whether the PLL can track and synchronize to the grid voltage during a large disturbance. For simplicity, the large-signal synchronization stability is also called transient stability, which will be used in this paper.

A lot of works have been conducted to analyze the transient stability of PLL-synchronized voltage source converters (VSC) under grid faults. In [6], the loss of synchronization (LOS) of the converter during grid faults is presented, and the mechanism is revealed because of no equilibrium point caused by the voltage drop on the load. In [7], several different mathematical models of the PLL during grid faults are built. It has been found that the damping ratio of the PLL is a key factor affecting transient stability. In [8]-[10], an efficient model and a systematic method for the synchronization stability assessment are proposed, and the effect of different parameters, such as bandwidth, damping ratio, the ratio between resistance and inductance (R/X) are analyzed. Furthermore, a non-linear damping ratio is defined to reveal the synchronization instability caused by the sudden change of active power or short circuit ratio (SCR) in [11]. In order to obtain the stability boundary, an analytical averaging method is applied for solving the non-linear equation in [12]. However, this method is still based on the small-signal approximation, which might have obvious errors under large disturbances. In [13]-[14], the interaction between the current control loop and the PLL control loop is considered to build a more accurate model to analyze the transient stability. All these papers are aimed at how to model the non-linear dynamic process during large-signal disturbances. In [15], a virtual impedance embedded with the PLL can make the VSC synchronized with a remote stronger voltage behind the virtual impedance. However, this method is applied for the small-signal improvement, and the performance of this enhanced PLL during the grid faults are unclear and need to be further analyzed.

To improve the transient stability during grid faults, some works have been done in the literature. In [16], an adaptive current injecting method was developed for improving synchronization stability. However, this method depends on an accurate estimate of the grid impedance. A PLL freezing method is proposed in [17], which freezes the PI regulator of

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the PLL. The PLL output then follows the frozen pre-fault frequency and phase-angle values. In [18], the active current is changing with the PLL frequency to improve the dynamic stability, which lacks further theoretical proof. An adaptive PLL structure is proposed by eliminating the integral link during the grid fault, which is achieved by the detection of the change rate of the grid frequency [19]-[20]. In [21], a variable structure PLL (VSPLL) is proposed by disabling the integral part and reducing the PLL to a first-order system during the grid fault.

In conclusion, most of these methods aim to improve the damping ratio of the PLL by modifying the controller parameters. However, the operation of the PLL will also be significantly changed by modifying these parameters. Moreover, the PLL damping is significantly reduced during the grid fault since the damping ratio of the PLL is strongly dependent on the magnitude of the input PCC voltage. Therefore, to maintain the designed damping ratio during the grid fault and improve the transient stability, this work introduces a novel voltage normalization control (VNC) in the PLL. The transient benefits of the VNC applied in PLL have previously been highlighted in [22]-[24]. However, the VNC in [22] applies numerically sensitive division for the normalization, and it is performed in the stationary reference frame, which makes it difficult to analyze with the *dq*-frame PLL dynamics. The normalization methods in [23]-[24] are obtained by the *d*-axis voltage of the PLL, however, still with the drawbacks of a numerical division. To that end, only the small-signal model is built in these papers without considering the transient stability during grid faults.

In this paper, a novel PLL structure is put forward for enhancing the transient stability during grid faults by introducing a different voltage normalization control. Instead of using division by the real-time voltage magnitude, an additional *d*-axis voltage control is introduced for the VNC. This method can keep a unified PLL structure during the normal or grid fault conditions, without the necessity for detecting the grid voltage magnitude or frequency. The mathematical model of the PLL+VNC is established and validated by simulation results. Both phase-plane analysis and simulation results verify that the PLL+VNC can enhance synchronization stability during grid faults. Furthermore, the small-signal model is built for a qualitative analysis of the voltage normalization control, which demonstrates the damping ratio can be maintained the same as the normal voltage even under grid faults. The attraction region is also calculated based on large-signal analysis to prove that faster voltage normalization control is better for synchronization stability during grid faults.

The outline of this paper is arranged as follows. In section II, the mathematical model of conventional PLL is built, and the effect of *R*/*X* ratio and grid voltage magnitude are studied. The improved PLL structure with voltage normalization control is presented in Section III, and the phase portrait based on the mathematical model is illustrated for interpreting the function of the additional *d*-axis voltage control. In section IV, the mathematical model of the PLL+VNC is first verified by the simulation results. Then, the effect of voltage normalization control is examined by qualitative and quantitative analysis. In Section V, the experimental results based on a 7.35 kVA VSC is conducted to test the effectiveness of the proposed PLL+VNC. Lastly, the conclusions are drawn in Section VI.

II. System Description

The topology of the grid-connected converter is illustrated in Fig. 1. $\boldsymbol{U}_{pcc}$ and $\boldsymbol{U}_f$ represent the PCC voltage and grid voltage, $\boldsymbol{I}_{pcc}$ is the current injected into the grid, L_{cf} is the converter filter which is applied for suppressing current harmonics, Z_L is the grid impedance, U_{dc} is the dc voltage, which is assumed constant.

The grid-connected converter is working as a current source. In order to achieve accurate control of the current injected into the grid, the commonly used control method is vector control, which is highly relying on the PLL to estimate the angle of PCC voltage. Based on the Park transformation, the converter current can accurately be controlled by PI controllers in the *dq* frame. In this paper, the converter is being represented as an ideal controllable current source whose orientation is determined by the PLL dynamics. Such a representation can be assumed for two reasons. First, the dominating dynamics of loss of synchronization lies in the low-frequency range. Secondly, the bandwidth of the inner current regulator is usually placed much higher than that of the PLL, which facilitates that they can be analyzed individually [6],[8],[16].

The reference direction of the current injected into the grid can be seen in Fig. 1. In the steady-state, the PCC voltage can be expressed by the grid voltage and PCC current as,

$$\boldsymbol{U}_{pcc} = Z_L \boldsymbol{I}_{pcc} + \boldsymbol{U}_f \tag{1}$$

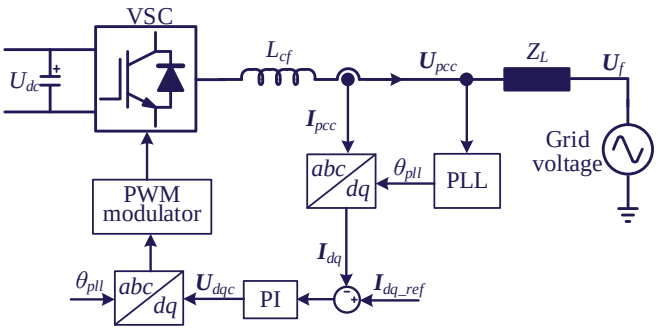

Fig. 1. Topology and control diagram of VSC connected to a weak grid.

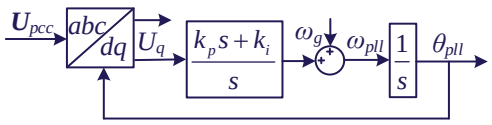

Fig. 2. Structure of conventional SRF-PLL.

The commonly used PLL block in Fig. 1 is the synchronous reference frame PLL (SRF-PLL), the structure of which is shown in Fig. 2. The input is the three-phase PCC voltage, and the output is the estimated angle of PCC voltage, which is denoted as θ_{pll} to distinguish from the PCC voltage angle θ_{pcc}. In the steady-state, $\theta_{pll}=\theta_{pcc}$. However, in the dynamic process, such as a phase jump or a grid fault, $\theta_{pll}\neq\theta_{pcc}$. ω_g is a constant grid frequency feedforward term, which is 100π rad/s in this paper, ω_{pll} is the PLL angular frequency, $f_{pll} = \omega_{pll}/(2\pi)$ is the PLL frequency. k_p and k_i are the proportional and integral parameters of the PI controller applied in the SRF-PLL.

A. Damping ratio of conventional PLL

The *q*-axis voltage in Fig. 2 can be expressed as,

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$$U_q = U_{pcc}\sin\left(\theta_{pcc}-\theta_{pll}\right) \tag{2}$$

where U_{pcc} is the magnitude of PCC voltage.

As can be seen from Fig. 2, the small-signal model of the conventional PLL can be deduced, as shown in Fig. 3.

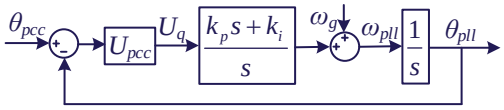


Fig. 3. Small-signal model of conventional SRF-PLL.

The transfer function of the conventional PLL is expressed as,

$$G_{PLL}(s)=\frac{\theta_{pll}}{\theta_{pcc}}=U_{pcc}\frac{k_p s+k_i}{s^2+U_{pcc}k_p s+U_{pcc}k_i}=\frac{2\zeta\omega_N s+\omega_N^2}{s^2+2\zeta\omega_N s+\omega_N^2} \tag{3}$$

where ζ is the damping ratio and ω_N is the undamped natural frequency of the system, which can be expressed as,

$$\zeta=\frac{k_p}{2}\sqrt{\frac{U_{pcc}}{k_i}},\qquad \omega_N=\sqrt{U_{pcc}k_i} \tag{4}$$

As can be seen from (4), the damping ratio will decrease if the magnitude of PCC voltage decreases. Thus, it can be concluded that the magnitude of PCC voltage is introduced into the SRF-PLL, which will have a significant influence on synchronization stability. It should be noted that the conventional SRF-PLL will always be stable under a strong grid without grid impedance since the PCC voltage is unaffected by the power injected into the grid. However, the PCC voltage will change a lot with the variation of injected power under a weak grid, which might cause the instability of the PLL during a large disturbance like grid voltage sags. In the following analysis, the effect of grid impedance and the magnitude of the grid voltage will be further emphasized.

B. *Effect of R/X ratio*

In actual situations, the grid impedance is a combination of inductance and resistance. The grid impedance is more likely to be resistive for low-voltage networks, while in high-voltage systems, the grid impedance is more likely to be inductive. The impedance characteristic depends on the voltage level, typical line impedance values of different voltage levels are seen in Table I. Thus, it is necessary to study the effect of different *R*/*X* ratios given a fixed short circuit ratio (SCR). Assuming that the inductance of grid impedance is X_L, the resistance of grid impedance is R_L.

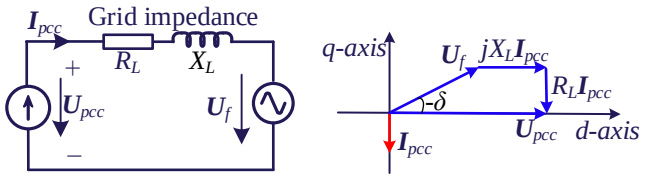
Table I Typical line impedance values [25]

Type of Line	R(Ω/km)	X(Ω/km)	R/X (p.u.)
Low voltage line	0.642	0.083	7.7
Medium voltage line	0.161	0.190	0.85
High voltage line	0.06	0.191	0.31

Given an RL type grid impedance, the equivalent circuit is shown as Fig. 4 (a). Under a severe grid fault, only the pure reactive current is injected to the grid and the corresponding phasor diagram can be shown as Fig. 4(b), where the angle difference between the PCC voltage and grid voltage is defined as $\delta=\theta_{pll}-\theta_g$.

According to Fig. 4, the *d* axis and *q* axis component of the PCC voltage can be expressed as,

$$\begin{aligned} U_{pccd} &= U_f\cos\delta + R_L I_d - X_L I_q \\ U_{pccq} &= -U_f\sin\delta + R_L I_q + X_L I_d \end{aligned} \tag{5}$$



(a) (b)

Fig. 4. Simplified representation of VSC connected to weak grid
(a) Equivalent circuit of VSC considering grid impedance.
(b) Phasor diagram when only injecting reactive current to the grid.

If the fault is very severe, the active current changes to zero and only injecting reactive current to the grid, the *dq* voltage can be simplified as,

$$\begin{aligned} U_{pccd} &= U_f\cos\delta - X_L I_q \\ U_{pccq} &= -U_f\sin\delta + R_L I_q \end{aligned} \tag{6}$$

In the steady-state, U_{pccq}=0. Thus, the magnitude of the PCC voltage is equal to U_{pccd}, which can be calculated by the grid voltage and injected current as,

$$U_{pcc}=\sqrt{U_f^2-R_L^2 I_q^2}-X_L I_q \tag{7}$$

According to this formula, since the I_q is negative during the fault, the magnitude of PCC voltage will increase with the increase of X_L, which is good for increasing the damping ratio. However, the magnitude of PCC voltage will decrease with the increase of resistance, which indicates that the resistance is harmful to transient stability when injecting pure reactive currents. Thus, a pure resistive grid is the worst case for transient stability under very serious grid faults.

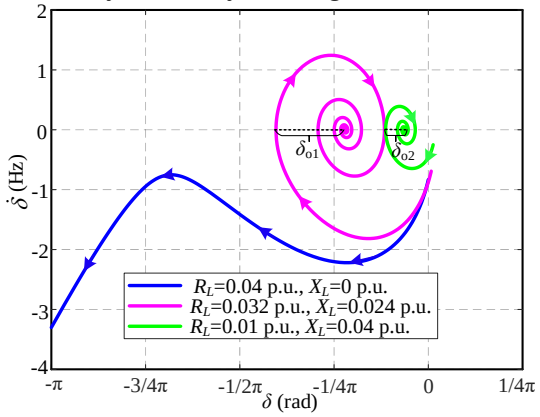


Fig. 5. Phase portrait of conventional SRF-PLL with different R/X ratios.

The phase portrait with the same SCR but with different *R*/*X* ratios is shown in Fig. 5., where Z_L = 0.04 p.u. and the faulty voltage is 0.05 p.u. The parameters of the PLL are shown in Table I. The biggest angle deviation from the equilibrium point is defined as the angle overshoot, which is denoted as δ_{o1} and δ_{o2}. It can be seen that it is easier to lose synchronization with a large *R*/*X* ratio. With the decrease of the *R*/*X* ratio, the angle overshoot during the grid fault is smaller, which is better for synchronization during the grid fault given a fixed SCR. Thus, the case with pure resistance is the worst case for maintaining synchronized with the grid. Therefore, in the latter work, a purely resistive impedance is considered for investigating the worst case.

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C. *Effect of magnitude of grid voltage*

As it can be seen from (3), for a second-order system, the decrease of damping ratio will increase the overshoot of angle, which is prone to cause the loss of synchronization during the grid fault. Furthermore, it can be seen in (4) that the damping ratio is highly dependent on the grid voltage magnitude, which indicates that the decrease of voltage magnitude will also decrease the damping ratio and increase the angle overshoot. To that end, the decrease of the voltage magnitude is the main reason for causing the instability during grid fault.

In order to verify this point, the phase portrait of different PCC voltage magnitudes with conventional SRF-PLL can be shown in Fig. 6. The grid impedance is purely resistive, the value of which is 0.04 p.u. The proportional gain and integral gain of PLL are 0.4 and 25, respectively. The initial grid voltage is 1 p.u. but the fault voltages are different, which leads to different phase portraits during the transient process. The largest angle deviation from the equilibrium point is defined as the angle overshoot, which is denoted as δ_{o3} and δ_{o4}. As can be seen from Fig. 6, with the decrease of the grid voltage, the angle overshoot is increasing, which corresponds with the damping ratio in (4). If the angle overshoot exceeds the other unstable equilibrium point, the SRF-PLL will lose synchronization stability, which can be seen as the blue line in Fig. 6.

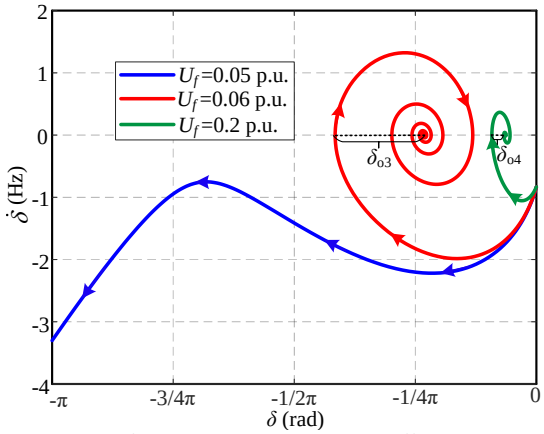

Fig. 6. Phase portrait of conventional SRF-PLL with different grid voltage dips with purely resistive impedance R_L=0.04 p.u.

III. MATHEMATICAL MODEL OF PLL+VNC

As can be seen from section II-C, the main problem causing the synchronization instability is the decrease of voltage magnitude. Thus, the intuitive idea is to increase the magnitude of the PCC voltage. It is difficult to increase the real PCC voltage, which is constrained by the physical circuits. However, the voltage magnitude inside the PLL block can be increased by controlling the *d*-axis voltage to the base value, which can also be called as the voltage normalization control. This improved PLL+VNC structure can be seen in Fig. 7. The obvious difference between the conventional SRF-PLL is that the *d*-axis voltage is also controlled to the base value through an integrator. The output of the *d*-axis voltage control is a gain λ, which is multiplied by the real PCC voltage to make the magnitude of voltage input to PLL still equal to the rated voltage even during grid faults, which can effectively improve the synchronization stability under grid voltage dips.

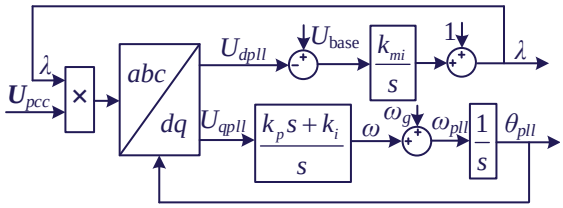

Fig. 7. Structure of the improved PLL with voltage normalization control.

The conventional PLL structure is illustrated in Fig. 2, which is a second-order system. However, the improved PLL structure shown in Fig. 7 is a third-order system since there is an integrator added in the *d*-axis voltage control. Thus, it is essential to rebuild the mathematical model of the improved PLL+VNC.

In section II-B, it is concluded that the converter is more vulnerable to lose synchronization under a purely resistive network during grid faults because the converter is only injecting reactive current to the grid. Thus, the grid impedance is assumed purely resistive to consider the worst situation. Before the grid fault, the converter only injects active current. During a severe grid fault, the converter should inject reactive current according to grid codes. Thus, the phasor diagram before and during grid fault can be illustrated in Fig. 8, where $\boldsymbol{U}_g$ represents the grid voltage before fault and I_{pcc} is the current magnitude.

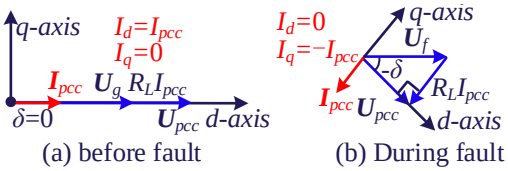

Fig. 8. Phasor diagram before and during grid fault.

As can be seen from Fig. 8, the real PCC voltage in *dq* frame during grid fault can be expressed as,

$$\begin{aligned} U_d &= U_f \cos(\delta) \\ U_q &= -U_f \sin(\delta) - R_L I_{pcc} \end{aligned} \tag{8}$$

During a grid fault, U_q should be equal to 0 in the steady-state. Thus, the angle δ in the steady-state can be deduced from (8) as,

$$\delta = \arcsin\left(\frac{-R_L I_{pcc}}{U_f}\right) \tag{9}$$

As can be seen from (3), the angle δ during a grid fault is a negative value, which means that the PCC voltage is lagging behind the grid voltage. When using the improved PLL structure for acquiring the angle and frequency of the PCC voltage, the *dq* axis voltage applied in PLL can be expressed as,

$$\begin{aligned} U_{dpll} &= \lambda U_f \cos(\delta) \\ U_{qpll} &= -\lambda\left(U_f \sin(\delta) + R_L I_{pcc}\right) \end{aligned} \tag{10}$$

For the conventional PLL, the PCC voltage in the *dq* axis is the same as the PLL voltage. However, a magnitude gain λ is introduced in the PLL+VNC structure for regulating the real PCC voltage to the rated grid voltage even under grid voltage faults. In Fig. 7, λ is the magnitude gain for voltage normalization control, which can be expressed as,

$$\lambda = 1 + k_{mi} \int \left(U_{base} - U_{dpll}\right) dt \tag{11}$$

In the time-domain, the PLL phase angle in the improved

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PLL structure from Fig. 7 can be expressed as,

$$\theta_{pll} = \int \left(k_p U_{qpll} + k_i \int U_{qpll} dt + \omega_g \right) dt \tag{12}$$

where ω_g is the grid frequency and $\int \omega_g dt = \theta_g$, substituting this to the right-hand side of (12) and performing differentiation twice, the dynamic response of the system can be deduced as,

$$\begin{aligned} \ddot{\delta} = &-\dot{\lambda} k_p \left(R_L I_{pcc} + U_f \sin(\delta) \right) - \lambda k_p U_f \cos(\delta) \dot{\delta} \\ &-\lambda k_i \left(R_L I_{pcc} + U_f \sin(\delta) \right) \end{aligned} \tag{13}$$

The differentiation of magnitude gain λ can be expressed by,

$$\dot{\lambda} = k_{mi} \left(U_{base} - U_{dpll} \right) \tag{14}$$

Combining (10), (13), and (14), the phase portraits of the improved PLL+VNC during grid fault can be plotted, as shown in Fig. 9. The phase portrait of the conventional PLL is also plotted for comparison.

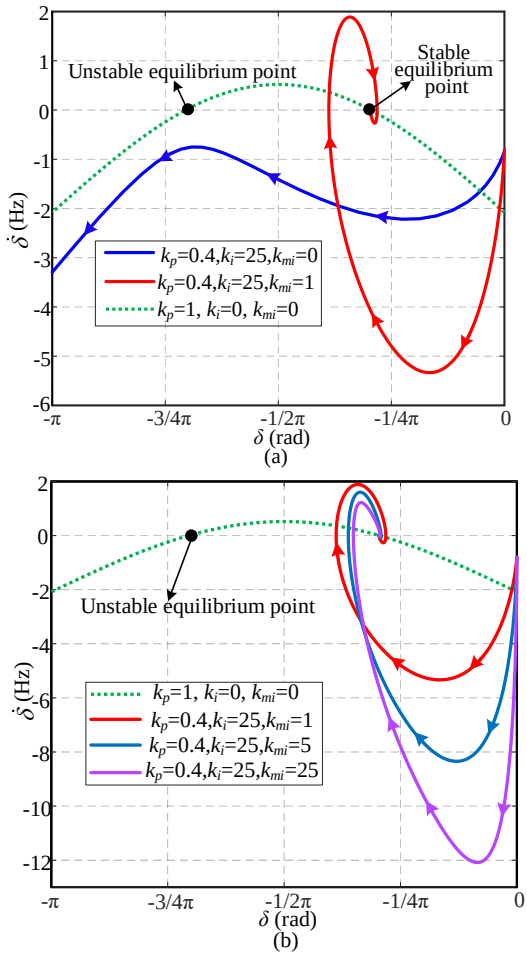

Fig. 9. Phase portraits of different PLL structures and different parameters (a) conventional PLL and PLL+VNC(k_{mi}=1) (b) PLL+VNC (different k_{mi}).

In Fig. 9, k_{mi}=0 (λ=1) means there is no additional control of the *d*-axis voltage, which is just the conventional PLL structure. k_i=0 and k_p=1 mean the integral link is disabled in the conventional PLL, which is reduced to a first-order system. As can be seen from the phase-plane analysis, the conventional PLL structure will lose synchronization when k_p is small. However, when the voltage normalization control is added in the conventional PLL, the PLL can arrive at the stable equilibrium point with the same PLL parameters. This validates that the PLL+VNC structure can improve synchronization stability.

In order to analyze the effect of different integral coefficients in the *d*-axis voltage control loop, Fig. 9(b) is plotted to show that a larger integral coefficient will cause a larger overshoot of frequency and smaller overshoot of angle δ. This indicates that the *d*-axis voltage control ability is increased with the increase of k_{mi}. The decrease of the angle overshoot demonstrates the effectiveness of enhancing transient stability by introducing the voltage normalization control.

IV. Performance Analysis of PLL+VNC

In this section, the mathematical model of the proposed PLL+VNC is firstly validated by simulations. Then, the effect of k_{mi} on the performance of the PLL+VNC is analyzed by the small-signal analysis and large-signal analysis. The small-signal analysis gives a qualitative view of seeing why the additional voltage normalization control can improve the transient stability under grid faults. On the other hand, the large-signal analysis presents a quantitative analysis to prove that the increase of k_{mi} can increase the attraction region of PLL, which is better for transient stability under different initial conditions.

A. Verification of the mathematical model

In order to verify the mathematical model in (13) and (14), this is compared to a detailed VSC model conducted in Matlab Simulink. The results of the mathematical model are solved by using the ode45 solver in Matlab. The parameters of the VSC in Matlab Simulink can be seen in Table II.

Table II main parameters of the system in Fig. 1

Symbol	Description	Value
S_b	Rated power	7.35 kVA
V_b	Nominal grid voltage	400 V
V_{dc}	DC-link voltage	730 V
f_0	Nominal frequency	50 Hz
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
L_{cf}	Converter-side inductor	0.14 p.u.
k_p	Proportional gain of PLL	0.4
k_i	Integral gain of PLL	25
k_{mi}	*d*-axis gain of PLL+VNC	0.1,1,5,25

The PLL frequency response with different k_{mi} during grid fault can be seen in Fig. 10. At 0 s, the grid voltage suddenly decreases to 0.05 p.u. As can be seen from the results, the PLL frequency f_{pll} also decreases due to the *q*-axis voltage is negative, and the PLL tries to resynchronize with the grid. The variation of the frequency increases with the increase of k_{mi}, since the k_{mi} has a similar effect to k_p of the conventional PLL during grid faults. Furthermore, it is clear to see that all the simulation results and mathematical results match very well, which proves the correctness of the derived reduced-order non-linear mathematical model in Section III.

The angle response with different k_{mi} during a grid fault can be seen in Fig. 11. Before the grid fault, since only active power is injected into the grid and the grid impedance is a pure resistance, the angle difference between the grid voltage and PCC voltage is zero. During the grid fault, the PCC voltage will

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lag the grid voltage, as shown in Fig. 8. With the increase of the k_{mi}, the angle overshoot during the grid fault is decreased, which is beneficial for transient stability. Furthermore, all the simulation results are almost overlapping with the mathematical results, verifying the accurateness of the mathematical model. Thus, the mathematical model can be applied for further analysis instead of using the complex simulation model.

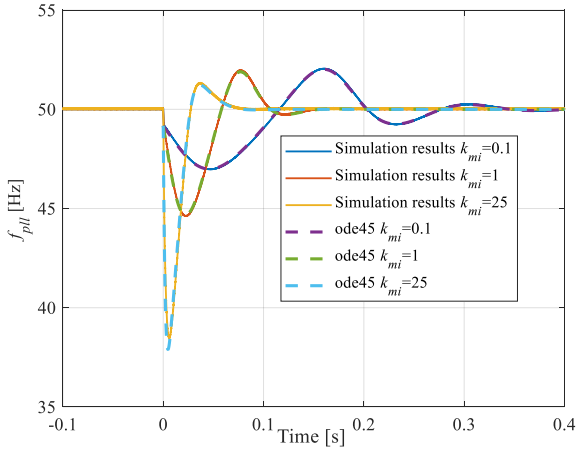

Fig. 10. Frequency response with different k_{mi} during a grid fault.

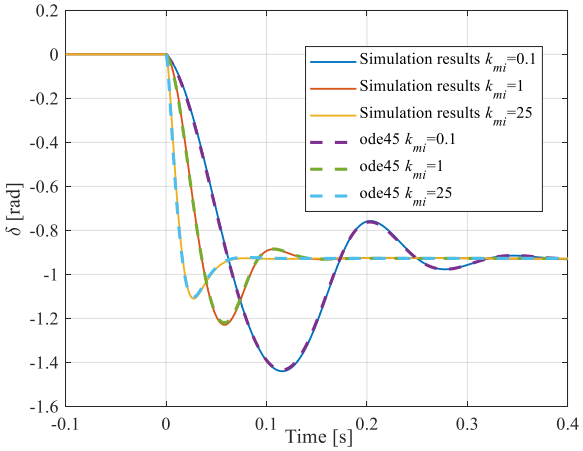

Fig. 11. Angle response with different k_{mi} during a grid fault.

B. *Analysis of k_{mi} effect*

The k_p and k_i design is the same as for the conventional PLL to consider both the steady filtering ability and the dynamic tracking performance. The damping ratio is set as 0.707 for an optimization design [26]. The bandwidth of the PLL is always set between 10-40 Hz. In this paper, k_p is set as 0.4, and k_i is set as 25. With these parameters, the damping ratio of the PLL is 0.72, and the bandwidth of the PLL is 30 Hz. Hence, the key task of this part is to analyze the effect of k_{mi} on transient stability through small-signal and large-signal analysis.

As can be seen from (13), the mathematical model is a non-linear system, which does not have any general analytical solution. In order to give a qualitative analysis, the small-signal model based on (13) and (14) is analyzed. Since the proposed PLL is a third-order system, defining the state variables [δ, ω, λ]=[x_1, x_2, x_3]. Thus, the state space equations can be expressed as,

$$\begin{aligned}
\dot{x}_1 &= x_2 = f_1 \\
\dot{x}_2 &= -k_i x_3 \left(U_f \sin(x_1) + R_L I_{pcc}\right) - k_p U_f \cos(x_1) x_2 x_3 \\
&-k_p k_{mi} \left(U_{base} - x_3 U_f \cos(x_1)\right)\left(R_L I_{pcc} + U_f \sin(x_1)\right) = f_2 \\
\dot{x}_3 &= k_{mi}\left(U_{base} - U_f \cos(x_1) x_3\right) = f_3
\end{aligned} \tag{15}$$

Here, $\boldsymbol{A}$ is the Jacobian matrix containing the partial derivatives of the system evaluated at the equilibrium point and it is expressed as,

$$\boldsymbol{A} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix}, \text{ where } A_{ij} = \left[\frac{\partial f_i}{\partial x_j}\right]_{x=x_0}, i, j = 1,2,3$$

$$\boldsymbol{A}_{VNC} = \begin{bmatrix} 0 & 1 & 0 \\ -k_i x_{30} U_f \cos(x_{10}) & -k_p x_{30} U_f \cos(x_{10}) & 0 \\ k_{mi} U_f \sin(x_{10}) x_{30} & 0 & -k_{mi} U_f \cos(x_{10}) \end{bmatrix} \tag{16}$$

where x_{10}, x_{20}, and x_{30} are the stable equilibrium points of δ, ω, and λ, which can be calculated by setting (15) to zero. Thus, the equilibrium points can be deduced as,

$$\begin{aligned}
x_{10} &= -\arcsin\left(R_L I_{pcc} / U_f\right) \\
x_{20} &= 0 \\
x_{30} &= U_{base} / \left(U_f \cos\left(x_{10}\right)\right)
\end{aligned} \tag{17}$$

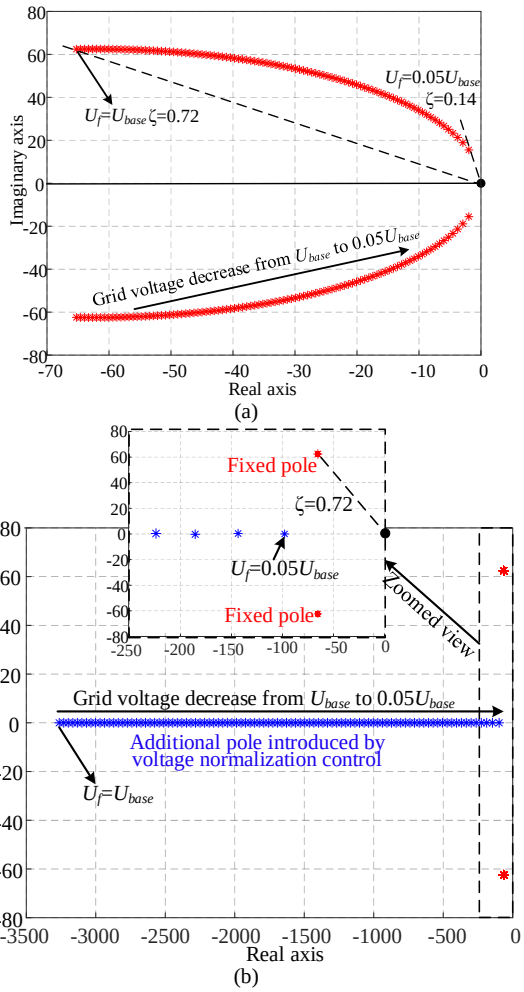

Fig. 12. Root locus of conventional PLL and improved PLL with the decrease of grid voltage (a) conventional PLL. (b) improved PLL with k_{mi}=10.

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If k_{mi} is equal to zero, the proposed PLL will be reduced to the conventional PLL structure. Thus, the mathematical model is reduced to a second-order system, and the Jacobian matrix of the conventional PLL can be deduced as,

$$\boldsymbol{A}_{conv}=\begin{bmatrix}0 & 1\\ -k_iU_f\cos(x_{10}) & -k_pU_f\cos(x_{10})\end{bmatrix} \tag{18}$$

As can be seen from (18), the voltage magnitude has a direct effect on the roots of the system. Based on (17) and (18), the root locus of the conventional PLL with the decrease of grid voltage can be seen in Fig. 12(a). With a decreasing grid voltage, the damping ratio decreases significantly. At the nominal grid voltage, the damping ratio of the PLL is 0.72. However, the damping ratio reduces to 0.14 when the grid voltage drops to 0.05 p.u., which is the main reason that causes synchronization instability during grid faults. Thus, it is necessary to maintain the damping ratio even during the grid voltage sags.

In order to avoid the decrease of damping ratio caused by grid faults, the additional *d*-axis voltage control is introduced, which means that the k_{mi} is not equal to zero. The Jacobian matrix changes to a third-order expressed as (16), substituting (17) into (16), the Jacobian matrix of PLL+VNC can be deduced as,

$$\boldsymbol{A}_{VNC}=\begin{bmatrix}0 & 1 & 0\\ -k_iU_{base} & -k_pU_{base} & 0\\ -k_{mi}R_LI_{pcc}x_{30} & 0 & -k_{mi}U_{base}/x_{30}\end{bmatrix} \tag{19}$$

As can be seen from (19), the elements in the top two rows are only related to k_p, k_i, and U_{base}, which have no relationship with the fault voltage. According to (17) and (19), the root locus of the PLL+VNC with a decreasing grid voltage can be seen in Fig. 12(b). With the decrease of the grid voltage, only the additional real pole changes on the real axis, the two conjugate poles are fixed without any change. Furthermore, since the real part of the additional pole is much larger than the real part of the conjugate poles, which means that the additional pole has almost no effect on the dynamic performance. The dynamic performance is determined by the fixed pole, which is the same as the normal voltage. To that end, the voltage normalization control method can guarantee the damping ratio as the normal condition even under highly sagged grid voltages, which is beneficial for the synchronization stability during grid fault.

Furthermore, since the improved PLL structure is non-linear, the synchronization stability during grid faults is also related to the initial conditions. With different initial conditions, the stability might be different even with the same control parameters under identical grid faults. Thus, the attraction region is introduced for the stability comparison with different parameters. The attraction region means that if the initial state belongs to this range, the PLL+VNC will be stable during the grid fault.

Since the frequency and angle are used for the current control, the *d*-axis output λ is just a constant value under a fixed grid voltage. To this end, the initial value of the λ is assumed constant under the normal grid voltage, and the key point is to discuss the different initial values of frequency ω and angle δ, which are more important for the transient stability. Thus, only the state variables ω and δ are employed for calculating the attraction region. The 2-D basin of attraction can be seen as a slice of 3-D basin of attraction when λ is given a constant value. The attraction region with different k_{mi} is shown in Fig. 13. The method for obtaining the attraction region is just simply by scanning all the different initial values and then using numerical integration to calculate (15) to verify whether it is stable or not. It can be clearly seen that the attraction region can be expanded with an increase of k_{mi}, which verifies that the voltage normalization control is effective in improving the transient stability during the grid faults.

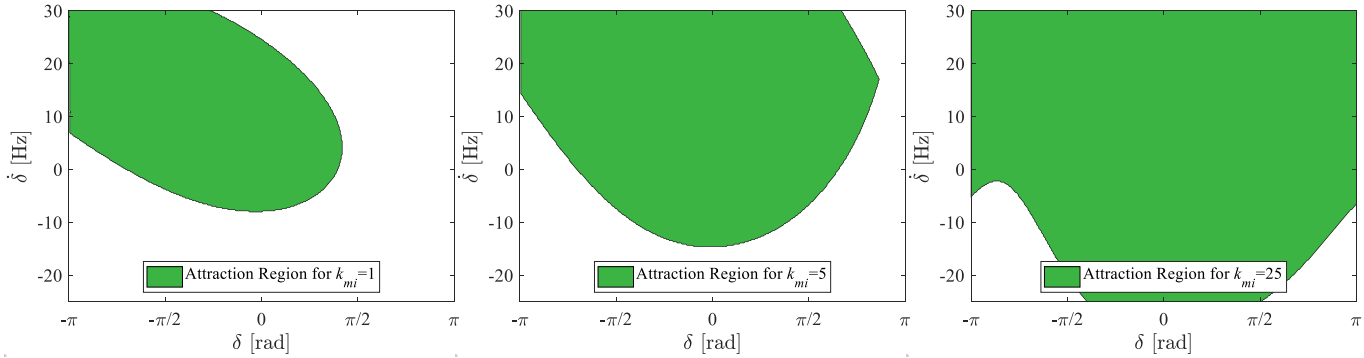

Fig. 13. Attraction region of improved PLL+VNC with different k_{mi}.

V. Experimental Results

In order to verify the effectiveness of the novel PLL+VNC, the experiments are carried out with a 7.35 kVA three-phase grid-connected converter. The parameters of the converter are shown in Table I. A 45 kVA Chroma 61845 grid emulator is employed for generating normal grid voltage and faulty grid voltage. The grid impedance is purely resistive with a value of 0.04 p.u. When the grid voltage drops to 0.05 p.u., the active current is reduced to zero, and the reactive current injected into the grid is 1 p.u.

Firstly, in order to validate the performance of PLL+VNC during the normal grid, the experimental results of frequency and phase tracking performance are shown in Fig. 14. As can be seen from Fig. 14(a), the frequency of PCC voltage changes from 50 Hz to 60 Hz, the frequency of the PLL can track the reference in 60 ms. The rising time of firstly arriving at the reference value is 16 ms, which corresponds with the bandwidth setting at 30 Hz. This experimental result validates the

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effectiveness of the PLL+VNC for tracking the frequency change. The phase tracking performance of PLL+VNC during phase jump can be seen in Fig. 14 (b). In this case, the phase of the grid voltage suddenly increases by 30° (pi/6 rad). The frequency also increases fast to track the phase jump. In 40 ms, the PLL frequency comes back to the rated value, demonstrating that the PLL output angle has tracked the phase jump quickly. Thus, the PLL+VNC well tracks both the phase and frequency.

As can be seen from Fig. 15, the conventional PLL will lose synchronization during grid fault since the frequency drops quickly without the possibility to resynchronize. The angle difference δ is oscillating, and the frequency of the converter current is changing quickly due to the loss of synchronization. However, when applying the PLL+VNC, the PLL frequency resynchronizes in 40 ms during the grid fault, and the angle difference δ and converter current are both stable during the grid fault, which validates the effectiveness of the PLL+VNC.

In order to test the effect of different k_{mi}, the experimental results under the same grid faults but with different k_{mi} are shown in Fig. 16. As can be seen from the results, the frequency variation is increased with the increase of k_{mi}. However, the overshoot of δ is decreased since the k_{mi} increases the control ability of the d-axis voltage control, which makes it faster to reach the base value. The experimental results are also consistent with the theoretical analysis and the simulation results in Fig. 10 and Fig. 11.

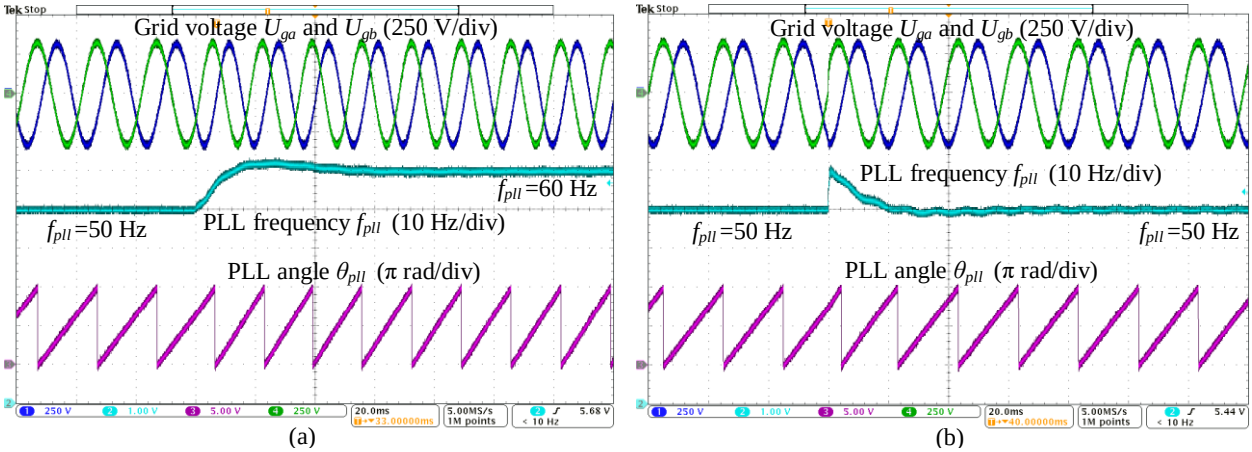

Fig. 14. Experimental results of PLL+VNC during normal grid (a) Frequency tracking performance, (b) Phase tracking performance.

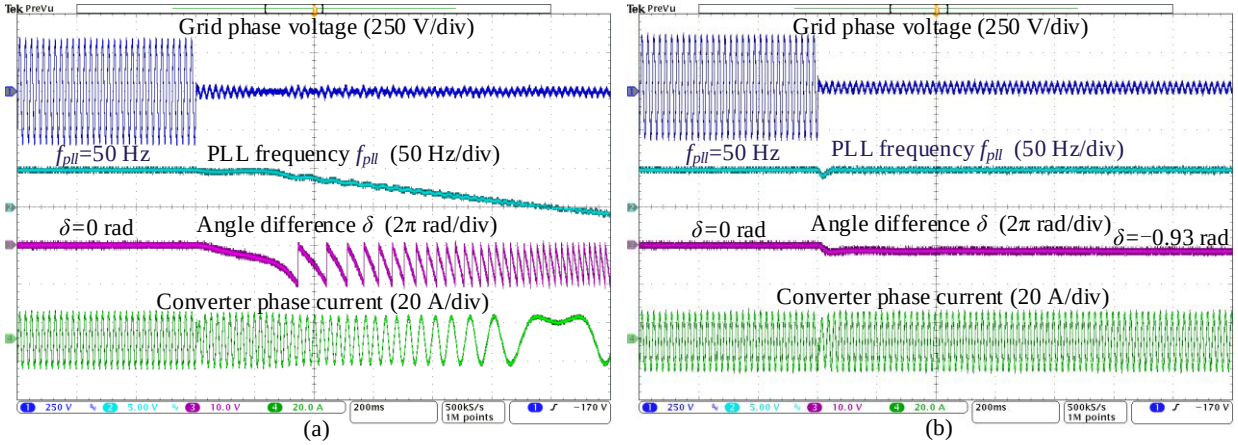

Fig. 15. Experimental results of VSC under grid fault with different PLL structures (a) conventional PLL, (b) PLL+VNC (k_{mi}=5).

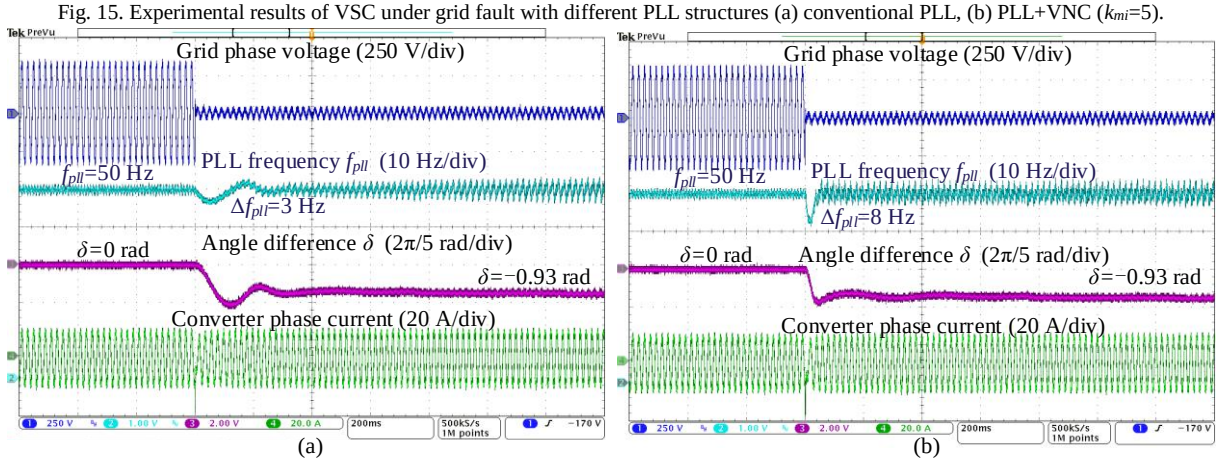

Fig. 16. Experimental results of VSC under grid fault with PLL+VNC (a) k_{mi}=0.1, (b) k_{mi}=5.

VI. Conclusions

An improved PLL+VNC structure is proposed for enhancing the transient stability of the grid-connected converter during grid faults. The magnitude of the PCC voltage inside the PLL is controlled to the rated value for maintaining the damping ratio of PLL. The detailed non-linear mathematical model of the improved PLL+VNC is built, which shows a high accuracy compared to detailed simulation model studies. The overshoot of the angle δ is greatly reduced by the PLL+VNC, which can enhance the transient stability during grid faults. Furthermore, small-signal analysis is employed for qualitative analysis to reveal the key mechanism of improving synchronization stability. Additionally, large-signal analysis is used for calculating the attraction area with different initial states, which proves that the transient stability can be improved by introducing the proposed voltage normalization control. Lastly, the experimental results verify the effectiveness of the improved PLL+VNC.

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