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Advanced active pixel architectures in standard CMOS technology

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Abstract
This paper aims at exploring and validating the adoption of standard fabrication processes for the realization of CMOS active pixel sensors, for particle detection purposes. The goal is to implement a single-chip, complete radiation sensor system, including on a CMOS integrated circuit the sensitive devices, read-out and signal processing circuits. A prototype chip (RAPS01) based on these principles has been already fabricated, and a chip characterization has been carried out; in particular, the evaluation of the sensitivity of the sensor response on the actual operating conditions was estimated, as well as the response uniformity. Optimization and tailoring of the sensor structures for High Energy Physics applications are being evaluated in the design of the next generation chip (RAPS02). Basic features of the new chip includes digitally configurable readout and multi-mode access (i.e., either sparse of line-scan readout). © 2005 IEEE.

Keywords
cmos, advanced, technology, active, pixel, architectures, standard

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***Abstract*—This paper aims at exploring and validating the adoption of standard fabrication processes for the realization of CMOS active pixel sensors, for particle detection purposes. The goal is to implement a single-chip, complete radiation sensor system, including on a CMOS integrated circuit the sensitive devices, read-out and signal processing circuits. A prototype chip (RAPS01) based on these principles has been already fabricated, and a chip characterization has been carried out; in particular, the evaluation of the sensitivity of the sensor response on the actual operating conditions was estimated, as well as the response uniformity. Optimization and tailoring of the sensor structures for High Energy Physics applications are being evaluated in the design of the next generation chip (RAPS02). Basic features of the new chip includes digitally configurable readout and multi-mode access (i.e., either sparse of line-scan readout).**

I. Introduction

In RECENT years, active-pixel (APS) architectures, commonly exploited for vision applications, have been proposed for detecting minimum ionising particles [1], [2], as an alternative to customary architectures based on microstrips or passive pixel arrays. In APS schemes, each pixel includes a few control devices (usually, MOSFETs), which take care of photodiode buffering, precharge and reset. This potentially improves the signal-to-noise ratio (S/N) and, thus, makes it unnecessary the adoption of dedicated fabrication technologies (e.g., high-resistivity or epitaxial substrates). Standard fabrication processes bring a number of advantages, in term of both performance and costs. This work aims at implementing a single-chip, complete radiation sensor system, including sensitive device as well as read-out and signal processing sections, by means of a fully standard CMOS technology. In [3], [4], design and development of a prototype chip based on these principles were introduced, the functionality of which was experimentally validated in [5]. In this paper, this approach is extended, and the organization and design of a new architecture is discussed. We still focus on a flexible read-out scheme, through which the same sensor array can be interrogated either in a fast, sparse mode, or in a conventional line-scan mode, tailoring its behavior for different operating requirements.

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II. Technology and Design Issues

In solid-state detectors, an impinging ionising particle can be identified by collecting the free charge generated in the semiconductor bulk: detection capability depends, thus, on both the charge generation rate and the charge collection efficiency. High bias-voltages and low-doped (i.e., high-resistivity) substrates are, hence, used in several solid-state radiation detectors (e.g., [6]) so that thick (200–500 μm) semiconductor layers can be fully depleted. Unfortunately, full-depletion of the substrate layer cannot be achieved in advanced CMOS technologies: low supply voltages are to be used (to avoid breakdown), and low-resistivity substrates are needed (due to latch-up concerns). Some technologies may offer a relatively thick, low-doped epitaxial layer, which can be exploited for enhancing charge sensitivity [2]. On the other hand, the adoption of mainstream technology ensures definite advantages in terms of steady, progressive reduction of fabrication costs and increase of performance figures [7].

A more specific advantage of deep submicron technologies consists of the intrinsic radiation hardness of MOS conventional circuitry: due to the thinning of gate oxide, radiation-induced leakage current and threshold voltage shift become less critical. Radiation damage also influences charge sensing devices: traps induced into the sensitive volume may alter charge collection properties to some extent. A recent literature work, however, discusses such an issue, with reference to APS fabricated in a 0.25 μm CMOS technology. According to [8], radiation tolerance constraints for linear colliders or space applications, can still be readily fulfilled by advanced CMOS technologies.

In this work, the photodiode response was preliminarily evaluated by means of physical device simulation [9], allowing for taking into account most geometrical and physical details related to the actual technology process.

The first prototype was fabricated by UMC, with a 0.18 μm CMOS process, which features 1 polysilicon layer and 6 metal interconnect layers. It provides no epitaxial layer and the supply voltage is limited to 1.8 V. The substrate is, therefore, far from being fully depleted; simulations [3], [10] show that the effective charge collection is practically limited to a sensitive volume which is about ten microns deep. Hence, the hit of a Minimum Ionising Particle (MIP) generates less than 1000 electron/hole effective pairs. Due to such a small charge budget, the careful control of parasitic devices and the actual sizing of sensitive area are of the utmost importance, in order to optimize charge-collection and noise properties.

Proper amplifier stages were designed, to ensure a proper output S/N ratio. The transfer function of such amplifiers can

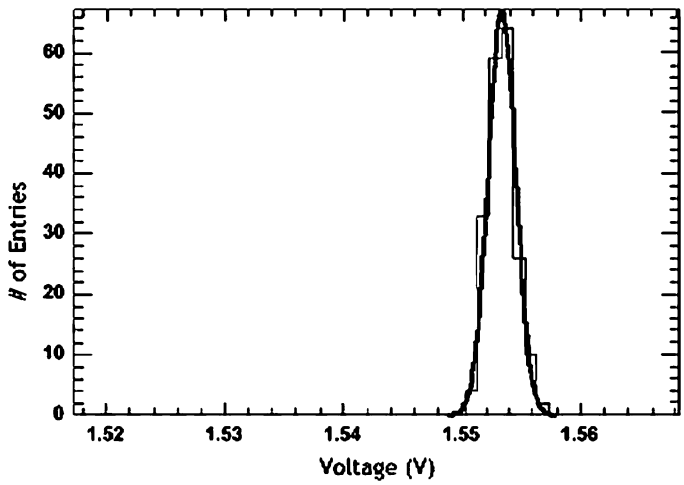

Fig. 1. Single pixel total noise evaluation: values are sampled 75 μsec after the reset falling edge for several acquisitions. A mean value of 1.553 V has been measured, with a 1.157-mV deviation (σ).

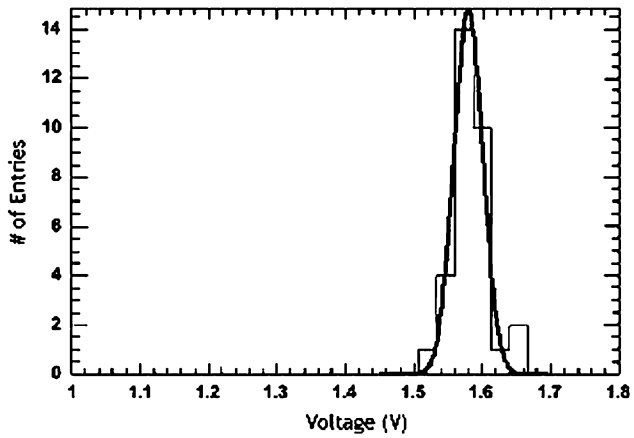

Fig. 2. Mean values of all 64 pixels of a 8×8 APS structure; values are evaluated during the reset phase. A mean value of 1.58 V has been measured, with a 21.13-mV deviation (σ)).

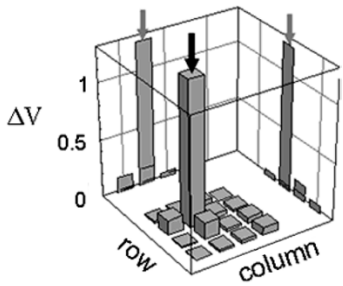

Fig. 3. Alpha particle response: voltage shift at the output node (ΔV) for a particle crossing position in the middle of a sensitive area. Histogram bars represent output data from adjacent pixels in the matrix structure. Digital (on/off) readout mode.

be digitally controlled, allowing for adjusting the bias point and the actual gain. Configurability is useful for calibrating the actual chip with respect to fabrication process tolerances, as well as for adapting the chip response to different applications (e.g., different radiation sources). Such a flexibility can be exploited to select optimal trade-offs among sensitivity, spatial resolution and read-out speed.

III. RAPS01 Chip Test

The RAPS01 chip includes several prototypal matrix structures ranging from 8×8 to 32×32 pixel arrays: different pixel layout options have been investigated; several arrays differing in pixel size (ranging from 4.4×4.4 μm^2 to 16×16 μm^2) and pitch were included, thus resulting in a large number of control signals and I/O pins. In order to efficiently manage the corresponding large amount of data, a dedicated PCB test board has been designed and realized: it communicates with three data acquisition boards. Two digital boards (National Instruments PCI-DIO-96, PCI-6503) and an analog/digital one (PCI-6014) are used, managing about 130 I/O and control signals. LabView routines, combined in a common graphic interface, have been written, which allow for fast, flexible and inexpensive setting of control and addressing signal and for analog/digital output read-out.

Pixel noise has been evaluated: in Fig. 1, the distribution of several acquisitions, taken during the reset pulse, is reported. An overall single pixel noise below 1.6 mV has been extracted from the distribution's sigma. A pixel kTC noise of 22 electrons has been evaluated, in line with results reported in literature for such devices [11].

This value includes signal-amplification and noise-reduction effects of read-out circuitry and, thus, can be quite different from the noise estimated at the photodiode [5].

Uniformity of the response over the whole matrix has been checked for as well. In particular, Fig. 2 shows the distribution of the pixel responses for a 8×8 APS matrix during the reset phase. Fixed pattern noise effects can be reduced by means of correlated double sampling techniques, if needed.

After preliminary functional tests [5], more articulated characterizations were carried out in order to validate the re-configurable read-out electronics capabilities and their effect on the sensor performance (e.g., on spatial resolution and sensitivity). For the sake of simplicity, the structure was illuminated by means of 5.4 MeV alpha-particles source (i.e., an Americium Am_{241} source, featuring a 1.6 KBq/cm^2 disintegration rate).

With reference to spatial resolution, it is worth observing that substrate doping significantly affects charge collection and lateral diffusion. Device simulation tools have been exploited in order to evaluate its impact, suggesting that thick epitaxial substrates, although more effective in collecting the charge, should suffer form a larger lateral diffusion of the generated carriers. This possibly makes the charge spreading over a larger number of pixels (depending on pixel size and pitch). Without a low-doped epi-layer, the overall amount of collected charge is reduced, whereas a more selective spatial response should be obtained. It is worth observing, however, that debate is still open on this point [10].

By properly configuring the output amplifiers, however, a highly nonlinear (i.e., a step function) can be obtained, thus, straightforwardly selecting the hit pixel. Such a behavior ("winner-take-it-all") is demonstrated in Fig. 3, which illustrates the response to an alpha particle hit of a subset of pixels: due to amplifiers configuration, only the pixel closer to the particle hit site exhibits a significant (>1 V) voltage swing.

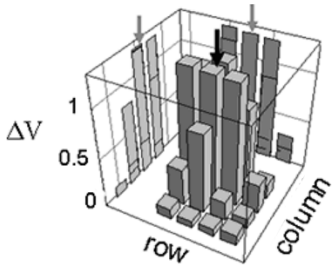

Fig. 4. Alpha particle response: voltage shift at the output node (ΔV). Histogram bars represent output data from adjacent pixels in the matrix structure. Analog readout mode.

Quite different information can be obtained through reconfiguration: by selecting a more linear response (i.e., reducing the gain) of the amplification chain, a larger cluster of pixels exhibit nonnegligible swing, as shown in Fig. 4. Such a pattern can be analyzed in order to extract the cluster centroid, thus enhancing spatial resolution beyond the pixel pitch. Centroid-extraction algorithm can be implemented on-chip, thus, again taking advantages from the enhanced processing power given by advanced CMOS technology.

Extensive testing of RAPS01 chip is still under way: test plans include detailed spatial-resolution and crosstalk anlyses, as well as the evaluation of the sensibility to different radiation sources. To this purpose, an optical test bench has been implemented, which allows for precise mechanical movements (position repeatability below 0.2 μm) and includes a laser beam, which can be focused to a few microns wide spot and features MIP-equivalent energy.

IV. RAPS02 Chip Design

In the development of RAPS01 chip, an asynchronous readout mode has been introduced, conceived for faster detection of sparse particle hit. In the so-called WIPS scheme [5], the sensor array acts as a switch matrix, in which column- and row-lines are precharged at opposite values. As soon as a pixel is hit, its output turns on the switch so that charge sharing between row and column lines occurs, allowing for asynchronous detection of $x - y$ hit coordinates. In order to maximize the voltage swing, in the original WIPS scheme the switch transistor is biased close to its threshold voltage, which may imply relatively large leakage (i.e., dark) currents. In this work, we discuss an alternative approach, which still allows for sparse access to the array (if needed), at the same time allowing for reduced leakage and introducing some further degree of flexibility in the control scheme. The pixel scheme shown in Fig. 5 has been devised and investigated; the small voltage swing at the photodiode cathode drives a high-gain, on-pixel CMOS amplifier, which, in turn, still drives the source-follower buffering stage (i.e., the switch): the voltage swing there is, thus, greatly enhanced, and the column-row charge sharing can be more neatly controlled. By using an inverting pixel amplifier, the switch can be implemented by means of a nMOSFET, instead of the pMOSFET originally included in the WIPS scheme: since the switch should drive a nonnegligible current, transistor size does matter, and avoiding relatively large pMOSFETs reduces parasitic charge drain effects. An

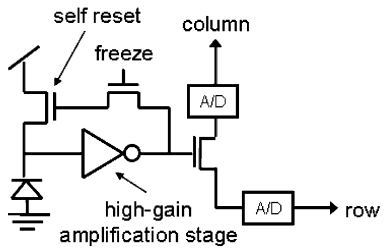

Fig. 5. SHARPS basic circuit.

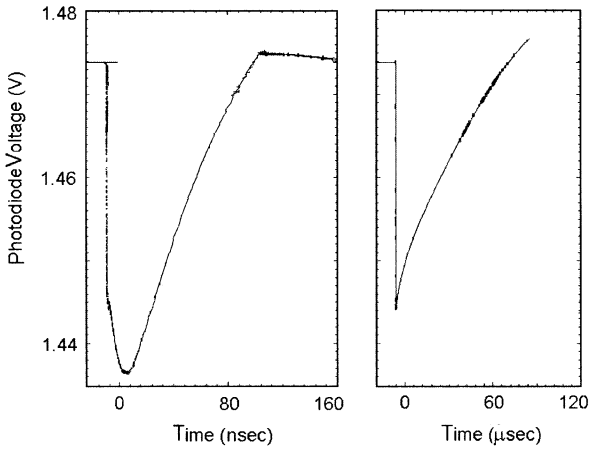

Fig. 6. Simulated photodiode response: feedback enabled for event-triggered reset (left); feedback disabled by the "freeze" transistor for synchronous readout (right). Note the different time scales.

additional advantage comes from the availability of a positive pulse at the amplifier output of the hit pixel, which can be straightforwardly fed back to drive the photodiode RESET transistor. So doing, a self-triggered reset can be carried out, and fully asynchronous operating mode is attained, with no need of periodic reset signals.

The feedback path is actually controlled by a "freeze" transistor: if the transistor is cut off, self-resetting is turned off, and the array can be used in a more conventional synchronous frame-scan access mode. Subthreshold currents of the freeze transistor (which features zero threshold voltage) actually may limit the "hold" time of the reset transistor: estimates however show that a reasonable operating window is available; resetting time-constants may range from 100 ns (feedback active) to 80 μs (when the feedback path is inhibited), as shown in Fig. 6.

This scheme has been named Self-resetting high-gain active radiation pixel sensor (SHARPS), and the overall pixel layout is shown in Fig. 7: the pixel size is 10.3 μm by 10.3 μm; the size of the n-well needed by the pMOS device is much smaller than the sensitive area of the photodiode, so that charge collection efficiency is not significantly affected by this.

Simulations have been carried out, to evaluate the competitive action of the n-well and to estimate parasitic capacitances. To this purpose, an accurate model of the photodiode charge collection [3] has been accounted for.

In Fig. 8, simulated pixel response is reported, accounting for different relative positions of the impinging radiation. The estimated output voltage swing is in the range of several hundreds of mV, and a marked response discrimination is attained. This suggests that a fair charge resolution can also be achieved.

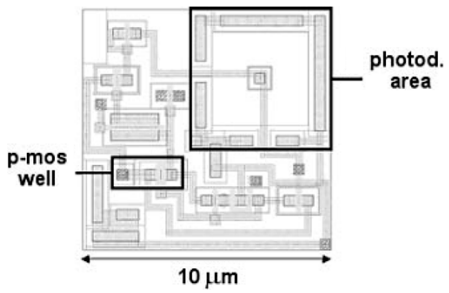

Fig. 7. SHARPS pixel layout.

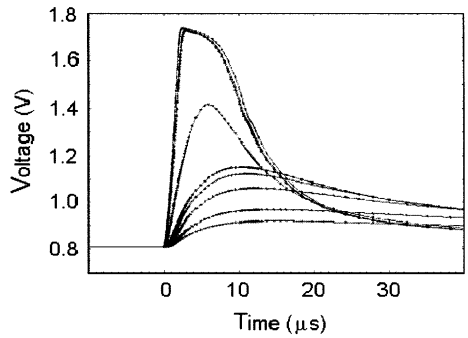

Fig. 8. SHARPS pixel simulated response, at different relative positions of the impinging radiation respect to the photodiode center: 0.0 μm ("central" hit), 1.3 μm, 2.6 μm, 5.15 μm, 6.5 μm 7.8 μm, 9.1 μm, 10.3 μm (hit "at the boundary" between adjacent pixels).

To exploit such a possibility, an on-chip 2-bit A/D conversion is performed at each row and column, so that a spatial resolution finer than the pixel pitch can be achieved: by analysing the cluster response, a spatial resolution of 2.6 μm is obtained.

More generally, the adoption of CMOS technology makes it possible to implement versatile and powerful function in a straightforward manner: here, configurable row and column amplifiers allows for digitally configuring the detector response. Some circuit features have been explicitly devised for the detection of sparse events: nevertheless, conventional frame-scan readout can be carried out as well.

This task is accomplished by the control unit, which can manage control signals in a suitable way (i.e., inhibiting the pixel feedback and activating in a given sequence line amplifiers). Digital signal processing does not pose critical speed issues, since the operating frequency is actually limited by the analog section (down to 1.5 MHz for sparse, event-triggered readout; 10 MHz for traditional synchronous readout). A small area impact is expected as well, with respect to the pixel array. The flexible, configurable readout circuitry, introduced above can also be exploited to make the same chip suitable for detection of radiation of different kind; the chip configurability will be tested against different radiation sources, prospectively evaluating applications.

V. Conclusion

A prototype chip (RAPS01) based on standard CMOS technology has been fabricated, aimed at exploiting the inherent advantages coming from the adoption of advanced fabrication processes.

Test and characterization has been carried out, demonstrating the practicality of the submicron-CMOS approach. Further optimization and tailoring of the integrated sensor system has been included in the design of the next-generation chip (RAPS02). A novel pixel scheme has been suggested, featuring high-gain on-pixel amplification (to increase S/N ratio) and capable of operating in a fully asynchronous fashion. Thanks to the intrinsic system flexibility allowed by CMOS design, further perspective application fields, not strictly limited to HEP experiments, can be considered such as $\alpha-, \beta-, \gamma$-microdosimetry, spectrography, and X-microradiography.

Acknowledgment

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