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# Five-level active NPC converter topology: SHE-PWM control and operation principles

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## Abstract

The neutral-point-clamped (NPC) inverter topology has been the centre of research and development effort for numerous applications, including medium- and high-voltage electric motor drives, static compensators (STATCOMs) and other utility type of power electronic systems for almost three decades now. Pulse-width modulation (PWM) control methods have been developed for such topology for respective three-level and multilevel versions. The issue of voltage balancing between the DC bus capacitors is a drawback that requires attention and the problem becomes more serious as the number of levels increases. Selective harmonic elimination PWM can be applied to control the topology as a method to reduce the switching transitions to the lowest possible number. The active NPC (ANPC) topology is derived from the NPC topology by adding an active switch in anti-parallel to each clamping diode. Hybrid configurations combining flying capacitors are also possible. The five-level topology discussed in this paper is derived through different connections of active clamping paths. A novel recently proposed five-level symmetrically defined SHE-PWM method is applied. The simulation results presented in the paper confirm the suitability of the new method.



## Keywords

topology, she, five, pwm, converter, control, npc, operation, level, principles, active


## Disciplines

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# Five-Level Active NPC Converter Topology: SHE-PWM Control and Operation Principles

Sridhar Reddy Pulikanti, *Student Member, IEEE*, and Vassilios. G. Agelidis, *Senior Member, IEEE*

***Abstract*-- The neutral-point-clamped (NPC) converter topology has been the centre of research and development effort for numerous applications, including medium- and high-voltage electric motor drives, static compensators (STATCOMs) and other utility type of power electronic systems for almost three decades now. Pulse-width modulation (PWM) control methods have been developed for such topology for respective three-level and multilevel versions. The issue of voltage balancing between the DC bus capacitors is a drawback that requires attention and the problem becomes more serious as the number of levels increases. Selective harmonic elimination PWM can be applied to control the topology as a method to reduce the switching transitions to the lowest possible number. The active NPC (ANPC) topology is derived from the NPC topology by adding an active switch in anti-parallel to each clamping diode. Hybrid configurations combining flying capacitors are also possible. The five-level topology discussed in this paper is derived through different connections of active clamping paths. A novel recently proposed five-level symmetrically defined SHE-PWM method is applied. The simulation results presented in the paper confirm the suitability of the new method.**

***Index Terms*— SHE-PWM method, ANPC converter topology, floating capacitor.**

## 1. Introduction

There are mainly three types of multilevel converters, namely, the neutral point clamped (NPC) converter [1], the flying capacitor (FC) converter [2] and
the cascaded H-bridge converter [3] which are shown in Figure 1. The introduction of three-level NPC converter topology in early 1980's has made revolutionary changes in the utilization of power electronics in high power applications. However, as the converter level increases, voltage unbalances between the series capacitors need attention [4] which can be solved by separate DC sources or by voltage regulators for each level. The above mentioned method is not suitable for many applications because extra isolation transformers and switching devices are necessary [4].
However, in order to reduce unbalance voltages across the series DC capacitors, to improve the distribution of losses across the devices of the multilevel converter and to increase the level of converter topology to higher than three-level, different level versions of the above mentioned multilevel topologies can be connected in different combinations, such as: two-level and three-level NPC converters [5] and combination of NPC and FC converters [6]. The topology introduced in [6] shown in Figure 2 is known as the five-level active neutral-point-clamped (ANPC) converter topology. The three-level ANPC converter topology [7] is the extension of the three-level diode-clamped NPC VSC topology derived by replacing the clamping diodes with active switches. The ANPC VSC allows a significant improvement of unequal loss distribution among the switches [7], [8].

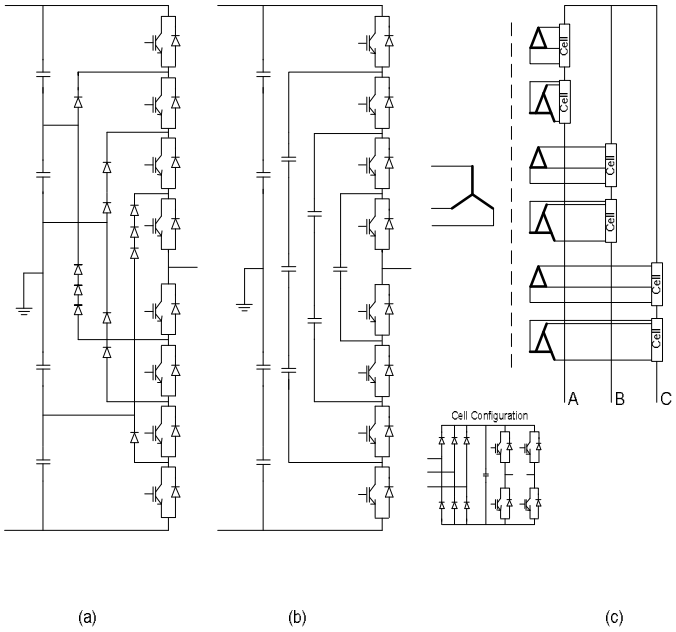


Figure 1. Multilevel converter topologies. (a) NPC, (b) Flying capacitor and (c) Cascaded H-bridge and basic cell.

This paper reports on the suitability of a recently presented novel five-level symmetrically defined SHE-PWM method proposed in [11] through its implementation in the five-level three-phase ANPC converter topology proposed in [6].The paper is organized in the following way: Section 2 presents the five-level ANPC converter topology operational principles and control. The simulation results obtained by implementing a five-level SHE-PWM method in the five-level three-phase ANPC converter topology are presented in section 3 and conclusions are summarized in section 4.

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## 2. FIVE-LEVEL ANPC CONVERTER TOPOLOGY, OPERATIONAL PRINCIPLES AND CONTROL

The simplified five-level ANPC converter topology is shown in Figure 2 [6]. This topology consists of one floating capacitor ($C_f$) and is capable of generating the five different voltage levels, namely, *-2E*, *-E*, 0, *E* and *2E*. The charging or discharging of $C_f$ takes place at middle voltage levels *–E* and *E* depending upon the direction of the load current as shown in Table 1. The voltage across the floating capacitor $V_{C_f}$ should be maintained at *E* which is affected by the switching states V2, V3, V6 and V7 [6]. The voltage across each switch in this topology is one fourth of the DC bus voltage *4E*. This topology has redundancy in switching states which balance the voltage across the $C_f$. $E_{out}$ in Figure 2 represents the line-to-neutral voltage of the phase.

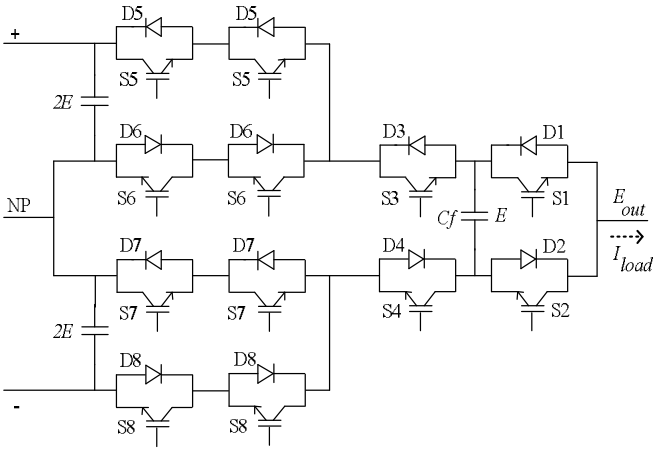


Figure 2. Simplified five-level ANPC converter topology [6].

| Switch state | | | | | | | | Phase Voltage ($E_{out}$) | Effect on $C_f$ | | Switching State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | | $I_{load}>0$ | $I_{load}<0$ | |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | *-2E* | - | - | V1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | *- E* | Discharge | Charge | V2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | *-E* | Charge | Discharge | V3 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | *0* | - | - | V4 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | *0* | - | - | V5 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | *E* | Discharge | Charge | V6 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | *E* | Charge | Discharge | V7 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | *2E* | - | - | V8 |

TABLE 1. SWITCHING STATES AND ITS EFFECT ON THE FLOATING CAPACITOR VOLTAGE.

### *2. 3 Different switching states and their behaviour*

In Figure 2 it is seen that the ANPC converter topology consists of twelve switching devices (S1 to S8) with antiparallel diodes across each switching device namely, D1 to D8. For notation S5 to S8 there are two switching devices in series with their respective diodes in antiparallel (D5 to D8). In the above mentioned switches there exist switch pairs that require complementary control signals. These switch pairs are: (S1, S2), (S3, S4), (S5, S6) and (S7, S8). The switches (S5, S7) require same control signals and the switches (S6, S8) require same control signals which are complementary to (S5, S7) respectively. For simple analysis, it is assumed that $I_{load}$ is greater than zero.

$$I_{C_f} = (X_3 - X_1).I_{load} \quad (1)$$

$$\frac{d}{dt}V_{C_f} = \frac{I_{load}}{C_f}.(X_3 - X_1) \quad (2)$$

$X_1$ and $X_3$ are the switch states of the switches S1 and S3 respectively. The rate of change of the voltage across the floating capacitor $V_{C_f}$ depends on size of the capacitor, the current $I_{C_f}$ flowing through it and the switch states $X_1$ and $X_3$. During the switching states V1, V4, V5 and V8, the switch states of the switches S1 and S3 is equal to 1 which implies that $I_{C_f}$ is equal to zero from equation (1) and during these switching states $C_f$ is not connected to the load. During these switching states the operation principles of five-level ANPC converter topology are similar to the three-level ANPC converter topology [7], [8] which generates *2E*, 0 and *-2E* voltage levels of the phase voltage across the load. During the switching states V2 and V7, this topology generates middle voltage levels *–E* and *E* respectively. Charging or discharging of $C_f$ depends on the switch states $X_1$ and $X_3$. During the switching states V2 and V7, the operation principles of the five-level ANPC converter topology are similar to the three-level FC converter topology but in the three-level FC converter topology the DC bus is connected to the load through the floating capacitor in order to generate zero output phase voltage.

During switching states V3 and V6, the neutral point of the five-level ANPC converter topology is connected to the load through floating capacitor and during these states, this topology generates middle voltage levels *–E* and *E* respectively. In switching state V3 the values of S1, S3 are 0, 1 and in switching state V6 the value of S1, S3 are 1, 0 respectively. The voltage deviation at the neutral point NP can be controlled by using the switching state V3 and V6 for same time interval during each fundamental period such that the time interval of charging and discharging of $C_f$ is equal and the average variation of voltage across the floating capacitor is zero.

The direction of the flow of current through different conducting elements depends on the direction of load current ($I_{load}$). The following discussion is about the conduction of different elements for different switching states when $I_{load}>0$

(a) Switching state V1: During this state the current flows through the conducting elements D8, D4 and D2 as mentioned in Table 2.
(b) Switching state V2: In this state the current flows through the conducting elements D8, D4 and S1 as

mentioned in Table 2. During this state $C_f$ discharges.

(c) Switching state V3: In this state the current flows through the conducting elements D6, D2 and S3 as mentioned in Table 2. During this state $C_f$ charges.

(d) Switching state V4: During this state the current flows through the conducting elements D6, S3 and S1 as mentioned in Table 2.

(e) Switching state V5: During this state the current flows through the conducting elements D4, D2 and S7 as mentioned in Table 2.

(f) Switching state V6: In this state the current flows through the conducting elements D4, S7 and S1 as mentioned in Table 2. During this state $C_f$ discharges.

(g) Switching state V7: In this state the current flows is through the conducting elements D2, S5 and S3 as mentioned in Table 2. During this state $C_f$ charges.

(h) Switching state V8: During this state the current flows through the conducting elements S5, S3 and S1 as mentioned in Table 2.

| Switching State | Conducting elements when $I_{load} > 0$ | Conducting elements when $I_{load} < 0$ |
|---|---|---|
| V1 | D8, D4 and D2 | S8, S4 and S2 |
| V2 | D8, D4 and S1 | S8, S4 and D1 |
| V3 | D6, D2 and S3 | S6, S2 and D3 |
| V4 | D6, S3 and S1 | S6, D3 and D1 |
| V5 | D4, D2 and S7 | S4, S2 and D7 |
| V6 | D4, S7 and S1 | S4, D7 and D1 |
| V7 | D2, S5 and S3 | S2, D5 and D3 |
| V8 | S5, S3 and S1 | D5, D3 and D1 |

TABLE 2. CONDUCTING ELEMENTS FOR EACH SWITCHING STATE MAPPED AGAINST THE SWITCHING STATES AS SHOWN IN TABLE 1.

*2. 3 The five-level SHE-PWM waveform*

The five-level SHE-PWM strategy is proposed in [11] where seventeen angles were considered for the first quarter wave cycle of the line-to-neutral voltage waveform as shown in Figure 3. In a generalized form, the set of equations that need to be solved is as follows:

$$M = \sum_{i=1}^{k}\left((-1)^{i-1}\cos(\alpha_i)\right) + \sum_{i=k+1}^{k+m}\left((-1)^{i-(1+k)}\cos(\alpha_i)\right) \quad (4)$$

$$0 = \sum_{i=1}^{k}\left((-1)^{i-1}\cos(5\alpha_i)\right) + \sum_{i=k+1}^{k+m}\left((-1)^{i-(1+k)}\cos(5\alpha_i)\right) \quad (5)$$

$$\vdots$$

$$0 = \sum_{i=1}^{k}\left((-1)^{i-1}\cos(n\alpha_i)\right) + \sum_{i=k+1}^{k+m}\left((-1)^{i-(1+k)}\cos(n\alpha_i)\right) \quad (6)$$

Where

$$n = 3N - 2 \quad (7)$$

$$0 \le M \le 2 \quad (8)$$

If $V_1$ is the amplitude of the fundamental component to be generated, then

$$V_1 = \frac{4M}{\pi} \quad (9)$$

$$0 \le \alpha_1 \le \alpha_2 \le \ldots\ldots\ldots \alpha_i \le \alpha_{k+m} \le \frac{\pi}{2} \quad (10)$$

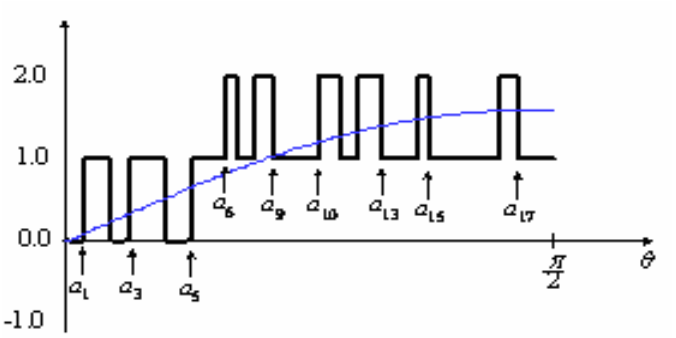


Figure 3. A five-level defined (line-to-neutral) SHE-PWM waveform shown for a distribution ratio of 5/12.

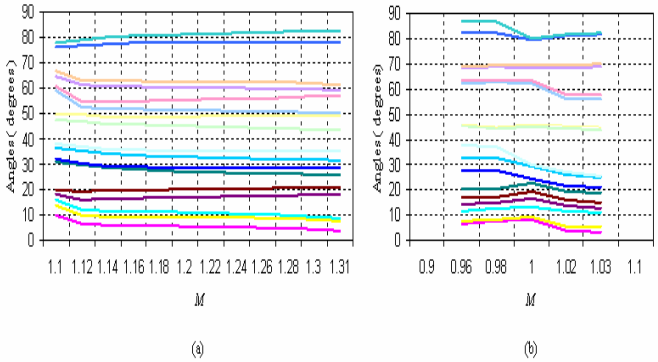


Figure 4. Switching angles for ratios (a) 5/12 ($1.1 \le M \le 1.31$) (b) 9/8 ($0.96 \le M \le 1.03$) [11].

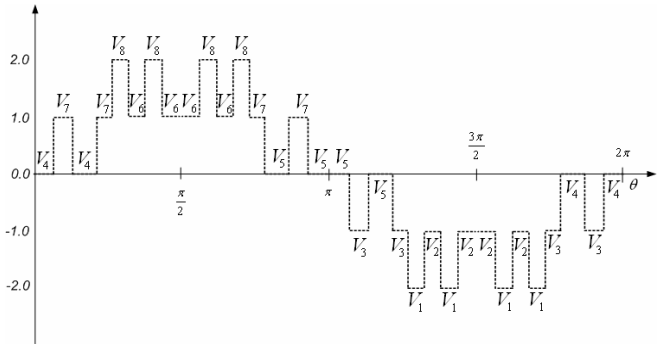


Figure 5. Switching pattern for multiple angles SHE-PWM method ($k$ = 3/4).

By solving the above set of transcendental equations (4)-(6), angles for different ratios of *k/m* are obtained. The value of *k* is odd and the value of *m* is even. The total sum of *k* and *m* must always be equal to the maximum switching transitions. In this case the maximum switching transitions *N*=17 for different *k/m* ratios are shown in Figure 4. The switching angles obtained for all the modulation indices are between zero and 90 degrees following the constraints of eqn. (10). This makes certain that by reflection of these angles we

obtained a line-to-neutral waveform in which $N$-1 harmonics are eliminated other than the triplen harmonics. The switching pattern shown in Figure 5 is implemented in this paper. The states V4 and V5 mentioned in Table 1[6] are defined in such a way that there is no change in switching states at 0 and π. The switching transitions of the switches S1, S2, S3, and S4 is 2$N$ and the switching transition of the switches S5, S6, S7 and S8 is 2$k$.

## 3. Simulation Results

In this section the above mentioned techniques are implemented to confirm their suitability for the five-level ANPC converter topology. The three-phase five-level ANPC converter with power rating 2MVA and 4.0kV DC link voltage is considered. The floating capacitor value is chosen to be 400μF. Some of the solutions obtained from the five-level symmetrically defined SHE-PWM method (Figure 4) are implemented in the three-phase five-level ANPC converter topology. In Figure 6 the charging or discharging of the floating capacitor is observed at the middle voltage levels of the line-to-neutral voltage of phase A ($E_A$) and it is also observed that $E_A$ is deviating from zero due to the variation of the neutral point voltage. Due to the variation in the neutral point voltage, it is noticed that in the harmonic spectrum of line-to-line voltage of phase A and phase B ($E_{AB}$) there are small amounts of lower order harmonics. The SHE-PWM method implemented in this paper can eliminate harmonics up to the 49$^{th}$ harmonic. The 51st harmonic happens to be a multiple of three which is cancelled out in a three-phase system for the line-to-line voltage waveforms. If the voltage across the floating capacitor is maintained constant, as shown in Figure 8, the frequency spectrum shown in Figure 9 is almost a clear spectrum till the 53rd harmonic. Also it is observed that the magnitude of fundamental line-to-neutral voltage in Figure 9 is higher than the fundamental line-to-neutral voltage in Figure 7. The variation of the neutral point voltage would effect the fundamental line-to-neutral voltage output.

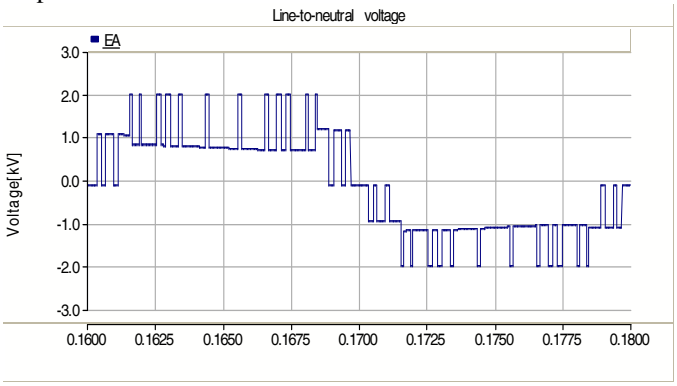


Figure 6. The line-to-neutral voltage of phase A ($E_A$) across the Y-connected load for 5/12 SHE-PWM pattern, $M$=1.16.

Figure 10 represents the harmonic spectrum of the $E_{AB}$ across the Y-connected load for 9/8 SHE-PWM pattern contains lower order harmonics in small amounts because of the variation in voltage at neutral point. The variation of the neutral point voltage can be controlled by using the switching state V3 and V6 for same time interval during each fundamental period such that the time interval of charging and discharging of $C_f$ is equal. From Figure 11 it is observed that if the voltage across the floating capacitor is maintained constant, the harmonic spectrum of $E_{AB}$ across the Y-connected load is clear spectrum till the 53rd harmonic.

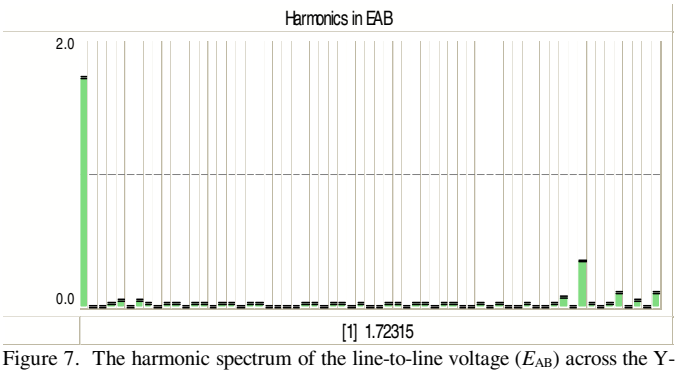


Figure 7. The harmonic spectrum of the line-to-line voltage ($E_{AB}$) across the Y-connected load for 5/12 SHE-PWM pattern, $M$= 1.16.

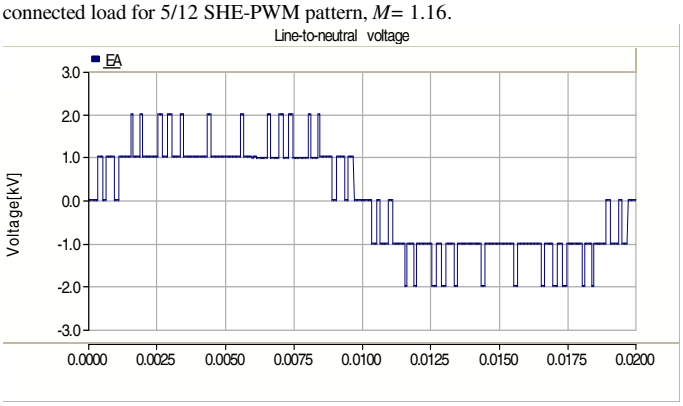


Figure 8. The $E_A$ across the Y-connected load when the floating capacitor is replaced by DC voltage source of 1.0kV for 5/12 SHE-PWM pattern, $M$=1.16.

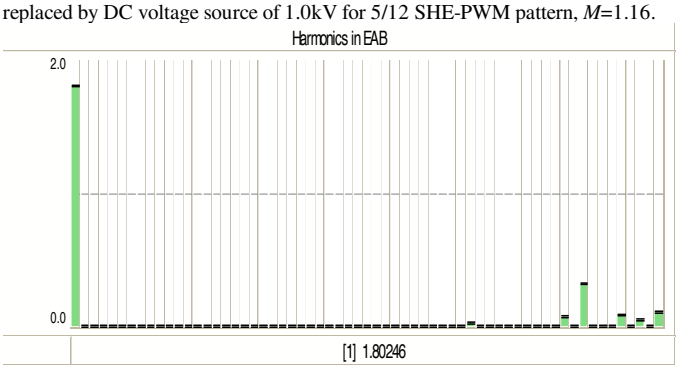


Figure 9. The harmonic spectrum of $E_{AB}$ across the Y-connected load when the floating capacitor is replaced by DC voltage source of 1.0 kV for 5/12 SHE-PWM pattern, $M$= 1.16.

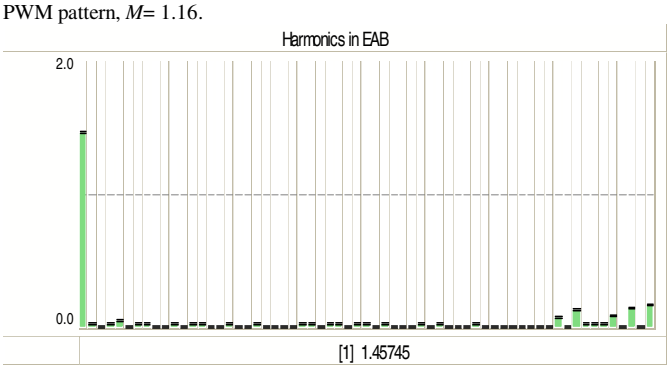


Figure 10. The harmonic spectrum of $E_{AB}$ across the Y-connected load for 9/8 SHE-PWM pattern, $M$= 0.96.

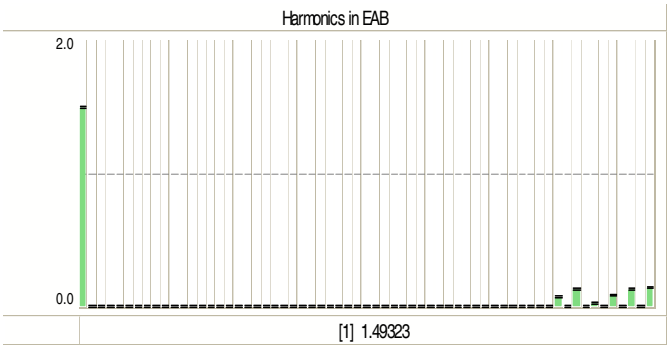


Figure 11. The harmonic spectrum of $E_{AB}$ across the Y-connected load when the floating capacitor is replaced by a DC voltage source of 1.0kV for 9/8 SHE-PWM pattern, $M$= 0.96.

## 4. CONCLUSION

The five-level three-phase ANPC converter topology has potential in high-power high-voltage power electronic systems not only for motor drives applications but also utility apparatus such as STATCOMs and FACTS in general. The simulation results presented in this paper confirmed that the novel five-level symmetrically defined SHE-PWM method can be implemented successfully in the said topology**.**

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Dr. Agelidis received the Advanced Research Fellowship from the United Kingdom's Engineering and Physical Sciences Research Council (EPSRC-UK) in 2004. He was the Vice President Operations within the IEEE Power Electronics Society for 2006-2007. He was an Associate Editor of the IEEE POWER ELECTRONICS LETTERS from 2003 to 2005, and served as the PELS Chapter Development Committee Chair from 2003 to 2005. He is currently an AdCom member of IEEE PELS for 2007-2009. He will be the Technical Chair of the 39th IEEE PESC'08, Rhodes, Greece.