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SHE-PWM switching strategies for active neutral point clamped multilevel converters

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Abstract

The main drawback of the diode neutral-point-clamped (NPC) converter is the unequal loss distribution among the semiconductor devices which confines the maximum output power and the switching frequency. To address this drawback, switching state redundancy is required to evenly distribute the losses and can be achieved differently as the level of the converter changes. For instance, the three-level active NPC (3L-ANPC) converter has switching state redundancy and is derived from the 3L-NPC converter by adding an anti-parallel switch to the clamping diodes; in the 4L-ANPC converter, the combination of a 2L converter and a 3L-ANPC converter is used; in a 5L-ANPC converter, the combination of the 3L-ANPC and 3L-flying capacitor (FC) converter is advantageous. The paper discusses selective-harmonic-elimination (SHE) pulse-width-modulation (PWM) strategies for the above mentioned converters and explains how loss distribution can be achieved.

Keywords

switching, pwm, converters, she, multilevel, clamped, point, neutral, active, strategies

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SHE-PWM Switching Strategies for Active Neutral Point Clamped Multilevel Converters

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***Abstract*- The main drawback of the diode neutral-point-clamped (NPC) converter is the unequal loss distribution among the semiconductor devices which confines the maximum output power and the switching frequency. To address this drawback, switching state redundancy is required to evenly distribute the losses and can be achieved differently as the level of the converter changes. For instance, the three-level active NPC (3L-ANPC) converter has switching state redundancy and is derived from the 3L-NPC converter by adding an anti-parallel switch to the clamping diodes; in the 4L-ANPC converter, the combination of a 2L converter and a 3L-ANPC converter is used; in a 5L-ANPC converter, the combination of the 3L-ANPC and 3L-flying capacitor (FC) converter is advantageous. The paper discusses selective-harmonic-elimination (SHE) pulse-width-modulation (PWM) strategies for the above mentioned converters and explains how loss distribution can be achieved.**

***Index Terms*— Selective harmonic elimination, pulse-width modulation, neutral point clamped converter, active neutral point clamped converter, three-level converter, four-level converter, five-level converter, floating capacitor converter**.

I. INTRODUCTION

Multilevel converters have made revolutionary changes in the utilization of power electronics in high-voltage and high-power applications. The basic concept involves generating output AC waveforms from small voltage steps by using series connected capacitors or isolated dc sources. The small voltage steps in the output voltage produce lower harmonic distortion, lower *dv/dt*, lower electromagnetic interference (EMI) and higher efficiency when compared with the conventional two-level (2L) voltage source converter (VSC).

One key multilevel converter topology is the well-known neutral-point clamped (NPC) converter [1], [2]. However, the unequal distribution of losses among semiconductor devices generates also an unequal junction temperature distribution which confines the converter maximum output power and the switching frequency [3], [4]. The unequal loss distribution in the 3L-NPC converter reduces its maximum output power which is less when compared to the 3L-flying capacitor (FC) converter [5] operating at the same switching frequency [6]. The reason being is that the 3L-FC converter offers equal loss distribution among semiconductors. Moreover, as the levels of the NPC converter increase, the voltage unbalances between the series capacitors need attention [7] which can be solved by separate DC sources or by voltage regulators for each level.

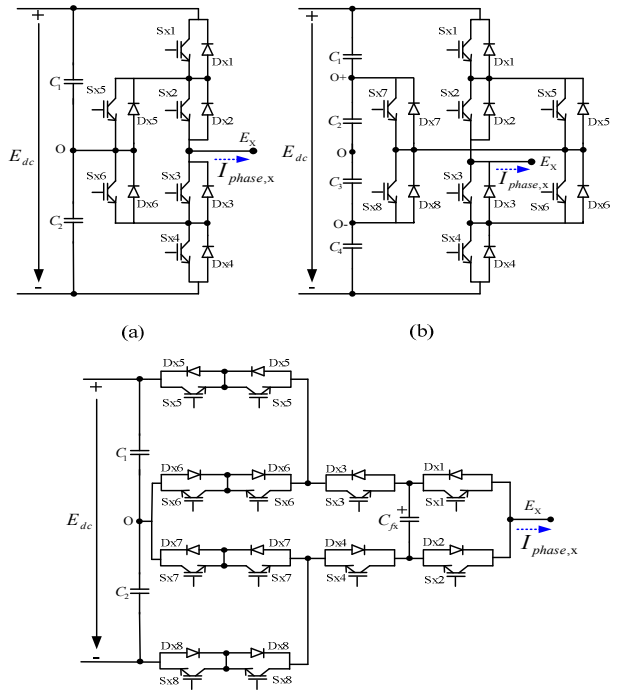

Fig. 1: Converter phase-leg of: (a) three-level ANPC converter (b) four-level ANPC converter [11] (c) five-level ANPC converter [12]

The above mentioned method is not suitable for many applications because extra isolation transformers and switching devices are necessary [7]. As the level of the FC converter increases a number of issues related to the large capacitor banks, additional pre-charging circuitry, complex control and voltage unbalance among the flying capacitors need to be addressed [8].

The 3L-ANPC converter [3], [4], [9], [10] offers opportunities for even loss distribution and is derived from the 3L-NPC converter [2] by adding an anti-parallel switch to each clamping diode (Fig. 1(a)). Specifically, in [9] the switch was introduced to ensure the equal voltage sharing between the main and the auxiliary switches. Reference [10] proposed a different switching control strategy which reduces the cost of the converters used in HVDC applications. The switch connected to the neutral point creates more switching states which are utilized to distribute the switching losses in 3L-ANPC converter phase-leg for various operating conditions in

medium voltage applications [3], [4]. However, in order to improve the distribution of losses across the devices of the multilevel converter and to increase the level of the converter topology to higher than three-levels, different combinations of converter topologies can be considered. The resulting topologies include the combination of a 2L conventional and a 3L-ANPC converter to construct the 4L-ANPC converter (Fig. 1(b)) [11]; the combination of a 3L-ANPC converter and a 3L-FC converter to make the 5L-ANPC converter (Fig. 1(c)) [12]. These converters offer the desired switching state redundancy.

In this paper, the selective-harmonic-elimination (SHE) pulse-width-modulation (PWM) [13], [14], [15] strategies are considered. The number of switching transitions per fundamental cycle decreases in SHE-PWM when compared to the well-known carrier-based PWM for the same bandwidth and hence associated converter switching losses will decrease. By implementing SHE-PWM technique in 3L-, 4L- and 5L-ANPC converters the distribution of losses among the semiconductor devices can be improved and this will increase the output power of the converter for the same bandwidth in comparison to carrier-based PWM control.

This paper is organized as follows. Section II presents the different level ANPC converters and the commutations between various redundant switching states to distribute the switching losses. Section III discusses the novel symmetrically defined SHE-PWM control strategies for various modulation indices. Simulation results based on the novel symmetrically defined SHE-PWM control strategies are presented in Section IV and finally, conclusions are summarized in Section V.

II. ANPC CONVERTER TOPOLOGIES

A. 3L-ANPC converter

The 3L-ANPC converter is shown in Fig. 1(a) [2]. The subscript 'x' represents the three phases 'A', 'B' and 'C'. The current and voltage ratings of the switches Sx5 and Sx6 should be the same as that of the Sx1, Sx2, Sx3 and Sx4. During the switching state V1, Sx1 and Sx2 are turned ON due to which phase 'x' connects to the positive rail of the dc link producing the line-to-neutral voltage equal to $+E_{dc}/2$ assuming the voltages across the capacitors C_1 and C_2 are equal to $E_{dc}/2$. During this switching state Sx6 is turned ON to ensure an equal voltage between the switches Sx3 and Sx4. During switching state V6, Sx3 and Sx4 are turned ON due to which the phase "x" connects to the negative rail of the dc link producing the line-to-neutral voltage equal to $-E_{dc}/2$. During the state V6, Sx5 is turned ON to ensure an equal voltage between Sx1 and Sx2. The switches Sx5 and Sx6 create four possible switching states, i.e., V2, V3, V4 and V5. During these states the phase "x" connects to the neutral point 'O' producing zero line-to-neutral voltage. The four zero switching states (V2, V3, V4 and V5) in this converter can be used to evenly distribute the switching losses within each phase-leg. In Table 2, the semiconductor devices undergoing switching losses during various commutations at positive phase current are shown. The symbol '↔' in Table 2 indicates the direction of the commutation from one switching state to another switching state and vice-versa

Switching state	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Phase voltage
V1	1	1	0	0	0	1	$+E_{dc}/2$
V2	0	1	0	0	1	0	0
V3	0	1	0	1	1	0	0
V4	1	0	1	0	0	1	0
V5	0	0	1	0	0	1	0
V6	0	0	1	1	1	0	$-E_{dc}/2$

Table 1: Switching states of output phase voltage levels for 3L-ANPC converter.

Commutation	S	D	S	D	S	D	S	D	S	D	S	D
	x1		x2		x3		x4		x5		x6	
Positive Phase Current												
V1↔ V2	×									×		
V1↔ V3	×									×		
V1↔ V4			×			×						
V1↔ V5	×					×						
V2↔ V6			×					×				
V3↔ V6			×			×						
V4↔ V6								×			×	
V5↔ V6								×			×	

Table 2: The semiconductor devices in 3L-ANPC converter undergoing switching losses during different commutations at positive phase current.

Considering the output phase current to be positive and when the commutation takes place from switching state V1 to V2 (V1→V2), the output phase current commutates through the upper neutral path. During this commutation Sx1 experiences turn OFF losses. During commutation V2→V1, the diode Dx5 experiences the recovery losses and switch Sx1 experiences turn ON losses. The commutation V1→V3 differs from the commutation V1→V2 only by turning ON the switch Sx4 which does not influence the commutation of phase current. During this commutation Sx1 experiences turn OFF losses. During commutation V3→V1, the diode Dx5 experiences recovery losses and switch Sx1 experiences turn ON losses. When commutation V1→V4 takes place, the output phase current commutates through the lower neutral path. During the commutation V1→V4, Sx2 experiences turn OFF losses and during commutation V4→V1, diode Dx3 experiences the recovery losses and switch Sx2 experiences turn ON losses. During the commutation from V1→V5, Sx1 experiences turn OFF losses and during commutation V5→V1, diode Dx3 experiences the recovery losses and switch Sx1 experiences turn ON losses. Similarly when the commutations between the zero switching states (V2, V3, V4, and V5) and the switching state V6 take place, the semiconductor devices experiencing losses are shown in Table 2.

B. 4L-ANPC converter

The 4L-ANPC converter is obtained by the combination of a 2L conventional and a 3L-ANPC converter as shown in Fig. 1(b)[11]. The converter phase-leg consists of eight switches (Sx1 to Sx8) with anti-parallel diodes connected across them. This converter has four dc-link capacitors which are charged to the voltage of $E_{dc}/4$, which is different from the conventional four-level diode-clamped converter with three dc-link capacitors. The converter has twelve switching states as shown in Table 3. The subscript 'O' in Fig. 1(b) represents the neutral point of this converter which is common point between the

capacitors C_2 and C_3. During the switching states V1, V2 and V3 the phase 'x' connects to the positive rail of the dc link producing the line-to-neutral voltage equal to $+E_{dc}/2$. The switching states V2 and V3 are used to reduce the switching losses during commutations V2↔V4, V2↔V5 and V3↔V6. During the switching states V4, V5 and V6 the phase 'x' connects to the dc link at 'O+' node producing the line-to-neutral voltage of $+E_{dc}/4$. During the switching states V7, V8 and V9 the phase 'x' connects to the dc link at 'O-' node producing the line-to-neutral voltage of $-E_{dc}/4$. During the switching states V10, V11 and V12 the phase 'x' connects to the negative rail of the dc link producing the line-to-neutral voltage of $-E_{dc}/2$. The switching strategy with combination of switching states V1, V4, V8 and V10 are discussed from now on since the distribution of losses in this switching strategy is uniform among the semiconductor devices [11]. Table 4 shows the semiconductor devices that experience the switching losses for different commutations during this switching strategy.

Considering positive output phase current and when the commutation takes place from switching state from V1 to V4 (V1→V4), the switch Sx1 experiences turn OFF losses. When V4→V1 takes place, the diode Dx5 experiences recovery losses and the switch Sx1 experiences turn ON losses. During V4→V8, the switches Sx2 and Sx7 experience turn OFF losses, the switch Sx6 experiences turn ON losses and the diode Dx5 experiences the recovery losses. During V8→V4, the diodes Dx3 and Dx8 experience the recovery losses, the switch Sx6 experiences turn OFF losses and the switches Sx7 and Sx2 experience turn ON losses. During V8→V10, the diode Dx8 experiences the recovery losses. During V10→V8, the diode Dx4 experiences the recovery losses.

State	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Sx7	Sx8	Phase voltage
V1	1	1	0	0	0	0	0	0	$+E_{dc}/2$
V2	1	1	0	0	0	0	1	0	$+E_{dc}/2$
V3	1	1	0	0	0	1	1	0	$+E_{dc}/2$
V4	0	1	0	0	1	0	1	0	$+E_{dc}/4$
V5	0	0	1	0	0	1	1	0	$+E_{dc}/4$
V6	1	0	1	0	0	1	1	0	$+E_{dc}/4$
V7	0	1	0	0	1	0	0	1	$-E_{dc}/4$
V8	0	0	1	0	0	1	0	1	$-E_{dc}/4$
V9	0	1	0	1	1	0	0	1	$-E_{dc}/4$
V10	0	0	1	1	0	0	0	0	$-E_{dc}/2$
V11	0	0	1	1	0	0	0	1	$-E_{dc}/2$
V12	0	0	1	1	1	0	0	1	$-E_{dc}/2$

Table 3: Switching states of output phase voltage levels for 4L-ANPC converter.

Commutation	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D
	x1		x2		x3		x4		x5		x6		x7		x8	
Positive Phase Current																
V1↔ V4	×									×						
V4↔ V8			×			×				×	×		×			×
V8↔ V10								×								×

Table 4: The semiconductor devices in 4L-ANPC converter undergoing switching losses during different commutations at positive phase current.

State	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Sx7	Sx8	Phase voltage
V1	0	1	0	1	0	1	0	1	$-E_{dc}/2$
V2	1	0	0	1	0	1	0	1	$-E_{dc}/4$
V3	0	1	1	0	0	1	0	1	$-E_{dc}/4$
V4	1	0	1	0	0	1	0	1	0
V5	0	1	0	1	1	0	1	0	0
V6	1	0	0	1	1	0	1	0	$+E_{dc}/4$
V7	0	1	1	0	1	0	1	0	$+E_{dc}/4$
V8	1	0	1	0	1	0	1	0	$+E_{dc}/2$

Table 5: Switching states of output phase voltage levels for 5L-ANPC converter.

C. 5L-ANPC converter

The 5L-ANPC converter is the combination of a 3L-ANPC converter and a 3L-FC converter [12] as shown in Fig. 1(c). This combination creates eight switching states as shown in Table 5. Using these states, the five different line-to-neutral voltage levels, namely, $-E_{dc}/2$, $-E_{dc}/4$, 0, $+E_{dc}/4$ and $+E_{dc}/2$ are generated. The phase-leg of the 5L-ANPC converter consists of twelve switches from Sx1 to Sx8 which are connected in anti-parallel to the diodes from Dx1 to Dx8 respectively. For notation Sx5 to Sx8 there are two switches in series with their respective diodes in anti-parallel (Dx5 to Dx8). In the above mentioned switching devices there exist switch pairs that require complementary switching control signals. These switch pairs are: (Sx1, Sx2), (Sx3, Sx4), (Sx5, Sx6) and (Sx7, Sx8). The switching devices (Sx5, Sx7) require same control signals and the switching devices (Sx6, Sx8) require same control signals which are complementary to (Sx5, Sx7) respectively. The charging and discharging of floating capacitor C_{fx} takes place at the middle of the line-to-neutral voltage levels $-E_{dc}/4$ and $+E_{dc}/4$ depending upon the direction of the output phase current. The voltage across the floating capacitor should be maintained at $E_{dc}/4$ which is affected by the switching states V2, V3, V6 and V7. Each switch in 5L-ANPC converter blocks one fourth of the dc-link voltage. The redundancy of switching states in 5L-ANPC converter balances the voltage across the floating capacitor C_{fx}. During the switching state V3 and V6, the neutral point 'O' is connected to the load through the floating capacitor C_{fx} and during this switching states, the voltage deviation at the neutral point 'O' can be controlled by using them for the same time interval during each fundamental period such that the time interval of charging and discharging of C_{fx} is equal so that the average variation of voltage across the floating capacitor is zero. The selection of switching states for the distribution of switching losses in 5L-ANPC converter phase-leg should consider the balancing of voltage across the C_{fx}. In Table 6, the semiconductor devices in 5L-ANPC converter undergoing switching losses during various commutations at positive phase current are shown. Considering the output phase current to be positive and when the commutation V1→V2 takes place, the diode Dx2 and switch Sx1 experience the recovery and turn ON losses respectively. When the commutation V2→V1 takes place, the switch Sx1 experiences turn OFF losses. When the commutation V1→V3 takes place, the diode Dx4 and Dx8 experiences the recovery

losses and switch Sx3 experiences the turn ON losses. During the commutation V3→V1, the diode Dx6 and the switch Sx3 experience the recovery and turn OFF losses respectively. During the commutation V2→V4, the diode Dx4 undergoes recovery losses and when commutation takes place V4→V2, the switch Sx3 undergoes turn OFF losses. During the commutation V2↔V4, the switches Sx6 and Sx8 are always turned ON which reduces the switching losses. When the commutation V2→V5 takes place, the switch Sx1 and diode Dx8 undergo turn OFF and recovery losses respectively. During the commutation V5→V2, the diode Dx2 experiences the recovery losses and the switches Sx1 and Sx7 experiences turn ON and turn OFF losses respectively. During the commutation V3→V4, the diode Dx2 and switch Sx1 experiences the recovery and turn ON losses respectively. During the commutation V4→V3, the switch Sx1 experiences turn OFF losses. When V3→V5 commutation takes place the switches Sx3, Sx7 and the diode Dx6 undergo turn OFF, turn ON and recovery losses respectively. When V5→V3 commutation takes place the switches Sx7, Sx3 and the diode Dx4 undergo turn OFF, turn ON and recovery losses respectively. Similarly the switches which undergo switching losses during the commutation between the switching states V4, V5, V6, V7 and V8 are tabled in Table 6.

Commutation	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D
	x1		x2		x3		x4		x5		x6		x7		x8	
Positive Phase Current																
V1↔ V2	×			×												
V1↔ V3					×			×								
V2↔ V4					×			×								
V2↔ V5	×			×									×			×
V3↔ V4	×			×												
V3↔ V5					×			×								
V4↔ V6					×			×				×	×			
V4↔ V7	×			×					×			×				
V5↔ V6	×			×												
V5↔ V7					×			×								
V6↔ V8					×			×								
V7↔ V8	×			×												

Table 6: The semiconductor devices in 5L-ANPC converter undergoing switching losses during different commutations at positive phase current.

III. SHE-PWM Waveforms For Different Multi-level Converters

The symmetrically defined (line-to-neutral) SHE-PWM waveforms for different multilevel converters are shown in Fig. 2. A set of different combinations of non-linear transcendental equations that contain trigonometric terms are solved to obtain the multiple sets of solutions for different symmetrically defined multilevel waveforms shown in Fig. 2. A generalized formula of SHE-PWM suitable for high-power high-voltage multilevel converters is proposed in [14]. The three-level symmetrically defined SHE-PWM (line-to-neutral) unipolar waveform is shown in Fig. 2(a). The number of total switching angles within the first quarter cycle of the fundamental period is considered to be N=7 for all symmetrically defined SHE-PWM waveforms for different multilevel converters as shown in Fig. 2. In order to obtain optimal switching angles, the non-linear transcendental equations are subjected to the constraint given by (1) where $\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5, \alpha_6$ and α_7 are the switching angles. The four-level symmetrically defined SHE-PWM (line-to-neutral) waveform is shown in Fig. 2(c), the number of levels of the waveform is assumed to be four, i.e., 1p.u., 0.5p.u., --5p.u. and -1p.u. The number of switching transitions angles placed between the -0.5p.u. level and the 0.5p.u. level are two (k =2). The number of switching transitions placed between the 0.5p.u. level and the 1p.u. level are five (m=5). The value of m could be odd or even which will depend on the total number of switching transitions per quarter cycle of the fundamental period N=k+m=7. The value of k is always even in this case. In four-level symmetrically defined SHE-PWM strategy when the modulation index M ranges between 0 and 0.5, the line-to- neutral waveform is a bipolar in nature as shown in Fig. 2(b).

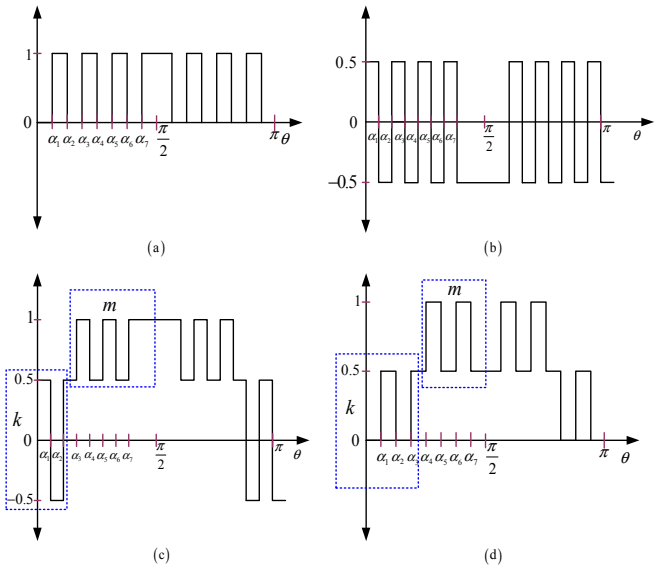

Fig. 2: (a) three-level symmetrically defined (line-to-neutral) SHE-PWM waveform (b) four-level symmetrically defined (line-to-neutral) SHE-PWM waveform which is bipolar waveform for low modulation index (0<M<0.5) (c) four-level symmetrically defined (line-to-neutral) SHE-PWM waveform for high modulation index (0.5<M<1) shown for a distribution ratio of 2/5 (d) five-level symmetrically defined (line-to-neutral) SHE-PWM waveform shown for a distribution ratio of 3/4.

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \quad (1)$$

The symmetrically defined five-level SHE- PWM strategy waveform is shown in Fig. 2(d). The number of levels of the waveform is assumed to be five, i.e., 1 p.u., 0.5p.u., 0p.u., -0.5p.u. and -1p.u. The number of switching transitions (angles) placed between the 0p.u. level and the 0.5p.u. level are three (k =3). The number of switching transitions placed between the 0.5p.u. level and the 1p.u. level are four (m=4). The value of m can be odd or even will depend on the total number of switching transitions per quarter cycle of the fundamental period N=k+m=7. The value of k is always odd. In five-level symmetrically defined SHE-PWM strategy when the modulation index M ranges between 0 and 0.5, the line-to-neutral waveform is unipolar in nature. Selected optimal switching angles, which are used in simulation study, for 3L-

ANPC converter, 4L-ANPC converter and 5L-ANPC converter whose modulation index M ranges between 0.7 and 0.9 are shown in Figs. 3(a), 3(c) and 3(d) respectively. Fig. 3(b) shows the optimal switching angles for 4L-ANPC converter whose modulation index varies between 0.06 and 0.5.

IV. Simulation Results

For the purpose of a meaningful comparison, the number of switching angles per quarter cycle are considered to be $N = 7$ and the rated output apparent power 330MVA is chosen for all different converters presented in this paper. The RMS line-to-line voltage is considered to be 220kV. Assuming the constant E_{dc}, the commutation voltages of the switches normalized to E_{dc} for all multilevel ANPC converters are tabled in Table 7. The simulations are carried out in MATLAB/SIMULINK® [17].

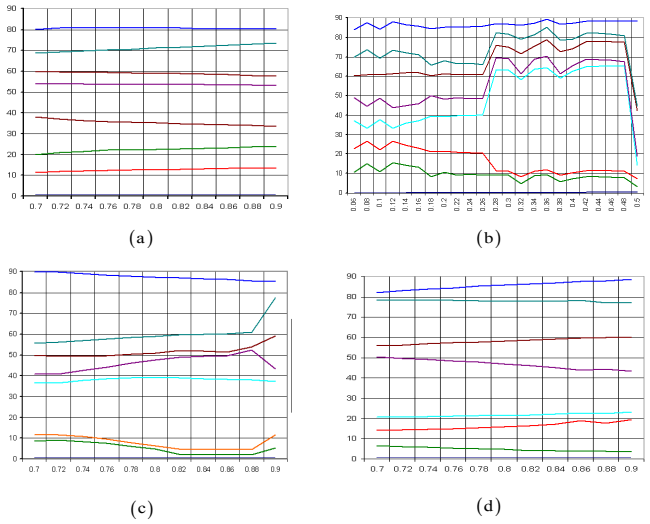

Fig. 3: Switching angles in degrees versus modulation index M for N=7. (a) three-level switching angles for modulation index (0.7<M<0.9), (b) four-level switching angles for low modulation index (0.06<M<0.5) (c) four-level switching angles for high modulation index (0.7<M<0.9), for a distribution ratio of 2/5 (d) five-level switching angles for modulation index (0.7<M<0.9), for a distribution ratio of 3/4.

The switching strategy with combinations of switching states V1, V2, V4 and V6 such that the commutations V1↔V2, V1↔V4 and V2↔V6, V4↔V6, take places alternatively is utilized in simulations for 3L-ANPC converter. This type of commutation arrangement leads to distribution of the switching losses among the semiconductor devices is referred in [3]. The normalized switching frequency of the switches for different ANPC converter using particular switching strategy is tabled in Table 8. The harmonic spectra of line-to-line voltage normalized with its fundamental line-to-line voltage at M=0.84 is shown in Fig. 5. By applying SHE-PWM strategy to 3L-ANPC converter the harmonic until 23rd are eliminated with less switching frequency which will reduce the switching losses in this converter. According to [10], the implementation of

Converter topology	3L-ANPC	4L-ANPC	5L-ANPC
Commutation voltage	0.5 p.u.	0.25 p.u.	0.25 p.u.

Table 7: Commutation voltage for all considered multilevel ANPC converters.

Switches	Switching frequency in p.u.		
	3L-ANPC	4L-ANPC	5L-ANPC
Sx1	8	5	9
Sx2	8	5	9
Sx3	8	5	9
Sx4	7	5	9
Sx5	8	10	1
Sx6	8	10	1
Sx7	-	10	1
Sx8	-	10	1

Table 8: The normalized switching frequency experienced by switches in different ANPC converters.

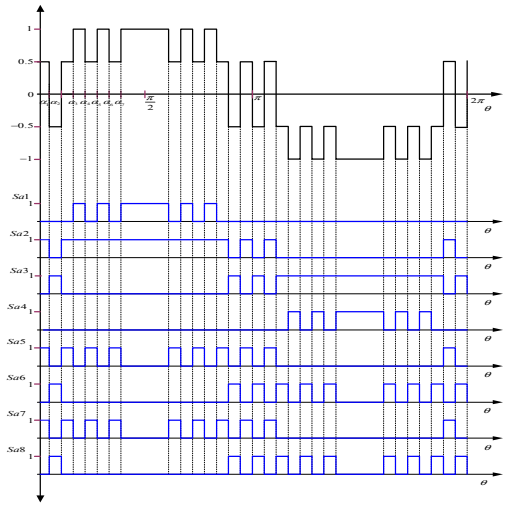

Fig. 4. Distribution of switching signals for switches in phase-leg of the 4L-ANPC converter.

SHE-PWM method for 3L-ANPC converter in HVDC applications is more suitable since the switching frequency of the clamping switches is similar to other switches in the converter. At same switching frequency, the frequency bandwidth of line-to-line voltage obtained is higher when compared to carrier-based PWM strategy. The control strategy implemented to control the voltage across the dc-link capacitors is not discussed in this paper. In Fig. 6, the normalized voltage across the dc-link capacitors is shown.

In 4L-ANPC converter, the switching strategy utilizes combination of switching states V1, V4, V8 and V10 to distribute the switching losses among the switches uniformly. The distribution of switching signals in phase-leg of 4L-ANPC converter for above mentioned switching strategy is shown in Fig. 4. The switching frequency of the clamping switches in 4L-ANPC converter is higher than other switches in the converter as shown in Table 8. According to [10], the switching strategy implemented for 4L-ANPC converter is not suitable for HVDC applications. The harmonic spectra of line-to-line voltage normalized with its fundamental line-to-line voltage at M=0.84 is shown in Fig. 7. The harmonic spectrum of line-to-line voltage has low order harmonics as shown in Fig. 7. In Fig 8, the normalized voltage across the dc-link capacitors is shown. The voltage across the dc-link capacitors is controlled by self-voltage balancing circuit [11].

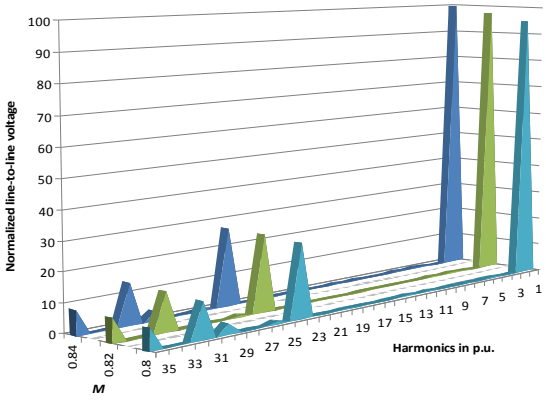

Fig. 5: The harmonic spectra of the normalized line-to-line voltage at various modulation indices for 3L-ANPC converter, power factor =0.8 (lagging)

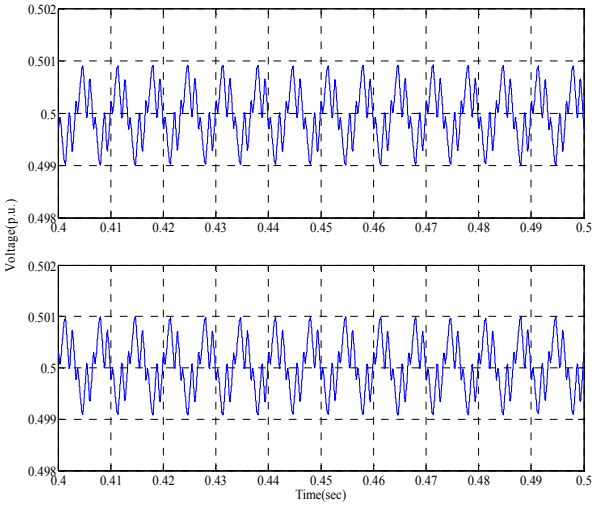

Fig 6: The normalized voltage across dc-link capacitors C_1 (top) and C_2 (bottom) in 3L-ANPC converter at power factor equal to 0.8 (lagging) and M=0.8.

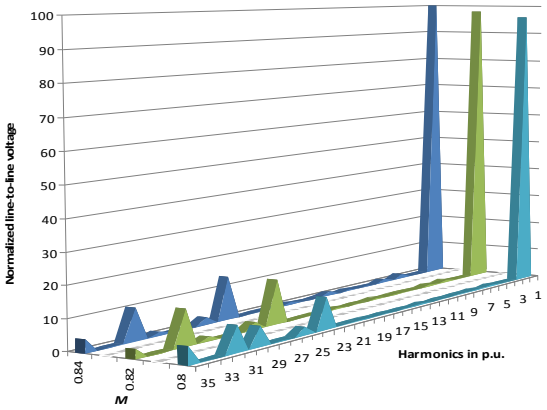

Fig. 7: The harmonic spectra of the normalized line-to-line voltage at various modulation indices for 4L-ANPC converter, distribution ratio=2/5, power factor =0.8 (lagging).

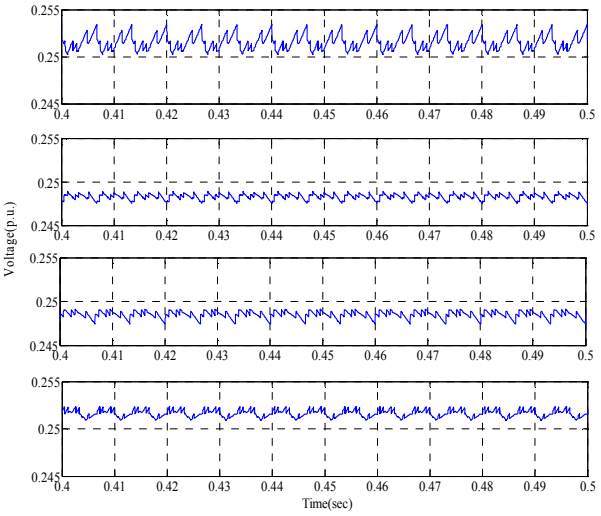

Fig. 8: The normalized voltage across dc-link capacitors C_1 (top), C_2 (middle top) C_3 (middle bottom) and C_4 (bottom) in 4L-ANPC converter at power factor equal to 0.8 (lagging) and M=0.8.

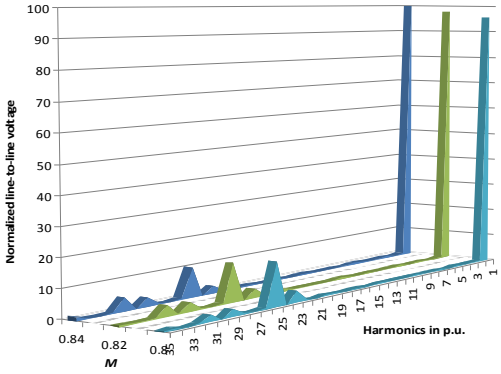

Fig. 9: The harmonic spectra of the normalized line-to-line voltage at various modulation indices for 5L-ANPC converter, distribution ratio=3/4, power factor =0.8 (lagging).

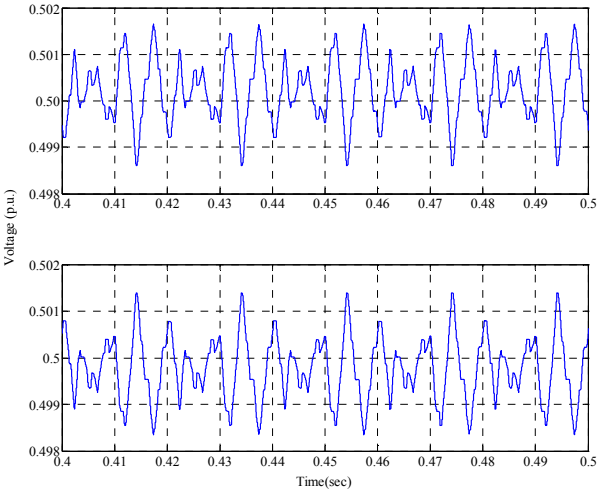

Fig. 10: The normalized voltage across dc-link capacitors C_1 (top) and C_2 (bottom) in 5L-ANPC converter at power factor equal to 0.8 (lagging) and M=0.8.

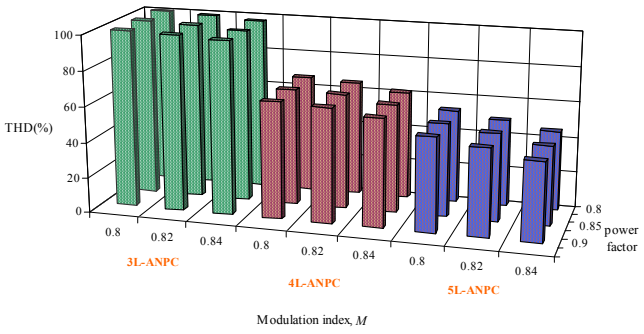

Fig. 11: The relative total harmonic distortion of the line-to-line voltage for the different level ANPC converters for different load power factors (lagging).

In comparison, the total harmonic distortion (THD) of 4L-ANPC converter is lower than the THD of 3L-ANPC converter as shown in Fig. 11. The major disadvantage of 4L-ANPC converter is non-zero line-to-neutral voltage at M=0 which is applicable for all converters with even number of voltage levels [11].

In 5L-ANPC converter, the implemented switching strategy considers the switches Sx5, Sx6, Sx7 and Sx8 to experience one switching transition in fundamental period. The switches Sx1, Sx2, Sx3 and Sx4 are turned ON and turn OFF to generate the five different output phase voltage levels. The voltage across floating capacitor C_{fx} is assumed to be constant whose voltage is quarter of the dc-link voltage. According to [10], the implementation of SHE-PWM method for 5L-ANPC converter in HVDC applications is suitable. A dedicated control strategy is required in order to control the neutral point voltage and the voltage across floating capacitors. The harmonic spectra of line-to-line voltage normalized with its fundamental line-to-line voltage at M=0.84 is shown in Fig. 9. In Fig. 10, the normalized voltage across the dc-link capacitors is shown. The relative THD of the line-to-line voltage is determined by normalizing the THD of 3L-ANPC, 4L-ANPC and 5L-ANPC converters to the THD of the 3L-ANPC converter at M=0.8 for respective power factor (lagging) as shown in Fig. 11. The 5L-ANPC converter has less THD when compare to the 4L-ANPC and 3L-ANPC converters.

V. Conclusion

The active neutral-point clamped multilevel converters offer redundant switching states which can be utilized to distribute the switching losses among the semiconductor devices. The novel symmetrically defined SHE-PWM strategies are implemented successfully in 3L-ANPC, 4L-ANPC and 5L-ANPC converters. It is confirmed that by implementing SHE-PWM strategy, the number of switch transitions per fundamental cycle decreases which will results in reduced switching losses. The application of SHE-PWM in ANPC converters will distribute the reduced switching losses. Therefore, the converter rated output phase current can be increased which will increase the apparent output power at constant output line-to-line voltage.

The implementation of SHE-PWM method for 3L-ANPC and 5L-ANPC converters confirms their suitability in HVDC applications. Due to high switching frequency in clamping switches of 4L-ANPC converter, the switching losses in clamping switches would increase which would limit the output power of the converter.

VI. References

[1] R. H. Baker, "Bridge converter circuit", U.S. Patent 4 270 163, May 26, 1981.

[2] A.Nabae, I. Takahashi, and H.Akagi, "A new neutral-point-clamped PWM inverter", *IEEE Trans. on Ind. Appl.*, vol. 17, no. 5, pp. 518-523, Sept. /Oct. 1981.

[3] T. Bruckner and S. Bernet, "Loss balancing in three-level voltage source inverters applying active NPC switches", in *Proc. IEEE Power Electron. Spec. Conf (PESC' 01)*, Vancouver, BC, Canada, 2001, pp. 1135-1140.

[4] T. Bruckner, S. Bernet and P.Steimer, "Feedforward loss control of three-level Active NPC Converters", *IEEE Trans. on Ind. Appl.*, vol. 43, no. 6, pp. 1588-1596, Dec. 2007.

[5] T.A. Meynard and H. Foch, "Multilevel conversion: High voltage choppers and voltage source inverters", in *Proc. of IEEE Power Electron. Spec. Conf, (PESC'92)*, pp. 397-403.

[6] D.Krug, S.Bernet and S.Dieckerhoff, "Comparison of state-of-the-art voltage source converter topologies for medium voltage applications", in *Proc. of IEEE Ind. Appli. 2003*, pp. 168-175.

[7] F.Z.Peng, J.S.Lai, J.McKeever and J.Vancoevering, "A multilevel voltage source converter system with balanced DC voltages" in *Proc. of IEEE PESC 1995*, pp.1144-1150.

[8] C.Feng, J.Liang and V.G. Agelidis, "A novel voltage balancing control method for flying capacitor multilevel converters", in *Proc. of IEEE IECON 2003*, pp. 1179-1184.

[9] X.Yuan, H.Stemmler and I.Barbi, "Investigation on the voltage self-balancing of the three-level capacitor clamping inverter", in *Proc. of IEEE Power Electron. Spec. Conf, (PESC'99)*, Charleston, USA, *1999,* pp.1059-1064.

[10] B.Bijlenga, "HVDC device for converting between alternating voltages and current voltages", US patent 6,480,403, Nov. 2002.

[11] G.S.Perantzakis, F.H.Xepapas and S.N.Manias, "A novel four-level voltage source inverter-influence of switching strategies on the distribution of power losses", *IEEE Trans. on Power Electron.*, vol. 22, no. 1, pp. 149-159, Jan 2007.

[12] P.Barbosa, P.Steimer, M.Winkelnkemper, J.Steinke and N.Celanovic, "Active-neutral-point clamped (ANPC) multilevel converter technology", in *Proc. of EPE Conf. 2005*, pp.11-14.

[13] P.M.Bhagwat and V.R Stefanovic, "Generalized structure of a multilevel PWM inverter", *IEEE Trans. on Ind. Appl.,* vol. IA-19, no 6, pp. 1057-1069, Nov/Dec 1983.

[14] M.S.A.Dahidah and V.G.Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: a generalized formula", *IEEE Trans. Power Electronics,* v 23, n 4, July 2008, pp.1620-1630.

[15] V.G. Agelidis, A. Balouktsis, I. Balouktsis and C. Cossar, "Multiple sets of solutions for harmonic elimination PWM bipolar waveforms: analysis and experimental verification", *IEEE Trans. Power Electronics,* v 21, n 2, Mar.2006, pp.415-421.

[16] V.G. Agelidis, A. Balouktsis and M.S.A.Dahidah, "A five-level symmetrically defined selective harmonic elimination PWM strategy: analysis and experimental validation", *IEEE Trans. Power Electronics,* v 23, n 1, Jan.2008, pp.19-26.

[17] MATLAB/SIMULINK software package, version R2007a, *The Math Works*. http://www.mathworks.com.