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Keywords

level, elimination, five, harmonic, control, inverter, hybrid, bridge, h, cascaded, ac, dc

Disciplines

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Harmonic Elimination Control of a Five-Level DC-AC Cascaded H-bridge Hybrid Inverter

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Abstract—A five-level hybrid cascaded inverter operating under selective harmonic elimination (SHE) pulse-width modulation (PWM) control is discussed in this paper. The topology is a cascaded connection of a conventional three-phase, two-level inverter and an H-bridge module for each phase with a single DC-source. The topology boosts the output voltage within limits and with no additional DC-DC converters. However, such boosting feature depends on the control of the floating capacitor voltage and the load power factor. The regulation of the floating capacitor for the given modulation strategy is also analyzed. Experimental results taken from a single-phase laboratory prototype are presented to confirm the operational characteristics of the converter.

Index Terms—cascaded hybrid inverter, harmonic elimination, multilevel inverter, pulse width modulation

I. INTRODUCTION

Multilevel converters offer a number of advantages when compared to the conventional two-level converter counterpart. The stepped approximation of the sinusoidal waveform using higher levels reduces the harmonic distortion of the output waveform, and the stresses across the semiconductor devices, and allows higher voltage/current and power ratings. The reduced switching frequency of each individual switch of the converter also reduces the switching losses and improves the efficiency of the converter [1].

A number of multilevel converter topologies have been proposed including: the neutral-point-clamped (NPC); the flying-capacitor (FC), and the cascaded H-bridge (CHB) converter [2]. The NPC and FC converters require a single DC-source. The additional voltage levels are created through capacitors and clamping diodes for the case of the NPC or through flying capacitor cells for the case of the FC. Both of these topologies allow for transformer-less operation, however their extension to higher number of levels becomes challenging mainly due to the balancing of the DC-link voltage and neutral point or FC voltages. The CHB converter can be extended to a number of levels, however, the need for isolated DC sources for each phase and cell largely complicates the DC side and increases size and weight requirements due to the need for isolation transformers [2].

A hybrid topology is the cascaded hybrid multilevel inverter [3]–[7]. In the case of the five-level topology discussed here, a conventional three-phase two-level inverter is connected in series with an H-bridge cell for each-phase. The H-bridge cells

use a capacitor as a voltage-source and the need for individual and isolated DC sources is eliminated. Only a single DC-source (battery, fuel cell, PV array etc) is required for the converter simplifying its layout.

Previous work has focused on the operation of the five-level cascaded hybrid inverter for hybrid electric vehicles [4] and electric drives [5]. The operation of the topology under carrier-based sinusoidal pulse-width modulation (SPWM) and fundamental frequency switching has also been reported [6]. In the case of the fundamental frequency switching and because of the low number of levels produced, only one harmonic can be controlled. This presents a limitation for the converter bandwidth and its performance. The SPWM allows for a larger bandwidth, but the increased number of switchings affects the switching losses and the overall efficiency of the topology.

The operation characteristics of the five-level cascaded hybrid inverter with selective harmonic elimination (SHE) PWM are reported in this paper. The proposed modulation focuses on eliminating a number of low-order harmonics from the output voltage spectrum while maintaining the voltage of the floating capacitors to the required level for proper operation. This extends the bandwidth of the converter while maintaining the necessary switchings and associated switching losses to a minimum.

The paper is organized in the following way. Section II describes the topology of the five-level hybrid cascaded inverter and the voltage balancing principles. Section III discusses the five-level harmonic elimination technique used in this paper and Section IV formulates the conditions for voltage balancing under the proposed SHE-PWM. Section V provides simulation results and Section VI presents experimental results taken from a laboratory converter. Finally, the conclusions are summarized in Section VII.

II. TOPOLOGY AND OPERATION

The five-level hybrid cascaded inverter configuration is shown in Fig. 1. The DC source is connected to all phase legs of the conventional three-phase, two-level inverter and the H-bridge cell utilizes a capacitor as a voltage source. Assuming that the DC voltage is equal to $2V_{dc}$, then the voltage of the capacitor of the H-bridge cell has to be maintained to V_{dc} so that a five-level waveform is synthesized in the output. Considering a split DC source, the output of the two-level

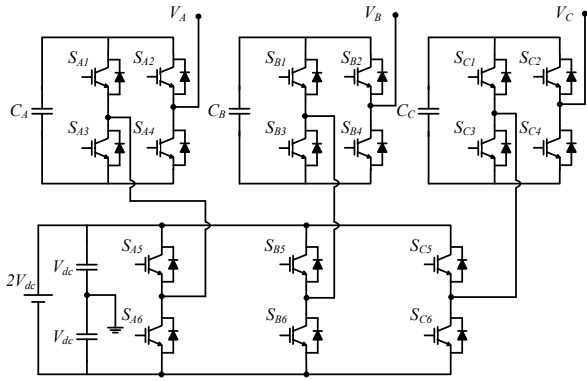


Fig. 1. Schematic of the three-phase, five-level hybrid cascaded inverter.

TABLE I
VOLTAGE OUTPUT AND SWITCHING STATES

V_{out}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}
$+2V_{dc}$	0	1	1	0	1	0
V_{dc}	1	1	0	0	1	0
V_{dc}	0	0	1	1	1	0
0 (State 1)	1	0	0	1	1	0
0 (State 2)	0	1	1	0	0	1
$-V_{dc}$	0	0	1	1	0	1
$-V_{dc}$	1	1	0	0	0	1
$-2V_{dc}$	1	0	0	1	0	1

leg can be equal to either $+V_{dc}$ or $-V_{dc}$. Table I shows the switching states and possible output voltages of the converter.

The voltage of the capacitor is affected during the converter states that the capacitor is connected to the load. These converter states occur during when the output voltage levels are $+2V_{dc}$ and $-2V_{dc}$ and during the zero voltage level. The first two cases can only be acquired by a single switching state combination, as shown in Table I, where x indicates the phase (A, B or C). The change in the capacitor voltage then depends on the direction of the load current. The zero level can be acquired by two different states. The capacitor is connected in such a way so that its voltage is opposite to the voltage of the lower phase-leg. Selection of the switching state is performed so that, together with the direction of the load current, the voltage of the floating capacitor is regulated within the predetermined limits.

The utilization of the two zero voltage output redundant states (State 1 and State 2), regulates the voltage level of the capacitor of the H-bridge cell. The two different switching strategies for attaining the same five-level output waveform are shown in Figs 2 (a) and (b). This means that there is no explicit need to know the capacitor current and only a voltage sensor is required on the H-bridge cell. The selection of the redundant states is based on the direction of the load current and the voltage across capacitor so an output current sensor for each phase is additionally required.

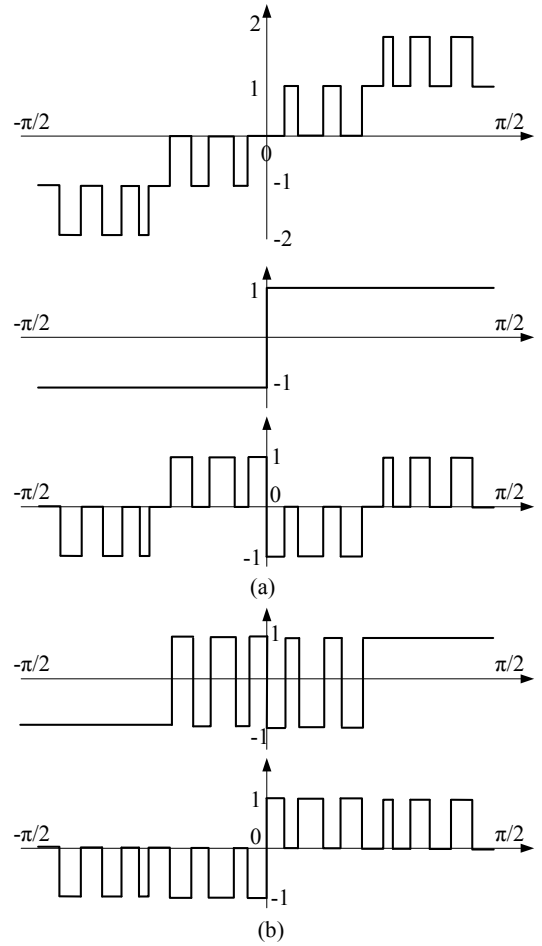


Fig. 2. Possible combinations of individual output voltages resulting in the five-level waveform (a) State 1, (b) State 2.

III. FIVE-LEVEL HARMONIC ELIMINATION PWM

A number of different methods can be used for the modulation of a five-level cascaded hybrid inverter, including SPWM [6] and fundamental frequency modulation [7]. In this paper, a five-level SHE-PWM is used [8]–[10]. Assuming a quarter-wave symmetry for the targeted PWM waveform, eleven and twelve angles are calculated over the quarter-period of the waveform. The eleven and twelve sought angles, representing the exact switching instants of the waveform, are calculated in order to control the fundamental component to the required level and eliminate the first ten or eleven low-order and non-triplen harmonics respectively. For these cases, the first harmonic expected on the line-to-line output voltage spectrum is the 35th and 37th harmonic respectively.

The angles are distributed to the two level transitions of the first quarter period. Assuming that the number of switchings between the zero and first level are k (where k is always an odd number) and the total number of switchings are equal to N , the equations describing the SHE-PWM are given in eqn. (1)–(3).

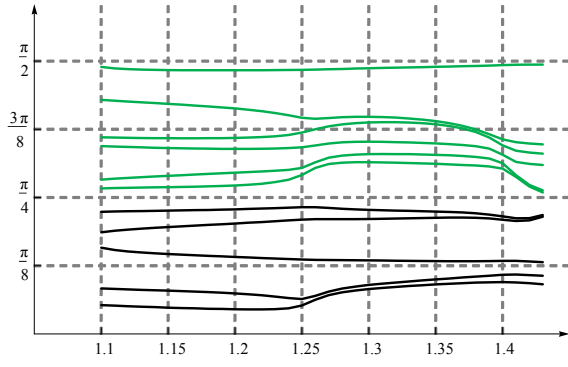


Fig. 3. Solution Trajectories for 11 angles, 5/6 angle distribution, Set 4

$$\sum_{i=1}^k (-1)^{i-1} \cos(a_i) + \sum_{i=k+1}^N (-1)^{i-1+k} \cos(a_i) = M \quad (1)$$

$$\sum_{i=1}^k (-1)^{i-1} \cos(5a_i) + \sum_{i=k+1}^N (-1)^{i-1+k} \cos(5a_i) = 0 \quad (2)$$

$$\sum_{i=1}^k (-1)^{i-1} \cos(na_i) + \sum_{i=k+1}^N (-1)^{i-1+k} \cos(na_i) = 0 \quad (3)$$

where

$$0 \leq M \leq 2 \quad (4)$$

$$a_1 < a_2 < \dots < a_N < \frac{\pi}{2} \quad (5)$$

and the amplitude of the fundamental component is:

$$\hat{V}_1 = \frac{4 \cdot M}{\pi} \cdot V_{dc} \quad (6)$$

The system of non-linear and transcendental equations with trigonometrical terms is solved for a number of distributions to the two levels and a number of solutions covering different ranges for the modulation index are acquired. As expected for this kind of equations, the system exhibits multiple solutions. Table II and Table III show the ranges of solutions for both eleven and twelve angles and for the various distribution ratios considered. These sets of solutions cover the whole modulation index range from 0.7, since lower modulation indices can be acquired by a three-level waveform, to 1.81 which is the theoretical maximum of harmonic elimination where triplen harmonics are not controlled. A set of solutions for eleven angles and 5/6 distribution, randomly selected from the pool of solutions, is shown in Fig. 3

IV. FLOATING CAPACITOR VOLTAGE REGULATION

The main difference between the control of typical DC source based cascaded inverters and the hybrid five-level inverter discussed in this paper is the balancing of the voltage of the floating H-bridge cell capacitor. Regulation of the voltage of the capacitor to the expected level is important to the proper operation of the converter. As discussed earlier, the two

TABLE II
DISTRIBUTIONS AND MODULATION INDEX RANGES FOR 11 ANGLES

11 angles	Set 1	Set 2	Set 3	Set 4
3/8	1.28-1.49	1.43-1.62	1.4-1.55	
5/6	1.05-1.23	0.92-1.06	1.04-1.26	1.1-1.43
7/4	0.92-0.99	0.7-0.99	1.25-1.34	

TABLE III
DISTRIBUTIONS AND MODULATION INDEX RANGES FOR 12 ANGLES

12 angles	Set 1	Set 2	Set 3	Set 4
3/9	1.74-1.81	1.6-1.81	1.5-1.69	1.44-1.54
5/7	1.04-1.23	1.04-1.46	1.04-1.32	
7/5	1.07-1.32			

states with which the zero level voltage can be acquired can be utilized in order to regulate the voltage to the required level. The voltage of the capacitor is also affected when $+2V_{dc}$ and $-2V_{dc}$ are generated, but since no redundant switching states exist for these two levels capacitor charging or discharging depends on the direction of the load current.

The voltage of the capacitor can therefore be maintained to the required level if the overall amount of charge of the capacitor over a period is at least equal to the discharge amount of the capacitor over a fundamental period. Since the only states that can be used for regulation of the voltage of the capacitor are those of the zero level, the condition can be simplified for the charging and discharging over the half period. This restriction can be rewritten in terms of the load current as shown in eqn. (7)

$$\int_0^{\pi} |i_{charging}| d\theta - \int_0^{\pi} |i_{discharging}| d\theta > 0 \quad (7)$$

where $i_{charging}$ is the part of the load current charging the floating capacitor and $i_{discharging}$ discharging the capacitor.

For the case of fundamental frequency switching only one switching occurs between the two levels and a single set of solutions only exists. Therefore a closed formula can be derived that estimates the regulation of the voltage to the required level for a given displacement power factor angle and with the simplification of only fundamental frequency currents [5]. For the case of SHE-PWM, the integrals of eqn. (7) have to be evaluated independently for a given set of solutions and displacement power factor. This can be performed in mathematical package such as MATLAB [11].

Fig. 4 shows half a period of the five-level waveform and the fundamental component of the current for two different power factors. Again a distribution of 5/6 angles and a total of eleven angles over the quarter period is considered. During the top level, the voltage of the capacitor is affected by the direction of the current and during the zero level, the switching states of the converter legs can be selected so that the capacitor either charges or discharges depending on the instantaneous voltage and the limits to which the voltage is allowed to vary.

For low values of load power factor and when the displacement power factor angle becomes greater than the $k+1$ angle,

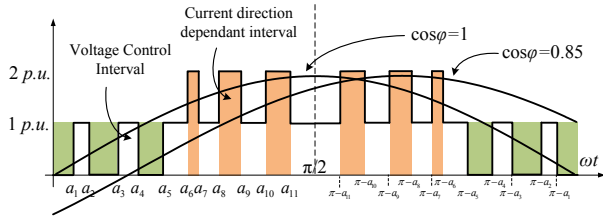


Fig. 4. Typical five-level waveform and capacitor voltage control intervals for 11 angles per quarter-wave.

a time interval exists where the current is negative during the top level. This means that the capacitor can be charged during the top level and partially explains the significant voltage boost to the output voltage for loads with rather low power factors.

Considering a conventional two-level inverter, the maximum value of fundamental component that can be achieved for a DC source of $2V_{dc}$ and for the cases of harmonic elimination and triplen harmonic injection is equal to $\frac{4-0.91}{\pi} \cdot V_{dc}$. In the case of the converter discussed in this paper and as can be calculated from eqn. (7) the fundamental can reach a value of $\frac{4-0.99}{\pi} \cdot V_{dc}$ under any load, representing a gain of approximately 10% and higher than that, depending on the displacement power factor of the load. This boost feature is also verified in the simulation and experimental results presented in the following sections.

V. SIMULATION RESULTS

The five-level hybrid cascaded inverter under SHE-PWM control is simulated in MATLAB/SIMULINK for both the cases of eleven and twelve angles. The simulation parameters match those of the experimental work and are summarized in Table IV. A split DC voltage of 80 V is considered for all cases and the floating capacitor is regulated so that it maintains its voltage to 40 V within a band of ± 0.5 V. Two different loading conditions are investigated, their characteristics are also shown in Table IV.

Initially, eleven angles are considered over the quarter-period with an angle distribution of 7/4 and for load A. Fig. 5(a) shows the line-to-neutral voltage and Fig. 5(b) the corresponding spectrum. It is observed that all non-triplen harmonics are eliminated from the output voltage waveform and the first non-triplen harmonic in the output waveform is the 35th as expected. The amplitude modulation index is equal to $M=0.95$ and the amplitude of the output voltage is higher than in the case of the two-level inverter when the same DC voltage is considered. Fig. 5(c) shows the load current.

A second simulation is also considered, twelve angles are used over the quarter-period with an angle distribution of 5/7 and for load B. Fig. 6(a) shows the line-to-neutral voltage and Fig. 6(b) the corresponding spectrum. Since one extra angle is considered in this case the first non-triplen harmonic in the output waveform is the 37th. The amplitude modulation index in this case is $M=1.15$. Fig. 6(c) shows the load current. In both cases the low-order triplen harmonics are eliminated from the connection of the power circuit.

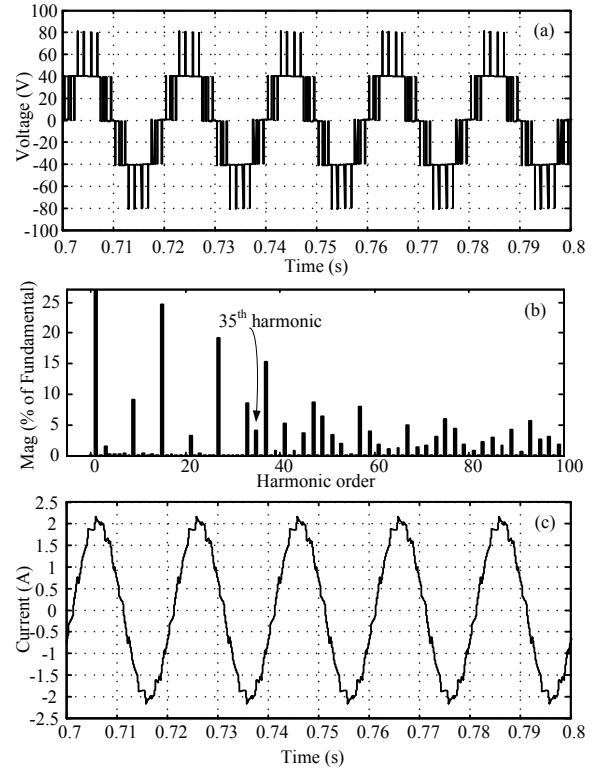


Fig. 5. Simulation Results, 7/4 distribution and $M=0.95$, Load A (22Ω , 30mH), (a) Line-to-neutral voltage (b) Line-to-neutral voltage spectrum, (c) Line current.

TABLE IV
SIMULATION AND EXPERIMENTAL PARAMETERS

DC Voltage	80 V
Capacitor Voltage	40 V
Capacitor Voltage Control Band	± 0.5 V
Load A	$R=22 \Omega$, $L=30 \text{ mH}$
Load B	$R=11 \Omega$, $L=30 \text{ mH}$
Load C	$R=11 \Omega$, $L=125 \text{ mH}$

VI. EXPERIMENTAL VERIFICATION

The theoretical considerations and simulation results are also verified in a laboratory prototype shown in Fig. 7. A single-phase, five-level hybrid converter was built using the FUJI 21MBI100TA-060 IGBT modules. The voltage regulation and SHE-PWM previously described have been implemented on a dSPACE 1104 R&D DSP board. A number of cases are again investigated, as shown in Table IV.

Fig. 8 shows the line-to-neutral voltage and corresponding spectrum for a 7/4 angles distribution and M of 0.95 when load A is connected in the output. In accordance with the simulation results, the first non-triplen harmonic appearing in the line-to-neutral spectrum is the 35th (1750 Hz for a 50Hz AC system). The top waveform of Fig. 9 shows the load current at the output of the single-phase topology and the bottom waveform shows the current through the capacitor. The effect of the voltage regulation control can be seen in the lower

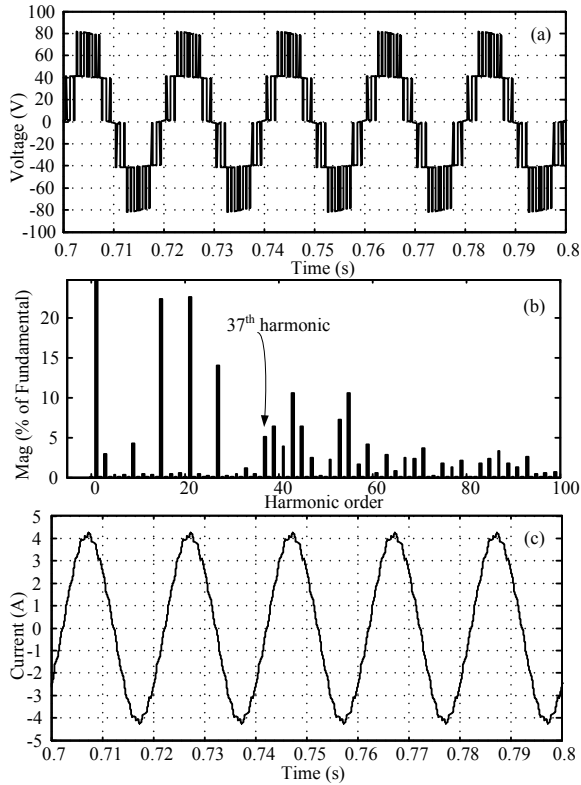


Fig. 6. Simulation Results, 5/7 distribution and $M=1.15$, Load B (11Ω , 30mH), (a) Line-to-neutral voltage (b) Line-to-neutral voltage spectrum, (c) Line current.

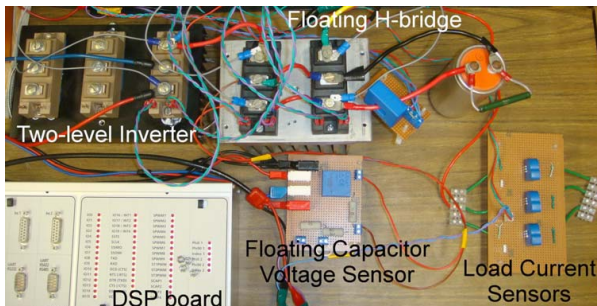


Fig. 7. Laboratory setup of the single-phase five-level hybrid inverter.

waveform of Fig. 9. The currents through the capacitor are not identical over consecutive periods since they depend on the actual voltage of the capacitor and the load current direction. Fig. 10 shows the deviation of the voltage of the floating capacitor over 20 periods (0.4 seconds) and the effect of the voltage regulation control on the floating capacitor voltage.

Similarly, Fig. 11 shows the five-level line-to-neutral output voltage of the topology and the corresponding output waveform of the two-level leg. Here, a 5/7 angle distribution over the two levels and a amplitude modulation index of $M=1.15$ are considered with load B connected in the output. As in the case with the current through the capacitor, the individual voltage of either the two-level or the H-bridge cell is not identical for consecutive periods but rather depends on

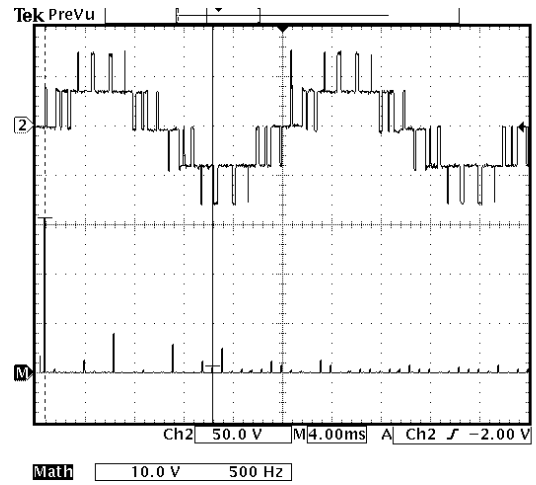


Fig. 8. Line-to-line voltage and harmonic spectrum, Load A (22Ω , 30mH), $M = 0.95$, angle distribution 7/4.

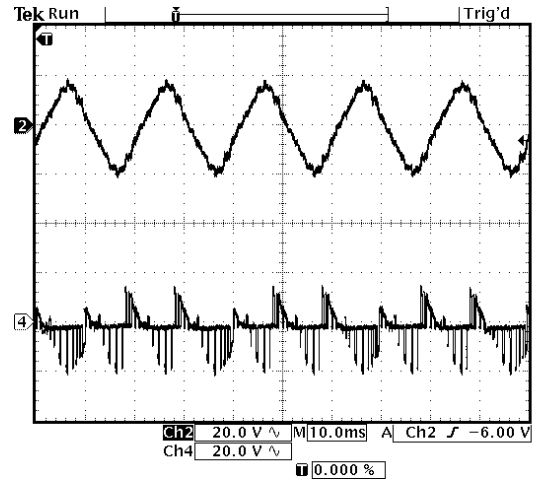


Fig. 9. Load and capacitor current, Load A (22Ω , 30mH), $M = 0.95$, angle distribution 7/4 (2 Amp/div).

the voltage and charging condition of the floating capacitor. Finally, an angle distribution of 3/8 over the two levels and amplitude modulation index of $M=1.35$ is considered. Load C (11Ω , 125mH) is connected in the output of the single phase topology. Fig. 12 shows the line-to-neutral waveform and corresponding voltage harmonic spectrum and Fig. 13 shows the load and capacitor current. Because of the very inductive nature of the load, the output current is almost sinusoidal and a boost gain of 150% can be achieved, compared with the conventional two-level case.

VII. CONCLUSION

The operation of a five-level cascaded hybrid inverter under SHE-PWM is discussed in this paper. The topology only requires a single DC source and produces a five-level line-to-neutral waveform. This reduces the total harmonic distortion of the waveform when compared to the typical two-level inverter and can also boost the fundamental component of the output voltage to a level that depends on the displacement power

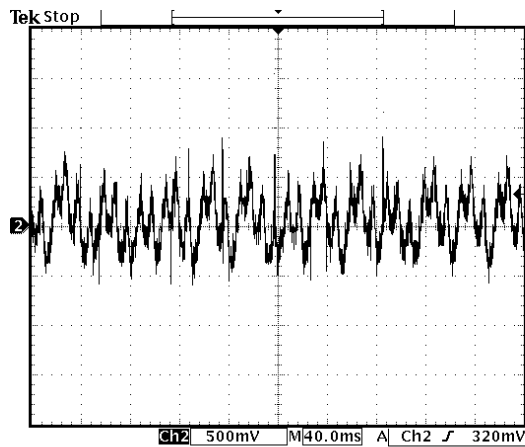


Fig. 10. Deviation of the floating capacitor voltage from the regulated voltage, Load A (22Ω, 30mH), $M = 0.95$, angle distribution 7/4.

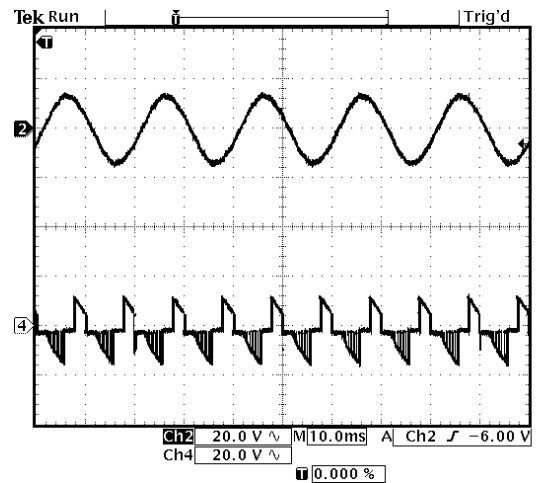


Fig. 13. Load and capacitor current, Load C (11Ω, 125mH), $M = 1.35$, angle distribution 3/8 (2 Amp/div).

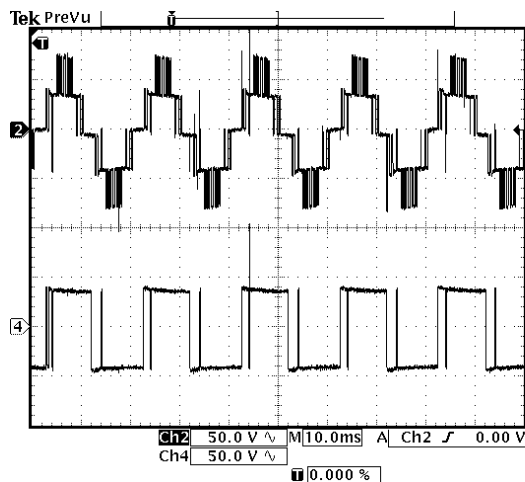


Fig. 11. Line-to-neutral and two-level leg output waveforms, Load B (11Ω, 30mH), $M = 1.15$, angle distribution 5/7.

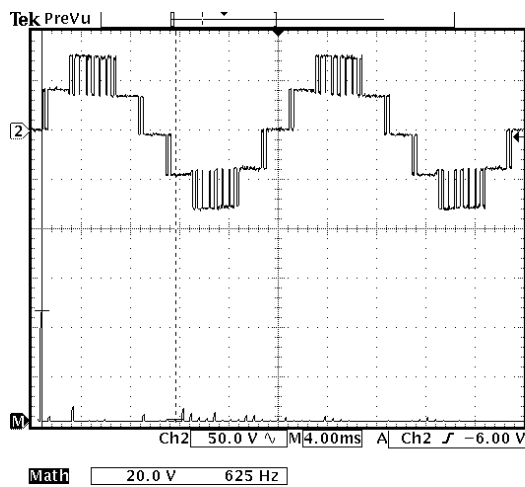


Fig. 12. Line-to-neutral waveform and corresponding harmonic spectrum, Load C (11Ω, 125mH), $M = 1.35$, angle distribution 3/8.

factor of the load, as long as the H-bridge capacitor voltage can be regulated to the required level. Simulation and experimental results from a laboratory prototype have been provided that verify the converter operation and its boost capabilities.

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