2007

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SLOPE LINE CODING FOR TELECOMMUNICATION NETWORKS

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***Abstract* - A new slope line code for information transmission and storage has been proposed. The line code operates on the principle of slope coding. Two alternative slopes are used to transmit or store the binary information 1s and 0s. The decoder extracts the binary information from the received multilevel signal using slope comparison technique with slope violation detector from the incoming symbols. The encoder and decoder operation is described. A simulation of the encoder and decoder has been carried out using MultiSIM® software. The simulated results are in thorough agreement with the theory. The slope line code also meets the many desirable features of other line codes. This makes it attractive and suitable for data transmission and storage on different types of telecommunication networks and multimedia systems.**

Index Terms - Data Transmission, Line Codes, Simulation and Modelling, Telecommunication Networks.

1. INTRODUCTION

The emergence of modern multimedia systems that are digitally processing voice, data, images and real-time interactive video necessitates the transfer of these services across efficient wire-connected and wireless telecommunication networks for their users.

The efficiency can be considered from several points of view such as the access and routing protocols, encoding and modulation techniques, system design complexity and cost and many others.

One of these important efficiency parameters is the coding which is thoroughly covered in the literature. Many codes have been proposed and then deployed as standards in telecommunication and computer networks.

Line codes have many desirable properties which give preference to the usage of one line code on another. The desirable properties involve its spectrum occupancy with no dc content, self-clocking information, power requirement, coding efficiency, transparency, error detection and correction capabilities, encoding and decoding complexities with their circuits, and finally, the cost of circuitry. A survey of the principle of operation, properties and applications of line codes may be sought from [1]-[3]. The most recent guide which involves the newly emerging technology and applications in multimedia systems, telecommunication and computer networks, and wireless systems may be sought from [4]-[7].

In previous work [8], the design of the encoder circuit has been covered. This paper involves the design of the decoder and the decoding results gathered of the new line code. It also reviews the principle of operation of the slope coding together with encoder design and results. Slope coding is a technique in which the slope of the reshaped transmitted/stored pulse is used to carry the information of the binary bit (1 or 0). At the receiving side the data is extracted from the slope of the incoming/received signal.

The rest of the paper is arranged into several sections. Section two describes the slope line code encoding and decoding principles. Section three is devoted to the encoder and decoder circuits design and their operational performance and results evaluation. Section four deals with the discussion and comparison with other line codes and also reports on further works to be carried out. Finally, the conclusion is given in section five.

2. ENCODING AND DECODING TECHNIQUES

The new line code operates on the principle of slope or stair-step encoding technique. The encoder generates either positive or negative pulse (slope). These two slopes are decoded at the receiving end to extract the original binary of 1s and 0s and also to derive the clock signal.

A. The Principles of Encoder Operation

The encoder function is to generate an output pulse for every binary bit it receives with the same bit/symbol duration. The generated pulse is either positive (i.e. has a positive level/amplitude with respect to the previous pulse) or negative (i.e. has a negative level relative to the previous pulse).

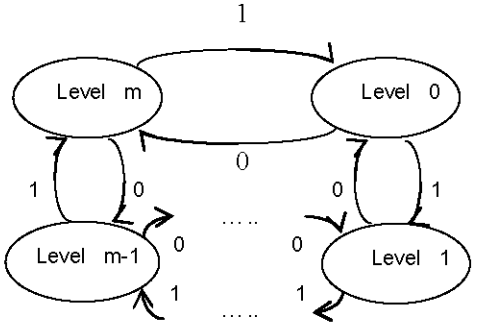

Fig. 1. State transition diagram of the encoder.

Fig. 1 shows the state diagram of the encoder. In this figure, the encoder output is assumed to have *m* signal levels (amplitudes) or states. The value of *m* is an application-specific parameter. It can be set to the desired number of encoder output levels. The output levels have direct influence on the shape of the power spectral density of the line code and on its peak-to-average power ratio.

The stair-step/slope line encoder operates as follows.

(1) When a binary 1 is received, the encoder generates a positive going pulse with respect to the previous output level for a time duration equivalent to the original input binary data time.

(2) When a binary 0 is received, the encoder generates a negative going pulse with respect to the previous output

level for a time duration equivalent to the original input binary data time.

(3) For both previous cases, when the encoder output level reaches the two extreme limits of the output m levels, the encoder refreshes its output with a pulse that has either the maximum or the minimum level. This means for a run of binary 1s at the encoder input, when the encoder output reaches the maximum (level m) level. In this case, the encoder switches back to the minimum (level 0) level and then generates a positive-going symbol in a stair-step form. The same procedure will happen for a run of binary 0s but with a negative-going symbol.

Fig. 2 shows the stair-step- or slope-encoded waveform for an arbitrary input binary sequence of 0s and 1s. In this example, it has been assumed that the encoder output has four levels (m=4), two positive (+ve) levels and two negative (-ve) levels. Other values of m can be taken and then the encoded waveforms can be generated accordingly. With (m=2), the encoder output produces a slope-encoded waveform similar to bi-phase (Manchester) code waveform, when a half bit slope decision criterion is introduced. In Fig. 2, other examples of line codes are also given for illustration purposes.

A quick inspection of the slope encoded waveform shows its ability to maintain a transition of signal level at every output symbol. Thus, the waveform has an excellent timing information and therefore, it facilitates clock recovery and maintains a strong synchronism between the encoder and decoder. This is perhaps one of the most desirable properties of line codes [1]-[5].

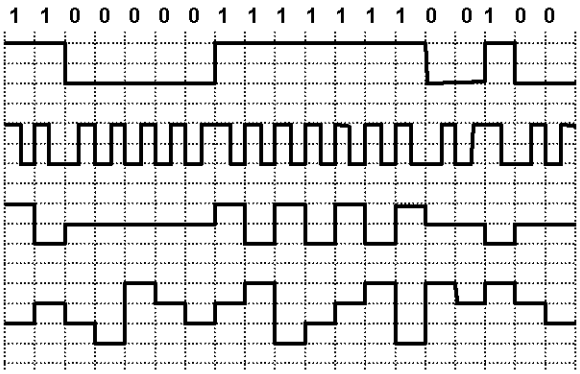

Fig. 2. Example of different encoded waveforms. From top to bottom: NRZ-L, Manchester, AMI, and slope line codes.

B. Principles of Decoder Operation

The decoding operation of the new slope line code is simple as shown in the state diagram in Fig. 3. The incoming multilevel–coded signal undergoes parallel comparison processes with its one-symbol delayed version. From the diagram, there are two binary states (0 and 1) at the decoder output. The operation of the decoder is as follows.

(1) When the current output state is binary 0, then the decoding process for the input m-level signal is carried out depending on the following.

(i) If the signal level is less (negative slope received) in comparison with its delayed version, then it stays in the same state and decode this symbol as an output binary 0.

(ii) If the signal level is higher (positive slope received), in comparison with its delayed version, then change state to binary 1, and decode this level as an output binary 1.

(iii) If there is a positive jump in signal level, where this jump is equal to two levels or more in comparison with its delayed version, then it stays at the same state and decodes this symbol as an output binary 0.

(2) When the current output state is binary 1, then the decoding process is carried out depending on the following.

(i) If the signal level is higher (positive slope received) in comparison with its delayed version, then it stays at the same state and decodes this symbol as an output binary 1.

(ii) If the signal level is less (negative slope received) in comparison with its delayed version, then changes state to binary 0, and decodes this symbol as an output binary 0.

(iii) If there is a negative jump in signal level, where this jump is equal to two levels or more in comparison with its delayed version, then it stays at the same state and decodes this symbol as an output binary 1.

The decoder has a threshold for the comparison process between the received signal and its one-bit delayed version. The threshold level is to be decided depending on the number of levels (m) used at the encoder. This is especially essential when a violation to the rule occurs when there is either a positive or a negative jump in signal level in comparison with the delayed version.

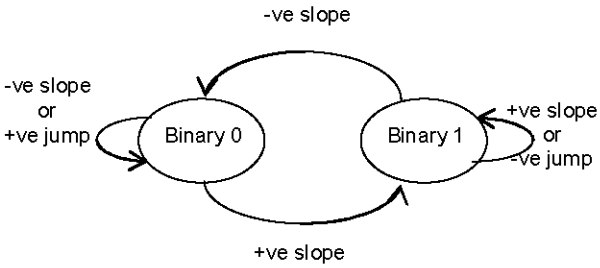

Fig. 3. State transition diagram of the decoder.

3. ENCODER AND DECODER CIRCUITS DESIGN

A. Encoder Circuit Design

The encoder circuit is designed to have four output levels (i.e. m=4). This number has been chosen in order to match the example given previously in Fig. 2. A block diagram of a generalised circuit is shown in Fig. 4 [2,9]. The 4-level encoder consists of a 2-bit up/down counter and a digital-to-analogue converter (DAC). The encoder is fed with a pseudo-noise (PN) binary data sequence. The PN sequence generator has four stages. Thus, with $n=4$, it generates $2^n-1=2^4-1=15$ pseudo-random binary bits. The counter that it follows is a two-stage up/down counter. Its count is controlled by the input binary sequence. If the input is binary 1 the counter counts up and when the input is binary 0, it counts down. The output count (2-bit) of the counter is fed to a binary-weighted-input inverting summer amplifier circuit. The latter circuit is a type of a digital-to-analogue converter. The DAC has two inputs that are fed from the outputs of the two-stage up/down counter. The output of the DAC is the required m-level stair-step-/slope-encoded waveform.

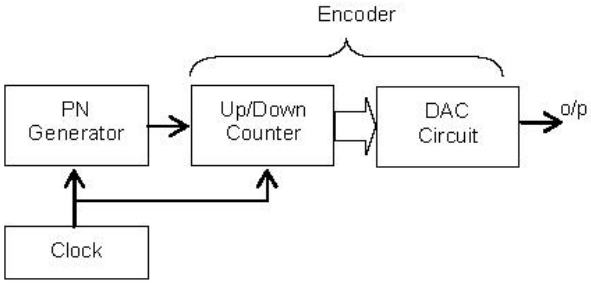

Fig. 4. PN generator and slope encoder block diagram.

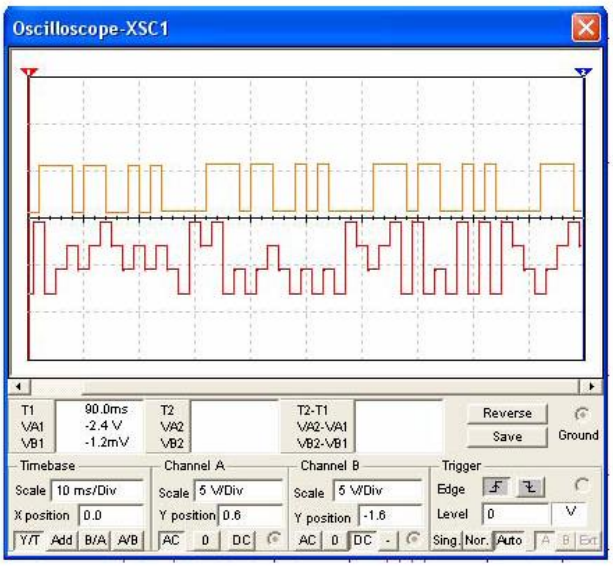

Fig. 5. Slope encoder input (PN sequence) and output (stair-step-/slope-encoded) waveforms.

Fig. 5 shows the results of the output waveforms of the PN binary sequence generator together with the stair-step-/slope-encoded waveforms. The results are obtained from a simulation model that is achieved using MultiSIM® package [10]. The encoded waveform has about a half-bit time delay with respect to the PN sequence data. This is due to the inherent logic circuits propagation delay. The encoded waveform starts at an arbitrary level of the four levels that are considered in the design of the encoder circuit.

The encoder operation was further investigated with a simulation test where the applied binary input has a continuous run of either 1s or 0s. This test has resulted in output encoded waveforms that have repeated patterns of positive and negative slope stair-case shape having four levels respectively.

A higher number of output encoded levels can be obtained with the use of a higher order up/down counter. The DAC circuit which complements the counter satisfactory operation needs in this case to have a number of inputs that matches the parallel bits produced at the output of the up/down counter.

B. Decoder Circuit Design

The decoder is designed to extract the binary information from the multilevel ($m=4$) slope-encoded received signal. The diagram in our design is a generic model which can be used for any number of levels [2,9]. It only needs adjustment from the point of view of the supply or reference voltage in order to cope with the minimum and maximum limits of the encoded signal. The block diagram of the decoder circuit is shown in Fig. 6. The input is the slope-encoded signal and the output is the binary information signal. The input signal is compared with its delayed version and a decision has to be made about the 1s and 0s it contains. The time delay circuit produces one symbol time duration delay (equivalent to one bit duration of the original binary data). The delayed signal is conditioned and compared with the currently received signal using a comparator circuit and two weighted adder/summer circuits. The last two circuits are used to deal with the violation (+ve and –ve jumps) of the encoding scheme that is adopted at the encoder/transmitter side. Recall that violation occurs when the slope-encoded signal reaches the two extreme level limits. The outputs of all these three circuits are then logically grouped to control a digital circuit. The digital circuit is mainly a memory element (D-type flip-flop with preset and clear asynchronous inputs) that is triggered by the recovered clock pulses at a rate that is equivalent to the original binary information rate. The output of the memory element is the required PN sequence that is fed to the encoder at the other end. The results of the simulation of the decoder circuit are shown in Fig. 7. it shows the decoded binary PN sequence together with the extracted clock signal.

C. Clock Recovery Circuit Design

The clock signal recovery circuit design is very simple. This is due to the fact that the received slope-encoded multilevel signal is rich with timing information. A block diagram of the clock recovery circuit is shown in figure 8. It consists of a differentiator circuit which detects the edges of the incoming slope-encoded signal in both the positive and negative directions. This is followed by a full-wave rectifier circuit which produces either positive or negative equi-spaced impulses. These impulses trigger a one-shot multivibrator (monostable) circuit. The time constant of the monostable circuit can be adjusted to get the desired mark-to-space ratio of the recovered clock signal. The clock signal can then be used with the aforementioned decoder circuit. The recovered clock waveform can be seen in figure 7.

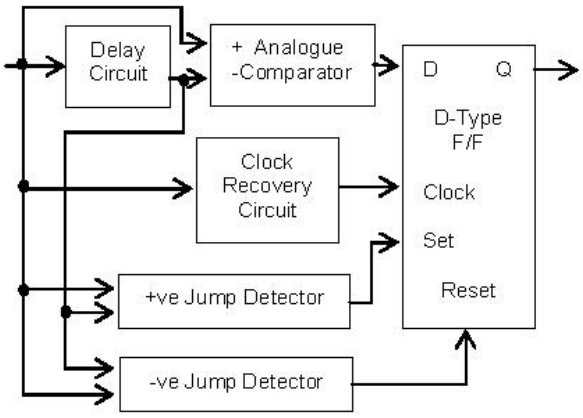

Fig. 6. Slope decoder block diagram.

4. DISCUSSION

Line codes are the main source that facilitates the transmission of data over telecommunication and computer networks and its storage in multimedia systems. The proposed line code in this paper has many characteristics which can be summarised into the following.

First, the slope line code introduces a new generic concept that is used for encoding messages to any required number of

levels. Thus, it has the ability of the inclusion of the binary, ternary and quaternary line codes that have been previously proposed for applications in data transmission and multimedia as special cases. With the selection of the output number of levels, the new line code can generate binary, ternary, quaternary, and in general a multi-level signal.

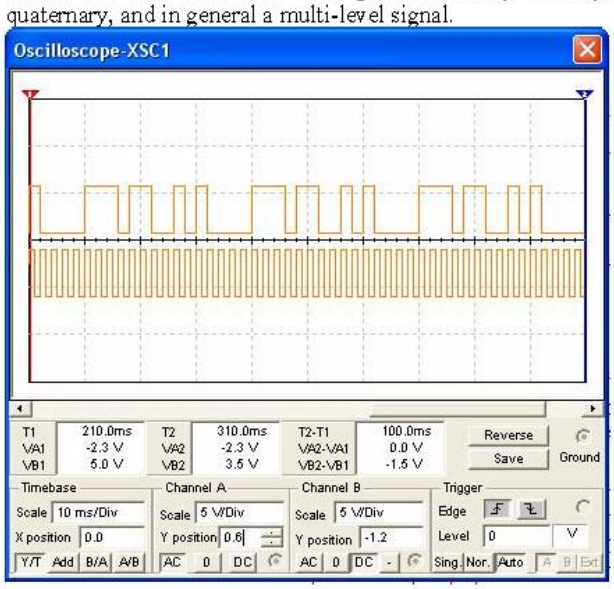

Fig. 7. Decoded output PN sequence and recovered clock waveforms.

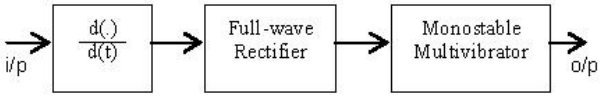

Fig. 8. Clock recovery circuit block diagram.

Second, the selection of the number of output levels is however influenced by two important parameters; the line code power spectral density and its peak-to-average power ratio. These parameters are considered very essential in the decision about the desirable features of line codes. Increasing the number of levels of the slope encoded signal tends to smooth the encoded waveform variation and hence tends to reduce the overall power spectral density of the code. This is considered as one of the most desirable features of line codes. This, however, has the disadvantage of increasing the peak-to-average power ratio of the line code. A trade off is thus needed to set these two parameters in order to optimise the design requirement.

Third, the method by which the input binary sequence is slope line encoded is simple and maintains continuous level change of the encoded waveform. The continuous change in the encoded signal provides self-clocking information which simplifies the process of clock recovery at the receiving side and thus keeps the encoder-decoder combination in continuous synchronism. This property is also one of the most recommended property of line codes.

Fourth, to design an encoder circuit that has encoded waveforms with a number of output levels that are not satisfying the formula $m = 2^k$, where k is a non-zero positive integer. In such a case, the count of the up/down counter needs to be truncated to match the desired number of output levels m. For example, for $m=6$, we need a 3-bit up/down counter that has modulus-6 count. With a 3-bit counter, there are 8 states of which two are considered as "don't care" (cannot happen) states. The DAC circuit in this case has three inputs.

Fifth, although the code gives the impression that the same principle as that of delta modulation is used, it completely differs in the way the encoding of the 1s and 0s of the binary information is represented. Delta modulation and Manchester codes are considered as a special case of slope line code when $m=2$. In line with its predecessor line codes, the new line code uses a multilevel slope coding technique in order to minimise the code power spectral density and to maintain other desirable features that were mentioned earlier.

Finally, the encoder is still under investigation and development. The quantitative noise performance evaluation and its bandwidth occupancy requirement are the main topic for future work. Further to that the extension of its operation is under consideration to include some of the substitutional line codes in its generic operation. This would involve the substitution of x-bit of 1s or 0s to represent single output symbol.

5. CONCLUSIONS

The investigation of a new line code that has been proposed previously is given in this paper. The line code is a generalised form that has m-level output. The value of m and hence the number of output levels can be chosen to meet specific requirements. The operation procedures of the encoder and decoder are well explained. The encoder and decoder circuits are designed for only one case that has four output levels. A PN sequence generator is used to mimic the data that control the encoding process. The encoder and decoder input and output results together with the PN sequence waveform are given. The simulated results are in thorough agreement with the theory. Additional features of the new line code are discussed and compared with other existing line codes. Moreover, a suggestion for further development of the proposal is also made.

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