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DC-link voltage ripple compensation for multilevel active-neutral-point-clamped converters operated with SHE-PWM

Sridhar R. Pulikanti
University of Wollongong, sridhar@uow.edu.au

Georgios Konstantinou
University Of New South Wales

Vassilios G. Agelidis
University Of New South Wales

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Sridhar R. Pulikanti, *Member, IEEE*, Georgios Konstantinou, *Graduate Student Member, IEEE*, and Vassilios G. Agelidis, *Senior Member, IEEE*

***Abstract*—This paper presents a dc-link voltage ripple compensation method for flying-capacitor (FC)-based active neutral-point-clamped multilevel converters operating under selective harmonic elimination pulsewidth modulation. The method is based on feedforward modification of the modulation index according to the ripple on the dc-link voltage, effectively altering the switching control functions. The low-order harmonics in the output due to the presence of the dc-link ripple are eliminated. In addition, a control strategy that actively regulates the flying capacitor voltages of each phase to the reference value and controls the neutral point voltage deviation is implemented. The performance of the dc ripple harmonic compensation method and regulation strategies are evaluated through simulation and experimental results from a three-phase, five-level laboratory prototype.**

***Index Terms*—Active neutral point clamped converter (ANPC), dc-ac power conversion, multilevel converter, selective harmonic elimination, pulsewidth modulation.**

I. Introduction

THE development of new semiconductor devices, new converter topologies, and advanced control and monitoring methods over the last two decades has resulted in a significant increase in the penetration of utility-grade voltage-source converters (VSC) in the power system. Applications, such as VSC-based high-voltage direct-current (HVDC) power transmission, static synchronous compensators (STATCOMs), static series compensators (SSSC), unified and interline power-flow controllers (UPFC and IPFC) are becoming more common in the modern power system [1].

Initial VSC-HVDC installations were based on the two-level and later on the three-level neutral point clamped (NPC) converter [1] while current and future installations utilize the modular multilevel (M^2LC [2] and CTL [3]) converter. Both of these configurations allow an extension to a large number of levels in the output waveforms, minimizing filtering and space requirements but adding to the complexity to the overall system.

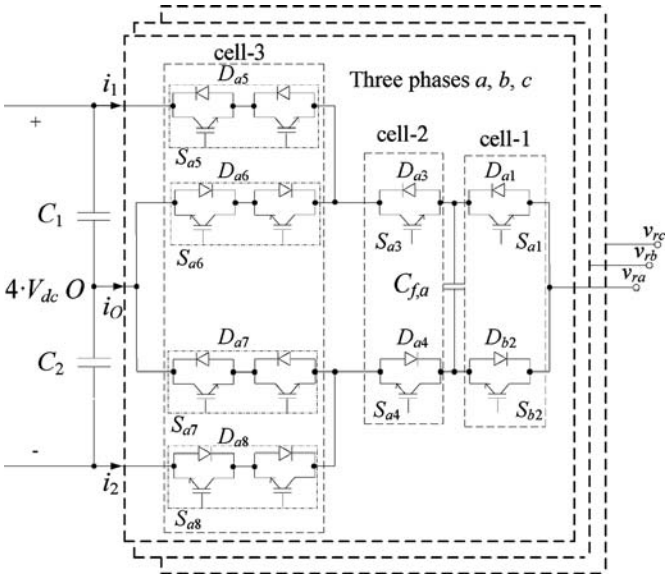

Fig. 1. Three-phase five-level FC-based ANPC converter.

For medium-voltage (MV) applications (grid connection of renewable energy sources and motor drives), typical multilevel topologies, such as the NPC and the cascaded H-bridges (CHB) converter [4], are typically employed. In recent years, hybrid multilevel converters using different connections of basic multilevel converter topologies have also been introduced [4]. Notable examples of these topologies include the five-level H-bridge NPC (H-NPC) converter [5], the three-level NPC converter with an H-bridge cell [6], the three-level active NPC (ANPC) converter [7] with an H-bridge cell [8], the four-level ANPC converter with a stacked multicell (SMC) converter [9], and the three-level ANPC converter with a two-level cell [10], [11]. The latter is referred to in this paper as the five-level FC-based ANPC converter, shown in Fig. 1.

The five-level FC-based ANPC converter was proposed in [10]. Various modulation methods have been proposed for the operation of the topology, including level-shifted carrier (LSC) pulse-width modulation (PWM) [10], phase-shifted carrier (PSC) PWM [12]–[14], as well as selective harmonic elimination (SHE) PWM [15].

In theory, modulation techniques assume a constant dc-link voltage. However, modern converters experience a significant

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S. R. Pulikanti is with the School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, 2522, NSW, Australia (e-mail: sridhar@uow.edu.au).

G. Konstantinou and V. G. Agelidis are with the Australian Energy Research Institute and the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney 2052, NSW, Australia (e-mail: g.konstantinou@unsw.edu.au; vassilios.agelidis@unsw.edu.au).

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ripple in the dc-link voltage [16], which is exacerbated when the converter is connected to the unbalanced or nonlinear loads or when the input of the front-end rectifier is connected to a weak or unbalanced ac grid. The ripple in the dc-link voltage causes variations in the converter output which deteriorate the quality of the converter output voltage introducing lower order harmonics.

Compensation techniques dealing with the dc-link voltage ripple have been reported for various converter topologies and modulation techniques [17]–[20]. In [17], a feedforward compensation method was implemented for a two-level converter and a one-cycle control method was presented in [18]. A dc-link voltage ripple compensation method for CHB converters under space vector modulation was presented in [19] and a dc-link voltage ripple compensation method using SHE-PWM, which alters the modulation function of two-level converters, was presented in [20] and [21]. However, the topic of dc-link voltage ripple on multilevel converters under SHE-PWM has not been investigated.

Under SHE-PWM, the application of the method to multilevel converters varies. CHB converters utilize multiple dc voltage sources as independent dc links in the configuration of the circuit. The effects of the variation of the dc link are localized only in the bridge and phase where it occurs. However, the five-level FC-based ANPC converter requires a single dc link for the operation of the three-phase topology. Variation in the dc-link voltage in combination with the presence of harmonic ripple affects the operation of the converter and a combined compensation approach is necessary.

The objective of this paper is to present a dc-link voltage ripple compensation method for the five-level FC-based ANPC converter under SHE-PWM. This method utilizes a feedforward scheme that modifies the modulation index according to the dc-link voltage ripple. This modification alters the switching functions so that the low-order harmonics generated in the output due to the dc-link voltage ripple are eliminated.

This paper is organized as follows. Section II describes the operational principles and SHE modulation of the five-level FC-based ANPC converter and voltage regulation for the flying capacitors and neutral point. Section III proposes the dc-link voltage ripple compensation method for the five-level FC-based ANPC and analyzes its application and limitations. Sections IV and V provide simulation and experimental results of the method and, finally, the paper summarizes its conclusions in Section VI.

II. Five-Level FC-Based ANPC Converter

A. Operational Principles

The three-phase, five-level FC-based ANPC converter is shown in Fig. 1 [10]. The phase leg of the five-level FC-based ANPC converter consists of switches (S_{x1}–S_{x8}), where x denotes the phase (a, b, or c), with antiparallel diodes (D_{x1}–D_{x8}) and a flying capacitor $C_{f,x}$. Assuming a constant voltage on the dc link equal to $V_{\rm dc}$, the voltage across each of the two dc-link capacitors (C_1 and C_2) is equal to $2V_{\rm dc}$. The voltage across the floating capacitor $C_{f,x}$ in order to generate five equal levels is $V_{\rm dc}$. The outer switches of the converter, which construct cell-3 of Fig. 1, should withstand a voltage equal to $V_{\rm dc}$ and typically two series-connected switches are considered in such a topology [10].

TABLE I
Switching States of the Five-Level FC-Based ANPC Converter

	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{rxO}
V_1	0	1	0	1	0	1	0	1	$-2V_{dc}$
V_2	1	0							$-V_{dc}$
V_3	0	1	1	0	0	1	0	1	$-V_{dc}$
V_4	1	0							0
V_5	0	1	0	1	1	0	1	0	0
V_6	1	0							V_{dc}
V_7	0	1	1	0	1	0	1	0	V_{dc}
V_8	1	0							$2V_{dc}$

One of the basic requirements of an FC-based ANPC converter is to operate the outer switches with a switching frequency equal to the fundamental [9]. Due to this requirement, two distinct half-periods can be identified where the converter is reduced to a three-level FC converter [14].

The switching states of the five-level FC-based ANPC converter are the combination of the switching states of the three-level ANPC converter and of the two-level cell. In order to decrease the switching frequency of the switches S_{x5}–S_{x8}, only four out of the six switching states of the three-level ANPC converter are considered. Eight switching states in total are available to generate the five different voltage levels at the output as shown in Table I.

Since the outer switches operate under fundamental frequency, the line-to-neutral voltage v_{xO} is given by

$$V_{rxO} = V_{\rm dc}[2 \cdot (S_{x5} - 1) + (S_{x3} + S_{x1})]. \tag{1}$$

The current through $C_{f,x}$ can then be expressed as

$$i_{cf,x} = (S_{x3} - S_{x1}) \cdot i_{rx} \tag{2}$$

and variation in the voltage of the floating capacitor is given by

$$\frac{d}{dt} v_{cf,x} = \frac{i_{rx}}{C_{f,x}} (S_{x3} - S_{x1}). \tag{3}$$

The voltage across the floating capacitors should be maintained at $V_{\rm dc}$. Switching states V_2, V_3, V_6, and V_7 affect the voltage across the FCs. The available redundancies in obtaining $+V_{\rm dc}$ (V_6 and V_7) and $-V_{\rm dc}$ (V_2 and V_3) are utilized to regulate the voltage across the FCs. During V_3 and V_6, the neutral point $'O'$ is connected to the load through the FC and both the voltages of the FC and the neutral point are affected.

The relation between the ac- and dc-side parameters is determined by the switching functions of the switches. The currents of the positive dc rail (i_1) are given by (4) and similar equations can be derived for the negative and neutral point of the converter [13]

$$i_1 = i_{ra} \cdot {\rm SF}_{a5} \cdot {\rm SF}_{a3} + i_{rb} \cdot {\rm SF}_{b5} \cdot {\rm SF}_{b3} + i_{rc} \cdot {\rm SF}_{c5} \cdot {\rm SF}_{c3} \tag{4}$$

where ${\rm SF}_x$ denotes the switching function of the respective switch. The dc current equations indicate that controlling the

voltage ripple across the FC influences the current through the neutral point. A proper control strategy is, therefore, necessary so that the voltages across the FCs and the dc-link capacitors are regulated at their reference voltage levels.

B. SHE-PWM for Five-Level Converters

SHE methods for multilevel PWM waveforms have been reported in [22]–[24]. The five-level waveform with N transitions per quarter-period is precalculated in such a way that a number of $(N-1)$ low-order harmonics are eliminated from the output spectrum while the fundamental frequency component is controlled to the required level.

A set of equations is solved to obtain solutions for the switching transitions [23]. In a generalized form, the system of equations is as follows:

$$\sum_{i=1}^{N_1}(-1)^{i-1}\cos(a_i)+\sum_{i=N_1+1}^{N}(-1)^{i-(1+N_1)}\cos(a_i)=M \tag{5}$$

$$\sum_{i=1}^{N_1}(-1)^{i-1}\cos(na_i)+\sum_{i=N_1+1}^{N}(-1)^{i-(1+N_1)}\cos(na_i)=0 \tag{6}$$

where $n=5,7,\ldots,3N-2$ and N is odd

$$0\le M\le 2. \tag{7}$$

If A_1 is the amplitude of the fundamental component to be generated, then

$$A_1=\frac{4V_{\rm dc}}{\pi}\cdot M \tag{8}$$

$$0<\alpha_1<\alpha_2<\cdots<\alpha_{k+m}<\frac{\pi}{2} \tag{9}$$

where M is the modulation index and $N_1+N_2=N$, N_1 is the number of switchings, or angles placed between 0- and 1-p.u. levels and N_2 is the number of waveform transitions placed between 1- and 2-p.u. levels and α_i is the ith switching angle in the quarter period of the waveform. By solving the system of (5)–(6) with the constraint of (9), the required solutions can be obtained.

For different distribution ratios N_1/N_2, a different set of equations describing new waveforms is solved [23], [24], providing multiple solutions. The multiple sets obtained, overlap for different N_1/N_2 ratios over the range of modulation indices. The multiple solutions available for the five-level case are presented in [23].

C. Flying Capacitor Voltage Regulation

The charging and discharging of the FC takes place at the middle voltage levels ±1 p.u. when the load current flows through the FC and depends upon its direction. The voltage across the FC, which should be maintained at ±1 p.u., is affected by switching states V_2, V_3, V_6, and V_7 and can be regulated using the switching states that result in time intervals of charging and discharging being equal over a fundamental period. Due to symmetrical pulse patterns over the quarter of the period, equal time intervals of charging and discharging over a fundamental period can be achieved. A more detailed explanation of the control strategy, the SHE-PWM implementation and gating signal generation, is given in [15].

III. Voltage Ripple Compensation

A. Effect of DC-Link Harmonic Ripple

The Fourier analysis of the converter phase voltages under a constant dc-link voltage is

$$S\bar{W}=\begin{bmatrix}\sum_{m=1}^{\infty}A_n\sin(n\omega_1 t)\\ \sum_{m=1}^{\infty}A_n\sin\left(n\omega_1 t-\frac{2\pi}{3}\right)\\ \sum_{m=1}^{\infty}A_n\sin\left(n\omega_1 t-\frac{4\pi}{3}\right)\end{bmatrix} \tag{10}$$

where the coefficients of the nth harmonic are calculated through (5)–(6). Assuming a ripple harmonic frequency $\omega_r=2\pi r f_1$ and the magnitude of $4R\cdot V_{\rm dc}$ in the dc-link voltage, given by (11), low-order harmonics are generated in the output ac voltage due to the interaction of the spectral components of the output voltage (10) and the dc-link harmonics

$$V'_{\rm dc}=4\cdot V_{\rm dc}(1+R\sin(r\omega_1 t)). \tag{11}$$

The harmonics due to the DC-link ripple are located at frequencies $(n-r)\omega_1$ and $(n+r)\omega_1$ as sidebands to the spectral components of the output voltage of (10). The amplitude of the harmonics generated at $n+r$ and $n-r$ are in direct correlation to the amplitude of the nth harmonic (A_n) and their normalized amplitude given by $((2R)\cdot A_n)/(2)$.

The amplitudes A_n of the harmonics are well defined through the SHE-PWM formulation of (5) and (6) and the solutions used in each application. These additional harmonics also vary in terms of their sequence. The sequence of the spectral components due to the $(n+r)$ terms in the output, along with the DC-link voltage being common for all three-phases, remains the same as in the nth harmonic. However, the sequence of the spectral components due to the $(n-r)$ terms depend on the values of n and r. If $n>r$, then the sequence of the components remains the same with that of the nth harmonic, but if $n<r$, the harmonics generated have inverted sequences and a positive-sequence nth harmonic generates a negative-sequence $(n-r)$th harmonic, a negative sequence nth harmonic (if present) generates a positive-sequence $(n-r)$th harmonic while zero-sequence harmonics are not affected.

This can be a major issue as the interaction of low-order harmonics with the fundamental frequency component (in which case $n=1$ and $r>1$) generates quite significant negative-sequence components in the output voltage. In addition, when $n-r=\pm1$, spectral components in the fundamental frequency are generated, affecting the balancing of the phase voltages in the output of the converter. These harmonics can be positive, negative, or zero sequence depending on the combination of n and r.

B. ANPC Voltage Ripple Compensation

The main difference in the application of ripple compensation methods in the ANPC converter when compared to other multilevel topologies is the common dc link for all three phases of the converter and the redundancies in acquiring intermediate levels of the waveform. Both of these differences need to be considered for the dc-link voltage ripple compensation method.

When the converter generates either the top or the bottom level in the waveform V_1 and V_8, the dc link appears directly in the output of the phase and the waveform follows the waveform of (11). However, when the levels $\pm V_{\rm dc}$ appear in the output and the dc link is connected to the output (V_2 and V_7), the actual level of the waveform is

$$V_{\pm V_{\rm dc}} = 2 \cdot V_{\rm dc}[1 + R \cdot \sin(r\omega_1 t)] - V_{C_{\rm fc}}. \tag{12}$$

Considering that the voltage of the flying capacitor is regulated to the reference voltage of $V_{\rm dc}$, the dc-link ripple appears in the output as double the amplitude of the level of the converter

$$V_{\pm V_{\rm dc}} = V_{\rm dc}[1 + 2 \cdot R \cdot \sin(r\omega_1 t)] \tag{13}$$

The remaining states (V_3 and V_6) for this level do not require the dc-link voltage but are generated through the neutral point of the converter and the flying capacitor. The ripple of the dc link does not affect this voltage level and, hence, no compensation is required for these states.

The compensation method is based on a feedforward modification of the switching function of the converter based on the average and instantaneous values of the dc-link voltage [20]. The modulating function of the converter M is modified so that the ripple in the dc link does not generate low-order harmonics as

$$M' = \frac{M(t)V_{\rm dc}}{V_{\rm level}}. \tag{14}$$

In the five-level FC-based ANPC converter, this is separated in three distinct occasions. When the output of the converter is $\pm 2V_{\rm dc}$, then the modulation index is modified based on (12) and the modulating waveform is

$$M'_{\pm 2V_{\rm dc}}(t) = \frac{M(t)}{1 + R \cdot \sin(r\omega_1 t)}. \tag{15}$$

When the output of the converter is equal to $\pm V_{\rm dc}$, then when the converter switching state connects the output to the neutral point and the FC, then the converter switching function is not modified (V_3 and V_6) and

$$M'_{\pm V_{\rm dc}A}(t) = M(t) \tag{16}$$

whereas when the states that connect the dc link to the output are used (V_2 and V_7), the modified modulation function is given by

$$M'_{\pm V_{\rm dc}B}(t) = \frac{M(t)}{1 + 2R \cdot \sin(r\omega_1 t)}. \tag{17}$$

The switching signals are obtained by comparison of the switching angles from the modified modulation index with triangular waveforms defining the fundamental frequency and phase angle θ. When the dc link is constant or no compensation method is used, the solutions remain constant as shown in Fig. 2(a). When the compensation method is used, the sets of angles used from the lookup table are separated into the N_1 first angles which are modified through the application of (16) or (17) and the remaining N_2 angles that are modified through (15) as shown in Fig. 2(b).

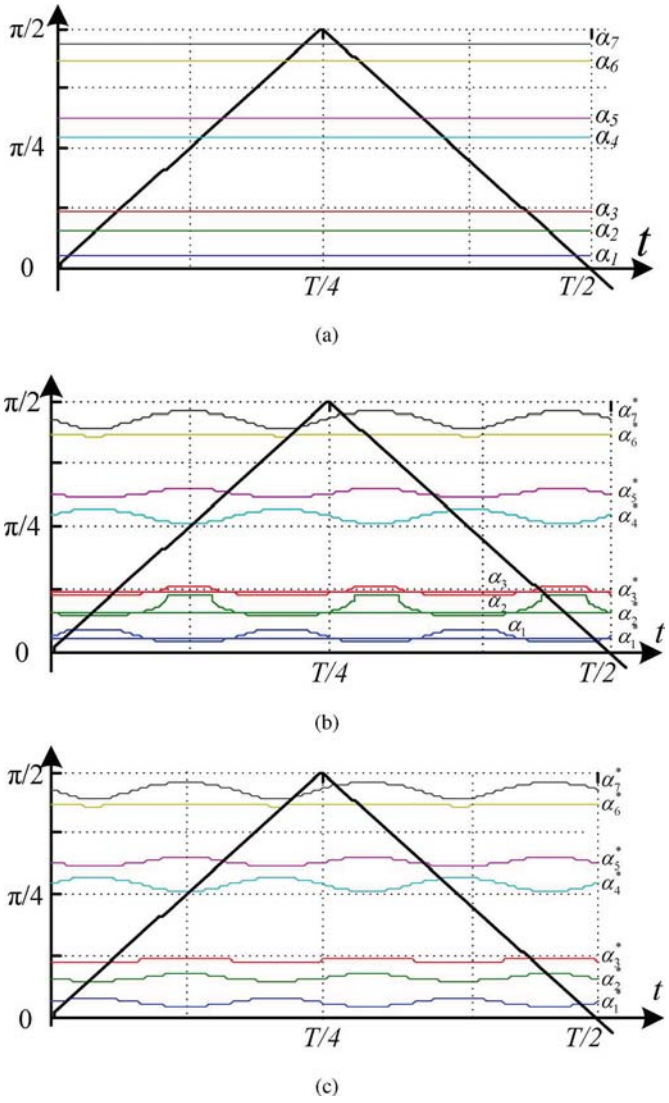

Fig. 2. Angle variation during the first half period of the waveforms. (a) Constant dc and no compensation. (b) Full compensation [(15)–(17)]. (c) Compensation based on (15).

C. Limitations and Variations in the Implementation

The application of the ripple compensation technique in multilevel converters under SHE-PWM poses a number of limitations. The percentage of ripple in the dc-link voltage, the operating point of the converter, and the solution pattern are limiting factors in the application of the technique. The first limitation appears through the variation of the N_1 angles where a dc-link ripple of amplitude R causes a variation in the modulating function of (17) that varies between

$$\frac{M}{1 + 2R} \leq M' \leq \frac{M}{1 - 2R}. \tag{18}$$

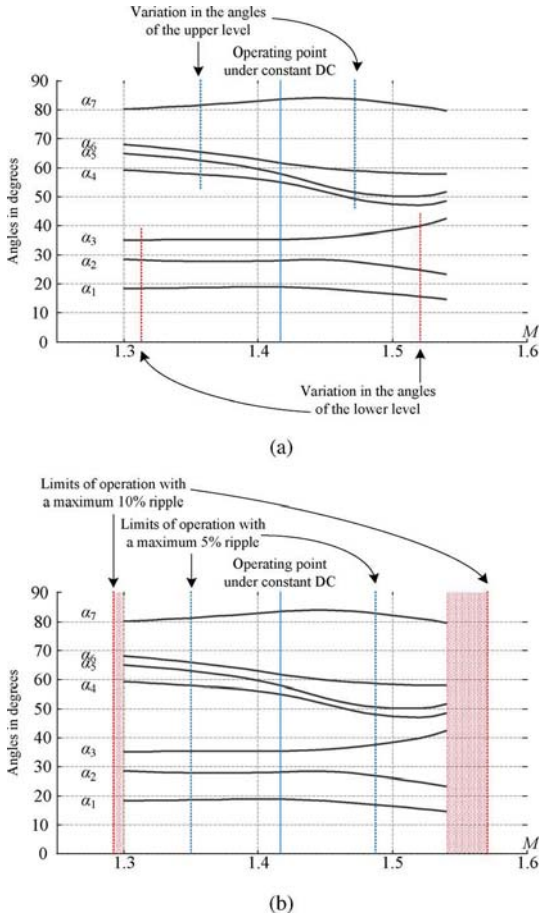

Fig. 3. Limits of dc ripple compensation method. (a) Full compensation. (b) Modified compensation.

The continuity of available solutions and the operating point of the converter can greatly vary the limits of (18), constraining the overall application of the method. In order to overcome this problem, all angles are chosen to vary based on the compensation of the top level given by (15). This is illustrated in Fig. 2(c). In this case, the limits of compensation are

$$\frac{M}{1+R} \leq M' \leq \frac{M}{1-R}. \tag{19}$$

Outside these limits, the application of the method can no longer fully compensate for the dc-link ripple, and low-order harmonics will appear in the output. However, these harmonics will be of much lower amplitude than in the case of uncompensated waveforms.

The limits of the application are illustrated in Fig. 3(a) and (b). If we consider the operating point under constant dc-link voltage to be given by the solid line in Fig. 3(a) and (b), a ripple on the dc link will result in a variation of the operating point for the N_1 and N_2 angles as shown in Fig. 3(a) and described by (15)–(17). As the lower angles N_1 have a higher compensation factor, they reach the limits in the continuity of the solution earlier than the upper angles (N_2).

The modification of the switching function, as proposed in (15), extends the operation of the compensation method as shown in Fig. 3(b). For the same operating point, the converter can operate with 5% ripple and the limits are reached when a harmonic component with approximately 10% for the particular operating point of the converter, is present in the dc link.

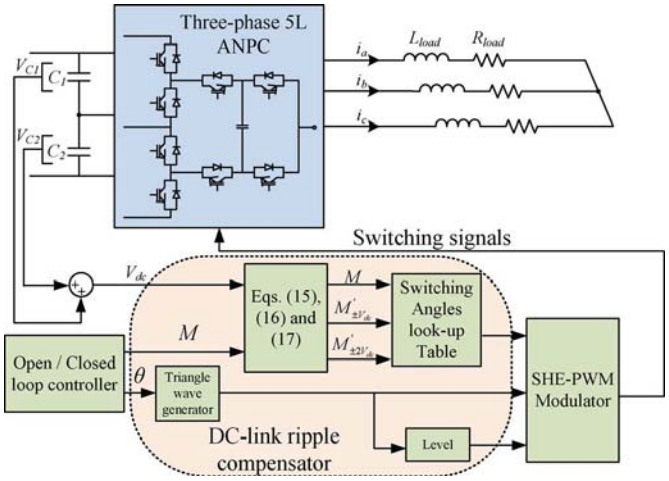

Fig. 4. Simulation and experimental setup of the five-level ANPC converter.

In addition, when the waveform is switching between the $\pm V_{\rm dc}$ and $\pm 2V_{\rm dc}$ levels, the selection of angle modification should be between (15)–(17) since the dc-link ripple is involved in multiple ways. In order to reduce the complexity of the selection scheme and to avoid multiple transitions between the levels, the modification of (15) is only applied to the angles as shown in Fig. 2(b). The angle modification of (15) lies always in between those of (16) and (17) and presents a valid compromise between the compensation requirements and the increased complexity of the selection scheme.

IV. Simulation Results

The dc-link voltage ripple compensation method for the five-level ANPC converter is simulated with MATLAB [27] and the PLECS toolbox [28]. A three-phase, five-level FC-based ANPC converter (Fig. 4) is simulated under a second harmonic dc-link ripple with an amplitude equal to 5% of the dc-link voltage. The converter is initially simulated with the ripple in the dc link and without the compensation method in Fig. 5(a). The presence of the second harmonic ripple generates low-order harmonics as well as a negative-sequence fundamental component resulting in unbalanced output voltage waveforms. The harmonic spectrum of the output voltage is shown in Fig. 5(b) and the phase currents of the converter are shown in Fig. 5(c) where the unbalance in the currents caused by the dc-link voltage ripple can be observed.

The operation of the five-level ANPC under the dc-link compensation method is shown in Fig. 6. The angles are modified based on the method of Section III-B with the switching angles being modified as shown in Fig. 3(a). Fig. 6(a) shows the output phase voltages and Fig. 6(b) shows the corresponding phase voltage harmonic spectra. The low-order harmonics as well as the unbalance due to the second harmonic ripple on the dc link are eliminated from the application of the compensation method. The additional harmonics that appear in the spectra around the noneliminated harmonics are due to the modification of the switching angles from the method which slightly modifies the quarter-wave symmetry assumed in the waveform formulation. The phase currents are given in Fig. 6(c).

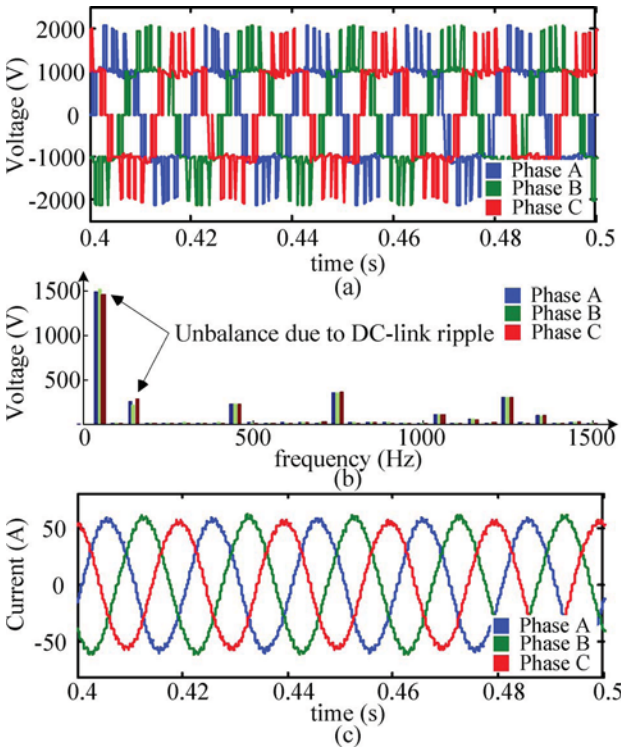

Fig. 5. Simulations results with 5% second harmonic ripple on the dc with no compensation. (a) Phase voltages. (b) Corresponding harmonic spectra. (c) Load currents.

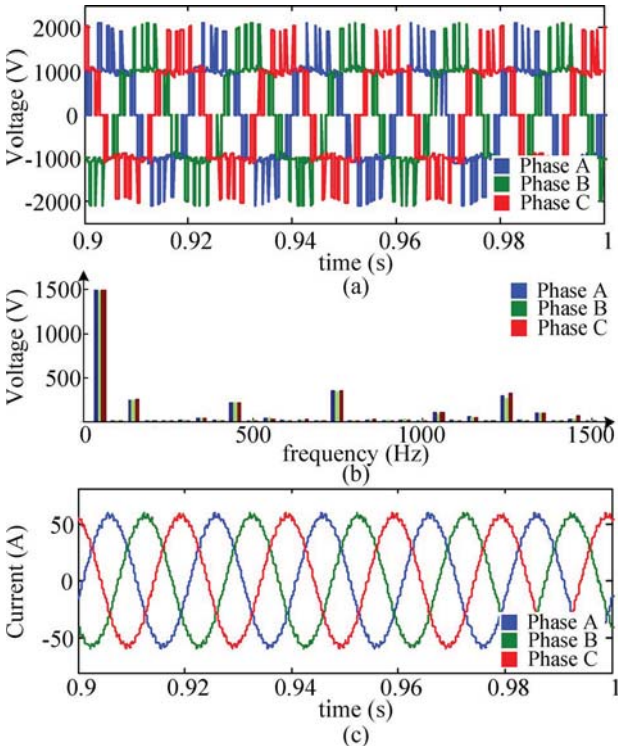

Fig. 6. Simulations results with 5% second harmonic ripple on the dc with full compensation. (a) Phase voltages. (b) Corresponding harmonic spectra. (c) Load currents.

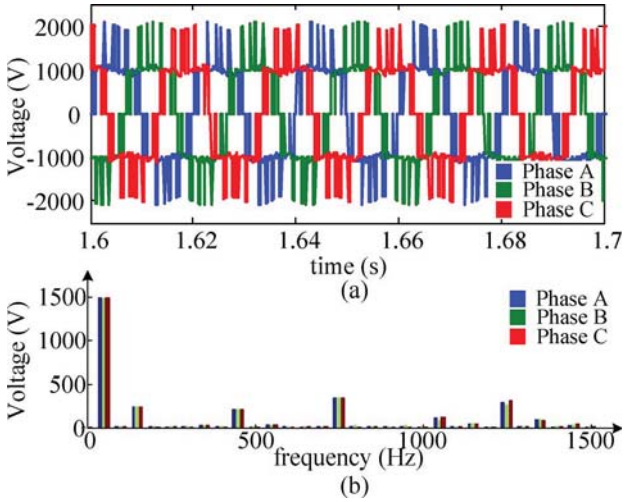

Fig. 7. Simulations results with 5% second harmonic ripple on the dc with modified compensation. (a) Phase voltages. (b) Corresponding harmonic spectra.

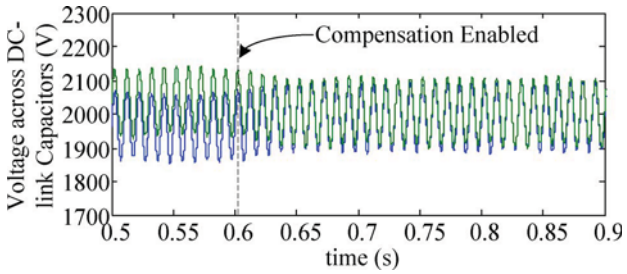

Fig. 8. Upper and lower dc-link capacitor voltages with dc-link voltage ripple. The compensation method is enabled at 0.6 s.

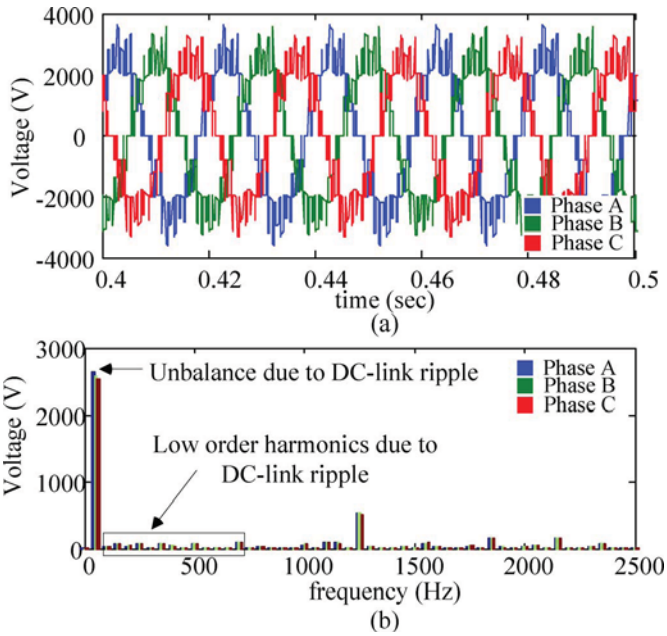

Fig. 9. Simulations results with 5% second and 5% sixth harmonic ripple on the dc without compensation. (a) Line-to-line voltages. (b) Corresponding harmonic spectra.

Fig. 7(a) and (b) shows the phase voltages and corresponding harmonic spectra of the method under the modified compensation of the method. The observed variance in the harmonic spectrum is acceptable and the modified method provides satisfactory compensation of the dc-link ripple harmonics when the full compensation method reaches its limits. The low-order harmonics present in the output current also affect the voltages of the dc link and result in deviation between the dc-link capacitors voltages.

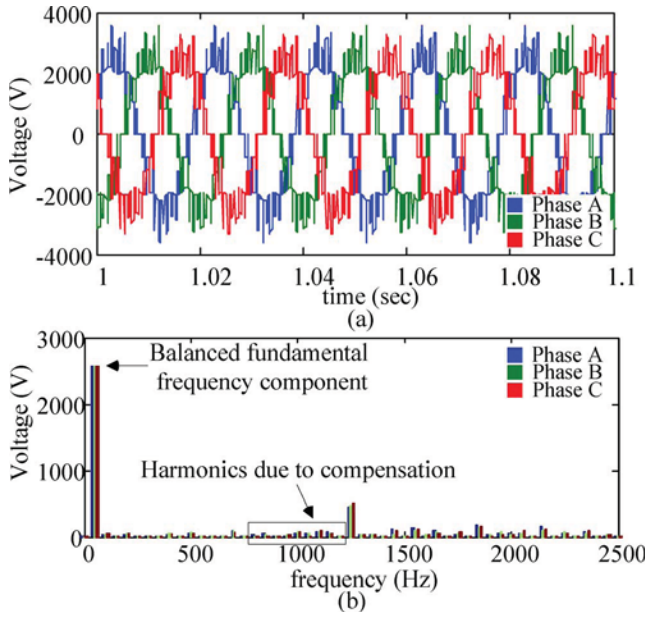

Fig. 10. Simulations results with 5% second and 5% sixth harmonic ripple on the dc with modified compensation. (a) Line-to-line voltages. (b) Corresponding harmonic spectra.

TABLE II
SPECIFICATIONS OF THE EXPERIMENTAL PROTOTYPE

Switching angles per quarter period	7
Flying capacitors	680 μF
DC-link capacitors	2000 μF
Load Resistance	R_{load}=22 Ω
Load Impedance	L_{load}=10mH
DC-link voltage	130 V
2nd harmonic component	5% of V_{dc}
6th harmonic component	5% of V_{dc}

The application of the compensation method also facilitates the balancing of the dc-link capacitors as shown in Fig. 8. Enabling the dc-link voltage ripple compensation method minimizes the drift between the upper and lower dc-link capacitor voltage and maintains the neutral point deviation to a minimum [26].

The system is also simulated for the simultaneous presence of a 5% second and a 5% sixth harmonic on the dc link. Fig. 9(a) shows the line-to-line voltages when no compenstation is used in the modulation scheme. The resulting low-order harmonics and unbalances in the fundamental frequency components can be observed in Fig. 9(b). The application of the compensation methods eliminates the unbalance and mitigates the harmonics to higher orders as shown in Fig. 10(a) and (b).

V. EXPERIMENTAL RESULTS

A three-phase five-level ANPC converter system was built in the laboratory to validate the presented FC control strategy. The control strategy was developed using MATLAB/SIMULINK and implemented with the dSPACE DS1104 board. The experimental results consider a second harmonic in the dc link with an amplitude equal to 5% of the dc-link voltage and a combination of a 5% second and 5% sixth harmonics simultaneously present on the dc-link voltage. The parameters of the laboratory

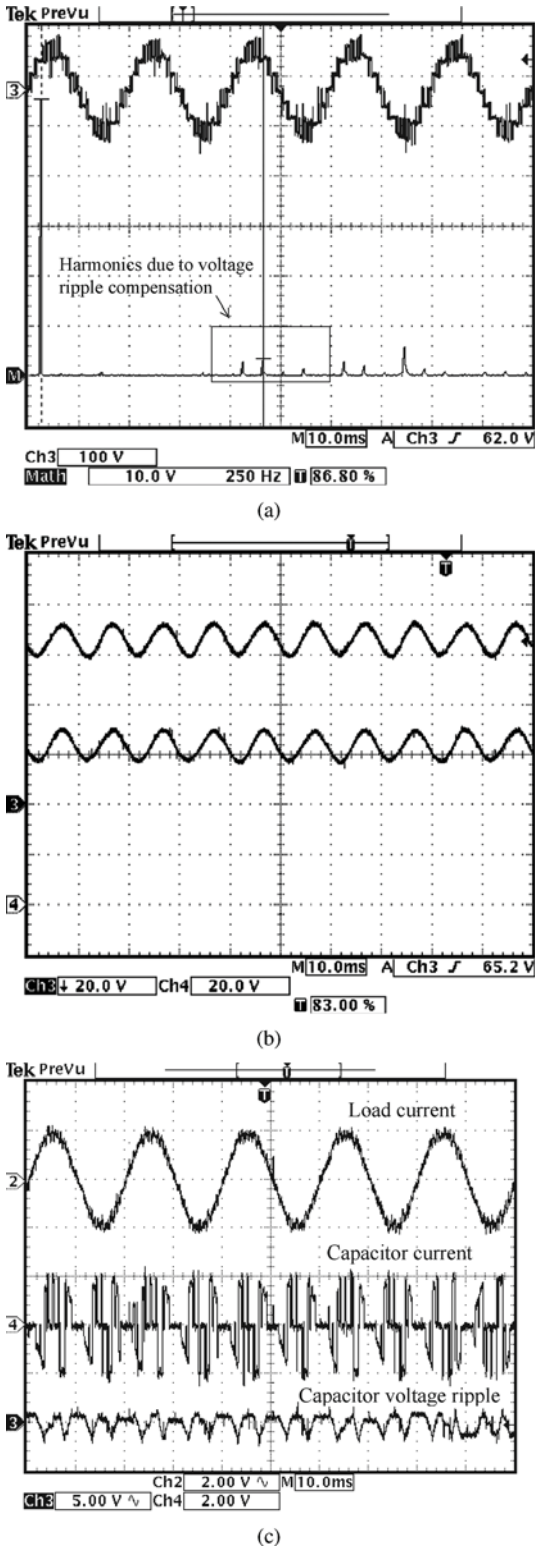

Fig. 11. Experimental results with 10% second harmonic ripple in dc-link voltage and compensation. (a) Phase voltage and associated harmonic spectrum. (b) Upper and lower dc-link capacitor voltages. (c) Output current (Channel2), current through FC (Channel4), and voltage ripple across the FC (Channel3).

prototype five-level ANPC converter used for the experimental verification of the dc-link voltage ripple are given in Table II.

A second harmonic on the dc link is initially considered. Due to the second harmonic in the dc-link voltage, a negative-sequence fundamental frequency component and a third harmonic

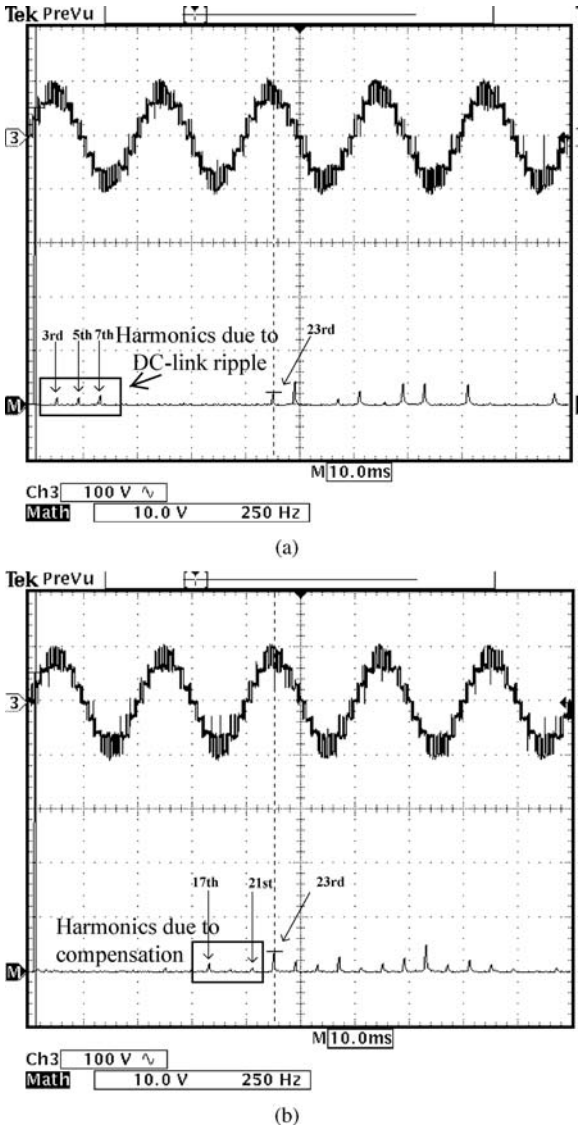

Fig. 12. Experimental results with 5% second and 5% sixth harmonic. Line-to-line voltages (a) without compensation and (b) with compensation.

are present in the output. The negative sequence generates unbalances in the waveform, and the third harmonic is present in the output of the converter since it is not of zero sequence. Fig. 11(a) shows the phase-output voltage and corresponding harmonic spectrum under the application of the compensation method when the dc-link voltage of Fig. 11(b) is imposed in the upper and lower capacitors. Fig. 11(b) shows that although the second-order harmonic in present on the dc link, the voltage of the two dc-link capacitors is balanced through the compensation method and, hence, the deviation of the neutral point is minimal.

Typical harmonics present in the dc-link voltage are lower order even harmonics [16], and the final case investigates the effect of a combined second and sixth harmonic in the dc link. When the compensation method was not applied, harmonics on the line-to-line voltage were present as shown in Fig. 12(a), and the application of the method successfully eliminates the low-order harmonics and the unbalance of the fundamental frequency component as shown in Fig. 12(b).

TABLE III
ABBREVIATIONS USED IN THIS PAPER

Abbreviation	Term
ANPC	Active Neutral Point Clamped
CHB	Cascaded H-bridges
CTL	Cascaded Two Level
FC	Flying Capacitor
LSC	Level Shifted Carriers
M^2LC	Modular Multilevel Converter
PSC	Phase Shifted Carriers
PWM	Pulse Width Modulation
SF	Switching Function
SHE	Selective Harmonic Elimination
SVM	Space Vector Modulation
VSC	Voltage Source Converter

VI. CONCLUSION

The presence of lower order harmonics in the dc-link voltage results in low-order harmonics in the output voltage which deteriorates the output voltage. This paper proposes a dc-link voltage ripple compensation method for the five-level FC-based ANPC converter under SHE-PWM. The method compensates for the dc-link ripple through a feedforward modification of the switching function of the converter.

The main difference with previous methods is that the compensation is specific to the levels of the waveform providing a variable modification for each of the converter levels. In addition, the waveform is modified based on the selection of redundant states which also regulates the neutral point voltage deviation. However, the method is limited by the range of solutions of the SHE-PWM technique. For this reason, a modification in the compensation method is proposed in order to extend the operating limits of the application. The results for both methods are verified through simulations. Experimental results from a three-phase laboratory prototype confirm the theoretical analysis.

APPENDIX A

Table III summarizes all of the abbreviations used in this paper.

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Sridhar R. Pulikanti (S'06–M'11) was born in Hyderabad, India. He received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, in 2003, the M.Sc. degree in electric power engineering from Chalmers University of Technology, Gothenburg, Sweden, in 2006, and the Ph.D. degree in electrical engineering from the University of Sydney, Sydney, Australia, in 2011.

Currently, he is a Research Fellow with the University of Wollongong, Wollongong, Australia. His research interests include hybrid and multilevel power converters, modulation techniques, and renewable energy conversion technologies.

Georgios Konstantinou (S'08–GS'11) received the B.Eng. degree in electrical and computer engineering from Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2007 and the Ph.D. degree in electrical engineering from the University of New South Wales (UNSW), Sydney, Australia, in 2012.

From 2008 to 2010, he was with the School of Electrical and Information Engineering, University of Sydney, Sydney, Australia. Currently, he is a Research Associate with the Australian Energy Research Institute , UNSW. His research interests include multilevel and hybrid converters, modular multilevel converters, renewable energy sources, and selective harmonic elimination (SHE-PWM) for power-electronics converters.

Vassilios G. Agelidis (SM'00) was born in Serres, Greece. He received the B.Eng. degree in electrical engineering from Democritus University of Thrace, Thrace, Greece, in 1988, the M.S. degree in applied science from Concordia University, Montreal, QC, Canada, in 1992, and the Ph.D. degree in electrical engineering from the Curtin University, Perth, Australia, in 1997.

From 1993 to 1999, he was with the School of Electrical and Computer Engineering, Curtin University. In 2000, he joined the University of Glasgow, Glasgow, U.K., as a Research Manager for the Glasgow-Strathclyde Centre for Economic Renewable Power Delivery. From 2005 to 2006, he held the inaugural Chair of Power Engineering in the School of Electrical, Energy and Process Engineering, Murdoch University, Perth. From 2006 to 2010, he held the EnergyAustralia Chair of Power Engineering at the University of Sydney. Currently, he is the Director of the Australian Energy Research Institute and Professor of Power Engineering in the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, Australia. He has authored/coauthored several journal and conference papers, as well as the book *Power Electronic Control in Electrical Systems* (Newnes, 2002).

Dr. Agelidis received the Advanced Research Fellowship from the U.K.'s Engineering and Physical Sciences Research Council (EPSRC-UK) in 2004. He was an Associate Editor of the IEEE POWER ELECTRONICS LETTERS from 2003 to 2005, and served as the Power Electronics Society's (PELS) Chapter Development Committee Chair from 2003 to 2005. He was the Vice President of Operations within the IEEE Power Electronics Society during 2006 to 2007, an AdCom member of IEEE PELS during 2007–2009, and Technical Chair of the 39th IEEE PESC'08, Rhodes, Greece. Since 2010, he has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.