View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by Research Online

University of Wollongong

Research Online

Faculty of Engineering - Papers (Archive)

Faculty of Engineering and Information Sciences

2009

Evaluation of silicon detectors with integrated JFET for biomedical applications

Mitra Safavi-Naeini
University of Wollongong, mitra@uow.edu.au

D. Franklin
University of Wollongong, danielf@uow.edu.au

Michael L. Lerch
University of Wollongong, mlerch@uow.edu.au

Marco Petasecca
University of Wollongong, marcop@uow.edu.au

Giorgio U. Pignatel
Università degli Studi di Perugia

See next page for additional authors

Follow this and additional works at: https://ro.uow.edu.au/engpapers

Part of the Engineering Commons

https://ro.uow.edu.au/engpapers/4175

Recommended Citation

Safavi-Naeini, Mitra; Franklin, D.; Lerch, Michael L.; Petasecca, Marco; Pignatel, Giorgio U.; Reinhard, Mark I.; Dalla Betta, G. F.; Zorzi, N.; and Rosenfeld, Anatoly B.: Evaluation of silicon detectors with integrated JFET for biomedical applications 2009, 1051-1055.
https://ro.uow.edu.au/engpapers/4175

Research Online is the open access institutional repository for the University of Wollongong. For further information contact the UOW Library: research-pubs@uow.edu.au

Authors
Mitra Safavi-Naeini, D. Franklin, Michael L. Lerch, Marco Petasecca, Giorgio U. Pignatel, Mark I. Reinhard, G. F. Dalla Betta, N. Zorzi, and Anatoly B. Rosenfeld

This journal article is available at Research Online: https://ro.uow.edu.au/engpapers/4175

Evaluation of Silicon Detectors With Integrated JFET for Biomedical Applications

M. Safavi-Naeini, *Student Member, IEEE*, D. R. Franklin, *Member, IEEE*, M. L. F. Lerch, *Member, IEEE*, M. Petasecca, *Member, IEEE*, G. U. Pignatel, *Member, IEEE*, M. Reinhard, *Member, IEEE*, G.-F. Dalla Betta, *Senior Member, IEEE*, N. Zorzi, and A. B. Rosenfeld, *Senior Member, IEEE*

***Abstract*—This paper presents initial results from electrical, spectroscopic and ion beam induced charge (IBIC) characterisation of a novel silicon PIN detector, featuring an on-chip n-channel JFET and matched feedback capacitor integrated on its p-side (frontside). This structure reduces electronic noise by minimising stray capacitance and enables highly efficient optical coupling between the detector back-side and scintillator, providing a fill factor of close to 100%. The detector is specifically designed for use in high resolution gamma cameras, where a pixellated scintillator crystal is directly coupled to an array of silicon photodetectors. The on-chip JFET is matched with the photodiode capacitance and forms the input stage of an external charge sensitive preamplifier (CSA). The integrated monolithic feedback capacitor eliminates the need for an external feedback capacitor in the external electronic readout circuit, improving the system performance by eliminating uncontrolled parasitic capacitances. An optimised noise figure of 152 electrons RMS was obtained with a shaping time of 2 μs and a total detector capacitance of 2pF. The energy resolution obtained at room temperature (21°C) at 27 keV (direct interaction of I-125 gamma rays) was 5.09%, measured at full width at half maximum (FWHM). The effectiveness of the guard ring in minimising the detector leakage current and its influence on the total charge collection volume is clearly demonstrated by the IBIC images.**

I. Introduction

NOISE is one of the fundamental limiting factors in the performance of radiation detectors. In order to achieve the best possible energy and timing resolution, it is essential to eliminate as much noise as possible. Modern solid-state radiation detectors and their associated readout electronics can now be fabricated on a common high-resistivity silicon substrate using a single manufacturing process [1]. This results in a reduction in the electronic noise, since the parasitic capacitance associated with preamplifier-detector connection is minimised.

Manuscript received July 12, 2008; revised October 09, 2008. Current version published June 10, 2009.

M. Safavi-Naeini, M. L. F. Lerch, M. Petasecca, and A. B. Rosenfeld are with the Centre for Medical Radiation Physics at the University of Wollongong, Australia.

D. R. Franklin is with the School of Electrical, Computer and Telecommunications Engineering at the University of Wollongong, Australia.

G. U. Pignatel is with the Università degli Studi di Perugia, Italy.

M. Reinhard is with the Australian Nuclear Science and Technology Organisation, Australia.

G. F. Dalla Betta is with University of Trento, Department of Information and Communication Technology, Italy.

N. Zorzi is with FBK-irst, Trento, Italy.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2009.2013949

Furthermore, it reduces the need for shielding against capacitively-coupled pickup noise [1] and simplifies the circuit process assembly [2], [3]. However, these benefits must be traded off against the increased complexity (and potentially cost) of fabrication. Therefore, the monolithic approach is normally only worth pursuing for detectors with a very low capacitance, such as pixel detectors and silicon drift chambers [4], [5].

Silicon PIN detectors are normally coupled to a charge-sensitive preamplifier circuit. In a standard detector preamplification configuration, this takes the form of a low-noise junction field-effect transistor (JFET) coupled to a specialised charge-sensitive operational amplifier such as the Amptek A250 with a capacitive feedback network. The idea of fabricating this JFET on high-resistivity silicon utilising detector-compatible processes dates back to the late 1980s. Early works by Radeka *et al.* [2] and Holland *et al.* [6] resulted in successful implementation of Single Sided JFETs (SSJFETs) using the same technological steps needed for producing Charge Coupled Devices (CCDs) [7]. Another example of a detector with embedded electronics (a Depleted Field Effect Transistor (DEPFET)) was proposed by Kemmer and Lutz and successfully fabricated [8], [1].

The detectors used in this paper are the result of ten years of research and development undertaken at FBK-irst (Trento, Italy) [9]. The results of experimental characterisation of these detectors, a selection of which are presented in this paper, will be used in the further development and enhancement of the devices and in the development of applications based on the device.

II. Device Description

The three-dimensional structure of the PIN and JFET detector is shown in Fig. 1, while Fig. 2 shows the layout of the monolithic circuit elements on the detector frontside. The device includes a PIN diode detector with a p^+ implantation on the top side of the chip (with an area of approximately of 2×0.4 mm^2), coupled to an integrated n-channel JFET.

The JFET is a based on a double-gate (tetrode) structure and is fabricated on high resistivity (6 kΩcm) 300 μm n-type substrate [10]. The JFET has radial symmetry and is realised by triple implants on the top side of the chip. The conducting n-channel is a phosphorus n-implantation, in which the drain, source (n^+) and top-gate (p^+) implants are embedded in successive concentric annular regions. Surrounding the n-channel is a p-well with an annular p^+ implantation which forms the back gate region.

The PIN diode's p^+ cathode, which collects the hole component of the event signal, is directly coupled to the JFET top

0018-9499/$25.00 © 2009 IEEE

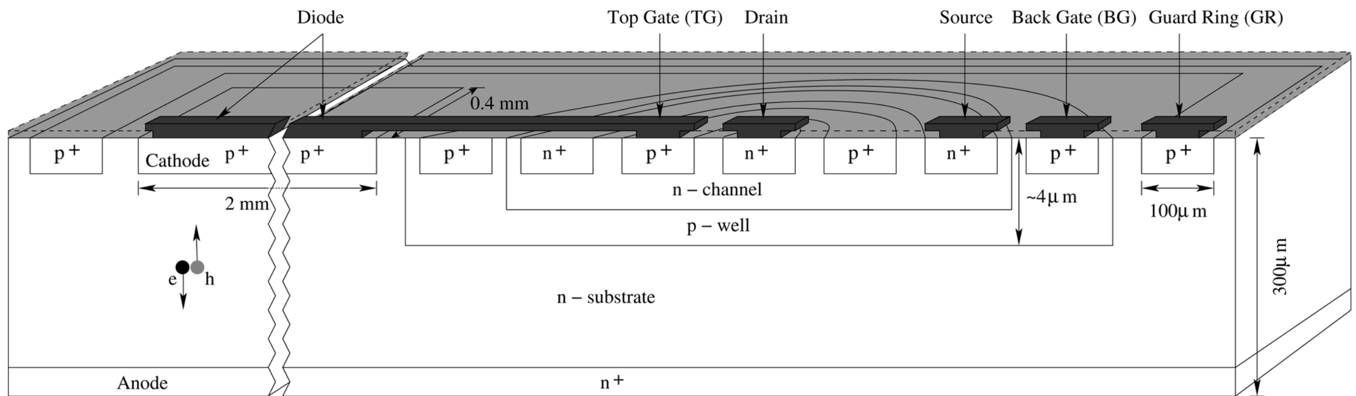

Fig. 1. PIN+JFET detector: cross-section (not to scale).

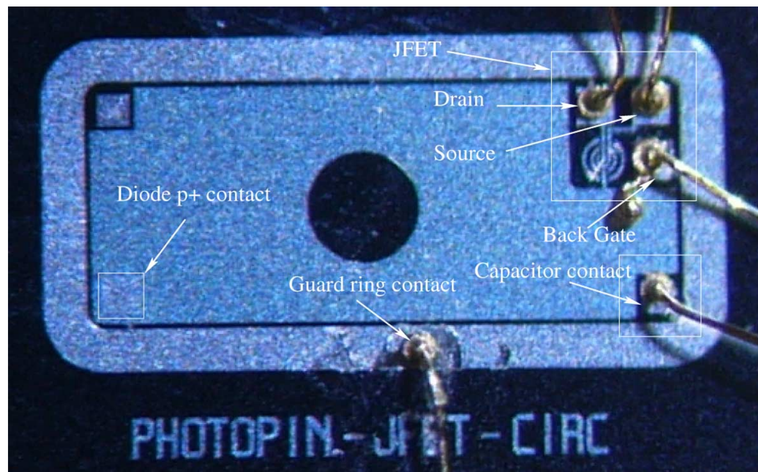

Fig. 2. Layout of the PIN+JFET structure.

gate through a metal strip [11]. A phosphorus-doped poly-silicon layer is present on the back-side to provide the n^+ substrate ohmic contact.

The JFET gate-source junction is forward biased and the drain current is stabilised by a low frequency feedback path to the JFET p^+ well contact (which serves as a secondary or back gate for the JFET). JFET channel conductivity is modulated by the bias voltages applied to the top gate and the p-well/back gate [11]. A 100 μm wide p$^+$ implanted guard ring surrounds the entire diode and JFET structure, collecting the leakage current and shaping the electric field. Since the detector is intended for spectroscopic applications which will require it to be coupled to a charge sensitive preamplifier (CSP), a feedback MOS capacitor of approximately 0.2 pF is incorporated in the device structure. The proximity of the feedback capacitor to the JFET minimises stray capacitance due to external wiring which would otherwise be needed [11]. A circular opening on the diode metal layer (300 μm diameter) is also present in the prototype samples and is used for evaluation of the electro-optical properties of the device.

The p-well allows the channel to be depleted simultaneously from both above and below, by applying the same negative voltage to the top gate and p-well contacts. Furthermore, it provides good confinement of the electrons flowing through the channel from source to drain, due to the high potential barrier existing at the channel-well junction [9].

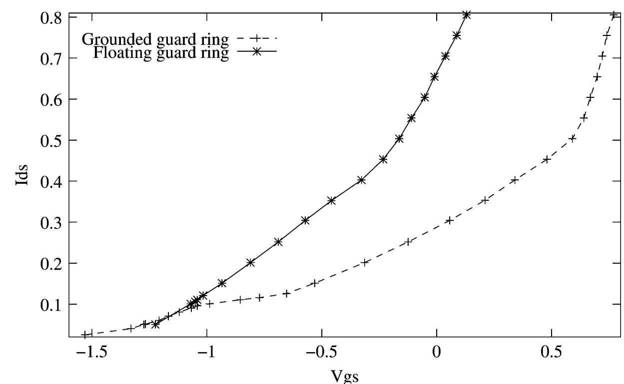

Fig. 3. JFET $V_{\rm gs} - I_{\rm ds}$ transfer characteristics. The bottom gate is grounded (0 V), the drain voltage is $+5$ V and the substrate was biased at 32 V.

III. Electrical Characterisation

The relation between $V_{\rm gs}$ (the potential between the top-gate and the source electrode) and drain-source current $I_{\rm ds}$ is shown in Fig. 3 (the drain voltage is held at 32 V and the p-well (back gate) is grounded). The curve exhibits the quadratic behaviour typical of field-effect transistors. The superficial component of the $I_{\rm ds}$, contributed by the leakage current is removed when the guard ring is grounded.

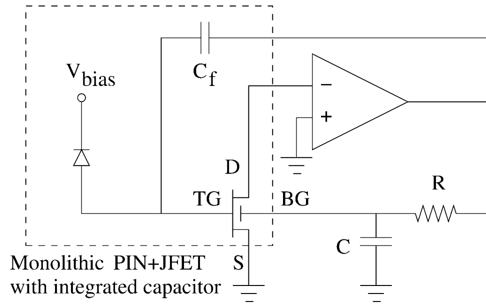

Fig. 4. Simplified schematic of the preamplifier circuit with the monolithic device replaced by an equivalent discrete-component model [11].

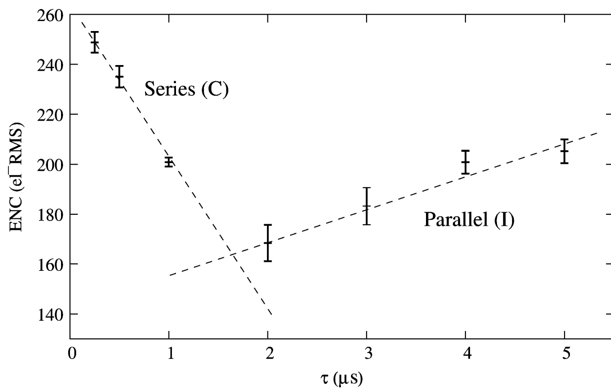

Fig. 5. Equivalent Noise Charge (ENC) measured for different shaping time constants. The fitted dotted lines show the parallel and series components of the ENC.

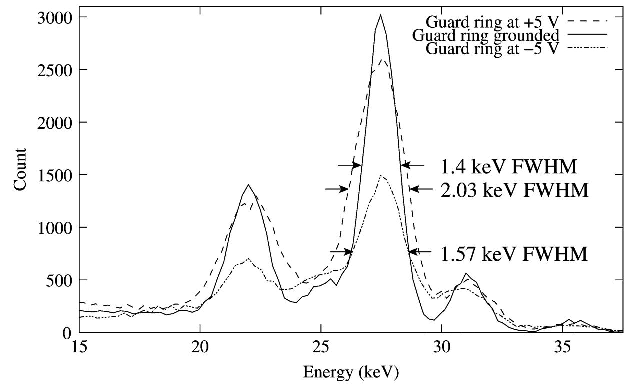

Fig. 6. Calibrated ^{125}I spectrum obtained from the PIN diode detector biased at 22 V with integrated JFET and capacitor. The frontside-illuminated gamma spectra acquired at three different guard ring potentials are shown superimposed. The best resolution was achieved when the guard ring is at zero volts.

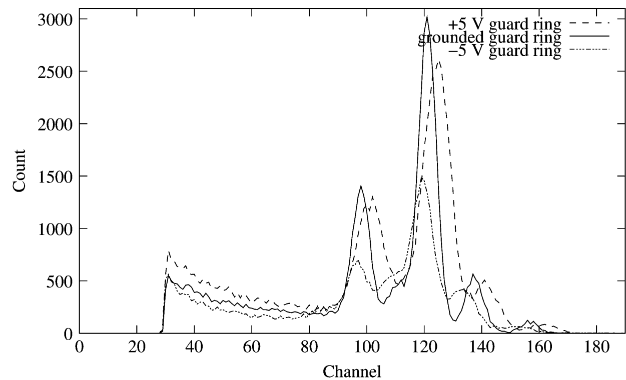

Fig. 7. Uncalibrated ^{125}I spectrum obtained with at various guard ring bias potentials. The progressive shift in the gain is due to the increase in the value of monolithic feedback capacitance as the guard ring potential becomes more positive.

Fig. 4 shows the complete preamplifier circuit, which utilises a 'double feedback' configuration [11]. The cathode (which collects the holes) is connected to the top-gate of the JFET, providing a path to the grounded source via the p-n gate-source JFET junction. The drain is coupled to the input of an A250 charge-sensitive preamplifier, whose output is capacitively coupled back to the top-gate of the JFET to complete the charge-integrating feedback loop. The resistive feedback path connecting the output of the A250 to the back-gate (BG) stabilises the drain current (I_d), which is strongly affected by variations in the quiescent leakage current [11].

A simplified schematic of the preamplifier circuit is shown in Fig. 4, where the device is modelled by the discrete components inside the dotted region.

A number of experiments were conducted to evaluate the electrical characteristics of the new detector. Since noise in semiconductor detectors is a major performance limitation, it is necessary to evaluate those properties which contribute the most to its noise performance [12], [13]. Equivalent noise charge (ENC) is a measure of the electronic noise of the detector. The two principal components of the ENC are leakage current (modelled as a parallel-connected noise source), and the bulk capacitance (modelled as a series-connected noise source) [14].

The asymptotic straight lines in Fig. 5 show the individual contribution to the total noise from the series and parallel components. Series noise is dominant for short shaping times, while for long shaping times, the parallel component dominates. A minimum ENC of 152 electron RMS is obtained with a shaping time of 2 μs. This shaping time is therefore used for the spectroscopic characterisation in Section IV.

IV. Spectroscopic Characterisation

The spectroscopic response of the detector to low energy γ-rays via direct interaction was measured using an ^{125}I source (27.47 keV) at room temperature (21°C). The pulser noise width was previously found to be 1.25 keV (4.55%, also at 27.47 keV) [15]. The resulting (calibrated) spectra are shown in Fig. 6, with the guard ring potential set to -5 V, 0 V and $+5$ V and the detector reverse biased at 22 V. The best energy resolution achieved was 1.40 keV full width at half maximum (FWHM) (or 5.09%) at 27.47 keV, which was obtained with a grounded guard ring.

This is because the guard ring can only efficiently remove surface leakage current when biased at the same potential as the cathode. Therefore, when the guard ring is grounded, leakage current (and noise) are minimised and energy resolution is maximised.

The same spectra are shown without calibration in Fig. 7. The progressive right shift in the spectrum as the guard ring potential becomes more positive shows that the gain of the charge-sensitive preamplifier circuit has also increased. This is because the

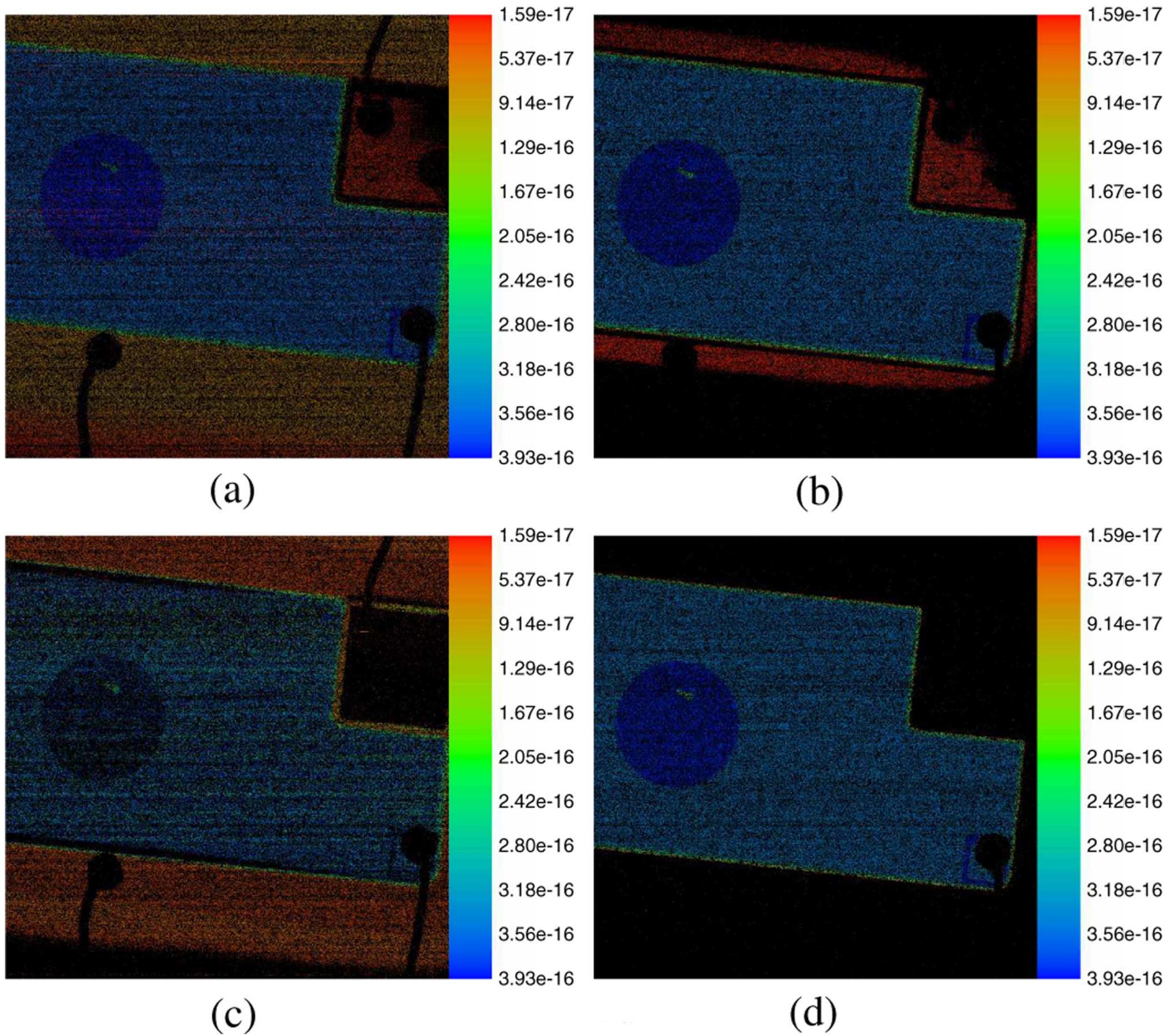

Fig. 8. IBIC images of the the photodetector biased at 10 V and 20 V. Black represents zero charge collection, while red, orange, yellow, green and blue indicate areas with progressively greater levels of charge collection. The colourmap shows the charge calculated for each colour in coulomb. (a) Underdepleted photodetector biased at 10 V-floating guard ring, (b) Underdepleted photodetector biased at 10 V-grounded guard ring, (c) Fully depleted photodetector biased at 20 V-floating guard ring, (d) Fully depleted photodetector biased at 20 V-grounded guard ring.

capacitance of the monolithic feedback capacitor $\mathrm{C_f}$ has effectively decreased in value due to the modification of the depletion under the p^+ region of the detector close to $\mathrm{C_f}$, thereby increasing gain (since the gain of a charge-sensitive amplifier is proportional to $1/C_f$).

V. IBIC Results

The charge collection pattern in the PIN/JFET detector structure was investigated using ion beam induced charge (IBIC) imaging [16]. IBIC measurements were performed using the Australian Nuclear Science and Technology (ANSTO) microprobe [17], where a 3 MeV He^+ beam with a spot size of 12 μm was scanned over the detector with a normal incident angle to the detector frontside (cathode). A spectroscopic shaping amplifier (CANBERRA 2025) was used for subsequent charge pulse amplification. Spectroscopic calibration was performed using a precision pulse generator and the low energy gamma peak from an ^{241}Am source. The detector and its readout circuit was positioned in an evacuated chamber, reverse-biased at various potentials between 0 and 50 V, and scanned in a 512×512 pixel matrix.

Fig. 8 shows four IBIC images in which the detector was biased below and above the full depletion voltage and the guard ring was either floating (Figs. 8(a) or (c)) or grounded (Figs. 8(b) and (d)). The IBIC maps clearly show the effect of the guard ring on the charge transport properties of the detector: when the guard ring is grounded, no charge is collected around the edge of the detector. The circular area visible within the p^+ region is caused by a fabricated gap in the aluminium metallisation, providing an optical window for electro-optical testing. The lack of aluminium layer results in a higher deposited energy (dark blue) in the photodetector.

The square region in the upper right-hand corner of the detector frontside (shown in Figs. 2 and 8) is the monolithic JFET. The bonding pads (ohmic contacts) are visible as small dark regions in the IBIC images due to their total lack of charge collection. As the bias voltage increases, the collected charge from the area under the JFET (p-well) decreases, reaching zero at 20 V. As shown in Fig. 1, the back gate contact (which is another p^+ region) surrounds the JFET's main electrodes. Therefore, the back gate contact behaves as a pseudo-guard ring around the JFET.

There are three separate P-N junctions in this device, each of which should be considered in order to fully understand the charge collection profile seen in the IBIC images. Specifically, these are the junctions between the cathode and anode, the guard ring and anode, and the pseudo-guard ring (p-well) and anode. When the bias potential is less than that required for full depletion, some of the electron hole pairs generated under the latter two junctions are collected by the cathode/anode junction (diffusion), and read out through the charge sensitive preamplifier circuitry. This is clearly seen across the partly illuminated JFET structure in Figs. 8(a) and (b): charge collection is greatest at the corner of the JFET which is closest to the p^+ detector region (the upper-left corner of the square area), and zero at the opposite corner.

As the bias potential increases, all three p-n junctions approach full depletion. Therefore, the electron-hole pairs which are generated within the substrate drift to the closest respective p^+ regions, and only those collected by the p^+ detector region are read out by the charge sensitive preamplifier. This lack of collected charge from underneath the JFET region is seen in Figs. 8(c) and (d), where the square area corresponding to the JFET is uniformly black. However, since the detector is designed to be illuminated from the backside, this apparent dead region will not significantly impede the collection of charge carriers at the detector frontside.

VI. Conclusion

The PIN photodiode with monolithic n-type JFET and MOS capacitor presented in this paper is a scalable design which is ideally suited for use in both low energy X-ray and high energy gamma-ray imaging (the latter requiring the device to be used in conjunction with a scintillator crystal).

The integration of a JFET and monolithic capacitor results in an excellent low energy gamma resolution, mainly due to the reduction of the electronic noise. The IBIC images show a uniform charge collection in the p^+ detector region, while grounding the guard ring removes the collected charge around the detector edge. The noise level of a single pixel $(152\,\mathrm{e}^-)$ is comparable to systems with non-integrated readout electronics. However, the ultimate objective is to extend this design to a pixellated detector array (of 8×8 or 16×16 pixels) for medical and spectroscopic applications in which the use of fully-external electronics is undesirable due to the variability of parasitic capacitances in the external feedback path. The use of an integrated JFET and monolithic feedback capacitor therefore will provide improved uniformity of gain across all pixels.

The effect of guard ring biasing on the MOS capacitance and therefore the detector resolution can be easily reduced by moving the capacitor away from the guard ring. The JFET could be surrounded by a low resistivity n^{++} pocket to effectively isolate it from the rest of the device.

Acknowledgment

The authors wish to express their appreciation to FBK-irst Italy for fabricating and processing and to Optoi Italy for assembling and packaging the samples. The authors would like to thank Dr. R. Siegle and Prof. D. Cohen for their support and assistance with the heavy ion experiments at ANSTO.

References

[1] G. Lutz, *Semiconductor Radiation Detectors*, 1st ed. New York: Springer, 1999, ch. 8, pp. 229–238.
[2] V. Radeka, P. Rehak, S. Rescia, E. Gatti, A. Longoni, M. Sampietro, G. Bertuccio, P. Holl, L. Struder, and J. Kemmer, "Implanted silicon jfet on completely depleted high-resistivity devices," *IEEE Electron Device Lett.*, vol. 10, no. 2, pp. 91–94, 1989.
[3] E. Pinotti, H. Bräuninger, N. Findeis, H. Gorke, D. Hauff, P. Holl, J. Kemmer, P. Lechner, G. Lutz, W. Kink, N. Meidinger, G. Metzner, P. Predehl, C. Reppin, L. Strüder, J. Trümper, C. V. Zanthier, E. Kendziorra, R. Staubert, V. Radeka, P. Rehak, G. Bertuccio, E. Gatti, A. Longoni, A. Pullia, and M. Sampietro, "The pn-ccd on-chip electronics," *Nucl. Instr. Meth. A*, vol. 326, no. 1–2, pp. 85–91, 1993.
[4] E. Gatti, P. Rehak, A. Longoni, J. Kemmer, P. Holl, R. Klanner, G. Lutz, A. Wylie, F. Goulding, P. N. Luke, N. W. Madden, and J. Walton, "Semiconductor drift chambers," *IEEE Trans. Nucl. Sci.*, vol. 32, no. 2, pp. 1204–1208, Apr. 1985.
[5] G.-F. D. Betta, M. Boscardin, L. Bosisio, P. Gregori, L. Pancheri, C. Piemonte, L. Ratti, G. Verzellesi, and N. Zorzi, "Monolithic integration of detectors and transistors on high-resistivity silicon," *Nucl. Instr. Meth. A*, vol. 579, pp. 658–663, 2007.
[6] S. Holland, "An ic-compatible detector process," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 1, pp. 283–289, Feb. 1989.
[7] S. E. Holland, D. E. Groom, N. P. Palaio, R. J. Stover, and M. Wei, "Fully depleted, back-illuminated charge-coupled devices fabricated on high-resistivity silicon," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 1, pp. 225–238, Feb. 2003.
[8] J. Kemmer, G. Lutz, U. Prechtel, K. Schuster, M. Sterzik, L. Strüder, and T. Ziemann, "Experimental confirmation of a new semiconductor detector principle," *Nucl. Instr. Meth. A*, vol. 288, pp. 92–98, 1990.
[9] G. F. D. Betta, G. Verzellesi, G. U. Pignatel, S. Amon, M. Boscardin, and G. Soncini, "Design of an n-channel jfet on high-resistivity silicon for radiation-detector on-chip front-end electronics," *Nucl. Instr. Meth. A*, vol. 567, pp. 368–371, 2006.
[10] G.-F. D. Betta, C. Piemonte, M. Boscardin, P. Gregori, N. Zorzi, A. Fazzi, and G. U. Pignatel, "An improved pin photodetector with integrated jfet on high-resistivity silicon," *Nucl. Instr. Meth. A*, vol. 567, pp. 368–371, 2006.
[11] A. Fazzi, G. F. D. Betta, and G. U. Pignatel, "Pin diode and integrated jfet on high resistivity silicon: A new test structure," in *Proc. Nucl. Sci. Symp. Conf. Rec.*, 2001, vol. 1, pp. 219–222, IEEE.
[12] R. Orito, H. Nishimura, K. Hattori, H. Kubo, K. Miuchi, T. Nagayoshi, Y. Okada, H. Sekiya, A. Takada, A. Takeda, and T. Tanimori, "Performance of large area si pin photo diode array," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, 2005, vol. 5, pp. 2993–2997, IEEE.
[13] T. Frach, W. Ruetten, K. Flieder, G. Maehlum, T. Solf, and A. Thon, "Assessment of photodiodes as a light detector for pet scanner," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, 2004, vol. 7, pp. 4177–4181, IEEE.
[14] C. Allier, H. Valk, J. Huizenga, V. Bom, R. Hollander, and C. van Eijk, "Comparative study of silicon detectors," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 576–580, Jun. 1998.
[15] M. Safavi-Naeini, M. L. F. Lerch, M. Petasecca, G. U. Pignatel, and A. B. Rosenfeld, "Evaluation of pixellated, back-sided planar photodetectors for high-resolution imaging instrumentation," *Nucl. Instr. Meth. A*, vol. 589, pp. 259–267, 2008.
[16] M. Jakšic, I. Bogdanović, M. Bogovac, S. Fazinić, S. Galassini, K. Kovačević, C. Manfredotti, and E. Vittone, "Testing of radiation detectors by ibic imaging," *Nucl. Instr. Meth. B*, vol. 113, pp. 378–381, 1996.
[17] R. Siegele, D. D. Cohen, and N. Dytlewski, "The ansto high energy heavy ion microprobe," *Nucl. Instr. Meth. B*, vol. 158, pp. 31–38, 1999.