A Four-Quadrant Switched Capacitor DC-DC Convertor for Use in Lab-Grade Potentiostats

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***Abstract*—This paper presents a low-power potentiostat based on a four-quadrant switched capacitor DC-DC convertor, optimized for a high overall efficiency. The potentiostat targets output currents in the range of $1\,\mu\mathrm{A}$ to $1\,\mathrm{mA}$ and achieves a compliance voltage of $\pm 2.5\,\mathrm{V}$. The system is designed and simulated in a $0.35\,\mu\mathrm{m}$ process.**

I. Introduction

THE design of modern sensors is driven towards more power efficient applications. A large class of sensors is based around the measurement of concentrations of compounds in a solution, which is typically the electrolyte inside an electrochemical cell. Voltammetric methods use the relationship between the current through this electrochemical cell, and the voltage across its electrodes to derive useful information about concentrations in the electrolyte [1].

The device used to apply the current and voltage to the cell is called a potentiostat. Voltammetric setups often use three-electrode systems, where power is applied to one pair of electrodes, and the resulting voltage drop is sensed across another. The first and simplest designs of potentiostats use an operational amplifier to power the cell, as shown in figure 1a. Op-amps are however not suited to supply power across a large range of output voltages, resulting in a large power dissipation inside the amplifier.

A common alteration to the basic op-amp architecture of figure 1a is to use a seperate linear output stage to power the cell [2], [3]. This allows the static power consumption of the op-amp to be reduced as it no longer has to supply a large current to the load, thereby decreasing the power consumption of the potentiostat.

In literature, several methods have been proposed to further increase the efficiency. In [4], the static power consumption of the op-amp is completely eliminated by replacing it by a latched comparator (shown in figure 1b). For integrated applications, techniques like bulk-driven amplifiers [5] enable the design of potentiostats at very low supply voltages, automatically increasing the efficiency of the output stage. Both of these techniques are however fundamentally limited by their linear output stage. They rely on bringing the supply voltage as close as possible to the required output voltage, which means these solutions have to be tailored to a specific application.

The use of a switching instead of a linear output stage, allows to decouple the efficiency from the required output voltage of the potentiostat. Ghanbari et al. [6], [7] therefore respectively propose to use a continuous or discontinuous conduction mode buck convertor in the output stage of the potentiostat. This significantly increases the efficiency of the potentiostat.

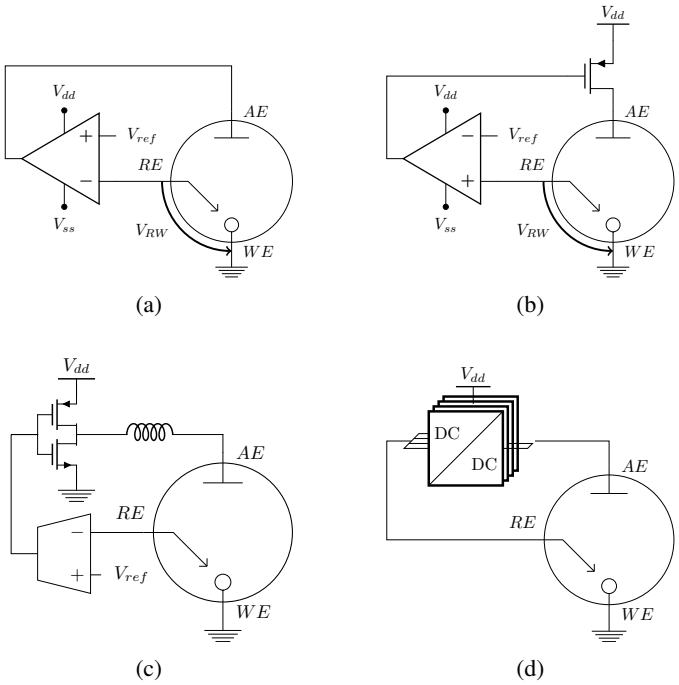


Fig. 1: (a) Basic operational amplifier architecture (b) architecture with seperate linear output stage (c) buck convertor based architecture (d) proposed solution

In reality, both electrochemical cells that require power as cells that deliver power exist, and so a truly universally employable potentiostat has to achieve a four-quadrant operation. Although operational amplifiers (figure 1a) are able to provide a four quadrant operation, they are unable to harvest energy from an electrochemical cell. Due to the transistor in the output stage, option 1b is only able to source current at positive output voltages. Even though two- and four-quadrant buck convertors exist, the solution in figure 1d only offers a single-quadrant operation.

This paper describes the design of a potentiostat based around a four-quadrant switched capacitor (SC) DC-DC convertor. Thanks to the switching nature of this convertor, this potentiostat is expected to have a good overall efficiency. Moreover, this potentiostat should be also be able to harness power from the electrochemical cell. The SC DC-DC convertor is designed and simulated in an ON Semiconductor $0.35\,\mu\mathrm{m}$ technology.

The rest of this paper is organised as follows. Section II

discusses voltammetric sensors and their requirements. Section III digs deeper into the requirement of a four quadrant operation, and its implications on the design of a SC DC-DC convertor. Section IV covers the transistor level design of the potentiostat. Finally, section V shows the results of the simulation in SPICE.

II. System requirements

Voltammetric methods observe the current through an electrochemical cell in function of the voltage across its electrodes. In a three electrode setup, a potentiostat attempts to make the voltage between the working electrode (WE) and the reference electrode (RE) track a reference voltage V_{ref} by sending a current into the auxiliary electrode (AE). The reference electrode is connected to a very high input impedance, such that all current going into the auxiliary electrode flows through the working electrode.

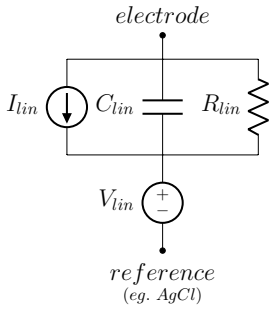


Fig. 2: Half-cell model

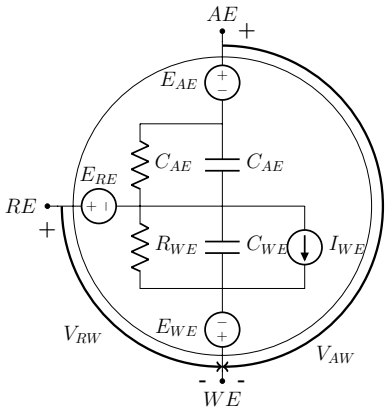


Fig. 3: Three electrode cell model

Although the relationship between the current through and the voltage across an electrode is heavily nonlinear [1], it is possible to linearize an electrode around an operating point. A linearized model of an three electrode cell is given by figure 3, and consists of three half-cell models (WE, RE, AE)[8], [9]. Both the working and the counter electrode contain a resistor and a capacitor. These respectively represent the ease with which the electrode conducts current, and the charge build-up between the electrode and the electrolyte. Since the reference electrode is very small and it does not conduct any current, the resistor and capacitor are omitted. Each electrode is linearised at some voltage E_{lin} and bias current I_{lin}.

The linearized model clarifies how the sign and magnitude of the output voltage and current, are mainly defined by the choice of electrodes. In general, the potentiostat will have to be able to source and sink currents at both positive and negative output voltages in order to be able to use it in combination with a wide variety of electrochemical cells.

Table I lists the targeted specifications for this design. The potentiostat has to achieve a compliance voltage of $-2.5\,\mathrm{V}$ to $2.5\,\mathrm{V}$, which is sufficient for most watery solutions [10]. The convertor has to be able to achieve efficiencies which are considerably better than those of an operational amplifier, for output currents between $1\,\mathrm{mA}$ and $1\,\mu\mathrm{A}$. A maximum $5\,\mathrm{mV}$ output ripple is desired for the potentiostat to accurately follow the reference voltage V_{ref}. The convertor should be able to accurately reproduce variations in the reference voltage up to a frequency of $100\,\mathrm{Hz}$.

TABLE I: Specifications for the potentiostat

Specification	Value
$I_{out,\ max}$	$\pm 1\,\mathrm{mA}$
$I_{out,\ min}$	$\pm 1\,\mu\mathrm{A}$
V_{AW}	$\pm 2.5\,\mathrm{V}$
V_{RW}	$\pm 2.5\,\mathrm{V}$
$V_{RW,\ ripple}$	$5\,\mathrm{mV}$
$f_{ref,\ max}$	$100\,\mathrm{Hz}$
Chip area	$3\,\mathrm{mm}^2$

Finally, since both the capacitance C_{lin} and the current I_{lin} are related to the surface of the electrode, it is assumed that the following relation holds:

$$\frac{C_{lin}}{I_{lin}} \approx 1\frac{\mu A}{nF} \tag{1}$$

III. Architecture level design

Whereas two quadrant convertors are a well established topic within the design of SC DC-DC convertors [11], [12], four-quadrant convertors have been relatively untouched upon. From the point of view of the three-electrode cell, the four-quadrant operation can be achieved in several ways.

A first option to achieve a four-quadrant operation is to use a symmetrical supply rail at -3.3 and $3.3\,\mathrm{V}$. The use of two seperate rails causes the voltage swing on the capacitor plates to lie anywhere between $-3.3\,\mathrm{V}$ and $3.3\,\mathrm{V}$. Since the breakdown voltage in the used $0.35\,\mu\mathrm{m}$ technology is only $3.6\,\mathrm{V}$, many switches in the convertor will have to be implemented as either cascodes or thick-oxide transistors. This will require additional area, and it complexifies the driving of the switches.

A better alternative is to use only a single supply rail, and to connect the second terminal of the output (in this case the working electrode) to the $3.3\,\mathrm{V}$-rail or ground, depending on whether a positive or a negative output voltage is required. Figure 4 presents a very simple model of this convertor, consisting of an ideal voltage conversion by a ratio VCR_i, which is determined by the topology, and a finite output resistance R_{out} [13]. The naming convention for the four-quadrant operation is shown in figure 5.

Since three-electrode cells can both function as an electrolysis as a galvanic cell, the efficiency of the convertor in quadrant I and III is defined differently from the efficiency in quadrant II and IV:

$$\eta_{1,\ 3} = \frac{P_{cell}}{P_{cell} + P_{losses}} = \frac{V_{out} * I_{out}}{V_{out} * I_{out} + P_{losses}} \tag{2}$$

$$\eta_{2,\ 4} = \frac{P_{cell} - P_{losses}}{P_{cell}} = \frac{V_{out} * I_{out} - P_{losses}}{V_{out} * I_{out}} \tag{3}$$

The potentiostat implements a gearbox convertor in order to achieve a high efficiency over a wide range of output voltages [14]. Suitable topologies for the gearbox are found by listing

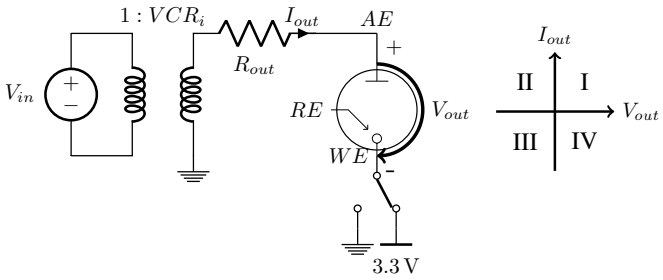


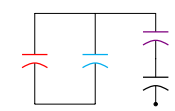
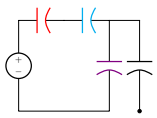
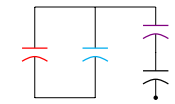
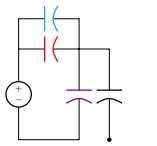
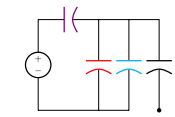
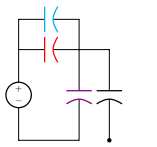
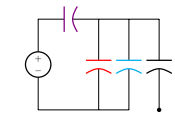
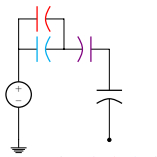
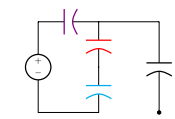
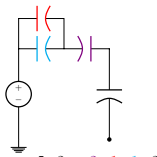
Fig. 4: DC-DC convertor model

Fig. 5: Four-quadrant operation

several options for every VCR_i, for which unfortunately no exhaustive strategy exists[15]. The different topologies for a single VCR are compared to each other using charge flow analysis [16]. Different topologies are combined to a gearbox based on their similarity, which reduces the complexity of the driving circuits. Table II for example shows that T1 and T2 have ϕ_1 in common. Furthermore, capacitor $C1$ always transfers the biggest charge in each of the topologies. These design strategies ensure that a component sizing exists which is beneficial for each of the topologies.

In order to limit its complexity, the gearbox implements 10 VCR_i's using 3 flying capacitors, as indicated in the left hand side of table II. Due to the switch at the working electrode, every topology realises two conversion ratio's VCR_i and $VCR_i - 1$.

TABLE II: Topologies in the gearbox

Name	VCR_i	ϕ_1	ϕ_2
T1	$\frac{1}{5}$ $\frac{-4}{5}$	 $\vec{a_c} = [0\ \frac{2}{5}\ \frac{-1}{5}\ \frac{-1}{5}\ \frac{2}{5}]$	 $\vec{a_c} = [\frac{-1}{5}\ \frac{-2}{5}\ \frac{1}{5}\ \frac{1}{5}\ \frac{3}{5}]$
T2	$\frac{1}{3}$ $\frac{-2}{3}$	 $\vec{a_c} = [0\ \frac{1}{3}\ \frac{-1}{6}\ \frac{-1}{6}\ \frac{1}{3}]$	 $\vec{a_c} = [\frac{-1}{3}\ \frac{-1}{3}\ \frac{1}{6}\ \frac{1}{6}\ \frac{2}{3}]$
T3	$\frac{1}{2}$ $\frac{-1}{2}$	 $\vec{a_c} = [\frac{-1}{4}\ \frac{1}{4}\ \frac{-1}{8}\ \frac{-1}{8}\ \frac{1}{2}]$	 $\vec{a_c} = [\frac{-1}{4}\ \frac{-1}{4}\ \frac{1}{8}\ \frac{1}{8}\ \frac{1}{2}]$
T4	$\frac{2}{3}$ $\frac{-1}{3}$	 $\vec{a_c} = [\frac{-1}{3}\ \frac{1}{3}\ \frac{-1}{6}\ \frac{-1}{6}\ \frac{2}{3}]$	 $\vec{a_c} = [\frac{-1}{3}\ \frac{-1}{3}\ \frac{1}{6}\ \frac{1}{6}\ \frac{1}{3}]$
T5	$\frac{4}{5}$ $\frac{-1}{5}$	 $\vec{a_c} = [\frac{-2}{5}\ \frac{2}{5}\ \frac{-1}{5}\ \frac{-1}{5}\ \frac{3}{5}]$	 $\vec{a_c} = [\frac{-2}{5}\ \frac{-2}{5}\ \frac{1}{5}\ \frac{1}{5}\ \frac{2}{5}]$

IV. Transistor Level Design

A. Capacitors and switches

The choice to implement a switch as either an n-type or p-type MOS transistor depends on the available gate-source voltage. Thanks to the use of only a single supply rail, both nMOS and pMOS switches can be driven by a $0-3.3\,\mathrm{V}$ signal, and no bootstrapping circuits are required.

Figure 7 shows the implementation of the switches and capacitors. S1 to S3 connect a capacitor to the 3.3 V-rail, and are implemented by pMOS-transistors. Switches S4 to S6 are nMOS transistors since they connect a node to ground. Finally, switches S7 to S17 interconnect plates of the capacitors. Some switches, like S8 and S9 can be implemented as a single transistor because the gate-source voltage in every topology sufficiently large to use a pMOS transistor. For others, like S7 and S10, the V_{GS} is always sufficiently large such that it is possible to use the same type of transistor in every topology. These are therefore implemented as a pass-gate.

Since the voltages in the gearbox stay within the $0-3.3\,\mathrm{V}$ range, every capacitor is implemented as a MIM-capacitor, offered by the technology [17].

The area of the chip is optimally divided between the switches and capacitors by a MATLAB® script, based around the built-in nonlinear constrained optimization function *fmincon* [18]. The script computes the FSL and SSL losses of the gearbox by means of the charge flow vectors $\vec{a_c}$ and $\vec{a_r}$. Furthermore, the energy required to charge or discharge the gate of the transistors, as well as the parasitic bottom-plate capacitance of the MIM capacitors are extracted by simulation in Cadence Virtuoso® and inserted into MATLAB. This data allows the script to estimate the gate and bottom-plate capacitance losses. In order to limit dynamic power consumption, the switching frequency ($\phi_1 \rightarrow \phi_2 \rightarrow \phi_1$) of the gearbox is limited to 2 MHz.

The optimization results in an area $A_{C1} = 1.598\,\mathrm{mm}^2$, $A_{C2} = 0.666\,\mathrm{mm}^2$ and $A_{C3} = 0.672\,\mathrm{mm}^2$. Finally, the convertor also implements a 1 nF output capacitor to limit the ripple, which is approximated by [19]:

$$V_{ripple} = \frac{I_{out}}{C_{out} * f_{sw}} \tag{4}$$

This requires an additional area of $0.67\,\mathrm{mm}^2$, bringing the area to a total of $3.67\,\mathrm{mm}^2$. At large output currents however, this capacitance will be negligible with respect to the cell capacitance (see formula 1).

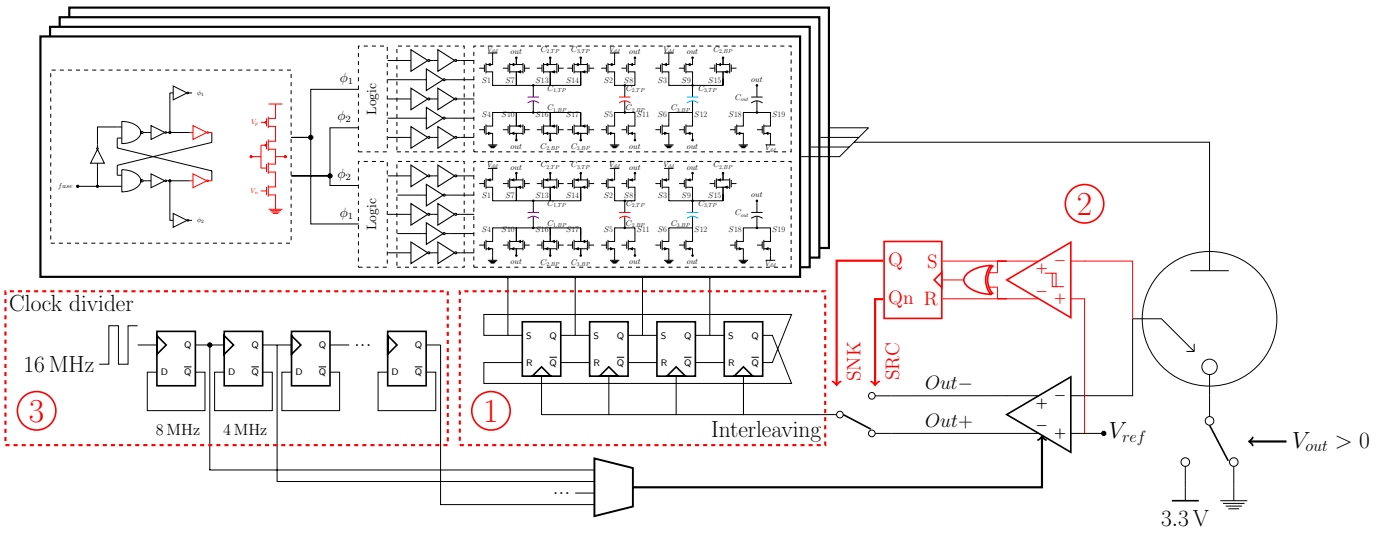


Fig. 6: Full overview of the potentiostat

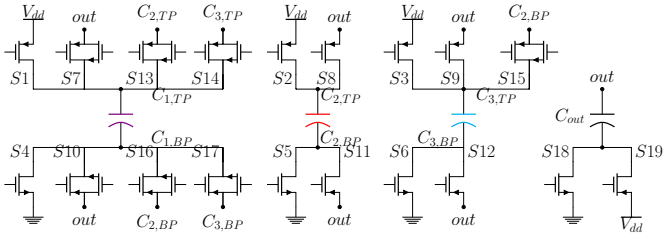


Fig. 7: Implementation of the switches

B. Control loop

Figure 6 shows a complete overview of the potentiostat. A hysteretic controller ensures that the voltage at the reference electrode V_{RE} accurately follows the reference voltage V_{ref}. Following sections cover the seperate building blocks of the control loop.

1) Logic and driving stage: Thanks to the use of a single supply rail, every switch can be driven with a $0-3.3\,\mathrm{V}$ signal. A chain of unit invertors buffer the logic output signal before applying it to the transistors. Since all of the logic is non-inverting, these buffers also provide an additional inversion for pMOS-switches.

2) Clock generator: A clock generator with a maximum dead time of 1.3% at a switching frequency of $f_{sw} = 2\,\mathrm{MHz}$ generates the phase signals ϕ_1 and ϕ_2.

3) Latched comparator: A popular choice for the clocked comparator is the so-called StrongARM latch [20]. This comparator features a very fast decision time thanks to its positive feedback loop. Moreover, it does not suffer from any static power consumption.

The independence of the voltage between the reference electrode and the working electrode from the voltage between the auxiliary and working electrode, requires a very broad input range of $-2.5\,\mathrm{V}$ to $5.8\,\mathrm{V}$. On the other hand, the comparator should generate rail-to-rail voltages between $0\,\mathrm{V}$ and $3.3\,\mathrm{V}$ at its outputs. This is not achieveable for the StrongARM latch, as the speed is strongly dependent on the common mode input voltage [21].

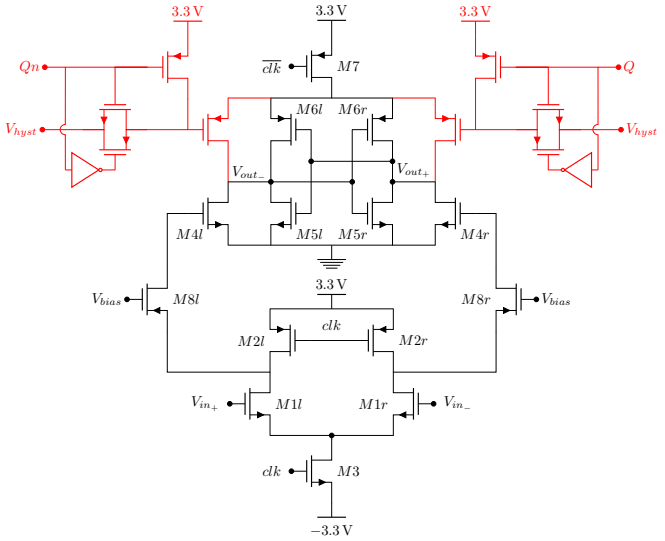


Fig. 8: Double tail comparator with hysteresis of section IV-C2 in red

Therefore, the convertor features a double tail comparator [22] with a seperate input and output stage. By providing the input stage with a symmetric supply rail at $-3.3\,\mathrm{V}$, the input range of the comparator reaches well below $0\,\mathrm{V}$. The output stage generates single-ended outputs. Two pMOS transistors $M8$ isolate the input from the output stage and avoid it from discharging the gates of transistors $M4$ below $V_{g,\ M4} \approx V_{bias} - V_{th,\ M8}$.

4) Topology selection: Finally, an algorithm implemented in Verilog-A allows the gearbox to change between different topologies depending on the output voltage and current.

C. Improvements

Previous sections already discuss a fully operational DC-DC convertor. The convertor however implements three more ad-

vanced methods to further increase the performance, indicated in red in figure 6.

1) Interleaving: A first improvement is the interleaving of the convertor. By splitting the convertor into N smaller fragments, and shifting each of these copies in time over $\frac{360°}{N}$, the output ripple of the convertor improves by a factor N [19]. In order to limit the dynamic power consumption of the comparator, the number of fragments in this design is limited to $N = 4$. Moreover, to make the output ripple constant over time, each fragment is splitted up into 2 smaller fragments in anti-phase.

2) Hysteretic double-tail comparator: For the potentiostat to accurately reproduce quick variations in the reference voltage V_{ref}, it has to be able to quickly change between charging and discharging the three-electrode cell by switching between the two outputs of the comparator.

A second, hysteretic comparator as indicated in figure 6 decides which comparator output drives the clock generators. In [12], a hysteretic comparator is realised by adding a pair of transistors to a StrongARM latch. In this case, this hysteretic comparator is realised by adding bleeding transistors to the second stage of a double-tail comparator. This generates a variable offset to the second stage of the convertor, depending on whether the convertor is currently sourcing or sinking current. Thanks to the slow variations in the reference voltage V_{ref}, this hysteretic comparator can generally be clocked much slower than the first, such that its power consumption is limited.

3) Frequency scaling: The dynamic power consumption of the comparator is reduced by decreasing the clock frequency at low output currents. This design achieves frequency scaling by a chain of D flip-flops acting as clock dividers.

V. Results

Firstly, figure 9 shows the simulated waveforms in the double-tail comparator. Since $V_{in_+} > V_{in_-}$, the input stage decharges the gate of $M4$ at a different rate. $M4r$ is turned of first, and the positive feedback loop converges to $V_{out_-} = 3.3\,\mathrm{V}$. Transistors $M8$ prevent the gates from discharging beyond $V_{gate} \approx 0\,\mathrm{V}$.

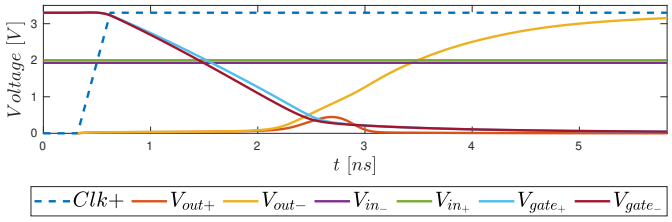


Fig. 9: Waveforms in the double-tail comparator

Figure 10 shows the the potentiostats efficiency in steady-state obtained by a series of transient simulations in Virtuoso. The efficiency is calculated with respect to the power supplied by the $3.3\,\mathrm{V}$ and $-3.3\,\mathrm{V}$ lines. The power consumption of clock signals, as well as that of the clock divider and hysteretic comparator, is not taken into account. The simulation shows a close correpondence to the results obtained from the optimization in MATLAB. The optimized result does not account

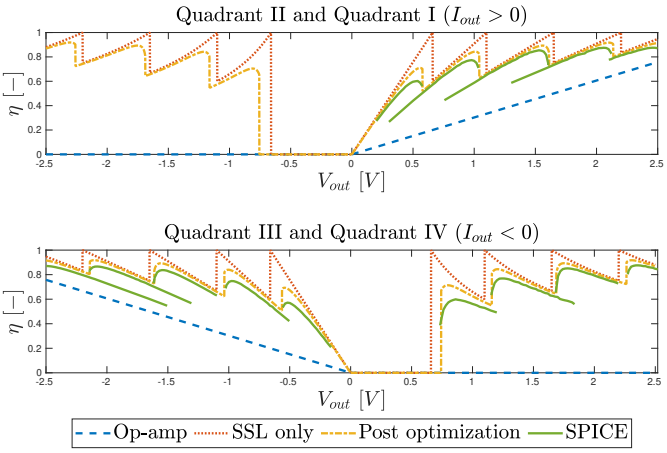


Fig. 10: Comparison of the efficiencies at $I_{out} = 1\,\mathrm{mA}$ (I, II) and $I_{out} = -1\,\mathrm{mA}$ (III, IV)

for the power consumption of the control loop, causing a discrepancy which becomes larger at low output powers. The graph also shows the theoretical maximum efficiency for this gearbox, if only SSL losses were present.

The efficiency in quadrant II and IV drops to zero near $V_{out} = 0$. This can be explained with the model from figure 4. The only suitable VCR_i in these regions is respectively the $1:1$ conversion and the $1:0$ conversion, and so all the power generated by the cell is dissipated in the convertor output resistance.

Furthermore, table III shows the difference in losses at a maximal and a minimal load. Frequency scaling clearly reduces the power consumption of the load, even though the power consumption of the comparator does not decrease as quickly as desired.

TABLE III: Allocation of losses for $V_{ref} = 2.5\,\mathrm{V}$

	$I_{cell} = 1\,\mathrm{mA}$	$I_{cell} = 1\,\mu\mathrm{A}$
P_{out}	$2492\,\mu\mathrm{W}$	$2565\,\mathrm{nW}$
$P_{loss,DC-DC}$	$196\,\mu\mathrm{W}$	$197\,\mathrm{nW}$
$P_{flip-flop}$	$45\,\mu\mathrm{W}$	$38\,\mathrm{nW}$
$P_{logic,buffer}$	$44\,\mu\mathrm{W}$	$60\,\mathrm{nW}$
$P_{comparator}$	$41\,\mu\mathrm{W}$	$1340\,\mathrm{nW}$
P_{NOCG}	$34\,\mu\mathrm{W}$	$26\,\mathrm{nW}$

The response of the potentiostat to changes in the reference voltage is evaluated using the model of figure 3, using the set of parameters shown in IV. Figure 11 shows the response of the convertor to a step response. The potentiostat accurately reproduces the applied waveform. The VCR selection block ensures that the convertor correctly switches between topologies at $t \approx 22.5\,\mu\mathrm{s}$, $t \approx 41\,\mu\mathrm{s}$ and $t \approx 44.5\,\mu\mathrm{s}$. The hysteretic comparator causes the potentiostat to switch from charging to discharging the output capacitance around $t \approx 40\,\mu\mathrm{s}$.

TABLE IV: Parameters for the linearized model of figure 3

C_{AE}	C_{WE}	R_{AE}	R_{WE}	f_{clk}
$1\,\mu\mathrm{F}$	$100\,\mathrm{nF}$	$100\,\Omega$	$500\,\Omega$	$16\,\mathrm{MHz}$

Figure 12 shows the potentiostats ability to accurately follow a sinusoidal reference with $f = 10\,\mathrm{kHz}$. The hysteretic

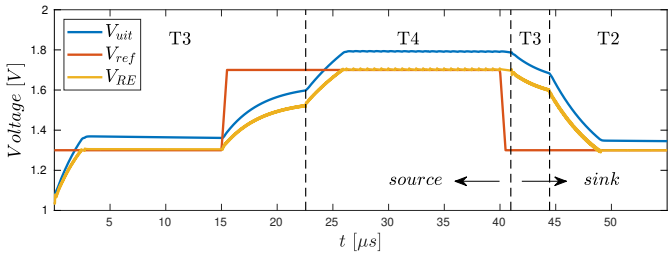


Fig. 11: Response of the convertor to a step in the reference voltage between 1.3 V and 1.7 V

TABLE V: Comparison to previous work

	[4]	[7]	This work
Type	Linear	DCM Buck	SC DC-DC
Process	2.5 μm	0.18 μm	0.35 μm
V_{out}	$0-5$ V	$0-1.8$ V	$-2.5-2.5$ V
I_{out}	$2-32\,\mu$A	12 μA	$\pm(1\,\mu\text{A}-1\,\text{mA})$
η	6%@2 μA	95%@12 μA	54%@12 μA
V_{ripple}	10 mV@2 kHz	2.5 mV@8 kHz	2 mV@27.5 kHz
Die size	$2.3\times2.8\,\text{mm}^2$	–	$3\,\text{mm}^2$

comparator is clocked at $f = 500\,\text{kHz}$ and causes the convertor to switch between sourcing and sinking current at $t \approx 40\,\mu\text{s}$ and $t \approx 80\,\mu\text{s}$.

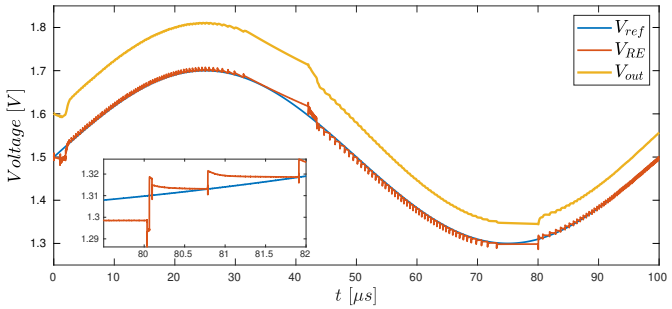


Fig. 12: Response of the convertor to a sinusoidal reference voltage with mean 1.5 V and amplitude of 200 mV

Table V shows a comparison of the presented potentiostat to previous publications. The comparison uses a similar setup to [4] with an output capacitance of 320 nF, an output resistance of 500 kΩ and a reference voltage $V_{ref} = 0.7\,\text{V}$.

Frequency scaling reduces the clock frequency of the comparator to 250 kHz. The convertor uses topology T2 to provide the 0.7 V output voltage, which causes a rather low efficiency of 55%, and a ripple at 27.5 kHz. The power consumption of the clock divider is not taken into account.

VI. Conclusion

In this paper, a potentiostat based on a four-quadrant switched-capacitor convertor was designed and simulated in a 0.35 μm technology. The system showed a high output voltage and current range in comparison to other efficient potentiostat designs. The potentiostat has a good overall efficiency and can be used for both amperometric and voltammetric experiments.

References

[1] A. J. Bard and L. R. Faulkner., *Fundamentals and Applications Fundamentals and Applications*, 2002.

[2] P. A. Boutet and S. Manen, "Low power CMOS potentiostat for three electrodes amperometric chemical sensor," *2011 Faible Tension Faible Consommation, FTFC 2011*, pp. 15–18, 2011.

[3] M. M. Ahmadi and G. A. Jullien, "A wireless-implantable microsystem for continuous blood glucose monitoring," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 169–180, 2009.

[4] S. Sutula, J. Pallares Cuxart, J. Gonzalo-Ruiz, F. X. Munoz-Pascual, L. Teres, and F. Serra-Graells, "A 25-μW All-MOS potentiostatic delta-sigma ADC for smart electrochemical sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 3, pp. 671–679, 2014.

[5] L. Zuo, S. K. Islam, I. Mahbub, and F. Quaiyum, "A low-power 1-V potentiostat for glucose sensors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 2, pp. 204–208, 2015.

[6] S. Ghanbari and M. Habibi, "Low power potentiostat using switching technique for three electrode amperometric sensors," *ICEE 2015 - Proceedings of the 23rd Iranian Conference on Electrical Engineering*, vol. 10, pp. 1154–1158, 2015.

[7] S. Ghanbari, M. Habibi, and S. Magierowski, "A High-Efficiency Discrete Current Mode Output Stage Potentiostat Instrumentation for Self-Powered Electrochemical Devices," *IEEE Transactions on Instrumentation and Measurement*, vol. 67, no. 9, pp. 2247–2255, 2018.

[8] J. C. Fidler, W. R. Penrose, and J. P. Bobis, "A potentiostat based on a voltage-controlled current source for use with atmospheric gas sensors," *IEEE Transactions on Instrumentation and Measurement*, vol. 41, no. 2, pp. 308–310, 1992.

[9] S. M. Martin, F. H. Gebara, T. D. Strong, and R. B. Brown, "A Fully Differential Potentiostat," *IEEE Sensors Journal*, vol. 9, no. 2, pp. 135–139, 2009.

[10] T. Dobbelaere, P. M. Vereecken, and C. Detavernier, "A USB-controlled potentiostat/galvanostat for thin-film battery characterization," *HardwareX*, vol. 2, pp. 34–49, 2017. [Online]. Available: https://doi.org/10.1016/j.ohx.2017.08.001

[11] A. Sarafianos and M. Steyaert, "A True Two-Quadrant Fully Integrated Switched Capacitor DC-DC Converter Supporting Vertically Stacked DVS-Loads With Up To 99 . 6 % Efficiency," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 210–211, 2017.

[12] A. Sarafianos, "Fully-Integrated Wide Input Range and Two-Quadrant Converters," Ph.D. dissertation, 2017.

[13] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *Proceedings of the IEEE Workshop on Computers in Power Electronics, COMPEL*, vol. 23, no. 2, pp. 216–224, 2006.

[14] T. Thielemans, N. Butzen, A. Sarafianos, M. Steyaert, and F. Tavernier, "A capacitive DC-DC converter for stacked loads with wide range DVS achieving 98.2% peak efficiency in 40nm CMOS," *2018 IEEE Custom Integrated Circuits Conference, CICC 2018*, vol. 2, no. 1, pp. 1–4, 2018.

[15] M. S. Makowski and D. Maksimović, "Performance limits of Switched Capacitor DC-DC Convertors," pp. 1215–1221, 1995.

[16] M. D. Seeman, "A Design Methodology for Switched-Capacitor DC-DC Converters," 2009.

[17] ON Semiconductor, "I3T50: 0.35 m Process Technology," pp. 1–4, 2016. [Online]. Available: https://www.onsemi.com/pub/Collateral/I3T50-D.PDF

[18] Mathworks Benelux, "fmincon." [Online]. Available: https://nl.mathworks.com/help/optim/ug/fmincon.html

[19] T. Van Breussegem and M. Steyaert, *CMOS integrated capacitive DC-DC converters*, 2013.

[20] B. Razavi, "The StrongARM latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015.

[21] Y. Lin, A. H. M. V. Roermund, K. Doris, and H. Hegt, *Power-Efficient High-Speed Parallel-Sampling ADCs for Broadband Multi-carrier Systems*. Springer International Publishing Switzerland, 2015.

[22] D. Schinkel, E. Mensink, E. Klumperink, and E. V. Tuijl, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *ISSCC International Solid-State Circuits Conference*, pp. 314–315, 2007.