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Design of a CMOS RF Front End Receiver in 0.18µm Technology

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Design of a CMOS RF front end receiver in 0.18μm technology

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by

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Vishwas Kudur Sastry ENTITLED Design of A CMOS RF front end Receiver in 0.18μm technology BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE DEGREE OF Master of Science in Engineering

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ABSTRACT

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An RF front end receiver system refers to the analog down conversion stages of the wireless communication system. The Digital base-band signals cannot be transmitted directly through wireless channels due to the properties of electromagnetic waves. The baseband signals need to be converted to analog through a digital-to-analog converter (DAC), up converted to higher frequency using an up conversion mixer and then transmitted through the channel. The received signals are down converted to base band frequency and then converted to digital again using the analog to digital converter (ADC). The processes which the analog signal undergoes at the RF front end include amplification, mixing and filtering.

The RF Front End receiver developed in this thesis makes use of a differential low noise amplifier (LNA) with center frequency at 1.75GHz.The incoming RF signal undergoes amplification by the LNA and is down converted by a Gilbert double balanced mixer to a first Intermediate frequency (IF) of 250 MHz A second Gilbert Double Balanced Mixer down converts to a low second IF of 50 MHz The local oscillator signal for the mixer is generated using a voltage controlled ring oscillator (VCO).The entire front end of the receiver was created in Cadence virtuoso schematic editor using CMOS 0.18μm technology. The total power consumed by the RF Front End Receiver is 113.36 mW.

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DEDICATED TO AMMA, APPA and DIDI

1 INTRODUCTION

1.1 Overview

Wireless Communication Systems market has seen resurgence especially in the last decade. The demand for High Frequency Transceivers has been explosive and unanticipated. Wireless products demands low-cost, low-power high speed and high volume. With the improvement of integrated circuit (IC) technology, the size of electronic components like transistors has consistently shrunk. Following the scale down in channel length, there has been an improvement in unity gain cut off frequency (f_t) and maximum operating frequency (f_{max}) which shows the potential of CMOS at the front end of a RF system. The decreasing supply voltages are making the design of Analog and RF circuits more challenging. The RF circuits are usually dominated by passive components (like resistors, capacitors and inductors), the size of which does not scale proportionately. As a result, the chip area does not shrink to the same extent. Hence there is a need to build a complete transceiver on a single CMOS chip to minimize the silicon area as well as the cost. Efforts are being made to bring the digital processing functions as close to the front end as possible but still most of the RF Front-end components like the Low Noise Amplifier and the Mixer are still designed in the Analog Domain.

Rapid Advancements have been made at the component level as the channel length continues to shrink, line width reduces, and the transistors occupy less silicon area and switch faster. However not so much has happened at the system level For example, the super heterodyne receiver [14] architecture which was invented decades ago is still the most popular architecture in modern RF Receivers.

1.2 Receiver Concepts.

1.2.1 Basics.

The main purpose of the receiver is to accept the signals through the antenna from the transmitter and perform various tasks such as amplification, mixing, demodulation and then pass it on for digital signal processing. Before seeing what are the different types of receiver architectures and its various components, let's cover some concepts related to any receiver: selectivity and sensitivity. These two parameters affect the performance of the receiver to a large extent. In addition to these noise performance of individual blocks, linearity, gain and image rejection are crucial in the receiver design.

1.2.2 Sensitivity.

Sensitivity of a receiver is defined as the minimum amount of the signal which can be detected at the input such that there is adequate signal to noise ratio at the receiver output at a given instance. It determines how far the receiver can be placed from the transmitter. Sensitivity is specified in terms of dBm(decibels relative to 1 mili watt).Overall sensitivity is related to the noise figure of the receiver which is due to noise from the individual blocks as well as the gain from the individual blocks. Noise Figure is defined as the ratio between the SNR at the input and the SNR at the output of the circuit.

$$F \equiv \frac{Input\ SNR}{Output\ SNR} \quad (1.1)$$

$$\mathbf{NF \equiv 10log\ (F)\ in\ dB} \quad (1.2)$$

Where F is the noise factor and NF is the noise figure of the system.

Noise Figure is usually calculated with respect to a specific source impedance and noise temperature. In wireless communication systems, the standard values for a source impedance, Rs = 50Ω and at temperature, T=293 K. For an individual block like an amplifier or mixer, the total noise figure can be derived in terms of the Gain and output noise added by the system. G is the power gain of the amplifier with input signal power P_{input} and input noise power N_{input}. The output signal power is GP_{input} and output noise power is given by $GN_{input} + N_{added}$ where N_{added} is the noise added externally. The noise figure of the amplifier can be calculated as follows:-

$$\boldsymbol{F = \left(\frac{P_{input}}{N_{input}}\right) / \left(\frac{GP_{input}}{GN_{input} + N_{added}}\right)} \quad (1.3)$$

$$\mathbf{F = 1+ (N_{added}/GN_{input}) = 1+(N_{added,input}/N_{input})} \quad (1.4)$$

Where $N_{added,\ input}$ is the input referred added noise from the amplifier.

1.2.3 Noise Figure.

The noise figure of the overall receiver can be derived by the calculating the noise figure of the individual cascaded blocks in the receiver chain. The noise figure of the entire cascaded chain depends on the noise figure of the individual blocks as well as the gain distribution. For a receiver chain consisting of 2 blocks cascaded with proper matching, the total output noise is given by

$$\mathbf{P_{noise,output} = F_1 P_{noise,input} G_1 G_2 + (F_2 - 1) P_{noise,input} G_2} \qquad (1.5)$$

Where G_1 and G_2 are the power gains of the individual blocks with corresponding noise figures F_1 and F_2.

The output SNR of the cascaded blocks is given by

$$\mathbf{SNR_{output}} = \frac{S_{out}}{P_{noise,output}} = \frac{S_{input} G_1 G_2}{F_1 P_{noise,input} G_1 G_2 + (F_2 - 1) P_{noise,input} G_2} \qquad (1.6)$$

Total cascaded noise figure can be calculated as

$$\mathbf{F} = \frac{SNR_{output}}{SNR_{input}} = \mathbf{F_1} + \frac{(F_2 - 1)}{G_1} \qquad (1.7)$$

From the above equation it can be seen that the total noise figure of the cascaded blocks depends on the noise figures of the individual blocks as well as the gain of the first block. If the gain G_1 is large then the noise from the succeeding blocks will have less effect on the overall noise figure. Hence the first block of the receiver (usually LNA) must have low noise figure and enough gain.

1.2.4 Selectivity

The performance of the receiver in terms of sensitivity to the required signal was discussed but the presence of interfering or unwanted signals was ignored. Selectivity is the measure of performance of the receiver to separate the wanted or required signals from those which are not required. Selectivity is very important when the receiver needs to choose between a weak desired signal and a strong neighboring interfering/undesired signal. There is no quantitative way how the selectivity of a receiver can be measured but usually specified as blocking masks used in filtering, nonlinearity and phase requirements in the circuit. The two tone test is one of the other ways to test the selectivity of the receiver.

1.3 Receiver Architectures.

The main purpose of the RF receiver is to perform certain tasks on the received signal like amplification, filtering, demodulation and analog to digital conversion with adequate signal to noise ratio (SNR) before it undergoes digital signal processing. The received signal can be strong or extremely weak; also a strong blocking signal might be present with certain offset from the wanted frequency which needs to be rejected. These factors affect the dynamic range, sensitivity blocking and inter modulation performance. The receiver architecture affects the requirements and the performance. Another critical criterion in the receiver architecture is the number of components (both external and integrated) which directly determine the cost. In addition external filters might be present which require a low impedance level to drive them. So the final aim would be to reduce the number of such filters and design a receiver with low power consumption.

The most common receiver architectures are super heterodyne, direct conversion, low IF, and wideband IF. The front end of the receiver topology used in this thesis is that of the low IF Architecture.

1.3.1 Direct Conversion Architecture

The direct conversion receiver topology is also called the zero-IF or the homodyne Architecture [1]. First published in 1924 by F. M. Colebrook [2] and practical Implementations were introduced in 1947[3].The block diagram of a typical direct-conversion receiver is as shown in the figure. The RF signal after the antenna is pre filtered so as to attenuate the signals outside the reception band. Then the signal is amplified through a low noise amplifier (LNA) and then it is down converted to zero intermediate frequency (IF).In some systems like CDMA, an external inter stage filter is used after the LNA attenuate the transmitter signal leakage and to relax the linearity requirements of the succeeding mixer[4][5]. For Frequency and Phase modulated signals, down conversion should be performed in quadrature to prevent signal sidebands from aliasing with one another [6]. Because the Local Oscillator frequency is centered in the desired channel, useful signal and noise occupy both the upper and lower sidebands. The low-pass filter with a bandwidth of a half of the symbol rate removes adjacent channels at baseband. Since filtering is performed at low frequencies the filters can be realized on chip. From the point of power consumption the direct conversion receiver architecture is very good. Here the RF signal is converted directly to zero intermediate frequency (IF), the image consists of the channel itself. Therefore this architecture eliminates the image reject problem existing in other receiver architectures. The Direct Conversion Receiver has a few drawbacks like high sensitivity to flicker noise and dc offsets [6][7].

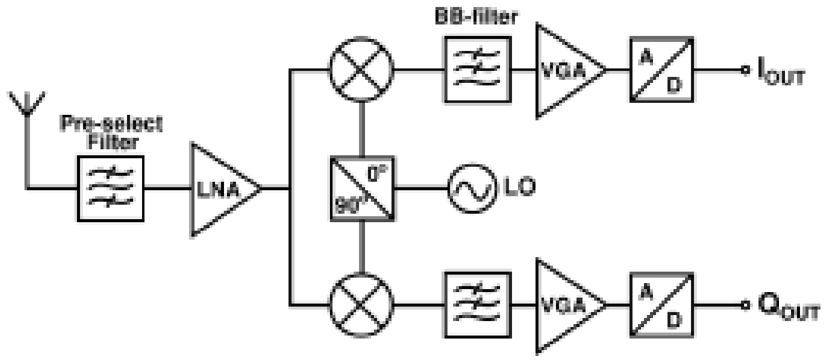


Fig1.1: Direct Conversion Receiver Architecture

1.3.2 Low IF Architecture.

The Basic Block diagram of low-IF receiver is similar to that the direct conversion receiver. The low IF receiver down converts the input signal directly to low IF frequency which is above dc but lower than half of the reception bandwidth. Single stage down conversion is performed in quadrature and the low IF receiver does not need an external intermediate filter. In comparison to the direct conversion receiver, the low IF receiver is not affected by dc offset problems and the flicker noise is less problematic. The low IF receiver architecture requires good matching for image rejection [8]. The choice of IF frequency is another critical decision. A very low IF complicates the requirements of the frequency synthesizer [9]. Higher IF frequency increases the complexity and current consumption of the IF stages.

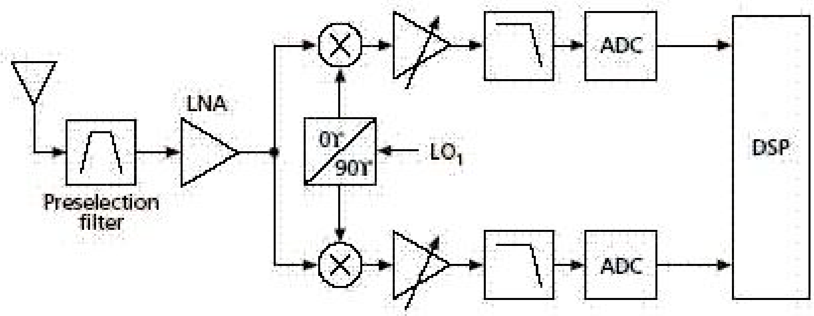


Fig 1.2: Low IF Receiver Architecture

1.3.3 Wideband IF Architecture.

In the Wideband Receiver Architecture as shown in the figure, the signal is down converted in two phases to zero frequency[10][11][12]. The whole reception band is down converted with quadrature mixers such that a large bandwidth at IF is maintained. Any up converted frequency components are removed using a simple low pass filter and then the signals are passed through to a second set of mixers [10]. Second Stage of down conversion to zero IF, the wanted channel is selected by adjusting the frequency of the second local oscillator. The channel filtering is done at baseband and discrete filters are avoided. The image rejection is achieved during the second down converting step. Compared to direct conversion receiver, wideband IF receiver has several advantages. Firstly, there are no local oscillators which operate at the same frequency as the receiver RF signal which minimizes the problems related to time varying dc offsets. Channel selection performed by tuning only the frequency of the second LO and reduction in phase noise of the first LO can be achieved [10]. Flicker noise of the first mixer is not very critical however the first stage down conversion should be performed accurately so as to not affect the image-reject capability and the sensitivity of the receiver [13]. Multistage realization leads to increased power consumption.

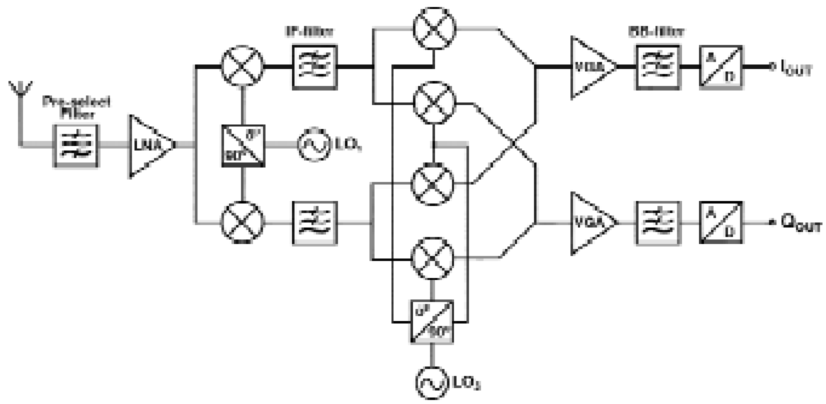


Fig 1.3: Wideband IF Receiver Architecture.

1.3.4 Super Heterodyne Receiver

One of the most popular forms of receiver in use today is the super heterodyne receiver or superhet radio. Used in a variety of applications ranging from broadcast receivers to mobile radio communication systems. It was first developed at the end of First World War by an American named Edwin Armstrong [14]. The main theory behind the superhet is the received signal enters one of the inputs of the mixer, a locally generated signal from the oscillator to the other input. As a result of the mixing of the two signals, new signals are generated. The resulting signal is applied to the intermediate frequency amplifier (of fixed frequency) and filter combination. The signals that are down converted and fall within the pass band of the IF amplifier will be amplified and passed on to the next stage and those outside the pass band are rejected. Tuning is accomplished by varying the frequency of the local oscillator. What makes this process advantageous is that very selective fixed frequency filters can be used which outperform the variable frequency counterparts. The intermediate frequency is normally a lower frequency than the incoming signal and thus enables a better performance and less expensive.

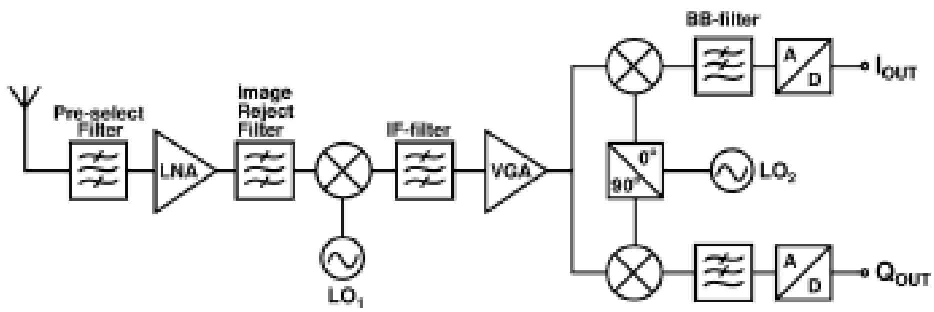


Fig 1.4: Super Heterodyne Receiver Architecture.

The block diagram of a basic superhet is as shown in the figure. The RF Signal enters the front end circuitry from the antenna. The front end unit contains tuning for the superhet to remove the image signal and often includes an RF amplifier to amplify the signals before they enter the mixer. The level of amplification is chosen such that it does not overload the mixer when strong signals are present, but enables the signals to be amplified efficiently to ensure a good signal to noise ratio is achieved. The Tuned and Amplified signal is applied to one port of the mixer while the local oscillator signal is applied to the other port of the mixer. The local oscillator signal may be generated from variable frequency oscillator which can be tuned by varying capacitor, a voltage controlled oscillator which can be tuned by varying the control voltage or by usage of a frequency synthesizer which enables greater stability and accuracy. The signals out of the mixer enter the IF stages. The IF stages contain most of the amplification in the receiver and as well as the filtering which separate the signals of one frequency from that of the other. Filters may consist simply of LC tuned circuits to provide inter stage coupling or might be there for a different requirement. The Signals from the IF stage needs to be demodulated; depending upon the type of transmission different types of demodulators are required. A Receiver may have a particular type of demodulator or variety of demodulators for the corresponding transmitted signals. The output of the demodulator is the recovered audio [28].

1.3.5 RF Front End Systems

The RF front end system refers to the analog front end of the wireless communication system. Digital base-band signals cannot be transmitted directly through wireless channels due to the properties of electromagnetic waves. As a result of which these signals need to be converted to analog through a digital-to-analog converter, up converted to higher frequency using an up conversion mixer and then transmitted through the channel. The received signals are down converted to base band frequency and then converted to digital again using the analog to digital converter. The processes which the analog signal undergoes at the RF front end include amplification, mixing and filtering [30]. From an RF Front end point of view, the type of receiver architecture is not of much difference. The LNA is a requirement in all receiver topologies and mixers are present in all receiver architectures. Hence the low noise amplifier and the mixer design discussed in this thesis are applicable for most of the receiver designs. The mixer is the immediate subsystem after the LNA unless the load of the LNA is an external filter in which the performance of the LNA needs to be measured individually and the output of the LNA needs to be matched to certain impedance.

1.4 Thesis Organization

Chapter 2 discusses about the design aspects of the Low Noise Amplifier, different topologies and the low noise amplifier used in this work which is the Cherry Hooper amplifier. Chapter 3 gives an overview of the mixer design considerations, its topologies and the mixer used in this thesis namely the Gilbert mixer along with the LC filter used. Chapter 4 throws some light on the voltage controlled ring oscillator used in this work. Chapter 5 includes the simulation and results of this thesis work and Chapter 6 summarizes the entire work ending with a short note on the future work which can be done.

2.1 Design Aspects.

2.1.1 Noise Figure

The low noise amplifier is the first stage in the front end of the receiver. The low noise amplifier is the first amplifying stage of the receiver and it sets the minimum noise figure of the receiver in accordance to the Friis' equation. Friis' formula is used to calculate the total noise figure of a cascade of stages [15], where each stage has its own noise factor and gain.

$$\boldsymbol{F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}} \quad (2.1)$$

Where F_n and G_n are the noise factor and available power gain respectively of the n-th stage.

In a cascaded system which is a receiver where the low noise amplifier (LNA) is the first block. The overall noise figure is given by

$$\boldsymbol{F_{receiver} = F_{lna} + \frac{F_{rest} - 1}{G_{lna}}} \quad (2.2)$$

Where F_{rest} is the overall noise factor of the subsequent stages. The overall noise figure, $F_{receiver}$, is dominated by the noise figure of the low noise amplifier F_{lna} provided the gain is sufficiently high.

2.1.2 Linearity

Linearity is defined is the region of operation where the output signal varies proportionally to the input signal. Linearity can be measured in several ways in terms on 1dB compression point as well as 3rd order intercept point (IP3).

2.1.2.1 1 dB compression point.

1 dB compression point is defined as input or output signal level where the gain is decreased by 1 dB from its ideal value. It is also used to estimate the largest input the circuit can handle.

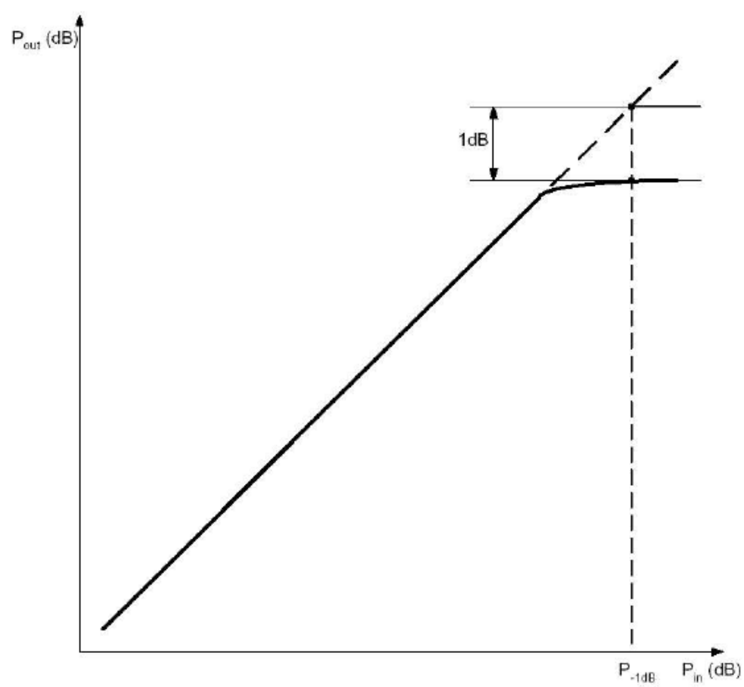


Fig 2.1 Graph showing the 1dB compression point.

2.1.2.2 Third order intercept point (IP3)

Third order intercept point is the point where the fundamental and the third order response intercept each other. Two signals, one which is the desired signal and the other which is the undesired interfering signal are applied to the circuit and the collaborated effect of these is known as intermodulation.

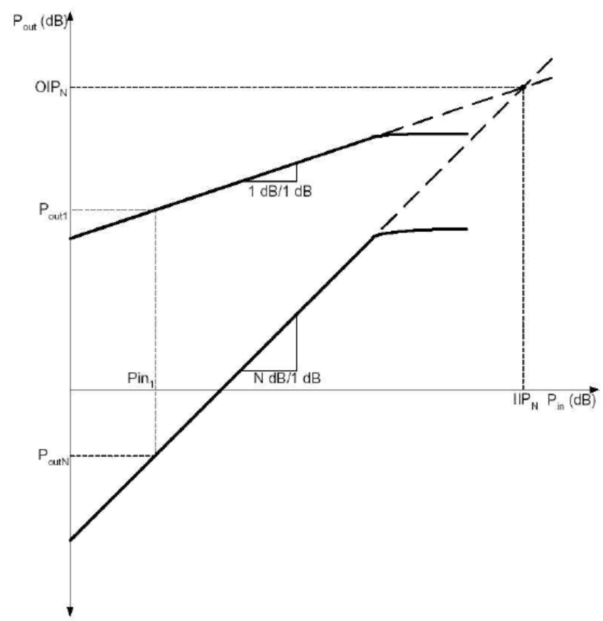


Fig 2.2 Graphical representation of the Third-Order Intermodulation Intercept Point (IIP3).

The LNA should provide enough gain to overcome the noise as well as not overload the following stages which might degrade the sensitivity of the receiver. The bandwidth of the LNA should be large enough to cover the desired signal band but should be narrow enough such that it should pre filter some on the unwanted signals. The linearity of the receiver front end depends of the subsequent stages after the LNA but however the LNA should have some linearity in order to prevent inter modulation tones in the reception band. In case a filter is preceding the LNA, Impedance matching is required otherwise the properties of the filter will degrade the input to the LNA.

2.2 Topology

Another important design criterion for LNA is the type of input which can be either single ended or differential structure. The single ended topology occupies less area on chip, providing better gain and noise figure for the same current as its differential counterpart. Single ended structure also eliminates the need for a balun (a passive electronic device which converts between balanced and unbalanced electrical signals) between the antenna and the LNA. However differential topology gives better rejection to substrate, supply noise and unwanted signals. The single ended LNA which uses inductors consume substantial amount of chip area in comparison to the differential design which might contain one or no inductors. In the structure of LNA's there are only one or two stacked transistors and with the supply voltages going down the performance can still be achieved.

2.2.1 Single Ended Topology.

Single Ended LNA's are typically used in narrowband wireless applications. Inductively degenerated common source or common gate LNA topologies are the ones which are popularly used. Inductively degenerated common source (IDCS) amplifier has the best noise figure and provides both voltage as well as current gain thereby reducing the noise contribution to the succeeding stages. In Inductive source degeneration impedance matching is achieved without the use of a physical resistor which is advantageous as a resistor would add to the LNA's noise. The degeneration inductance has low impedance at low frequency, hence the topologies using inductive degeneration are more linear compared to those using resistive degeneration for the same biasing current. Some of the common source amplifiers utilize cascode connection. This type of topology reduces miller effect and improves LNA stability.

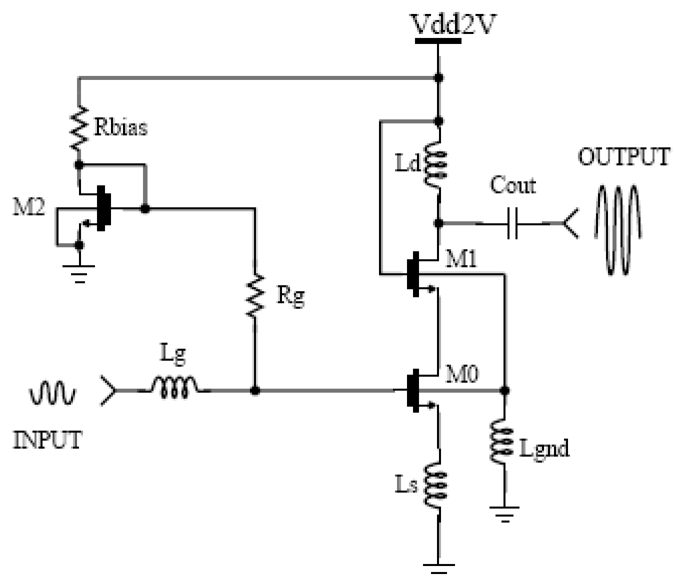


Fig 2.3: Schematic of a single ended LNA [22]

Common Gate LNA is also one of the popular topologies used in wireless communications. The common gate topology does not suffer from the miller effect. In CG stage the noise performance is independent of the operating frequency hence it is a suitable to use this configuration at higher frequencies.

2.2.2 Differential mode topology.

Most of today's high performance wide-band amplifiers employ the differential topology. Although the single ended LNA topology consumes less power as well as less chip area sometimes at twice the cost the differential architecture is preferred. Noise figure is a critical factor for the low noise amplifier; the differential design has better noise performance due to the ability to reject common mode noise. Linearity wise the differential LNA has a better performance because the circuit is symmetrical and natural ability to cancel out the even order distortions.

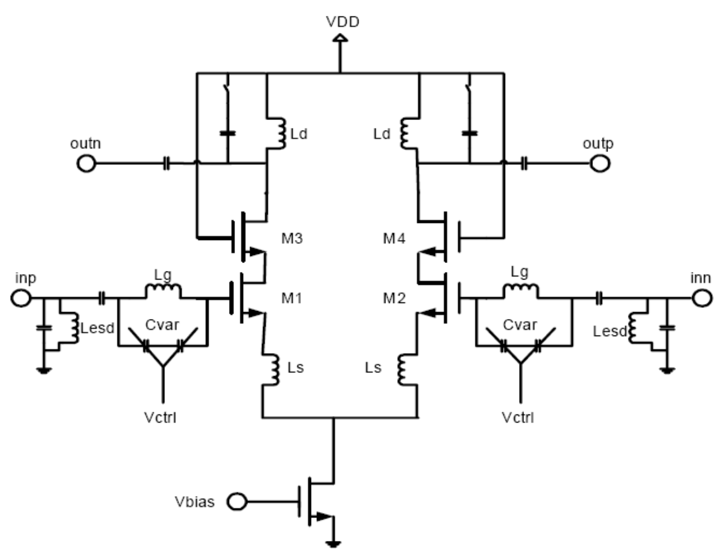


Fig 2.4 A fully differential tunable LNA [16]

Differential topology is not only beneficial for sensitive signals but even for noisy signals. The total current drawn from the power supply is more or less constant and alternates between the two symmetrical branches of the differential amplifier which maintains a constant load to the power supply thereby reducing the noise generated in the power supply. Due to doubling of the devices in differential topology, the input noise voltage is √2 times in comparison to that in the single ended structure.

2.3 Cherry Hooper Amplifier.

One of the main purposes for using the Cherry Hooper amplifier [18] is that it provides high gain bandwidth product without the need of extra supply voltage or chip area needed for inductively peaked gain stages which use active or passive inductors. The Cherry Hooper amplifier uses local feedback in the drain network to improve speed. A modification of the Cherry Hooper amplifier with source follower feedback and an additional feedback resistor to enhance the gain is used as the main amplifier. The modified Cherry Hooper is designed using NMOS FET's only as they are faster compared to the PMOS transistors and PMOS transistors provide unwanted capacitance at the output node of the amplifier. A CMOS implementation of Cherry Hooper amplifier is shown in the figure.

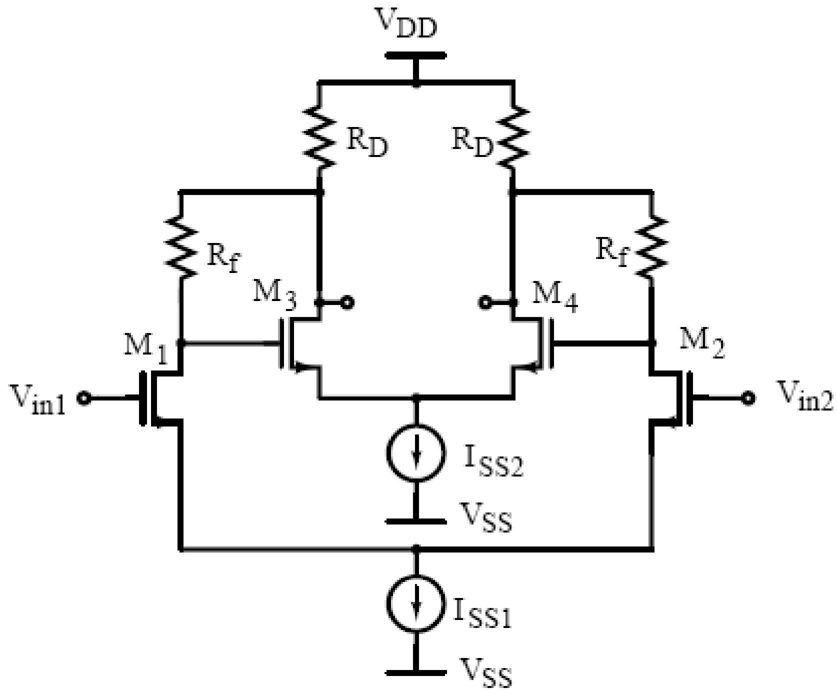


Fig 2.5: A CMOS Cherry Hooper Amplifier

The Transistors M_1 and M_2 form the input pair which is also known as the trans-conductance stage that converts input voltage into current. The Resistor R_f provides feedback between drain and gate of transistor M_3 and M_4 respectively. The current mode signal is then amplified and converted back to voltage by the second pair of transistors M_3 and M_4 which form the trans-impedance stage.

In order to improve the gain of the amplifier without a corresponding decrease in bandwidth the load resistor R_d in the conventional Cherry Hooper amplifier is split into two resistors R_1 and R_2.Transistors M_5 and M_6 provide source follower feedback through the Resistor R_f.

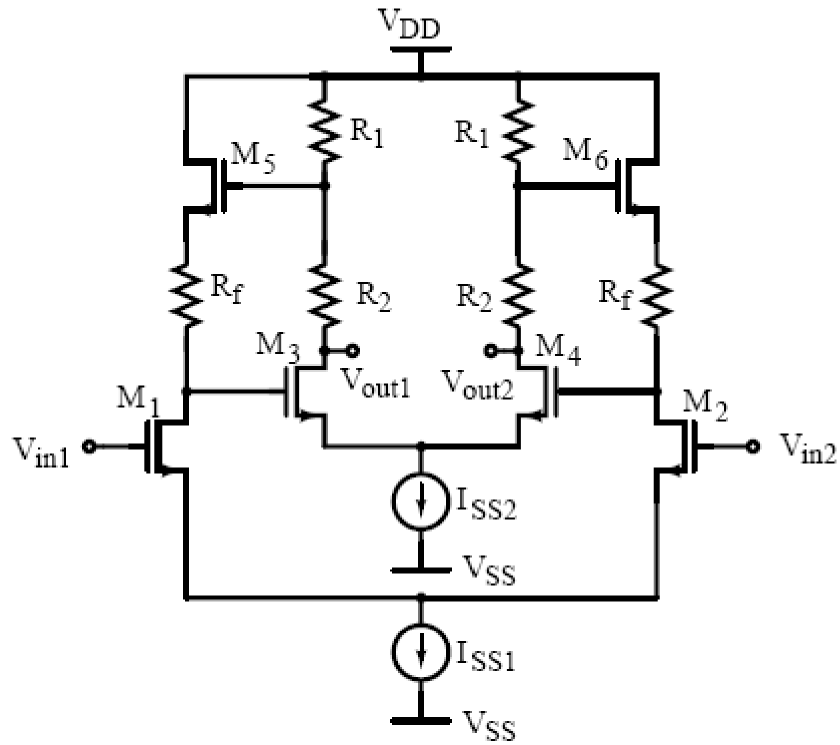


Fig 2.6: A Modified Cherry Hooper Amplifier with Source Follower[19].

The Cherry Hooper Amplifier topology allows high speed operation but faces difficulties at very low voltages.I_1 is equal to $(I_{ss1}+I_{ss2})/2$ and $I_{ss1}/2$ must flow through feedback resistor R_f. Therefore the minimum voltage required by the circuit is:-

$$\mathbf{V_{DD,\ min} = V_{I1} + \frac{\boldsymbol{I_{ss1}}}{2}.\ R_f + V_{GS\ 3,\ 4} + V_{Iss2}} \quad (2.3)$$

Here V_{I1} and V_{Iss2} represent the minimum voltages across I_1 and I_{ss2} respectively. These factors limit the voltage gain of the circuit. To improve the gain-headroom trade off, the modified Cherry Hooper topology is used. The differential mode half circuit [20] of the modified Cherry Hooper amplifier along with the most significant parasitic elements is shown in the figure.

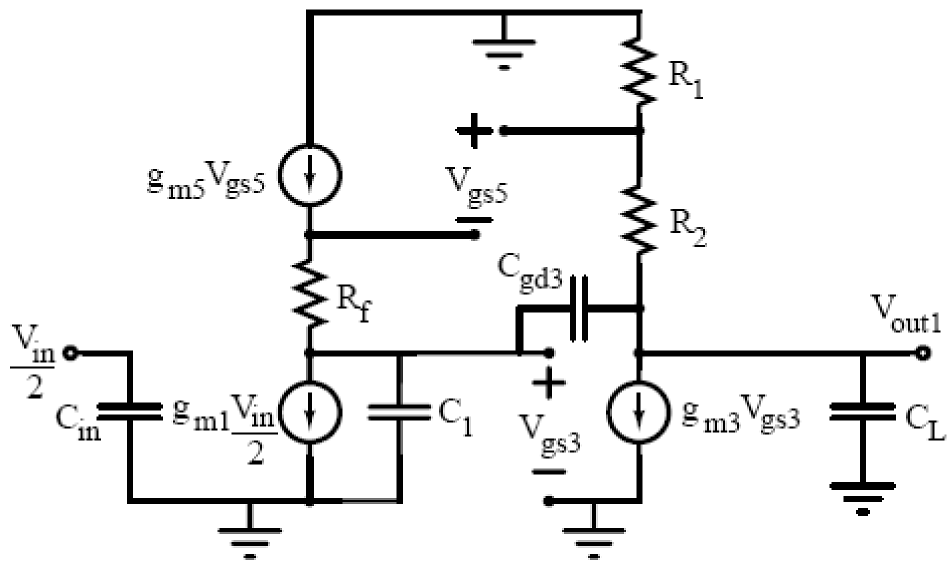


Fig2.7: Differential Mode Half Circuit Small Signal Model of modified Cherry Hooper Amplifier.

The low frequency small signal gain of the circuit is given by

$$\frac{V_{out}}{V_{in}} = \frac{\left\{g_{m1}(R_1+R_2)\left(\frac{1}{g_{m5}}+R_f\right)\right\}}{\left\{2\left(\frac{1}{g_{m3}}+R_1\right)\right\}} \quad (2.4)$$

The gain of the modified Cherry Hooper Amplifier is significantly greater than the circuit without R_2 or the source follower feedback.

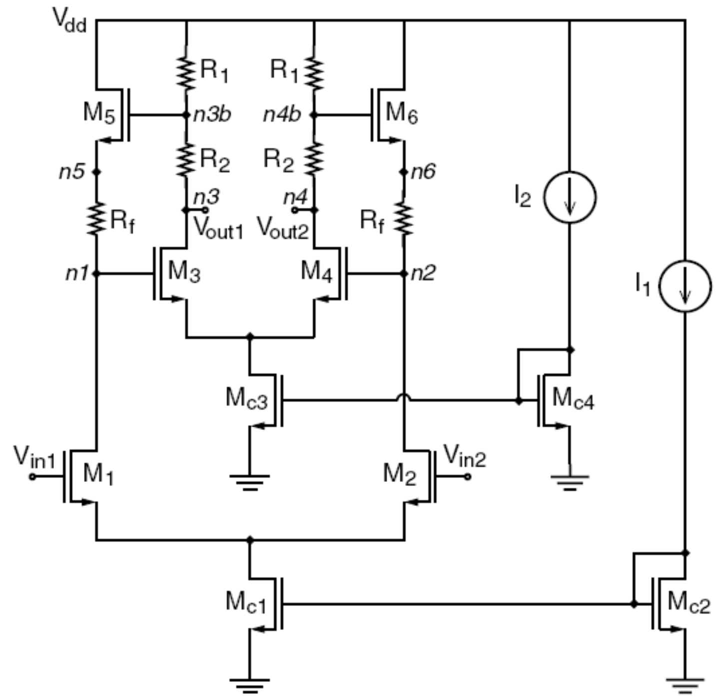


Fig2.8: Modified Cherry Hooper amplifier with biasing circuitary.

The topology has certain constraints. The major one being the amount of voltage headroom available in CMOS technologies which will become lesser as line width scales down and the power supply drops. The ratio of R_2/R_1 cannot be made extremely large as the DC voltages at nodes n_3 and n_4 must be high enough to drive the next stage in case of cascading several amplifiers. A critical path exists between the power supply and the ground hence it is important to keep all the transistors in saturation. The critical path includes the voltage drop over R_1, the gate-to-source voltage of transistor M_5 ($V_{gs,\ M5}$), the voltage drop over R_f, the gate-to-source voltage of transistor M_3 ($V_{gs,\ M3}$) and finally the drain-to-source voltage of biasing transistor M_{c3} ($V_{ds,\ Mc3}$).For 0.18um CMOS technology, V_{th} for nMOS transistor is around 0.5 V. For a overdrive voltage $V_{gs}-V_{th}$ of 0.2 V, $V_{gs,\ M3}$ and $V_{gs,\ M5}$ must be equal to 0.7 V. $V_{ds,\ Mc3}$ should be larger than the saturation voltage, which approximately equals the overdrive voltage V_{gs}-V_{th} of 0.2 V. As a result of which the voltage drop consumed by the transistors is almost 1.6 V. In a process using a power supply of 1.8 V, only 0.2 V of headroom is left for the resistors. Therefore, the current through these resistors is usually low and the resistance values should be chosen to be as small as possible within the constraint of high gain. The Ratio of R_2/R_1 has influence on the bandwidth as well as on the gain of the amplifier. A higher ratio ensures a large gain however it is less beneficial for bandwidth, hence the ratio should be one which is optimized for both gain and bandwidth.

3 MIXER

3.1 Theory

Mixers are used for frequency translation i.e. they are used to convert the RF signal (incoming signal after it is amplified by the LNA) to an intermediate frequency (IF) by multiplying it with a local oscillator (LO) signal. The block level representation is show in figure 3.1. The intermediate frequency can be the sum of frequencies of the two input signals or can be the difference between the two signal frequencies.

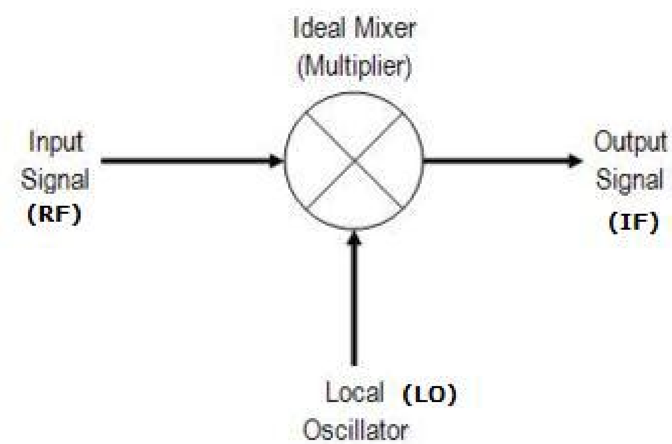


Fig 3.1 Block diagram of a mixer.

Suppose we consider the input signals are sinusoidal signals represented as [21]

$$\mathbf{V_1(t) = A_1 \sin 2\pi f_1 t}$$

$$\mathbf{V_2(t) = A_2 \sin 2\pi f_2 t}$$

We have

$$\mathbf{V_1(t)*V_2(t) = \frac{A_1A_2}{2}\,[\cos 2\pi\,(f_1\text{-}f_2)\,t - \cos 2\pi\,(f_1+f_2)\,t]} \quad (3.1)$$

Where (f_1+f_2), (f_1-f_2) are the sum and the difference of the frequencies respectively.

This is the simplest form of multiplication by the mixer. Different mixers employ different multiplication techniques which gives rise to various terms contain the sum of the two frequencies, the difference of the two frequencies, squares of the input frequencies and other weak signals which act as noise to the desired signal, All signals other than the desired signal need to be filtered out using various filtering techniques.

3.2 Design Considerations.

While designing a mixer, various parameters must be taken under consideration and there might be a tradeoff between one or two parameters in order to meet the design requirements. Impedance matching, conversion gain, noise figure, linearity, isolation and power consumption are few of the important ones.

3.2.1Impedance matching.

The super heterodyne receiver has an off chip image reject filter between the LNA and the mixer. The mixer input is connected to an off chip component should have an impedance of 50Ω in order to avoid reflections on the transmission line between the mixer and the image reject filter. The low IF and zero IF receivers have the output of the LNA connected directly to input of the mixer and there is no connection going off chip, hence matching is not required. On chip connections are much smaller than the wavelength of the input signal as a result of which reflections are not as big as a problem compared to when they go off chip.

Similarly the output impedance of the mixer needs to be matched in case of a connection going off chip. An output buffer can be added in case impedance matching has to be provided.

3.2.2 Conversion Gain

Conversion gain represents the efficiency with which the RF signal transposes to the IF frequency. By definition, it is the ratio of desired IF output to RF input. This ratio can be expressed in terms of voltage or power and is usually expressed in dB.

$$\boldsymbol{V_{gain} = 20\log\left(\frac{V_{out}}{V_{in}}\right)} \text{ Or } \boldsymbol{P_{gain} = 10\log\left(\frac{V_{out}}{V_{in}}\right)} \quad (3.2)$$

Conversion gain is a very important parameter because it affects the linearity and noise figure of the overall receiver. While calculating of the overall input noise figure of the receiver, the noise from the stages following the receiver will be attenuated by the gain of the mixer or amplified by its loss. The conversion gain also affects linearity as the signal level to the succeeding stages will change according to the gain or loss of the mixer.

3.2.3 Noise figure.

The measure of input noise corruption relative to the output noise corruption is called the noise factor. The noise factor when measured in decibels is known as noise figure (NF).Noise figure is given by

$$\boldsymbol{NF = 10\log\left(\frac{SNR_{input}}{SNR_{output}}\right)} \quad (3.3)$$

Where SNR_{input} and SNR_{output} are the signal-to-noise ratio at the input and output respectively.

3.2.4 Linearity

Linearity of a circuit can be measured in several ways. The 1 dB compression point and the Input third order intercept point (IIP3) help in defining the linearity of the mixer. The gain of the mixer increases linearly according to the input signal applied but beyond a certain point the gain of the mixer decreases and the point where the gain drops by 1 dB is called the 1 dB compression point. After the one dB compression point the linearity of the circuit is no longer valid. The third order intercept point indicates how well the mixer performs in the presence of nearby signals. This is mainly to understand the inter modulation distortion.

3.2.5 Isolation.

Port-to-Port isolation is very important in mixers. The LO-to-RF leakage is the most common problem in receivers. When the LO signal is very large, a significant amount may leak back to the RF input of the mixer causing a leakage back to the front end of the receiver. An LO-to-IF leakage degrades the performance of the stages following the mixer. RF-to-IF leakage also exists in certain receiver architectures which lead to distortions at the output.

3.2.6 Power.

For the mixer to function properly, the LO signal applied at the LO input must be sufficiently large. There is a tradeoff between the LO power and the conversion gain which can be determined at a reasonable LO voltage. The 1 dB gain compression input voltage also needs to be determined which requires a suitable amplitude of LO signal.

3.3 Mixer Topologies.

3.3.1 Single Balanced Mixers

A mixer with a single ended RF signal as input is called a single balanced mixer. The trans conductance transistor acts as a linear voltage-to-current converter i.e. V_{RF} to variation in drain current of the transistor. The differential pair act as switches and are driven by the LO signals which are in anti-phase. When the LO signal is a square wave, the LO amplitude must be chosen such that during operation only one transistor is saturated while the other is in cutoff region. An active or passive load converts the current to voltage at the output. Source Degeneration can be used to provide better linearity. Single balanced mixers are very susceptible to noise in the local oscillator (LO) signal and hence this configuration is rarely used. Its main drawback is the LO-IF feed through. The local oscillator signal could leak into the IF signal if the IF is not much lower than the LO frequency. The low pass filtering following the mixing stage may not suppress the LO signal completely without adding noise to the IF signal [1] (as the LO and IF frequencies are close to one another).

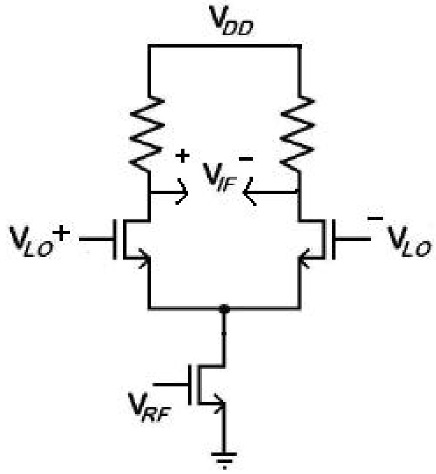


Fig 3.2 Single Balanced Mixer.

3.3.2 Double Balanced Mixers

Double balanced mixers are essentially two single-balanced circuits with the RF input transistors connected in parallel and the switching transistor pairs (or LO) connected in anti parallel. The double balanced structure provides high degree of LO-IF isolation and eases the job of filtering at the output [17]. This configuration is less susceptible to noise because of the differential RF signal. This topology results in zero LO terms at output while the converted signal is doubled at the output. This is also popularly known as the Gilbert cell mixer.

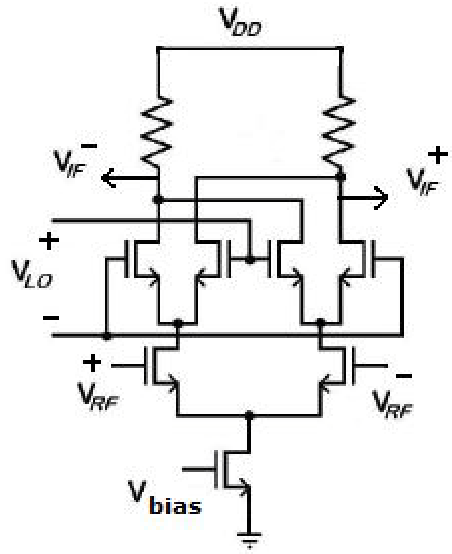


Fig 3.3 Double Balanced Mixer.

3.4 Gilbert Mixer.

The Gilbert cell is the most popular topology of double balanced mixers. It has two pairs of transistors connected in parallel which provides the double balanced structure which attenuates the RF-LO feed through produced by the mixer. When the two signals are given to the mixer, the output is the wanted frequency and the unwanted components which is the feed through. Since the inputs are 180 degrees out of phase some of the feed through gets cancelled as a result of this.

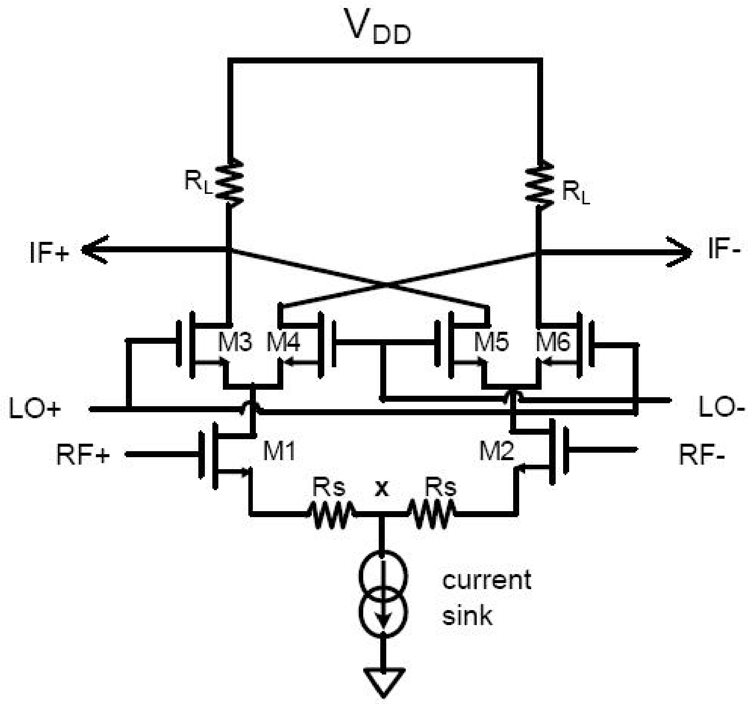


Fig 3.4 Schematic of Gilbert mixer.

The two transistors (M_1-M_2) at the RF input act as the amplifier increasing the gain before the RF signal undergoes mixing with the LO signal. This stage is also called the gain stage. The gain stage should have very high linearity in order to handle the power from the LNA. Degeneration resistors (R_s) can be added to increase or decrease the linearity. Source degeneration resistors can also be used to vary the gain. The RF transistors should be biased such that they have enough voltage headroom to swing without leaving the saturation region. The gain can be increased by either increasing the width of the transistor or by increasing the current through the transistors. The transistors which have the LO input going into them form the switching stage (M_3-M_4-M_5-M_6). Only one pair of transistors is on during a certain time, while the other pair is completely off. If both the pairs conduct at the same time, noise will be generated.

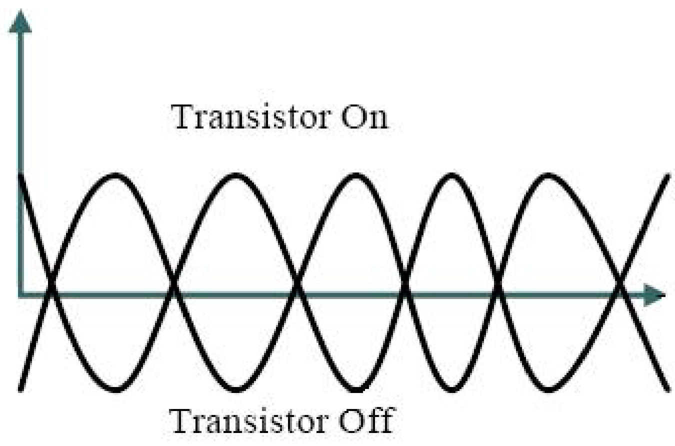


Fig 3.5 Illustration of proper LO transistor pair switching.

The output of the mixer is taken from the IF+ and IF- ports. No impedance matching is required for the mixer if the input comes from the LNA or image reject filter which is on chip otherwise impedance matching is necessary. The gain of the mixer with source degeneration resistor R_s and load resistor R_L is given by the expression:-

$$\frac{V_{out}(t)}{V_{rf}(t)} \approx \frac{2}{\pi}\left(\frac{R_L}{R_s+\frac{1}{g_m}}\right) \quad (3.4)$$

3.5 Mixer with Tuned Load.

When voltage headroom is a problem and there is need of large gain over a small frequency range, a tuned load can be used in the mixer. The RF input can be a broadband signal and the output IF is of fixed frequency. In the normal resistive load, there is a certain voltage drop across the resistor depending on the value of the resistance and the amount of current flowing through the resistor. When a tuned load in present, the inductor is acts as a short at DC and hence there is more voltage headroom to work with.

By choosing the proper values of L and C the tank circuit resonates at the required frequency ω_0 where

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (3.5)$$

and the gain of the tank circuit or mixer is given by gmR where R is the value of the resistor in the tank circuit.

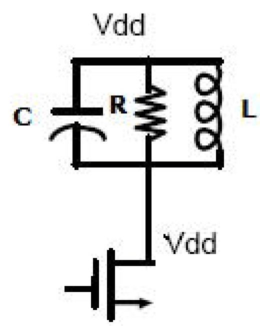


Fig 3.6 the mixer with tuned load.

3.6 Filters

Filters are electronic circuits which are used in signal processing mainly to remove the unwanted signals and allow the desired signals[25]. They are used in Analog as well as Digital circuits. Filters are classified as

- Active or Passive
- Analog or Digital
- Discrete time or Continuous time
- Linear or Non-Linear

- Finite Impulse Response(FIR) or Infinite Impulse Response(IIR)

The oldest types of filters are the passive analog linear which is constructed using Resistors, Capacitors and Inductors. The reason they are called passive filters is because they are made up of passive components like Resistors, Inductors and Capacitors and they do not require an external power supply. Inductors and Capacitors are the reactive elements of the circuit. Inductors conduct at very low frequencies but they block high frequencies, while capacitors are just the opposite they conduct at high frequencies and block low frequency signals. Resistors do not have frequency selection properties; they are used in combination with inductors and capacitors to determine the time constants of the circuit which in turn determine the frequency response of the circuit. Passive filters can be of RC, RL, LC or RLC types. These filters may be used as low pass, high pass, band pass or band stop configurations.

3.6.1 LC Filters.

LC filters are the most popularly used filters at radio frequencies. The LC filters can be used as low-pass, high-pass, band-pass and band stop filters depending on the requirements. Unlike RC or RL filters which are also used widely are attenuators because of the presence of resistive component in it.LC network is either used to generate a signal of a particular frequency or to select a particular frequency from a complex signal. The LC circuit stores electrical energy vibrating at its resonant frequency. The capacitor stores energy in the form of electric field depending on the voltage across it and the inductor stores energy in form of magnetic field depending on the current flowing through it.[24]

Resonance occurs when the inductive and capacitive reactances are equal. The LC circuit cannot resonate on its own; it must be driven by a power supply. The frequency at which it resonates is called the resonant frequency and is given by ω_o.

$$\text{Where } \boldsymbol{\omega_o} = \sqrt{\frac{1}{LC}} \quad (3.6)$$

Equivalent frequency in Hertz is

$$\boldsymbol{F_o} = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \quad (3.7)$$

LC Filters are constructed in L, T and π structures as shown in the Figure.

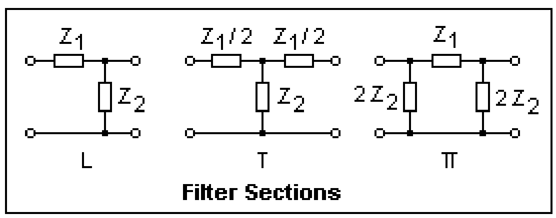


Fig 3.7 various topologies of LC filter.

LC filters can also be used as low pass, high pass; band pass and band reject filters as shown from the figure.

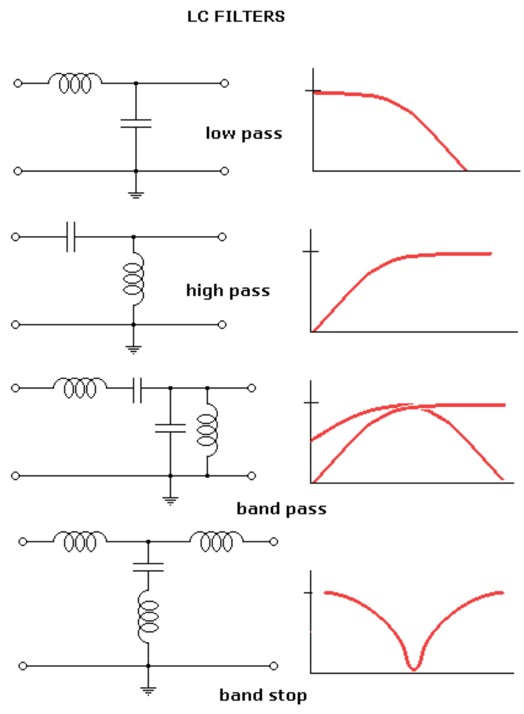


Figure 3.8 circuit and graphical representation of various configurations of LC filter circuits.

4 OSCILLATOR

4.1 Overview

An oscillator is an electronic circuit that produces a repetitive electronic signal which is often a sine wave and sometimes a square wave or saw tooth [23]. Oscillators are used in transmitters, receivers and various kinds of electronic circuits especially radio frequency circuits. Oscillator basically is an amplifier and a filter operating in a positive feedback loop [29]. In order for oscillations to begin the circuit must satisfy the Barkhausen criteria which is Firstly, At resonant frequency the loop gain should be greater than unity and Secondly the loop phase must be $n2\pi$ (where n is an integer).

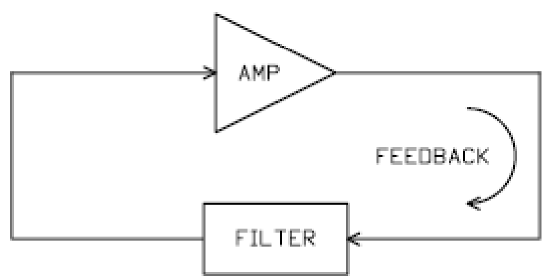


Fig 4.1 Simplified Block diagram of an oscillator

The amplifier provides the gain satisfying the first criteria. For the second criteria, the amplifier is of inverting type which provides a phase shift of π radians and the filter provides another additional phase shift of π radians making it a total of 2π radians around the feedback loop.

An ideal oscillator has a loop gain greater than 1.0 when the amplitude of the oscillations is small and they decrease to 1.0 when the signal reaches the desired amplitude.

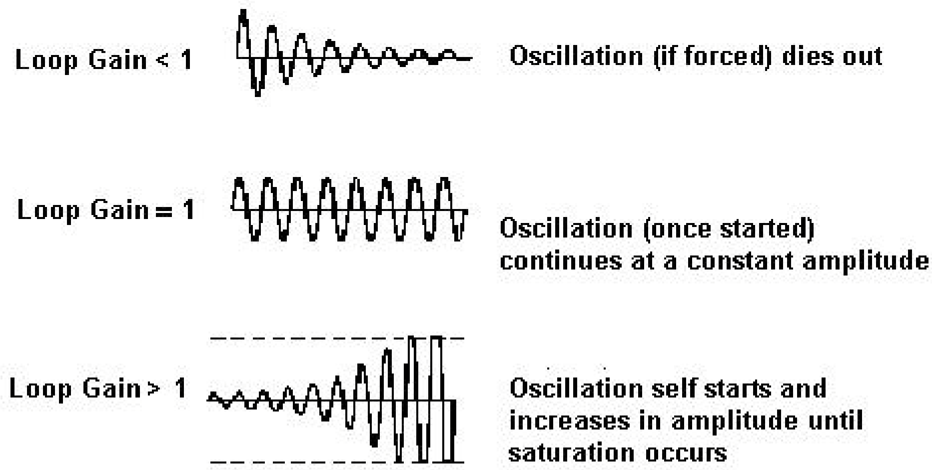


Fig 4.2 Graphical representation of Loop gain versus amplitude of oscillations.

4.2 Ring Oscillator

A ring oscillator is an electronic device composed of odd number of inverters or not gates whose output oscillates between the two voltage levels 0 and 1.The inverters are attached in a chain and the output of the last inverter is fed back to the input of the first inverter and hence the name ring oscillator.

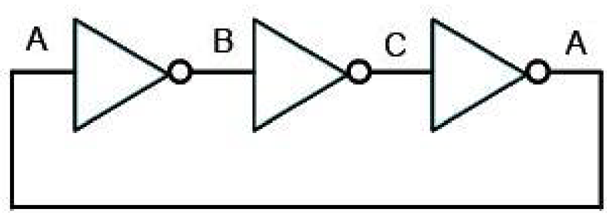


Fig 4.3 Representation of Ring Oscillator.

The input is applied to the first inverter which generates a logical not of the input, since the ring oscillator has odd number of inverters the output of last inverter is a logical not of the first input. The delay of the individual inverters keep adding up at every stage as each inverter introduces a delay of its own.

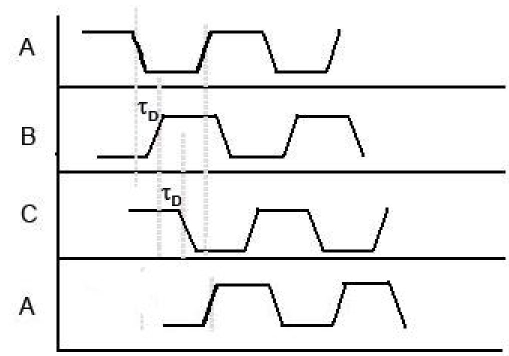


Fig 4.4 Waveform showing delay of individual inverters.

The output of the last inverter is fed back to the input of the first inverter. The final output occurs after a certain delay since when the input is applied and this is fed back to the first input which causes oscillations.

Period of Oscillations $\boldsymbol{T = \frac{1}{n\tau_D}}$ (4.1)

Where n is the number of stages and τ_D is the delay of the individual stage.

4.2.1 Principle.

The ring oscillator is a voltage controlled oscillator (VCO) whose frequency can be controlled by the applied voltage. As the control voltage increases, the frequency of oscillation also increases. The ring oscillator is based on the principal of gate delay. No logic gate can switch immediately as soon as the input is applied, the gate capacitance must be charged to a certain value before current can flow through the device. Hence in the ring oscillator the inverter output changes after a certain amount of time when the input changes. Each inverter contributes a certain delay to the inverter chain and the period of the square wave (or frequency) is equal to the sum of the inverter delays. Adding more inverters increases the total delay of the inverter chain, thereby reducing the frequency of oscillations.

Ring oscillator belongs to the class of time delay oscillators. It consists of a inverting amplifier with a delay element between the input and the output. At the required oscillating frequency the amplifier should have a gain greater than 1.Intially the amplifier input and output are balanced at a certain point but a small amount of noise can cause the output to rise to a certain point. After passing through the delay element a small change in output will be presented at the amplifier input. Hence the output will be amplified with a negative gain greater than 1 or the output changes in direction opposite to the input. This amplified inverted signal propagates from the output to the input, where it is amplified again and inverted and process continues. As a result a square wave is generated with the period of each half of the square wave equal to the delay. This square wave grows in amplitude till it reaches a stable value. Initially the waveform is not square but as it reaches the maximum amplitude, it stabilizes and the signal appears more as a square wave.[23]

4.2.2 Operation.

The ring oscillator consists of a ring of inverters connected to each other where the number of stages and the delay per stage control the frequency of oscillations. The delay through each stage or each inverter can be controlled by the amount of current available to charge or discharge the capacitive load at each stage. This type of circuit is called the current starved inverter [26]. The maximum current available for charge and discharge is controlled by the current source I_{ref}. If the control voltage V_{con} is increased, the current I_{ref} increases which in turn increases the current through transistor M_3 which decreases the time available to discharge the load capacitance of the next stage. The charging time is also decreased as the current through M_4 mirrors current though M_6.Therefore this causes a reduction in τ_D as a result of increase in V_{cont} which increases the frequency of oscillations [31].

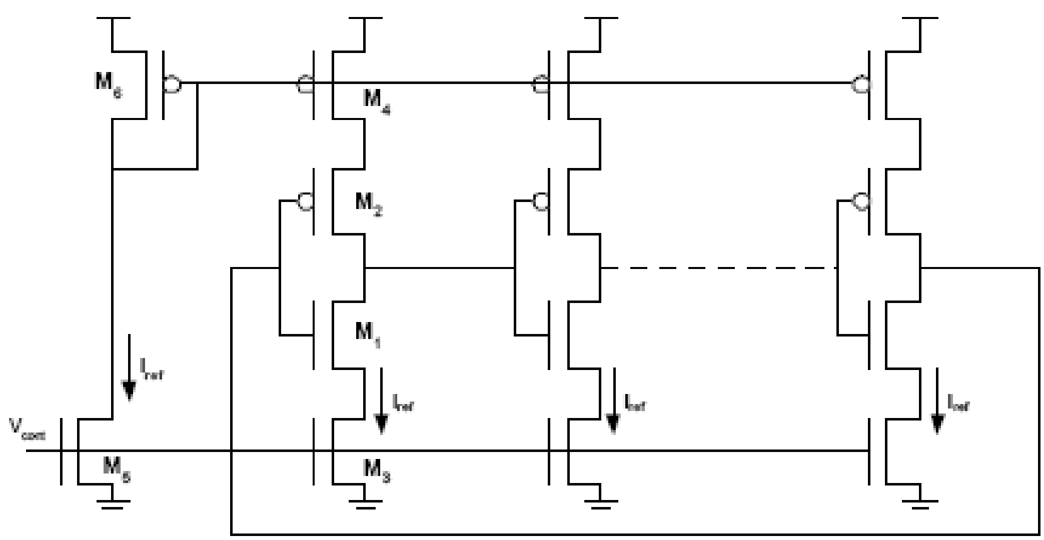


Fig 4.5: A Current Starved Voltage Controlled Oscillator.

5 DESIGN, SIMULATION AND RESULTS.

The main objective of this work was to design and develop the front end of a RF Receiver in 0.18µm CMOS technology. The incoming RF signal was a signal 1.75 GHz which was then down converted to a low IF signal for further signal processing by the digital components. The Front End of the receiver consists of the LNA which receives the incoming RF signal which might be weak in terms of signal strength as well as affected by noise. The low noise amplifier designed is of differential topology to reduce or eliminate the common mode noise and is of broadband configuration. The Signal amplified by the LNA is down converted to an IF signal by a down converting mixer. The mixer used is also of double balanced structure as it has better susceptibility of noise because of the differential RF signal and the differential LO signals used in the topology. The RF signal is down converted to an IF of 250MHz. The mixer is used in combination with an LC filter to remove the image signals and other unwanted higher order components.

The local oscillator signal for the mixer is generated by a VCO which is a ring oscillator. The ring oscillator is used because it has very fine tuning capacity. The preliminary IF signal of 250 MHz is again further down converted to a lower IF signal of 50MHz by another mixer stage from where the signal can be given to an ADC to be converted to digital type and undergo digital signal processing.

5.1 Low Noise Amplifier.

The Cherry Hooper amplifier used in this work is of differential topology. The circuit consists of only nMOS transistors as they are faster compared to pMOS transistors and pMOS transistors add unwanted capacitance at the output node of the amplifier. The Cherry Hooper Amplifier circuit used in this work is shown in the figure.

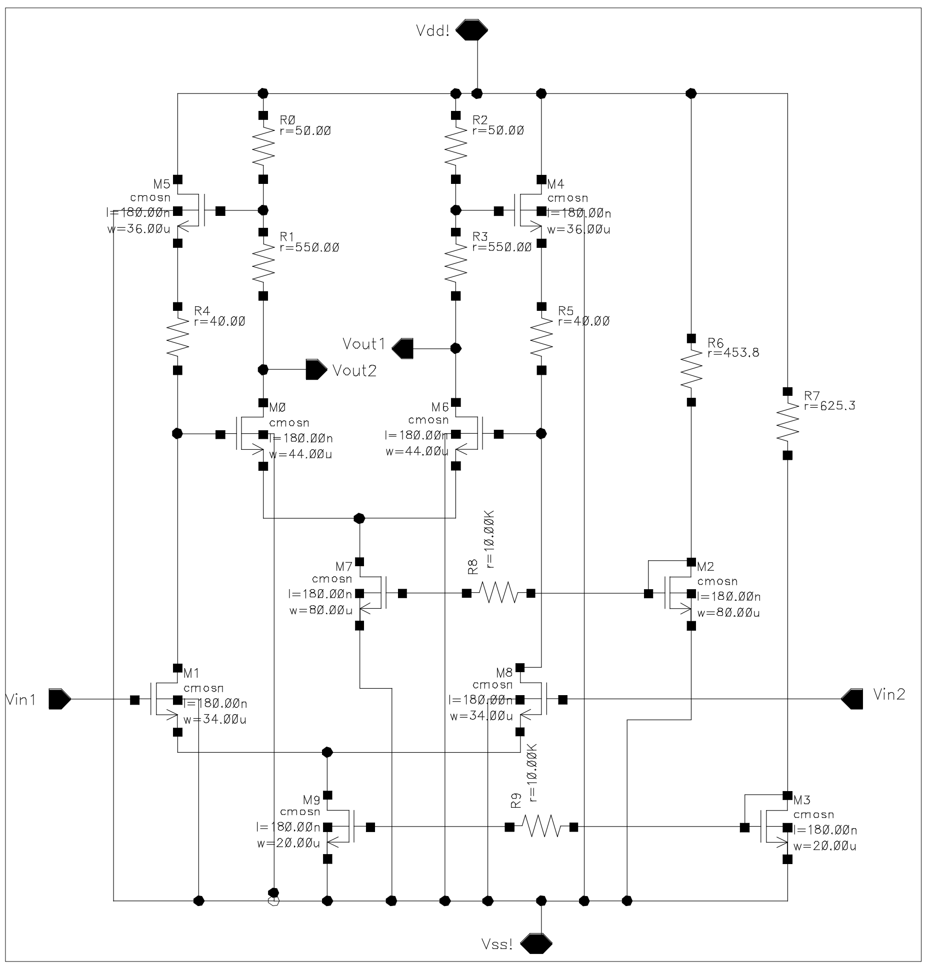


Fig 5.1 Modified Cherry Hooper Amplifier with Source Follower.

The Cherry Hooper amplifier is designed with an input dc offset of 0.9 V and output dc offset of 0.9 V. The amplifier is given an input signal of 1.75 GHz and the transient response is as shown in the figure.

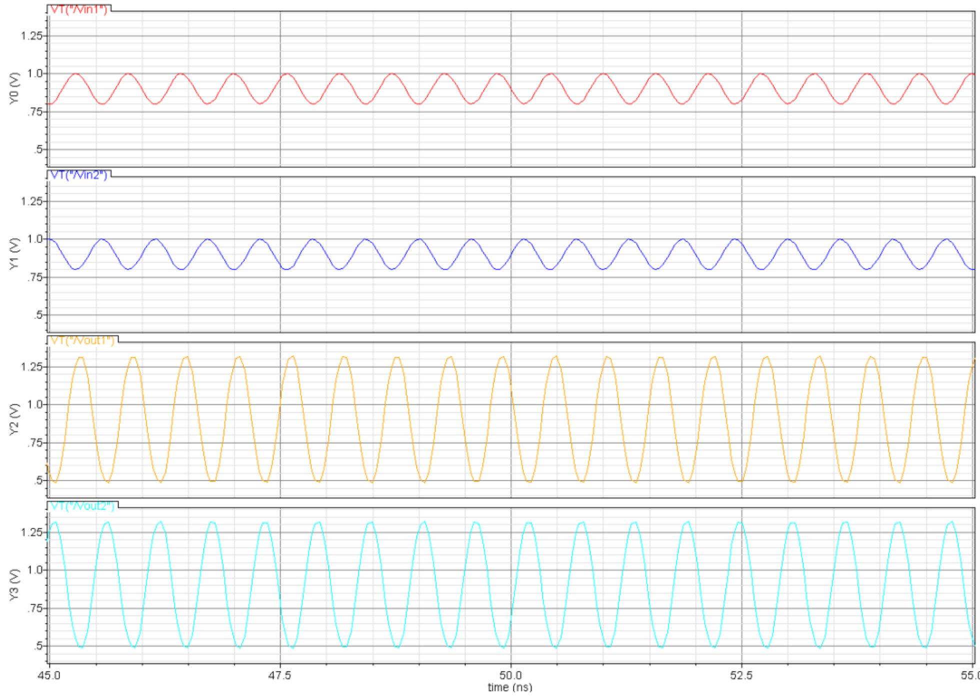


Fig 5.2 Transient response of the differential input differential output of Cherry Hooper amplifier for an input signal of 1.75GHz.

The Cherry Hooper amplifier has single ended ac gain of 9.08 dB and bandwidth of 1.752GHz with maximum operating frequency of 1.75 GHz. The differential gain of the circuit is about twice the single ended gain. The gain of the amplifier can be increased by making the ratio of resistors R_1 and R_2 as high as possible. The gain of the circuit can also be increased by increasing the biasing current but power dissipation is also another important consideration. The power dissipation for the LNA is 8.8mW.

Noise figure is another important parameter of the LNA which helps determine the amount of corruption of input noise relative to the output noise. The noise figure should be as low as possible and is measured in terms of dB.

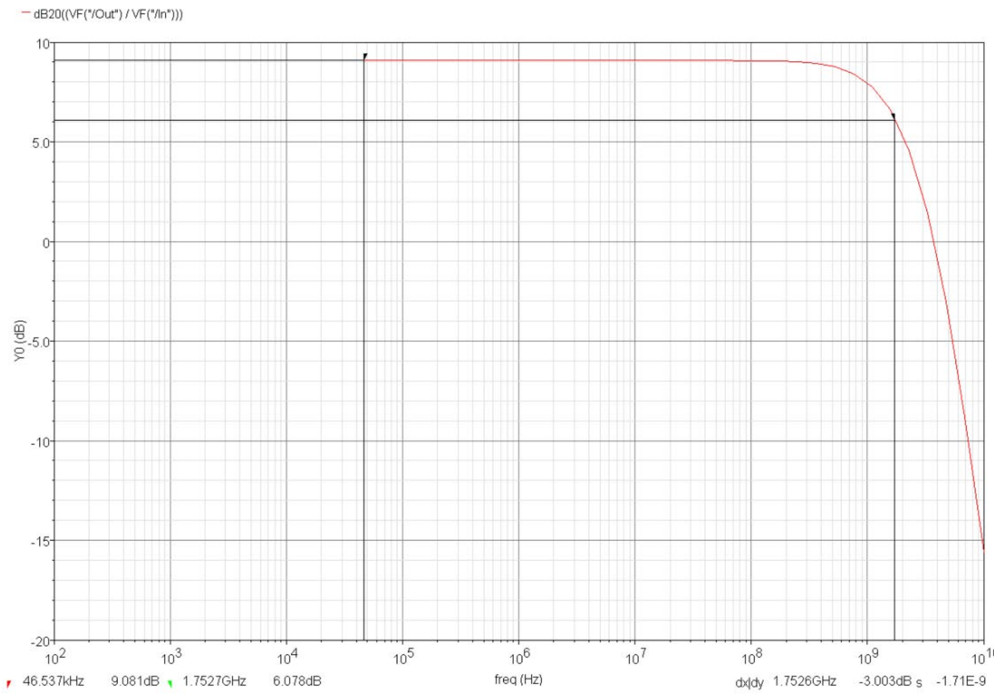


Fig 5.3 AC analysis showing the single ended gain of the LNA and the bandwidth.

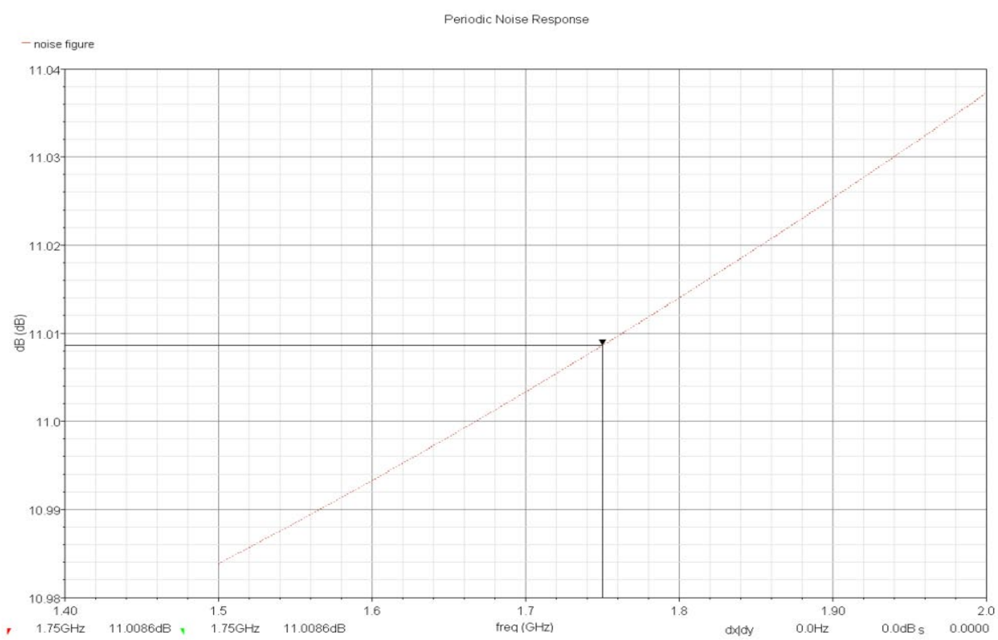


Fig 5.4 Noise Figure of the LNA in dB.

Linearity is a very important parameter which determines the performance of the circuit especially the Low Noise Amplifier. Linearity can be measure in terms on 1 dB compression point as well as the Input Third order Intercept point. The gain of the LNA remains linear till a particular frequency and then at certain point if the input signal is increased in lower it is not amplified by same amount. At this point where there is a 1 dB drop is called the 1 dB compression point and beyond this points the gain of the amplifier decreases. Hence beyond the 1 dB compression point the LNA loses its amplification property.

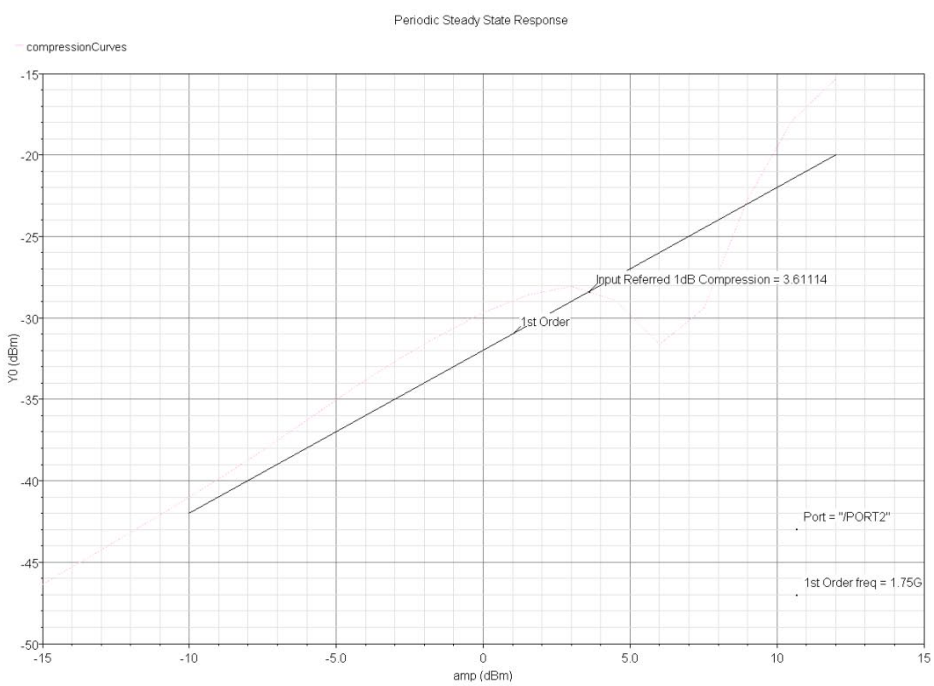


Fig 5.5 Graph showing the 1 dB compression point of the LNA which is 3.61 dBm.

IIP3 (Input third Order Intercept Point)

IIP3 is defined as the point where the fundamental and the third order response intercept. This parameter indicates how well the amplifier performs in the presence of nearby signals. Two signals in this case of frequencies 1.75 GHz (fundamental) and 1.76 GHz are applied to the LNA and their intercept point is as shown in the figure. The IIP3 is usually greater than the 1 dB compression point by 5~10 dB.

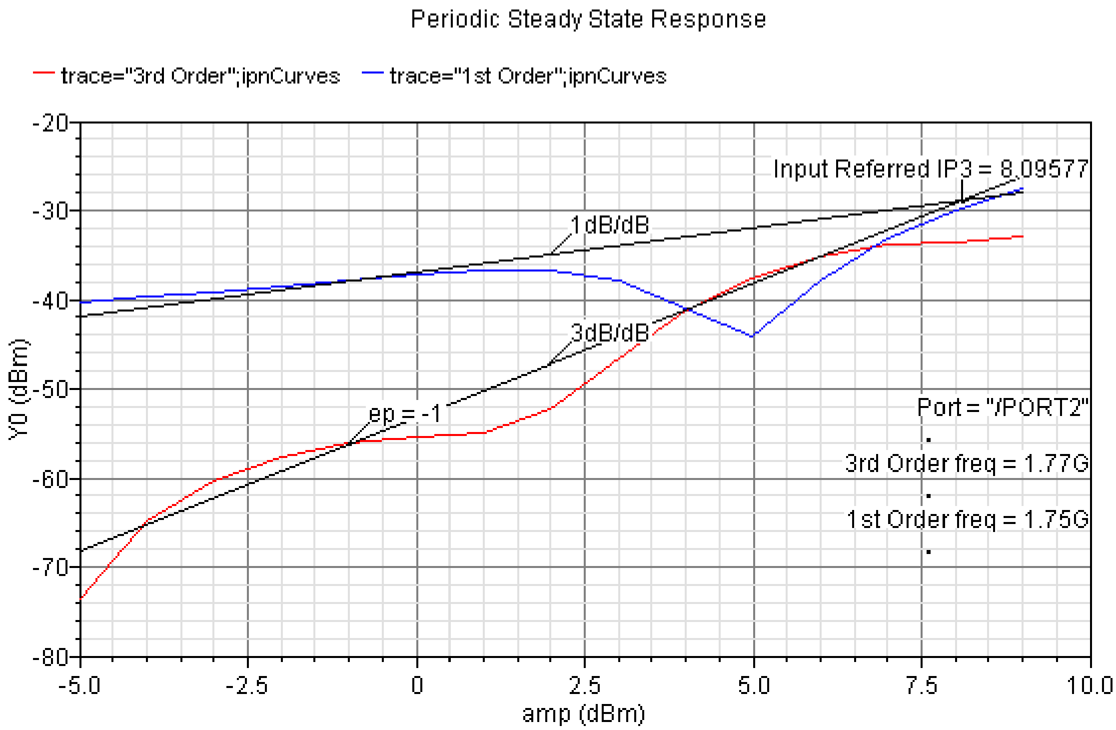


Fig 5.6 Graph Showing the Input Intercept Point of 3rd Order.

Circuit (LNA)	Single Ended Gain	Bandwidth	Technology	Noise Figure at I GHz	Supply voltage	Power Dissipation
Sackinger and Fisher[27]	8 dB	3 GHz	0.35um	16 dB	2.5 V	13.3 mW
Holdenreid,Lynch and Haslett[19]	10.4 dB	2.1 GHz	0.35um	14.2 dB	1.8 V	20.1 mW
This work	9.1 dB	1.75 GHz	0.18um	11.08 dB	1.8 V	9.8 mW

Table 1 Showing Comparison of this LNA results with previous works.

5.2 Down Conversion Mixer.

The RF signal from the antenna which is amplified by the low noise amplifier is of high frequency. These signals need to be converted to digital form for digital signal processing. In order to ensure signals can undergo proper signal processing they are down converted to lower intermediate frequencies (IF) and then passed forward. Gilbert mixer is used in this work as the LNA was of differential topology and it gives an amplified differential output signal. The double balanced mixer has a differential RF signal of 1.75 GHz and a locally generated signal of 2 GHz using a voltage controlled ring oscillator given to 2 inputs. The schematic of the Gilbert Mixer is as shown in the figure.

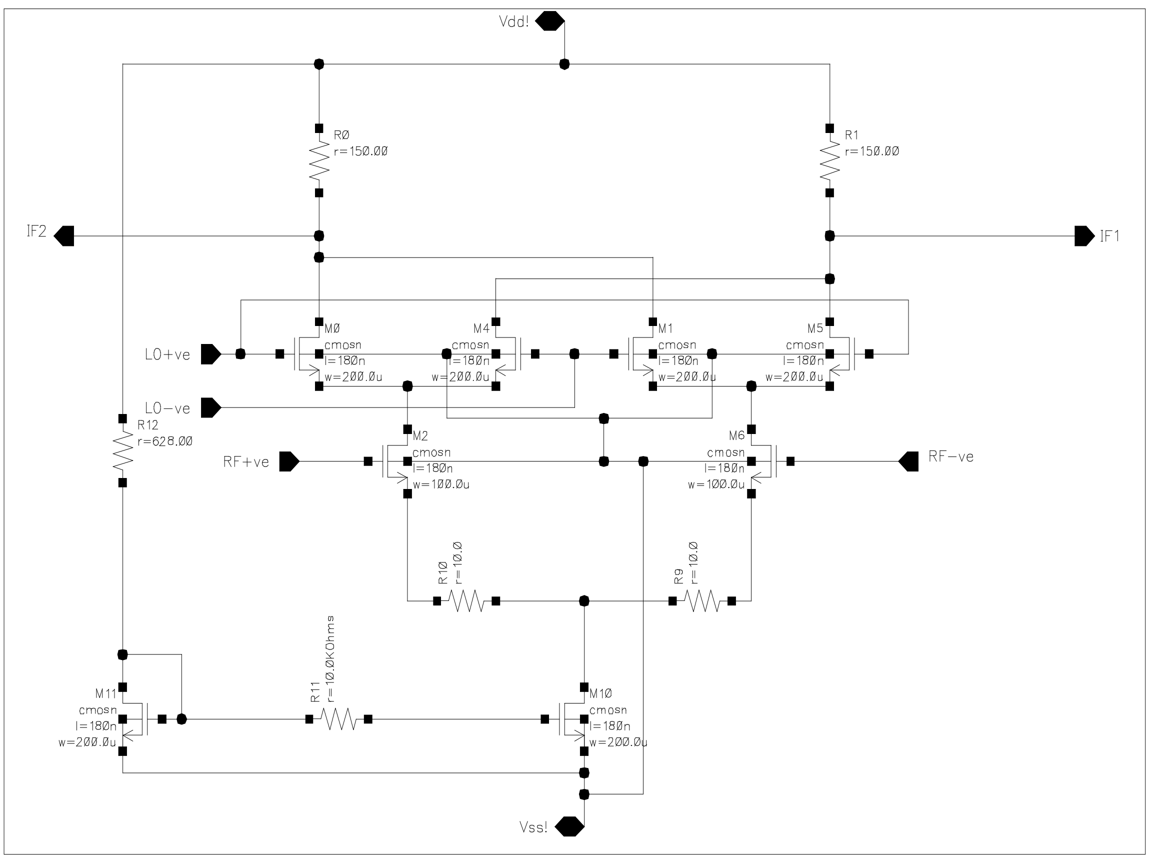


Fig 5.7 a double balanced Gilbert Cell Mixer.

The RF signal of 1.75 GHz is given to the differential RF inputs and the local oscillator signal of 2 GHz is given to the LO terminals. As a result of the mixing of the 2 signals the difference of the 2 signals and the unwanted higher order components are available at the IF (differential) output. In order to remove the higher frequency components a filter is used. The filter used in this work is an LC filter. The filter allows the difference of the RF and LO frequencies to pass through and blocks all the other unwanted components which contain the sum of the RF and LO frequencies as well as higher order RF and LO frequencies. The transient response of the mixer is as shown in the figure.

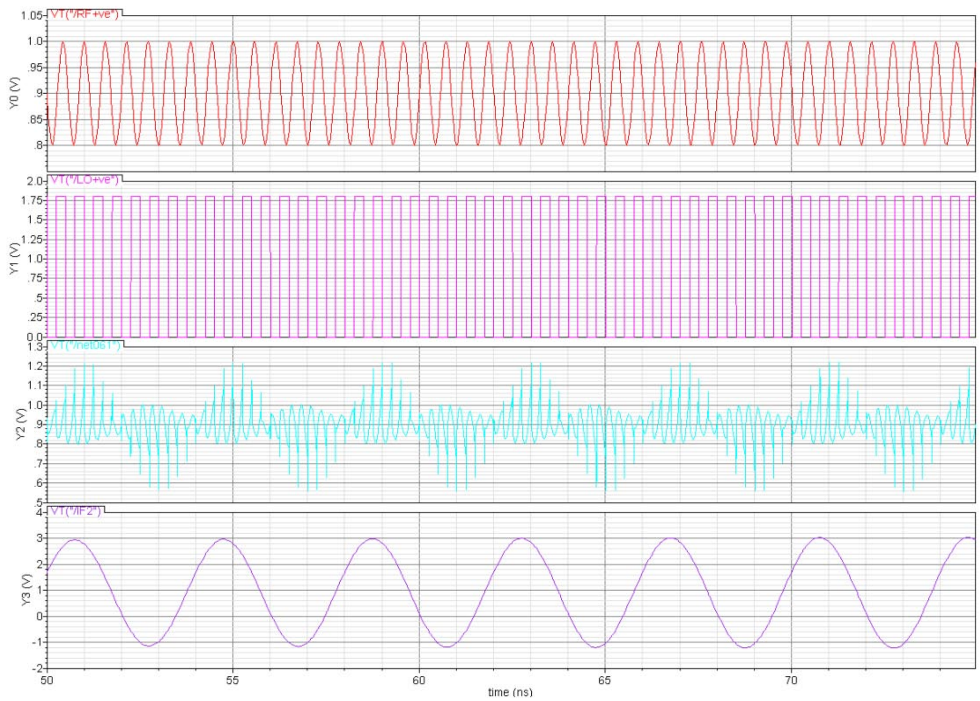
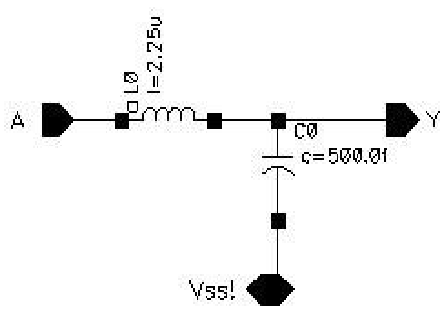


Fig 5.8 Transient Response of mixer for RF signal of 1.75 GHz and LO signal of 2 GHz.(output of mixer before and after filtering is shown)

5.3 Filter.

The mixer output contains the sum of the RF and LO frequencies, the difference of RF and LO frequencies which is the required signals and several higher order components of the RF and LO signals.The LC second order filter used for filtering allows only the difference or the wanted mixed signal to pass through the filter to undergo further processing. The second order LC filter schematic and the frequency response is as shown in the figure.



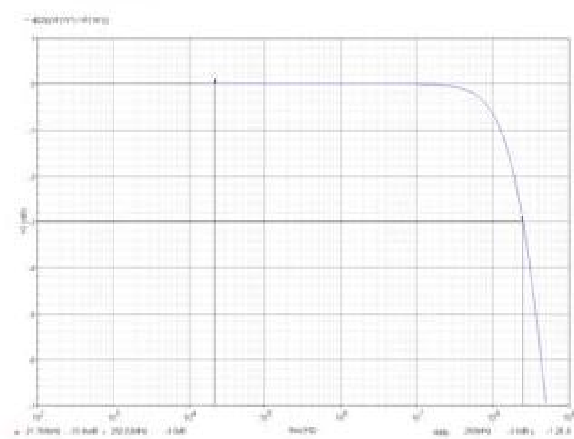


Fig 5.9: LC filter for cutoff frequency of 250 MHz and the frequency response of the filter.

5.4 Second Down conversion Mixer.

The IF signal from the output of the first mixer of frequency 250 MHz is further down converted to a lower IF frequency of 50 MHz using a second mixer. Here the local oscillator signal is of 200 MHz also generated using a voltage controlled ring oscillator.

This mixed signal contains the IF signal of 50 MHz and also the undesired higher order frequency components. These signals are filtered out using the second order LC filter of cutoff frequency 50 MHz The mixers chain might include a band pass filter in between the two stages. Impedance matching between the mixer and the filter or the mixer chain is not necessary in case they are on the same chip. The impedance matching between the mixer and filter is also not required unless the filter is off chip. The transient response of the second mixer is as shown in the figure.

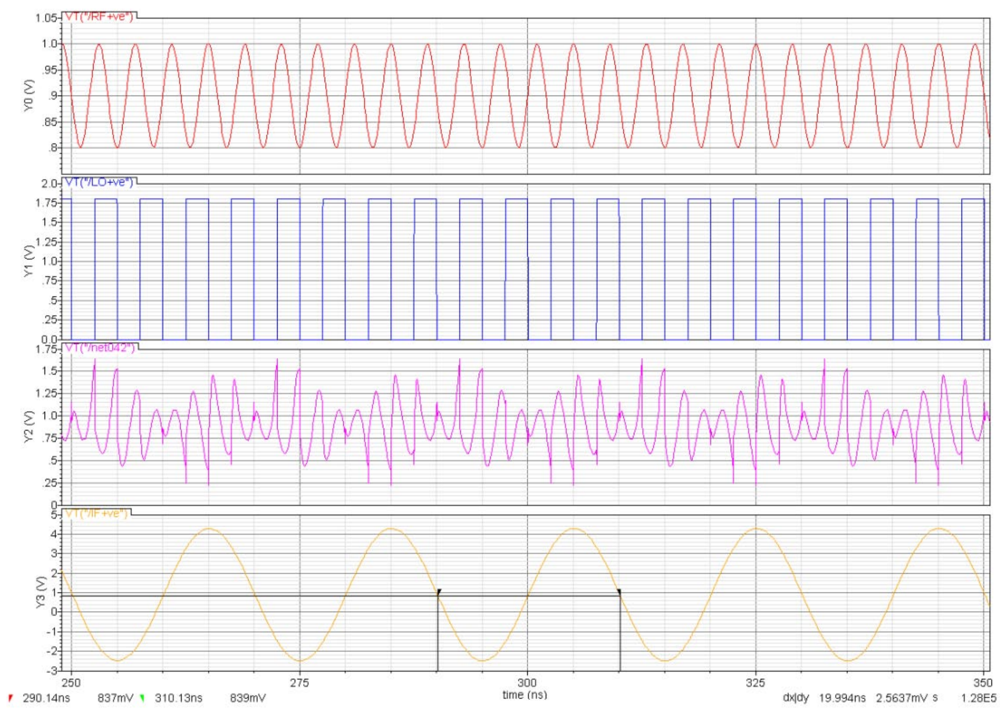


Fig 5.10 Transient response of the second down conversion mixer with RF signal of 250 MHz and LO of 200 MHz The mixer output and filtered output is also shown.

5.5 Oscillator.

The LO input to the mixer is a square wave which is generated using the voltage controlled ring oscillator. The voltage controlled ring oscillator generates different frequencies of oscillations depending on the control voltage. The ring oscillator has been used in this work as it has very fine tuning capacity to generate exact and precise oscillating frequencies. The ring oscillator has odd number of inverting stages. In this work it is a 3 stage ring oscillator and increasing the stages decreases the frequency of oscillations and tuning range. The schematic of the ring oscillator is as shown in the figure.

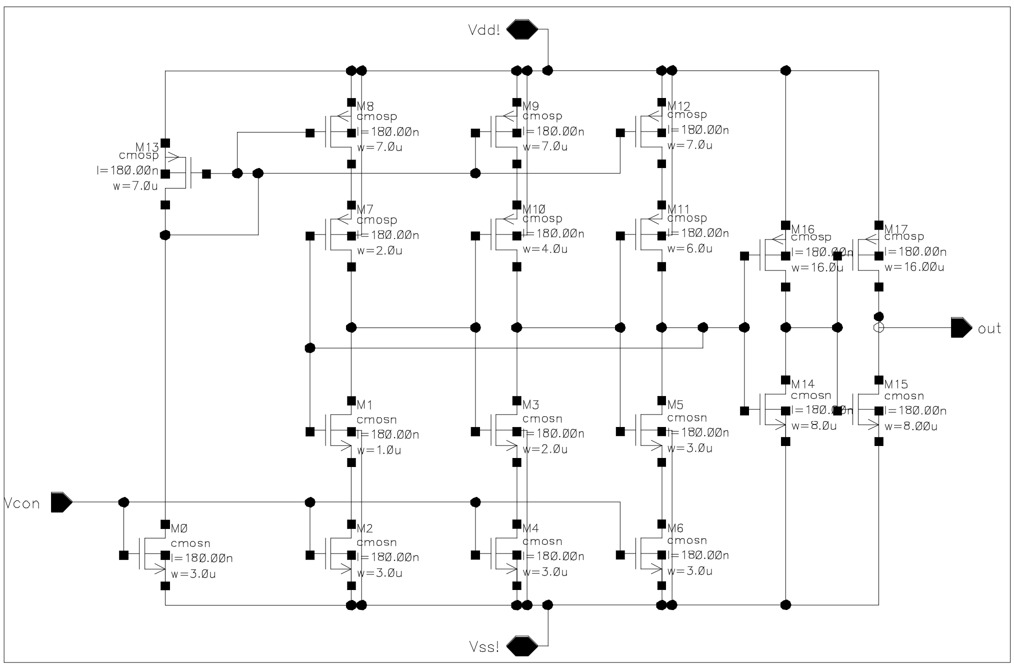


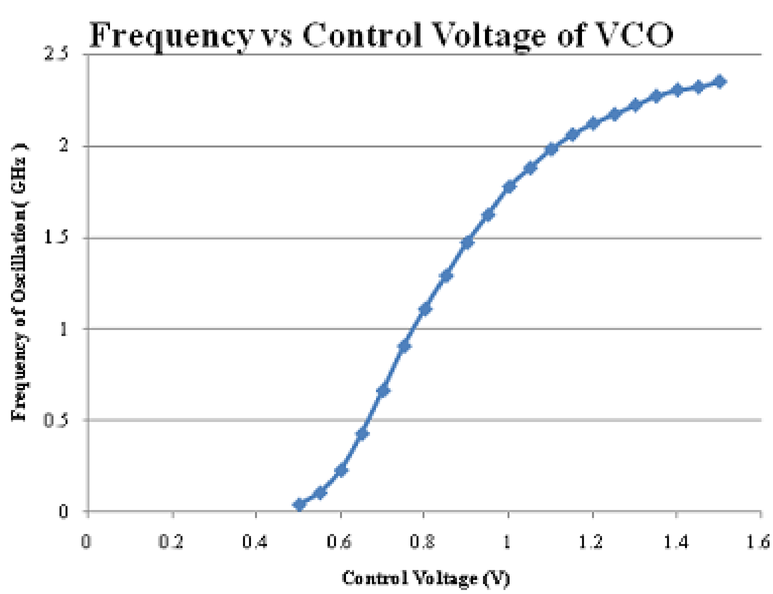
Fig 5.11 Schematic of Voltage Controlled Ring Oscillator.

The variation in control voltage causes the variation in the reference current through the transistors which in turn changes the time available of the charge and discharge at the output of each inverter which increases or decreases the delay of the inverter. Depending on the number of stages of the inverter and the delay of the individual inverter, the oscillating frequency is determined. The schematic of the control voltage to generate an oscillating frequency of 2 GHz is as shown in the figure.

Table 2 showing variation of control voltage with oscillation frequency

Vcontrol(V)	Frequency(GHz)
0.5	0.043
0.55	0.108
0.6	0.232
0.65	0.431
0.7	0.666
0.75	0.909
0.8	1.111
0.85	1.291
0.9	1.472
0.95	1.623
1.0	1.777
1.05	1.879
1.1	1.981
1.15	2.061
1.2	2.122
1.25	2.172
1.3	2.222
1.35	2.271
1.4	2.305
1.45	2.321
1.5	2.351

5.12 Graph of Control Voltage vs Oscillation Frequency.



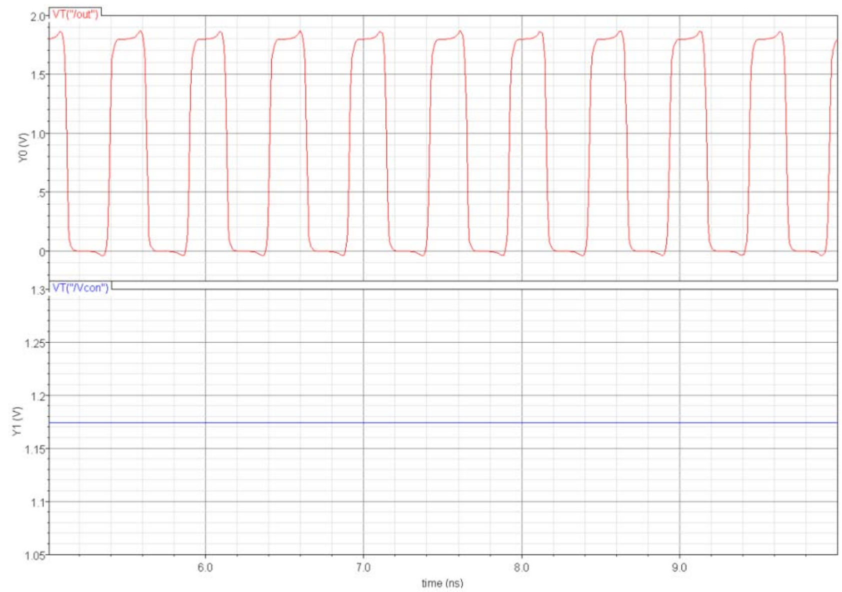


Fig 5.13 Waveform showing oscillator frequency of 2 GHz for a control voltage of 1.17 V.

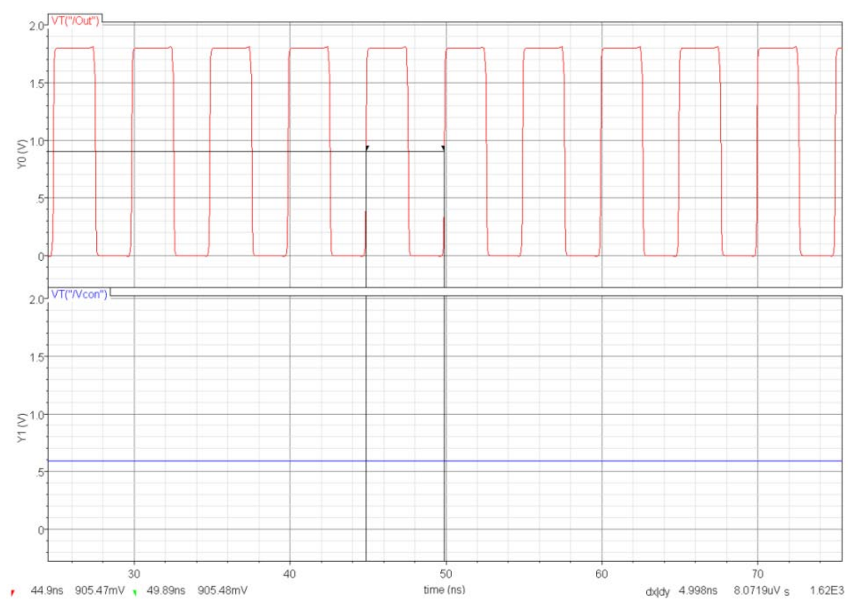


Fig 5.14 Waveform showing oscillator frequency of 200 MHz for a control voltage of 0.59 V.

5.6 Receiver Front End.

The schematic of the entire receiver front end consisting of the LNA-MIXER-VCO combination is as shown in the figure. Both the stages of mixers are shown in the schematic. The LC filters are combined with the mixer block and hence they are not shown in the schematic separately.

The Receiver has an incoming RF signal of 1.75 GHz into the LNA. The signal is amplified by the LNA and then passed into the RF input terminal of the mixer which is also fed by a local oscillator signal of 2 GHz. The Down converted IF signal is of 250 MHz and is the input to the RF terminal of the next mixer. The second mixer is fed by a local oscillator signal of 200 MHz and the mixing results in a lower IF signal of 50MHz.This signal continues to the other blocks of the receiver.

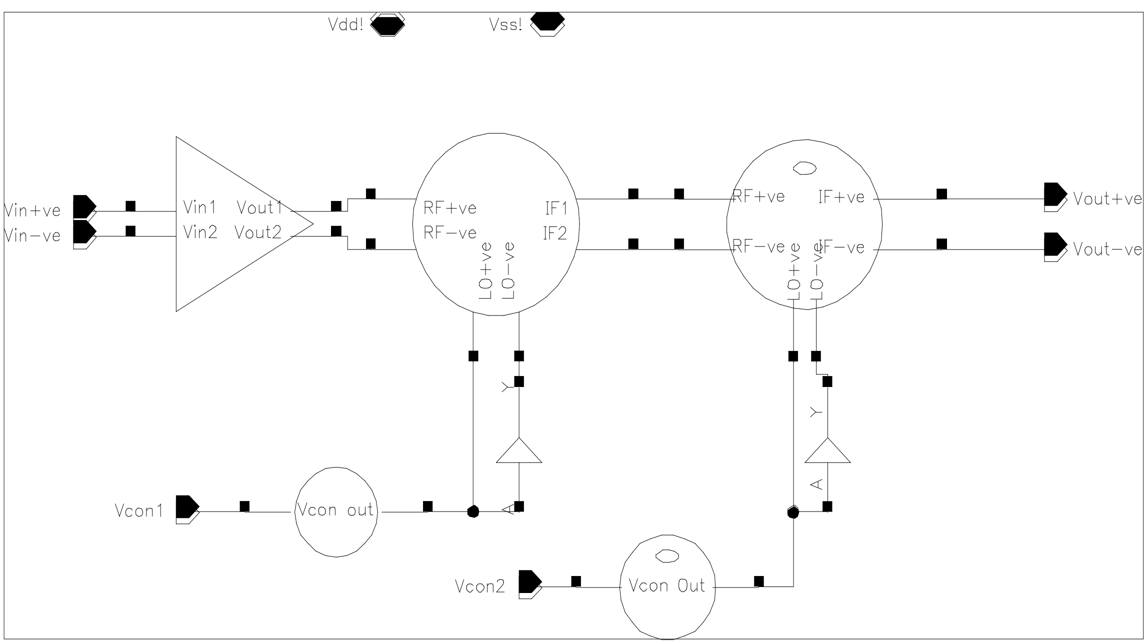


Fig 5.15 Schematic showing the receiver front end with LNA, 2 stages of MIXER and ring oscillator.

The first component of any receiver is the RF antenna which receives all the range of frequencies coming through the wireless channel.The antenna receives the signal which might contain added noise along with wanted RF signal.The RF antenna is followed by an RF bandpass filter which allows only the required message signal to go through to the front end of the receiver.The filtered signal strength might be weak in terms of signal amplitude and needs to be boosted in terms of amplitude and power .This signal is fed to the input of the low noise amplifier(LNA)

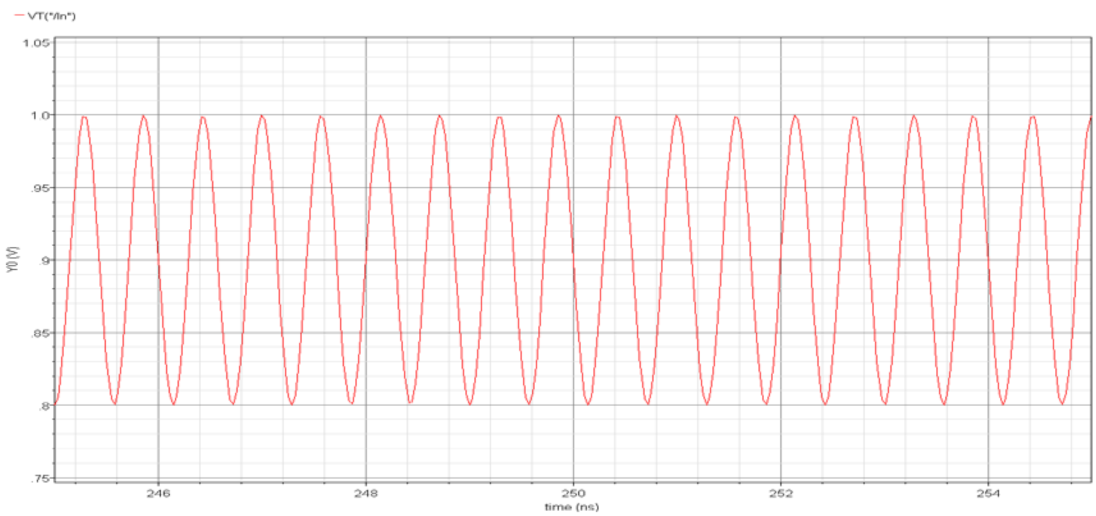


Fig 5.16 Waveform showing the input RF signal of 1.75 GHz.

The input signal of 1.75 GHz is fed to the differential inputs of the Cherry Hooper amplifier which in this work has a gain of 9.08 dB. The gain of the Cherry Hooper amplifier when connected in the receiver chain does not give the same gain due to the loading effect of the succeeding stages. The gain of the LNA is a little less than 9.08 dB. The amplified signal available at the output of the LNA is as shown in the figure.

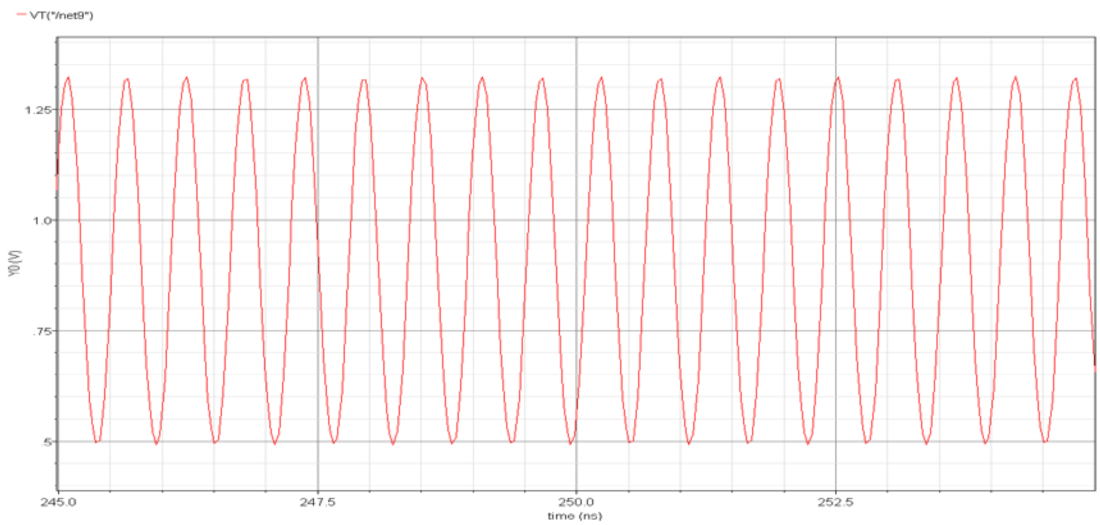


Fig 5.17 Waveform showing the output of the LNA.

The amplified signal from the LNA goes to the RF inputs to the first of the two mixer chain. The mixer has two inputs one is the RF signal and other is the local oscillator signal generated by the Voltage Controlled Oscillator (VCO).The local oscillator frequency of 2 GHz is generated for a control voltage of 1.17 V.

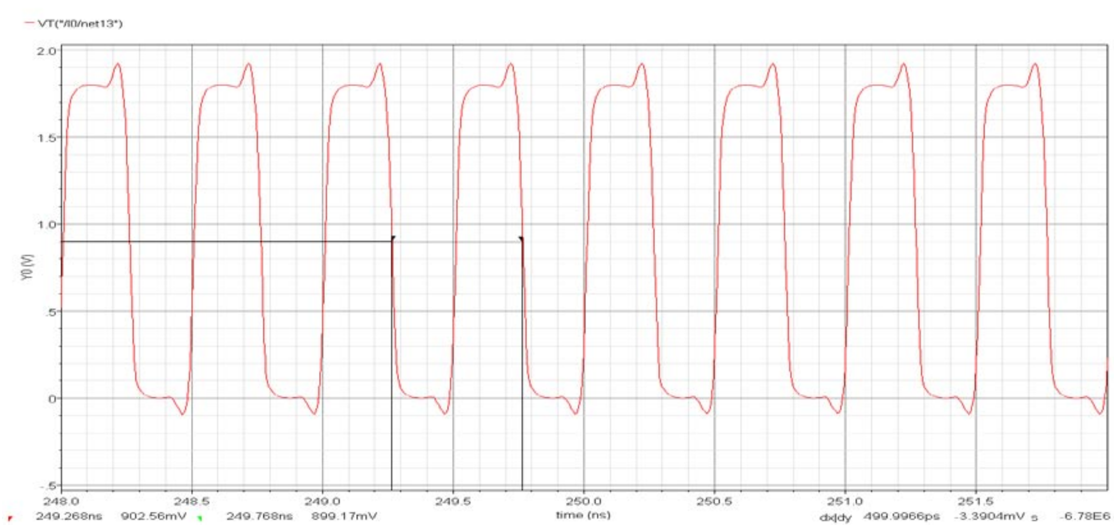


Fig 5.18 Waveform showing square wave of 2 GHz for a control voltage of 1.17 V generated using the Voltage Controlled Ring Oscillator.

The RF signal of 1.75 GHz and the LO signal of 2 GHz undergo mixing and result in signals which contain the sum,difference and higher order components of the input signals.The wanted signal ie the difference of 250 MHz is filtered out using a second order low pass LC filter.The transient response of the signal is as shown in the figure.

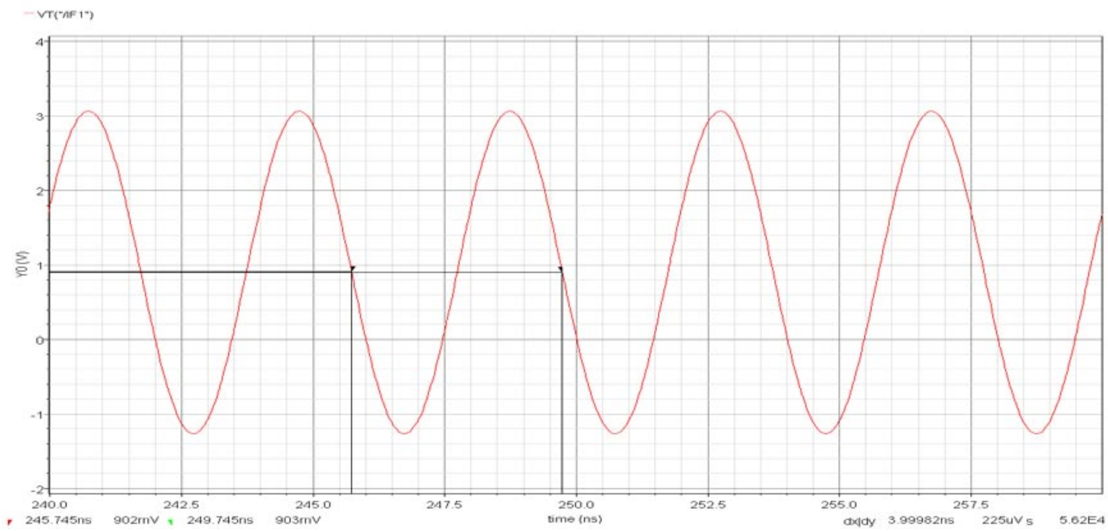


Fig 5.19 Waveform showing the output of mixer with frequency of 250 MHz resulting from an RF signal of 1.75 GHz and LO signal of 2 GHz.

The Intermediate Frequency of 250 MHz is fed into the RF input of the second mixer. The local oscillator signal of 200 MHz is generated also using the ring oscillator for a control voltage of 0.59 V. The transient response of the ring oscillator for control voltage of 0.59 V is shown in the figure.

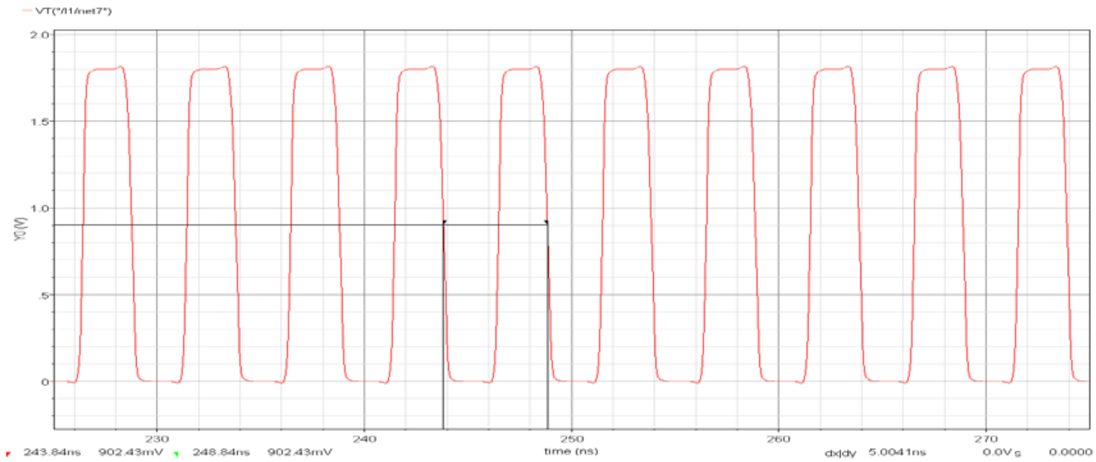


Fig 5.20 Waveform showing square wave of 200 MHz for a control voltage of 0.59 V generated using the Voltage Controlled Ring Oscillator.

The RF signal of 250 MHz and the LO signal of 200 MHz as a result of mixing produce signals which contain the sum, difference and higher order components of the input frequencies. The required IF signal of 50 MHz is obtained by low pass filtering the output.

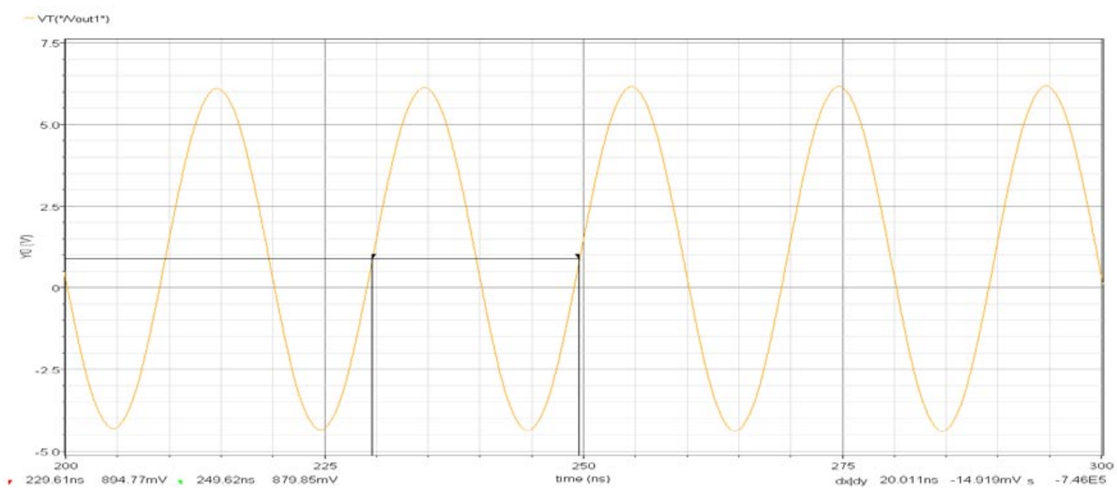


Fig 5.21 Waveform showing output of second mixer of 50 MHz resulting from difference of RF frequency of 250 MHz and LO signal of 200 MHz.

6 SUMMARY, CONCLUSION AND FUTURE WORK

The Front end of a RF CMOS Receiver was designed and implemented in 0.18um technology with a supply voltage of 1.8 V. The RF Front End consisted of the LNA-MIXER-OSCILLATOR combination. The summary of the entire work is as follows:

Technology: **0.18µm TSMC**

Supply Voltage: **1.8 V**

Low Noise Amplifier

Circuit Topology: Cherry Hooper Amplifier (differential architecture).

Single Ended Gain: 9.1 dB

Noise Figure: 11.08 dB

Bandwidth: 1.752 GHz

Power Dissipation: 9.8 mW

Mixer

Circuit topology: Gilbert Cell Mixer (double balanced architecture)

Power Dissipation: 20.9 mW

Oscillator

Circuit Topology: Voltage Controlled Ring Oscillator

Power Dissipation: 43 mW at a maximum frequency of 2.4 GHz.

Tuning Range: 43 MHz at 0.5 V to 2.35 GHz at 1.5 V.

The LNA implemented in this work had very low gain (< 10 dB) compared to the LNA using inductor peaking technique, therefore LNA with could be implemented with inductor peaking technique in order to increase the gain and the bandwidth of the LNA.A band pass filtering stage could be introduced between the mixer chain stages to provide better isolation between the two stages. An alternate topology for the Oscillator could be used as the ring oscillator as it has very low noise tolerance.

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