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Fall 2004

CEG 360/560 EE 415/651: Digital System Design

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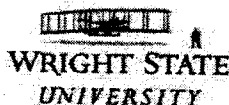


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Wright State University
College of Engineering and Computer Science
Department of Computer Science and Engineering

Digital System Design

CEG 360/560 - EE 451/651

Fall Quarter, 2004

Professor: Travis E. Doom, Ph.D.

Professor's Office: 331 Russ Engineering Center

Office Hours: 3:45-4:45 TR. Other office hours by appointment (via email).

Email: (Preferred contact) doom@cs.wright.edu

Office Phone: (937) 775-5105

Room & Time:

Section 01: 12:20 - 1:35 TR 148 Russ

Section 03: 2:15 - 3:30 TR 306 Oelman

Laboratory: 355 Russ Engineering Center

Lead Lab Instructor: Sridhar Ramachandran, sramacha@cs.wright.edu;

Lab Instructor: TBA

Time: Concurrent enrollment in a 1-hour, 50-minute weekly lab session is required:

Section 05: 2:00PM M

Section 06: 2:10PM T

Section 07: 10:20AM R

Section 08: 8:00PM M

Section 09: 8:00PM W

Course Description:

Design of digital systems. Topics include flip-flops, registers, counters, programmable logic devices, memory devices, register-level design, and microcomputer system organization. Students must show competency in the design of digital systems. 3 hours lecture, 2 hours lab. Prerequisite: CEG 260.

Textbook:

Required: Mano, Morris and Kime, Charles (1997). "Logic and Computer Design Fundamentals", any edition, New Jersey: Prentice-Hall, ISBN 0-13-031486-2 (2e), 0-13-140539-X (3e) .

Reference: Givone, Donald (2003). "Digital Principles and Design", New York: McGraw-Hill, ISBN 0-07-252503-7.

Prerequisites: CEG 260 or equivalent

1. Fundamentals of Boolean Algebra, including the minimization of logic functions to SOP or POS form.
2. Analysis of logic circuits.
3. The design and testing digital designs using SSI and MSI components.
4. Optimizations techniques to minimize gate count, IC count, or time delay.
5. The design and use of simple memory devices and sequential circuits
6. Decoders, multiplexors, and bus logic.
7. Documentation standards for logic designs.

Objectives: This course has two primary objectives. The first is content-based. We hope to teach students the fundamental principles of design for sequential digital devices. At the end of this course, each passing student should be able to:

1. Describe all the basic types of flip-flops with their characteristics.
2. Describe the characteristics of standard sequential devices, including counters and registers.
3. Describe the characteristics of a variety of programmable devices, including PLDs, RAMs, and ROMs.
4. Discuss basic microcomputer organization.

The second objective is skill-based. Students will exercise their ability to apply these principles in practical application through laboratory projects. At the end of this course, each passing student should be able to:

1. Analyze a given sequential circuit, producing an appropriate state table and state diagrams.
2. Design sequential systems of moderate complexity to satisfy given specifications for function and predict its timing behavior.
3. Produce an appropriate state table and state diagrams for a sequential system.
4. Utilize CAD tools to implement and debug simulations of any combinational or sequential design of moderate complexity.
5. Rigorously apply accepted standards to document sequential logic designs to their work.

Grading: A student's demonstration of their ability to discuss issues, solve problems, and demonstrate mastery of digital design will be the underlying metric for the determination of a student's overall grade in this course. Students will be provided the opportunity to demonstrate their mastery through examinations and laboratory projects. Grades will be assigned on a standard A/90%, B/80%, C/70%, D/60%, F/60%- scale. Clustering of grades may cause the thresholds to be lowered; they will not be raised. The instructor reserved the right to fail any student who does not attain both a passing grade (70%+) in the laboratory and at least a grade of 50% on the final. The overall course grade will be the weighted sum of the three grades:

40%	Laboratory Projects	Labs #1-3: @ 30 pts.; Lab #4 @ 40
30%	1/2-Hour Examinations	34 pts. each (best 3 of 4)
30%	Final Examination	100 pts.
332 pts. Total		

Retakes: Students who take this course a second time are strongly encouraged to also retake the laboratory. However, students who are re-taking this course may choose to waive the laboratory with instructor permission. In this case, their overall course grade will be determined on the basis of all four quizzes (no drop) and the final (236 point total). Laboratory grades from previous quarters are never used in grade calculation.

Laboratory Projects: The laboratory projects are designed to help you learn the course concepts and

are the primary course "homework". The laboratory projects may be very time consuming if you are not comfortable with the necessary concepts before beginning the project. Each lab consists of one or more "pre-lab" designs which must be turned in before your scheduled "in-lab" section where you will be asked to demonstrate and answer questions about your project.

Students must attend their scheduled lab section every week. This is the only time that a lab instructor is guaranteed to be present to sign-off in-lab demonstrations and to explain concepts necessary for the next pre-lab homework. Some pre-labs require that students have access to the laboratory tools. Student ID cards will permit access to the Lab in 355 RC at any time in which a scheduled lab section of CEG 260 or CEG 360 is not using the room. Students may perform their inlab work at home by installing the software that comes with the most recent version of the textbook.

Points will be deducted for projects submitted late. No points will be awarded for projects that are more than one week late. Corrupt files or other computer problems will not be considered a sufficient excuse to extend this deadline. It is your responsibility to back-up your work! I strongly suggest that you save your work to multiple diskettes to aid in the recovery of corrupt files.

Examinations: Four 1/2-hour midterm examinations and one final examination will be administered as announced throughout the quarter. Midterm examinations are "extended homeworks" and are designed to encourage students to cover course material at a steady pace and to provide feedback throughout the quarter. Midterms are provided to *help* enhance overall understanding, not to weight heavily against you in the final grade determination. Therefore, only the highest three of each student's four 1/2-hour midterm examinations will be used in the calculation of the final grade.

In order to be fair to all students and allow the timely return of examinations, make-ups of 1/2-hour examinations are not permitted under any circumstance. Absences, periodic poor performance, unexpected tardiness, and other difficulties are sometimes unavoidable and therefore each student's lowest midterm score is disregarded in the calculation of the overall grade. Students missing multiple midterm examinations for a documented emergency should consider petitioning for withdrawal from the course.

It is neither possible, nor desirable, to discuss every nuance of the material covered in this course during our limited class time. Students should be aware that although we will discuss the most important materials in class, the textbook contains important facts that may not be discussed in class. Students should not only be able to discuss course concepts in detail, but they should also be able to demonstrate their mastery by applying these concepts on examinations to related problems with which they have no previous experience.

Undergraduate students: The examinations will be closed-book but undergraduate students may use one sheet of 8.5 x 11" notes (double-sided) as reference. An undergraduate student who receives 90% or higher on each of the four midterm examinations as well as 90% or higher on each of the four laboratory projects may waive the final after verifying this fact with the instructor.

Graduate Students: Graduates students are expected to master this material and commit it fully to memory. Graduate students may not use notes during the examination. Furthermore, all graduate students are required to take the course final.

Midterm examinations will occur at the normally scheduled class time and location unless announced otherwise in class. The final examination is cumulative and will take place during the university scheduled time period in the normally scheduled class location unless announced otherwise in class.

Course Assignments: The instructor will provide a number of opportunities for students to develop their mastery of the subject throughout the course through ungraded course assignments. Homework will be assigned at the end of each class period as recorded in the on-line class schedule. Homework assignments should always be completed as if they were to be turned in and added to the student portfolio. Students are encouraged to work on homework problems in collaborative groups.

Each student is expected to keep a portfolio of course material. This portfolio should consist of a 3-ring binder containing returned examinations, lecture and textbook notes, homework assignments, documented excuses for absences, and other course material. Your *course portfolio* (in conjunction with your lab notebook) is the physical representation of your course effort and may be a factor in determining "border-line" grades; take care not to misplace it!

Students who follow the majority of the lecture material during class, complete the assigned readings and homework problems in full, and ask questions when confused will be well prepared to get a B on examinations. Exceptional students who, additionally, prepare for lectures by reading ahead, come to lectures with points of confusion identified in advance, spend time discussing class topics in small groups, and actively seek the answers to these questions both in lecture, via email, and during office hours are the most likely to achieve an A on examinations and in the course.

Academic Integrity : Student-teacher relationships are built on trust. For example, students must trust that teachers have made appropriate decisions about the structure and content of the courses that they teach, and teachers must trust that the assignments which students turn in are their own. Acts which undermine this trust undermine the educational process. It is the policy of Wright State University to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and truth. Furthermore, it is the policy of the university to enforce these standards. The following recommendations are made for students:

1. Be honest at all times.
2. Act fairly towards others. For example, do not seek an unfair advantage over others by cheating with or by looking at other individual's work during examinations or laboratory assignments.
3. Take group as well as individual responsibility for honorable behavior. Collectively, as well as individually, make every effort to prevent and avoid academic misconduct, and reports acts of misconduct that you witness.
4. Know the policy -- ignorance is no defense. Read the policy contained in the student handbook. If you have any questions regarding academic misconduct, contact your instructor.

Students are encouraged to get together in small study groups to discuss the course topics and homework problems. Small group discussion and collaboration is a vital aid to mastering the concepts presented in this course. Modern designs are rarely the work of a single engineer! Being able to communicate and work in teams is a necessary skill for any computer engineer. However, **students must work on all graded course assignments and examinations on an individual basis.**

Conduct for Laboratory Assignments: Students may discuss "general concepts" of laboratories assignments with each other, but may not, under any circumstances, work with anyone on their actual implementation. If you work with other student on "general concepts" be certain to acknowledge the collaboration and its extent in the assignment. Unacknowledged collaboration will be considered dishonest. Sharing (or copying) schematics or datafiles (including work from previous quarters) is strictly disallowed. If the same work is turned in by two or more students I will consider all students involved equally culpable. *You are responsible for ensuring that other students do not have access to your work* - do not give another student access to your account, do not leave printouts in the recycling

bin, pick up your printouts promptly, do not leave your workstation unattended, etc. If you suspect that your work has been compromised notify your instructor immediately.

Conduct for Examinations: The academic code demands that no student should have an unfair advantage over any other student during examinations. Thus, it is strictly forbidden for any student to refer to information from previous offerings of this course unless this information is provided by the instructor to all students fairly. Thus, the use of test banks of previous quizzes or asking questions about examinations or laboratory assignments to prior students is strictly forbidden.

Absences: Class attendance will not be a direct factor in your grade but will strongly effect the quality of your education. Students are expected to attend every class. Things may make less sense to students that do not attend class or arrive late. Students who miss class are responsible for the material or announcements presented. Any extenuating circumstances which impact on your participation in the course should be discussed with me as soon as those circumstances are known. Make-ups for laboratory demonstrates may be arranged if a student's absence is caused by documented illness or personal emergency. It is the student's responsibility to provide a written explanation (including supporting evidence) to the instructor in a timely manner. Students registering after the term begins are responsible for all missed assignments and cannot expect that due dates will be altered.

Additional Information: Copies of the transparencies used in lecture, supplementary textbooks, and additional course-related information are available in the laboratory for student reference. Information regarding assigned course readings, homework, and syllabus updates will be available via course web page. Students are responsible for reading this material on a weekly basis. Students that do not have active computer accounts or are otherwise unable to access the course WWW page should contact me.

Newsgroup: A newsgroup, wright.ceg.360, is maintained for the current students in this course. The newsgroup is used by the instructor and laboratory instructor to make class announcements as well as by students to arrange study groups, discuss homework problems, bring up class related issues, etc. The newsgroup is an open forum, anyone may ask/answer any questions posed to the group. All students should check the newsgroup on a weekly basis.

Additional Needs: Students with disabilities or any additional needs are encouraged to set up an appointment at their convenience to discuss any classroom accommodations that may be necessary.

CEG 360/560 - EE 451/651 Web Page: <http://www.wright.edu/~travis.doom/courses/CEG360>

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Wright State University
 College of Engineering and Computer Science
 Department of Computer Science and Engineering

Digital System Design

CEG 360/560 - EE 451/651

Fall Quarter, 2004

Section I: Digital System Analysis and Review		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 9/7	Class overview, review of combinational digital devices, and bistable elements	Review: Mano, Ch. 1-3, (Givone, Ch. 1-5) Prepare for entrance survey (ungraded quiz); Lab #0
R 9/9	Entrance survey and completion of combinational review	Review: Mano, Ch. 1-3, (Givone, Ch. 1-5); Lab #0
T 9/14	Review of sequential devices, clocked synchronous state machines, characteristic equations, timing	Read: Mano, Ch. 4.0-4.3, (Givone, Ch. 6.1-6.6); Problems: Mano, Ch. 4: 2, 3, 6, 7, 10, 14, 27; Lab #1a
R 9/16	CSSM analysis, input/excitation equations, state tables, CSSM models, state diagrams, CSSM timing	Read: Mano, Ch. 4.4-4.7, (Givone, Ch. 7.1-7.2); Problems: Mano, Ch. 4: 11-13, 15-18; Study for Half-hour Exam #1; Lab #1a
T 9/28	Half-hour Exam #1	Refer to next section

Section II: Digital System Design and Synthesis		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 9/21	Translating a design into a state diagram	Read: Mano, Ch. 4.5-4.7, (Givone, Ch. 7.2); Problems: as assigned in class; Lab #1b
R 9/23	Designing with state diagrams, implementing a design with D-type or JK-type flip-flops	Read: Mano, Ch. 4.5-4.7, (Givone, Ch. 7.3); Problems: Mano, Ch. 4: 19-21,23; Lab #1b
T 9/28	State minimization and assignment in CSSM design	Read: Ch 7.4-7.5 (Mano, Ch. 4); Problems: (Mano, Ch. 4: 34); Lab #2a
R 9/30	Muxes as next-state generators, ad-hoc design, finite memory machines, hierarchical	Read: Class Notes; Problems: as assigned in class;

	design/testing.	Study for Half-hour Exam #2; Lab #2a
T 10/12	Half-hour Exam #2	Refer to next section

Section III: Design with MSI, LSI, and VLSI Devices		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 10/5	Shift registers and their applications	Read: Mano, Ch. 5, (Givone, Ch 6.7); Problems: Mano, Ch. 5: 3, 5, 6, 8, 11; Lab #2b
R 10/7	Counters and their applications, ASM charts, designing with ASM charts, designing with ASM charts, transition lists	Read: Mano, Ch 5, 8.2-4, (Givone, Ch. 6.8, 8.1-8.2); Problems: Mano, Ch. 5: 10, 12, 13, 14, 16, 19, 22, 28 Ch. 8: 1-10; Lab #2b
T 10/12	LSI/VLSI Devices: ROM and other PLDs	Read: Mano, Ch. 6.5-6.8, (Givone, Ch. 5.7-5.10); Problems: Mano, Ch. 6: 11-13; Lab #3a
R 10/14	Static and Dynamic RAM: organization and application	Read: Mano, Ch. 6.0-6.4; Problems: Mano, Ch. 6: 1-3, 9-10; Study for Half-hour Exam #3; Lab #3a
T 10/26	Half-hour exam #3	Refer to next section

Section IV: Digital System Organization		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 10/19	Design decomposition: control and data, register transfers	Read: Mano, Ch. 7.0-7.5; Problems: Mano, Ch. 7: 1-6; Lab #3b
R 10/21	The datapath: micro-operations, control words, and pipelining	Read: Mano, Ch. 7.6-7.11; Problems: Mano, Ch. 7: 22, 27-30; Lab #3b
T 10/26	The control unit: design, hardwired vs. microprogrammed control, programmable control units, the machine cycle	Read: Mano, Ch. 8.0-8.5; Problems: Mano, Ch. 8: 1-8; Lab #4a
R 10/28	A simple computer architecture (lab 4)	Read: Mano, Ch. 8.6-8.10; Problems: Mano, Ch 8: 30-32, 34, 39, 43-44; Lab #4a
T 11/2	ISA design: CISC vs. RISC, data and control hazards; Contemporary microcomputer architecture	Read: Mano, Ch. 8.11, 9.1, 9.4, 10.3; Problems: None; Study for Half-hour Exam #4; Lab #4b
R 1/4	Half-hour exam #4; Instructor evaluation; Exit survey	Study for final examination; Lab #4c

Final Examination		
DATE	TOPIC / ACTIVITY	ASSIGNMENT/LOCATION
T 11/9	Class review	Study for final examination; Lab #4c
M 11/15	Administrative Deadline: Labs Due.	No late labs will be accepted after this date
T 11/16	Section 01: Final examination	1:00-3:00 PM; regularly scheduled classroom
R 11/18	Section 03: Final examination	3:15-5:15; regularly scheduled classroom

This page was last modified on Monday, 23-Aug-2004 15:03:06 EDT. Assignments prior to this date should be accurate. Assignments listed after this date are *projections* and may not correspond to the actual material and assignments presented in class.

The most recent version of this document is available on the world wide web via:
<http://www.wright.edu/~travis.doom/courses/CEG360>

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