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DESIGN AND PERFORMANCE ANALYSIS OF MAGNETIC ADDER AND 16-BIT MRAM USING MAGNETIC TUNNEL JUNCTION TRANSISTOR

A thesis submitted in partial fulfilment
of the requirements for the degree of
Master of Science in Electrical Engineering

By

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2015
Wright State University

WRIGHT STATE UNIVERSITY
SCHOOL OF GRADUATE STUDIES

MAY 28, 2015

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Surya Kiran Akkaladevi ENTITLE "Design and Performance Analysis of Magnetic Adder and 16-bit MRAM Using Magnetic Tunnel Junction Transistor" BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering.

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Abstract

Akkaladevi, Surya Kiran. M.S.Egr, Department of Electrical Engineering, Wright State University, 2015. Design and Performance Analysis of Magnetic Adder and 16-bit MRAM Using Magnetic Tunnel Junction Transistor.

The scaling down of IC's based on CMOS technology faces significant challenges due to technology advancing factors. The stand-by power becomes comparable to active power due to the increasing leakage current. Power gating and various low-power schemes have been proposed in the past to reduce the stand-by power in CMOS designs. As most random access memory (RAM) used for primary storage in personal computers is volatile memory, which needs constant voltage (power on) to store the data and results in a higher stand-by power. Magnetic Tunnel Junctions (MTJ) transistor has feature of non-volatility, endurance and high density, which makes it possible for next-generation logic and memory chips that do not need to have its memory content periodically refreshed. This thesis discusses design and performance analysis of magnetic logic gates, adders and memories using MTJs. Ultra-low stand-by power and dynamic power are observed and presented using MTJs.

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1 INTRODUCTION

1.1 Overview

The exponential growth of semiconductor logic and memory devices over the past few decades has been driven by the fast scaling of CMOS technology. This has permitted PCs to progress from being moved with forklifts to gadgets that can be conveyed effectively in your pocket. On the other hand, the developmental CMOS scaling has resulted in physical constraints and will probably get to be very difficult at and beyond the 22-nm hub. As the physical gate length of CMOS device is getting closer to the physical constraints, numerous short channel effects emerges, bringing about high device leakage and performance instability, which enormously decay the energy efficiency and usefulness of CMOS circuits.

Thus the scaling down of device size will not be the solution for increasing computational power (see Fig. 1.1), but innovative switches (transistors) which includes new physics like spin-based computing/Spintronics [1], bimolecular/DNA computing [2] and Organics computing [3] are among the candidates for these goals.

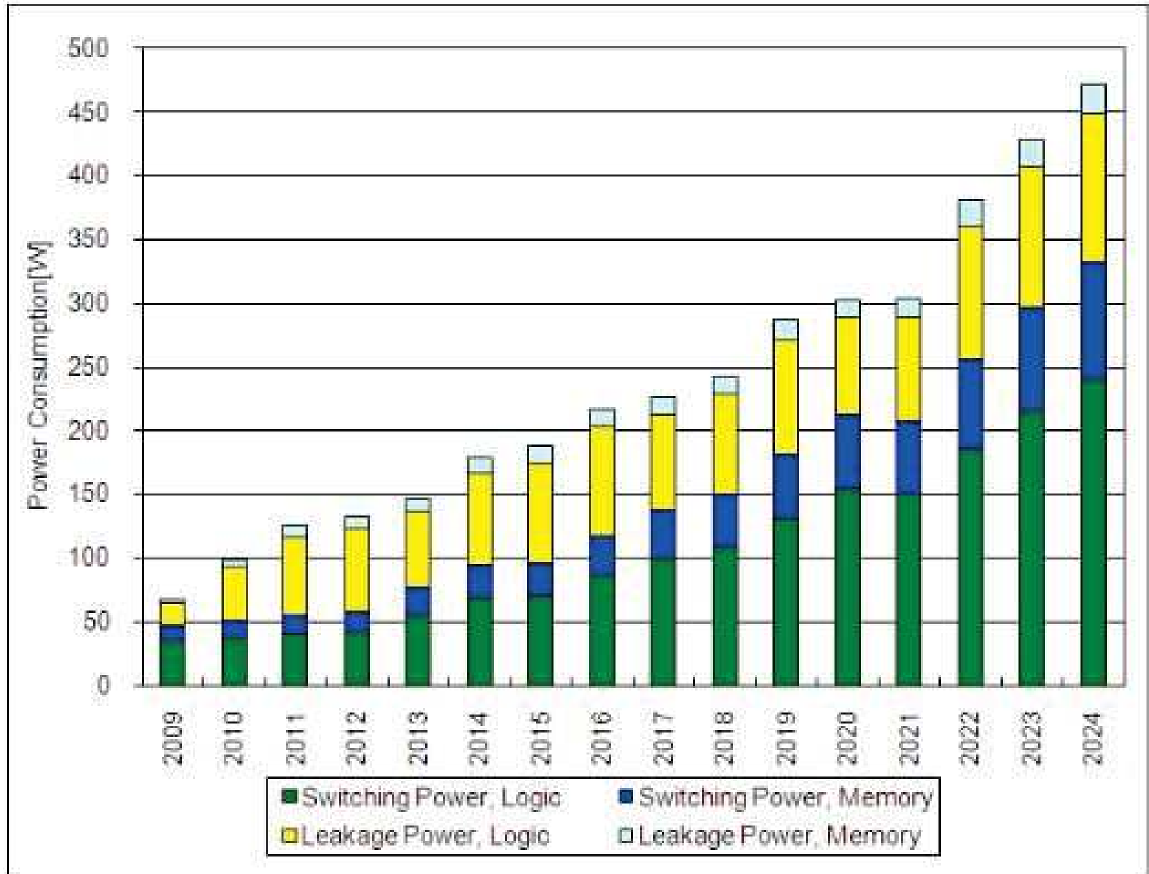

Figure 1.1: SOC consumer stationary power consumption trends

Some of the major factors that will determine the success or failure of these new computing devices will be energy consumption and added new functionality to an existing technology. Figure 1.2, illustrates this concept, which allows the need of research and development to promote, market growth for integrated circuits while they design and replace the standard applications such as SRAM, DRAM and CPU. The concept of this innovative physics in these specialized markets is referred as "Moore's Law and more" [4]. In the last decade, both academic and industrial institutions invested great effort in this emerging field, which resulted new logic and memory devices such as MRAM, Magnetic Logic devices. Fig. 1.3 represents, one such innovative design based on spin-based computing/Spintronics called Magnetic Tunnel Junction (MTJ).

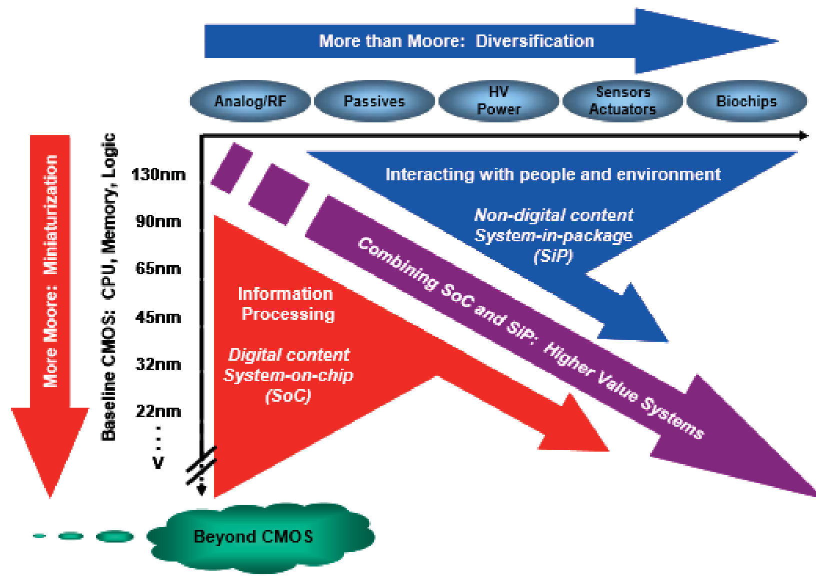

Figure 1.2: Illustration of the need for innovative devices referred as moore's law and more [4]

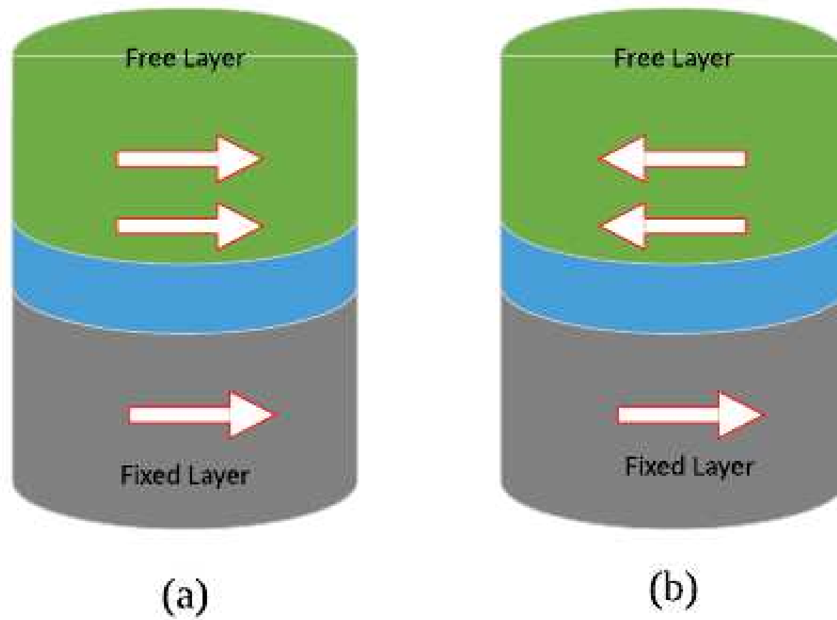

Figure 1.3: Structure of Magnetic Tunnel Junction illustrating two resistive states, (a) R_P and (b) R_{AP}

1.2 Spintronics

Spintronics is an emerging technology, which brings in a new degree of freedom by using both charge and a spin of electrons in solid to achieve devices with new capabilities [5]. Even though we cannot control and observe the individual spins of electrons, we still can control the spin of a group of electrons and observe its effects. This brings to study design structures of MTJ working on the principle of spin transfer torque. The concept of spintronics is closed to the phenomenon called as magnetoresistance (MR), which is generally an effective change of resistance based on the relative orientation of the two ferromagnetic layers.

Albert Fert and Peter Grunberg [6] observed firstly the giant magnetoresistance (GMR) effect in thin film structures made out of Fe/Cr/Fe multilayers in 1988, which is considered as conception of spintronics. Foundations of the spintronics can be followed back into the early works of spin transport phenomena, scattering, tunneling or injection would sit on the front line. Conventional electronic devices utilize just the charge of the electrons as the transporter of the data, in classical semiconductors as in silicon, the spin direction of the electron is random, and thus the spin polarization is zero. Actually, electrons have two spin states spin-up and spin-down, which are normally found in paired electrons, for Spintronics devices, spin polarization is characterized as the difference in the number of the spin-up and spin-down electrons that add to the electrical transport with respect to the total amount of conducting electrons.

1.3 Magnetic Tunnel Junction (MTJ)

MR devices, TMR or MTJ is one of the most promising Spintronics devices and applied as the basic memory cell in MRAM and magnetic logic development; it is a non-volatile ferromagnetic device, which is formed by sandwiching of two ferromagnetic material layers with a fixed layer pinned to constant direction with other pointing bi-directional free layer/storage layer, as depicted in Figure 1.3. These ferromagnetic layers are separated by thin non-magnetic insulating material. The insulating material is so thin that electrons can travel through it by tunneling. The spin polarization in the pinned layer and storage layer is in the same or opposite direction. The configuration of the MTJ stack can be switched simply by altering the spin magnetization direction of the storage layer, which may be induced by the magnetic field with opposite direction and superior than the threshold value.

In 1975, Julliere observed firstly that the resistance value of the MTJ stack in different as it is in two configurations known as parallel or anti-parallel and named this effect as tunnel magnetoresistance (TMR). The TMR ratio is defined as given Eq. (1).

$$TMR = \frac{R_{AP} - R_P}{R_{AP}} \tag{1.1}$$

The thin oxide barrier between the two ferromagnetic layers make MTJ stack change present resistance value compatible with CMOS transistor technology, which permits CMOS based sense amplifier to read the condition of MTJ stack. A high resistance termed as logic “1” is known as anti-parallel state, whereas a low resistance termed as logic “0” is known as parallel state. In order to avoid disturbance of mismatch and parameter variation in CMOS process and reduce the die area of

the amplification circuits, a high TMR value is preferred, which has been increased significantly in the last few years by using new ferromagnetic material in storage and pinned layers, new oxide barrier, and MTJ process.

1.4 Spin Transfer Torque (STT)

The real deterrent before the use of MTJ based memory or logic circuit is its switching technology, and some methodologies have been developed and exhibited in the most recent ten years. The primary exhibit of MRAM was acknowledged by IBM in 1996, and it is based on the field induced magnetic switching (FIMS), which requires two high currents to generate magnetic fields to switch the state of MTJ [7]. The intrinsic limitations like high power, large die and high noise make FIMS hard to be applied to high density and low power memory. Freescale developed a 4-Mb MRAM product in 2006 using toggle switching methodology based on the FIMS principle. It resolved the disturbance/noise issue, however, two required high switching currents limit its scalability. Two new methodologies were developed to reduce the switching currents so as to improve the density and power consumption. The first is thermally assisted switching (TAS), which utilizes likewise two currents for writing operation; one goes through and heats the MTJ, which subsequently cuts down the other for switching. The alternative switching methodology is based on spin transfer torque (STT), which uses only one low current going through the MTJ to switch its state. John Slonczewski at IBM firstly discovered this impact in 1996. STT switching is predicted as the most effective writing approach for MRAM and magnetic logic application till the date.

Figure 1.4 below, illustrates the STT switching approach, which demonstrates the two different states of MTJ. The state of the MTJ depends on the direction of current flow between the free and fixed layer. Writing current flowing from free

layer to fixed layer will store the logic "0" in the MTJ with the storage layer spin magnetization direction parallel to the pinned layer, whereas when current flows from the fixed layer to free layer it will store the logic "1" in the MTJ with the storage layer spin magnetization direction anti-parallel to that of the pinned layer resulting in high resistance of the MTJ. In order to change the resistance state or logic in MTJ, the writing current flowing through MTJ must be greater than the critical current density (J_c).

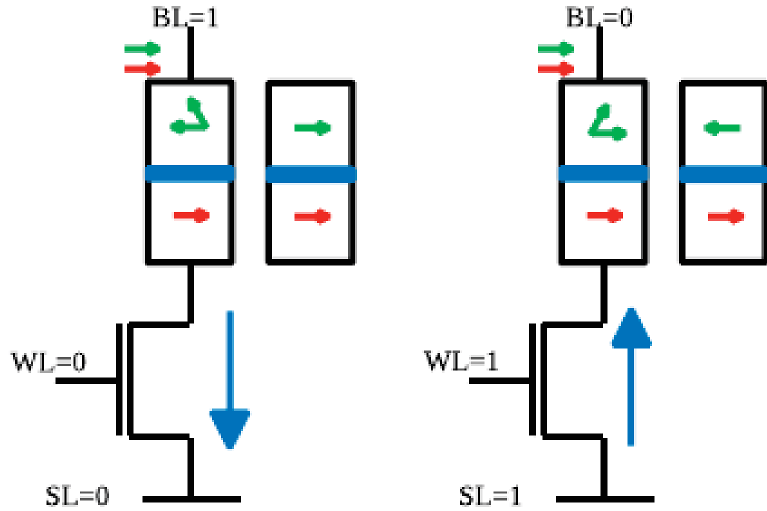

Figure 1.4: STT switching approach illustrating, (a) logic '0' or low resistance state and (b) logic '1' or high resistance state

1.5 Thesis Outline

The design and study of a full adder and magnetic random access memory (MRAM) using MTJ is focused through this research study. Magnetic full adders (1, 2 and 4 bit) using MTJ is designed and compared with the conventional CMOS full adders. A 16-bit MRAM using MTJ is designed and compared with 16-bit CMOS SRAM. In chapter 1, the functionality of MTJ by mentioning different switching

approaches used to switch the MTJ state is explained. Chapter 2 discusses device model files and simulation tools used in the design environment. Chapter 3 introduces "logic-in memory architecture" and discussed its application to switching circuit such as pre-charged sense amplifier (PCSA). MTJ/CMOS hybrid logic-in memory logic design is discussed and compared with the conventional CMOS pass transistor logic gates. Chapter 4 presents a magnetic full adder and its performance comparison with the conventional CMOS full adder. Carry look-ahead adders are introduced and discussed briefly. Chapter 5 introduces magnetoresistive random access memory (MRAM) design architecture. and its performance comparison with CMOS SRAM. Chapter 6 summarizes the contributions of this thesis and future work.

2 MTJ MODELS, DESIGN AND SIMULATION

Before demonstrating the "logic-in memory architecture" of magnetic logic device and memory it is important that we introduce you to the device models used through this work of research study. The design, architecture used in this work mainly rely on the spin-based computing element MTJ and the technology model of this element is described in further sections of this chapter.

2.1 Magnetic Logic Devices And MRAM

The main objective of this research is to design and simulate the transistor level magnetic full adder and MRAM using MTJ. Synopsys HSPICE simulator (version 2010) [8] and Waveview [9] are used to simulate and study the behavior of MTJ and its design. A 45-nm CMOS predictive technology models (PTM) [10] are used to integrate with MTJ models to create logic-in memory architectures. The MTJ model used throughout this research work is HSPICE macro model of MTJ [11] provided by the University of Minnesota.

2.2 45-nm PTM CMOS Model

Scaling down of IC's based on CMOS technology faces significant challenges due to technology advancing factors. Investigation of propelling circuit design must begin before future advancements are completely developed to illuminate difficulties postured by nanoscale CMOS technologies. To know these physical constraints, an intuitive approach is used to calculate the geometry and voltage parameters used for existing technology [12]. These PTM model files of n-MOS and p-MOS are developed and made available from Arizona State University. The n and p-MOS model files were designed and developed for a minimum supply voltage of 1.0 V and a minimum width of 54 nm with thickness of oxide of 1.1 nm.

2.3 MTJ Models

Spice models are essential to determine the characteristic and operation of the circuit. Many Spice models have been proposed for MTJ such as HSPICE, Verilog-A, MATLAB, etc. As previously declared, the MTJ model used throughout this research is MTJ macro model provided by the University of Minnesota [13]. Parameters of this macro model were changed in accordance to fit the MTJ model developed by Tohoku University. Despite the fact that this blending of technology is not perfect, the technologies are sufficiently good to guarantee solid conclusions on whether the proposed circuits would work on silicon and with what functionality. The macro model developed by the University of Minnesota depends on HSPICE behavioral sources to model the functionality of generic MTJ and this macro model can be customized further by changing initial data for process so as to meet the behavior of the MTJ macro model, which depends on the curve-fitting approach described in [13]. Parameters like initial critical currents for anti-parallel and parallel state (ICAP and ICP) and parallel and anti-parallel resistance (R_P and R_AP) are set to different

values which control device's behavior for different designs used. Other parameters which are used to process this macro model are kept at default.

The behavior STT-MTJ is complex to model as the switching probability depends on the current pulse duration by which this reliance of switching probability follows different rules depending on switching current is lower or higher than the critical current. Macro model used in the research and device properties are discussed below [13].

2.3.1 Hysteresis

MTJs are two-terminal current-controlled hysteresis devices. The resistance of an MTJ changes when adequately high currents go through the device. The MTJ can be in either the parallel or the antiparallel state. At the point when the current through the device surpasses the basic switching current, the condition of the device can be switched. The discriminating switching currents for the two distinct states won't generally be indistinguishable, and all in all, it is simpler to change from the antiparallel to the parallel state [14]. The antiparallel state will have a higher cell resistance than the parallel state.

2.3.2 Voltage Bias Versus Resistance

Fig. 2.1 (a) demonstrates that the device resistance drops with the increase in the applied voltage. This reliance can be approximated utilizing Gaussian capacity [15]. Fig. 2.1 (b) was measured with no offset, implying that write current was applied, however, the resistance was measured utilizing a small read pulse at every point after removing write current. In Fig. 2.1 (a), the resistance was measured amid write pulse and incorporates the bias voltage effect.

2.3.3 Critical Switching Current Versus Critical Switching Time

Critical Switching currents are associated with critical switching time and Fig. 2.1 (c) demonstrates the relationship between them for long pulses of writing time, that are approximated by the equation given below:

$$I_C = I_{c0}\left[1 - \frac{K_B}{E}\left(\ln\frac{t_p}{t_0}\right)\right] \quad (2.1)$$

where t_0 is set to 1ns, and I_{C0} is the critical switching current plotted to 1ns of pulse width. The thermal stability $\frac{E}{K_B T}$ can be derived by differentiation of I_C with respect to $\ln(\frac{t_p}{t_0})$ and describes the device resistance to random switching due to thermal energy.

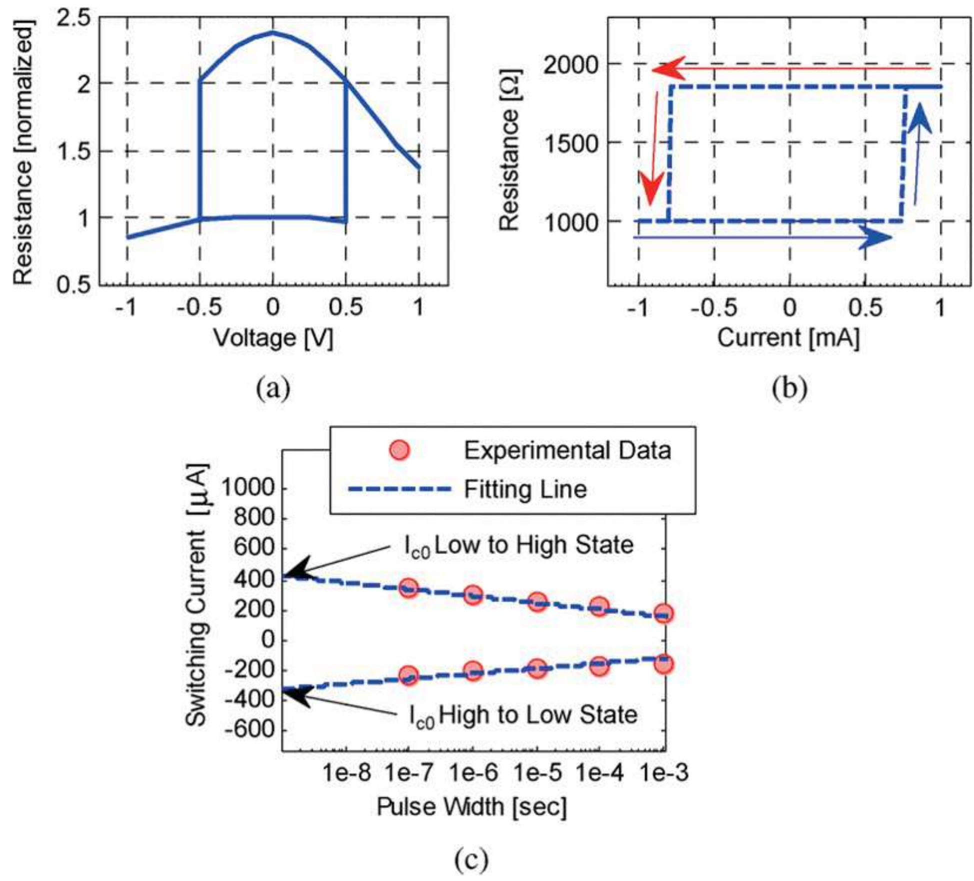

Figure 2.1: (a) Voltage versus resistance measured with bias voltage [21]. (b) Current versus resistance curve measured with no offset voltage [22]. (c) Critical write current versus critical switching time for long pulse width [23]. Image Curtesy of [13]

3 LOGIC-IN MEMORY ARCHITECTURE

3.1 Motivation

As mentioned earlier, scaling down of IC's based on CMOS technology faces significant challenges due to technology advancing factors. The stand-by power becomes comparable to active power due to the increasing leakage current. So we use power gating and various other schemes to reduce the stand-by power. Another challenge is interconnection delay, as we know, present architecture separates logic and memory unit and we need a long interconnect, signal bottleneck and power to charge and discharge those interconnects between these units within a processor. As memory units are volatile, which needs constant voltage to store the information even considering leakage currents. The following problems give rise to the need of logic-in memory architecture where the logic circuit is built based on the memory device. Magnetic tunnel junctions (MTJ) device has a feature of non-volatility, endurance, high density and compatible with CMOS, which makes it possible for next generation logic and memory chips. All these features of magnetic tunnel junction is capable to build hybrid architecture of CMOS/MTJ logic circuits and memories where the logic and memory are combined such that it brings non-volatility of MTJ to the design by which off-state leakage currents can be avoided.

3.2 Basic Structure Of Logic-in Memory Architecture

To design the hybrid MTJ/CMOS logic circuit we use logic-in-memory architecture [16]. MTJ is not suitable for direct logical output with integrated CMOS since it requires a sense amplifier to detect the state in it, so we use a pre-charged sense amplifier (PCSA) [17]. The basic block diagram hybrid MTJ/CMOS circuit is shown in Figure 3. The MTJ/CMOS block consists of PCSA, NMOS-transistor logic (Volatile logic) integrated with Non-Volatile MTJ logic.

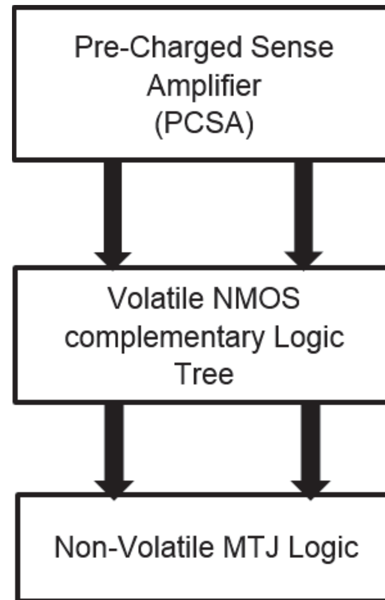

Figure 3.1: Basic block diagram of hybrid MTJ/CMOS circuit (Logic-in memory architecture) [17]

3.3 Pre-Charged Sense Amplifier (PCSA)

As noted earlier, MTJ device presents the resistive property compatible with CMOS transistors, which enables the sensing of the MTJs configurations with CMOS amplifier circuits. Fig. 3.2 presents a 7-transistor based pre-charged sense amplifier integrated with a two-MTJ complementary structure used in our login-in memory architecture, which operates in low power, high speed and a low surface. It consists of four P-MOS transistors (MP0 to MP3), three N-MOS transistors (MN0 to MN2) and two complementary MTJs connected with the configuration show in Figure 3.2. The two MTJs are configured in a complementary mode to present one logic-bit; if one MTJ has anti-parallel or high resistance then the other MTJ will be a parallel or low-resistance state. This sense amplifier works in two phase: pre-charge and evaluate. First, the complementary MTJs are pre-charged with logic "1" using a switching circuit when the clock input of sense-amplifier is set to logic "0" i.e., pre-charge phase. When the clock input in the sense amplifier changes to logic "1" i.e., evaluate phase, the outputs of the sense amplifier is complementary. As shown in Fig 3.3. the PCSA detects the two complementary outputs of MTJs resistance after a delay of 45 ps during evaluate phase. The N-MOS transistor MN0 acts as a sensing transistor, which senses the logic in the two complementary transistors and its width should be adjusted such that it senses logic values for both the MTJs. The switching circuit used in this design will be discussed in further sections of this thesis.

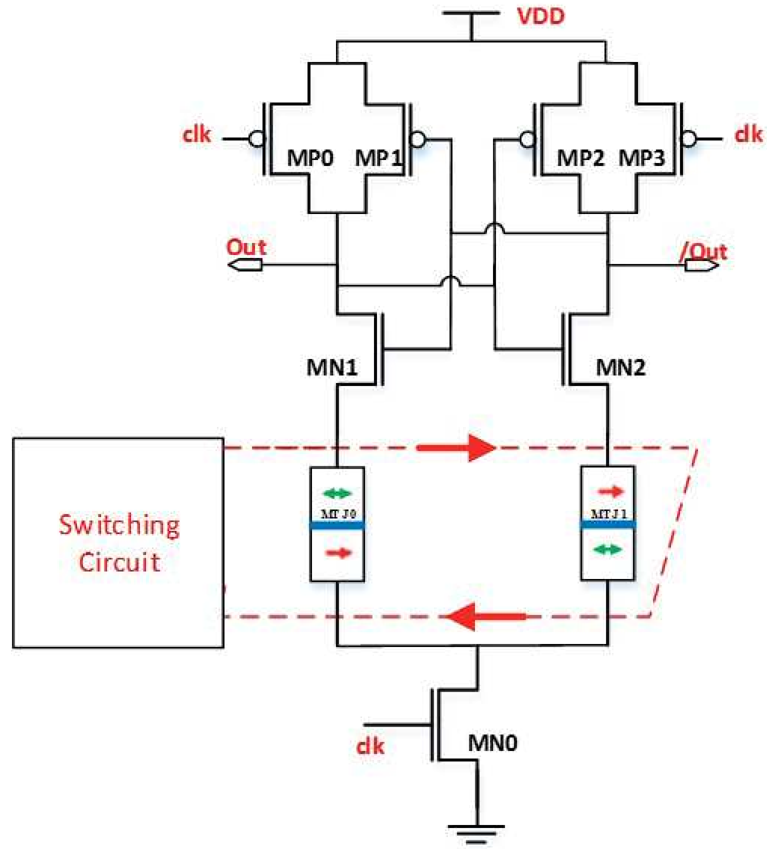

Figure 3.2: 7-Transistor based pre-charged sense amplifier [15]

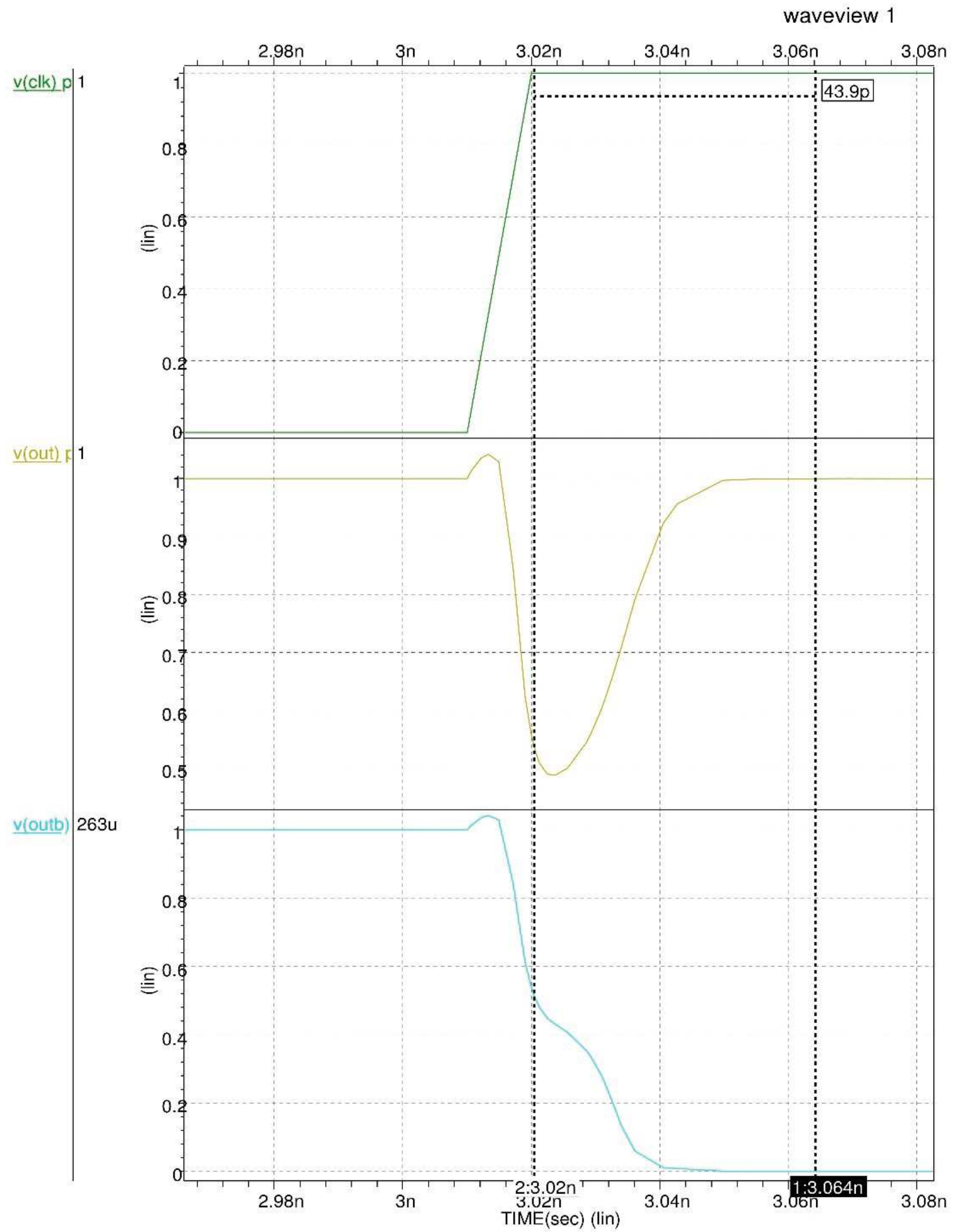

Figure 3.3: Simulation result of pre-charged sense amplifier using two complementary MTJs

3.4 Switching Circuit

A bi-directional current generator [15] is required in hybrid MTJ/CMOS logic designs to change the spin direction in the storage layer of MTJ device. The sense amplifier discussed above allows the reading circuit in low power and small area, and as a result the MTJ writing circuit dominates main power and surface of the whole hybrid MTJ/CMOS logic circuit. Since we are using STT writing approach a very low bidirectional current pulse is needed, which is less than 200 micro amps.

Fig. 3.4 represents the switching circuit used for generating bidirectional currents. It consists of two-NMOS and two-PMOS configured in a way that two of these four transistors are always closed.

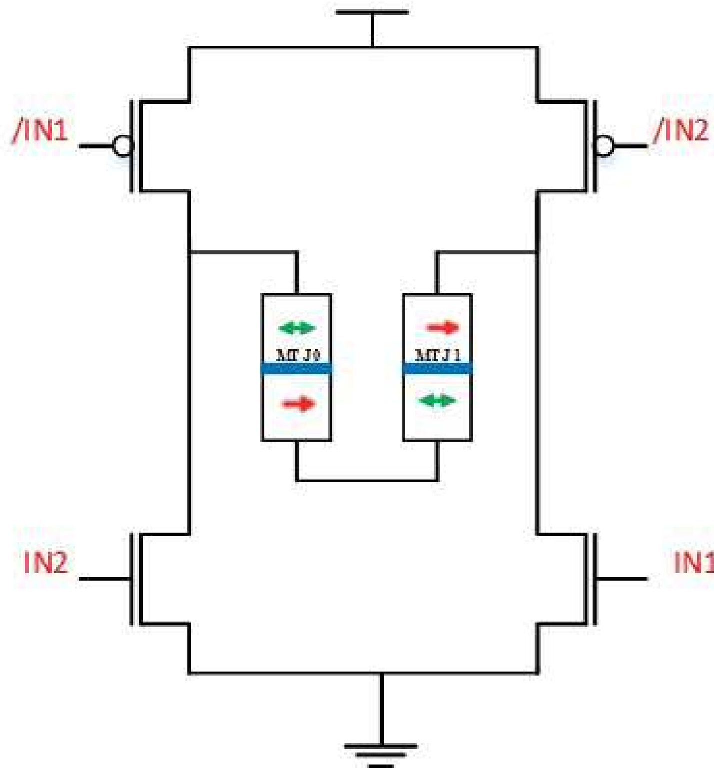

Figure 3.4: Switching circuit of MTJ producing bidirectional current [15]

3.5 Logic Circuit Design Using MTJ/CMOS Hybrid Architecture

There are two ways to design logic circuits using MTJs: one is discussed above, using hybrid CMOS/MTJ designs, whereas the other method is using the only MTJ device. As shown in Fig. 3.1 for hybrid MTJ/CMOS logic, we need a pre-charged sense amplifier integrated with complementary MTJ and NMOS logic.

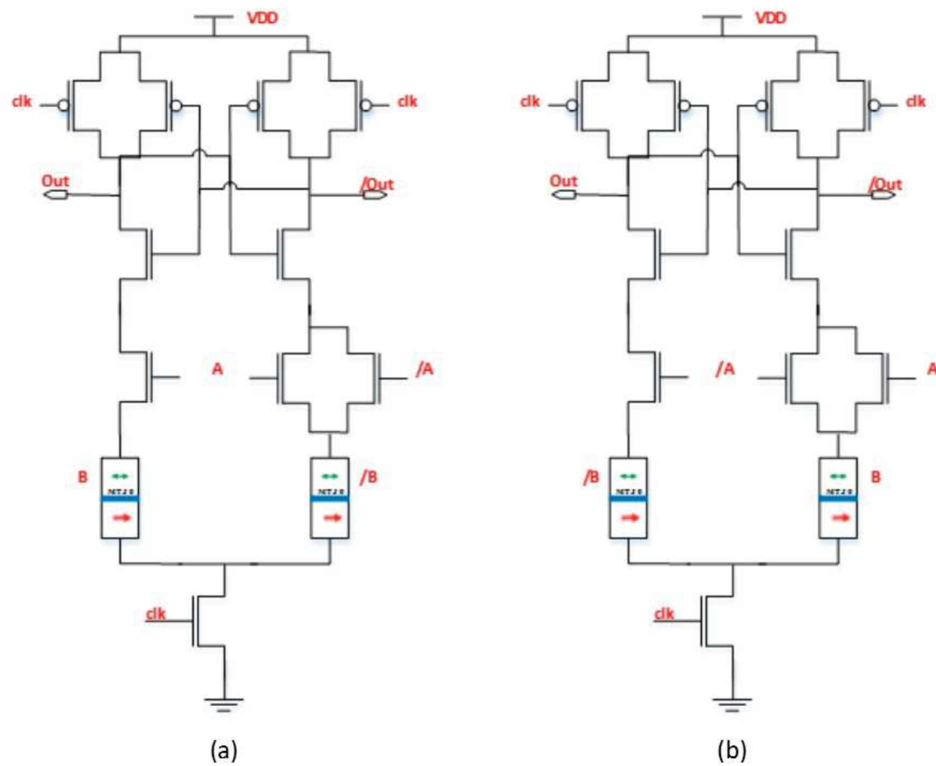

Figure 3.5: (a) 2-input NAND/AND gate and (b) 2-input NOR/OR gate using hybrid MTJ/CMOS logic

For instance, we demonstrate the basic two-input NAND/AND gate as shown in Fig. 3.5 (a). For this circuit, we have two outputs out and /out (or $\overline{out}$) which gives AND and NAND logic respectively. The AND logic is formed such that the NMOS with input A and MTJ with input B are connected in series such that output, $out = AB$, whereas, the other output is NAND from the series connections of NMOS and MTJ which has only $A\bar{B} + \bar{A}B$ Logic with $B\bar{A}$ and BA missing (all these three connections give the output logic '1' for NAND gate). As we can see, we cannot form these missing connections to the above circuit as the architecture does not allow us to do so. But still we get correct NAND logic by adjusting the widths of sensing NMOS transistors connecting the bottom electrodes of MTJs properly to sense the resistance of the two MTJ sub-branches. It is noteworthy that this missing connections has no impact on these logic. Table 3.1 exhibits the truth table for resistance configuration of NAND/AND logic. The resistance R_L and R_R are the two resistance of MOS transistors of two sub-branches of NMOS transistor with input A at the left and NMOS transistors connected in parallel with inputs 'A' and '/A' or '$\bar{A}$' at the right sub-branch of the circuit. Assuming that $R_{OFF} > R_{AP}$ the pre-charged sense amplifier sense the output accordingly. See Fig. 3.6 for simulation results of the hybrid MTJ/CMOS NAND/AND logic gate. By changing the parameters of the above circuit we can convert the NAND/AND gate to NOR/OR gate as shown in Fig. 3.5 (b) and the simulation results are shown in Fig. 3.7. These hybrid MTJ/CMOS NAND-AND and NOR-OR gate are compared to its equivalent conventional CMOS NAND/NOR gates illustrated in Fig. 3.8 and their simulation results are shown in Figs. 3.9 and 3.10 respectively.

Table 3.1: Resistance configuration of NAND/AND hybrid MTJ/CMOS circuit

A	B	Resistive Switching	out	sub-branch R_L	sub-branch R_R
0	0	$R_L < R_R$	1	R_{OFF}	$R_{OFF} + R_{ON}$
0	1	$R_L < R_R$	1	R_{OFF}	$R_{OFF} + R_{ON}$
1	0	$R_L < R_R$	1	R_{ON}	$R_{ON} + R_{OFF}$
1	1	$R_L > R_R$	0	R_{ON}	$R_{ON} + R_{OFF}$

Table 3.2: Resistance configuration of NOR/OR hybrid MTJ/CMOS circuit

A	B	Resistive Switching	out	sub-branch R_L	sub-branch R_R
0	0	$R_L > R_R$	0	R_{ON}	$R_{ON} + R_{OFF}$
0	1	$R_L > R_R$	1	R_{ON}	$R_{ON} + R_{OFF}$
1	0	$R_L > R_R$	1	R_{OFF}	$R_{OFF} + R_{ON}$
1	1	$R_L < R_R$	1	R_{OFF}	$R_{OFF} + R_{ON}$

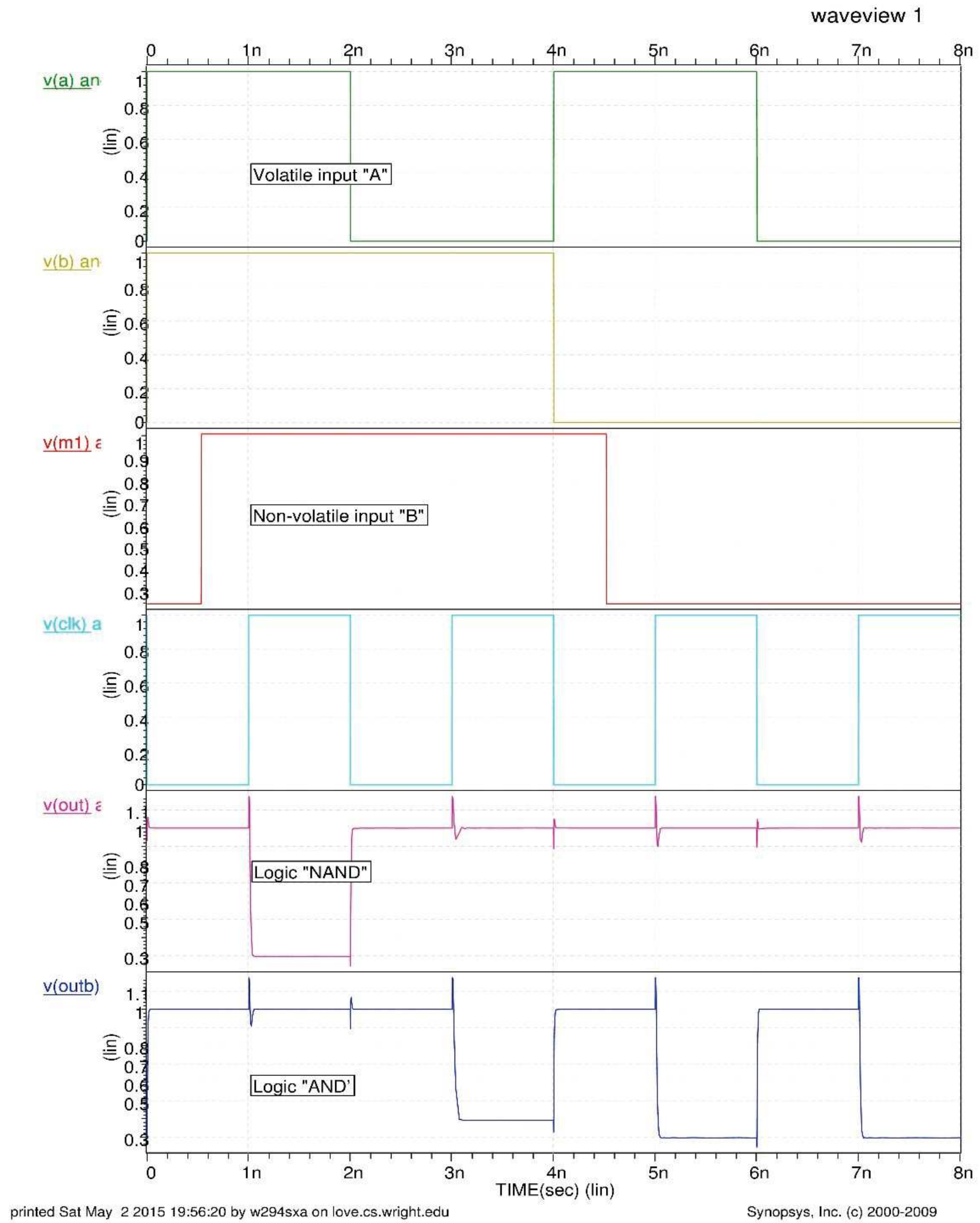

Figure 3.6: Simulation results NAND/AND logic gate operations using hybrid CMOS/MTJ

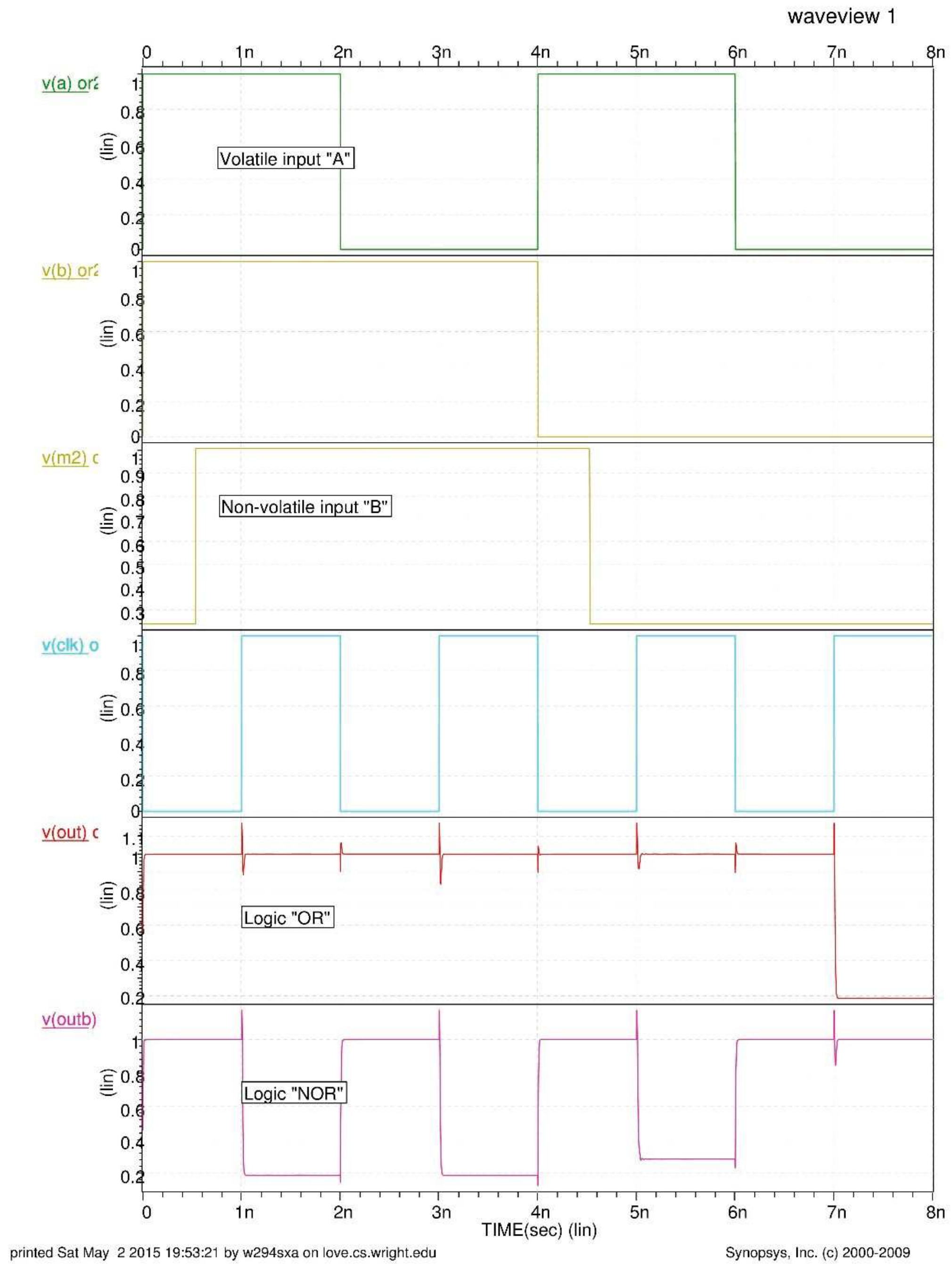

Figure 3.7: Simulation results NOR/OR logic gate operations using hybrid CMOS/MTJ

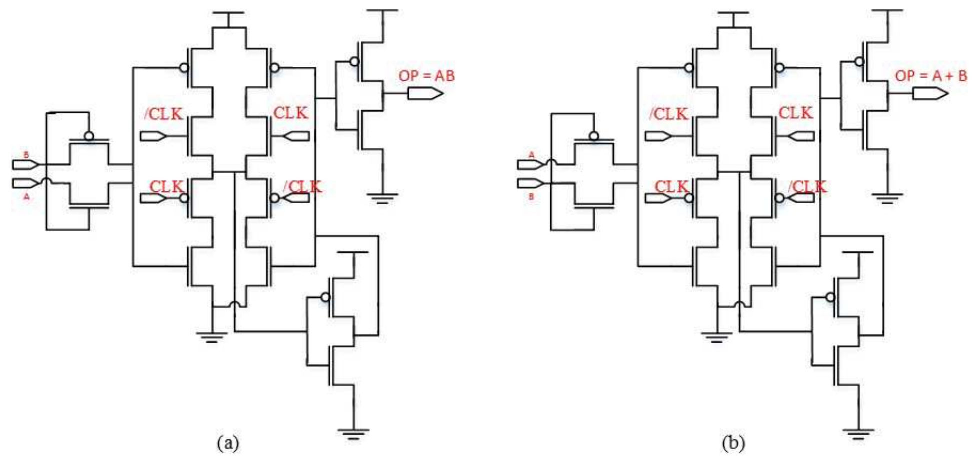

Figure 3.8: (a) 2-input NAND/AND gate and (b) 2-input NOR/OR gate using conventional pass transistor logic with synchronize outputs

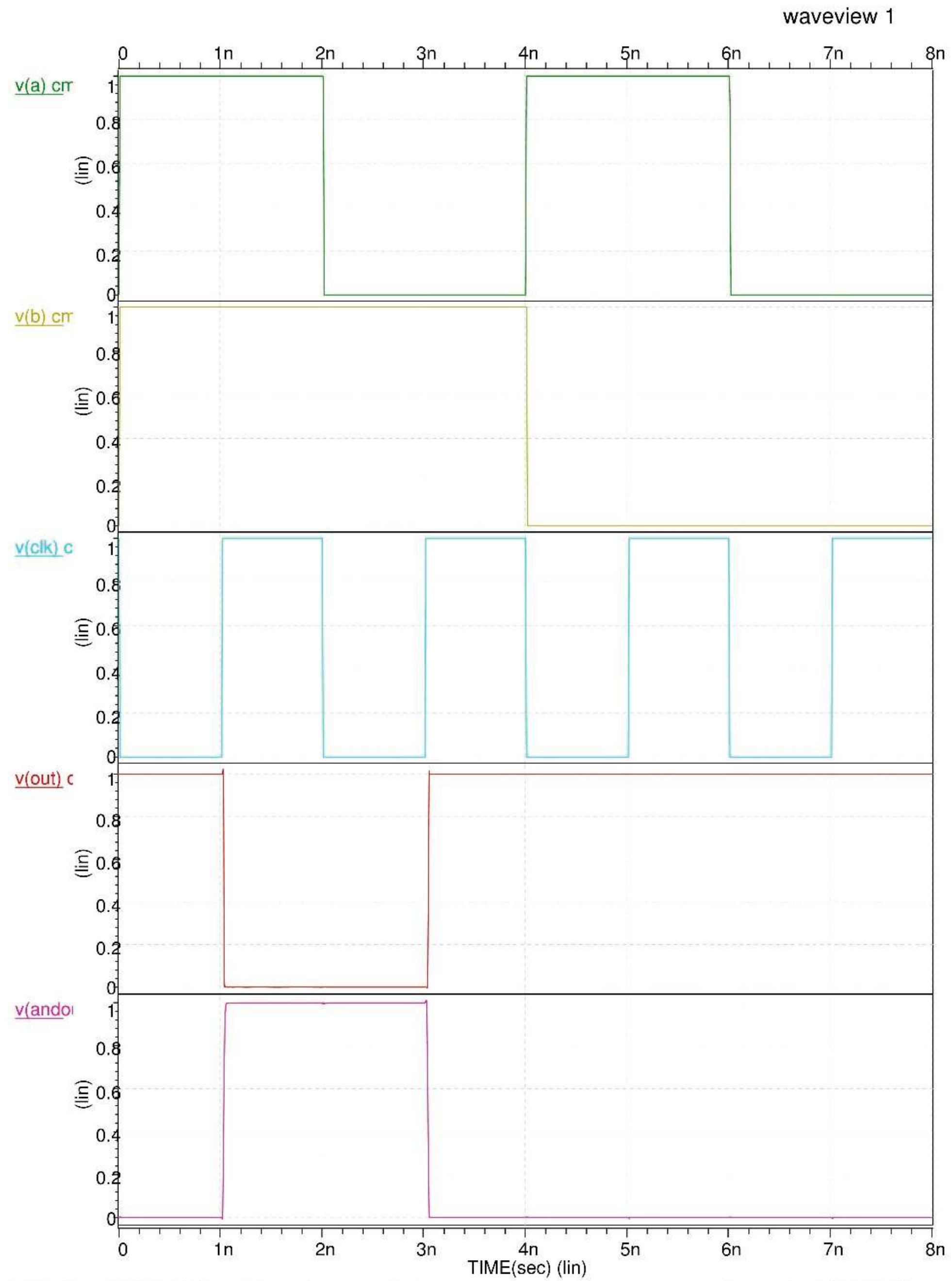

Figure 3.9: Simulation results NAND/AND logic gate operations using conventional CMOS with synchronized outputs

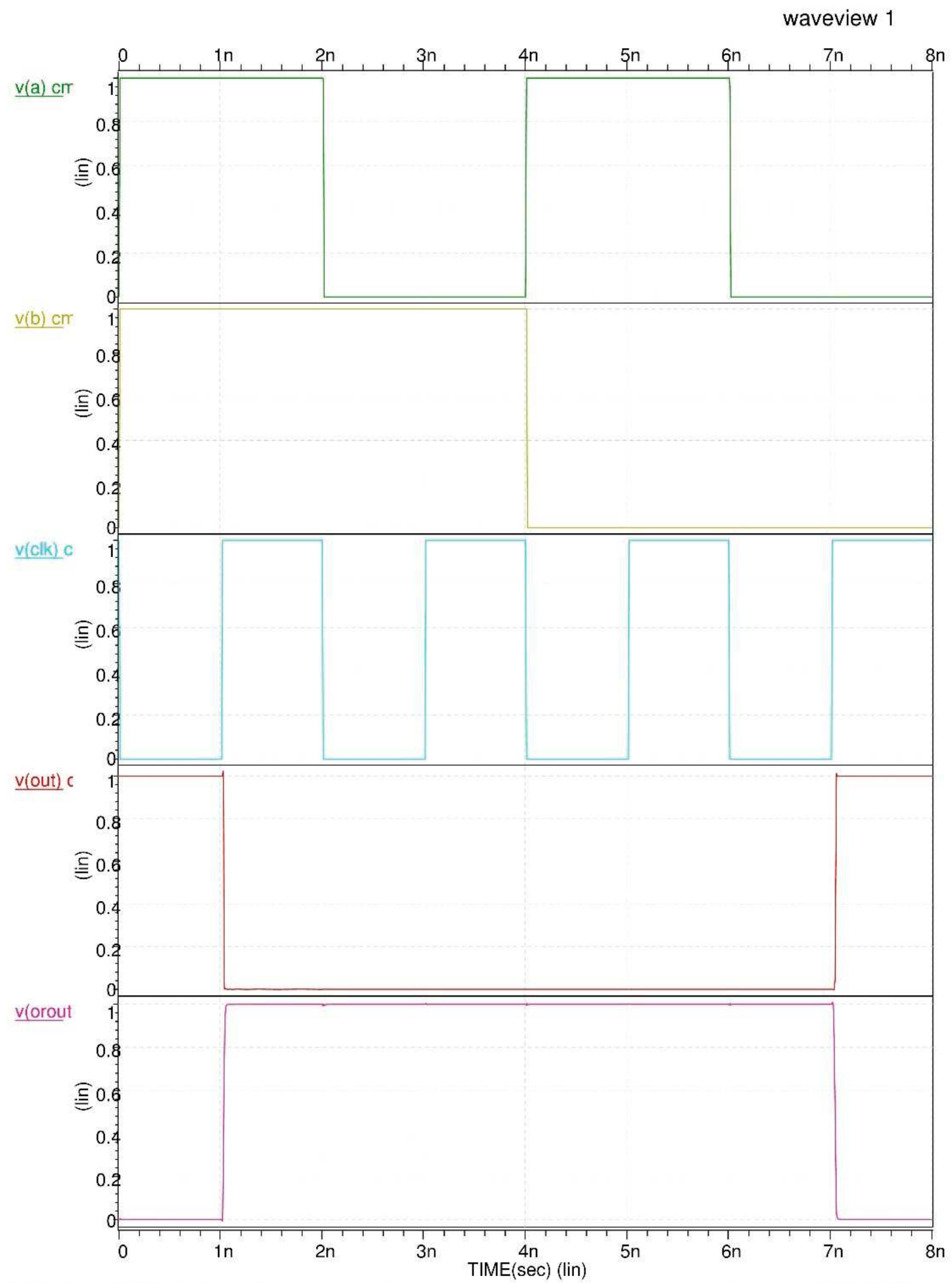

Figure 3.10: Simulation results NOR/OR logic gate operations using conventional CMOS with synchronized outputs

3.6 Performance Evaluation Of MTJ/CMOS Logic Circuit

Tables 3.3 and 3.4 below, illustrates the performance of these two types of logic design on different factors. The dynamic and leakage power consumed by the MTJ/CMOS based is far less than that of conventional CMOS circuits. The processing speed of these hybrid circuit is also very high than that of conventional CMOS.

Table 3.3: Performance evaluation of NAND/AND logic using CMOS/MTJ hybrid circuit design and conventional pass transistor logic design with synchronized outputs

Factors	NAND/AND logic using Conventional CMOS	NAND/AND logic using CMOS/MTJ hybrid circuit	Improvement
Dynamic Power	1.1 µW	0.4 µW	Consumes ≈ 74% less dynamic power
Propagation Delay	29 ps	22 ps	≈ 25% Faster
Stand-by Power	3 nW	50 pW	Consumes ≈ 98.5% less stand-by power

Table 3.4: Performance evaluation of NOR/OR logic using CMOS/MTJ hybrid circuit design and conventional pass transistor logic design with synchronized outputs

Factors	NOR/OR logic using Conventional CMOS	NOR/OR logic using CMOS/MTJ hybrid circuit	Improvement
Dynamic Power	1.9 µW	0.53 µW	Consumes ≈ 73% less power
Propagation Delay	25 ps	18 ps	≈ 28% Faster
Stand-by Power	2.75 nW	110 pW	Consumes ≈ 96% less power

4 LOW POWER HYBRID MTJ/CMOS ADDER

There are many applications for adder, which is considered as a building block in digital systems and micropressors [18]. It is also used in arithmetic operations as addition, multiplication,and etc.. As discussed earlier in the introduction the stand-by power and interconnect delay are important challenges for any CMOS based circuit. Both can be overcomed by using MTJ. In this chapter a low power hybrid MTJ/CMOS full adder [19] by integrating 45 nm CMOS with 50 nm MTJ is first designed and followed by designing 2-bit and 4-bit full adder using the 1-bit Hybrid MTJ/CMOS full adder. The performance of these designs is compared with the conventional CMOS full adder circuits.

4.1 1-Bit MTJ/CMOS Hybrid Adder (MFA)

To design hybrid MTJ/CMOS logic circuit we use the same logic-in-memory architecture [20] as mentioned earlier. Pre-Charge sense amplifier produces a bidirectional high speed output at every clock evaluation pulse. As shown in Fig 4.1 one bit magnetic full adder consists of a three-bit XOR gate which is designed according to the Eq. 4.2 and 4.3 for sum logic, whereas, the circuit is designed according to Eq. 4.4 and 4.5, for output carry logic. From this circuit we can note that the output carry logic consists of sub-branches "AC" and "$\overline{AC}$" that cannot be connected directly since they have no impact on the output by comparing inputs A and C. If these two inputs are different then these two sub-branches will have the same resistance, but

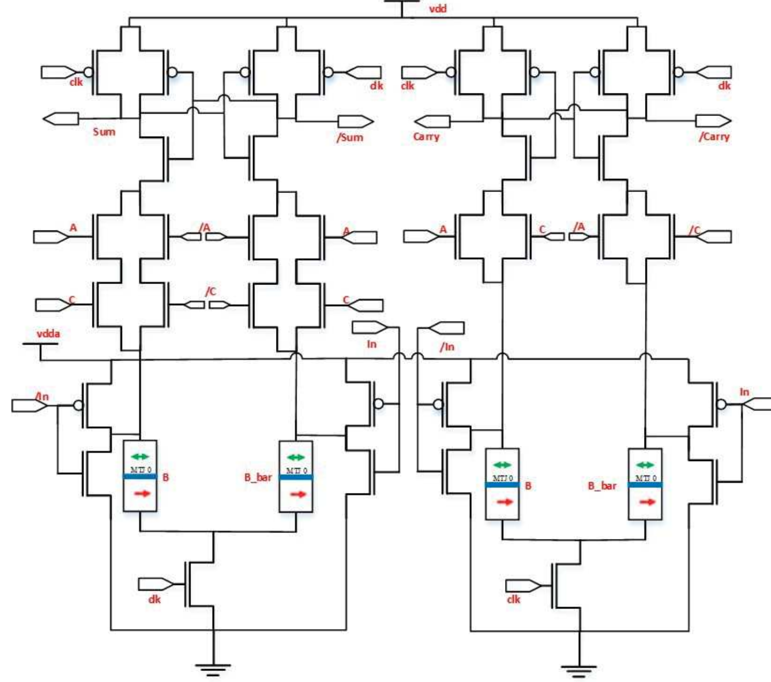

Figure 4.1: 1-bit hybrid MTJ/CMOS low power full adder [19]

if they are same we can note that there will be two different resistances in those sub-branches namely R_L and R_R in the condition that $R_{OFF} > R_{AP}$, which is true for STT-MRAM. Table 4.1 below, exhibits the resistance output carry logic function using resistive conditions.

$$SUM = A \oplus B \oplus C = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} \tag{4.1}$$

$$\overline{SUM} = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C} \tag{4.2}$$

$$C_{out} = AB + BC + CA \tag{4.3}$$

$$\overline{C_{out}} = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A} \tag{4.4}$$

The 1-bit hybrid MTJ/CMOS Magnetic full adder is compared with 1 bit pass gate based conventional CMOS full adder with synchronized output, shown in Fig. 4.2.

Table 4.1: Truth table and resistive configuration of output carry logic [19]

A	B	C	Resistance Comparison	C_{out}	Sum-branch AC	Sum-branch $\overline{AC}$
0	0	0	$R_L > R_R$	0	$2R_{OFF}$	
0	0	1	$R_L > R_R$	0	$R_{OFF} + R_{ON}$	$R_{ON} + R_{OFF}$
0	1	0	$R_L > R_R$	0	$2R_{OFF}$	$2R_{ON}$
0	1	1	$R_L < R_R$	1	$R_{OFF} + R_{ON}$	$R_{ON} + R_{OFF}$
1	0	0	$R_L > R_R$	0	$R_{ON} + R_{OFF}$	$R_{OFF} + R_{ON}$
1	0	1	$R_L < R_R$	1	$2R_{ON}$	$2R_{OFF}$
1	1	0	$R_L < R_R$	1	$R_{ON} + R_{OFF}$	$R_{OFF} + R_{ON}$
1	1	1	$R_L < R_R$	1	$2R_{ON}$	$2R_{OFF}$

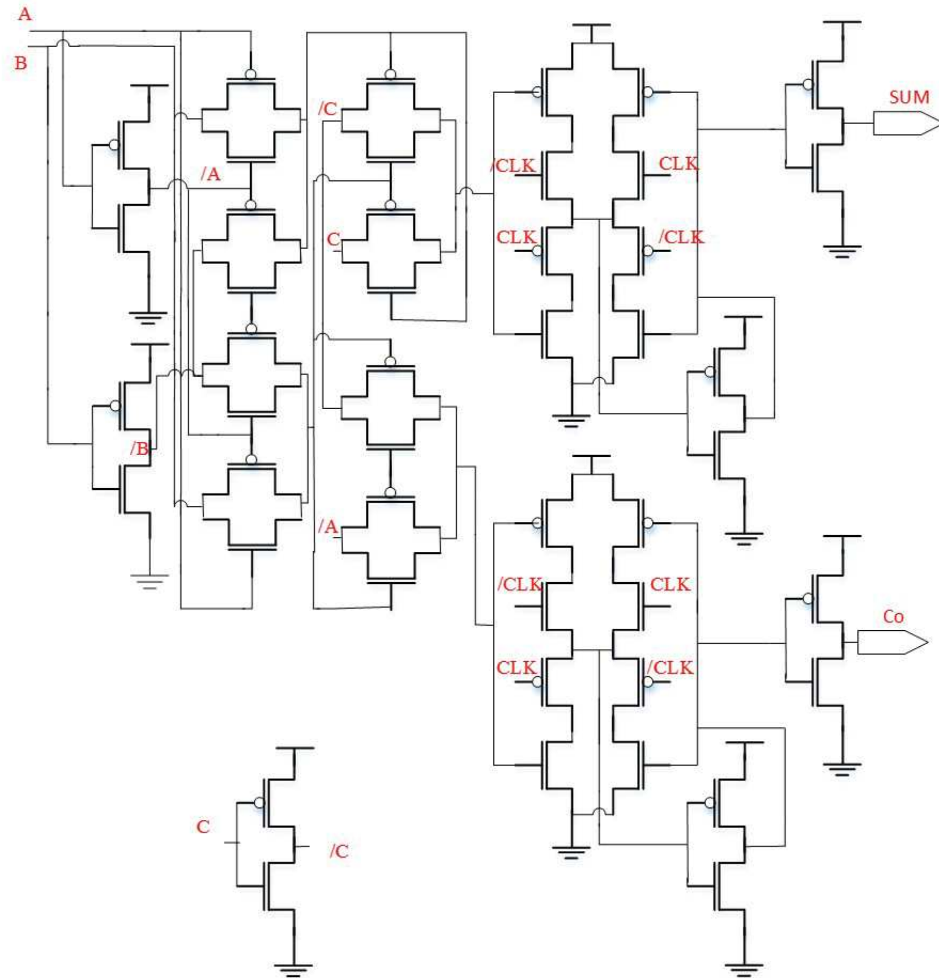

Figure 4.2: 1-bit pass gate based conventional CMOS full adder with synchronized output [19]

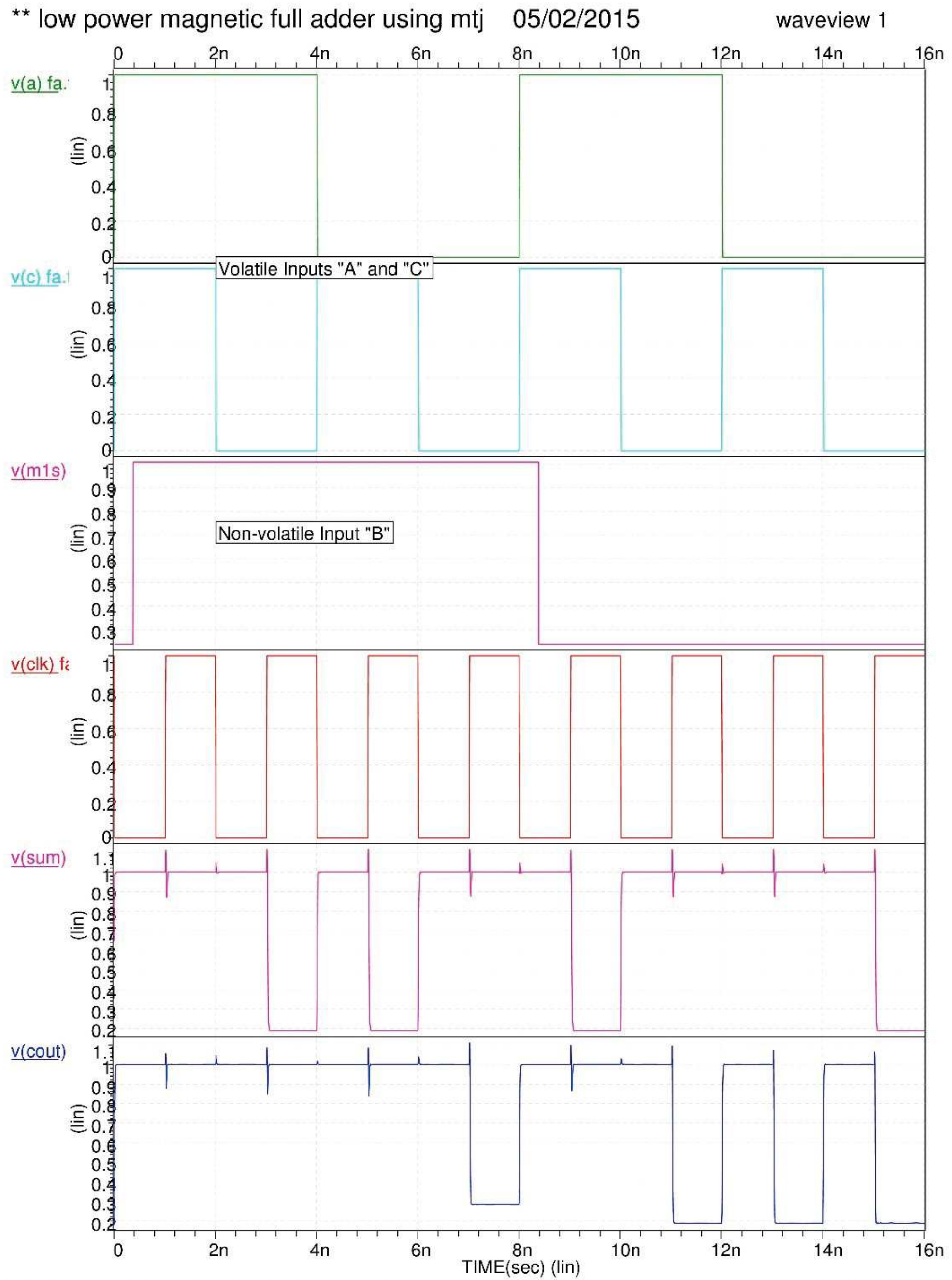

Figure 4.3: Simulation results of 1-bit magnetic full adder using logic-in memory architecture [19]

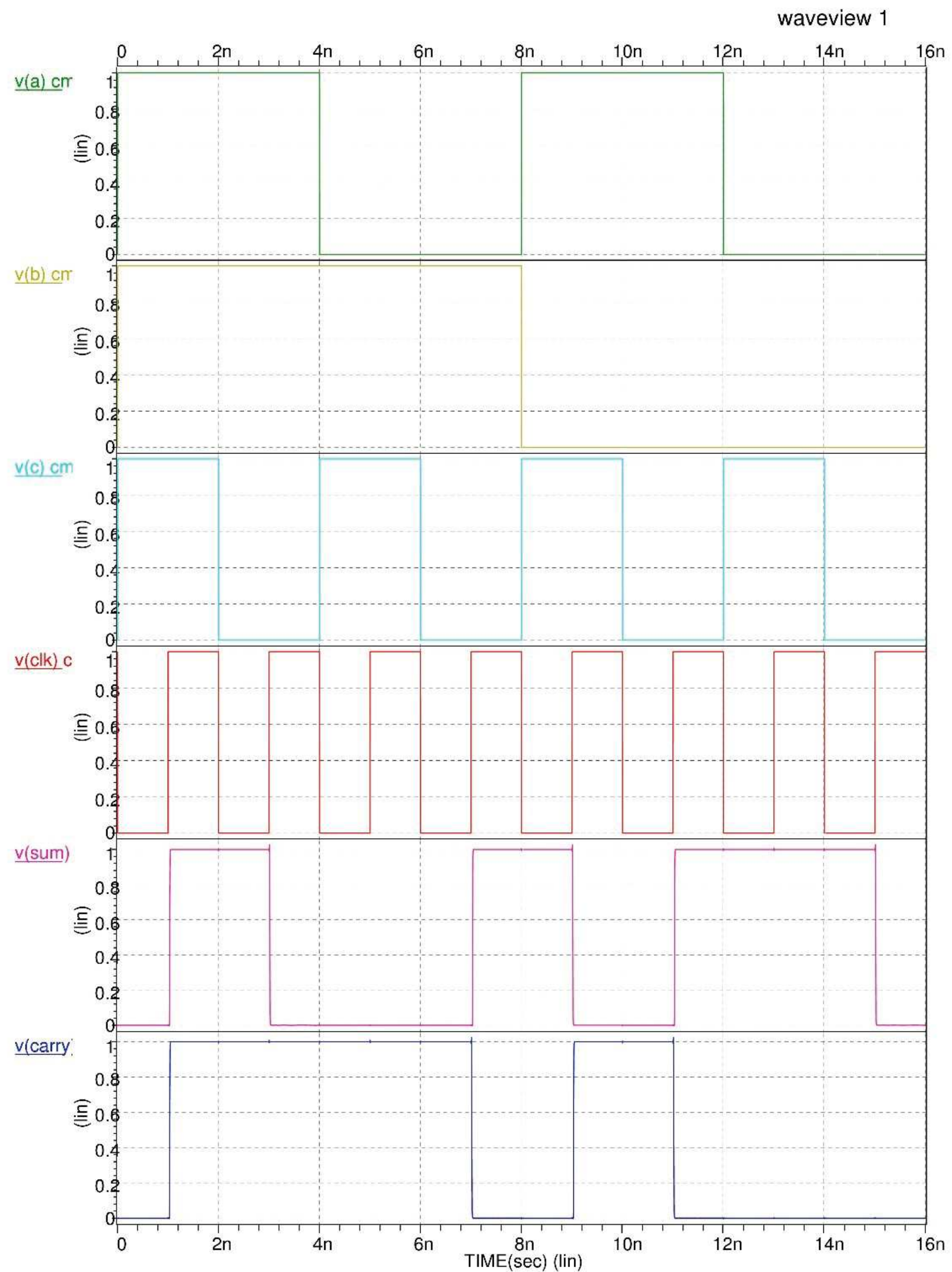

Figure 4.4: Simulation results of 1-bit pass gate conventional CMOS full adder with synchronized output

4.2 Two-Bit Carry Look Ahead MFA

Fig. 4.5 below, illustrates the 2-bit magnetic full adder. As shown in the figure, we can use two 1-bit full adder for designing this circuit. Since, the used one bit hybrid full adder is a synchronous circuit using a pre-charged sense amplifier producing bi-directional outputs, we can connect the output carry of first full adder directly to the second full adder as shown in the figure. The only problem here will be controlling the logical output carry circuit, as previously mentioned the carry circuit used here uses the resistive logic to control the output and it is necessary to set the sensing transistor widths so that the PCSA senses the logic correctly. Similarly 4-bit carry look ahead adder can be constructed. Figs. 4.6 and 4.7 below, illustrates the spice simulations of two bit carry look ahead magnetic and conventional adders respectively.

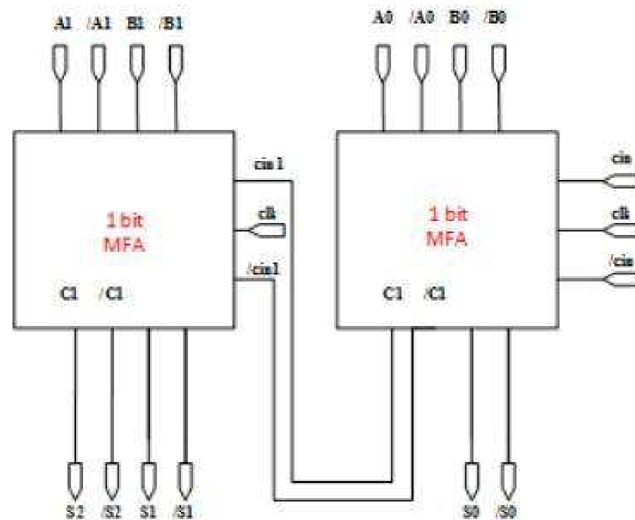

Figure 4.5: Circuit diagram of two-bit carry look ahead magnetic full adder

Table 4.2: Table illustrating the performance comparison of 1-bit magnetic and conventional full adder with synchronized outputs [19]

Factors	CMOS FA (45 nm CMOS)	MFA (45 nm MTJ and CMOS)	Improvement	MFA (40 nm MTJ and CMOS) Zhao[19]
Dynamic Power @ 500 MHz	9.25 µW	2.1 µW	Consumes ≈ 88% less dynamic power	1.98 µW
Sum Delay	39.15 ps	26.4 ps	-	-
C_out Delay	43.15 ps	37.8 ps	-	-
Propagation Delay	43.15 ps	37.8 ps	≈ 23% faster	26.4 ps
Stand-by Power	21 nW	23 pW	Consumes ≈ 99.99% less stand-by power	<1 nW

Table 4.3: Table illustrating the performance comparison of 1-bit magnetic and conventional full adder with synchronized outputs

Factors	2- bit CMOS FA (45 nm CMOS)	2-bit MFA (45 nm MTJ and CMOS)	Improvement
Dynamic Power @ 500 MHz	200 µW	17 µW	Consumes ≈91.5% less dynamic power
Propagation Delay	90 ps	59 ps	≈ 35% faster
Stand-by Power	1 µW	0.2 nW	Consumes ≈ 99.5% less stand-by power

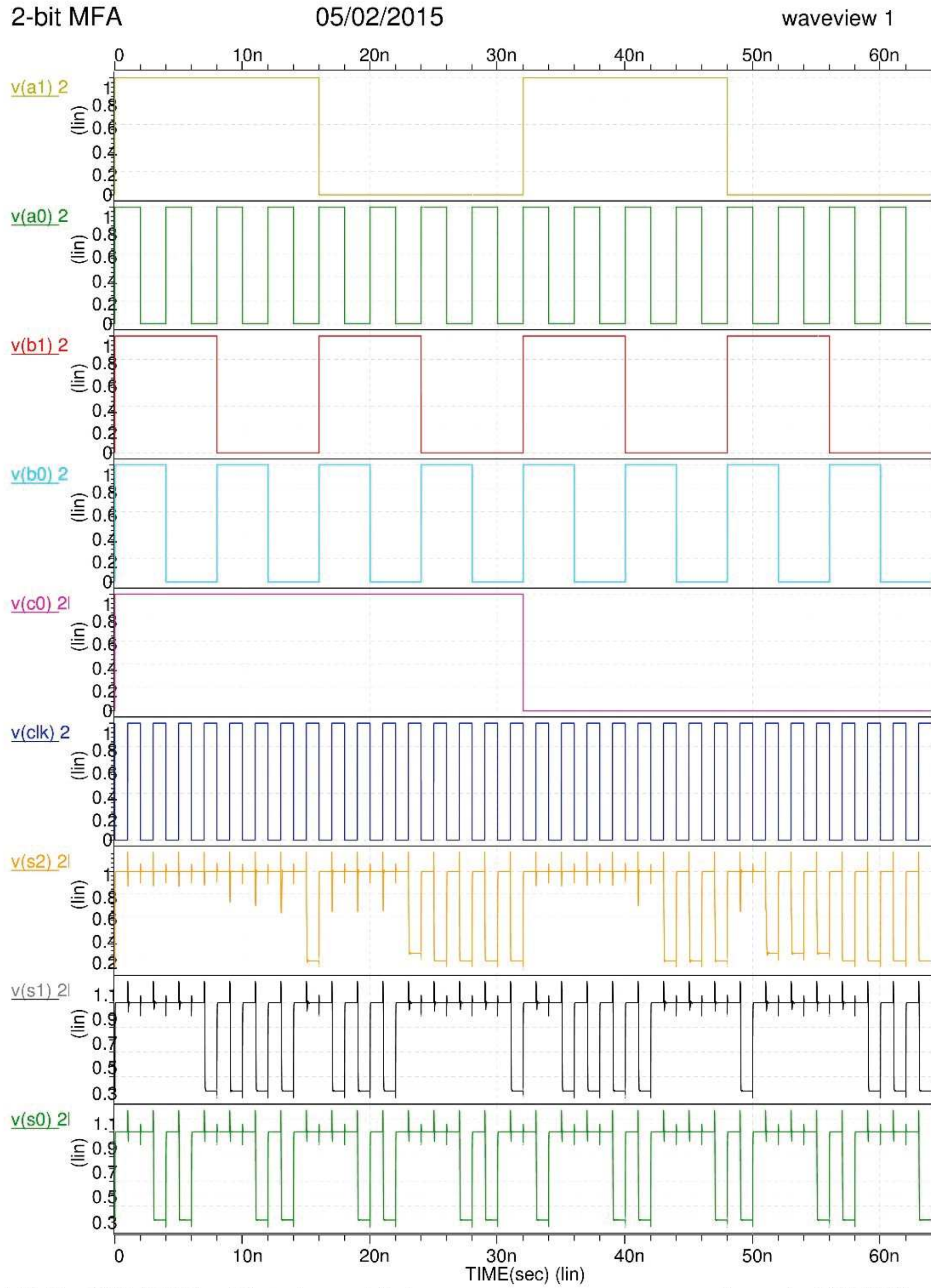

Figure 4.6: Simulation results of two-bit carry look-ahead magnetic adder

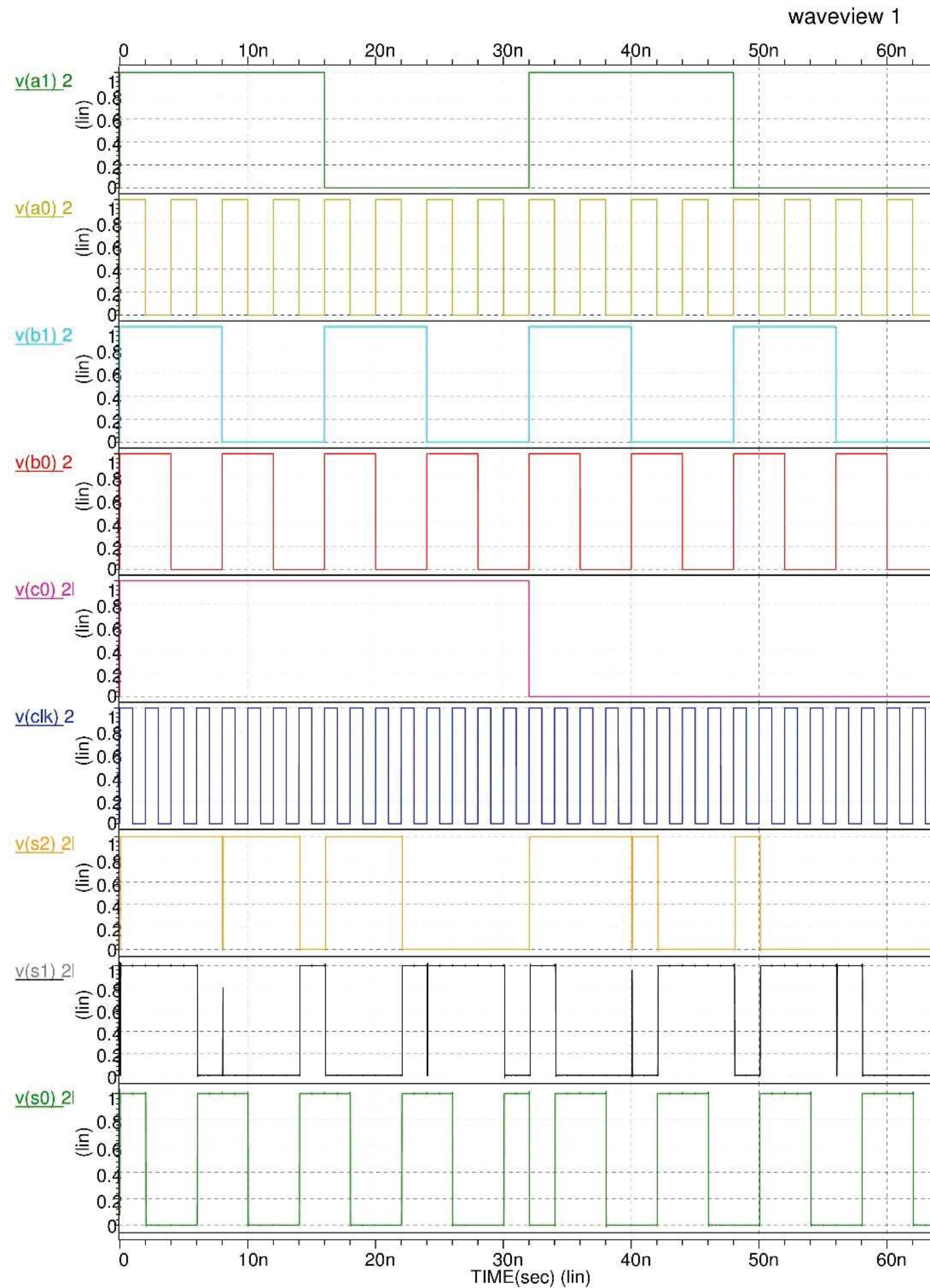

Figure 4.7: Simulation results of two-bit carry look-ahead conventional adder with outputs synchronized

4.3 Performance Evaluation of Multi-Bit Adders

Table 4.2 and 4.3, illustrates the performance comparison of 1- and 2 bit magnetic full and conventional adders with synchronized outputs. As illustrated above, the dynamic power of one-bit magnetic full adder is less than the half of dynamic power consumed by conventional CMOS full adder with almost equal speeds and follows the same trend of low consumption of power when the system is in standby modes, the magnetic full adder consumes far less leakage power than that of conventional adder. When the same one bit adders were used to design the two-bit carry look ahead adders there was a huge increase of consumption power (both dynamic and standby) for both conventional and magnetic full adder due to the high fan-out and increase in the capacitive load. As mentioned above, there is a huge amount of increase in the dynamic power consumed by two-bit conventional carry look ahead adder of about 20 times with an approximate 2.5 times of the increase in delay, whereas, in case of two-bit magnetic adder there was approximately 8 times of increase in dynamic power with 1.5 times higher than that of one-bit MFA.

Dynamic power is calculated using the total energy of a system to pass a set of data and it is given by:

$$P_{dynamic} = E_{tot} \cdot f_{clk} \tag{4.5}$$

Where the total energy is given by:

$$E_{tot} = \int I_D \cdot V_{DD} dI \tag{4.6}$$

5 16-BIT MAGNETORESISTIVE RANDOM ACCESS MEMORY (MRAM)

MRAM is a type of RAM, which uses magnetic charge to store the data in magnetic tunnel junction unlike conventional SRAM or DRAM, which uses an electrical charge to store the data. The MRAM is a non-volatile memory, which stores the data in the form of electrical resistance using a special magnetoresistive metal (ferromagnetic materials) separated by thin non-magnetic oxide layer. Unlike conventional RAMs (SRAM and DRAM) in CMOS, MRAMs retains the data even when supply-voltage (power) is off. MRAM [21] has a wide range of applications in the memory market, which can store the huge amount of data in electronic devices by consuming very less power. The real deterrent before the wide uses of MTJ based memory or logic circuit is its switching technology and few methodologies have been proposed and exhibited in the most recent ten years. In this research we use spin transfer torque writing approach to write the data bits into the MTJ. The critical currents and the resistances used in the MTJ model are determined as ICAP = $-350\,\mu A$, ICP = $350\,\mu A$, RAP = $1.08\,k\Omega$ and RP= $0.3\,k\Omega$. In this section we discuss the 16-bit MRAM design and architecture, and compare its performance with 16-bit conventional SRAM.

5.1 Crossbar Architecture Using 2R-Complementary Resistive Switching Memory Cell [24]

The crossbar architecture of 16-bit MRAM is illustrated in fig. 5.1 below. It consists of three main components [24]: 1) memory arrays for data storage, 2) bit line and word line drivers, and 3) sense amplifiers for read operations. The operation of each component is discussed in detail below.

5.1.1 Memory Cell Structure And Operation

As shown in fig 5.1, every one bit memory cell consists of 2R complementary MTJ whose bottom electrodes (BE) are connected to each other and these BEs connected to the word line (WL) while their top electrodes (TE) are connected to the bit line (BL) and complementary bit line (/BL). These memory cell operate in two phases:

Phase 1: The word line is set to "0" and the input data (BL and /BL) is pre-charged to VDD. During this phase, current flows from top to bottom and the resistance value of both MTJs is set to the initial condition value ($R_{AP} = 1.08\,\mathrm{k}\Omega$).

Phase 2: The selected word line is set to logic "1" and the input data is written to these MTJs and current flows from bottom to top. At the end of this phase, both MTJs results in opposite resistance state. It is important to note that all other word lines that are unselected are to be biased to VDD/2 to keep the resistive elements unchanged. One sub array that shares bit line or word line with the selected word will have "VDD/2" biasing while the other cells see a biasing of 0V. The read operation is performed on each of four columns and bit-line and complementary bit-line are sensed using the pre-charged sense amplifier as discussed in the previous chapter.

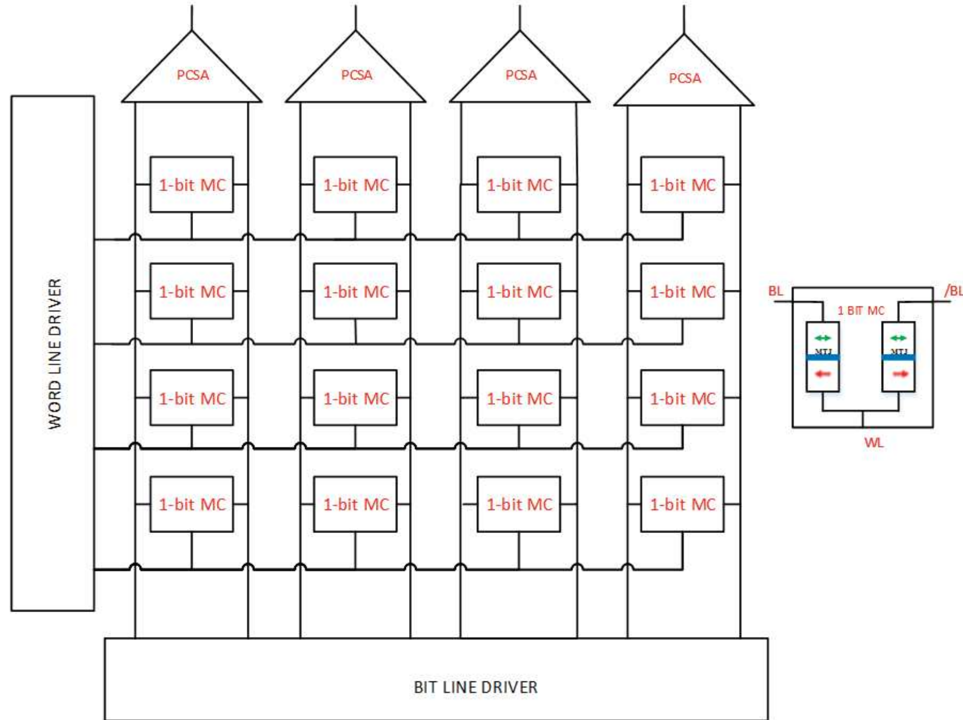

Figure 5.1: Crossbar architecture based on 2R complementary resistive switching 16-bit MRAM [24]

5.1.2 Memory Array, Bit Line And Word Line Driver

As shown in fig. 5.1, the array is divided into 4 word lines. Each word is composed of 4 bits (memory cells). There is one driver circuit associated with each word-line and bit line to ensure the proper biasing condition for all three modes of operation i.e., write, read and unselected [24]. Fig. 5.2 illustrates the word line driver configuration for selected and unselected words. The data coming from the word line decoder will go through the word line driver which decides the biasing voltage for selected and unselected words. It is important to maintain the present electro-resistive data in the group of memory cells that are not selected by the word line, which is completed by decoders. Bit-line decoders work with the same mechanism as that of word-line decoder, which are controlled by the write and read enable pin.

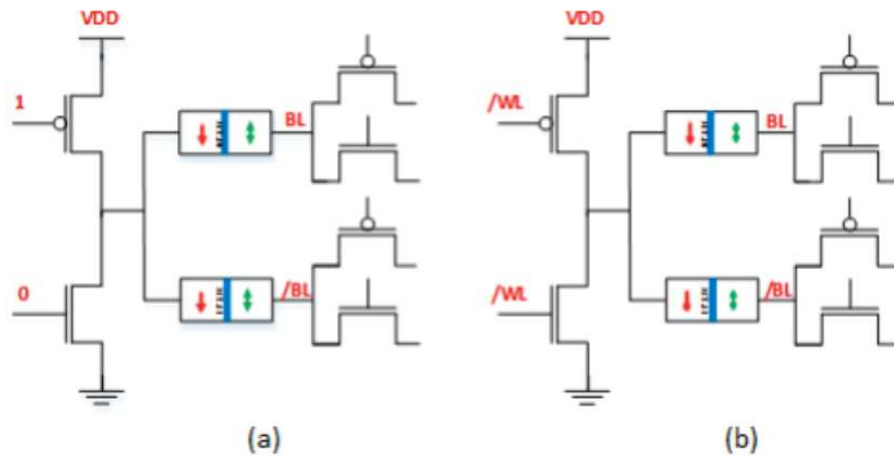

Figure 5.2: Bit-line and word line drivers. Word line configuration for (a) unselected and (b) selected word

5.2 Controlling Mechanism For MRAM Word Line And Bit Line Driver

As illustrated in fig 5.2, these drivers are needed to be controlled by the specific logic such that, their output is biased to VDD/2 for the word line selected 0 whereas, the output of this decoder should be pre-charged to VDD for the word line selected 1. Fig 5.3 below, illustrates such mechanism to control these drivers.

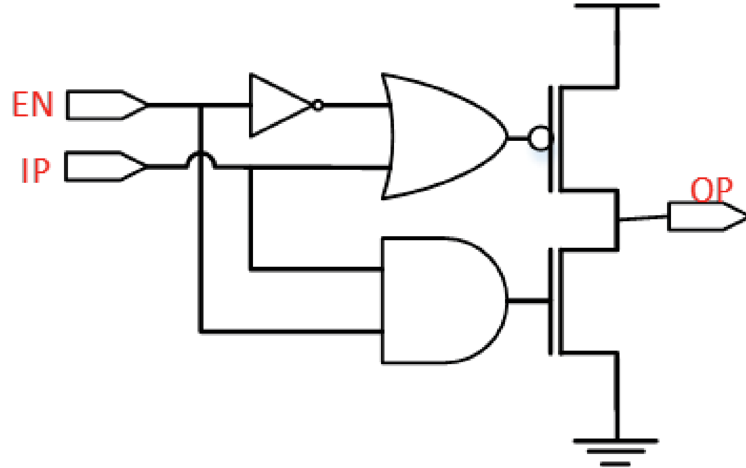

Figure 5.3: Control logic for word-line and bit line driver

In case of a bit line driver, it is important that the driver does not write any data to MTJs while reading the data from them. We can control this operation by selecting the enabling pin (EN) as write and read enable pin ($\frac{W}{R}$) and input pin (IP) as bit line or complementary bit line respectively.

5.3 2-to-4 Decoder For MRAM

We need to 2-to-4 decoder to control the word line operation for selecting a memory cell. Fig. 5.4 shown below, illustrates the 2-to-4 decoder design used for this RAM. Here, I0, I1 and complementary /I0 and /I1 are the two address lines from which 4-word lines (WL0, WL1, WL2 and WL3) are generated.

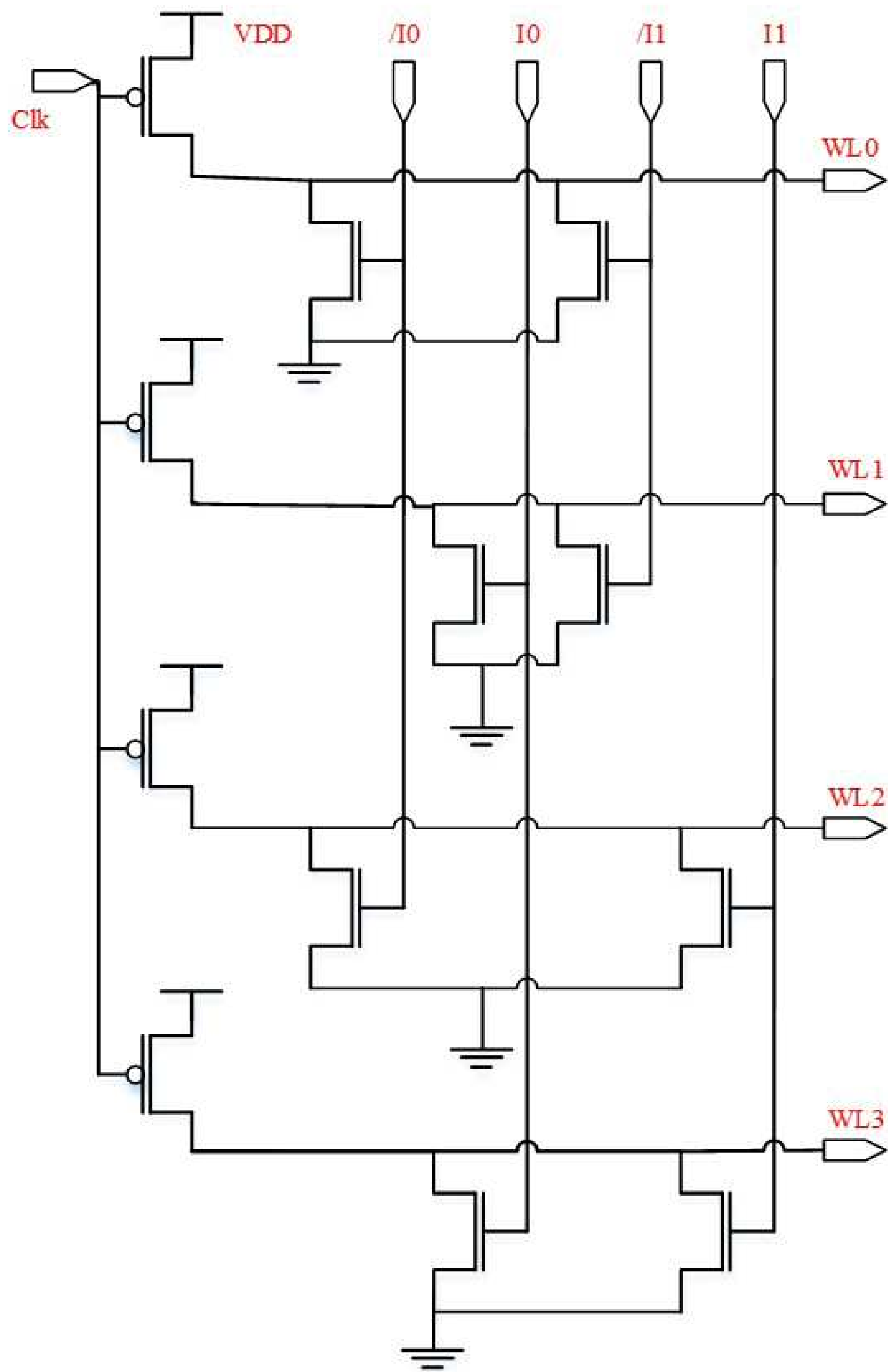

Figure 5.4: 2-to-4 decoder

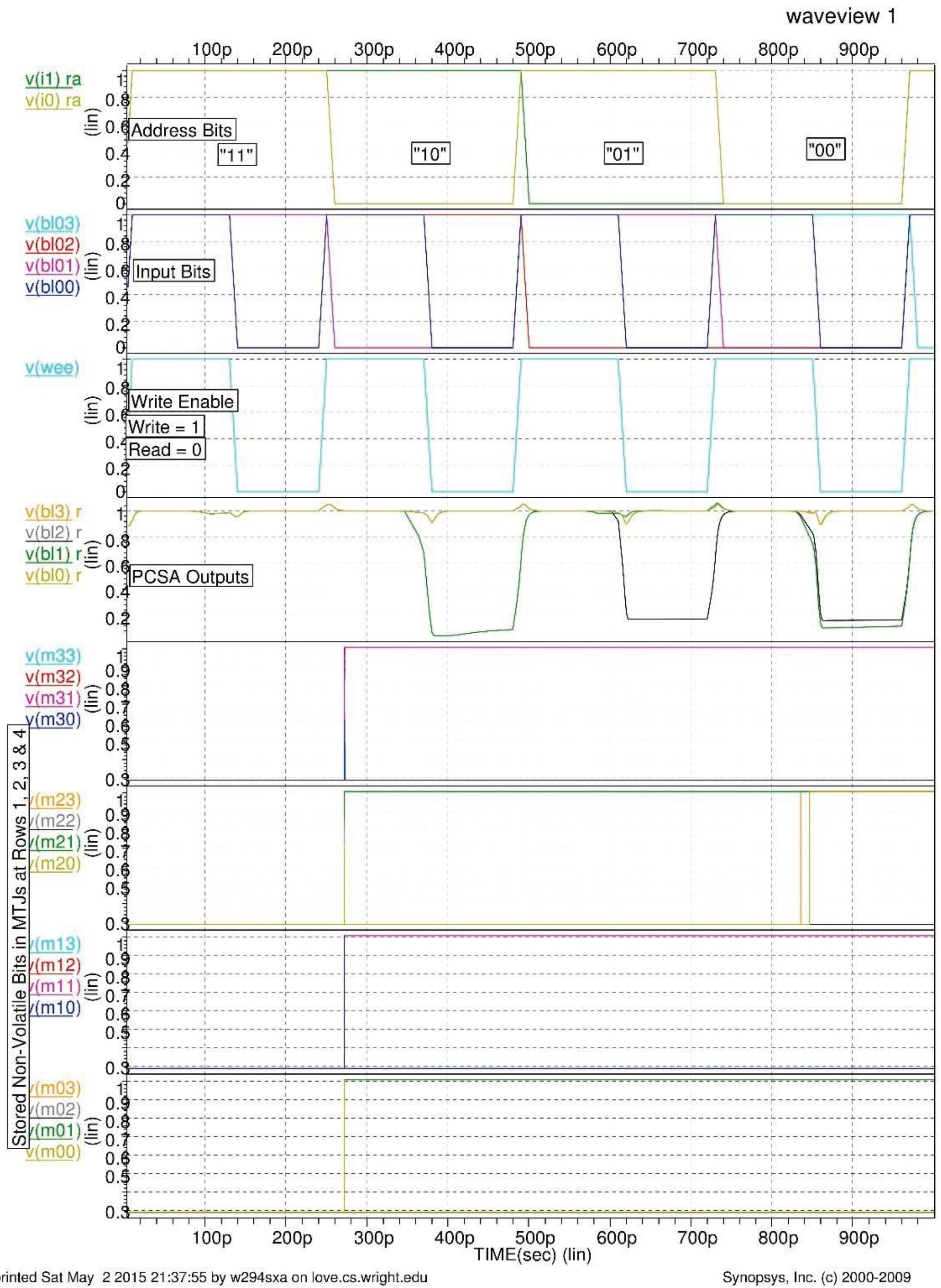

Figure 5.5: Simulation results of 16-bit MRAM without considering magnetic storage

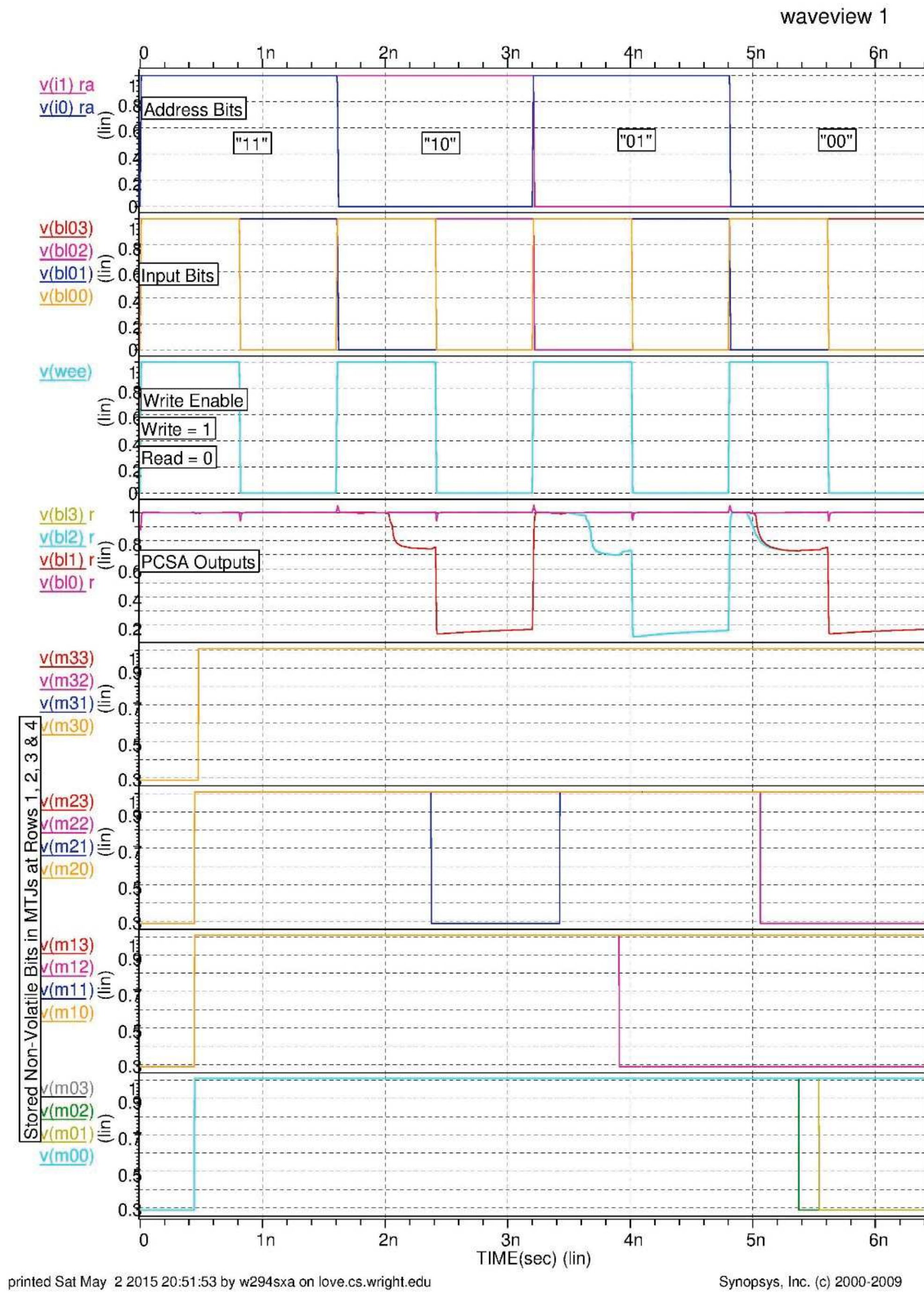

Figure 5.6: Simulation results of 16-bit MRAM with magnetic storage

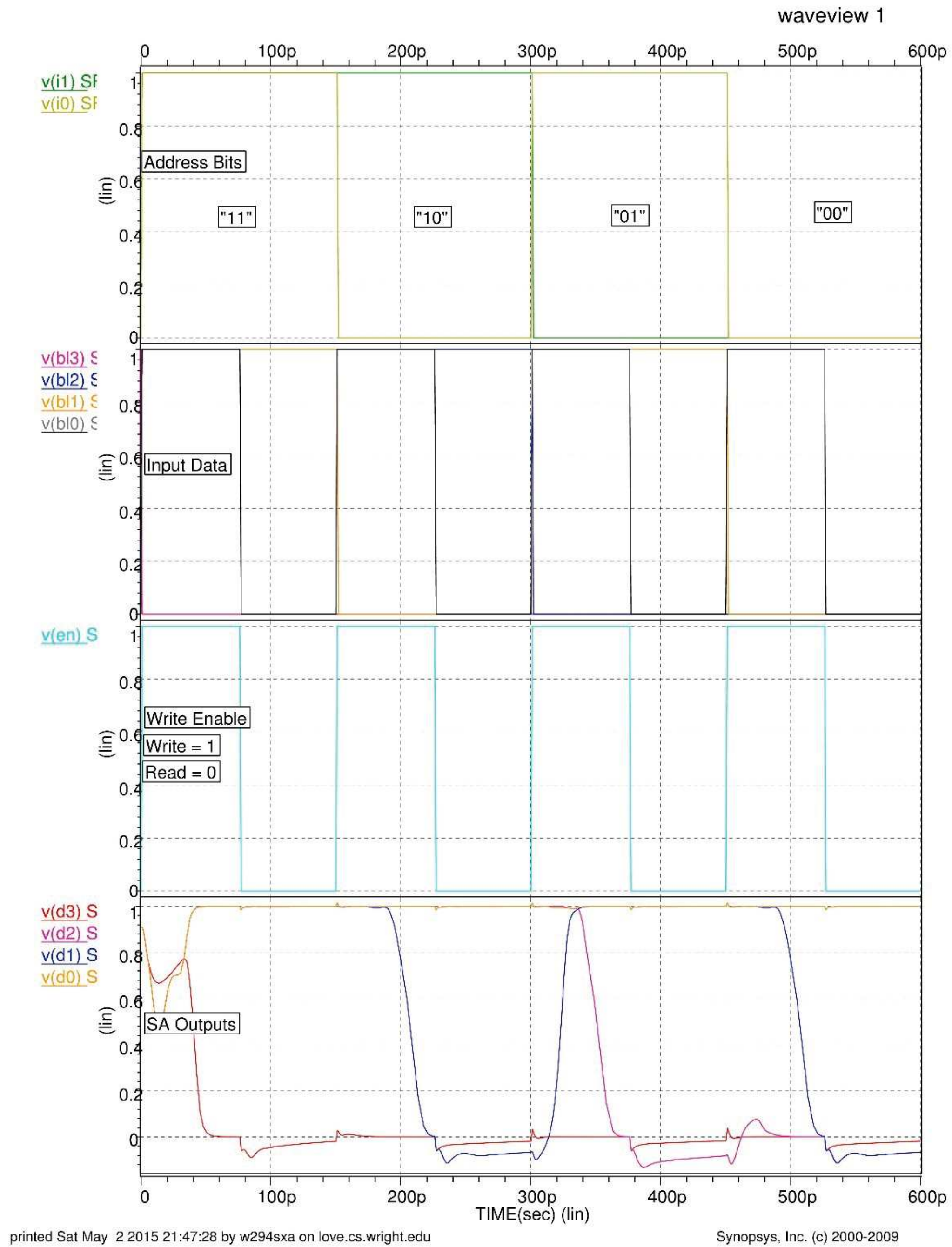

Figure 5.7: Simulation results of 16-bit SRAM

5.4 Performance Evaluation Of 16-Bit MRAM

In this section, the performance of both SRAM and MRAM are compared. In case of MRAM, magnetic tunnel junction used does not speed up storing and projecting the data at the same time. On the contrary the MTJ takes an additional time to store and project the data as output. In our simulation we took two cases in which we considered the non-volatility of MTJ. In the first case, we allow sufficient time for each address where the MTJ would process properly and project the non-volatile data in the form of its resistance value.

In the second case, we do not consider its non-volatility, i.e., by not giving sufficient time to each address at the decoder. In the second case of our study, it is found that though the MTJ resistance change after writing it with a short pulse of BL, it needs additional time to project the data written in the form resistance which it normally does for storing the data. In this case, the power sense amplifier is able to detect the data that was stored in the memory cell although the MTJ's are not projecting the data written into them. Fig. 5.5 and 5.6 illustrate these two different cases of writing and reading the data in volatile and non-volatile case, respectively. Table 5.1 presents the performance of SRAM and MRAM on different factors. The 16-bit SRAM used here is one the basic design of its kind and its simulation results are shown in fig. 5.7.

Table 5.1: Table illustrating the performance comparison of 16-bit SRAM and MRAM considering volatile and non-volatile case

Factors	SRAM (45 nm CMOS)	MRAM (45 nm MTJ and 45 nm CMOS) (Without Considering Magnetic Storage)	MRAM (45 nm MTJ and 45 nm CMOS) (Considering Magnetic Storage)	*Zhao*[24], [25] Model: MRAM (45 nm MTJ and CMOS)
Dynamic Power	1.1 mW	90 µW	0.15 mW	-
WAT	75 ps	120 ps	0.8 ns	1.1 ns
RAT	50 ps	60 ps	0.8 ps	1.1 ns
Stand-by Power	10 µW	3.6 nW	1.5 nW	-

As shown in fig. 4.6 and 4.7, while considering magnetic storage, the stored non-volatile resistance value changes when the word line is set to “1” for one row of memory cells at a given particular time of address to the decoder as shown fig. 4.6, whereas, while not considering the magnetic storage the stored magnetic values are constant for all 16-bits of memory cells as shown in fig. 4.5. From table 5.1, given above, It’s shown that even though the dynamic and leakage power consumed by MRAM is much less than that of SRAM, the write and read access times of SRAM are less than that of MRAM.

6 CONCLUSION AND FUTURE WORK

6.1 Conclusion

In this research, we have investigated the use and impact of magnetic tunnel junction from the device to the architectural level, which covers the design, analysis and performance evaluation of logic circuits combining MTJ devices with CMOS technology. A general study of design principles and simulations of non-volatile circuits such as magnetic logic circuits and MRAM is conducted. Their impacts on architecture and power issues of advanced conventional CMOS based logic circuits and memories have been presented.

Using logic-in memory architecture, we have designed the magnetic logic gates that consume only half of power consumed by conventional CMOS logic gates circuits. It is shown that magnetic logic circuits are faster. We have implemented the two-bit magnetic carry look-ahead adder using the 1-bit magnetic adder by setting the widths of switching circuit and the sensing transistor accordingly such that all the logical operations are covered by these adders. It is found that due to the high fan-out in these circuits the power consumed by the 2-bit magnetic adder is significantly increases to 8 times with an increase in delay of 1.5 times when compared with the 1-bit magnetic adder. When it comes to the conventional CMOS adders, the power consumed by two-bit synchronous CMOS adder was increased to 20 times with 2.25 times increase in delay when compared with the 1-bit CMOS synchronous adders.

When it comes to 16-bit MRAM, we have discussed two different cases of simulating it, i.e., with or without considering the magnetic storage of MTJ (non-volatility). When compared to SRAM, MRAM is slower but consumes much less power due to the significant decrease in leakage currents when memory is in stand-by mode. The dynamic power consumed by SRAM is 12.2 and 7.3 times higher than MRAM of two different cases. The read and write access time of MRAM is 1.6 and 10.6 times and 1.2 and 16 times slower than the SRAM. The leakage power consumed by MRAM in two different cases is negligible when compared with SRAM. When we consider magnetic storage of data in MRAM it takes additional time to write and read data from MTJ, which results in slower and little increase in power as illustrated in table 5.1.

6.2 Future Work

This research study presents the advantages of memories and logic designs using MTJ in terms of its power consumption and there performance during stand-by mode. These hybrid architectures of using CMOS and MTJ can be improved further by developing new MTJ models with novel switching technologies to consumes less power and possess fast read and write access times. Another important future work includes developing improved architectures which includes less no. of transistors than MTJ which would eliminate the power consumption of dynamic CMOS. Furthermore, developing model files of MTJ for post layout performance evaluation using Monte Carlo simulations.

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