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# Analysis and Comparison of Popular Models for Current-Mode Control of Switch Mode Power Supplies

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# Analysis and Comparison of Popular Models for Current-Mode Control of Switch Mode Power Supplies

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By

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Ramchandra Mahendrabhai Kotecha ENTITLED Analysis and Comparison of Popular Models for Current-Mode Control of SMPS BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

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# Abstract

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Current-mode control is the most popular scheme used for the operation of SMPS (Switch Mode Power Supplies). Current-mode control, also known as current-programmed mode or current-injected control is a multi-loop control scheme that has an inner loop and an outer voltage loop. The current loop controls the inductor peak current while the voltage loop controls the output voltage. The inner loop follows a set program by the outer loop. Some of the most popular small-signal models that predict the small-signal characteristics of current-mode control scheme have been analyzed and compared in this thesis. A PWM dc-dc buck converter in CCM(Continuous Conduction Mode) has been chosen to explain the phenomenon of current-mode control in all these models. Small-signal characteristics are generated in MATLAB using the simplified analytical transfer functions. Some of the important small-signal characteristics include the current loop gain, control-to-output gain with the current-loop closed and outer loop open, audio susceptibility, and output impedance. The two most important models in consideration are: 1) Continuous-Time Model and 2) Peak Current-Mode control Model. Despite the fact that both these models predict the instability of current-mode control at a duty ratio of 0.5, these models differ significantly in deriving the expression for the sampling gain. As a result, their small-signal characteristics differ over a wide frequency range. Also, a very less explored average currentmode control is compared with the peak-current mode control based on the similar small-signal characteristics.

# Contents

# List of Figures

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# 1 Introduction

## 1.1 Background

The controller design for SMPS has always been a complicated issue and a unique topology that can be optimum for all power supply technology is yet to be developed [2]. There are two fundamental approaches for designing the control circuit for the power converters. They are:

1) Voltage-mode control Scheme

2) Current-mode control Scheme

Previously, it was believed that current mode control was the most superior approach to design the control circuit for the PWM dc-dc power converters until the introduction of UCC3570 (a voltage mode controller) by Unitrode IC corporation. After the introduction of this controller, it became clear that there is no unique scheme that can render optimum results for all power supply applications. However, current-mode control scheme is still a widely used approach to design the control circuits for SMPS [2]. A brief review of both the approaches is explained as follows:

### 1.1.1 Voltage-Mode Control Scheme

The circuit diagram for this scheme is shown in Fig. 1.1. The major advantage of this circuit is its single voltage feedback path wherein the duty ratio is controlled by comparing the waveform obtained from the resulting error voltage from the operational amplifier with an external ramp which is fixed citekazpwm. Owing to this single loop, the circuit topology becomes easier to design and analyze. The modulation is stable in voltage-mode control because of high amplitude ramp. Cross-regulation is better compared to current-mode control because of low-impedance at the output [2].

However, there are certain disadvantages of this method that limits its use to certain applications only and they are listed as follows:

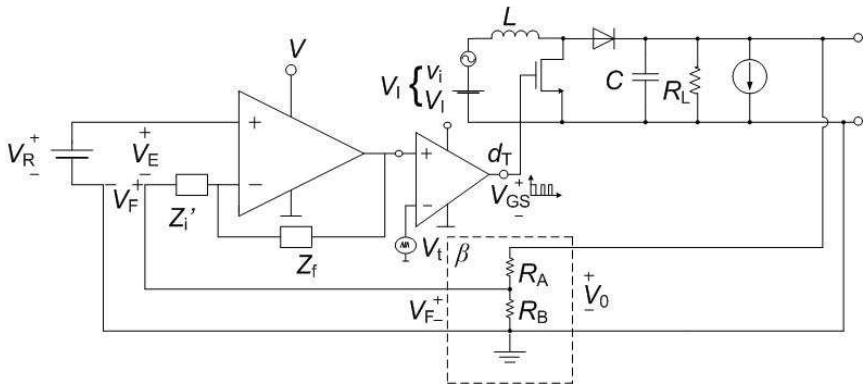


Figure 1.1: Voltage-mode control of a boost converter [1].

- Voltage-mode control has slow response compared to current-mode control because any change in input voltage or load resistance will be first required to be sensed by the change in output voltage. The voltage feedback loop will then correct any changes in the input voltage and load resistance [1] and [2].

- The RC-circuit at the output adds an extra pole in the feedback loop. Therefore, a zero will be required to be added by the controller [2] and [1].

- The open loop gain of the circuit changes with the change in line voltage [2] and [1].

### 1.1.2 Current-Mode Control Scheme

The disadvantages of the voltage-mode control are significant in most power supply topologies and most of these were effectively alleviated by this scheme. Consequently, current-mode control scheme became popular for designing the control circuits compared to other schemes of control. The circuit diagram for the current-mode control scheme is shown in the Fig. 1.2 [2].

This scheme is a multi-loop control scheme as shown in Fig. 1.2. The inner loop controls the peak value of the inductor current, while the outer voltage loop controls output voltage. Modelling of current-mode control is slightly complicated and

requires sampled-data modelling. This scheme provides short-circuit protection and over-current protection in PWM converters [1] and [2]. The output response of the this scheme is fast and wide-band [1].Having said that, current mode control provides certain disadvantages that are detailed as follows:

- The circuit analysis becomes difficult with two current loops in this method [2] and [1].
- The control loop has inherent instability at the duty ratio of 0.5. For higher duty cycles, slope compensation is required which makes the analysis even more complicated [2] and [1].
- When the ripple due to inductor current is small, it may well introduce noise in the loop [2] and [1].
- The capacitance in the transformer winding sometimes creates resonance in the current loop, which is also one of the sources for the noise [2].
- Load regulation is significantly affected since the control loop is forcing a current drive [2].

From above disadvantages, it is clear that even though this scheme alleviates the limitations by the voltage-mode control, it is still not the optimum mode of control for the operation of PWM converters. In fact, the recent developments in the Power Control Technology indicate that the shortcomings of voltage-mode control can be overcome. Hence, even though, current mode control was believed to be the best approach, there is possibility of the revival of the voltage mode control. This possibility has resulted in the invention of UCC3570 with an effort to correct the flaws in voltage mode control. This controller significantly improved the design of voltage-mode control by providing feed-forward voltages to the changes in the input voltage and by

using BicMOS processing resulting in smaller parasitics [2]. If the compensating ramp is made proportional to the input voltage, then voltage feed-forward can be achieved [2] and [1]. The control modulation is accomplished without providing voltage feedback. This eventually results in a fixed loop gain and fast response to the changes in line voltage. Therefore, the problem of slow response is eliminated. These design changes results in high frequency capabilities and a higher bandwidth for RC-circuit at the output [2] and [1]. Therefore, many of the problems of the earlier topologies in voltage mode have been alleviated in UCC3570 [2].

## 1.2 Motivation for Thesis

The current-mode control scheme is still the most widely used scheme for the control of PWM converters. The most commonly used model in the industry these days is the "Continuous Time Model" proposed by Ridley. The model approximated for small-signal characteristics has a sampling gain with more zeros than poles. However, the model has been purposefully approximated such that it is accurate upto half the frequency of interest beyond which the system is unstable unless compensated externally. Hence, this model is widely used in the industry for the control of switch mode power supplies. As a result, this model is slightly difficult to understand owing to its complexities in the derivations and expressions. Also, there is an unbelievable mess in the current mode control theory with several conflicting theories prevailing. Another popular model for the educational purpose is the peak current-mode control model proposed by Kazimierczuk. This model overcomes the anomaly of the improper transfer function unlike the continuous time model. There was a motivation to compare the two models which have not been compared so far in any research publication. However, the small-signal characteristics are substantially different in the two models owing to these fundamental differences. Another application of this scheme is average current-mode control scheme which is very less explored. There was a motivation to

explore an alternate method as well so that another alternate model can be developed in future which overcomes the limitations of the current-mode control [1] and [3].

## 1.3 Thesis Objectives

- To explore different methods used so far for control of SMPS.
- To compare and analyze the two main types of control schemes for SMPS.
- To analyze current-mode control in depth and understand the limitations of this method.
- To study average current-mode control method of for PWM dc-dc converters as an application of current-mode control scheme.
- To generate the small signal characteristics using the simulation results obtained from the MATLAB.
- To compare and analyze the models based on the small signal characteristics.
- To propose a recommendation for the future work.

## 1.4 Choice Between the Two Main Types of Control Schemes

All of the above discussions clearly indicate that both modes of control are viable choices in today's environment. The choice between the two topologies actually depends on the application and hence there is no single control scheme which can be considered optimum for all the applications [2].

### 1.4.1 Applications suitable for Current-Mode Control

- When the output of SMPS is desired to be a current source as in case of buck converters [2].
- When at a given frequency, a fast dynamic response is needed [2].

- More suitable for a PWM dc-dc converters changes in the line voltage are relatively lesser [2].
- When pulse by pulse modulation is needed and when load sharing with parallel multiple power units is required [2].
- In low-cost applications where fewest components are required [2].

### 1.4.2 Applications Suitable for Voltage-Mode Control

- When there are a large line or load variations possible [2], [1].
- When the current ramp is too small for stable PWM operation particularly with low line and light load conditions [2] and [1].
- When noise due to the resonance in the current loop would very high, particularly with high power and noisy applications [2] and [1].
- When relatively good cross regulation is needed compared to current mode control [2] and [1].
- Where less complexities in design are needed and multi-loops are to be avoided [2] .

Even-though, current-mode control is still most widely used method till now, there are several other methods developed recently in an effort to try and overcome the limitations of this control scheme. Average current-mode control is one of those promising methods which can overcome many of the demerits of the previously derived models that were based on controlling the current. The motivation behind this thesis is to understand the complexities and several contradictory ideas prevailing in the control schemes [4], [3] and [5].

In this thesis, first the peak current mode control is studied in detail so that the disadvantages offered by this method can be understood in detail. Two popular models for current-mode control topology are studied and compared in detail. This will provide the platform for a similar kind of approach for the controller design but will overcome the limitations of the peak current mode control to a substantial extent. After that, the average current mode control will be studied in detail [4] and [5].

## 1.5 Current-Mode Control Scheme

This control scheme is a multi-loop control scheme as explained in brief in the earlier section. Some other popular names of this method are 'current programmed mode' or 'current injected control' [2] and [1]. The inner loop follows a set program to control the peak value of inductor current whereas the outer loop is copensates any changes in the load voltage [1] and [24]. The inductor peak current is directly controlled whereas the output voltage is controlled indirectly by the current loop [2] and [1]. The relationships between the inductor average current, inductor peak current and the load current are different for different type of converters [2] and [1]. In buck and buck-derived converters, the inductor is on the output side. Therefore, the actual current flowing on the load-side is average inductor current. In case of a boost converter, the average inductor current represents the actual current flowing into the converter system[1]. The inner current loop dynamically changes the duty ratio during the initial stages in response to the disturbances in the line current [1]. The outer loop produces a reference voltage for the inner loop in response to the changes in the converter output voltage [1]. The duty ratio is calculated based on time instants at which the inductor or switch current reaches a maximum level determined by the outer loop program. This inductor current is fed into the inner loop. Thus the inductor is changed into a voltage dependent current source at frequencies lower than those beyond the threshold level [1] and [2]. There are two fundamental types of current

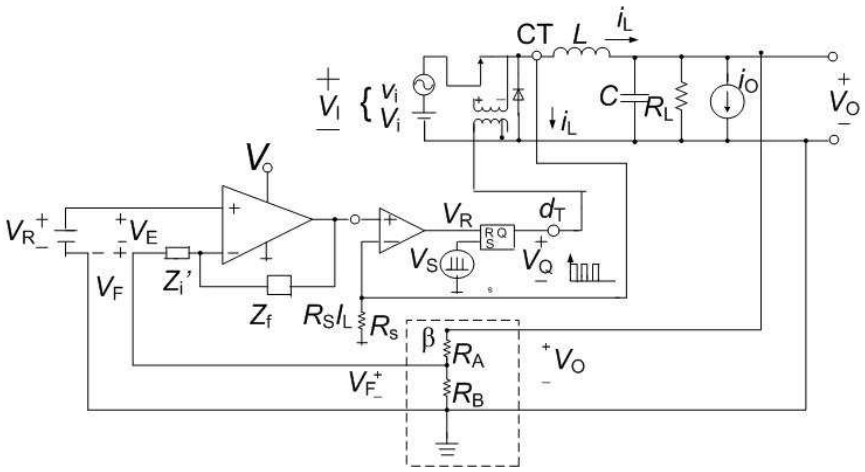


Figure 1.2: Circuit of a PWM dc-dc buck converter operating under current-mode control scheme [1].

mode control: Fixed frequency control and variable frequency control methods [1]. In the first type, the switching frequency is constant and synchronized to a clock signal i.e. $f_s = f_{clk}$ [1]. This type contains peak-current-mode control scheme, valley current-mode control scheme, PWM conductance control scheme with triangle-wave compensation and average-current-mode control scheme [1]. The second type contains either with a fixed on-time or off-time and hysteric methods [1]. Even-though it has a lot of limitations, the fixed frequency peak current mode control with fixed slope compensation ramp is still most widely method. As mentioned earlier, current-mode control scheme is the most widely used method and so is mentioned in detail [1].

### 1.5.1 Current-Mode Control

The circuit for PWM dc-dc buck converter with fixed-frequency current-mode control is shown in Fig 1.2.

As mentioned earlier, the circuit has two loops making it a multi-loop control scheme. The inner loop contains a comparator, a set-reset latch, a frequency signal, and a current sensor which could be a current transformer or a non-inductive sense resistor $R_S$, which senses the inductor current $i_L$ or the switch current $i_S$ [1]. Thus, $R_S$

is the transfer function with voltage across the sensor as the output and the inductor or switch current as the input [1]. It could be the transfer function of a current transformer which has corner frequencies in the dc and high frequency ranges. The latch performs set and reset operation for the Q. The peak current-modulation is achieved by the comparator, SR latch and the frequency signal from the clock. $V_c$ is applied to the comparator inverting terminal and the $R_s i_L$ is applied to the non-inverting terminal [1]. The controlled switching operation is carried out by a set current which is due to the control voltage and a non-inductive resistance in the path of the inverting input and ground of the voltage comparator [1]. The principle of operation of the buck converter with current-mode control scheme can be explained with the waveforms shown in Fig 1.3.

The clock generates voltage pulses at a constant clock frequency $f_{CLK}$ equal to the switching frequency $f_S = 1/T_S$. When the clock output voltage $v_{CLK} = v_S$ goes high, the latch Q output sets to 1. Therefore, the gate to source voltage $v_{GS}$ also goes high turning the switch on. This event initiates the transistor on-time and starts the cycle $T_S$ of the switching frequency $f_S$. This is an example of constant frequency current-mode control since the turn-on times are periodically clocked. While the switch is on, the inductor current and the switch current increase linearly. The inductor current $i_L$ is sensed by a probe which flows through the resistor $R_S$ and develops a voltage $R_S i_L$ [1]. When this voltage is less than the control voltage, the comparator output voltage $v_R$ is low since the control voltage is negative and higher. And once this voltage reaches a level set by the program, the comparator output voltage $v_R$ goes high, and the latch resets resulting in the switch to turn off. In short, the switching operation follows the current program, where the peak current follows the current set by the program [1]. The inductor average current is given by

$$I_L \approx I_{Lpk} - \frac{\Delta i_L}{2}. \tag{1.1}$$

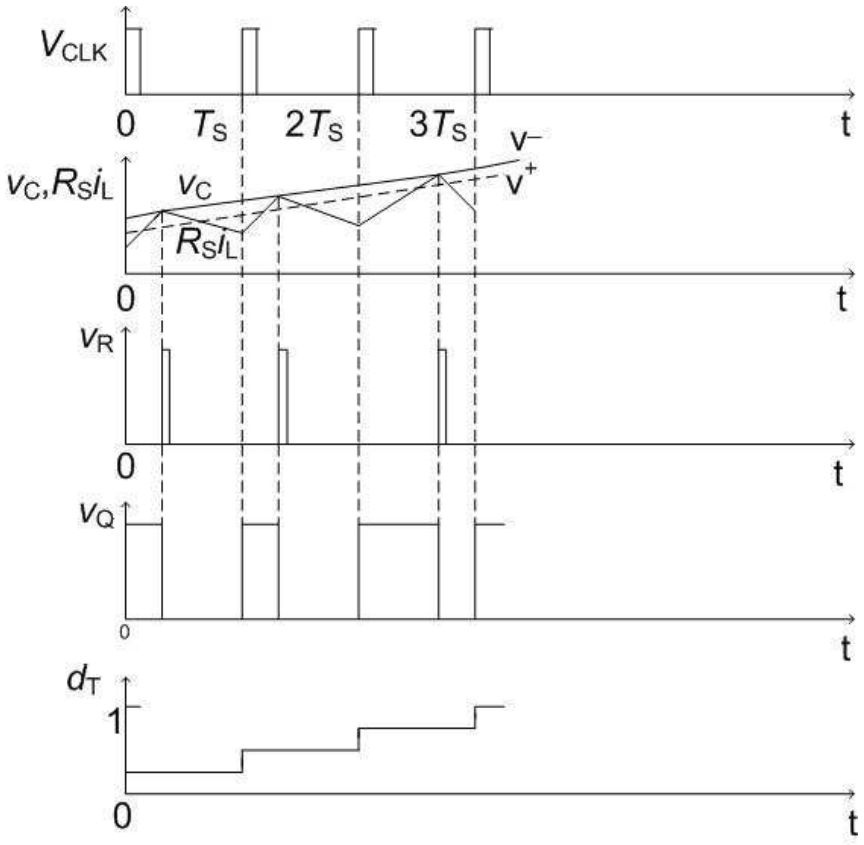


Figure 1.3: Voltage and current waveforms for dc-dc buck converter with constant frequency pulse-width modulation [1]

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Thus, this current program controls the inductor peak current directly. The inner loop, in this scheme, is responsible for fast response to any changes in input and load side [1].

The control scheme here, belongs to the category of fixed-frequency type and the modulation is of the trailing-edge type since the amplitude of the inductor current follows a set program. The peak value here is nothing but the sum of average value and peak-to-peak current ripple which results in indirect control of the inductor average current. The current in the inner loop follows the set program given by the outer loop. The negative feedback path is created by a non-inductive resistance for the inductor current. And the negative feedback for the load voltage is provided through a voltage

divider network which is compared with a reference voltage through a comparator. The control voltage is set/reset based on that [1]. The corresponding values of output voltage and inductor current are determined by the duty ratio. Thus, the inductor now becomes a voltage-dependent current source because of this inner current loop [1]. Even-though, with many disadvantages, the peak current mode control has several problems which have still left the quest for a better mode of control open. Some of the important problems with the current mode control have been listed as below.

## 1.6 Problems with Peak Current-Mode Control

### 1.6.1 Poor Noise Immunity

As shown in the Fig. 1.2, in this method, the rising slope of the inductor current waveform is compared with the control current. The switching operation is controlled by this control current. The current ramp is usually quite small compared to the control current set by the outer loop and hence this method is less immune to noise compared to voltage-mode control. Thus, every time the switch is turned on, there is spike generated due to above reason. Since the control current is higher than the current ramp, even a fraction of the voltage coupled to the outer loop will cause the switch to turn off resulting in sub-harmonic oscillations with large magnitudes of ripple. For the stable operation of this scheme, the circuit topology and current bypassing are very important [1] and [4].

### 1.6.2 Necessity of Slope Compensation

From the above, it is quite clear that current-mode control becomes unstable half the switching frequency resulting in sustained oscillations. An external ramp is therefore required to be added to the comparator input for stable converter operation. In a buck converter, the inductor current down-slope equals $\frac{V_O}{L}$ and thus varies considerably as the input voltage follows the rectified sine waveform. However, a fixed external ramp

in most cases, overcompensates the inductor current, which will eventually result in performance degradation and increased distortion [1] and [4].

### 1.6.3 Peak to Average Current Error

In case of buck converters, this isn't a major problem because the average value of inductor is much higher than the noise ripple. Also, the voltage feedback loop compensates for this error by compensation [1], [4]. However, in case of boost converters, this is a major issue. The peak inductor current is controlled by the modulator waveform while the average current is not. In discontinuous conduction mode, this error is even higher as the sine wave of the modulator approaches zero half cycle. This error must be made small as possible to achieve low distortion levels. To make the noise ripple small, the size of the inductor has to be large. However, this further reduces the noise immunity as the inductor ripple gets smaller [1] and [4].

### 1.6.4 Topology Related Problems

Conventional current-mode control scheme controls the peak value of inductor current. Inductor current is on the load-side of the buck converter and hence this scheme is most effective in case buck-derived converters. But for the boost or the fly-back converter schemes, the inductor is not at the output. Average current needs to be controlled in these schemes. Hence much of the benefits of this scheme are lost with this kind of topology where the inductor is on the load-side. Therefore, the input current control is more suitable for the boost and the flyback kind of topology [1] and [4].

# 2 Comparison Between UMT and NCT Models

## 2.1 Introduction

There are several models proposed so far for the Current-Mode control scheme for power converters. The state space averaging technique is a very popular technique for the modelling of current-mode control scheme for power converters. However, important research work has been made in modifying this traditional approach towards small-signal modelling. This kind of approach takes into consideration the fact that current-mode control modelling requires discrete-time analysis. Two of the popular approaches in this direction are considered here for the comparison:

1)The Unified modelling technique.

2)New continuous time technique.

These two techniques have been combined and the resultant small signal characteristics can be obtained. Average modelling techniques have been used to derive approximate small-signal transfer functions of modular DC-DC switching converters. All these small-signal characteristics will be derived based on a buck-derived converter [8].

The two approaches, namely UMT(Unified Modelling Technique) and NCT(New continuous time technique) are compared using a two-module buck-derived converter. Two peak current mode control schemes considered for this converter are:

1) the double current-mode control scheme(DCMC) as shown in Fig 2.1 and

2) Single current-mode control(SCMC) scheme as shown in Fig 2.2. In DCMC scheme, a separate feedback is applied from the output inductor current and the capacitor voltage of each module[8].

Whereas in the SCMS scheme, a single current loop and a single voltage loop is used to track the behavior of the peak current and the control voltages. The converter boxes in these figures are the constant frequency Pulse Width Modulated buck-derived DC-

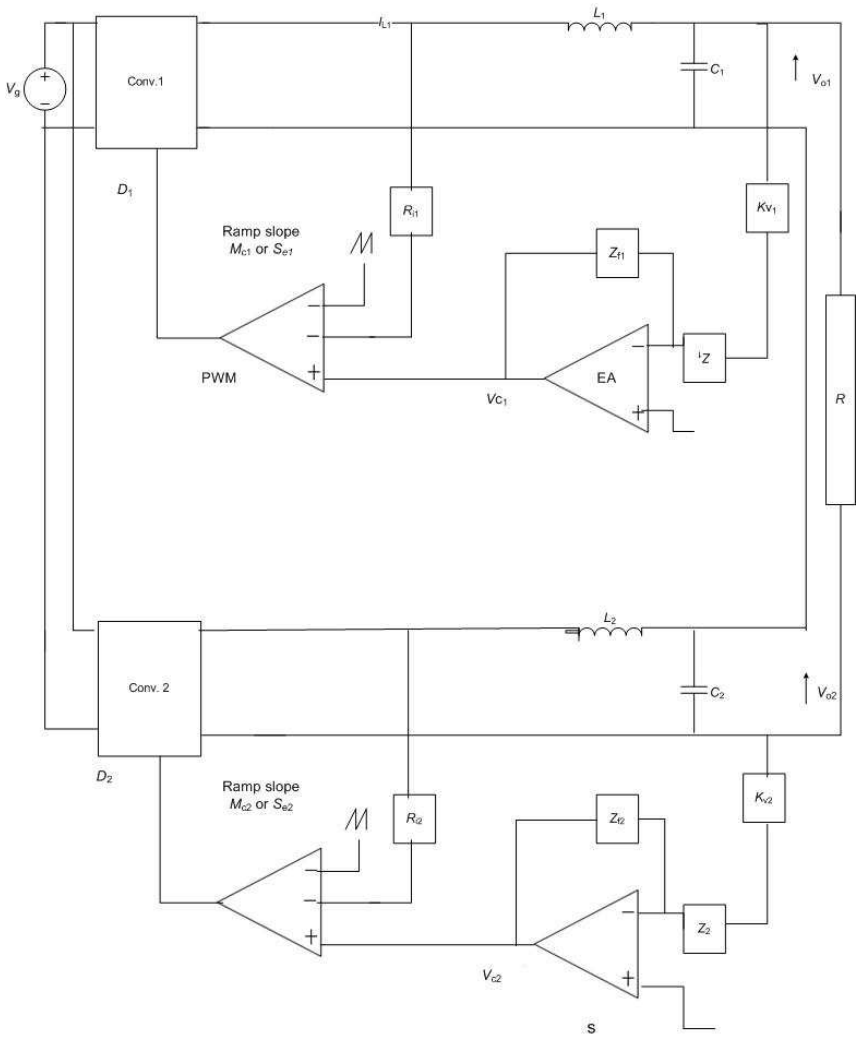


Figure 2.1: Circuit diagram of a two-module buck converter using DCMC scheme [8].

DC converters. Pulse-width modulation is provided by the use of these converters to the passive components of the circuit [8]. The approximate small-signal transfer functions can be compared for both the techniques. The comparison between the models will be based upon the design equations for determining the size of the external ramp signal. This compensation is required for providing necessary damping to the control-to-output response with the outer loop closed at 50 percent duty ratio. The two techniques are also compared based on their predictions for the current-loop gain characteristics and control-to-output response. Small-signal models are helpful

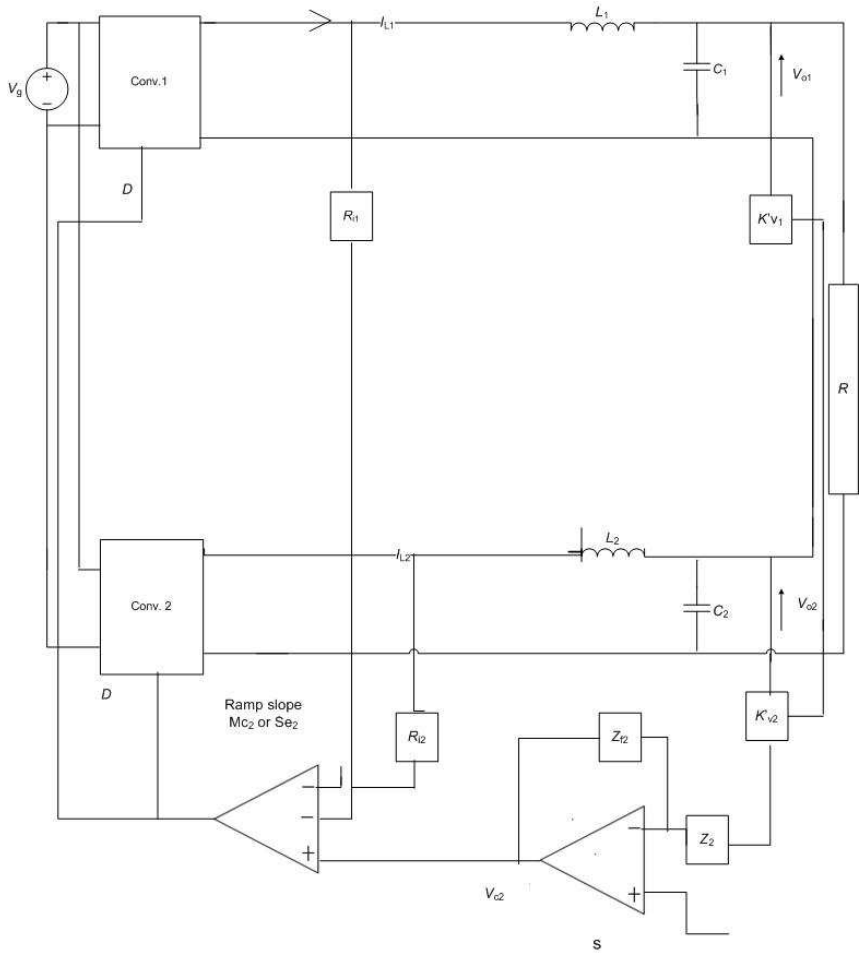


Figure 2.2: Circuit diagram of a two-module buck converter using SCMC scheme [8].

in determining the behavior of a system upto the frequency range of interest. In this case, the range of frequency of interest is upto half the switching frequency [8].

## 2.2 Small-signal Modelling of DCMC Scheme

The small-signal modelling of the current-mode control scheme was carried out based on the following assumptions.

- The two converter modules are identical.
- The transistor and the diode are ideal.

- Parasitic elements are linear,time-invariant, frequency-dependent.
- Only the continuous conduction mode of inductor current is considered.
- The diode in the on-state is modelled by a linear battery source and with a linear forward resistance; therefore, the input voltage is ripple-free. The switching components have infinite resistance during the turn-off period [8].

To derive the small-signal modelling of the Double Current-Mode Control Scheme(DCMC), each of the converter modules can be treated as the single-stage peak CMC converter with a fixed frequency. The inductor current is sensed by the resistor $R_i$ which develops a voltage $R_i i_L$. The on-time slope of its waveform is given by $M_1$ (or $S_n$ according to some other publishers). The duty cycle $D$ is determined when the voltage $R_i i_L$ reaches the values set by $V_c$. An external ramp with a slope $M_c$ (or $S_e$ according to some other publishers) is added to the sensed waveform to stabilize the inner current loop. Fig. 2.3 shows the circuit of a single-stage current-mode controlled buck converter. The waveform of the inductor current, control voltage and the external ramp required for stabilizing the inner current loop is shown in the Fig 2.4 [6],[7],[12], and [8].

Based on the Unified Modelling Technique, the small-signal duty cycle is determined based on the geometry of the steady-state inductor current waveform. Referring to the geometry of the inductor current waveform, the equation for the steady-state waveform is given by

$$I_C = I_L + \frac{M_1 DT}{2} + M_c DT, \tag{2.1}$$

$$I_L = I_C - \frac{M_1 DT}{2} - M_c DT, \tag{2.2}$$

$$I_L R_i = V_c - M_c DT - 0.5 M_1 DT. \tag{2.3}$$

For a buck-converter, the upward slope of the inductor current waveform is given by

$$M_1 = S_n = \frac{R_i V_g D'}{L}, \tag{2.4}$$

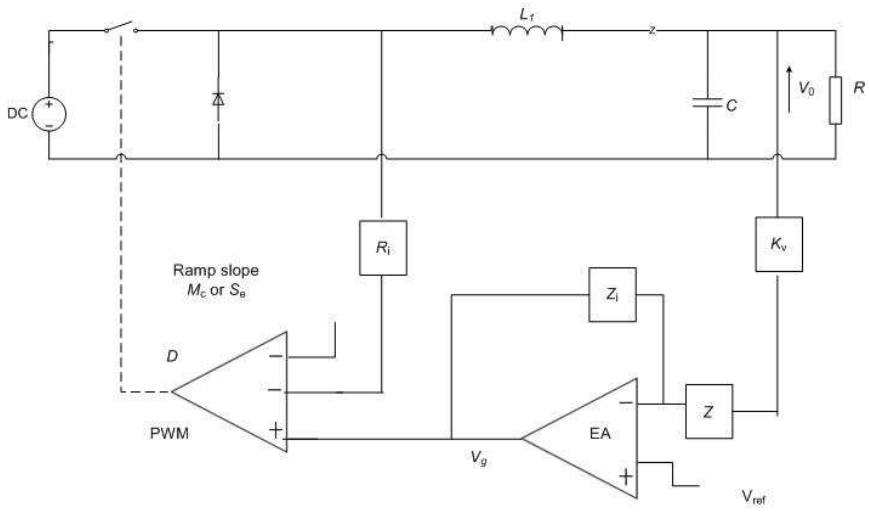


Figure 2.3: Circuit of a single-stage CMC buck converter [8].

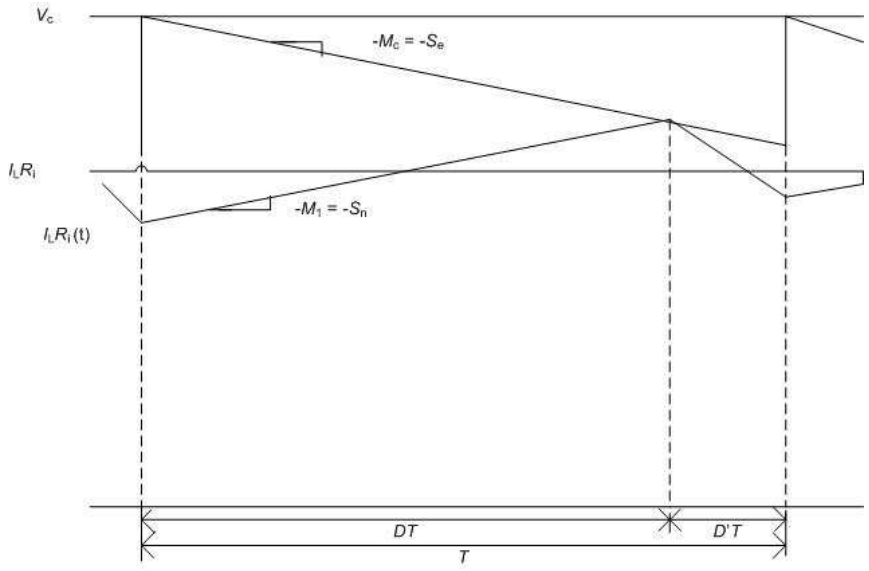


Figure 2.4: The sensed inductor current waveforms in steady state [8].

where $D' = 1 - D$ and $V_g$ is the input voltage. Using $M_1$ in the expression for $I_L R_i$, which gives [6], [7], [3], [12], [10], and [8]

$$I_L R_i = V_c - M_c DT - \frac{0.5 DD'TV_g R_i}{L}. \tag{2.5}$$

The small-signal control law for duty cycle can be derived by introducing perturbations into the above equation. The perturbation of the above equation leads to the

following expression:

$$(I_L + \hat{i_L})R_i = V_c + \hat{v_c} - M_c(D + \hat{d})T - \frac{0.5(D + \hat{d})(1 - D - \hat{d})TV_gR_i}{L}. \tag{2.6}$$

The above equation is expanded to derive the low-frequency duty law.

$$I_LR_i + \hat{i_L}R_i = V_c + \hat{v_c} - M_cDT - M_c\hat{d}T - \frac{0.5DD'TV_gR_i}{L}, \tag{2.7}$$

which gives

$$I_LR_i + \hat{i_L}R_i = V_c + \hat{v_c} - M_cDT - M_c\hat{d}T - \frac{0.5(DD' - D\hat{d} + \hat{d}D')(V_g + \hat{v_g})R_iT}{L}. \tag{2.8}$$

The small-signal component from the above expression is given by

$$\hat{i_L}R_i = \hat{v_c} - M_c\hat{d}T + \frac{0.5D\hat{d}V_gR_iT}{L} - \frac{0.5D\hat{d}D'V_gR_iT}{L} - \frac{0.5DD'\hat{v_g}R_iT}{L}. \tag{2.9}$$

Solving the above expression for $\hat{d}$, gives

$$\hat{d}\left(M_cT + \frac{0.5DV_gT}{L} + \frac{0.5D'V_gR_iT}{L}\right) = -\hat{i_L}R_i + V_c - \frac{0.5DD'\hat{v_g}R_iT}{L}. \tag{2.10}$$

If

$$k_g = \frac{-0.5DD'TR_i}{L}, \tag{2.11}$$

than

$$\hat{d} = \frac{\hat{i_L}R_i + V_c + \hat{K_g}\hat{v_g}}{M_cT - \frac{0.5DV_gR_iT}{L} + \frac{D'V_gR_iT}{L}}. \tag{2.12}$$

Now, we simplify only the denominator for the above expression, which gives

$$\frac{1}{M_cT + \frac{0.5D'V_gR_iT}{L} - \frac{0.5DV_gR_iT}{L}} = \frac{L}{M_cTL + 0.5D'V_gRiT - 0.5DV_gR_iT}, whichimplies \tag{2.13}$$

$$= \frac{L}{R_iV_gT\left(\frac{M_cLD'}{D'R_iV_g} + 0.5D' - 0.5D\right)} = \frac{L}{R_iV_gT\left(\frac{M_cD'}{M_1} + 0.5D' - 0.5 + 0.5D'\right)},$$

which gives

$$\frac{1}{M_cT + \frac{0.5D'V_gR_iT}{L} - \frac{0.5DV_gR_iT}{L}} = \frac{L}{R_iV_gT\left(D'\left(1 + \frac{M_c}{M_1}\right) - 0.5\right)}. \tag{2.14}$$

Let

$$\frac{L}{R_i V_g T\left(D'\left(1+\frac{M_c}{M_1}\right)-0.5\right)} = F_{mu}, \tag{2.15}$$

where $F_{mu}$ is the low-frequency modulator gain. Thus, the low frequency control law is given by

$$\hat{d} = F_{mu}\left(-\hat{i_L} R_i + \hat{v_c} + K_g \hat{v_g}\right). \tag{2.16}$$

From the above expression, the minimum value for $D'$ required to maintain a finite positive value for $F_{mu}$ can be given by [6], [7], [3], [12], and [10]

$$D'_{min} = \frac{0.5}{(1+\lambda)}, \tag{2.17}$$

where $\lambda$ is the slope ratio $\frac{S_n}{S_e}$.

In the above derivation, the the discrete nature of the inner loop is neglected, but for the prediction of high frequency small-signal behavior up to the frequency of interest, the sampling effect of the loop gain is taken into consideration[11]. The sampling effect is represented by the addition of a pole in the inner current loop. Therefore, the high-frequency modulator gain becomes

$$F_{mu}(s) = \frac{F_{mu}}{1+\frac{s}{\omega_p}}, \tag{2.18}$$

where

$$\omega_p = \frac{\pi^2}{T}[D'(1+\lambda)-0.5]. \tag{2.19}$$

The duty ratio law for the high-frequency small-signal model can be given by [6], [7], [3], [12], [10], [11], and [8]

$$\hat{d} = F_{mu}(s)\left[-\hat{i_L} R_i + \hat{v_c} + K_g \hat{v_g}\right]. \tag{2.20}$$

Based on these derivations, the small-signal model for this control scheme can be as shown in the Fig. 2.5. This model is based on the UMT technique.

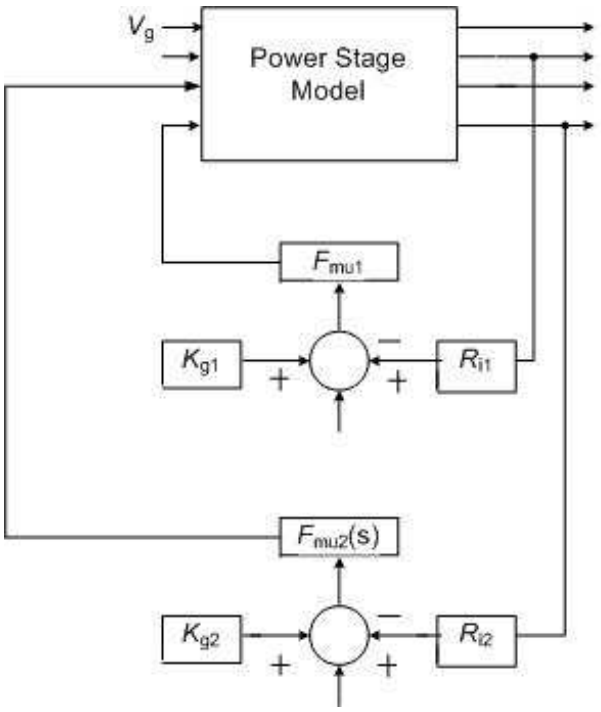


Figure 2.5: Small-signal model of DCMC scheme using unified modelling technique [8].

The similar kind of model can be derived based on the NCT technique. In this technique, the sensed inductor current of the CMC scheme is treated as the sawtooth modulator waveform similar to the voltage-mode control scheme [3] and [8]. The modulator gain for the single stage converter can therefore be written as [17], [6], and [16]

$$F_{mn} = \frac{1}{(S_n + S_e)T}. \tag{2.21}$$

The same expression holds true with the perturbation as well. Substituting the value of $S_n$ for buck converters, the above expression is modified to

$$F_{mn} = \frac{L}{R_i V_g D' T\,(1+\lambda)}, \tag{2.22}$$

where $F_{mn}$ is the modulator gain for the NCT technique, in which, $\lambda$ is the slope ratio $\frac{S_e}{S_n}$. Comparing the expression for the modulator gain for the NCT model with that for

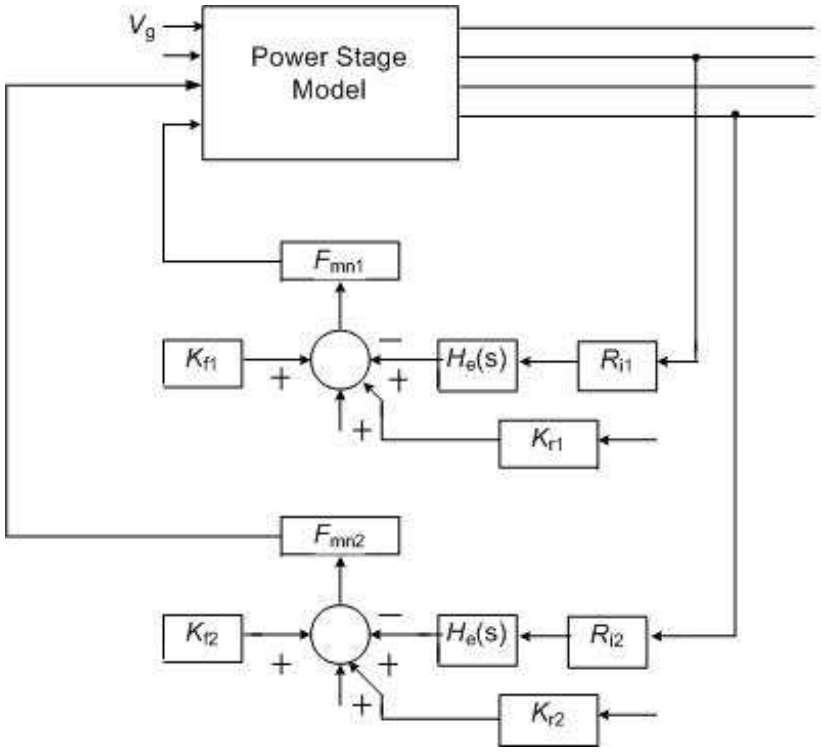


Figure 2.6: Small-signal model of DCMC scheme using the new continuous time modelling technique [8].

the UMT model, one can figure out the major difference between the two techniques. The sampling gain for the NCT technique is approximated using certain mathematical steps which is also one of the major differences between the two techniques [12], [6], and [7]. The sampling gain is is represented by two complex conjugate RHP zeros, which is given by the expression [3]

$$\hat{d} = F_{mn}[-\hat{i}_L R_i H_e(s) + v_c + K_f \hat{v_{on}} + K_r \hat{v_{off}}]. \tag{2.23}$$

$$H_e\,(s) \simeq 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}. \tag{2.24}$$

Another difference between the two techniques is that in the NCT approach, the feed-forward of the voltages is provided by the two feed-forward blocks $k_f$ and $k_r$ with the inner current loop closed [3], [8] and [6]. The values for $K_f$ and $K_r$ for the single

stage buck converter are given by

$$K_f = \frac{-DTR_s(1-\frac{1}{2})}{L}[8], \tag{2.25}$$

and

$$K_r = \frac{D'^2TR_s}{2L}[8]. \tag{2.26}$$

where $Q_z = -\frac{2}{\pi}$ and $\omega_n = \frac{\pi}{T}$ [8]. Fig. 2.6 shows the small-signal model for the two stage buck converter with Current-mode control scheme using the NCT technique. The small-signal duty ratio law for the buck converter module using this technique is given by [8] and [3] Here, $\hat{v_{on}}$ and $\hat{v_{off}}$ are the partial changes in the voltages after introducing perturbations in the model.

# 3 Current-Mode Control Scheme Using Discrete-Time Analysis

## 3.1 Introduction

As mentioned previously, Current-Mode Control has been the most popular approach for the control design of power converters. Several models have been proposed so far to characterize the current-mode control scheme with small-signal models. Most of these models had limited degrees of accuracy and a lot of inconsistencies. Some of these models provided the low-frequency model for the system but failed to deal with the current-loop instability [6]. Predictions have been made in the past to explain the sub-harmonic oscillations at a duty ratio of 0.5. But these predictions were never confirmed by the hardware measurements. Another approach was presented to predict the high-frequency behavior with a low-frequency model in which the duty cycle ratio was derived by perturbing the inductor average current in steady state [3] and [6]. The power stage model was derived using the averaging techniques of state-space. The entire model of the control scheme is derived after interfacing the duty-ratio control law model with the power stages. This leads the cross-over frequency of the inner current-loop in general to be wide-band. This implies that a low-frequency model would possibly degrade in performance. Another model, that deals with the potential deficiencies, also predicts the instability, which occurs when the duty ratio is greater than 50 percent and the external compensation is not used. In this model, a discrete-time model for the current loop is designed and it is shown that the sub-harmonic oscillations occur at one-third of the switching frequency. However, this estimate is too conservative and many models later on have shown that the peaking actually occurs at half the switching frequency [3], [6], [10], [19], [7], and [12].

The two most significant models derived during the 90's decade were:

1) Current-mode control with discrete-time analysis by Ray Ridley [3].

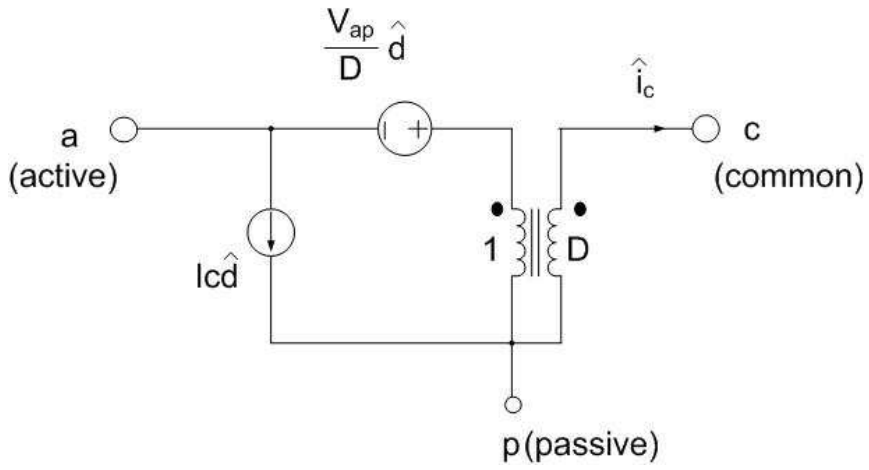


Figure 3.1: Invariant Switch Model [6].

2) Current-mode control with unified modelling scheme by Middlebrook [7].

## 3.2 Ridley's Model

Here, the small-signal model is derived using the power stages and a modulator scheme. The power stage model replaces the non-linear operation of the circuit with a linearized circuit. The invariant PWM three-terminal switching model is used to develop the power stage model as shown in Fig. 3.1 [11]. In this model, the steady state dc voltage across the terminals, and the duty ratio of the power stages determine the voltage source [3]. The dc current coming out of the common end determines the current source [6].

Power stage model is obtained by substituting the switch model in the modulator [6]. Fig. 3.2 shows the power stage model for the buck converter.

The modulation scheme used for the current-mode control scheme is shown in Fig. 3.3. The switch is turned on by a constant- frequency clock. The inductor current is sensed which generates the modulator ramp. The switch is turned off based on the control current set by the modulator. Since the modulator ramp is not enough for stability, current compensation is required by use of a compensating ramp [6].

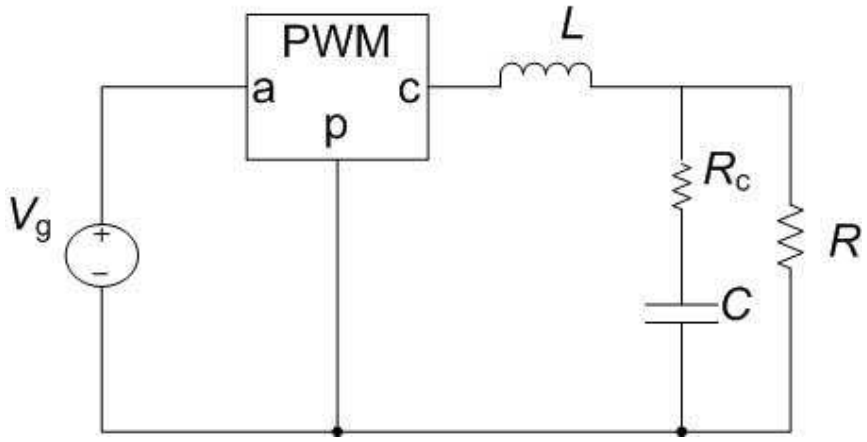


Figure 3.2: Power stage model for buck converter [6].

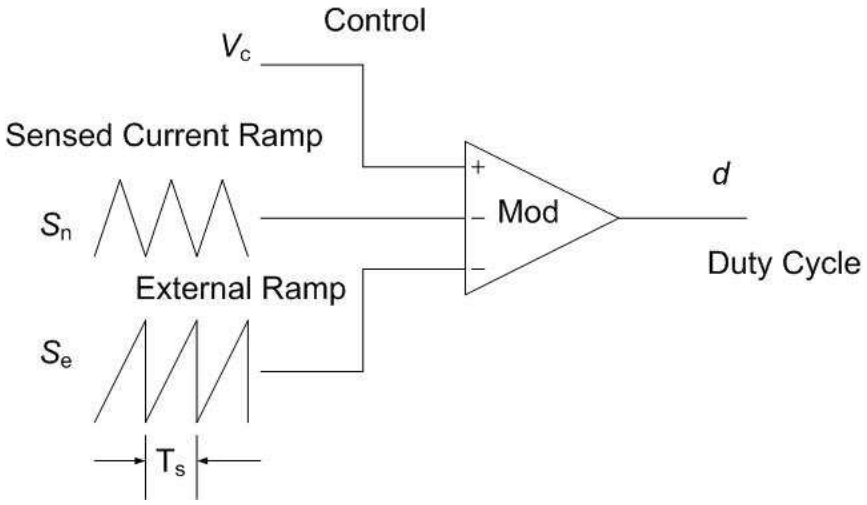


Figure 3.3: Current-mode control modulator [6].

The modulator gain for this circuit is given by

$$F_m = \frac{1}{(S_n + S_e)T_s} = \frac{1}{m_c S_n T_s}[3], [16], and[17], \tag{3.1}$$

where

$$m_c = 1 + \frac{S_e}{S_n}, \tag{3.2}$$

in which $S_n$ is the upward slope or the rising slope of the sensed current [6].

The power stage model shown before is used for designing the complete small-

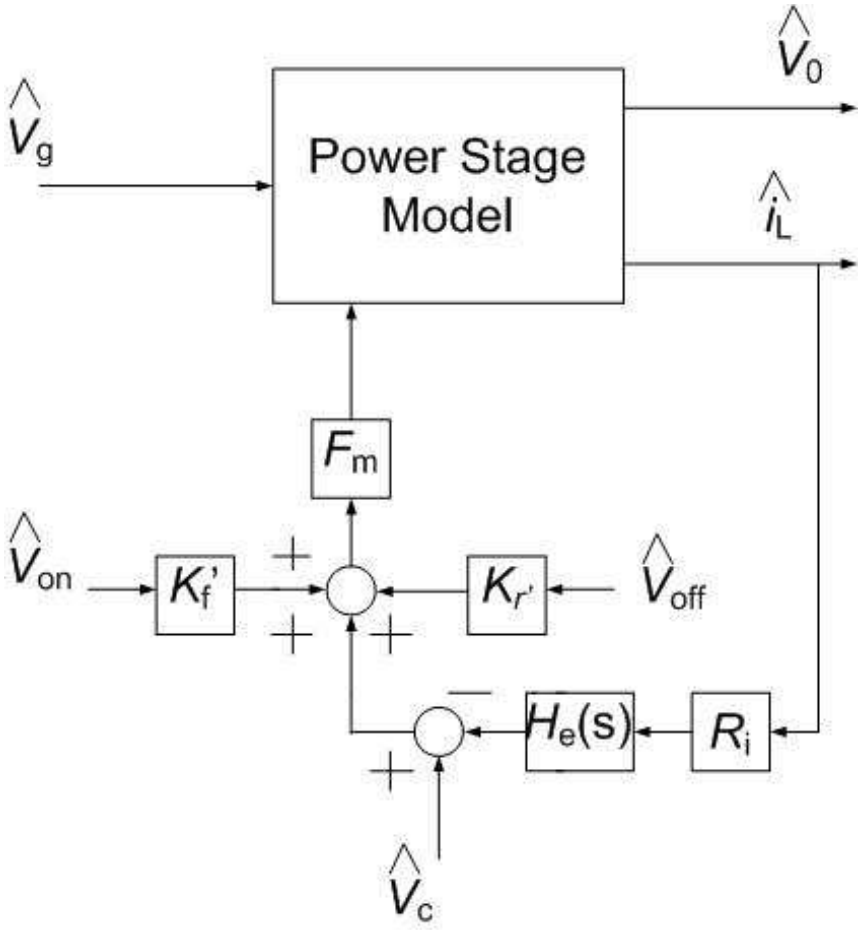


Figure 3.4: Current-mode control scheme after combining power stages with modulator [6]

.

signal model for the buck converter. The power stage model remains unaffected regardless of the control circuit. The current-mode control totally depends on the gain blocks which model the control circuit. The complete small-signal model for the current-mode control scheme of a buck converter is shown in Fig. 3.4. In this fig., $H_e(s)$ represents the current-sampling function. The current feedback path is closed and the two gain blocks $k_f'$ and $k_r'$ are created in different paths. When the switch is turned on, $k_f'$ block provides the fee-forward gain; while the switch is turned off, $k_r'$ provides the feed-forward gains [3]. $F_m$ is the modulator gain block and is affected only by the external ramp. The model described here is different from the other models

described previously, by the fact that the feed-forward blocks were directly given from the line and load sides in the previous models. This would however, render the same results for a buck converter but would give different results for different types of converters. However, the model described here is invariant of the converter topology [6] and [3].

Another significant aspect of this model is that this model is invariant of the control scheme. With zero current compensation, $R_i = 0$, resulting in the inner current loop gains to be 0. This makes it advantageous over many other control schemes. This model is not just invariant of the converter topology, but it's also the same regardless of the control scheme [3].

## 3.3 Discrete-Time Modelling

The power stage model shown previously would not require sampled-data modelling and would still render reasonably accurate transfer functions. However, in case of current-mode controlled converters, discrete-time modelling is necessary. Power stages do not involve sampled signals. The inner loop however, needs to be modelled with discrete-time analysis in order to combine with the power stages. So, in order to combine this with the other blocks of the system, it is necessary to find the sampling gain of the system [11], [3], [15], and [14].

It is necessary to find out the small signal value of the inductor current to derive the transfer function from the control voltage to inductor current. The small-signal inductor current is actually the sum of natural response of inductor current to a perturbation and the forced response of the inductor current to a unit step change in the control voltage [3], [1], [24], [25] and [10].

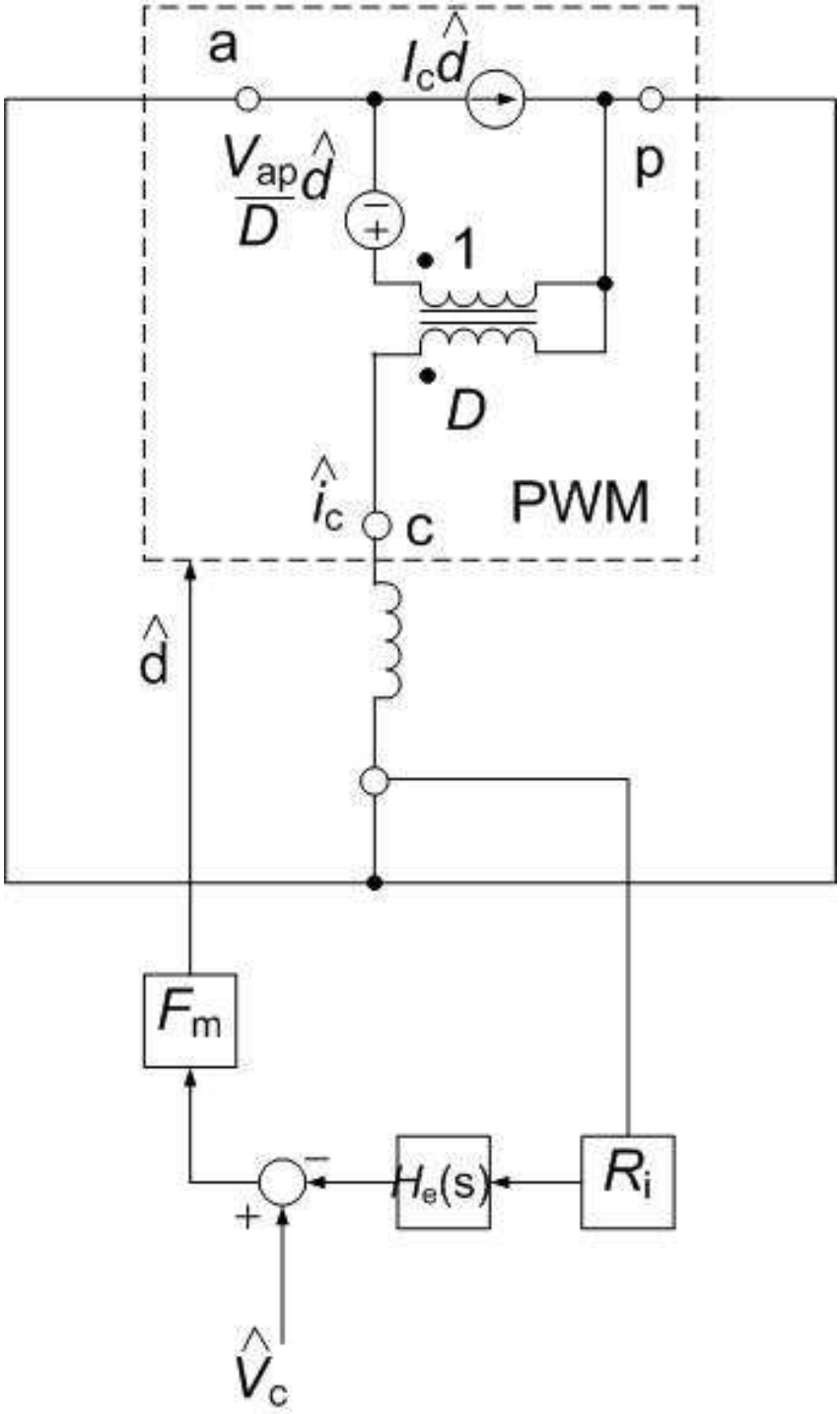


Figure 3.5: Invariant small-signal model for all types of converters [6].

### 3.3.1 Natural Response of Inductor Current to Small Perturbation in Closed-Current Loop

A small perturbation is introduced in the inductor current at the instant $t = kT_s$ with all other perturbations being zero. The sampling occurs at the instants when the two

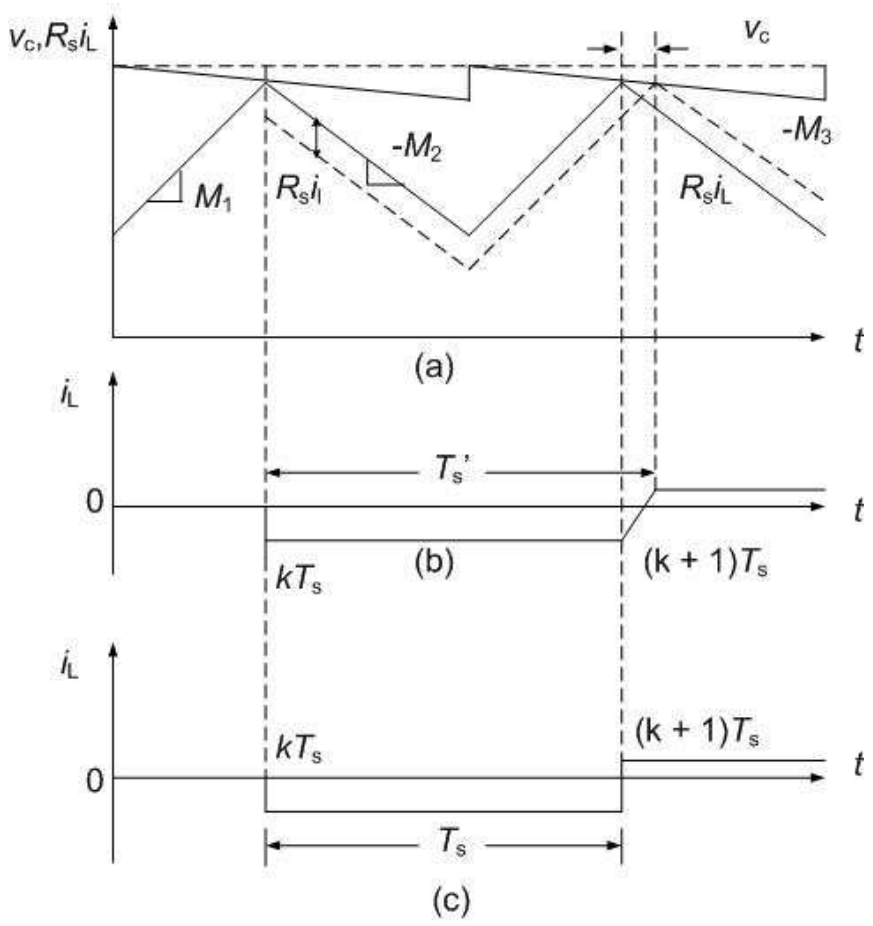


Figure 3.6: Natural response of the inductor in the closed-current loop [1].

voltages $R_s i_L$ and $v_C - v_A$ are equal. The subtraction of the perturbed waveform from the steady-state waveform would give the small-signal inductor current as shown in Fig. 3.6. This waveform can be approximated to the waveform shown in Fig. 3.7, where the finite slope after the sampling is replaced by an infinite slope. There is barely any difference between the two waveforms and hence can be ignored. This waveform is the sample-and-hold system. The time instants between the sampling instants are not constant but can be considered constant since the differences between them are too small. From the geometry of the Fig. 3.6, and the enlarged waveforms shown in Fig. 3.7 [1], [3], [24], [25] and [10],

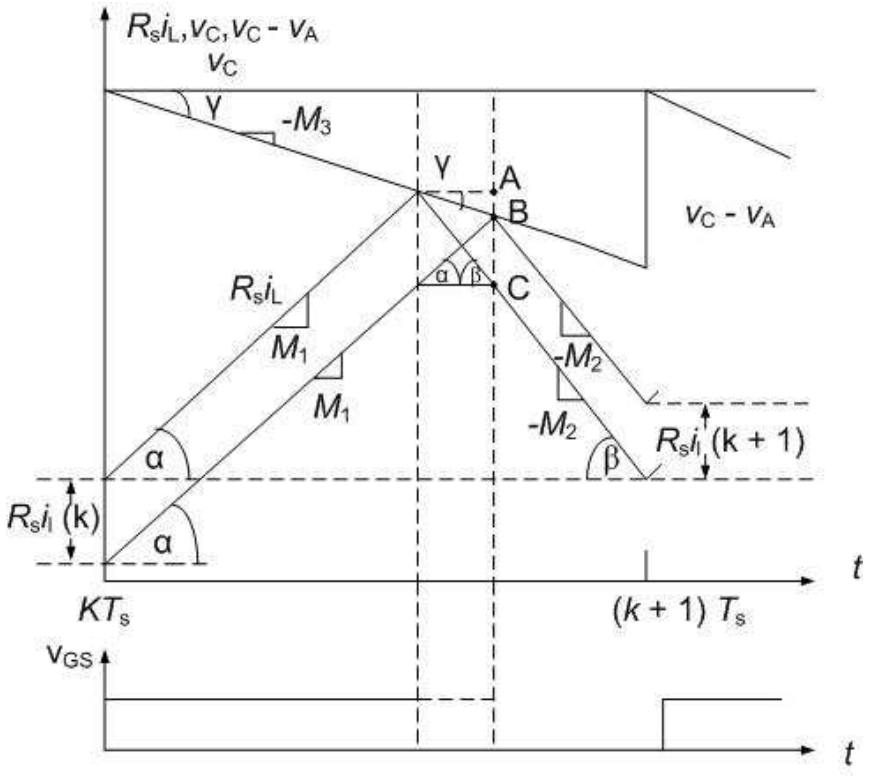


Figure 3.7: Enlarged waveform for the natural response [1].

$$M_1 = \tan\alpha = \frac{BC}{\Delta t_k} \tag{3.3}$$

and

$$M_3 = \tan\gamma = \frac{AB}{\Delta t_k}, \tag{3.4}$$

Now, the small-signal component of the inductor current at the time of the perturbation $t = kT_s$ is given by

$$R_s i_{ln}(k) = -(AB + BC) = -(M_1 + M_3)\Delta t_k. \tag{3.5}$$

Similarly,

$$M_2 = \tan\beta = \frac{AC}{\Delta t_k}, \tag{3.6}$$

So, the small-signal component at the instant $(k+1)T_s$ is given by

$$R_s i_{ln}(k+1) = AC - AB = (M_2 - M_3)\Delta t_k. \tag{3.7}$$

So, using the sampling theory, the small-signal component at the instant $t = (k+1)T_s$ is divided by the one at the instant $t = kT_s$, which gives

$$\frac{R_s i_{ln}(k+1)}{R_s i_{ln}(k)} = -\frac{(M_2 - M_3)\Delta t_k}{(M_1 + M_3)\Delta t_k} = -\frac{(M_2 - M_3)}{(M_1 + M_3)} = -a, \tag{3.8}$$

where

$$a = \frac{M_2 - M_3}{M_1 + M_3}. \tag{3.9}$$

Therefore, the discrete-time natural response of the small-signal inductor current from one sampling instant to another is given by [1], [24], [25], [10], and [3]

$$i_{ln}(k+1) = -a i_{ln}(k). \tag{3.10}$$

The variable $M_1$, $M_2$, and $M_3$ are equivalent to $S_n$, $S_f$, and $S_e$ in the continuous-time model [1], [10], and [3].

### 3.3.2 Forced Response of Inductor Current to Step Change in $V_c$ in Closed-Current Loop

Fig. 3.8 shows the forced response of the inductor current to a unit step change in the control voltage in the closed current loop. At the instant $t = kT_s$, there is a small change in the control voltage $v_C$ from $V_C$ to $V_C + v_c$ to introduce a perturbation in the in the inner loop. Since there is no change in line or load, the rising slope $S_n$ and the falling slope $S_f$ of the inductor current waveform remain constant. The sampling occurs when the control voltage reaches the value of the reference voltage. Fig. 3.9 shows the enlarged forced response [1], [24], [25], [10], and [3].

From the geometry of Fig. 3.9,

$$S_n = \tan\alpha = \frac{AB}{\Delta t_k}, \tag{3.11}$$

and

$$S_e = \tan\gamma = \frac{BC}{\Delta t_k}. \tag{3.12}$$

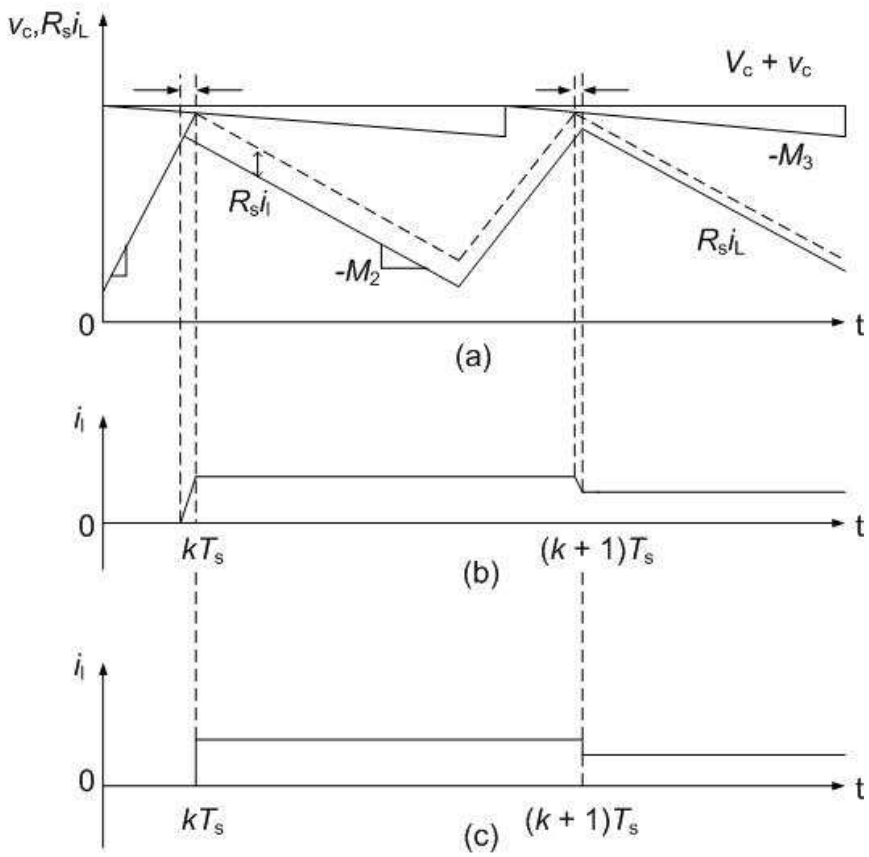


Figure 3.8: Forced response of the inductor current in the closed-current loop [1].

From the geometry of the figure, the step change in control voltage is given by

$$v_c(k+1) = AB + BC = (M_1 + M_3)\Delta t_k. \tag{3.13}$$

The falling slope is given by

$$S_f = \tan\beta = \frac{BD}{\Delta t_k}, \tag{3.14}$$

which gives the small-signal inductor current at the instant $t = (k+1)T_s$. This is given by

$$R_s i_{lf}(k+1) = AB + BD = (M_1 + M_2)\Delta t_k. \tag{3.15}$$

Now using the sampling theory, the discrete time forced response can be derived as,

$$\frac{R_s i_{lf}(k+1)}{v_c(k+1)} = \frac{(S_n + S_f)\Delta t_{k+1}}{(S_n + S_e)\Delta t_{k+1}} = \frac{(S_n + S_f)}{(S_n + S_e)} = 1 + \frac{(M_2 - M_3)}{(M_1 + M_3)} = 1 + a. \tag{3.16}$$

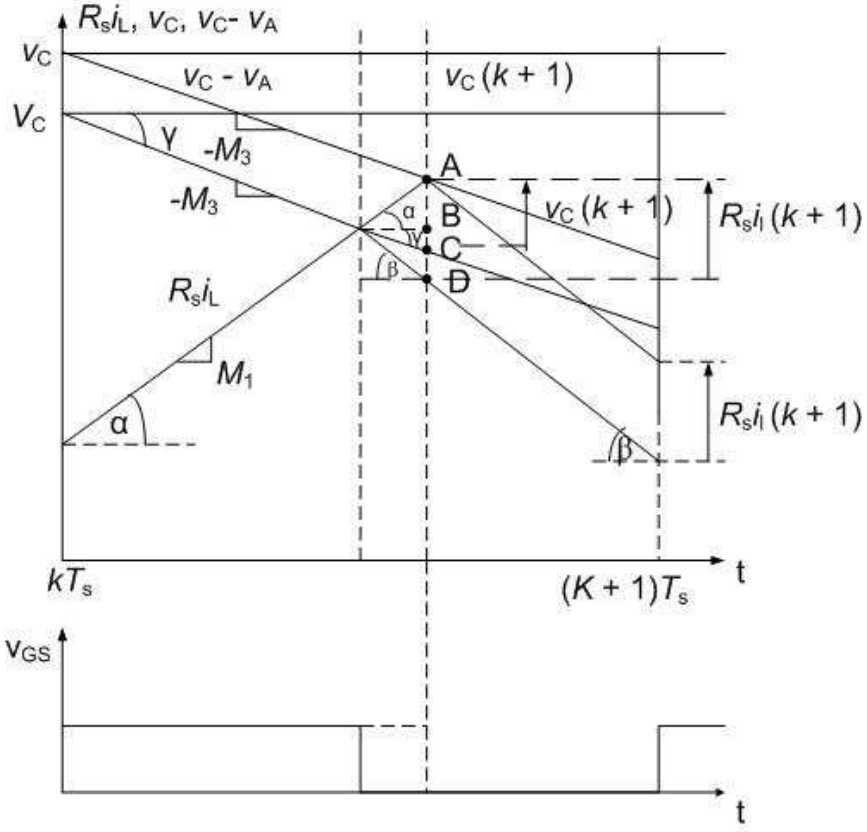


Figure 3.9: Enlarged waveform for the forced response of inductor current [1].

Therefore, the discrete-time forced response for the inductor current is given by [3]

$$i_{lf}(k+1) = \frac{1+a}{R_s} v_c(k+1). \tag{3.17}$$

The total discrete-time response for the inductor is the sum of the natural response and the forced response, which is given by [1], [3], [24], [25], and [10]

$$i_l(k+1) = i_{ln}(k+1) + i_{lf}(k+1) = -a i_l(k) + \frac{1+a}{R_s} v_c(k+1). \tag{3.18}$$

### 3.3.3 Transfer Function of Closed-Current Loop

Using the definition of z-transform, the discrete-time inductor current in the z-domain is given by [1]

$$Z\{i_l(k)\} = i_l(z) = \sum_{k=0}^{\infty} i_l(k)z^{-k} = i_l(0)+i_l(1)z^{-1}+i_l(2)z^{-2}+....+i_l(k)z^{-k}+...., \quad (3.19)$$

using the shifting theorem [1],

$$Z\{i_l(k+1)\} = zi_l(z) \quad (3.20)$$

and

$$Z\{v_c(k+1)\} = zv_c(z) \quad (3.21)$$

Therefore, the z-transform of the total discrete-time response is given by [1]

$$zi_l(z) = -ai_l(z) + \frac{1+a}{R_s}zv_c(z). \quad (3.22)$$

Hence,

$$(z+a)i_l(z) = \frac{(1+a)z}{R_s}v_c(z). \quad (3.23)$$

Thus, the discrete-time transfer function from control voltage-to-inductor with inner loop closed and outer voltage loop open, is given by [1], [3], [24], [25], and [10]

$$H_{icl}(z) = \frac{i_l(z)}{v_c(z)} = \frac{1+a}{R_s}\frac{z}{z+a} = \frac{1+a}{R_s}\frac{z}{z-p}. \quad (3.24)$$

According to the definition, the transformation from the z-domain representation to the continuous-time representation of the current-mode control system is given by [20], [3]

$$F(s) = H(e^{sT_s})\frac{1}{sT_s}(1-e^{-sT_s}). \quad (3.25)$$

Using the above definition, the transfer function from control voltage to the inductor current, with the inner loop closed, is given by [1]

$$F(s) = \frac{\hat{i_L}(s)}{\hat{v_s}(s)} = \frac{1}{R_i}\frac{1+a}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+a}. \quad (3.26)$$

This model is highly complex and hence is never used in this form. Instead, approximate averaged models are often used. The model proposed by Ridley was approximated such that it is accurate upto half the switching frequency. Since, the closed-loop, continuous time model has been already found, what is needed is the open loop model to derive the expression for $H_e(s)$. The modulator gain $F_m$ is same as the one derived for voltage-mode control scheme. For current-mode control scheme, the ramp is formed by the sensed inductor current, and an external ramp, $S_e$, in case of constant-frequency controlled converter with controlled on-time, the modulator gain is still derived the same way. The modulator gain for constant-frequency controlled converter is given by the reciprocal of the height of the ramp that would be obtained if the modulator signal continued with the slope $S_n + S_e$ towards the completion of one period. The modulator gain is given by [1], [24], [25], [10], and [3]

$$F_m = \frac{1}{S_n + S_e)T_s}. \tag{3.27}$$

The modulator gain for constant-frequency control, with the off-time clock is given by [1], [10], and [3]

$$F_m = \frac{1}{(S_f + S_e)T_s}. \tag{3.28}$$

The modulator gain for constant-frequency control with a naturally-sampled control signal is $F_c = 1$ since there is no frequency dependence of modulator gain. The transfer function from duty cycle to inductor current can be derived using the same small-signal [3]. Now, the switch model and the complete model gives [3]

$$F_i(s) = \frac{\hat{i_L}(s)}{\hat{d}(s)} = \frac{V_{ap}}{sL}. \tag{3.29}$$

And from the figure, we can see that $V_{ap} = V_{ac} + V_{cp}$, also $S_n = \frac{R_i V_{ac}}{L}$ and $S_f = \frac{R_i V_{cp}}{L}$ [3], this expression can be re-written in terms of the rising and falling slopes as

$$F_i(s) = \frac{1}{R_i} \frac{S_n + S_f}{s}. \tag{3.30}$$

The product of the modulator gain $F_m$ and the current gain $F_i(s)$ is now a single expression for all the converters and is given by

$$F_m F_i(s) = \frac{1}{R_i} \frac{1+a}{sT_s}. \tag{3.31}$$

Using the standard formula for closed-loop expression, the open-loop gain term $H_e(s)$ can now be found. The closed-loop expression is given by [3]

$$\frac{1}{R_i} \frac{1+a}{sT_s} \frac{e^{sT_s} - 1}{e^{sT_s} + 1} = \frac{F_m F_i(s)}{1 + F_m F_i(s) R_i H_e(s)}. \tag{3.32}$$

Substituting the value of $F_m F_i(s)$ from previous expression, the expression for $H_e(s)$ is given by [1], [10], [11] and [3]

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1}. \tag{3.33}$$

This expression is not only invariant of the converter-type but also invariant for the control scheme.

## 3.4 Continuous-Time Approximation to Discrete-Time Model

The continuous-time model shown before has a current-sampling function that cannot be bound into finite limits of poles and zeros. This model is inconvenient for analysis of the current-mode system since it contains an exponential term in s-domain. A second-order approximation was subsequently been made to the sampling gain to model a system which is accurate upto half the switching frequency. The approximation is a second-order polynomial which can help in deriving the transfer function for the design purpose. Fig. 3.10 shows the location of poles and zeros of the actual transfer function [3], [6], [11], [12], and [19].

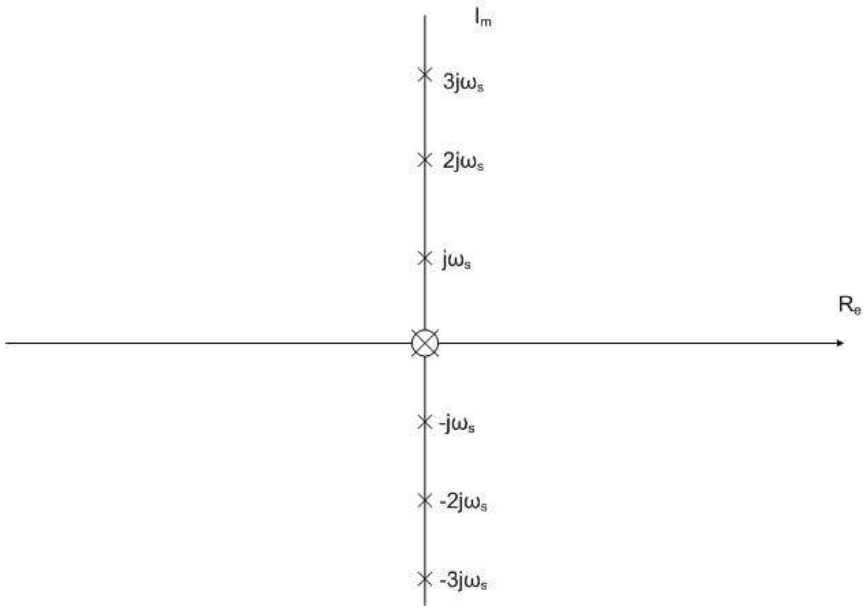


Figure 3.10: Pole Zero Location of the sampling gain [3].

These poles are derived using the condition,

$$H_e(s_p) = \frac{s_p T_s}{e^{s_p T_s} - 1} = \infty. \tag{3.34}$$

The finite solution for this condition is given by [3] and [11]

$$e^{s_p T_s} = 1. \tag{3.35}$$

This condition is satisfied at frequencies which are integer multiples of the switching frequency. The exponential expression above can be approximated to a continuous-time transfer function with the same poles and zeros in a polynomial form. And then, the lower frequency poles could be retained to make an approximation for the lower frequencies. However, this approach is not satisfactory for modelling since it would result in poor phase characteristics. The main reason why the model needs to be simplified is that the sampling gain should be close enough to the gain and phase characteristics of the transfer function upto the frequency of interest. The discrete-time model requires that the model should be legit upto the Nyquist frequency, which

is equal to half the switching frequency [3] and [11].

Several approaches can be taken to derive this transfer function. However, there are some specific requirements related to current-mode control. The transfer function should match exactly at the DC frequency. Also, current-mode control has inherent problem of oscillation exactly at a 50 percent duty ratio. So, the approximated transfer function should be exact at half the switching frequency [3].

$H_e(s)$ exhibits a change in phase from 0 to -90 at a duty ratio of 50 percent, and a change in gain of about 4 DB. An approximate expression is chosen such that

$$H_e(s) \simeq 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}. \tag{3.36}$$

This approximate transfer function is equal to unity at dc frequency, i.e at $s = 0$, $H_e = 1$. The parameters $\omega_n$ and $Q_z$ can be chosen such that [3], [11], and [6]

$$Q_z = \frac{-2}{\pi} \tag{3.37}$$

and

$$\omega_n = \frac{\pi}{T_s}. \tag{3.38}$$

These parameters meet the requirements for the buck converter at half the switching frequency. Fig. 3.11 and 3.12 shows the small-signal characteristics for the approximate second-order model which is accurate upto the frequency range of interest, which in this case is from dc to the nyquist frequency.

The gain does not deviate from the exact expression by 0.2 dB, and the phase does not deviate by more than 3 degrees, which is reasonably accurate [6].

## 3.5 Complete Continuous-Time Model with Feed-forward Gains

The discrete-time model derived previously was for the simple current-mode control scheme with fixed input and output voltages. A complete continuous time model can be derived by allowing perturbations in these voltages. As shown previously,

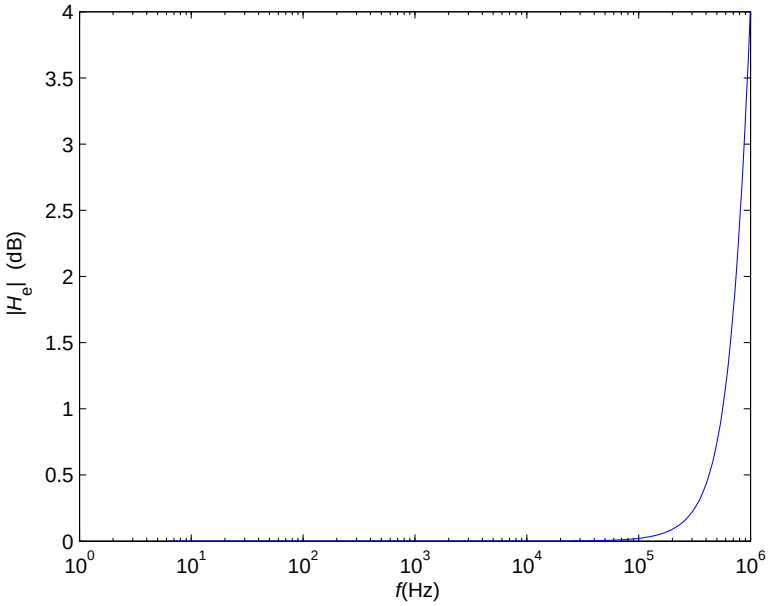


Figure 3.11: Gain of the sampled data model.

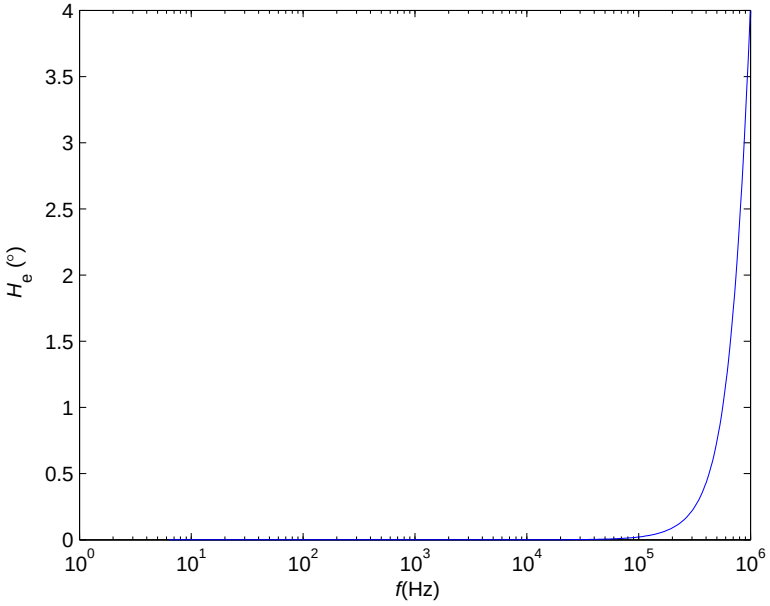


Figure 3.12: Phase of the sampled data model.

it was seen that perturbations away from the steady-state of the peak current lead to perturbations which were held constant over the whole switching cycle. It was not important that the peak current was the controlled quantity. However, when

deriving the complete model, the fact that the average current is different from the peak current is significant. The average current in steady-state is equal to the peak current minus or plus half the ripple current, depending on the control scheme being used. Ripple current is a function of the duty cycle, line and load voltage of the current cell. With the changes in line and load voltages, there will be changes in average current value [3] and [6].

The complete small-signal model shown previously is used to model the effect of input and output voltages. Feed-forward gains from the line and load sides to the duty cycle must also be included in the model [3]. Modulator gain has been arbitrarily included in the feed-forward path for simplifying the expressions for the feed-forward terms. This choice gives expressions independent of modulator gain parameters. In this model, the feed-forward gains are introduced from the inductor on-time voltage and off-time voltage via $k'_f$ and $k'_r$, respectively. This model is invariant of the converter topology as well as the control scheme. The feed-forward gains can be found from the steady-state equation that relates the average and peak inductor currents [3] and [6].

The expression for inductor current containing the control voltage, switching period, and the external ramp, for constant off-time, is given by [3]

$$R_i < i_L >= v_c - dT_s S_e - \frac{S_f d' T_s}{2}. \tag{3.39}$$

For the control during the transistor on-time, the describing function is given by [3] and [6]

$$R_i < i_L >= v_c + d' T_s S_e + \frac{S_f d' T_s}{2}. \tag{3.40}$$

Where, $< i_L >$ is the inductor average current without any perturbations. Fig. 3.4 shows the small-signal model used for the prediction of characteristics. For the small-signal model, the expressions for the duty cycle and falling inductor current

slope is given by [3] and [6]

$$d = \frac{v_{off}}{v_{on} + v_{off}}. \tag{3.41}$$

$$d' = \frac{v_{on}}{v_{on} + v_{off}}, \tag{3.42}$$

and

$$S_f = \frac{v_{off} R_i}{L}. \tag{3.43}$$

For constant-frequency, trailing-edge control [3], [17], and [16],

$$F_m = \frac{1}{(S_n + S_e)T_s}, \tag{3.44}$$

and the feed-forward gain was found to be [3]

$$k'_f = \frac{-DT_s R_i}{L}\left[1 - \frac{D}{2}\right]. \tag{3.45}$$

Using the similar procedure, the feed-forward gain from the off-time voltage is given by [3]

$$k'_r = \frac{D'^2 T_s R_i}{2L}. \tag{3.46}$$

# 4 Predictions of the Complete Small-Signal Model

## 4.1 Buck Converter for Example

The small-signal characteristics are plotted using the example of a buck converter. A buck converter with the following values of the circuit elements is used as an example: $V_g = 11$ V, $V_0 = 5$ V, $L = 37.5$ $\mu$H, $C = 400$ $\mu$F, $R = 1$ $\Omega$, $R_c = 14$ m$\Omega$, $R_i = 0.33$ $\Omega$, $F_s = 50$ kHz, and $D = 0.45$ [3] and [6].

## 4.2 Open-Loop Characteristics

The loop gain of the system is studied to ensure that the system is stable for all conditions. Fig. 4.1 shows the model modified from the complete model to derive the current loop gain. The load current is fed back through the resistor $R_i$. For the closed current loop, a feedback block $k_r$ is shown in the figure. The effect of this block is only to be seen at low frequencies. The feed-forward gain $k_f$ shown previously is not shown because the input voltage perturbations are zero when deriving the current loop gain [3] and [6]. With both of these gains ignored, the approximate expressions for the current loop gain, $T_s$, is given by

$$T_i(s) \simeq \frac{L}{RT_s m_c D'} \frac{1 + sCR}{\Delta(s)} H_e(s). \tag{4.1}$$

Where $\Delta(s)$ is the denominator of the power stage transfer function from the invariant switch model combined with the passive components to form the buck converter. This is given by [3] and [6]

$$\Delta(s) = 1 + \frac{s}{\omega_0 Q_{ps}} + \frac{s^2}{\omega_0^2}, \tag{4.2}$$

where

$$\omega_0 = \frac{1}{\sqrt{LC}}, \tag{4.3}$$

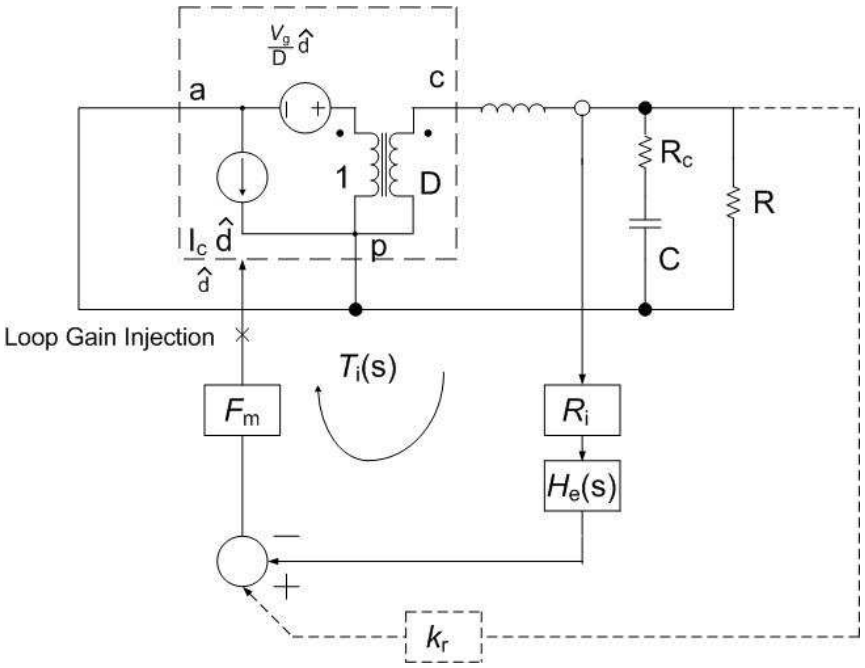


Figure 4.1: Current loop of buck converter [3].

and

$$Q_{ps} = \frac{1}{\omega_0 \left[\frac{L}{R} + CR_c\right]}. \tag{4.4}$$

This model differs from the other averaged models by the dc gain, and the presence of the sampling gain, $H_e(s)$. The predictions for the current loop shows that the model has a zero in the dc frequency range, and a pair of complex conjugate poles at a 50 percent duty cycle. The dc gain of the current loop is inversely proportional to $m_c$. Fig. 4.2 and 4.3 shows the open loop characteristics with different values of $m_c$ at a given frequency and duty ratio. The sampling gain introduces a pair of complex complex conjugate zeros in the right half of s-plane, which causes the gain of the loop to become flat at a 50 percent duty cycle, and the phase to drop an additional ninety degrees at this point [3] and [6].

With the increase in the duty cycle, the gain also increases. And after a certain level, the gain increases to a level when the system exhibits oscillations at duty ratio of 0.5 [3], citeridleypaper, and [1]. This model characterizes the instability of the

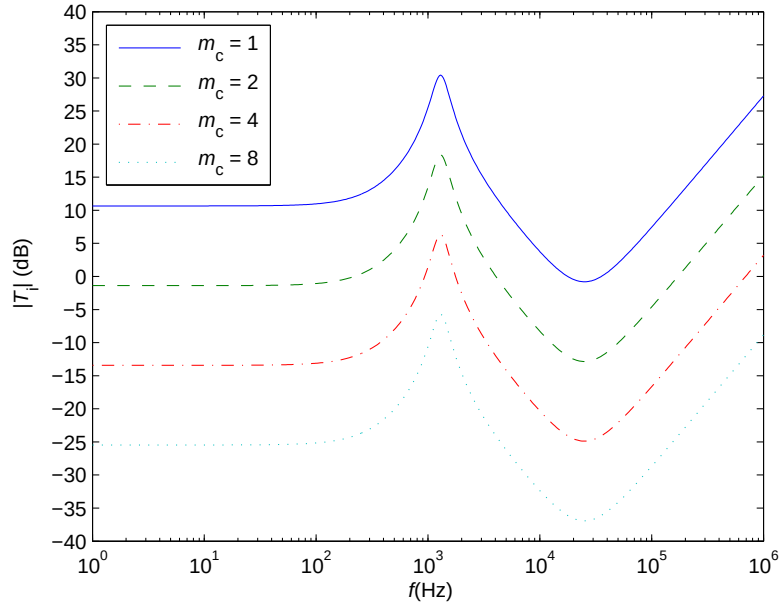


Figure 4.2: Open loop gain of buck converter.

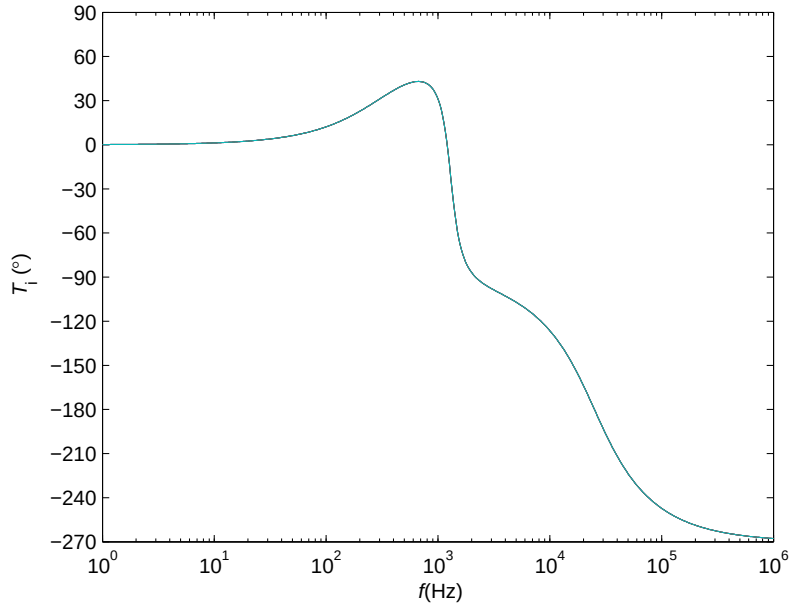


Figure 4.3: Open loop phase of buck converter.

current-loop at 50 percent duty ratio with a small phase margin as the instability is approached. Above the peaking frequency of the power stages, the loop gain is approximated by [3] and [6]

$$T_i(s) \simeq \frac{F_s}{m_c D'} H_e(s). \tag{4.5}$$

This high-frequency transfer function is same for all the power stages when a constant frequency control is used. A proper average model of the current mode system would produce the same transfer function equation as shown previously, with the sampling gain $H_e(s) = 1$, is given by [3] and [6]

$$T_i^{ave} \simeq \frac{1}{s} \frac{F_s}{m_c D'}. \tag{4.6}$$

The slope of this transfer function is -1 and has a crossover frequency of $f_s = \frac{F_s}{2\pi m_c D'}$. The crossover frequency becomes $\frac{F_s}{\pi}$ with no external ramp and at a duty ratio of 50 percent. Therefore, the system goes unstable at about one-third the switching frequency according to the averaged model. No model should predict a crossover frequency in excess of half the switching frequency, since this would exceed the Nyquist frequency. The open loop characteristics of the converter show how the external ramp of the system should be selected based upon the desired phase margin and crossover frequency. However, many designers find this way of selecting the external ramp as inconvenient because it is more easier to select the appropriate levels of compensation using the transfer function from $V_c$ to $V_o$ [3] and [6].

## 4.3 Control-to-Output Gain

Fig. 4.4 shows the small-signal model for derivation of transfer function from control-to-output of the control scheme with the inner loop being closed. The input control parameter is the voltage $\hat{v}_c$ for the closed current loop. The stability of the current loop can be assessed by looking at the characteristics of this transfer function [3] and [6]. The approximate control-to-output transfer function with inner loop closed and outer voltage loop open, is given by [3] and [6]

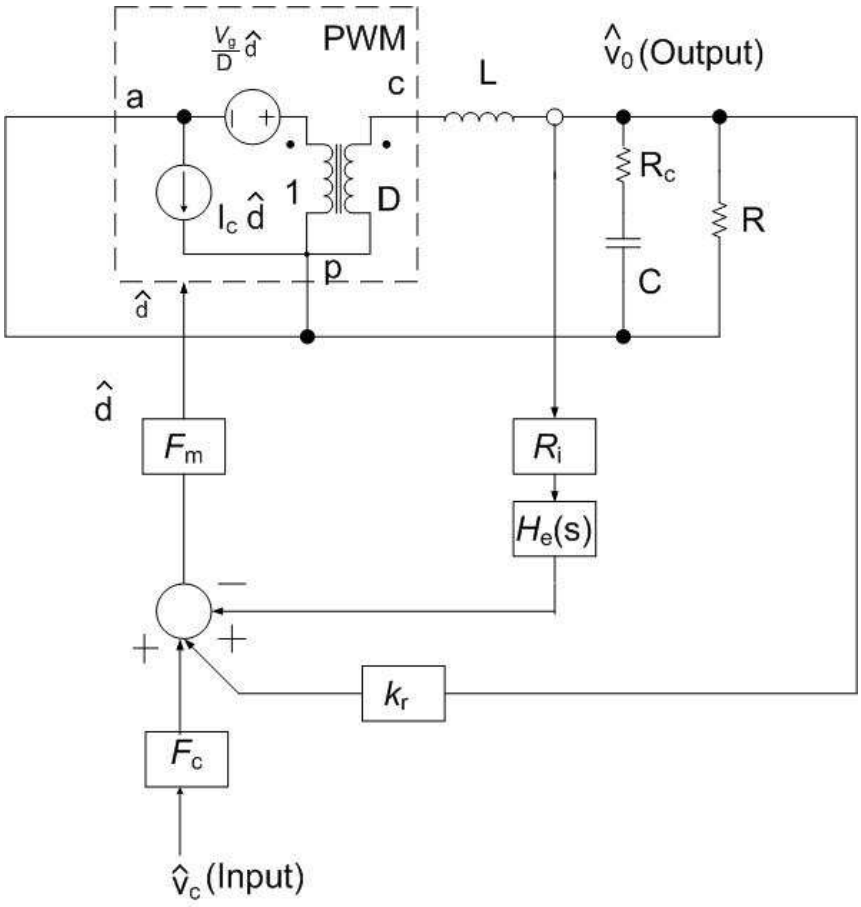


Figure 4.4: Buck-converter with current-loop closed [3].

$$\frac{\hat{v}_0}{\hat{v}_c} \simeq \frac{R}{R_i}\frac{1}{1+\frac{RT_s}{L}[m_cD'-0.5]}F_p(s)F_h(s)[3]and[6]. \tag{4.7}$$

Where

$$F_p(s) = \frac{1+sCR_c}{1+\frac{s}{w_p}}[3]and[6], \tag{4.8}$$

$$w_p = \frac{1}{CR} + \frac{T_s}{LC}(m_cD'-0.5)[3]and[6], \tag{4.9}$$

$$F_h(s) = \frac{1}{1+\frac{s}{w_nQ_p}+\frac{s^2}{w_n^2}}[3]and[6], \tag{4.10}$$

and

$$Q_p = \frac{1}{\pi(m_cD'-0.5)}[3]and[6]. \tag{4.11}$$

The transfer function $F_p(s)$ gives the low-frequency characteristics of the system. In most average models, the high-frequency effects are ignored and the closed loop is characterized by only this expression. However, this model overcomes that drawback and effectively shows how the low-frequency pole moves to a higher frequency as more compensation is introduced into the system. $F_h(s)$ gives a pair of complex conjugate poles at a 50 percent duty ratio, and the quality factor, $Q_p$, of this double pole depends on the duty ratio of the converter and the external ramp. This pole pair is produced by the complex RHP zeros in the closed current loop due to the sampling action on the system [3] and [6].

Fig. 4.5 and 4.6 shows the characteristics of control-to-output transfer function for different values of $m_c$. Fig. 4.7 and 4.8 shows the pole locations of the system without any compensation. The poles at half the switching frequency($D = 0.5$) are always complex and located on the imaginary axis. For $D = 0$, the poles have a $Q_p = \frac{2}{\pi}$. As the duty cycle increases towards $D = 0.5$, these poles move towards the imaginary axis and approaching $Q_p = \infty$. For the duty cycles higher than 0.5, they move towards the right-half plane [3] and [6].

As more compensation is introduced into the system, the pole starts moving closer to the real-axis. They eventually split into two poles on the left half of s-plane. One of them moves out to higher frequency levels upto infinity and the other moves in towards the frequency where peaking occurs. When sufficient compensation is added to the system to reduce the current loop gain to a point where the gain at the resonant frequency is less than 1, this pole combines with the low frequency poles of $F_p(s)$ to provide the resonant-frequency poles characteristics of voltage-mode control. This is the limiting case for the accuracy of the control-to-output transfer function. So, effectively, this model is not only independent of the converter topology, but also it is independent of the type of control [3] and [6].

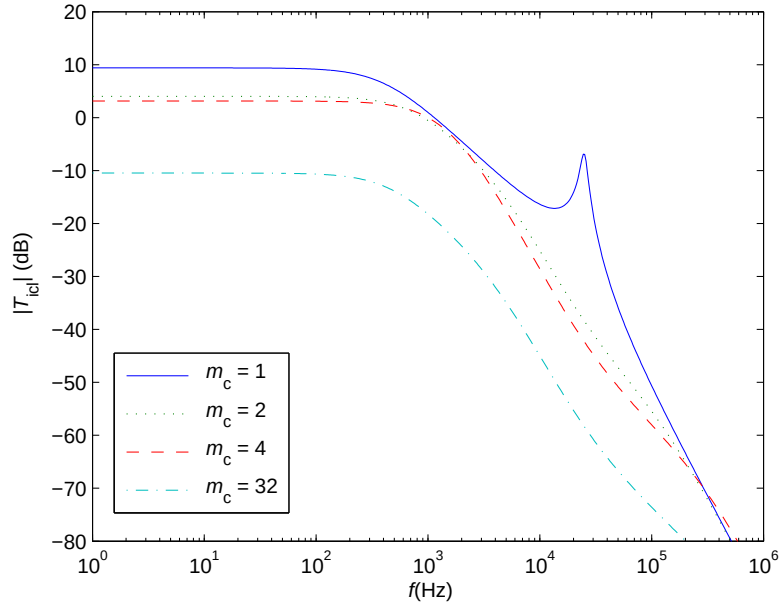


Figure 4.5: Closed-loop gain of buck converter.

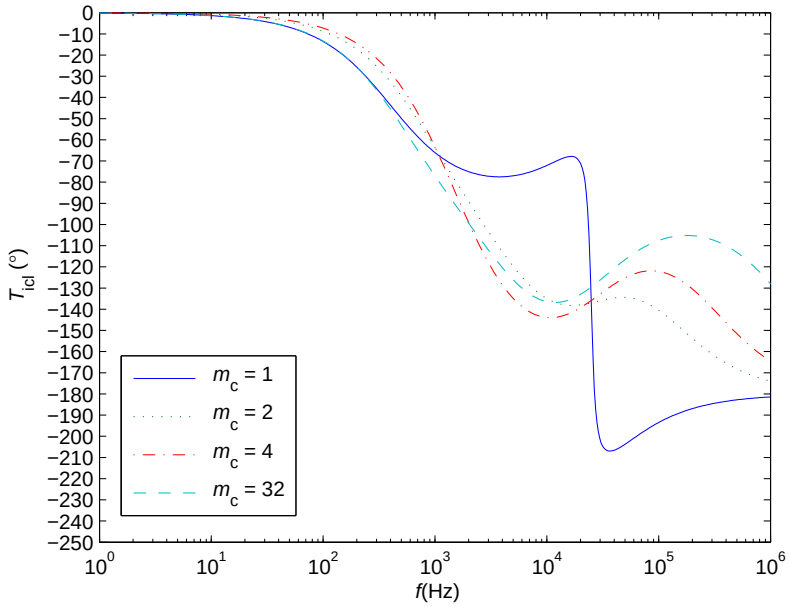


Figure 4.6: Closed-loop phase of buck converter.

## 4.4 Audio Susceptibility

The same small signal model is chosen to show the audio susceptibility of the converter. Fig. 4.9 shows the diagram used to derive the audio transfer function. The

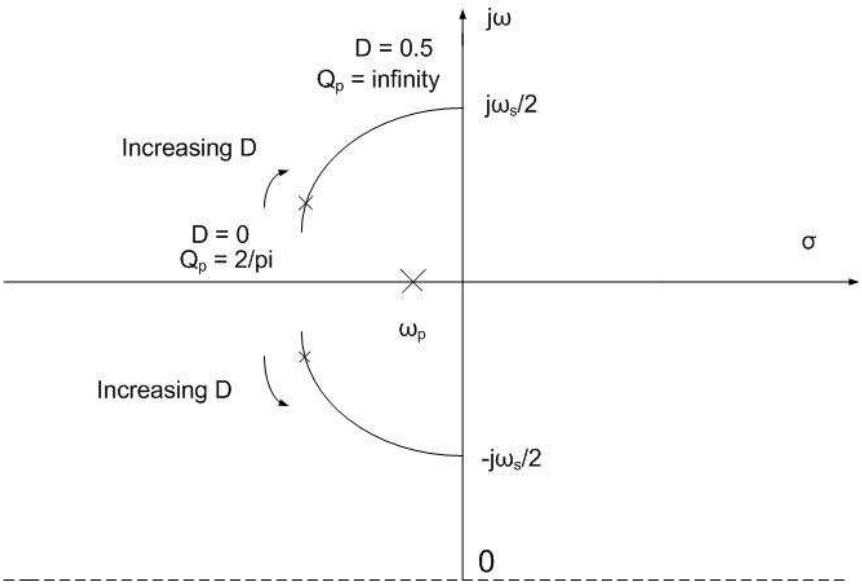


Figure 4.7: Movement of poles without any ramp [3].

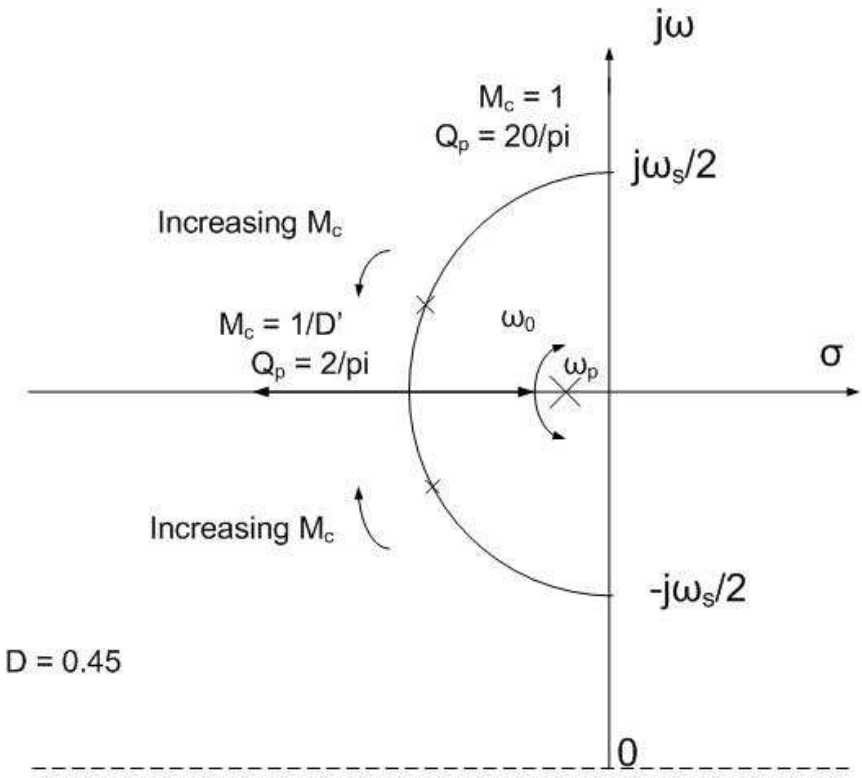


Figure 4.8: Movement of poles with external ramp [3].

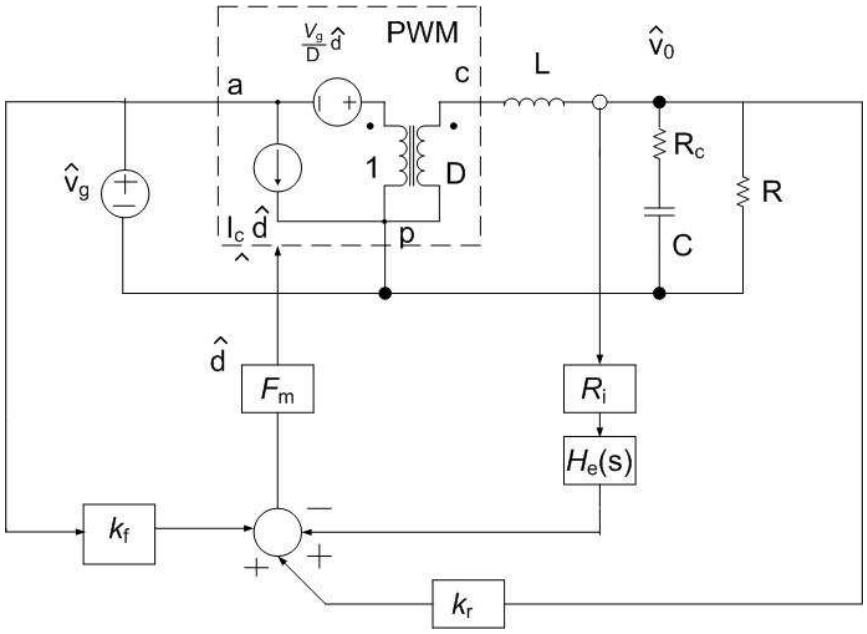


Figure 4.9: Converter system with current-loop closed and input perturbation [3].

input voltage perturbations can be fed into the power stage by two mechanisms. The first way is to feed perturbations through the power stage, where the input source, $\hat{v}_g$, is connected to the small-signal transformer. Another way is into the duty cycle perturbation, $\hat{d}_s$, via the feed-forward gain term, $k_f$. The feed-forward term is negative and the controlled source is in series with the input voltage source in the small-signal model. And because of that, it is possible to have conditions in the circuit where the net effect of line variations is nullified on the load side. [3] and [6].

The approximate transfer function for audio-susceptibility of the buck converter is given by [3] and [6]

$$\frac{\hat{v}_0}{\hat{v}_g} = \frac{D[m_c D' - (1 - D/2)]}{\frac{L}{RT_s} + (m_c D' - 0.5)} F_p(s) F_h(s). \tag{4.12}$$

Notice that the numerator of the dc gain is a difference of two terms. That means, voltage perturbations at the input can be nullified with the output voltage perturbations of the buck converter circuit $m_c$ [3]. Figure 4.10 shows the plots of

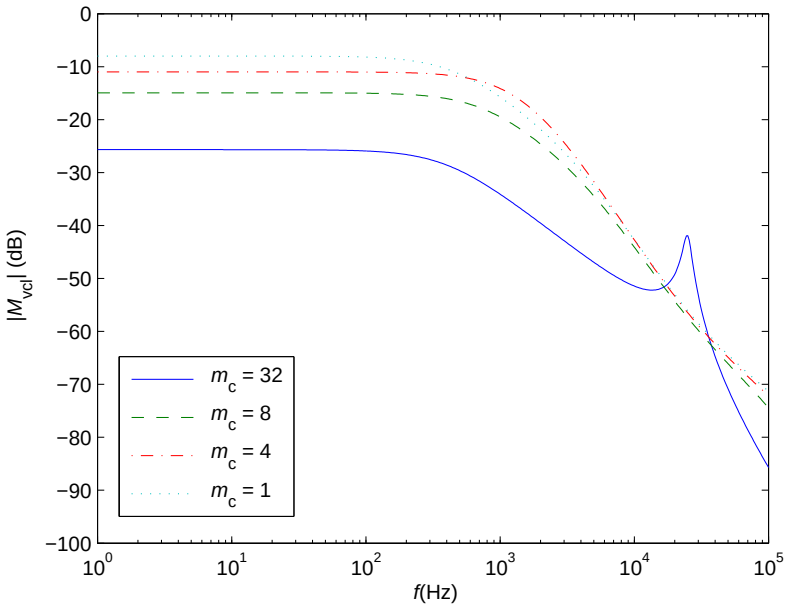


Figure 4.10: Audio-susceptibility gain of buck converter.

audio susceptibility for different values of $m_c$. It can be seen from the fig. that with $m_c = 32$, the characteristics approach the voltage-mode system. Without any external ramp, the transfer function shows the effect of dominant poles just as the control-to-output characteristics. These poles approach the imaginary axis as the duty ratio is increased upto 50 percent. The audio susceptibility of the buck converter lowers with added compensation to the system. As more compensation is introduced into the system, damping is provided to the system which prevents the peaking of the complex conjugate pole-pair at 50 percent duty ratio. Audio susceptibility keeps on reducing with the added compensation but only until the null value is reached(voltage-mode control characteristics). This value is reached at $S_e = S_f/2$ [3] and [6].

## 4.5 Output Impedance Transfer Function

Fig. 4.11 shows the circuit of the buck converter with the inner loop closed to derive the output impedance. Input voltage perturbation is zero and the disturbances in the duty cycle are introduced through the current feedback loop and in the output

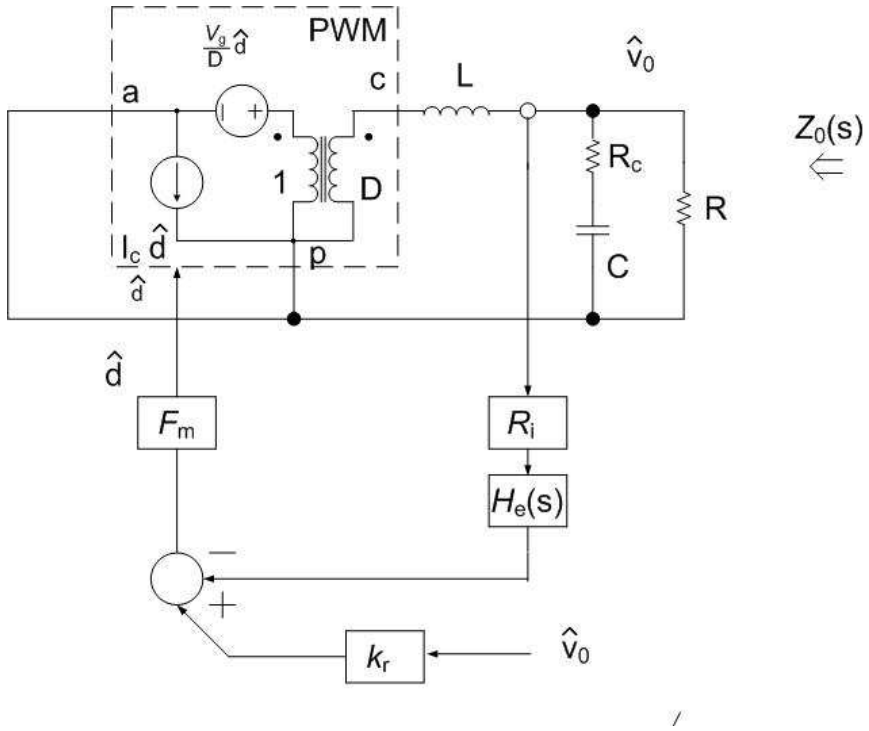


Figure 4.11: Converter system with current-loop closed and load current perturbation [3].

voltage via $k_r$ block. There is a small-signal current source applied on the load-side of the converter which results in input perturbations. The resulting output impedance transfer function is than given by [3], [6]

$$Z_0(s) \simeq \frac{R}{1 + \frac{RT_s}{L}(m_c D' - 0.5)} F_p(s). \tag{4.13}$$

However, this expression is accurate only when the current loop has a high gain at the frequency where resonance occurs in the filter circuit. At low frequencies, the value of the output impedance is approximately the dc load resistance, $R$, which is similar with the lines of averaged models. The output impedance has a dominant pole and a zero due to the ESR corner frequency of the output filter capacitor. The complex conjugate pole-pair at 50 percent duty ratio do not appear in this transfer

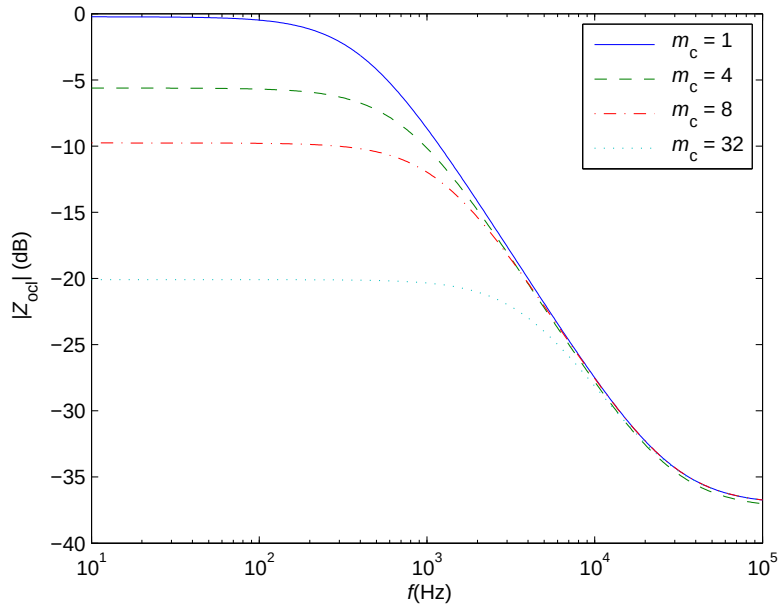


Figure 4.12: Output impedance of buck converter.

function. Fig. 4.12 shows the bode plot for output impedance [3] and [6].

# 5 Peak Current-Mode Control Model

## 5.1 Introduction

The peak current-mode control scheme proposed by Kazimerczuk results into different small-signal characteristics mainly due to the following reasons:

- The power stage models used are different.
- Both the models differ significantly in their way of deriving the sampling gain.
- The models also differ in their block diagram representation.

Despite the fact that both the models predict the instability of the current-mode control at 50 percent duty ratio, their small-signal characteristics differ significantly over a wide frequency range due to the above stated differences in the two models [1].

## 5.2 Sampling Gain in Peak Current-Mode Control Scheme

The discrete-time control voltage-to-inductor current transfer function, as shown previously, is given by [1]

$$H_{icl}(z) = \frac{i_l(z)}{v_c(z)} = \frac{1+a}{R_s}\frac{z}{z+a} = \frac{1+a}{R_s}\frac{z}{z-p}. \tag{5.1}$$

This transfer function has a pole at $p = -a$, and hence, for $a > 1$, the closed-loop system becomes unstable causing instability at a duty ratio beyond 50 percent and sometimes even before. For $a = 1$, the closed-loop system is marginally stable. This discrete-time transfer function can be transformed into a continuous-time expression in the s-domain. The continuous-time approximation of the above expression can be obtained using the definition of z-transform and by multiplying the result by the zero-order hold transfer function [1] and [10].

$$H_{ZOH} = \frac{1 - e^{-sT_s}}{s}. \tag{5.2}$$

The inductor current in the s-domain is given by [1]

$$i_l(s) = \frac{1+a}{R_s}\frac{e^{sT_s}}{e^{sT_s}+a}\frac{1-e^{-sT_s}}{s}v_c^*(s) = \frac{1+a}{R_s s}\frac{e^{sT_s}-1}{e^{sT_s}+a}v_c^*(s). \tag{5.3}$$

Where the asterisk represents a sampled variable [10] and [1]. The Laplace transform of the $v_c(s)$ and $v_c^*(s)$ are related by the expression [1]

$$v_c^*(s) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} v_c = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} v_c\left(s + \frac{j2\pi n}{T_s}\right). \tag{5.4}$$

The above approximation assumes that the control voltage $v_c$ does not contain significant components above $\frac{f_s}{2}$. This approximation assumes that control voltage is tested by a sinusoidal waveform. The control voltage-to-inductor current transfer function can be approximated in the s-domain by [10] and [1]

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} = \frac{i_l(s)}{i_l^*(s)} \times \frac{i_l^*(s)}{v_c^*(s)} \times \frac{v_c^*(s)}{v_c(s)} \approx \frac{1+a}{R_s}\frac{e^{sT_s}-1}{e^{sT_s}+a}. \tag{5.5}$$

At this point, there is a major difference between the two models. In the peak-current mode control scheme, this function has been approximated using the Padé Approximation for $e^{-sT_s}$ which gives the approximated expression for the above as [1]

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} \approx \frac{1}{R_s}\frac{1}{1+\frac{1-a}{1+a}\frac{sT_s}{2}+\frac{(sT_s)^2}{12}s} = \frac{1}{R_s}\frac{1}{1+\frac{1-a}{1+a}\frac{s}{2f_s}+\frac{s^2}{12f_s^2}}. \tag{5.6}$$

Comparing this with the standard expression for a second-order prototype system, we get the roots of the above equation which are nothing but a pair of complex conjugate poles given by [1]

$$p_{i1}, p_{i2} = -\frac{1-a}{1+a}3f_s \pm j2\sqrt{3}f_s\sqrt{1-\frac{3}{4}\left(\frac{1-a}{1+a}\right)^2}. \tag{5.7}$$

At $s = 0$,

$$H_{icl}(0) = \frac{1}{R_s}. \tag{5.8}$$

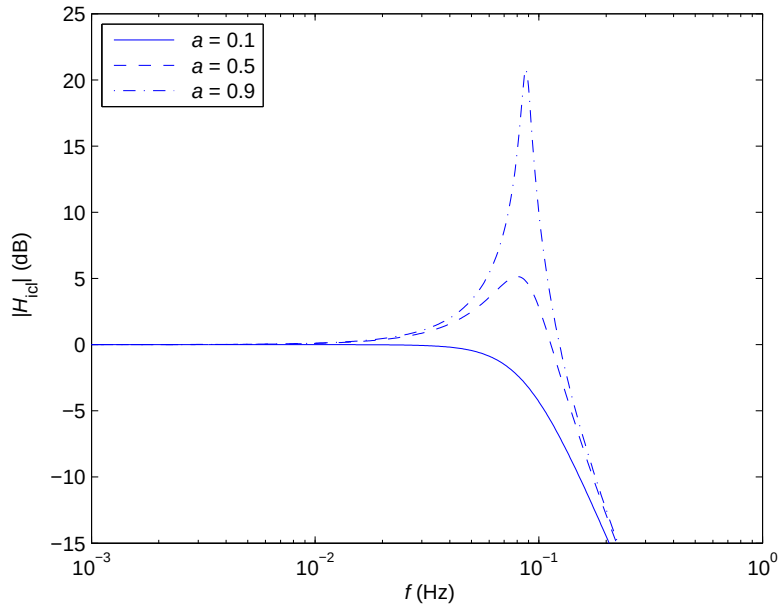


Figure 5.1: Magnitude plot of $H_{icl}$ for $a = 0.1, 0.5$ and 0.9.

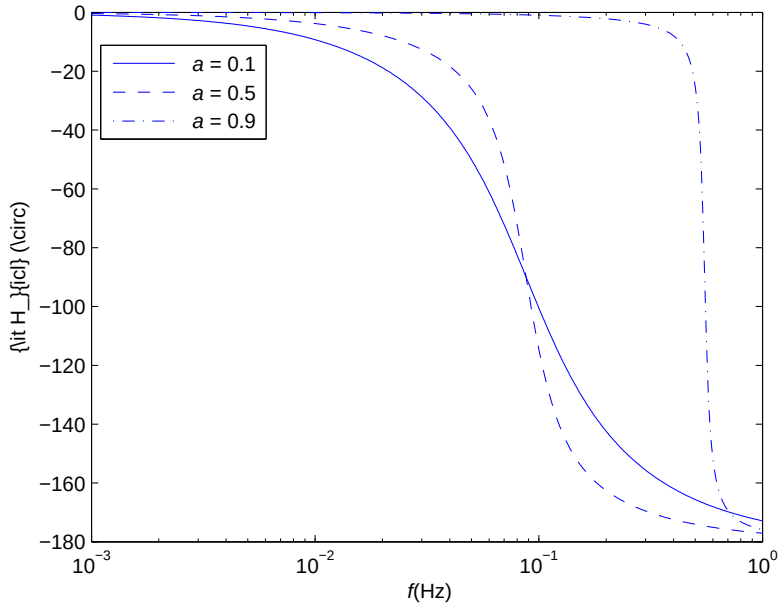


Figure 5.2: Phase plot of $H_{icl}$ for $a = 0.1, 0.5$ and 0.9.

Thus, the sampling gain depends only on $f_s, a, and R_s$. The complex conjugate poles are either on the LHP or RHP. For $a < 1$, the two poles are in the LHP and hence the closed-loop system is stable. For $a = 1$, the system is marginally stable with

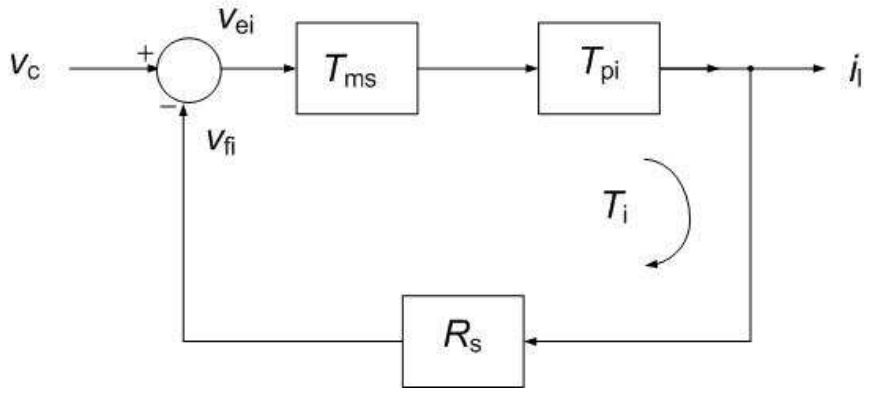


Figure 5.3: Closed-Current Loop of Buck Converter without Slope Compensation [1].

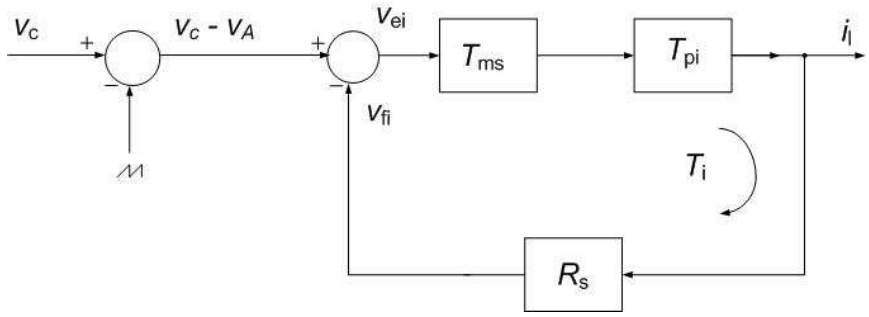


Figure 5.4: Closed-Current Loop of Buck Converter with Slope Compensation [1].

sustained oscillations. For $a > 1$, the system is unstable, causing growing oscillations. Fig. 5.1 and 5.2 shows the magnitude and phase plot $H_{icl}$. As seen from the diagram, the magnitude of the sampling gain is 12.4 dB at 50 percent duty ratio, while the phase is -40.9 degrees at that frequency. Both these values are significantly different for the same switching frequency of 50 kHz when compared to the Ridley's model [3]. This is significantly different because of the different ways in which sampling gain is derived in both the models. For 50 percent duty ratio, the value of $a$ is 1. And the system is marginally stable with a phase margin of 0 [1].

## 5.3 Loop Gain of Current Loop

Fig. 5.3 shows the diagram of the closed-current loop without the slope compensation. Fig. 5.4 shows the diagram for the closed-current loop with the slope compensation.

This block diagram is significantly different from that of Ridley's model. The loop gain of the system can be mathematically written as follows based on the block diagram representation [1].

$$T_i(s) = \frac{v_{fi}(s)}{v_{ei}(s)} = T_{ms}T_{pi}R_s \approx \frac{12f_s^2}{s\left(s + \frac{1-a}{1+a}6f_s\right)} = \frac{12f_s^2}{s(s + w_{sh})}. \tag{5.9}$$

From the equation, it is clear that the current loop has two poles. One of the poles is located at the origin, while the location of the second pole depends on a. For $a < 1$, the pole is in the LHP, and the current-loop is stable. For $a = 1$, the second pole is at the origin, and the current loop is marginally stable. For $a > 1$, the second pole is in the RHP, and the current loop is unstable. Fig. 5.5 and 5.6 shows the small-signal characteristics for the open-loop gain. For $a = 0.82$, which is the value obtained for a duty ratio of 0.45, the gain margin of the system is infinity since the phase never crosses 180 deg, and the phase margin is 65.6 deg. The gain and the phase at half the switching are also significantly different. This is because the current loop has 2 poles, while in the continuous time model, the current loop is characterized by 2 zeros due to a different approximation for the sampling gain [1].

## 5.4 Conclusions

Based on the above characteristics of the Current-Mode Control, it is quite clear why the two models are significantly different. In the continuous time model, the sampling gain is represented by 2 zeros to show characteristics that are accurate upto half the switching frequency. This transfer function has more zeros than poles which is actually a kind of defect according to the fundamentals of the control theory. But this model is legit upto half the switching frequency which is the main requirement in modelling the current-mode control theory. This is a specific choice been made to model a system which is accurate upto the frequency of interest. If the model is to be extended for the higher frequencies, than more poles will be needed to accurately

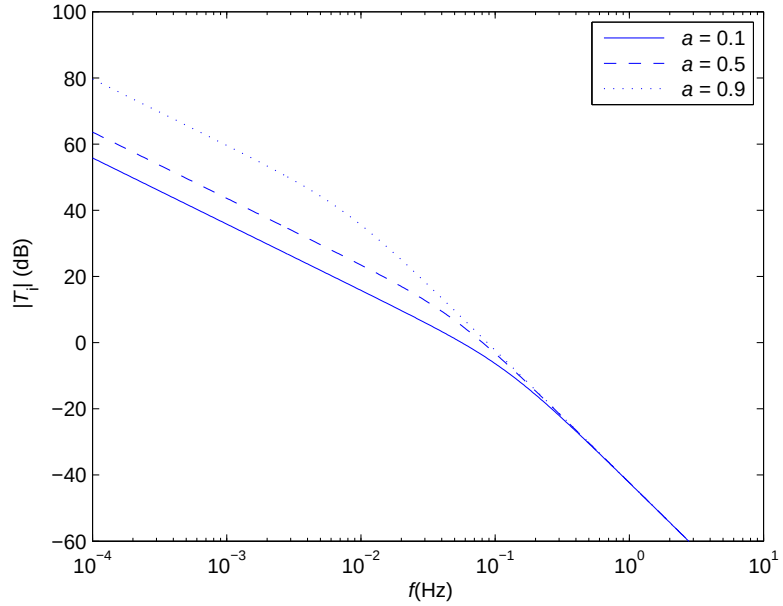


Figure 5.5: Magnitude Plot of Current-Loop Gain for $a = 0.1, 0.5$ and 0.9.

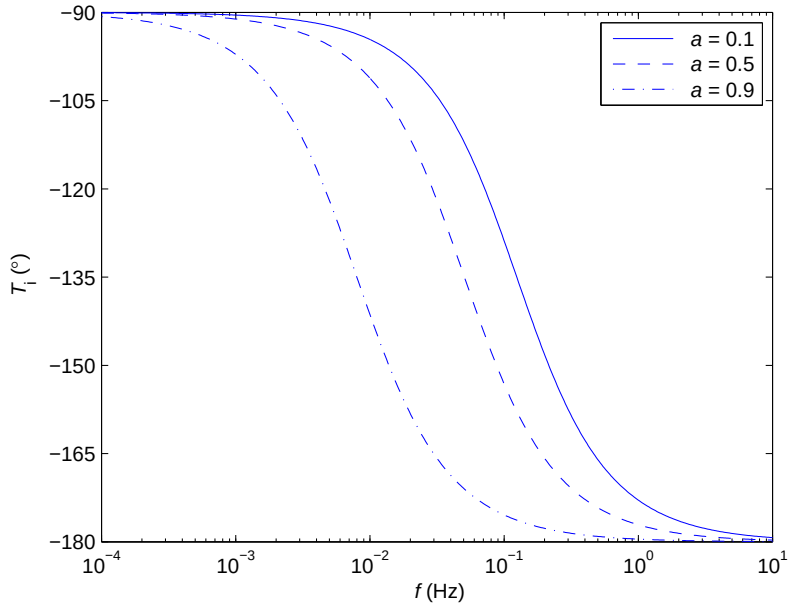


Figure 5.6: Phase Plot of Current-Loop Gain for $a = 0.1, 0.5$ and 0.9.

model the sampling gain. This will result in number of zeros to be either less than or equal to the number of poles. While in the peak current-mode control model, a second order Padé approximation is used to model the sampling gain which results

in more poles than zeros. This model also predicts the instability of the current-mode control at a duty ratio of 50 percent, which is on the similar lines with the new continuous time model. Slope Compensation is needed to achieve the stability of the current mode control beyond 50 percent duty ratio for CCM. External compensation is required to compensate the actual inductor current waveform which is not enough for controlled operation. As the external ramp increases, the range for the duty cycle for stable operation increases beyond 0.5. Also, in this model, for the closed loop transfer function, the output is considered as the duty cycle as in case with the actual converters [1] and [3].

## 5.5 Comparison between the two models

As already seen in the previous discussion, the two models have a different way of deriving the sampling gain, as a result the small-signal analytical transfer functions are vastly different for the two models. The expression for the parameter, $a$, has the rising slope of the inductor current as well as the external ramp required for slope compensation, in the model proposed by Kazimierczuk [1]. The similar parameter with a different expression is given by, $m_c$, in Ridley's model for current mode control [3]. A comparison between the two models is carries out by deriving a relationship between $a$ and $m_c$. The parameter,$a$, in kazimierczuk's model, is given by [1]

$$a = \frac{M_2 - M_3}{M_1 + M_3}. \tag{5.10}$$

Where, $M_1$ is the rising slope of the inductor current waveform, $M_2$ is the falling slope of the current waveform, and $M_3$ is the external ramp required for slope compensation.

Similar parameter, $m_c$, in the continuous-time model is given by [3]

$$m_c = 1 + \frac{S_e}{S_n}. \tag{5.11}$$

In this equation, $S_e$ is equivalent to $M_3$ and $S_n$ is equivalent to $M_1$ in the peak current-mode control model. So, the above equation can be re-written as

$$m_c = 1 + \frac{M_3}{M_1}, \tag{5.12}$$

which gives

$$M_3 = M_1(m_c - 1). \tag{5.13}$$

Substituting the value of $M_3$ in equation for $a$, we get

$$a = \frac{M_2 - M_1(m_c - 1)}{M_1 + M_1(m_c - 1)}. \tag{5.14}$$

Dividing the numerator and denominator by $M_1$, we get

$$a = \frac{\frac{M_2}{M_1} - (m_c - 1)}{m_c}. \tag{5.15}$$

But, $\frac{M_2}{M_1} = \frac{D}{1-D}$. Substituting the value for $\frac{M_2}{M_1}$ in the above equation gives [1], [3]

$$a = \frac{\frac{D}{1-D} - (m_c - 1)}{m_c}. \tag{5.16}$$

Therefore, $a = \frac{\frac{D}{1-D} - (m_c - 1)}{m_c}$ is the relationship between the two parameters. Based on this relationship, a comparison can be drawn between the two models. For particular values of $m_c$, corresponding values of $a$ are used based on the above relationship to determine the small-signal characteristics. However, the values for $a$ are restricted by the choice of external ramp $M_3$ and duty cycle $D$. This restriction is based on the expression [1], [24], [25] and [3]

$$\frac{M_3}{M_1} = \frac{D - 0.5}{1 - D}. \tag{5.17}$$

The value for $D$ obtained from this is the limiting value for duty cycle, beyond which the system is unstable. For a value of $m_c = 1$, $\frac{M_3}{M_1} + 1 = 1$. Which gives $M_3 = 0$, and the corresponding value for $D$ is 0.5 based on the above expression. Substituting the

values for $m_c$ and $D$ in the expression relating $a$ and $m_c$, gives the value for $a$ as 1 [1] and [3]. Similarly, for the value of $m_c = 2$ and $m_c = 4$, the limiting values for $D$ are 0.75 and 0.875, respectively. The system will be marginally stable for these values of $D$. i.e $a = 1$ for these values of duty cycle. Any values of $D$ chosen below this range will give a stable system with $a < 1$. The values for $D$ are chosen as $\frac{2}{3}$ and $\frac{4}{5}$ corresponding to $m_c = 2$ and $m_c = 4$, respectively [1], [24], [25] and [3].

Again, buck converter is chosen as an example for comparing the two models. The parameters are the same as those being used previously in the continuous-time model. The values for $a$ are chosen corresponding to $m_c$ based on the relationship derived previously.

### 5.5.1 Comparison of Current-Sampling Function

As already discussed previously, modelling of current-loop involves the sampled-data modelling. The sampling gain expression in the continuous-time model is given by

$$H_e(s) \simeq 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}[3] and [8], \tag{5.18}$$

where [3]

$$Q_z = \frac{-2}{\pi}, \tag{5.19}$$

and

$$\omega_n = \frac{\pi}{T_s}. \tag{5.20}$$

The current-sampling function in kazimierczuk's model is given by [1]

$$H_{icl}(s) = \frac{1}{R_s} \frac{12 f_s^2}{s^2 + \frac{1-a}{1+a} 6 f_s s + 12 f_s^2}. \tag{5.21}$$

Evidently, from the two transfer functions that the sampling gain in Ridley's model is same regardless of the external ramp and depends only on the switching frequency.

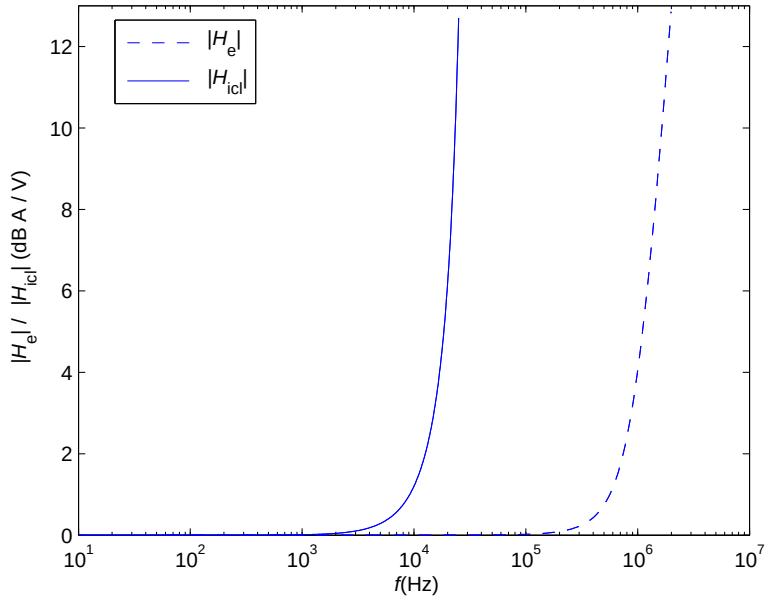


Figure 5.7: Magnitude curves of sampling function.

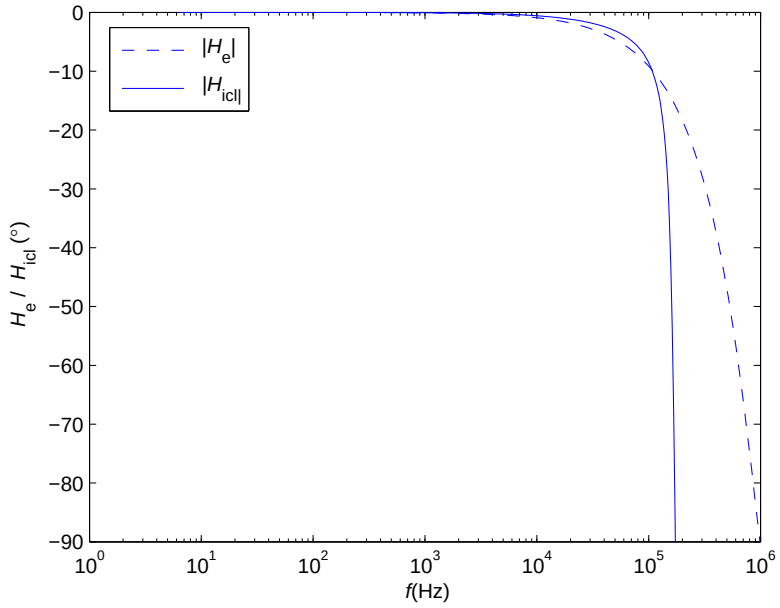


Figure 5.8: Phase curves of sampling function.

While in case of the Kazimierczuk's model, it depends on the external ramp as well as the switching frequency. As seen from from Fig. 5.7 and 5.8, the bode plots for the sampling gain of the two models shows differences across wide frequency range

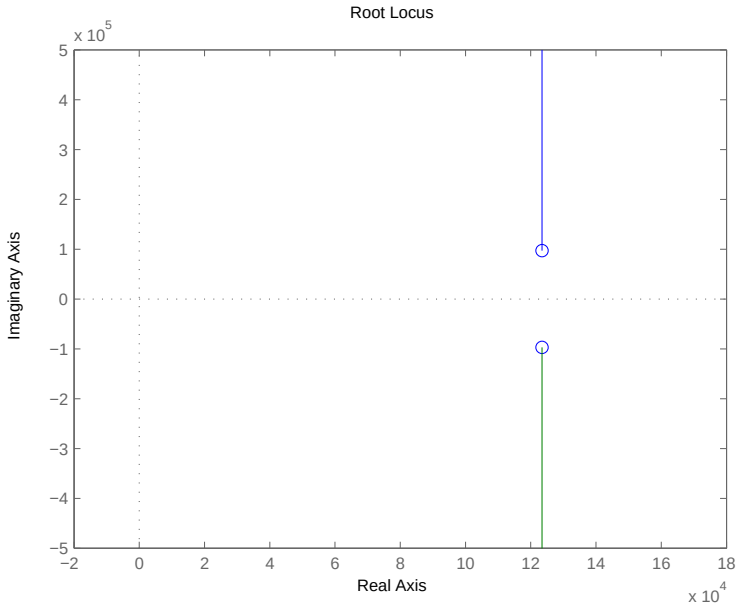


Figure 5.9: Root locus for $H_e(s)$.

[1] and [3].

Also, from the two functions, it can be seen that the sampling function has two complex RHP zeros in the continuous-time model while it has two complex conjugate poles in the kazimierczuk's model. The root locus plots for both these models are shown below. Since the continuous-time model is invariant, it's root locus does not change with the duty cycle or external ramp. While in case of kazimierczuk's model, it depends on the parameter $a$, which in turn depends on the duty cycle as well as the external ramp [1] and [3].

Fig. 5.9 and 5.10 shows the root locus plots for $H_{icl}$ and $a$. Evidently, from the root locus plot for $H_{icl}$ function, that as $a$ changes from 0 to 2, the complex conjugate poles start moving towards the right half of the s-plane. At $a = 1$, the poles are on the imaginary axis, beyond which they are on the right half of s-plane.

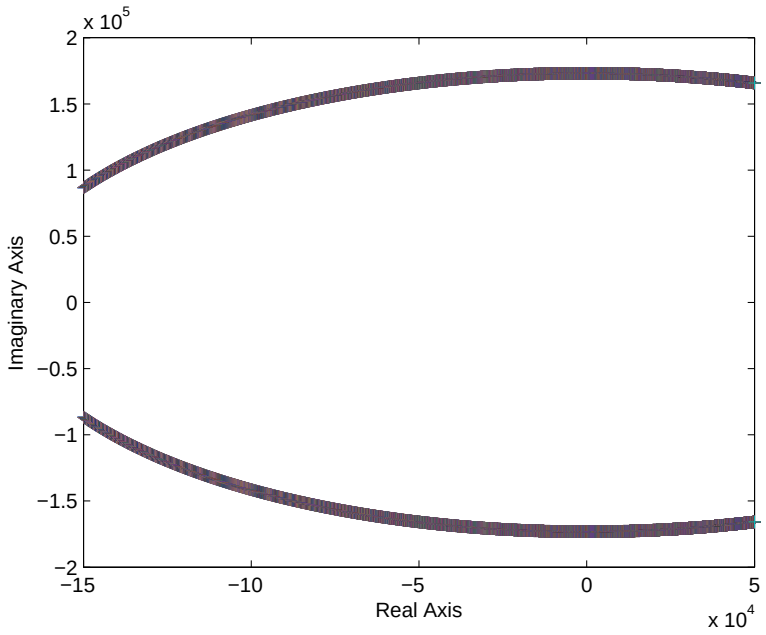


Figure 5.10: Root locus for $H_{icl}$ with $a$ changing from 0 to 2.

### 5.5.2 Comparison of Loop Gain

The loop gain transfer function for Ridley's model is given by [3]

$$T_i(s) \simeq \frac{L}{RD'T_s m_c} \frac{1 + sCR}{\triangle(s)} H_e(s). \tag{5.22}$$

The bode plot for the loop gain is shown in Fig. 5.11. The open-loop characteristics are plotted for $m_c = 1, 2$, and 4. Evidently, with $m_c = 1$, i.e. with no external ramp, the system is close to instability. By increasing the duty ratio, additional gain can be provided to the system. But the system becomes unstable at 50 percent duty ratio. With added compensation, gain and phase margin increases in the system. Therefore, the range of duty cycle in which the system is stable increases beyond 0.5 as more ramp is added [3].

Now, the open loop gain for the inner loop in Kazimierczuk's model is given by [1]

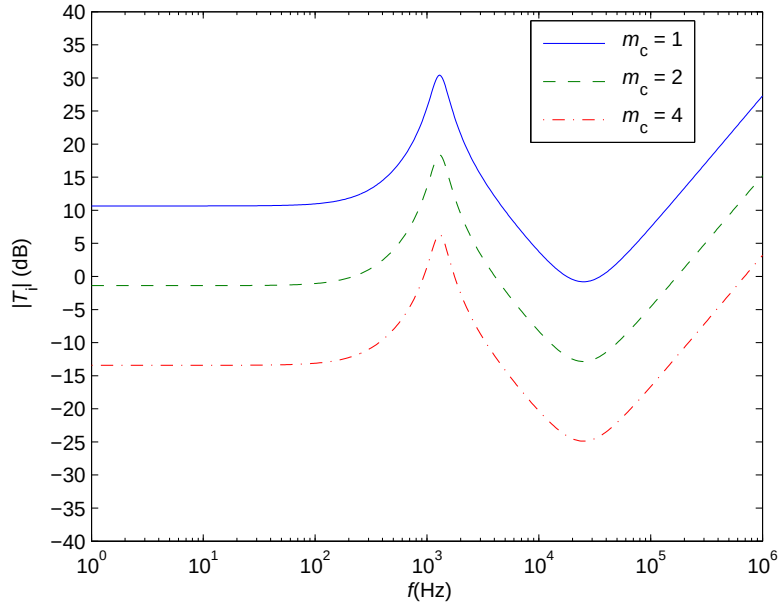


Figure 5.11: Loop gain for Ridley's model with $m_c = 1, 2$, and 4.

$$T_i(s) \simeq \frac{12 f_s^2}{s(s + \omega_{sh})}, \tag{5.23}$$

where [1]

$$\omega_{sh} = \frac{1 - a}{1 + a} 6 f_s. \tag{5.24}$$

Using the relationship derived before,for the given values of $m_c$ the corresponding values for $a$ are, $a = 1, 0.5$, and $0.25$. Using these values of $a$, the open-loop characteristics are plotted as shown in the figure 5.12. The vast differences between the two characteristics can be seen evidently from their open loop characteristics. Also, the bode plots for $a = 0.25$ and $m_c = 4$ are superimposed on the same plot to show he differences between the two models based on the corresponding values of $a$ for different values of $m_c$ [1].

The stability of the two models are compared based on the nyquist stability cri-

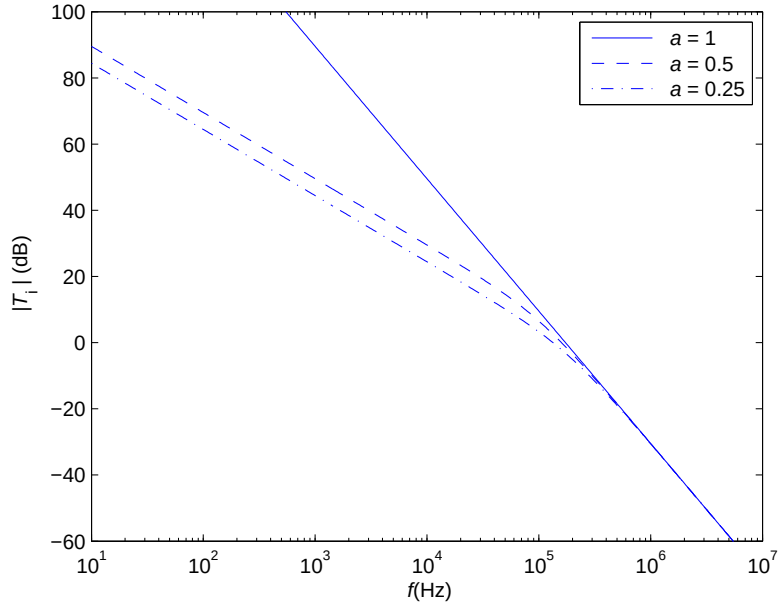


Figure 5.12: Loop gain for kazimierczuk's model with $a = 0.25, 0.5$, and 1.

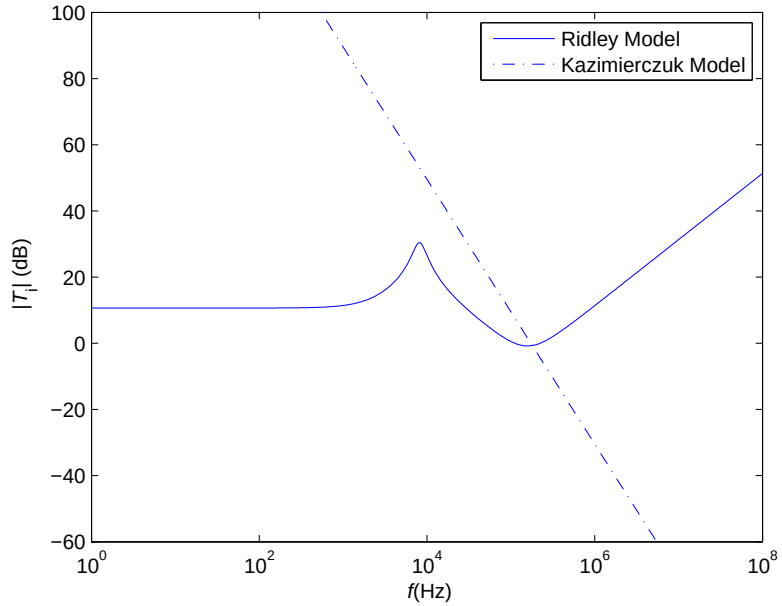


Figure 5.13: Respective loop gains for both the models $m_c = 1$ and $a = 1$.

terion for the open loop transfer function of the two models for different values of $m_c$ and corresponding values of $a$. The nyquist diagrams for both the models are shown below. From the nyquist plots of Kazimierczuk's model, for $0 < a < 1$, the system

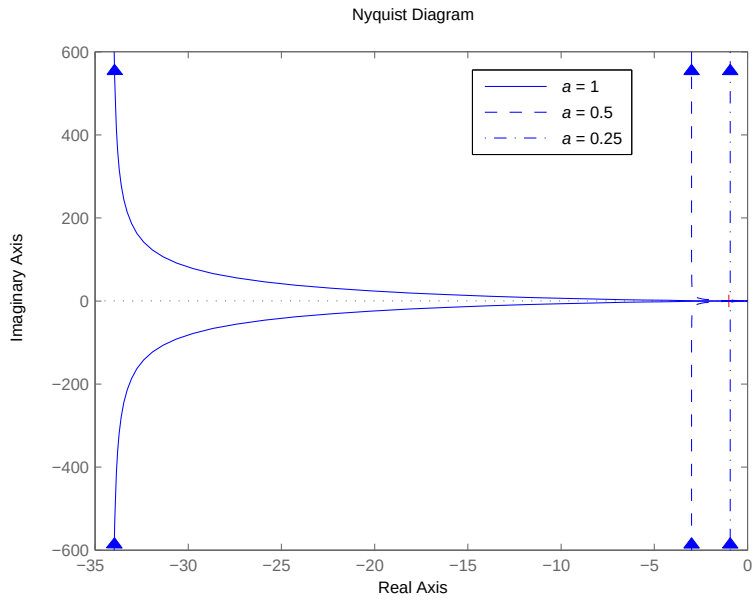


Figure 5.14: Nyquist plots for loop gain of kazimierczuk's model.

is stable, while for $a = 1$, the system is marginally stable and the contour touches the point $-1 + j0$. For $a > 1$, the nyquist contour encircles the $-1 + j0$ point. Since the second order system has infinite gain margin, it is assumed that the contour will encircle the $-1 + j0$ point at some point [1], [3].

For the continuous-time model, it can be seen that without any external ramp, i.e. $m_c = 1$, the open loop system is stable for the duty cycle below 0.5. While for a duty ratio of more than 0.5, the nyquist contour encircles the $-1 + j0$ point [1] and [3].

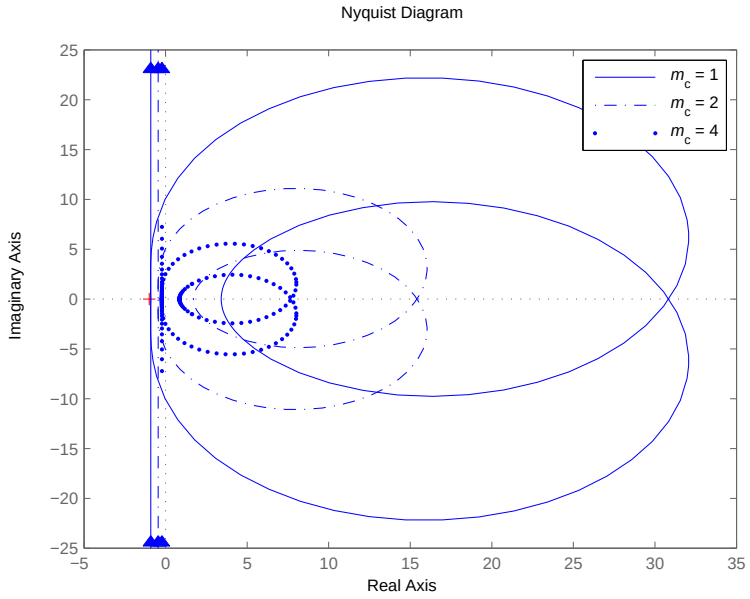


Figure 5.15: Nyquist plots for loop gain of ridley's model.

### 5.5.3 Comparison of Control-to-Output Transfer Function

The approximate transfer function from control-to-output gain with inner current loop closed, for buck converter is given by [3]

$$\frac{\hat{v}_0}{\hat{v}_c} \simeq \frac{R}{R_i} \frac{1}{1 + \frac{RT_s}{L}[m_c D' - 0.5]} F_p(s) F_h(s), \tag{5.25}$$

where [3]

$$F_p(s) = \frac{1 + sCR_c}{1 + \frac{s}{w_p}}, \tag{5.26}$$

$$w_p = \frac{1}{CR} + \frac{T_s}{LC}(m_c D' - 0.5), \tag{5.27}$$

$$F_h(s) = \frac{1}{1 + \frac{s}{w_n Q_p} + \frac{s^2}{w_n^2}}, \tag{5.28}$$

and

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)}. \tag{5.29}$$

The values chosen for $m_c$ are 1,2 and 4. The magnitude plot for control voltage-to-output voltage gain is shown in the Fig. 5.16.

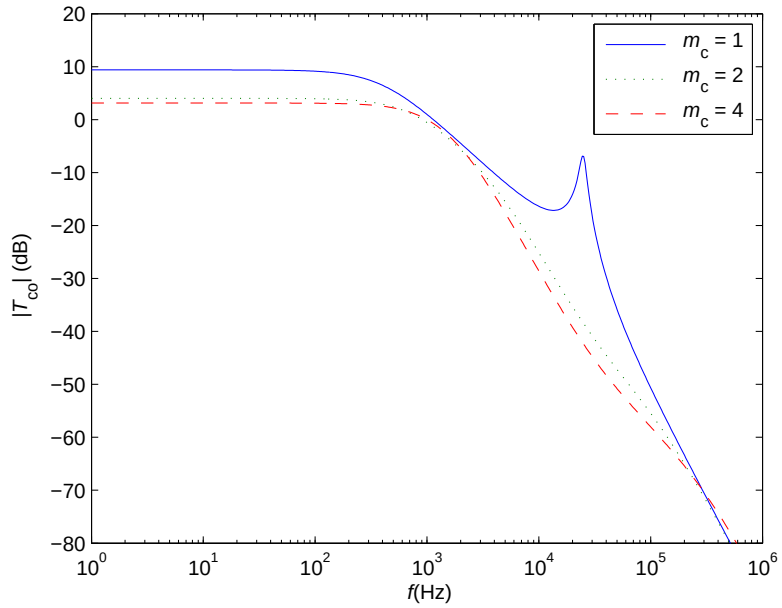


Figure 5.16: Control-to-output gain for continuous-time model with $m_c = 1$, 2 and 4.

The transfer function from control-to-output for Kazimierczuk's model described previously is given by [1]

$$T_{co}(s) = \frac{R_L r_c \omega_h^2}{R_s(R_L + r_c)} \frac{s + \omega_{zn}}{(s^2 + \omega_{sh} s + \omega_h^2)(s + \omega_{zi})}, \tag{5.30}$$

where [1]

$$\omega_h = \sqrt{12} f_s, \tag{5.31}$$

$$\omega_{sh} = 6\frac{1-a}{1+a} f_s, \tag{5.32}$$

$$\omega_{zn} = \frac{1}{C r_c}, \tag{5.33}$$

and

$$\omega_{zi} = \frac{1}{C(R_L + r_c)}. \tag{5.34}$$

The magnitude plot for the control-to-output gain is plotted for $a = 1, 0.5$, and 0.25. These values of $a$ are the corresponding values for $m_c$ in the continuous-time model.

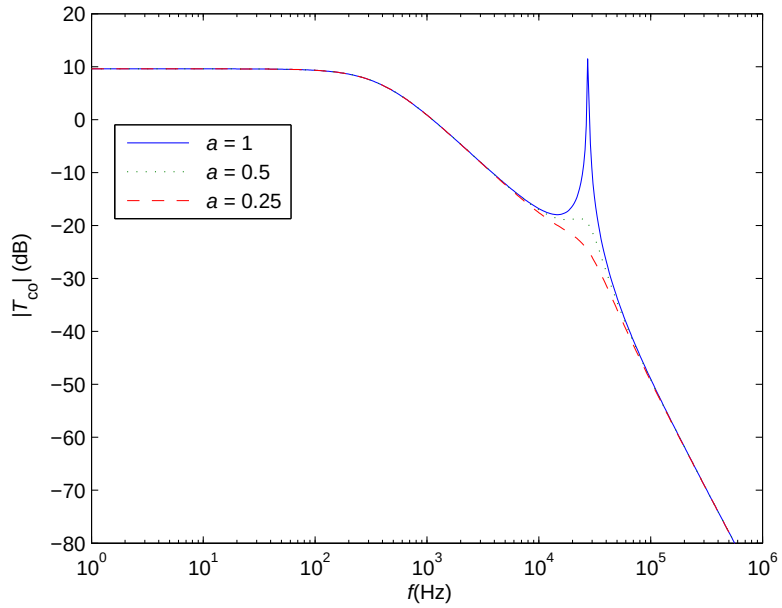


Figure 5.17: Control-to-output gain for continuous-time model with $a = 1$, 0.5 and 0.25.

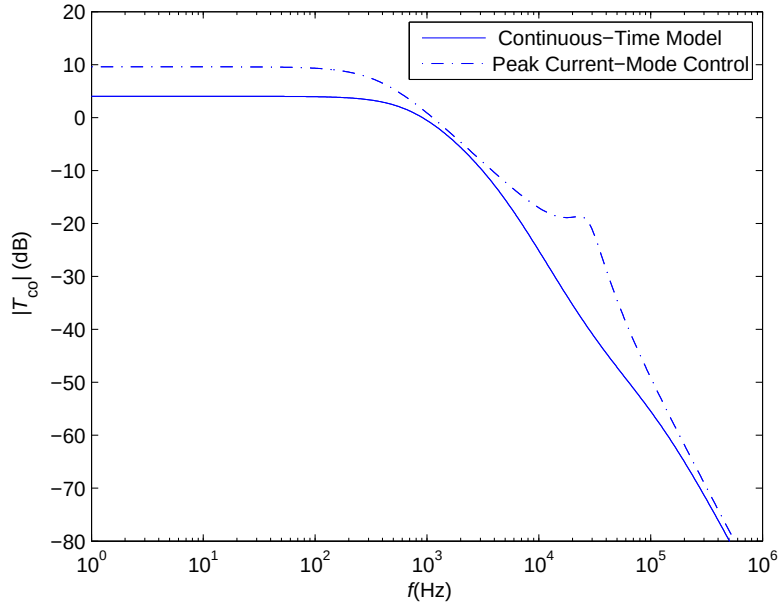


Figure 5.18: Control-to-output gain for Both Models with $m_c = 2$ and $a = 0.5$.

The magnitude plot for the two models are superimposed in Fig. 5.18, clearly, two curves are very close and are within the same frequency range.

# 6 Average Current-Mode Control Scheme, an Application of Current-Mode Control Scheme

## 6.1 Introduction

This scheme is an application of the current-mode control scheme, the only difference in this case is that here, the average inductor current is controlled instead of the peak current and the average current ramp is compensated dynamically by the external ramp as well as an RC circuit compensating network. While in conventional control schemes, the inductor peak current follows set program that provides a fixed compensation. PWM dc-dc converter behaves as an ideal current source, which is an advantage in this scheme when compared with other schemes of control [5]. This model also exhibits sustained oscillations at a duty ratio of 50 percent. This model is also suitable for power-factor improvement in boost converters because of a different kind of topology in which the input current represents the inductor current. Similar to the previous schemes, a small-signal model was developed after using the discrete-time analysis. The difference here is that the sensed average current in this case is further compensated by a RC circuit network. This compensation network further complicates the small-signal analysis. Fig. 6.1 shows the circuit diagram for average current-mode control scheme [4], [5], and [3].

## 6.2 Modulation Scheme and RC Circuit Compensation

Fig. 6.2 shows the current compensation network used for the control of averaged inductor current. The modulator gain in this case is different in this case compared to other models because of this compensation network. From the fig., it is quite clear that the shape of inductor current is no longer the same due to this additional RC circuit network [5]. The modified slope of this waveform can be calculated as [5]:

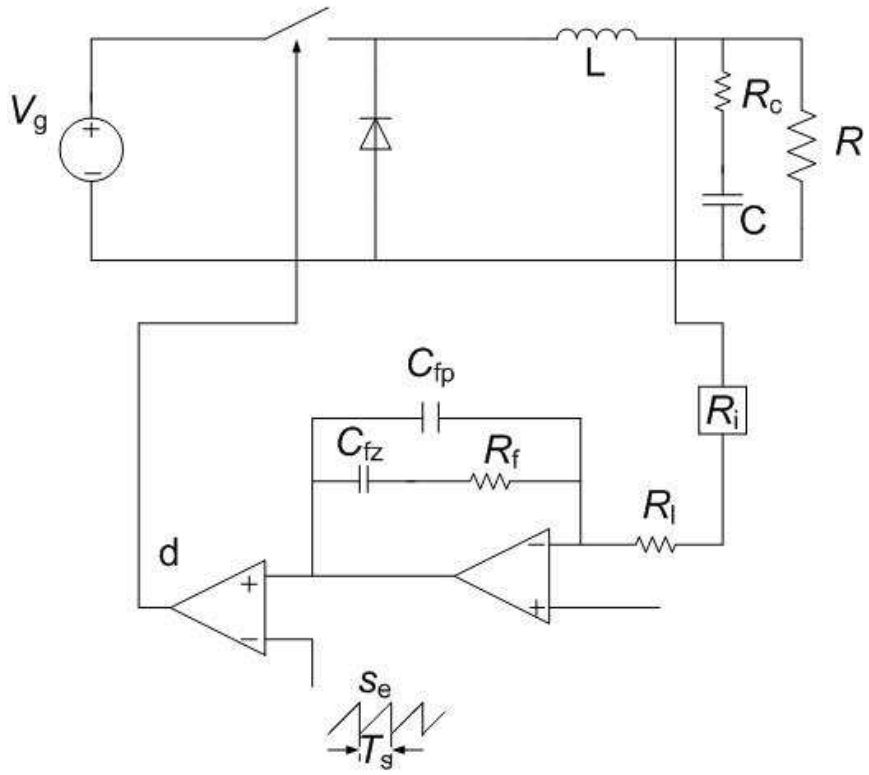


Figure 6.1: Circuit diagram for Average current-mode control scheme [5].

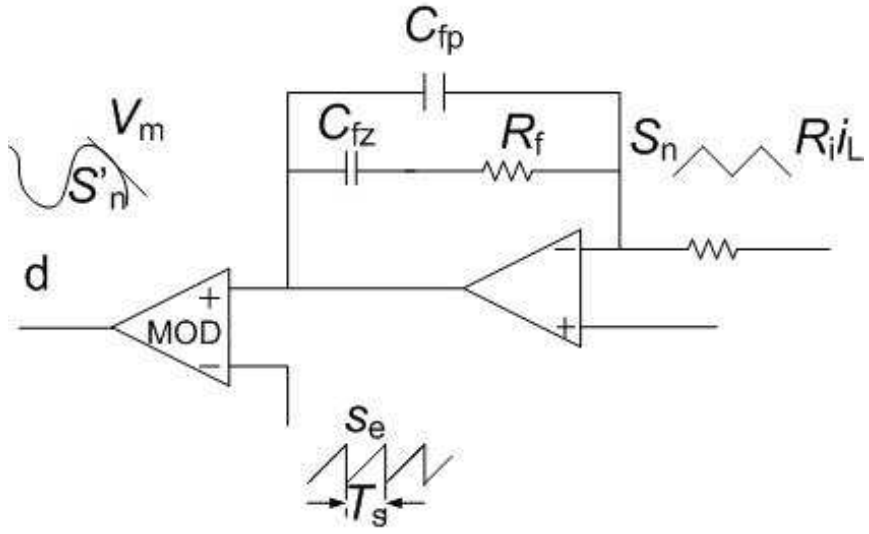


Figure 6.2: Current modulator and compensator [5]

$$S_n' = \omega_i S \left[ DT_s + \left( \frac{1}{w_z} - \frac{1}{w_p} \right) \left( 1 - e^{-w_p DT_s} \right) \right]. \tag{6.1}$$

Where, $S'_n$ is the modified slope of current waveform due to the presence of RC circuit network, $S_n$ is the upward slope of the inductor current, $S_e$ is the slope of the external ramp required for compensation, and [5]

$$\omega_i = \frac{1}{R_l(C_{fp} + C_{fz}}), \tag{6.2}$$

$$\omega_z = \frac{1}{R_f C_{fz}}, \tag{6.3}$$

and

$$\omega_p = \frac{C_{fz+C_{fp}}}{R_f C_{fz} C_{fp}}. \tag{6.4}$$

As shown previously, the modulator gain for this scheme is given by [5]

$$F_m = \frac{1}{(S_e + S'_n)T_s}. \tag{6.5}$$

Since the compensation network is an RC circuit, it has a filtering action. Due to this filtering action, $S'_n \leq S_n$. i.e. for the same external ramp, the modulator gain for this scheme is less than that for previously derived models [5], [3].

The sampling gain in average current mode-control is the same as the peak current-mode control. Fig. 3 shows the small-signal model for this scheme. The two blocks, $G_s(s)$ and $G_p(s)$, were derived based on the RC circuit in the current loop. The two transfer functions are given by [5]

$$G_s(s) = \frac{w_i\left(1 + \frac{s}{w_z}\right)}{s}, \tag{6.6}$$

and

$$G_p(s) = \frac{1}{\left(1 + \frac{s}{w_p}\right)}. \tag{6.7}$$

From the figure,evidently, the shape of the inductor current waveform is not a saw-tooth shape. However, by making certain adjustments and by drawing tangents to the curve, this waveform can be made comparable to the compensating ramp

mathematically [5]. The resulting current is a function of the RC circuit network and the line and load voltages. Under steady-state conditions, the duty cycle would remain constant. The duty cycle would remain constant without any line or load variations [5]. However, this is rarely the case and hence disturbances in the line and load voltages have to be taken into consideration. The effect of these disturbances on the duty cycle can be shown by feed-forward blocks, $k_r$ and $k_f$ [5].

## 6.3 Predictions of Model

The model shown in Fig. 6.3 is used to make predictions using MATLAB. A buck converter in CCM was used to make predictions based on the following parameters [5].

$V_g = 14$ V, $V_0 = 5$ V, $R = 1\ \Omega$, $L = 37.5\ \mu$H, $C = 380\ \mu$F, $R_c = 20$ m$\Omega$, $F_s = 50$ kHz [5].

The elements in the inner loop were: $R_i = 0.1\ \Omega$ $R_l = 2.2$ k$\Omega$ $R_f = 30.5$ k$\Omega$ $C_{fz} = 5.8$ nF , and $C_{fp} = 220$ pF [5] and [3].

### 6.3.1 Loop Gain

From fig.6.3, the transfer function for the loop gain of the system is given by

$$T_i(s) = \frac{F_m R_i V_g}{R} \frac{(1+sRC)}{\left[1+s\left(\frac{L}{R}+CR_c\right)+s^2LC\right]}.H_e(s)\frac{\omega_i\left(1+\frac{s}{w_z}\right)}{s}, \tag{6.8}$$

where [5]

$$\frac{V_g}{R}.\frac{(1+sRC)}{\left[1+s\left(\frac{L}{R}+CR_c\right)+s^2LC\right]} \tag{6.9}$$

is the transfer function for buck converter ignoring the parasitic components. In this model, the additional RC circuit also affects the loop gain characteristics unlike the previous models. Fig. 6.4 and 6.5 shows the characteristics of the open loop gain. By changing $\omega_i$ and $\omega_z$, dc gain and the shape of the curve can be obtained as

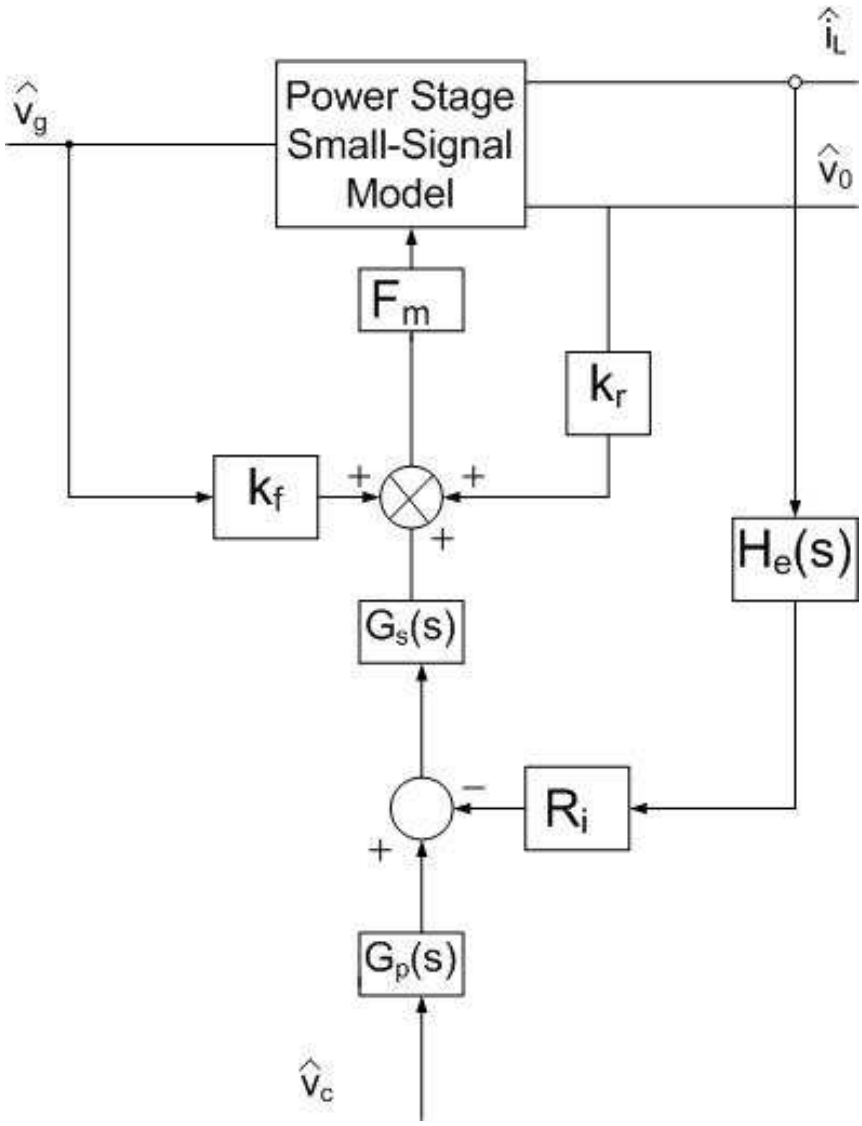


Figure 6.3: Small-signal model to predict the characteristics [5].

required. So, there is more design flexibility compared to the previous schemes where a fixed ramp is used for compensation. Evidently, the curve from dc to the frequency range of interest has quite a large region . This implies that this scheme has less low frequency error compared to the current-mode control scheme [5] and [3].

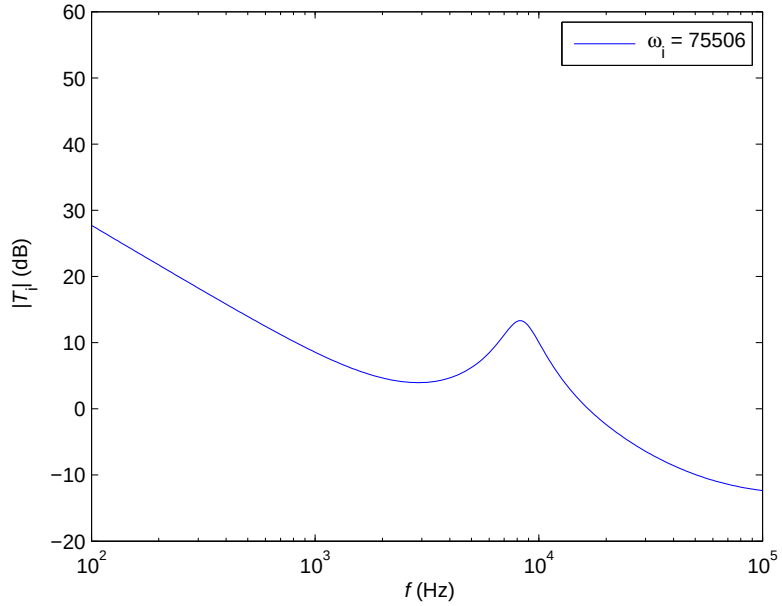


Figure 6.4: magnitude plot of current-loop gain.

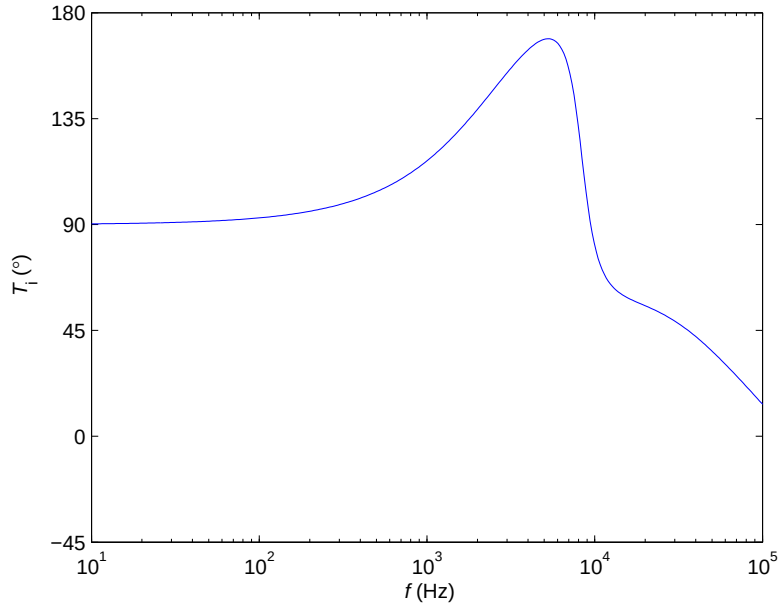


Figure 6.5: phase plot of current-loop gain.

### 6.3.2 Transfer Function for Control-to-Output

The transfer function from control-to-voltage can be derived having inner loop closed and outer loop open. The approximated expression for that is given by [5]

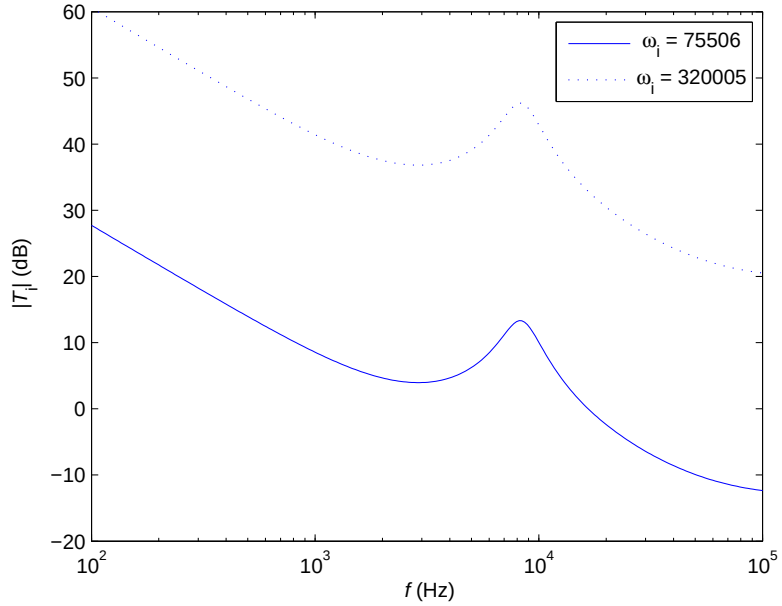


Figure 6.6: magnitude plot of current-loop gain varying $\omega_i$.

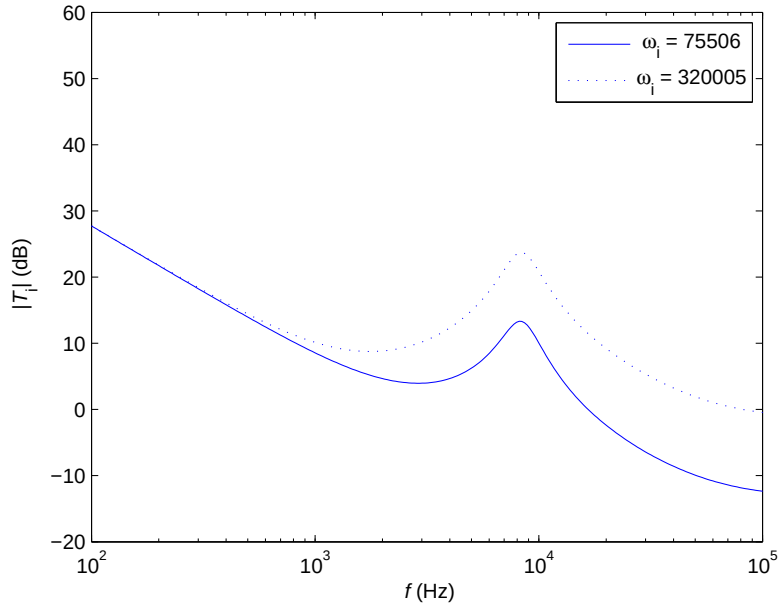


Figure 6.7: magnitude plot of current-loop gain varying $\omega_z$.

$$\frac{\hat{v_0}}{\hat{v_c}} \simeq \frac{1}{R_i} \frac{(1+sR_cC)}{[1+sR(C+C_x)]\left(1+\frac{s}{\omega_p}\right)} F_h(s), \tag{6.10}$$

where

$$C_x = \frac{1}{F_m V_g \omega_i R_i}, \tag{6.11}$$

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n} Q_p + \frac{s^2}{\omega_n}^2}, \tag{6.12}$$

and

$$Q_p = \frac{1}{\pi \left( \frac{L F_s \omega_z}{F_m V_g \omega_i R_i} - \frac{1}{2} \right)}. \tag{6.13}$$

At low frequency range, one pole cancels the only zero, and thus there remains the effect of a single pole out of the two poles. At high frequencies, the pair of complex conjugate poles is responsible for peaking. The peaking of poles at higher frequencies can be prevented by the use of external compensation and the RC series network [5], [3].

### 6.3.3 Audio-susceptibility

The approximate expression for the feed-forward gain is given by [5]

$$\frac{\hat{v_o}}{\hat{v_g}} \simeq \frac{R(k_f F_m V_g + D)}{F_m V_g R_i \omega_i} \frac{(1 + sR_c C)}{[1 + sR(C + C_x]} . \frac{s}{\left(1 + \frac{s}{\omega_z}\right)} F_h(s). \tag{6.14}$$

In this scheme, $k_f$ has a negative value inherently. As a result, the audio-susceptibility for this scheme is less than that of previously shown scheme of control. In this scheme as well, the effect line and load perturbations can be nullified $\omega_z$. However, the modulator gain and the feed-forward gain have a non-linear relationship with the external ramp and $\omega_i$. Consequently, it becomes difficult to set the values for these parameters, so that response to perturbations is nullified. This is one of the disadvantages of this scheme compared to that of the current mode control scheme [5], citeridleyphd.

# 7 Conclusions

## 7.1 Ridley's Model

The continuous time model uses a three-terminal switch model which is invariant for all the converters. This model is highly accurate upto half the switching frequency compared to the averaged models [3].

Current-mode control modelling involves discrete-time signals. Discrete-time modelling, basic to all PWM converters, was used for analysis of the current-mode control scheme. An approximated second order expression for the sampling gain was used to analyze the current-mode control scheme which is fairly accurate upto the frequency-range of interest. However, this approximation results in an improper transfer function, with the order of the numerator being higher than that of the denominator, which is usually not seen in control theory [3] and [11].

The transfer function for the inner loop has a pair of complex conjugate zeros in the right half of s-plane at nyquist frequency [3].

The phase of the inner loop reduces considerably as the duty cycle approaches to 0.5 [3]. This low phase margin produces a pair complex conjugate poles in the transfer function from control-to-output at high frequencies [3]. A suitable value for the external ramp can be chosen to provide necessary damping for these poles [3] and [6].

Two high-frequency poles are required for accurate modelling unlike the previous averaged models. The system can do away with one pole only if a sufficiently large compensation is added [3].

The disturbances in line and load can be nullified by choosing appropriate compensation [3]. The null occurs at the point where the compensation is half the falling slope of inductor current. This is possible only with a model which has feed-forward terms from the input voltage [3] and [6].

## 7.2 Kazimierczuk's Model

This model proposed by Kazimierczuk uses a switch model which is not invariant for all the converters, unlike the model proposed by Ray Ridley. This model also predicts the instability of the current-mode control at a duty cycle of 50 percent in CCM [1].

Another important difference between the models lies in the modelling of sampling gain. The discrete-time model, in this case, has been approximated to a continuous time expression using a second order Padé approximation. This approximation leads to a transfer function with two imaginary conjugate poles in the LHP or RHP, depending on the value of $a$. While in the continuous-time model, the sampling gain has two zeros [1], [10], [1], and [7].

The current-loop gain has a pair of complex conjugate poles at a 50 percent duty ratio, unlike the continuous-time model, which has zeros due to a different mathematical approximation for the discrete-time expression [1] and [3].

## 7.3 Average Current-Mode Control Scheme

In this scheme, it is the inductor average current which is controlled unlike the peak inductor in previous models. Hence, this method controls the real averaged current [4] and [5].

When this scheme is applied to a PWM dc-dc buck converter, the output current is also controlled due to averaging. i.e the converter behaves as an ideal current source [4] and [5].

In case of a boost converter, the input current represents the inductor average current due to a different converter topology wherein the inductor is at the input side. Therefore, this scheme can be used for power factor improvement when applied to boost topology [4] and [5].

The small-signal characteristics differ significantly from the previously derived

models due to the presence of the RC circuit in the inner loop [4], [5], and [3].

The inner loop always changes the phase by 180° at high frequencies regardless of the combination of gain chosen from the RC circuit [5]. While designing, if the positioning of second pole of the RC circuit is done after the nyquist frequency, necessary damping can be provided to avoid peaking conditions, and the sampling gain same as that used previously is applicable in this scheme as well[4], [5], and [3].

The control-to-output voltage gain has more phase delay than that of peak current mode control due to the existence of the second pole in the compensator. The peaking of the complex conjugate poles can be controlled by selecting a proper combination of the compensator gain as well as the external ramp. This provides more design flexibility [4], [5], and [3].

Despite all these advantages, when it was tested with hardware by the researchers, this model showed more susceptibility to noise. As a result, there is still room for a better design of average current mode control scheme [5].

## 7.4 Recommendations for the future work

The exploration of current-mode control scheme in digital controllers is one of the key potential areas for research. Current-mode control, though immune to over-current protection and short-circuit protection, it is less immune to noise compared to voltage current-mode control [2], [1], and [3]. There's room for creating a model which can overcome the noise issues. The peak-current mode control uses fixed ramp for compensation [1]. A model can be created similar to average current-mode control model [5], which deals with the noise issues as well as provides more design flexibility. It will also be a challenge to use digital controllers to the performance level for current-mode control since they have to delay for a full cycle.

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