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Fall 2008

CEG 360/560 EE 451/651: Digital System Design

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Wright State University
College of Engineering and Computer Science
Department of Computer Science and Engineering

Digital System Design

CEG 360/560 - EE 451/651

Fall Quarter, 2008

Professor: Travis E. Doom, Ph.D.

Professor's Office: 331 Russ Engineering Center

Office Hours: 1:00-2:00 T TH. Other office hours by appointment (via email).

Email: (Preferred contact) doom@cs.wright.edu

Office Phone: (937) 775-5105

Room & Time:

Section 01: 2:15 - 3:30 T TH 161 Rike

Laboratory: 355 Russ Engineering Center

Course Description:

Design of digital systems. Topics include flip-flops, registers, counters, programmable logic devices, memory devices, register-level design, and microcomputer system organization. Students must show competency in the design of digital systems. 3 hours lecture, 2 hours lab. Prerequisite: CEG 260.

Textbook:

Required: Vahid, Frank (2007). "Digital Design", First Edition, John Wiley and Sons, ISBN 978-0-470-04437-7.

Reference: Mano, Morris and Kime, Charles (1997). "Logic and Computer Design Fundamentals", any edition, New Jersey: Prentice-Hall, ISBN 0-13-031486-2 (2e), 0-13-140539-X (3e).

Prerequisites: CEG 260 or equivalent

1. Fundamentals of Boolean Algebra, including the minimization of logic functions to SOP or POS form.
2. Analysis of logic circuits.
3. The design and testing digital designs using SSI and MSI components.
4. Optimizations techniques to minimize gate count, IC count, or time delay.
5. The design and use of simple memory devices and sequential circuits
6. Decoders, multiplexors, and bus logic.
7. Documentation standards for logic designs.

Objectives: This course has two primary objectives. The first is content-based. We hope to teach students the fundamental principles of design for sequential digital devices. At the end of this course,

than one week late. Corrupt files or other computer problems will not be considered a sufficient excuse to extend this deadline. It is your responsibility to back-up your work. I strongly suggest that you save your work to multiple storage media to aid in the recovery of corrupt files.

Examinations: Four 1/2-hour midterm examinations and one final examination will be administered as announced throughout the quarter. Midterm examinations are "extended homeworks" and are designed to encourage students to cover course material at a steady pace and to provide feedback throughout the quarter. All students may drop their lowest quiz grade automatically. Thus, make-ups of 1/2-hour examinations are only permitted for documented emergencies on two or more quiz dates.

It is neither possible, nor desirable, to discuss every nuance of the material covered in this course during our limited class time. Students should be aware that although we will discuss the most important materials in class, the textbook contains important facts that may not be discussed in class. Students should not only be able to discuss course concepts in detail, but they should also be able to demonstrate their mastery by applying these concepts on examinations to related problems with which they have no previous experience.

Undergraduate students: The examinations will be closed-book but undergraduate students may use one sheet of 8.5 x 11" notes (double-sided) as reference. Four such sheets may be used on the Final.

Graduate Students: Graduates students are expected to master this material and commit it fully to memory. Graduate students may not use notes during the examination.

Midterm examinations will occur at the normally scheduled class time and location unless announced otherwise in class. The final examination is cumulative and will take place during the university scheduled time period in the normally scheduled class location unless announced otherwise in class.

Course Assignments: The instructor will provide a number of opportunities for students to develop their mastery of the subject throughout the course through ungraded course assignments. Homework will be assigned at the end of each class period as recorded in the on-line class schedule. Homework assignments should always be completed as if they were to be turned in and added to the student portfolio. Students are encouraged to work on homework problems in collaborative groups.

Each student is expected to keep a portfolio of course material. This portfolio should consist of a 3-ring binder containing returned examinations, lecture and textbook notes, textbook problems corresponding to the assigned readings, documented excuses for absences, and other course material. Your *course portfolio* (in conjunction with your lab notebook) is the physical representation of your course effort and may be a factor in determining "border-line" grades; take care not to misplace it!

Students who follow the majority of the lecture material during class, complete the assigned readings and homework problems in full, and ask questions when confused will be well prepared to get a B on examinations. Exceptional students who, additionally, prepare for lectures by reading ahead, come to lectures with points of confusion identified in advance, spend time discussing class topics in small groups, and actively seek the answers to these questions both in lecture, via email, and during office hours are the most likely to achieve an A on examinations and in the course.

Academic Integrity : Student-teacher relationships are built on trust. For example, students must trust that teachers have made appropriate decisions about the structure and content of the courses that they teach, and teachers must trust that the assignments which students turn in are their own. Acts which undermine this trust undermine the educational process. It is the policy of Wright State University to uphold and support standards of personal honesty and integrity for all students consistent with the goals of a community of scholars and students seeking knowledge and truth. Furthermore, it is the policy of

newsgroup is used by the instructor and laboratory instructor to make class announcements as well as by students to arrange study groups, discuss homework problems, bring up class related issues, etc. The newsgroup is an open forum, anyone may ask/answer any questions posed to the group. All students should check the newsgroup on a weekly basis.

Additional Needs: Students with disabilities or any additional needs are encouraged to set up an appointment at their convenience to discuss any classroom accommodations that may be necessary.

CEG 360/560 - EE 451/651 Web Page: <http://www.wright.edu/~travis.doom/courses/CEG360>

Dr. Travis Doom, doom@cs.wright.edu.

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Digital System Design

CEG 360/560 - EE 451/651

Fall Quarter, 2008

Section I: Digital System Analysis and Review		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 9/9	Class overview, review of combinational digital devices, and bistable elements	Review: Vahid, Ch. 1, 2, 6.2, Appendix A; (Review: Mano, Ch. 1-5); Prepare for entrance survey (ungraded quiz); Lab #0
R 9/11	Entrance survey and completion of combinational review	Review: Vahid, Ch. 4.3, 4.4, 4.5, 4.8, 4.9; (Review: Mano, Ch. 1-5); Lab #0
T 9/16	Review of sequential devices, clocked synchronous state machines, characteristic equations, timing	Read: Vahid, Ch. 3.1, 3.2, 3.5; (Read: Mano, Ch. 6.0-6.3); Lab #1a
R 9/18	CSSM analysis, input/excitation equations, state tables, CSSM models, state diagrams, CSSM timing	Read: Vahid, Ch. 3.3; (Read: Mano, Ch. 6.4, Class notes, Timing Tutorial); Study for Half-hour Exam #1; Lab #1a
T 9/30	Half-hour Exam #1	Refer to next section

Section II: Digital System Design and Synthesis		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 9/23	Translating a design into a state diagram	Read: Vahid, Ch. 3.3; (Read: Mano, Ch. 6.5); Lab #1b
R 9/25	Designing with state diagrams, implementing a design with D-type or JK-type flip-flops	Read: Vahid, Ch. 3.4, 5.4; (Read: Mano, Ch. 6.6); Lab #1b
T 9/30	State minimization and assignment in CSSM design	Read: Vahid, Ch. 6.3; (Read: Mano, Ch. 6.5); Lab #2a
R 10/2	Muxes as next-state generators, ad-hoc design, finite memory machines, hierarchical design/testing.	Read: Class Notes; Study for Half-hour Exam #2; Lab #2a
T 10/14	Half-hour Exam #2	Refer to next section

Section III: Design with MSI, LSI, and VLSI Devices		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT

T 10/7	Registers, counters, and register transfers	Read: Vahid, Ch. 4.1, 4.2; (Read: Mano, Ch. 7.1, 7.6); Lab #2b
R 10/9	Design decomposition	Read: Class notes; (Read: Mano, Ch. 8.2-8.3); Lab #2b
T 10/14	Designing with ASM charts	Read: Vahid, Ch. 5.6, Ch. 7; (Read: Mano, Ch. 3.6); Lab #3a
R 10/16	LSI/VLSI Devices: PLDS, ROM, and RAM	(Read: Mano, Ch. 9); Study for Half-hour Exam #3; Lab #3a
T 10/28	Half-hour exam #3	Refer to next section

Section IV: Digital System Organization		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
T 10/21	Register files, function units, and datapath control words	Read: Vahid, Ch. 5.1-5.3; (Read: Mano, Ch. 7.2-7.3, 7.5); Lab #3b
R 10/23	Pipelining	Read: Vahid, Ch. 6.5; (Read: Mano, Ch. 10.1-10.6, 12.1); Lab #3b
T 10/28	The control unit: design, hardwired vs. microprogrammed control, programmable control units, the machine cycle	(Read: Mano, Ch. 8.1, 8.4, 8.7); Lab #4a
R 10/30	A simple computer architecture (lab 4)	Read: Vahid, Ch. 8.1-4; (Read: Mano, Ch. 10); Lab #4a
T 11/4	ISA design: CISC vs. RISC, data and control hazards;	(Read: Mano, Ch. 12.1-12.3); Lab #4b
R 11/6	Contemporary microcomputer architecture	Lab #4b
T 11/11	Half-hour Exam #4 Instructor evaluation; Exit survey	Study for final examination; Lab #4c

Final Examination		
DATE	TOPIC / ACTIVITY	HOMEWORK ASSIGNMENT
R 11/13	Course Review	Study for final examination; Lab #4c
R 11/20	Section 01: Final examination, 3:15-5:15	Regularly scheduled class room

This page was last modified on Monday, 25-Aug-2008 15:29:45 EDT. Assignments prior to this date should be accurate. Assignments listed after this date are *projections* and may not correspond to the actual material and assignments presented in class.

The most recent version of this document is available on the world wide web via:
<http://www.wright.edu/~travis.doom/courses/CEG360>

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