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Costas PLL Loop System for BPSK Detection

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COSTAS PHASE LOCKED LOOP FOR BPSK DETECTION

A thesis submitted in partial fulfillment
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by

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY RAJESH KUMAR KEREGUDADHAHALLI ENTITLED Costas Phase Locked Loop For BPSK Detection BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering.

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Abstract

Keregudadhahalli, Rajesh Kumar. M.S. Egr., Department of Electrical Engineering, Wright state University, 2008. Costas Phase Locked Loop for BPSK Detection.

A 2GHz carrier recovery Costas Loop based BPSK detector is designed using CMOS 0.18μm technology. The designed BPSK detector consists of single to differential conversion circuit, phase/frequency detector, Voltage Controlled Oscillator, differential to single conversion circuit, first order loop filter and a third multiplier. Different architectures available for each block have been discussed along with the design methodology adopted. The schematics were simulated in analog design environment.

The Costas loop presented in this work can sense both 0° and 180° phases at its input. Thus the Costas loop carrier recovery circuit overcomes the 180° phase ambiguity presented by the conventional PLL. The designed Costas loop for BPSK detection is able to detect and demodulate data rates up to 50Mbps. The loop can track with in the VCO frequency range of 1.99GHz to 2.01GHz. The lock range achieved for this loop is 20MHz. The power consumption of the Costas Loop BPSK detector was found to be 144mw.

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ACRONYMS

PLL   -   Phase Locked Loop

VCO   -   Voltage Controlled Oscillator

ASK   -   Amplitude Shift Keying

FSK   -   Frequency Shift Keying

BPSK   -   Binary Phase Shift Keying

AM   -   Amplitude Modulation

FM   -   Frequency Modulation

SSB   -   Single Side Band

SM   -   Space Modulation

OOK   -   On-Off Keying

QAM   -   Quadrature Amplitude Modulation

MSK   -   Minimum Shift Keying

CPM   -   Continuous Phase Modulation

PPM   -   Pulse-Position Modulation

TCM   -   Trellis Coded Modulation

OFDM   -   Orthogonal Frequency-Division Multiplexing

FHSS   -   Frequency-Hopping Spread Spectrum

DSSS   -   Direct Sequence Spread Spectrum

CMOS   -   Complementary Metal Oxide Semiconductor

PMOS   -   p-Channel Metal Oxide Semiconductor

NMOS   **-**   n-Channel Metal Oxide Semiconductor

IC   **-**   Integrated Circuit

VCV   **-**   VCO Correction Voltage

AFC   **-**   Automatic Frequency Control

Acknowledgements

Firstly I would like to thank my Parents, Prema and Aswathaiah for being so supportive throughout my master's degree. I want to thank my sisters, Ashwini and Pramila for inspiring me to get this degree and make my dream come true.

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INTRODUCTION

1.1   BACKGROUND

Today, microprocessor design is running through some enormous changes to enable and optimize the key survival factors such as Speed and power to the world of microprocessor design. The semiconductor technology is also rapidly changing to cope-up with some of the major requirements like speed, power, clock-skew and signal synchronization. The high-end systems performance degradation could result, if the clock-skew and clock synchronization issues are not properly dealt with.   The performance of the microprocessor has improved at the surprise rate of doubling every 18 months resulting hike in their operating frequency and thus leading the Input/output circuit speed [11].

Phase locked loops (PLL) was found to be the most efficient way to address these issues. PLL has a variety of applications which could address most of these issues. On-chip signal integrity and Chip-to-chip signal integrity is avoided by clocking the chip faster than the bus speed. Here PLL could be used to generate lower and higher frequencies required for a bus and Chip respectively. The clock frequencies with multiple-phase could be generated using PLL suiting different applications. Also PLLs could be used to generate a frequency output with respect to the input digital word.

Usage of PLLs has led to some of the innovations such as embedded microcontrollers, personal computer, advanced workstations, applications and file servers, web servers for the internet, large-scale computing clusters, handheld and mobile devices.

1.2 What is PLL?

A **phase-locked loop** is a closed loop control system that generates a signal that has a fixed relation to the phase of a "reference" signal that is present at its input. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, which will automatically increase or decrease the frequency of a controlled oscillator until it is matched to the reference signal in both frequency and phase. The basic block diagram of a PLL is shown below,
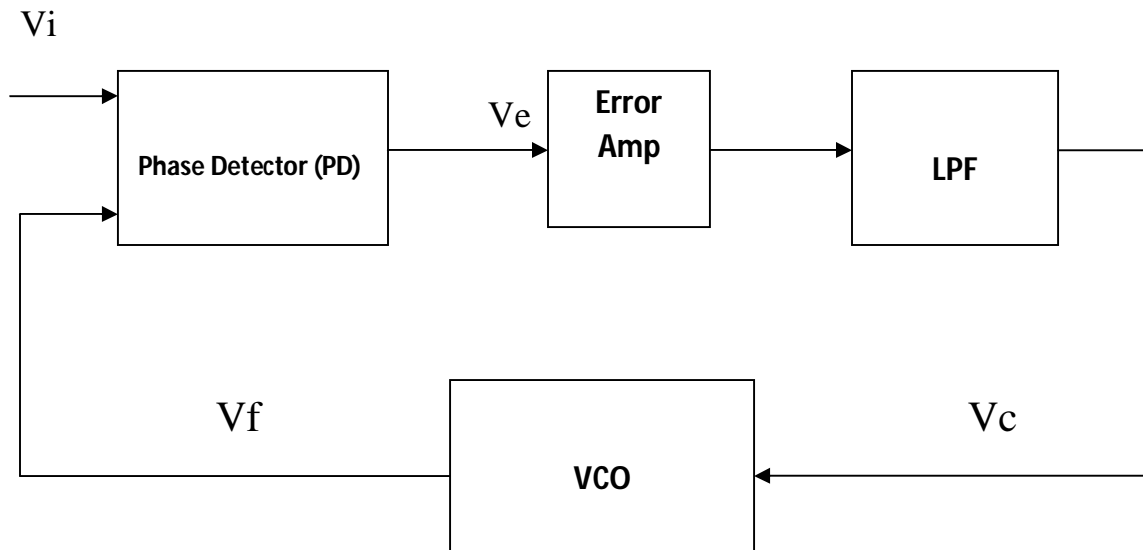
Figure 1.1: Basic PLL Model

The basic model of PLL consists of phase detector, Error amp, low pass filter and a Voltage controlled oscillator. The feedback loop automatically corrects any phase/frequency difference between the incoming frequency and the VCO generated signal.

1.3 Evolution of PLL

In the early 1930's super-heterodyne receiver was mainly used for the signal detection which was designed by Edwin Howard Armstrong in 1918 for the Army Signal Corps of France [2]. The super-heterodyne receiver was extended far beyond the commercial broadcast applications like microwave radar receivers developed during World War II. To eliminate the number of tuned stages that super-heterodyne receiver had a simpler method was found. As a method to eliminate the disadvantage of the super-heterodyne receivers, a French engineer Henri De Bellescize designed and implemented the first PLL in 1932. The first implementation of his invention was a vacuum tube based synchronous demodulator for an AM receiver [1]. The invention and the implementation of the PLL were limited by its expense.   It was found that when the incoming signal and the local oscillator signal was mixed at the same frequency and phase the base band signal that modulated the carrier was able to be recovered. This technique was first implemented on electronic motor systems and then was soon realized on oscillators which led to the evolution of Phase-Locked Loop. PLL was then used in 1943 to realize horizontal and vertical oscillators of a television receiver to synchronize a continuous clocking signal with the transmitted sync pulses [4]. PLL also played a vital role in the evolution of color television. PLL found broad acceptance when the first PLL IC was introduced in the year 1965.

Today, PLL's finds variety of applications which proves its versatility in applications like AM and FM Detectors, FSK Detector, Motor Speed Controller, Frequency Synthesizers, Radio Telemetry, Touch-tone Decoder, Light coupled Analog Isolator, Clock and Data recovery circuits, Robotics etc.

1.4 Applications of PLL

Phase lock loop finds variety of applications and is configured according to the requirements. Some of the PLL applications are listed below,

1) Clock generation

Many applications use different processors to implement its functionality with a different processor speeds. The clock signal is provided to these processors through PLL which can convert a low frequency signal to a high frequency operating frequency of the processor.

2) De-skewing

The Delay-locked Loop is used normally for this application. The clock can be used to sample the data when it is sent along with the data at the transmitter. The receiver uses this clock as a reference to detect the received data pattern. There will be a finite delay between the received clock and the data even though they are transmitted in parallel. The De-skew PLL is used on the receiver side to eliminate this delay and to provide efficient data detection at higher data rates.

Frequency Synthesis

The PLL finds its application in wireless communication systems like GSM, CDMA etc. PLL is used to provide local oscillator for up conversion at the transmitter and down conversion at the receiver. Normally the PLL synthesizers will have a digital word that would select the frequency output.
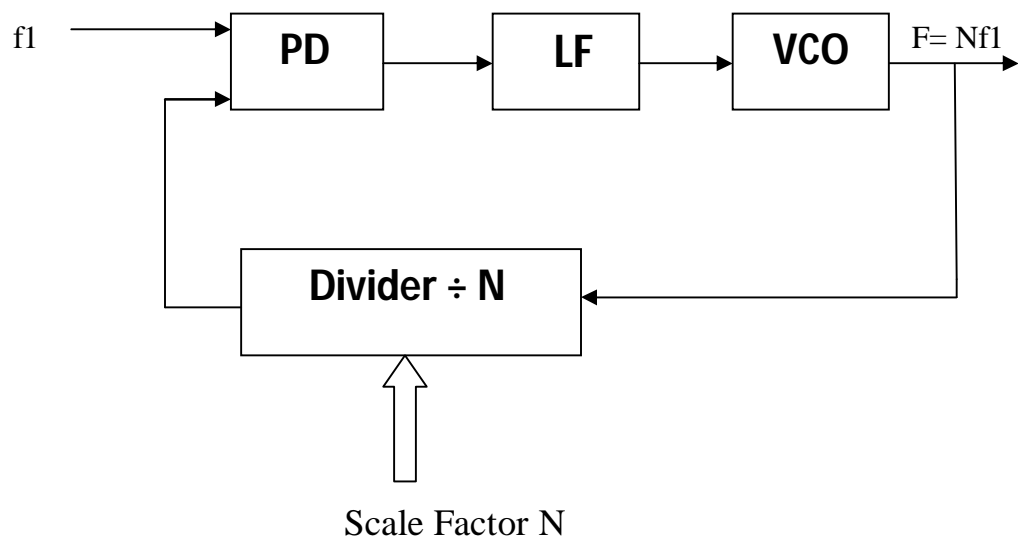
Figure 1.2: Basic Frequency Synthesizer System

A frequency synthesizer is a device that accepts some reference signal and generates a frequency range depending on the command word or control word. The frequency synthesis is achieved with the help of a variable counter (divider) that generates multiple frequencies F by modifying the division ratio N. F=Nf1, where 'F' is the output or desired frequency and 'f1' is a reference frequency.

BASIC ARCHITECTURE OF COSTAS LOOP

2.1   Overview

Amplitude-Shift keying (ASK), Frequency -Shift keying (FSK) and Phase-Shift keying (PSK) are the three basic types of digital modulation techniques. In digital modulation scheme, an analog carrier is modulated by a digital data bit stream. In BPSK we change the phase of the sinusoidal carrier to represent information bit. The information bit '0' is transmitted by shifting the phase of the sinusoid by 180° and information bit '1' is transmitted without any phase change in sinusoid i.e. with a 0° phase shift. Binary-Phase shift keying is one of the most efficient binary data modulation techniques in terms of noise immunity per unit bandwidth. The basic block diagram of the Costas loop for BPSK is shown below,
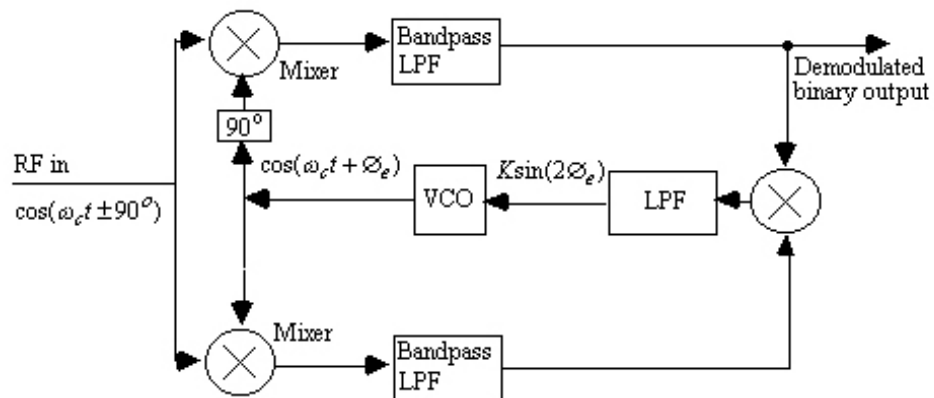
Figure 2.1: Basic Block of Costas Loop for BPSK

The BPSK demodulation using conventional PLL presents $180^{°}$ phase ambiguity whenever the data signal changes its phase from 0˚ to 180˚ and vice versa. Thus the demodulated data signal will be the reverse of the data that is originally transmitted that is not desirable. The solution to overcome this 180˚ phase ambiguity is the Costas Loop. The Costas Loop can sense both the 0˚ and 180˚ phases at its input. Thus when the incoming data reverses its phase the loop will not anti-lock and still detect the data in the order it was transmitted.

To optimally demodulate the BPSK signal meaning to recover the data that was transmitted the frequency and phase of the carrier needs to be exactly reproduced at the receiver end. The Costas loop consists of two branches namely 'I' branch which is a coherent branch since the signal with same phase will be multiplied coherently to demodulate the data and the 'Q' branch is called orthogonal branch since the incoming BPSK signal is multiplied by an orthogonal carrier. The output of these two 'I' and 'Q' branches are multiplied again to obtain a phase difference which is again converted into proportional DC voltage. The DC control voltage is proportional to the phase difference between incoming RF signal and the internally generated carrier. In this paper the mathematical analysis of Costas loop for BPSK is done which proves that the I-coherent branch will detect and demodulate the transmitted data.

2.2   Modulation Techniques

Types of Modulation Techniques

The figure below shows different types of modulation techniques under Analog, Digital and Spread spectrum modulation methods,

```
                    ┌──────────────────────────────┐
                    │   Modulation Techniques       │
                    └──────────────────────────────┘
                              │
              ┌───────────────┴───────────────┐
              ▼                               ▼
      ┌──────────────┐               ┌──────────────┐
      │   Analog     │               │   Digital    │
      │  Modulation  │               │  Modulation  │
      └──────────────┘               └──────────────┘
              │                       ┌───────┴────────┐
              ▼                       ▼                ▼
  ┌────────────────────┐  ┌──────────────────────┐ ┌──────────┐
  │                    │  │ ASK, FSK, PSK, OOK,   │ │          │
  │                    │  │ QAM, MSK, CPM, PPM,   │ │   FHSS,  │
  │ AM, SSB, FM, PM, SM│  │ TCM, OFDM             │ │   DSSS   │
  └────────────────────┘  └──────────────────────┘ └──────────┘
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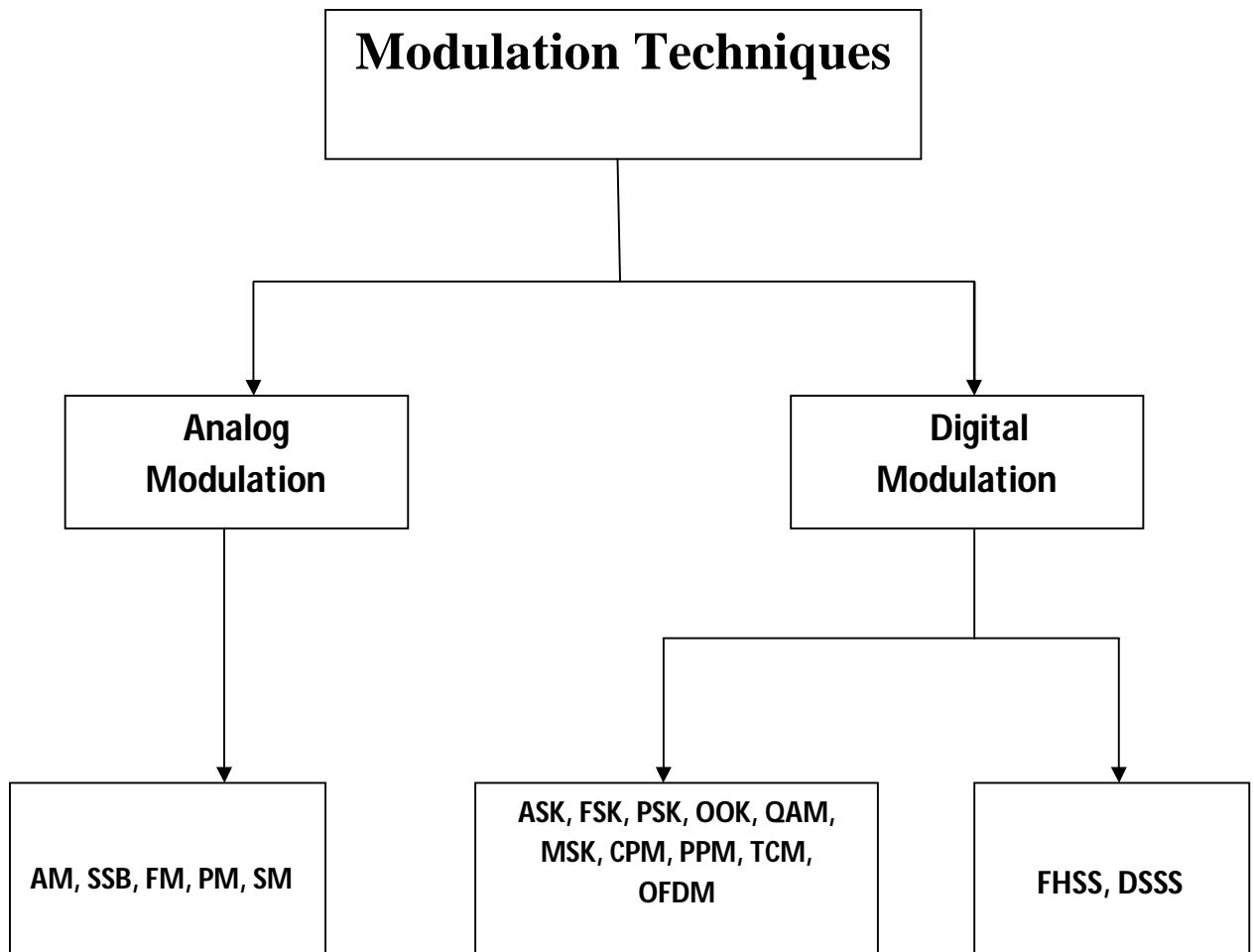
Figure 2.2: Types of Modulation Technique

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2.2.1 Digital Modulation

The three basic digital modulation technique are ASK, FSK and PSK.

2.2.1.1   Amplitude Shift Keying

Amplitude shift keying (ASK) is one of the basic digital modulation schemes available in a digital communication system. Amplitude shift keying also know as on-off keying since a high frequency carrier is turned on or off to represent a binary '1' or '0' respectively. The on-off keying has some of the drawbacks like steep transients due to the switching of high frequency carrier which in turn will broadens the signal spectrum of interest [1]. It still finds some applications due to some of its advantages like low bit rates specific applications and in low bandwidth application. The receiver built using a PLL would be a PLL tuned to the center frequency of the carrier signal. The basic plot of the Amplitude shift keying is shown below,
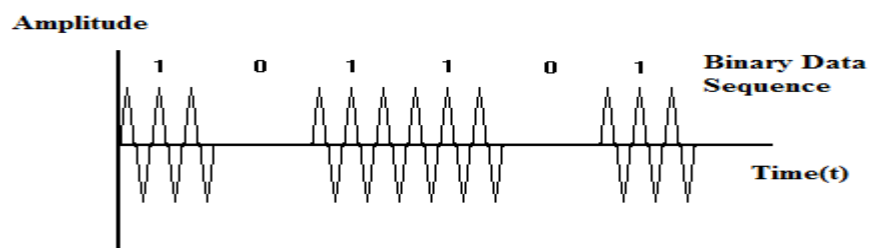
Figure 2.3: Amplitude Phase Keying

2.2.1.2   Frequency Phase Keying

Frequency shift keying (FSK) is a digital modulation technique in which two different frequencies are transmitted to represent a binary data signal. Here two frequencies are selected like may be fq1 to transmit symbol '0' and fq2 to transmit symbol '1'. This type is called non-orthogonal FSK. If these two frequencies have a phase difference with respect to the relationship $fq_i = k_i * 1/2T_s$ [1], which means both the symbols are integer multiples of half the symbol rate. The orthogonal FSK is very useful when it comes to recover the signal that is buried in noise.   The non-orthogonal FSK can cause some sharp transients due to the abruptly changing the two frequencies which would lead to the extension of the bandwidth in an undesired manner. The minimum phase shift keying is another modulation technique used to avoid this drawback since in MSK every symbol starts and ends with a zero crossing of the same direction [1]. The FSK technique is shown below,
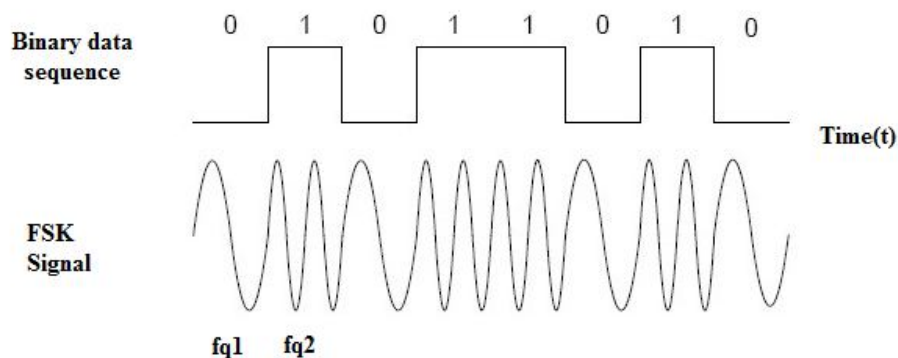
Figure 2.4: Frequency Shift Keying

2.2.1.3   Phase Shift Keying

Due to its low noise immunity per bandwidth Phase Shift Keying is the most widely used modulation technique in digital communication system today [5]. The Phase Shift Keying is again has different techniques like Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), m-ary Phase Shift Keying (QAM). The QPSK and QAM are bandwidth efficient since they can more information bits per symbol transmitted. The Binary Phase Shift Keying (BPSK) is a digital modulation technique where in '0˚' carrier phase is transmitted to represent symbol '1' and a 180˚ phase shifted carrier is transmitted to indicate symbol '0' and vice-versa if it is desired or required. The phase can take only two values for BPSK which is 0 or π, since each phase represent only one symbol at a time. The BPSK technique is shown in the next page,

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Carrier Signal
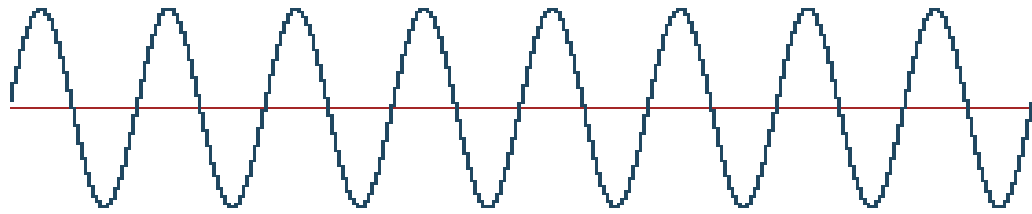
Modulating Wave (digital)

0   1   0   0
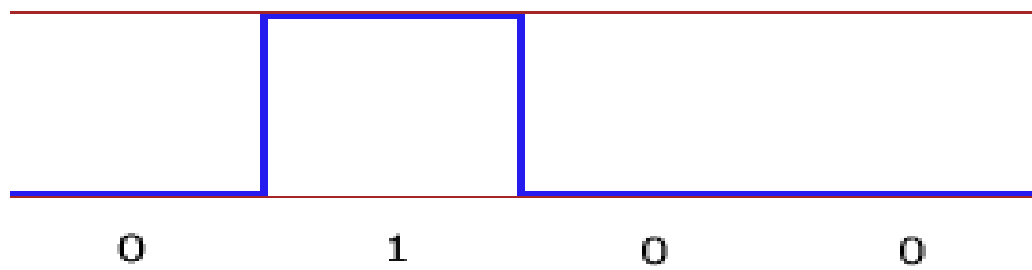
Modulated Result
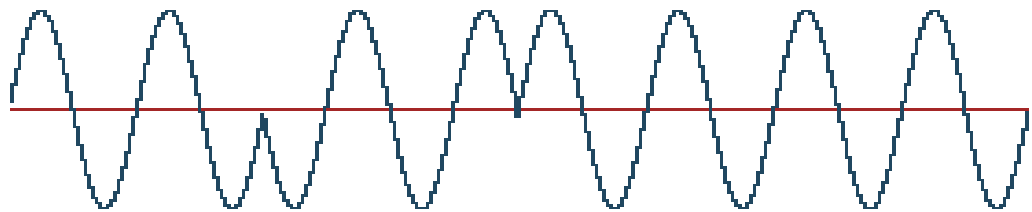
Figure 2.5: Binary Phase Shift Keying

2.3   Phase Detection

Phase detector is a frequency mixing circuit that would give an output voltage that is proportional to the phase difference between the two input signals. Phase detection is very vital in many applications such as motor speed control, servo mechanisms, demodulators, radar and telecommunication systems [14]. Phase detection is an important part of the Phase Locked Loop. Different types of Phase detectors are used in today's PLL based applications. They are basically divided into two types as,

1. Memory Less Phase Detectors and

2. Sequential Phase Detectors

2.3.1   Memory less Phase Detector

The name memory less is due to the reason that these phase detectors does not have any kind of a sequential components involved in their design. They are simply multiplier-type circuits as their output is a product of two inputs signals. These multipliers are very useful for high frequency applications as they can provide the product of high frequencies applied to its input. The following stages of this phase detectors could be designed accordingly to remove any high frequency noise or unwanted signal present at its output. Apparently some of these detector types can only provide the phase difference but not the frequency difference. Some of the memory less phase detectors are,

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1. Exclusive-OR Gate

2. Diode ring oscillator

3. Single balanced Mixer

4. Doubled Balanced Mixer

a. Exclusive-OR gate

An Exclusive-OR gate is a digital gate which will give an output high '1', when it has got non-linear inputs and an output low '0' when it has linear inputs. Thus Exclusive-OR gate is also known as non-linear gate. The truth table of the two input Ex-OR gate is shown in the table 2.1. Its output is high '1' when inputs are not equal and its output is low '0' when inputs are equal. The Ex-OR gate could be used only when mixer as digital waveform at its input, since it cannot follow the instantaneous changes of the input signal. The Ex-OR gate exhibits input-dependent skew, meaning that delay from the input changing to the output changing is different depending on which input is changed or selected. The circuit symbol of Ex-OR gate is shown in the next page,
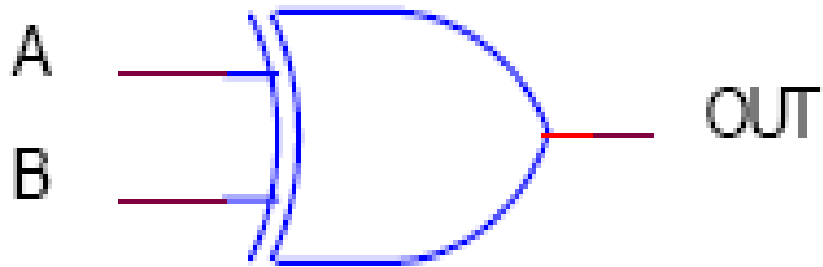
Figure 2.6: Circuit Symbol of Ex-OR gate

Truth Table		
A	**B**	**A ⊕ B**
0	0	0
0	1	1
1	0	1
1	1	0

Table 2.1: Truth Table of Ex-OR Gate

b. Diode Ring Double – Balanced Mixer

The arrangement of a diode ring double – balanced mixer is shown in the figure 2.7. The arrangement has two ports namely local oscillator LO port and RF port. The local oscillator signal is applied to the LO port and an incoming RF signal is applied to the RF port. The LO port will switch the diodes on to the left hand side once and right hand side once alternatively depending on the polarity of the VCO generated reference signal. Accordingly we will have the product of local oscillator signal and RF signal available at the Intermediate frequency IF port. This signal obtained at the IF port is then passed through the filter to remove the unwanted signal. The output after filtering will be a demodulated data signal.
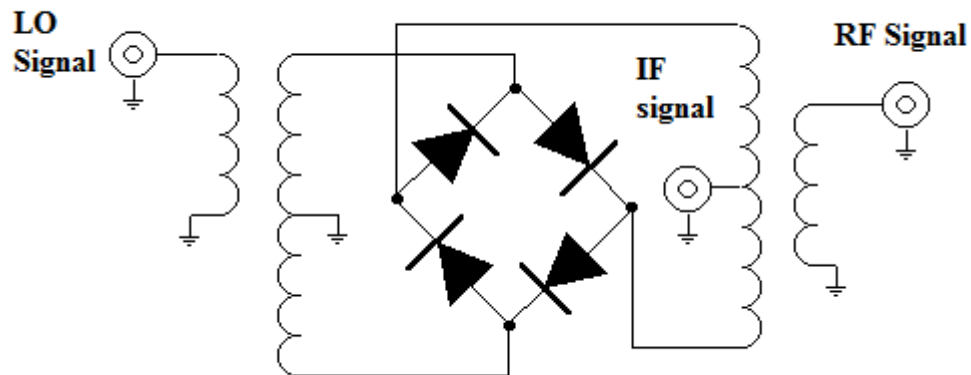
Figure 2.7: Diode Ring Double – Balanced Oscillator

c. Single Balanced Mixer

The single balanced mixer is as shown in the figure 2.8,
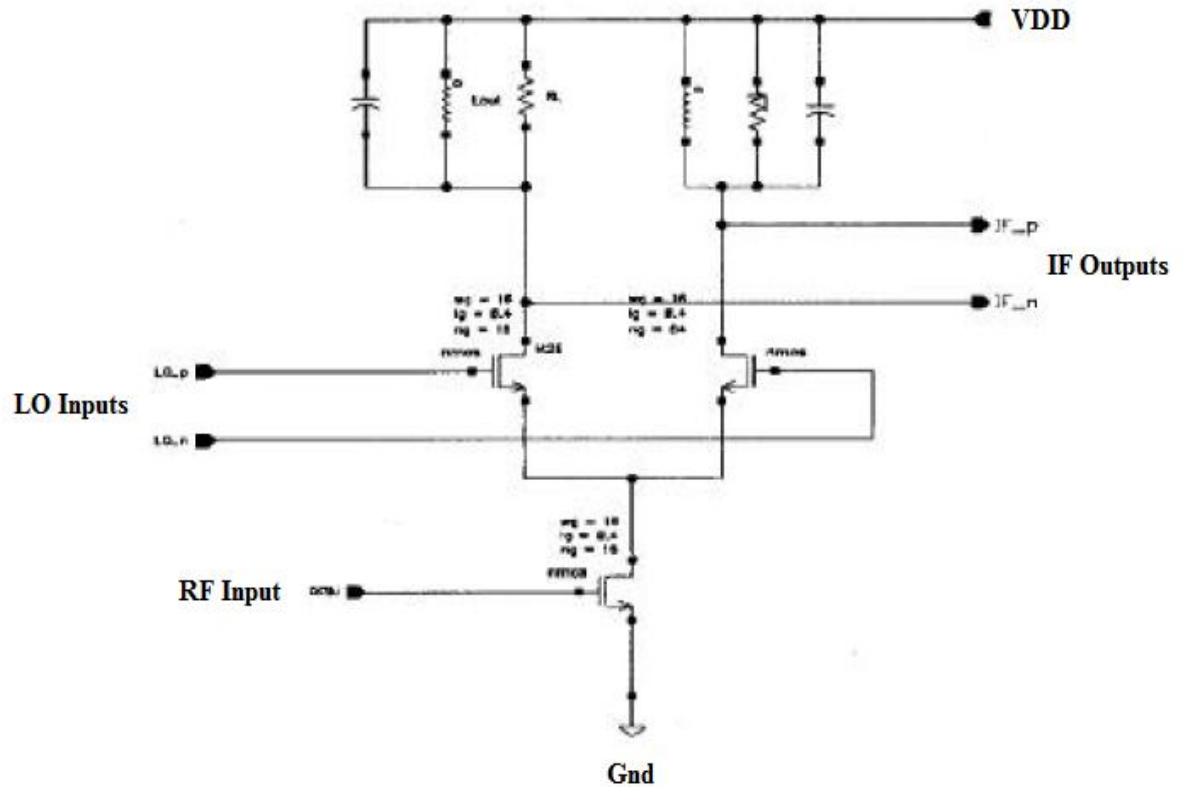
Figure 2.8: Single Balanced Mixer

This is one of the simplest and easiest mixers that could be implemented in a process. It offers the most desired single ended input for ease of operation. The single balanced mixer has a differential LO inputs that would switch the one of the upper or switching transistors at a time depending on the polarity at its input.

Thus the incoming RF signal gets multiplied by one of the LO inputs depending on which transistor is turned on at that point of time. The drawback of this mixer is there is no port-to port isolation since one of its inputs is not differential which in turn would lead to LO feed-through and RF feed-through at the IF port. This simplicity of this mixer has to trade-off with moderate gain and low noise figure. However, the design has low 1-db compression point, low input Ip3, Low port-to-port isolation and high input impedance [15]. The figure 2.8 shows a tuned load single balanced mixer which can have a resistive load depending on the IF frequency and the gain requirements.

d. Doubled Balanced Analog Mixer or Multiplier

A Gilbert cell double balanced analog mixer is as shown in the figure. A mixer is a non-linear device since it exhibits a non-linear characteristic. The name double balanced mixer is due to its differential inputs and differential outputs configuration. The most popular double-balanced mixer used in the RFIC design today is Gilbert cell mixer [16]. The operation of double balanced Gilbert cell is similar to that of single balanced mixer, but in the former we have four switching transistors and two of them are turned on at once. The differential configuration is very useful for some critical and high accuracy applications since the LO feed through and RF feed through are effectively rejected from appearing at the IF ports. Some of the advantages of the double balanced mixer over single balanced are increased linearity, better RF and LO feed-through rejection, good port-to-port isolation and higher interception points.

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The main drawback of this configuration is the need for Single-to-Double ended and Double-to-Single ended converters and also certain circuit parameters can drift from the designed or expected values.
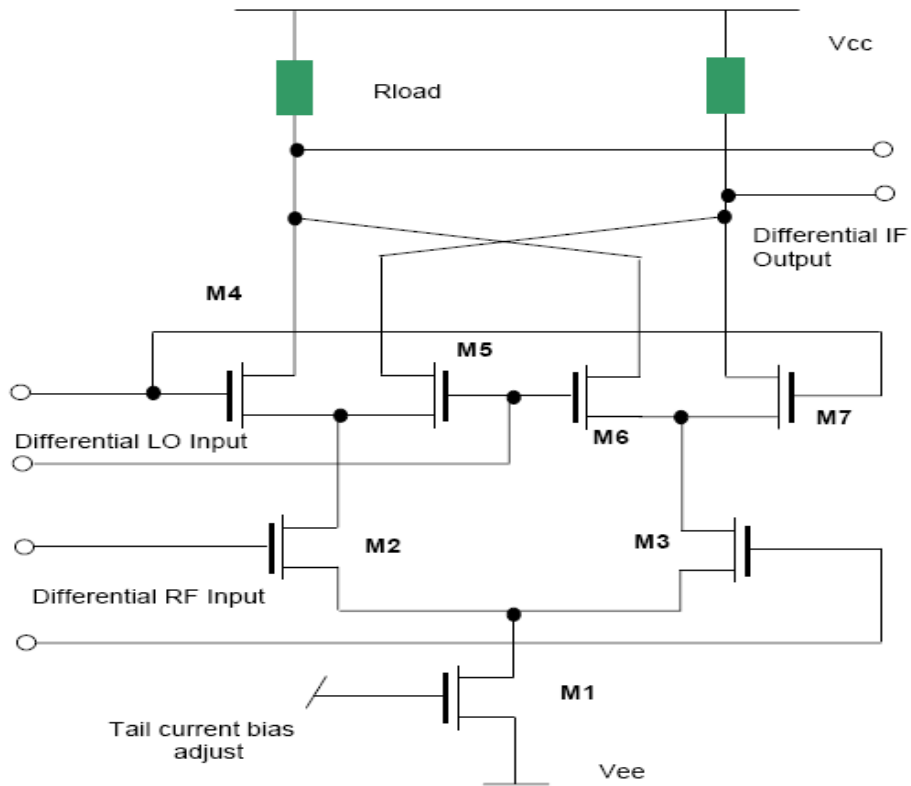

Figure 2.9: Doubled Balanced Gilbert Cell Mixer

2.3.2 Sequential Phase Detectors

The sequential phase detectors as the name suggests will have sequential circuits or components in their design. These detectors are constructed using both of sequential and combinational circuits and thus will have a memory for storing the previous states. The functionality of the sequential phase detectors are such that they can detect both frequency and phase error of the input signal. The output signal of detector generally depends on the two negative edges of the input signals that had occurred previously. The phase error is the linear function over a wide range of frequency with respect to its multiplier-type phase detector counterparts. Since the circuit transition occurs with respect to the clock edges these types of detectors are very useful in an application where in the input signals have very well-defined transitions.

a. Phase Detector with Charge Pump Output

The arrangement of PFD with a passive filter is as shown in the figure 2.10. The arrangement consists of two delay flip-flops, AND gate, NOT gate, Pull-up & Pull-down transistors and a passive filter at the output. The Phase frequency detector unlike the EX-OR gate and JK flip-flop configuration measures the frequency difference between two input signals in unlocked state. The positive and negative current sources are generated by the help of two delay flop-flops.

The circuit operation could be analyzed with respect to its two inputs and four input combinations.

0 0: Both the outputs Q1 and Q2 will be at zero, thus Uf' will be floating or at at high impedance state.

1 1: Both the outputs are high and again disabled by AND gate.

1 0: P is turned ON and N is turned OFF, so output is UB.

0 1: P is turned OFF and N is turned ON, so output is GND.
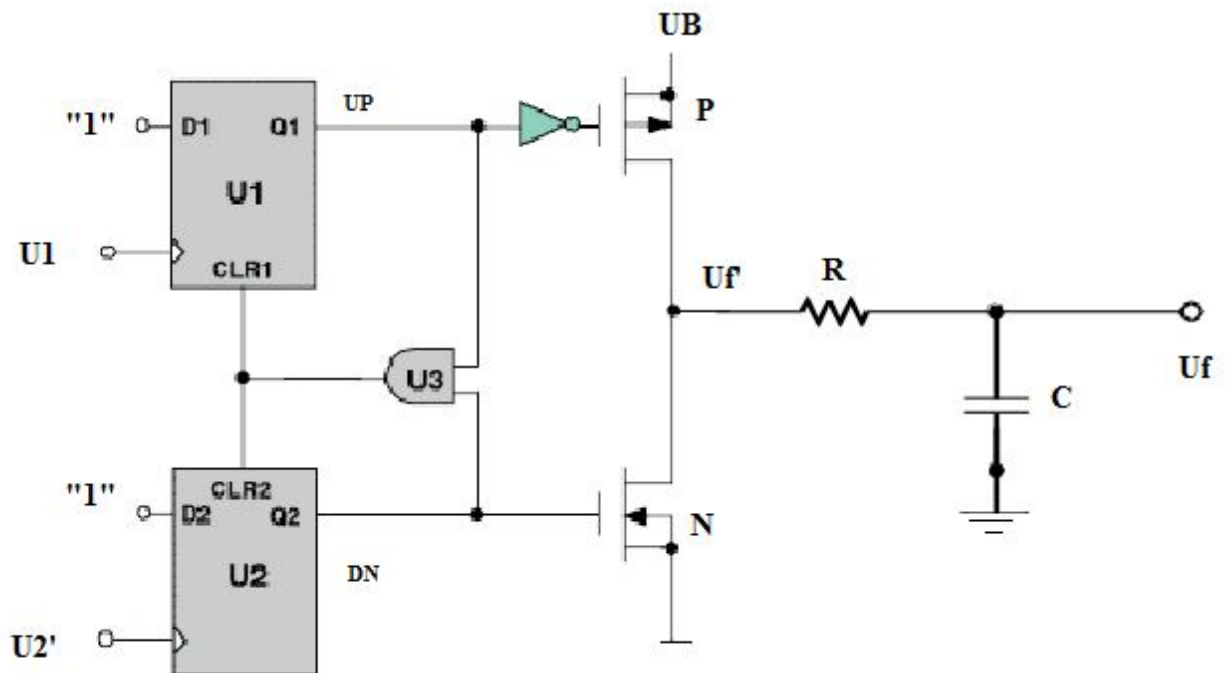
Figure 2.10: Phase Frequency Detector with passive filter

The output of PFD at Uf' for the inputs U1 and U2' is as shown in the figure 2.11 below,
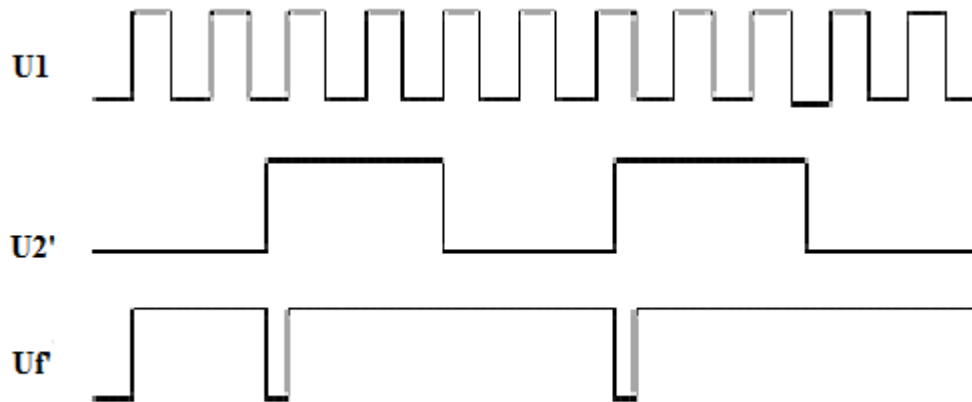
Figure 2.11: PFD waveform at uf'

The wide pull-in range of the PLL is easily achieved with PFD as a phase detector [1]. The phase detectors that have   current output instead of voltage output are said to be Phase detectors with charge pump output. The outputs of two delay flip-flops are controlling two current sources. Depending on which output is set high '1', one current source is driven at a time. In order to get the average loop filter output signal Uf, we need to multiply the PFD output current by the impedance of the loop filter. Phase detectors with Charge pump output could be combined with different types of loop filters which could be either passive or active. In most of the applications passive filters are used since they behave like a real integrator [1].

2.4   Types of Voltage controlled oscillator (VCO)

A VCO is an electronic device that coverts the constant DC power to a periodic signal whose frequency is proportional or a function of the control voltage applied to its input. VCO's are used in many signal processing and communication applications. VCO's can be built for different capabilities and performances depending on the application and the technology it is used in. The controlled oscillators are of voltage and current types depending on whether voltage or current is used as its control voltage. VCO design considerations depends on some of its design requirements such as center frequency, low phase noise, high spectral purity, tuning range and linearity, response time and the design cost [17]. The most important part of PLL is VCO. The VCO's performance inside the loop bandwidth is determined by the loop parameters and its performance outside the loop is determined by VCO design itself. The VCO's can be classified as shown below in the figure 2.12.
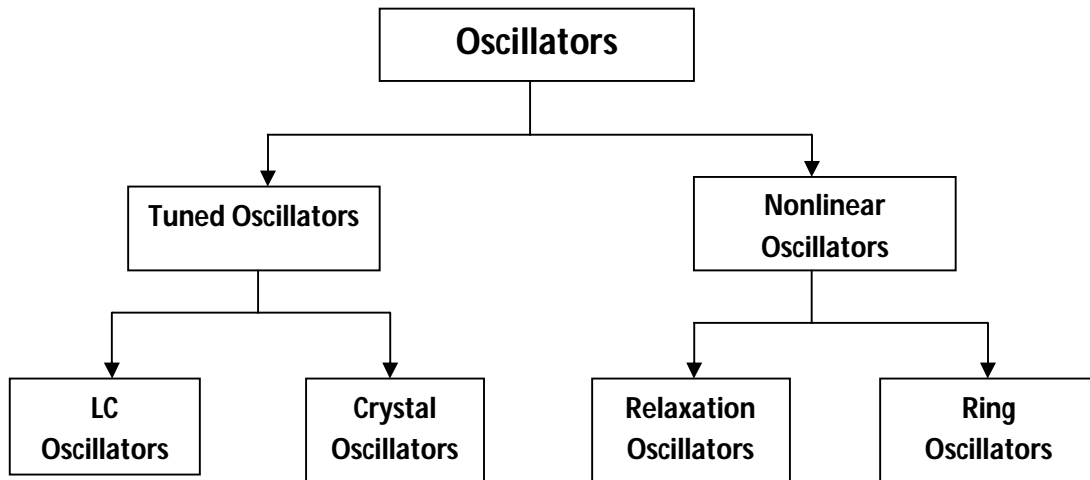
Figure 2.12: VCO Types

2.4.1 Tuned Oscillators

a.   Resonant Circuit Oscillator (LC Circuit)

The LC oscillator basically consists of a transistor and a tank or a resonant circuit. Depending on how the resonant circuit is arranged they are again of two types, one is Hartley oscillator and Colpitts oscillator. Here we can discuss any one two know how the tuned LC oscillators work. Let's take colpitts oscillator in here to understand the operation of the tuned oscillator since they are mostly used in todays PLL based applications. The colpitts oscillator arrangement is as shown below in the figure 2.13,

Figure 2.13: Colpitt's Oscillator

The circuit output oscillation frequency depends on the design of tuned circuit. For instance, if the tuned circuit is designed for 200MHz, then due to the positive feedback concept once the barkhausen criteria is satisfied, we can expect an oscillations at the output running for 200MHz.
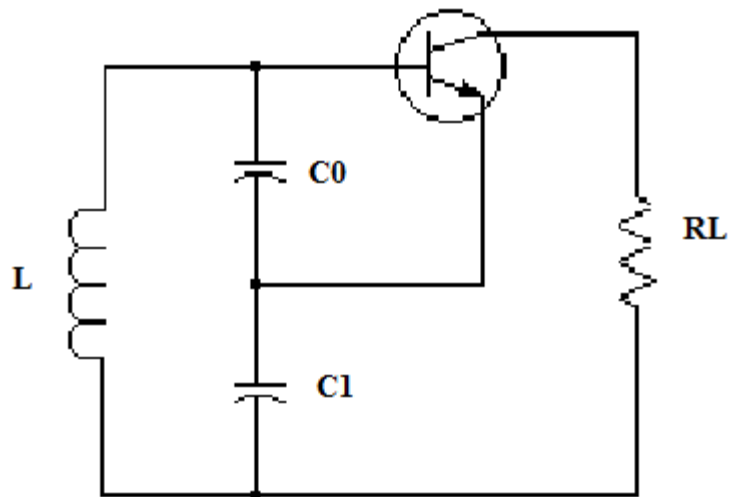
b. Voltage Controlled Crystal Oscillator (VCXO)

A VCXO is designed using a crystal oscillator with Varactor diode and some additional circuitry to control the output frequency over a narrow range with the application of a control voltage. The tuning of the VCO is done by applying a DC voltage across the Varactor diodes to vary the net capacitance applied to the tuned circuit [18]. In a design with critical accuracy, crystal oscillator would be the first choice considering the fact that crystal cannot be integrated with the other circuit components. The basic arrangement of a crystal oscillator is shown in the figure 2.14,

In a VCXO, the crystal can be modeled as inductance and capacitance C_0 and C_1 used to adjust the amount of feedback. The application of a control voltage will cause the capacitance of the varactor diode C_{V1} and C_{V2} which in turn affects the crystal model thus causing the change in the frequency of oscillation. The shunt capacitors C_{S1} and C_{S2} will provide the offset and tuning in the center frequency. The resonant frequency of the VCXO shown is given by,

$$fc = \frac{1}{2\pi\sqrt{L1C1}} \sqrt{1 + \frac{C1}{C0+CL}}$$

Where $C_L = (C_{V1}+C_{S1}) \,||\, (C_{V2}+C_{S2})$

        The main advantage of the voltage controlled crystal oscillator is that it offers very good thermal stability, high linearity and an excellent spectral purity [17].
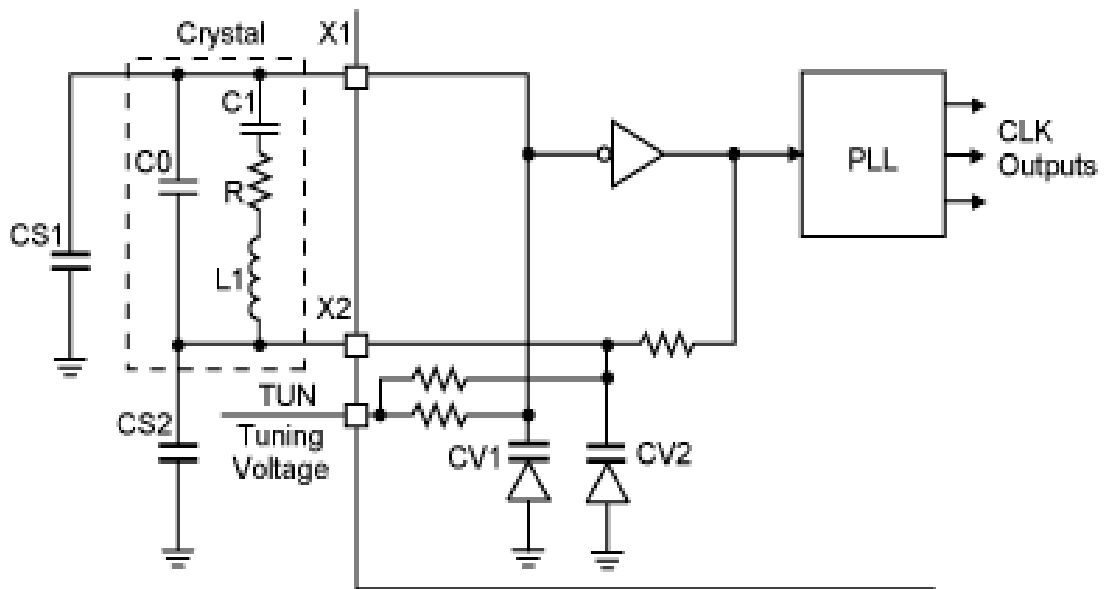
Figure 2.14: VCXO (Voltage Controlled Crystal Oscillator)

2.4.2   Non-linear Oscillators

a.   Ring Oscillators

The simplest and most popular type of VCO is ring oscillator. Ring oscillator is widely used due to low cost design and simplicity despite their poor phase noise characteristics. The arrangement of a typical 5-stage ring oscillator is shown below in the figure 2.15,
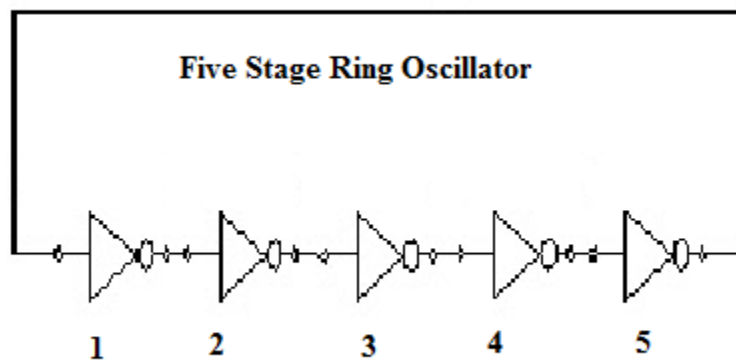
Figure 2.15: Typical 5-Stage Ring Oscillator

A ring oscillator is basically a cascade of 'n' inverters or NOT gates where 'n' should be an odd number. This odd chain will lead to the final output of ring oscillator to be inverted version of the first input. This final output has to be fed back to the first inverter input in order to produce oscillations.

b. Relaxation Oscillator

When a high center frequency and large linear tuning range at a low cost are the constraints relaxation oscillator is an excellent option. Relaxation oscillators do not use very less reactive elements or components thus could be easier for fabrication. Phase jitter and poor stability are the main shortcomings of these kinds of oscillators. The relaxation oscillators works on the principle of charging the capacitor gradually and discharging the capacitor rapidly.

2.5 LOOP FILTER

A loop filter is the most common and very vital block in the design of any PLL system. It is very important part of a PLL design since some of the key design factors such as Phase noise, phase jitter, spurious output, high side component, settling time and the stability of the loop depends on the loop filter design parameters. The type and the order of the loop filter depend on the specific PLL application. The loop filters are divided into two types depending on whether passive or active components are used in the design of a loop filter:

1. Passive Loop Filter
2. Active Loop Filter

2.5.1 Passive Loop Filter

A passive filter is a type of electronic filter that is built only from passive circuit components like resistors, capacitors, inductors, and transformers. The passive filter with respect to an active filter does not require an external power source and it has only the input signal that needs to be filtered, a ground to sink the unwanted signal and an output signal. An application that requires linear behavior from the loop filter will use mostly passive filters since they only consists of linear elements. The selection of the order of the passive filter depends on the requirements of the application it's in use.
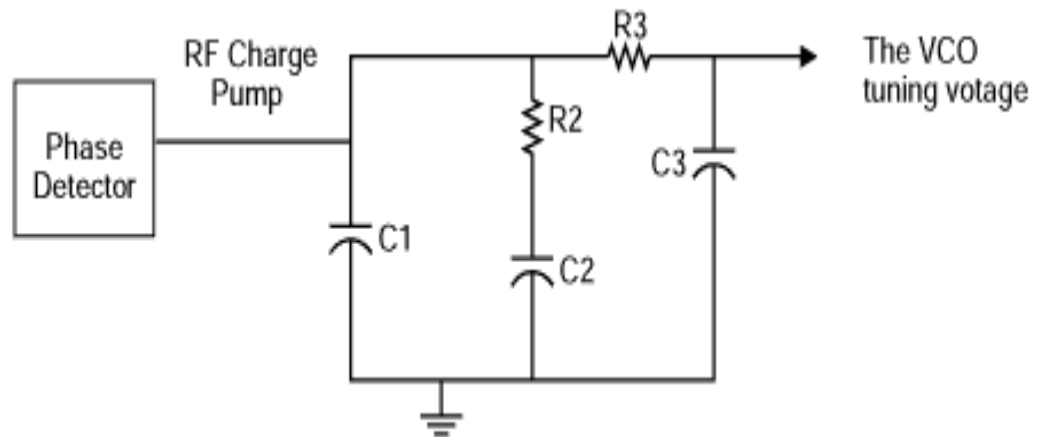
Figure 2.16: Passive Loop Filter

Passive filters are most commonly used in PLL's since they do not contribute for the system phase noise and are easier to design as they only consists of few passive elements depending on the order of the filter. For many applications second order loop would be sufficient but for some critical applications a higher order loop filters will be needed. The main design consideration for the passive loop filter would be $VCO_{cap,}$ which is the VCO input capacitance and thermal noise of the resistor. The design constraints get bigger for third order or higher since the VCO_{cap} acts in parallel to the loop filter capacitance. The thermal noise becomes a major concern when the loop filter resistance is in terms of several 10's of KΩ as it increases the thermal noise which in turn will increase the phase noise outside the loop bandwidth.

2.5.2 ACTIVE LOOP FILTER

An active filter is an electronic filter built using active circuit components like transistors, vacuum tubes and operational amplifiers. The active filters provide superior performance which would not be tradeoff for problems like thermal drift, noise and high cost. The active device of the loop filter would normally be an integrated circuit operational amplifier in the inverting mode. The transfer function of an active loop filter is given by,
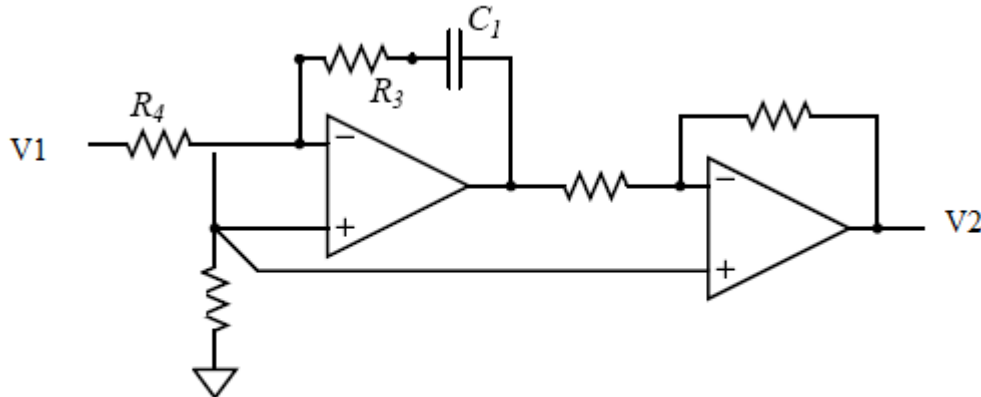
F(s) = - (R3/R4) [1 + 1/ (R3*C1)]

Figure 2.17: Active Loop Filter

DESIGN METHODOLOGY

3.1   Introduction

The Costas PLL Loop receiver for BPSK signal detection is designed at the transistor-level using Cadence Design System Tools. TSMC 0.18μm process was used along with TSMC RF libraries. All the simulations were performed in Analog Design Environment.   The BPSK signal is the input to the designed Costas PLL Loop BPSK demodulator or detector. Thus the BPSK signal was required to work on and perform its detection. The required BPSK signal was generated through BPSK modulator which is built using few transmission gate switches.

The Costas PLL Loop BPSK Detector consists of the following blocks:

- Single Ended I/P to Double Ended O/P Converter
- Phase/Frequency Detector (Gilbert Cell Mixer)
- Third Multiplier (Song and Kim Multiplier)
- Double Ended I/P to Single Ended O/P converter
- Current Starved Voltage Controlled Oscillator
- First-Order Loop Filter
- Attenuator

The Costas PLL Loop BPSK Detector is as shown in the figure 3.1. A sinusoidal carrier signal of 2GHz is modulated by a square wave data signal of 50MHz.

The Gilbert Cell mixer is used as a phase frequency detector which will multiply the incoming BPSK signal and VCO generated signal to recover the data (50MHz) that modulated the carrier at the transmitter.
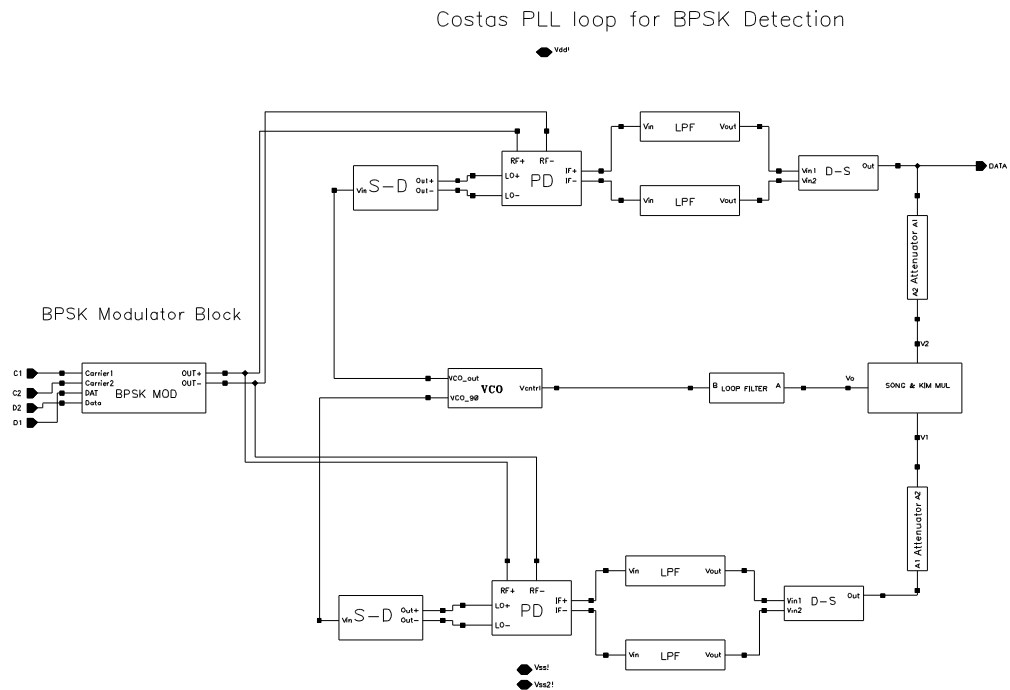

Figure 3.1: Costas PLL Loop BPSK Detector

3.2   BPSK Modulator

The BPSK signal is generated using a transmission gate switch technique as shown below in the figure 3.3. A transmission gate is nothing but a PMOS and NMOS transistor connected in parallel. It acts like an analog switch with complementary inputs. A transmission gate switch is as shown below in the figure 3.2,
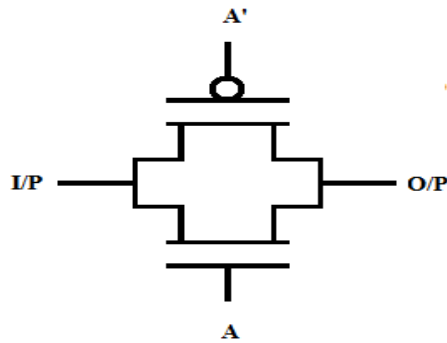
A	Gate
0	Open
1	Closed

Figure 3.2: Transmission Gate   **Table 3.1: Truth Table**

The logic used to generate a BPSK signal is very simple with the help of few transmission gates as shown. A high '1' on NMOS and a low '0' on PMOS would close the switch passing input to the output and a low '0' on NMOS and a high '1' on PMOS would open the switch. To generate a BPSK signal, two complementary data signal running at 50MHz are applied to the gates of the two transistors. The signal to be modulated, a high frequency sine wave signal running at 2GHz is applied as an input. Thus whenever the switch closes the respective carrier wave will be at the output.

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The sizing should be carefully done here since the output switching from one carrier wave to another carrier wave is instantaneous and also to avoid any kind of a delayed switching. In the detector design we have used a double balanced Gilbert cell mixer. The mixer has differential inputs and differential outputs. So in order drive the differential inputs of the Gilbert cell mixer the differential BPSK signal was needed to be generated. So with the use of two other transmission gates and by just switching their inputs it is possible to generate a differential BPSK signal. This is one of the two differential inputs to the mixer.
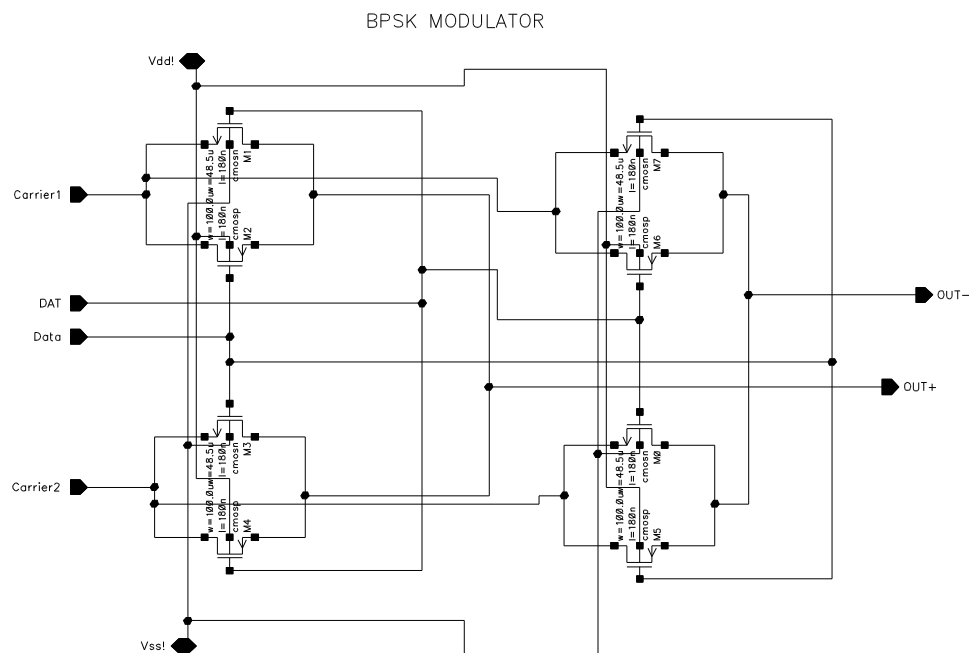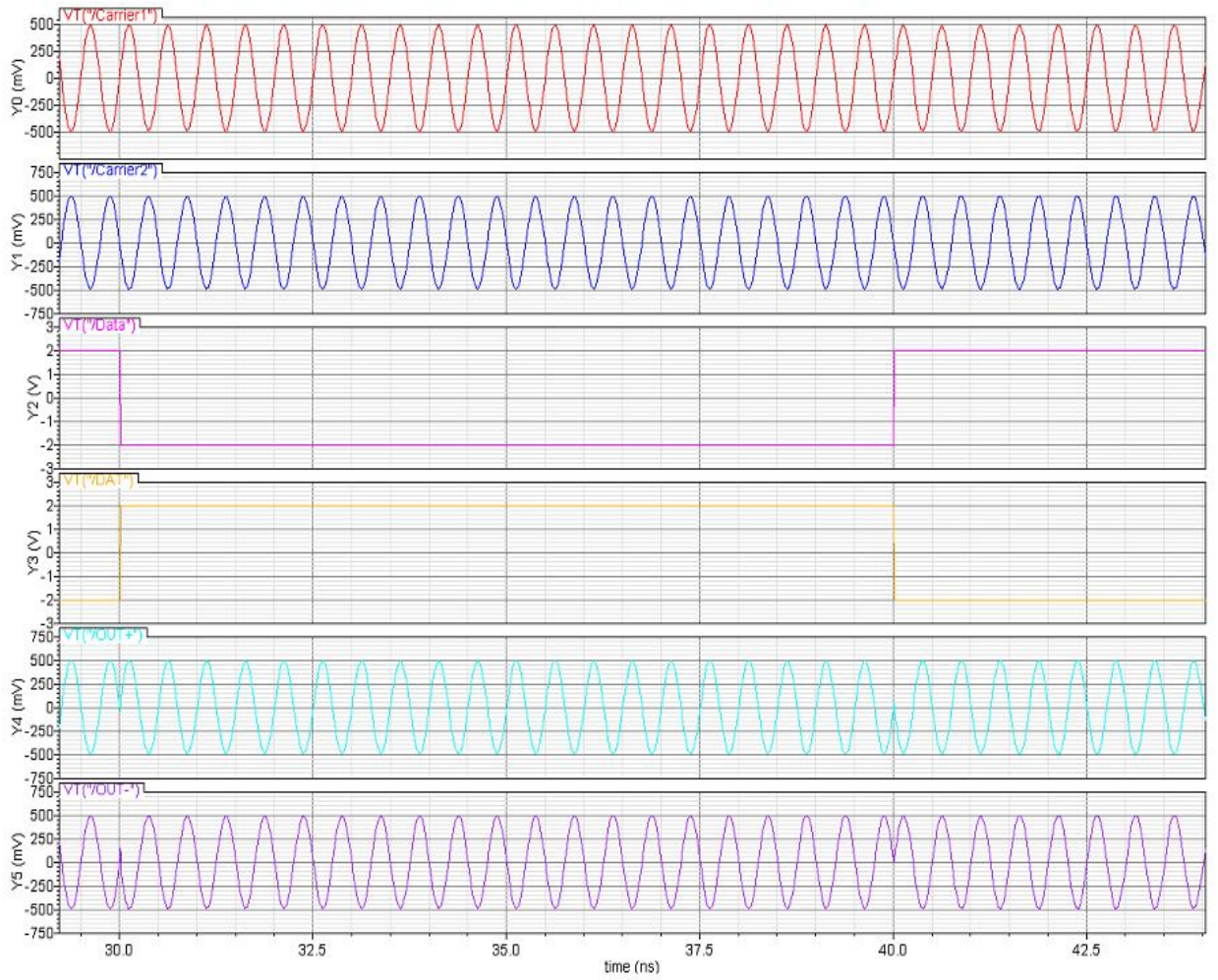

Figure 3.3:   Transmission Gate Based BPSK Modulator

Figure 3.4: BPSK Signal Generated using Transmission Gates

3.3 Gilbert Cell Mixers as a Phase Frequency Detector

The Phase detector is an analog device that would produce an output voltage that is proportional to the phase and frequency difference between its applied input signals. The phase/frequency detection in here is achieved with help of a four quadrant Gilbert cell mixer. The four quadrant multiplier is used here since both input and output signals have positive and a negative polarity. A Gilbert cell mixer is basically a frequency translation system that would allow frequency down-conversion. The purpose of the Gilbert cell mixer in here is to produce the output that is proportional to the phase/frequency difference between the two input signals. The Gilbert cell mixer is nothing but a multiplier circuit and the multiplication process is shown below,

$V1 = A1\sin(\omega_1 t + \theta_1)$...1

$V2 = A2\sin(\omega_2 t + \theta_2)$...2

The multiplied result will be:

$V1 * V2 = A1A2[\sin(\omega_1 t + \theta_1) * \sin(\omega_2 t + \theta_2)]$

Where $A = (\omega_1 t + \theta_1)$ and $B = (\omega_2 t + \theta_2)$

Multiplying 1 and 2 using Trig Identity will give:

$$= -\frac{A1A2}{2}[\cos((\omega 1t + \theta 1) + (\omega 2t + \theta 2)) - \cos((\omega 1t + \theta 1) - (\omega 2t + \theta 2))]$$

$$= -\frac{A1A2}{2}[\cos((\omega 1 + \omega 2)t + (\theta 1 + \theta 2)) - \cos((\omega 1 - \omega 2)t - (\theta 1 - \theta 2))]$$
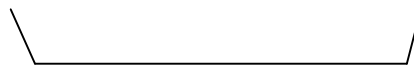
Frequency of Interest: Difference Frequency

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The schematic of Gilbert cell mixer is as shown in the figure 3.5 below. The transistors M0 and M5 are the RF transistors to which the RF inputs are applied. These two transistors perform voltage to current conversion and again these differential RF inputs get multiplied from M2 through M6 multiplying RF current from M0 and M5 with local oscillator signal applied across M2 and M6 transistors. The load resistors will cause current to voltage conversion producing differential output IF signals IF+ and IF- shown in the waveform.
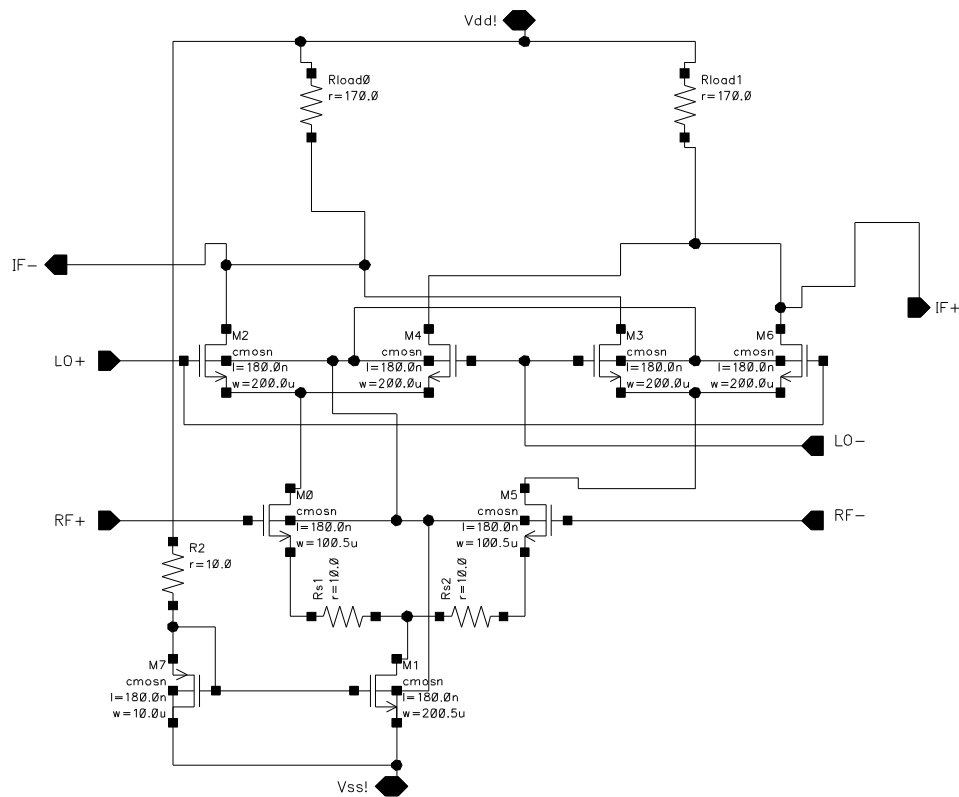

Figure 3.5: Gilbert cell mixer as a Phase Frequency Detector

The designed Gilbert cell mixer in this research will multiply the incoming BPSK signal running at 2GHz±50MHz with the coherent carrier running at 2GHz generated at the receiver. Thus incoming BPSK signal is varying between the ranges of 1.95GHz to 2.05 GHz gets multiplied with a 2GHz carrier at the receiver producing an output signal component that has sum and difference frequency components. The Loop filter designed for the incoming data rate will let only the data signal to pass through and all the high side components will be grounded. The differential IF outputs of a mixer running at a difference of 2.05GHz and 2.0GHz signal is shown in the figure 3.6 below,
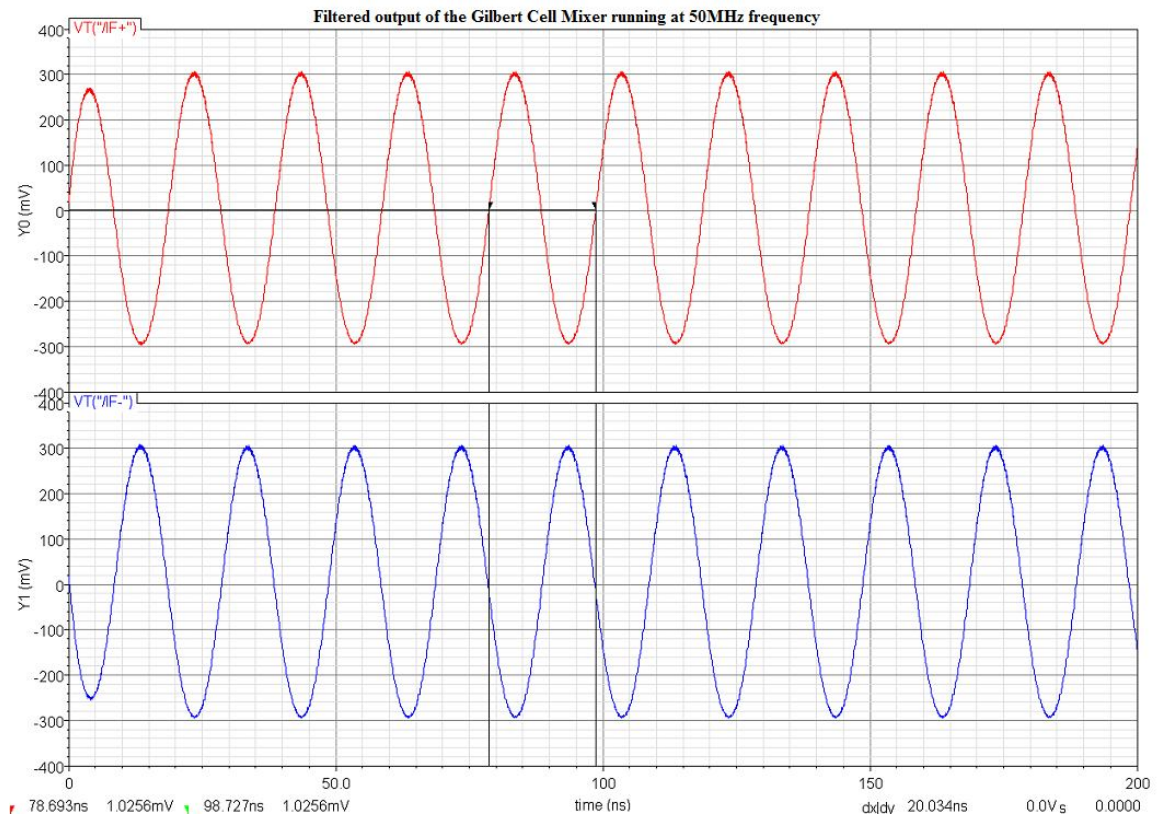

Figure 3.6: Filtered IF output of a Gilbert Cell Mixer

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3.4   Song and Kim Multiplier

A four quadrant Song and Kim multiplier is used as a third multiplier in the Costas loop design. The function of the third multiplier is to produce a signal that is proportional to the phase difference between 'I' and 'Q' branch signal. This signal is passed through an integrator type filter which will produce a DC voltage proportional to variations in the signal applied to its input.

This four quadrant analog multiplier is based on the square-law dependence of the transistor drain current on the gate-to-source voltage Vgs in the saturation region [8]. In the circuit configuration one input is directly applied to the gate while the other one is applied through the source follower stage. This multiplier in the Costas loop design uses the square-law of the MOS transistor in saturation region which requires four source followers, four squaring transistor and four main current sources. The multiplier action can be written as

$$V_0 = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2$$

Usually the summing, subtracting and squaring circuits are implemented. This would normally lead to poor performance for high frequency applications due to the effects of parasitic capacitances of the MOS transistor. The inherent square law of the MOS transistor drain current in saturation region with two input signals applied to the gate and the source will achieve the sum and difference squared components without the need for a separate summing, subtracting and a squaring circuit.

The drain current of a MOS transistor in saturation region is

$$Ids = \frac{1}{2} Kn \left(\frac{w}{l}\right) (Vgs - Vt)^2$$

If two inputs V_1 and V_2 are applied to the gate and source of the transistor, the drain current is proportional to the square of the difference of the two inputs [8]. Since the gate-to source voltage would give us directly either sum or difference of the two inputs no additional circuitry is required. Normally we get a difference voltage of V_1 and V_2 applied to gate and source, respectively, and they get squared in saturation region meaning we obtain $(V_1 - V_2)^2$. In order to get the sum squared term one of inputs has to be inverted. In this design the Voltage V_2 is inverted. Thus when two inputs V_1 and $-V_2$ applied we obtain drain current that is proportional to $(V_1 + V_2)^2$. To achieve negative V_2 an inverting amplifier with unity gain is designed. The Schematic of the inverting amplifier is shown below,
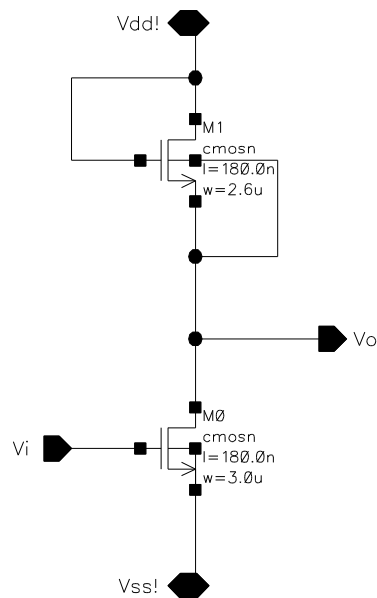

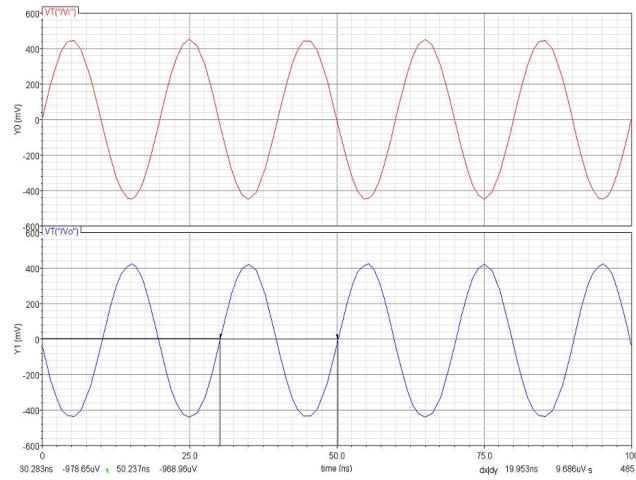**Figure 3.7: Inverting Amplifier with a unity Gain**

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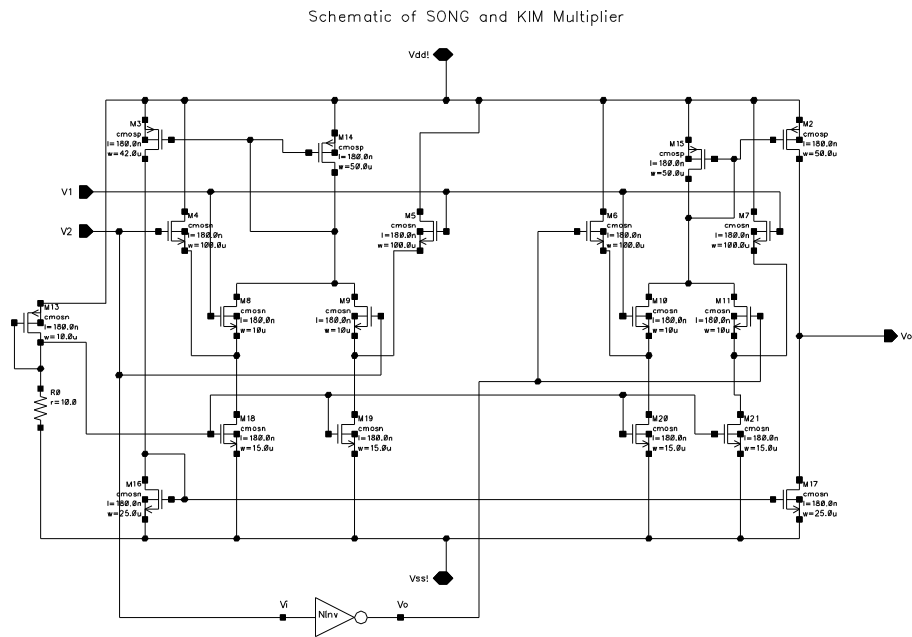**Figure 3.8: Transient Response of an Inverting Amplifier**

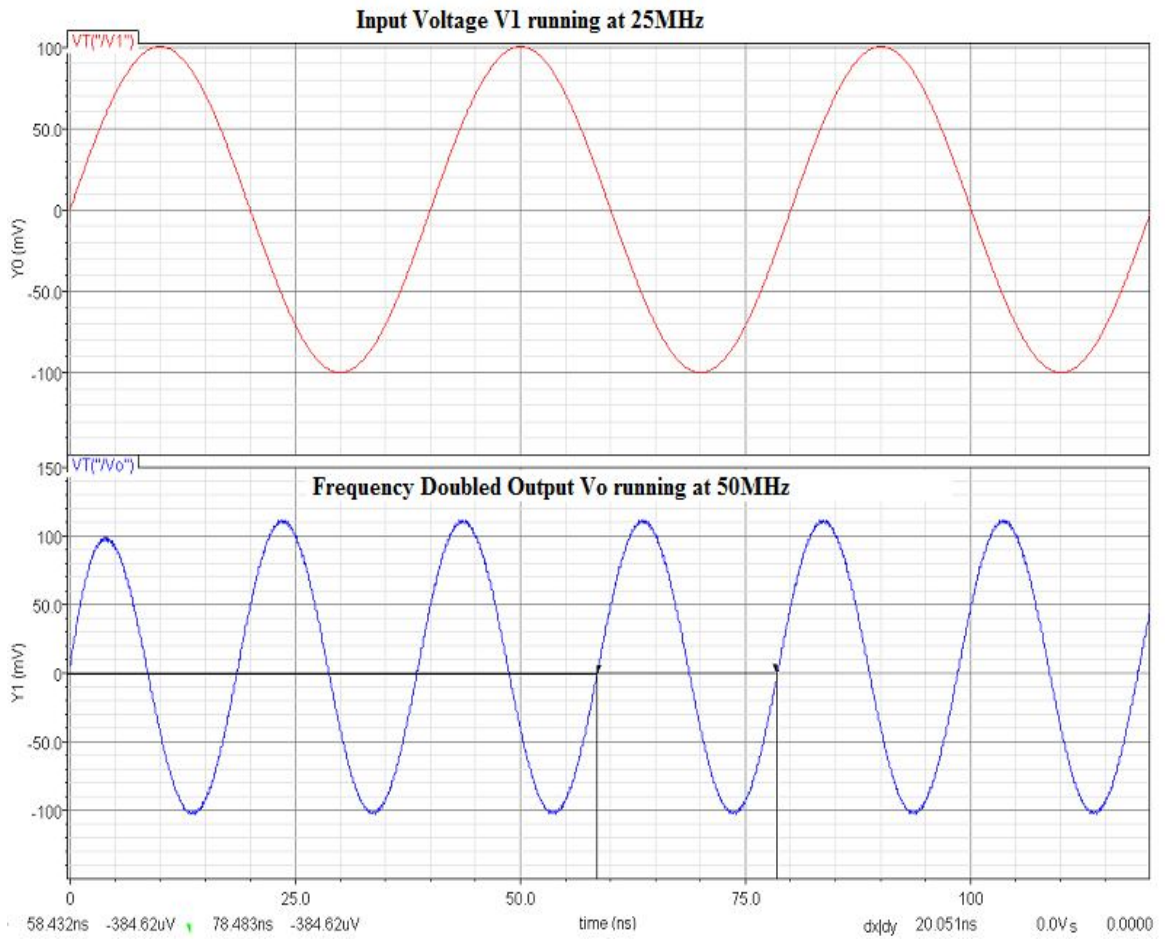**Figure 3.9: Song and Kim Multiplier**

Figure 3.10: Transient Response of a Song and Kim Multiplier

3.5 Single Ended Input to double Ended Output Conversion

The circuit diagram of a Single ended input to double ended output is as shown in the figure 3.11. This circuit will drive the second differential input of the phase/frequency detector. The '0˚ phase shift signal generated by a VCO is a single ended output. This output of the VCO is one of the differential inputs to the phase detector. Thus a single ended I/P to Double ended O/P circuit is used between VCO and a Phase detector to convert the single ended VCO output to double ended phase detector input. To generate a differential output means to produce signals which are out of phase by 180˚.

Schematic of Single ended I/P to Double ended O/P
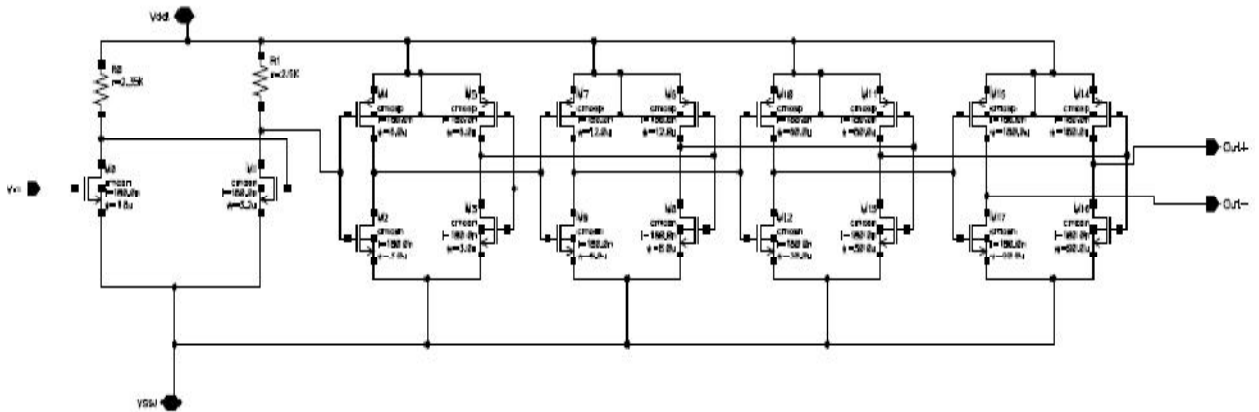
Figure 3.11: Single Ended Input to Double Ended Output Circuit with 4 stage Buffer

Since it is the square wave to be converted from single ended to double ended, the sizing of the transistors chosen are very small compare to the output load to be driven. The output of this circuit will be driving the phase detector. The phase detector transistor width is too large compared to that of the conversion circuit. Thus a four stage buffer is used to drive the phase frequency detector.
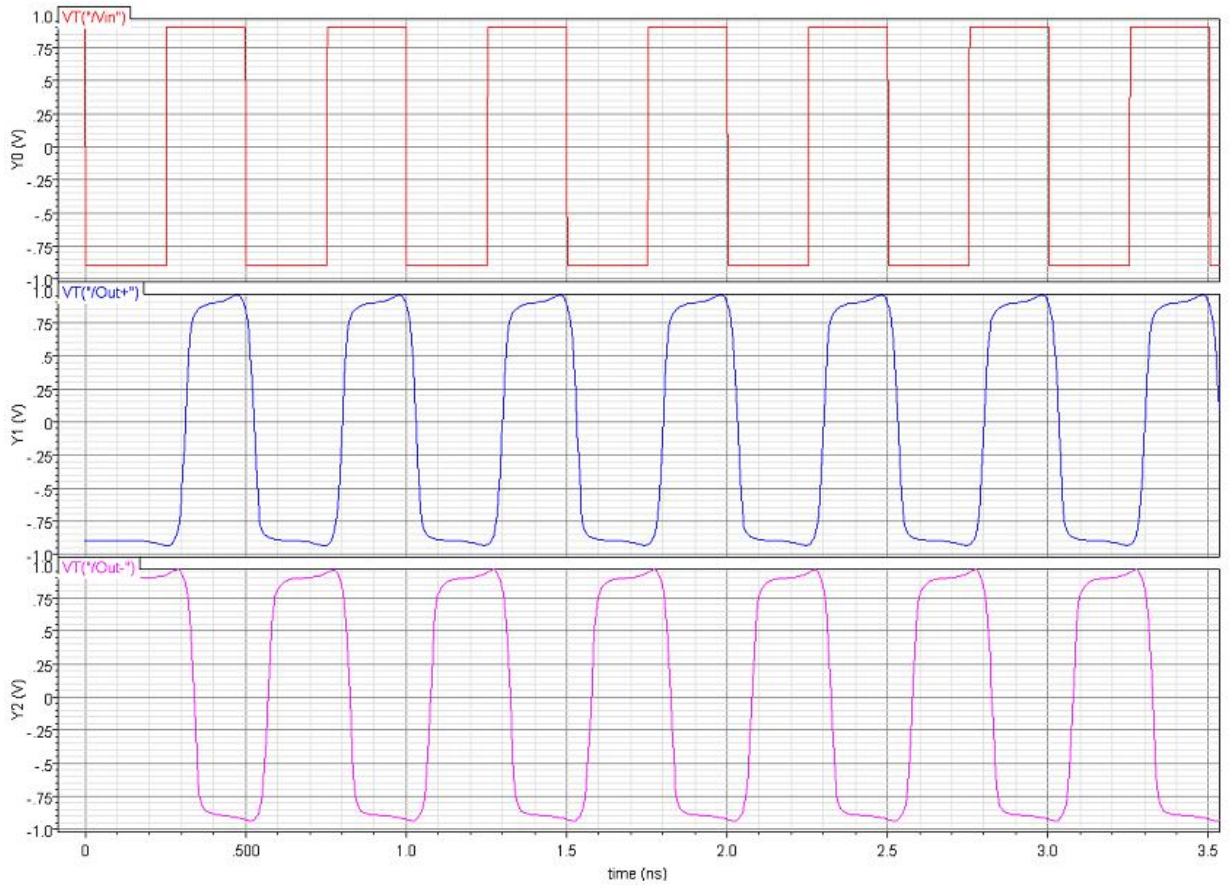
Figure 3.12: Single Ended Input to Double Ended Output Waveform

3.6 Double Ended Input to Single Ended Output Conversion

The Double Ended Input to Single Ended Output or a differential circuit is as shown in the figure 3.13. The differential output of the phase frequency detector is to be converted in to single ended output. This conversion takes differential output from the mixer instead of a single output which is necessary to reject the local oscillator feedthrough. The transistor width is chosen in such a way to handle the drain current of the biasing transistor and to provide sufficient voltage gain.
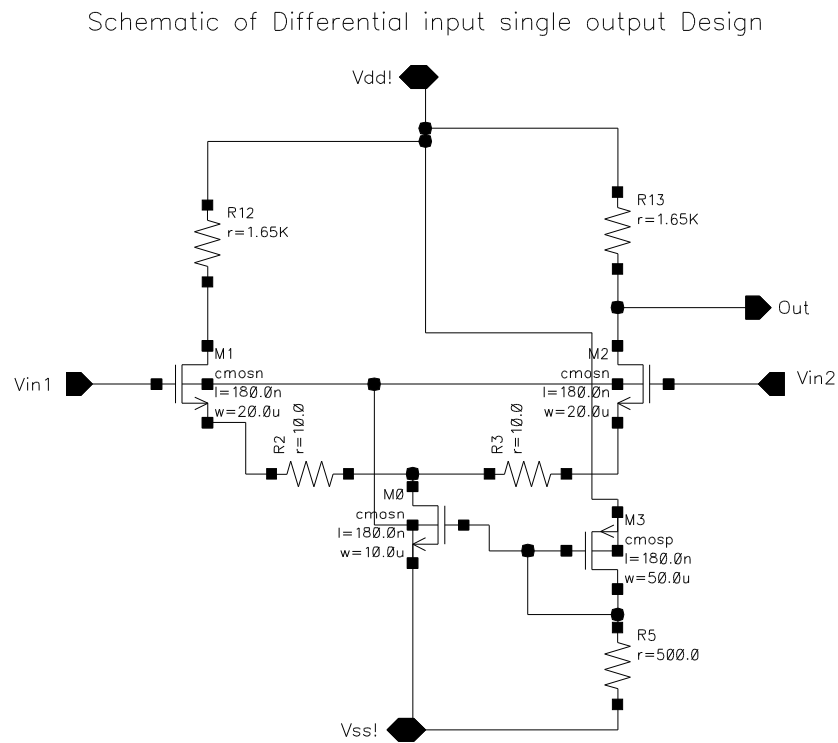
Figure 3.13: Differential to single conversion stage

The differential to single stage conversion circuit is designed for a differential square waves since the differential output of the mixer is square wave in nature. In the figure 3.14, either Vin1 or Vin2 could be selected or taken as the output depending on the required polarity of the output signal meaning Vout could be either Vin1 or Vin2.
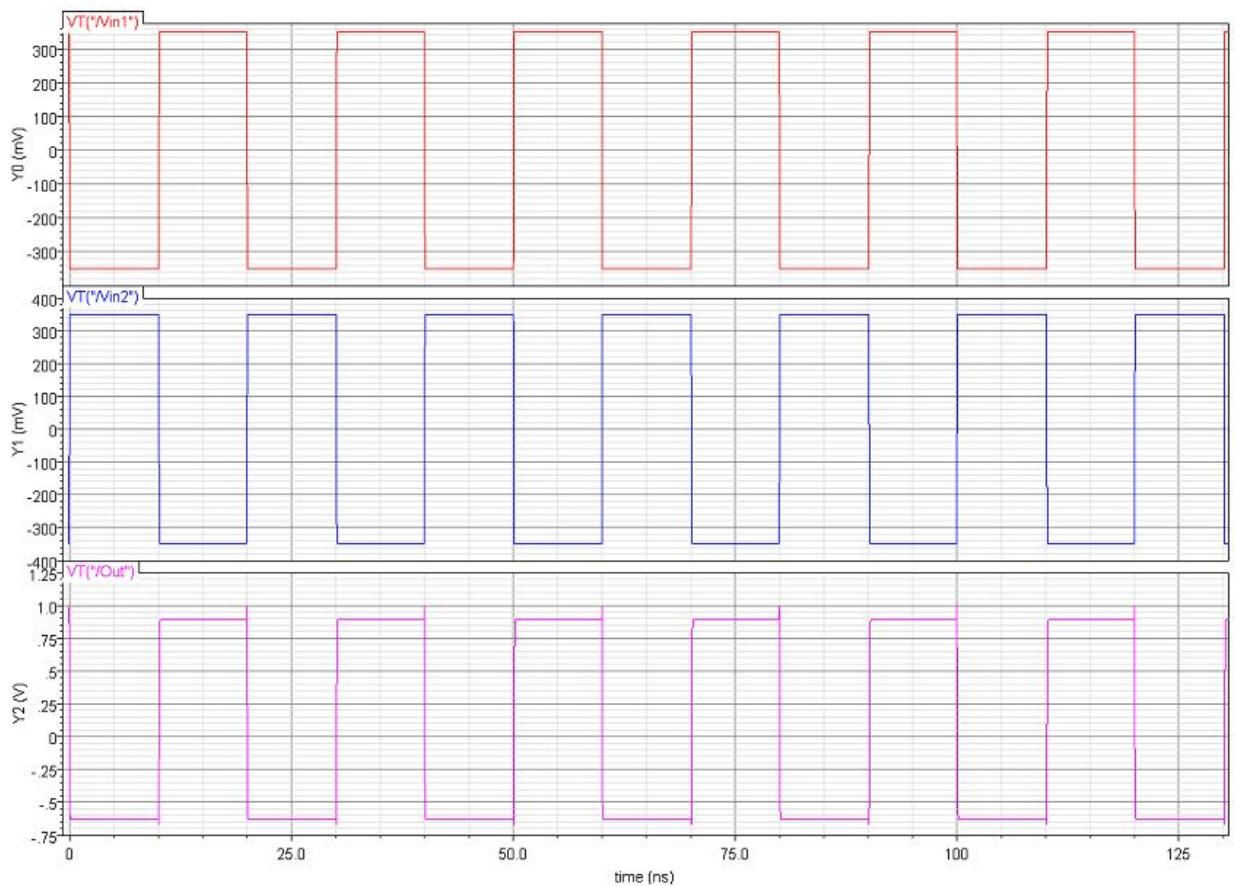

Figure 3.14: Differential Input to single Output waveform

3.7   Current Starved VCO

The current starved VCO designed here has 3 stages of inverters as shown in the figure 3.15. The PMOS and NMOS transistors at the top and the bottom of the inverters act as a current source. The current that is delivered to these inverters depends on the control voltage being applied to the leftmost current source. The drain currents of the first stage current source will be approximately the same which is again controlled by the control voltage applied to its control input shown in the figure 3.15. It is called current starved VCO since the current supplied to the inverters is limited by the respective current source. Achieving required frequency is quiet easier since there is a direct relationship between the current supplied to the inverters and its propagation delay. The progressive sizing is done to obtain the required frequency for the applied control voltage. The output of the third stage is fed back to the first stage and this mechanism would cause oscillations to build. The current starved VCO or a ring oscillator designed here has three stages; each stage provides a phase shift of 45˚. Thus there is a phase shift of 90˚ from the first stage inverter to the third stage inverter. The VCO for the Costas loop requires generating signals with 0˚ and 90˚ phase shift. The output of the first stage is buffered to generate a signal with 0˚ phase shift and output of the third stage is buffered to obtain a signal with 90˚ phase shift. The 0˚ phase shift signal is going to the in phase 'I' branch and 90˚ is connected to the orthogonal branch. The frequency range of the ring oscillator is larger than the tuned LC oscillator.

Design procedure for a current starved VCO

For a NMOS transistor in saturation region, the equation for Drain Current is given by

$$Ids = \frac{Kn}{2}\frac{W}{L}\ (Vgs - Vtn)^2\ (1 + \lambda Vds)$$

where W = effective channel width ,

L = Effective channel length

V_{GS} = Gate to Source Voltage

V_{tn} = Threshold Voltage

λ = Channel length modulation parameter per volt

V_{DS} = Drain to Source Voltage

The total capacitance on the drains of NM12 and PM13 is given by

$$Ctotal = \frac{5}{2}\ Cox\ [Wp.Lp + Wn.Ln]$$

The oscillation frequency of the Current starved VCO for N (an odd number ≥ 3) of Stages is,

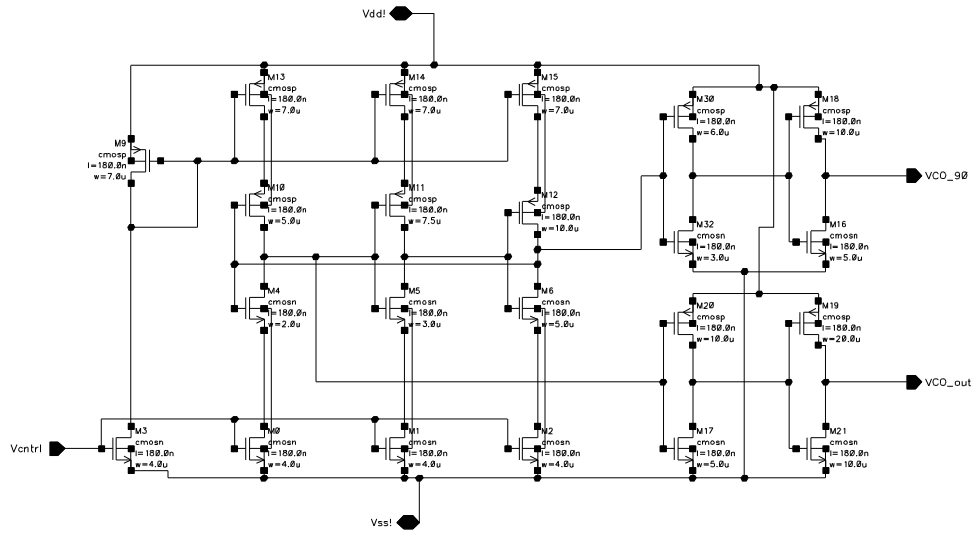$$Fosc = \frac{ID}{N} * \frac{1}{Ctotal} * \frac{1}{VDD}$$

Figure 3.15: 3-Stage Voltage Controlled Oscillator

V_{cntrl} in volts	T_{ON} in ps	T_{period} in ps	Frequency in GHz	Duty cycle (%)	Avg. Power Dissipation in mw
-0.35	6200	12033	0.0831	51.52	0.5256
-0.30	2928.6	5658.1	0.1767	51.75	0.7252
-0.25	1586.8	3070.6	0.3256	51.67	1.0279
-0.20	1001.1	1937.6	0.5161	51.66	1.3897
-0.15	712.79	1384.5	0.7222	51.50	1.7635
-0.10	553.028	1091.8	0.9159	50.65	2.1288
-0.05	456.057	909.03	1.100	50.16	2.4812
0.00	393.362	789.264	1.2670	49.83	2.8161
0.05	352.242	706.581	1.4152	49.85	3.3141
0.10	325.30	647.50	1.5444	50.23	3.4336
0.15	303.596	607.709	1.6455	49.95	3.7105
0.20	288.602	575.831	1.7366	50.11	3.9637
0.25	276.244	550.113	1.8178	50.21	4.1921
0.30	268.360	531.231	1.8824	50.51	4.3953
0.35	261.110	518.057	1.9302	50.40	4.5689
0.40	255.380	507.578	1.9701	50.31	4.7112
0.45	251.349	499.532	2.0018	50.31	4.8256
0.50	246.779	491.625	2.0340	50.19	4.9217
0.55	246.316	487.362	2.0518	50.54	5.0002
0.60	241.661	482.720	2.0715	50.06	5.0677
0.65	239.644	478.215	2.0911	50.11	5.1263
0.70	238.918	473.367	2.1125	50.47	5.1751
0.75	238.325	470.795	2.1240	50.62	5.2178
0.80	235.218	469.719	2.1289	50.07	5.2558
0.85	230.550	466.184	2.1450	49.45	5.2879
0.90	232.392	466.042	2.1457	49.86	5.3171

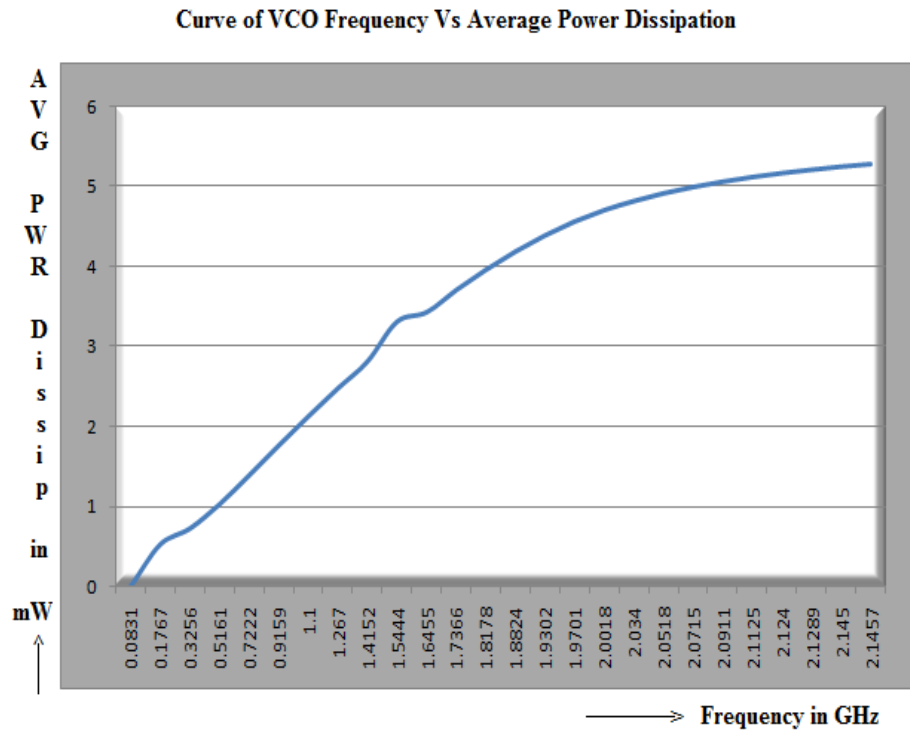**Table 3.2: Simulation Results of Voltage Controlled Ring Oscillator**

Curve of VCO Frequency Vs Average Power Dissipation

Figure 3.16: Plot of VCO Frequency Vs Avg Power Dissipation

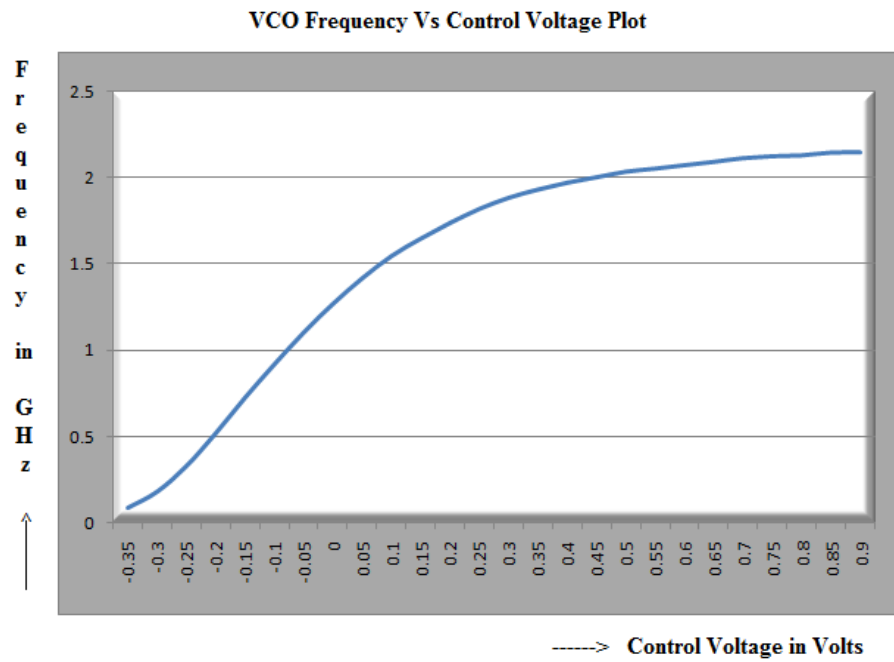**VCO Frequency Vs Control Voltage Plot**

Figure 3.17: Plot of VCO Frequency Vs Control Voltage
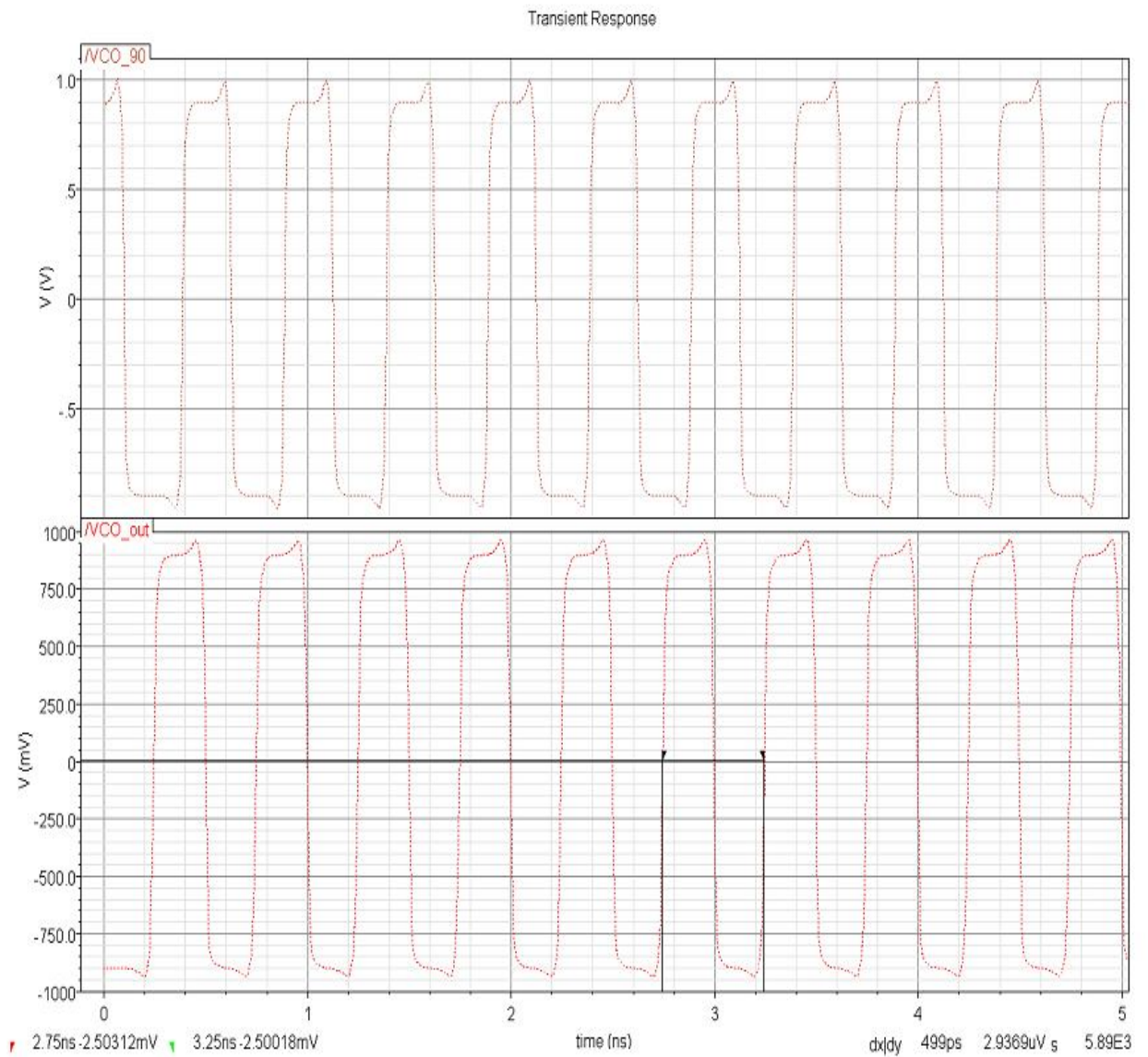
Figure 3.18: Ring Oscillator square wave Output of 2.0GHz @ 0.45v

3.8 Loop Filter

Schematic of a loop filter

R1
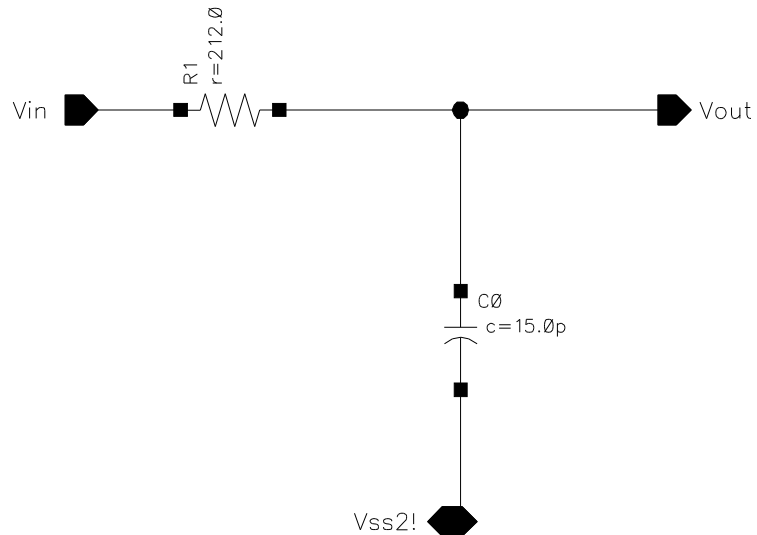r=212.0

Vin

Vout

CØ
c=15.0p

Vss2!

Figure 3.19: First Order Passive Loop Filter

The first order passive Loop filter has chosen to be twice to that of the received data rate in the Costas loop design. The first order filter was selected since it is very simple to design with few passive components and has low phase noise. This filter has one pole in the denominator and one zero in the numerator. The filter is designed to scale a data rate of 50Mbps. The two arms of the Costas loop, in-phase branch and quadrature branch has one RC filter.

The data signal is a 50MHz square wave. The transfer function of a single pole RC filter is given by,

$$Vo = \frac{\frac{1}{j\omega c}}{R + \frac{1}{j\omega c}} \ Vi$$

$$H(s) = \frac{1}{1 + j\omega Rc}$$

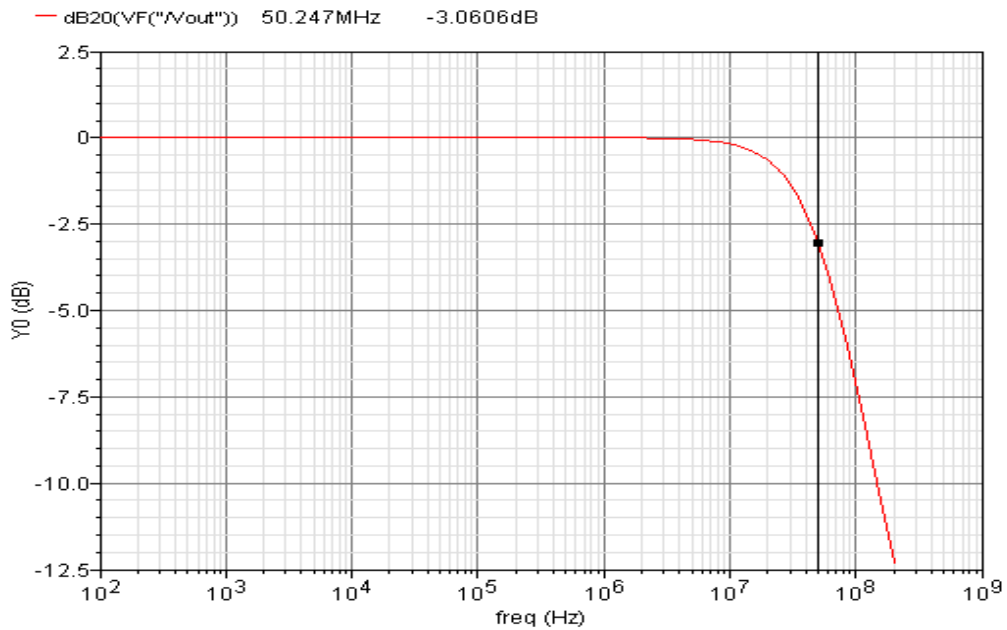The frequency response of the single pole RC filter is shown below,

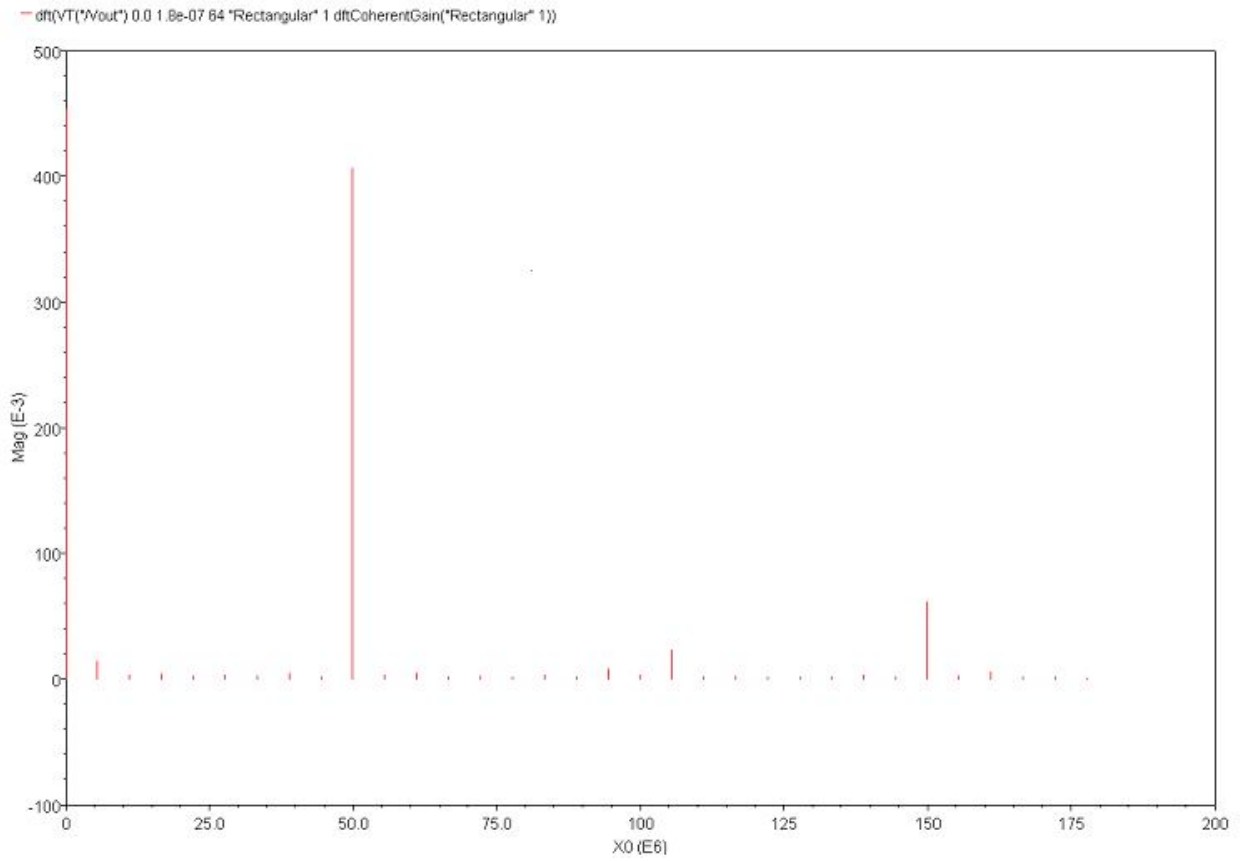**Figure 3.20: Frequency response of Single pole RC filter**

Figure 3.21: DFT of a 1st Order Loop Filter

3.9   Attenuator

Attenuators are devices used to adjust signal levels, to control impedance mismatch and to isolate circuit stages [19]. Attenuators as the name suggest will attenuate the input signal amplitude level to the required output db level depending on the attenuation factor for different applications. Attenuation is normally done without or with little signal distortion. They are nothing but a voltage divider network designed for a specific attenuation factor or desired loss in db. Attenuators are again divided into passive attenuators and active attenuators. The passive attenuator is divided into 'Tee' type attenuator and 'pi' type attenuator. The attenuator output is driving the third multiplier which is Song and Kim multiplier. The Song and Kim multiplier inputs should be within certain range for its proper operation. Thus here The Attenuator has been used in to provide Song and Kim multiplier with the required input voltage range. The attenuator model is shown below,
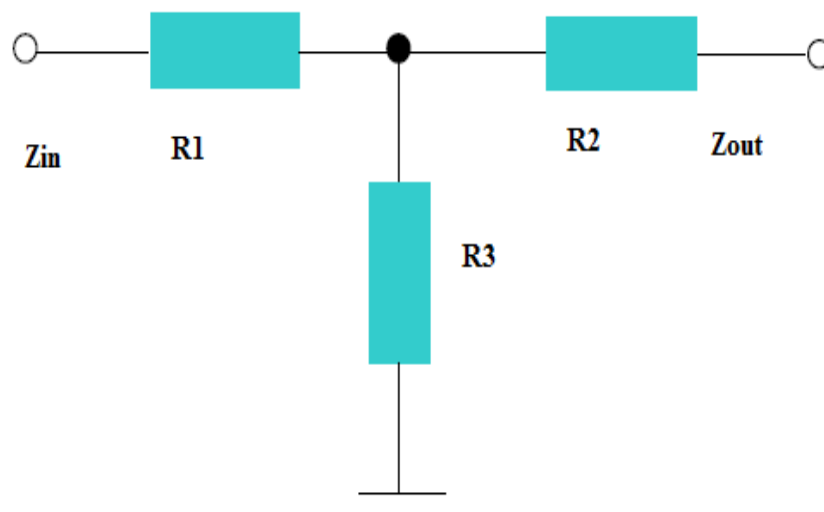
Figure 3.22: 'Tee' Type Model

To drive the Song and Kim multiplier an attenuation of -5.46 db was required. The voltage divider network was designed randomly to get the required amount of attenuation. The attenuation loss of -5.46db to the input of Song and Kim multiplier was required for its proper operation. The Schematic and attenuation waveform of 'Tee' type attenuator is shown below,

Figure 3.23: Tee-type Attenuator Schematic
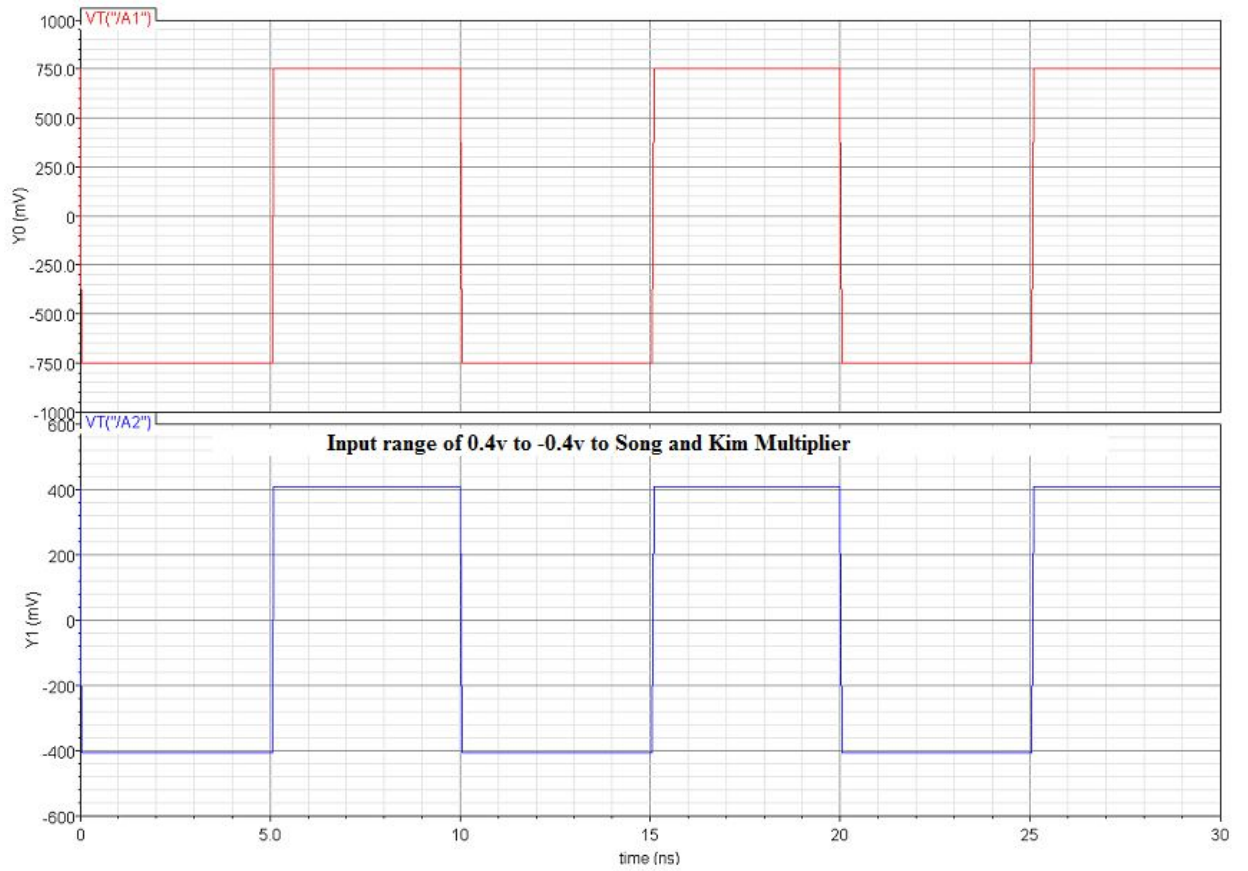
Figure 3.24: Attenuation waveform showing attenuation loss of -5.46db

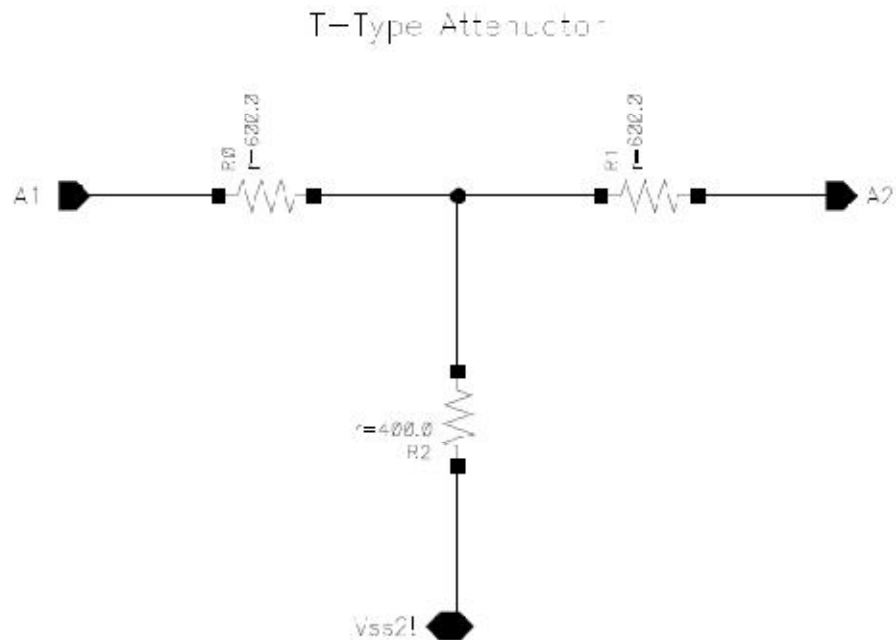# SIMULATIONS & RESULTS

4.1 RESULTS

Figure 4.1 shows the simulation results of the designed Costas Loop BPSK Detector.
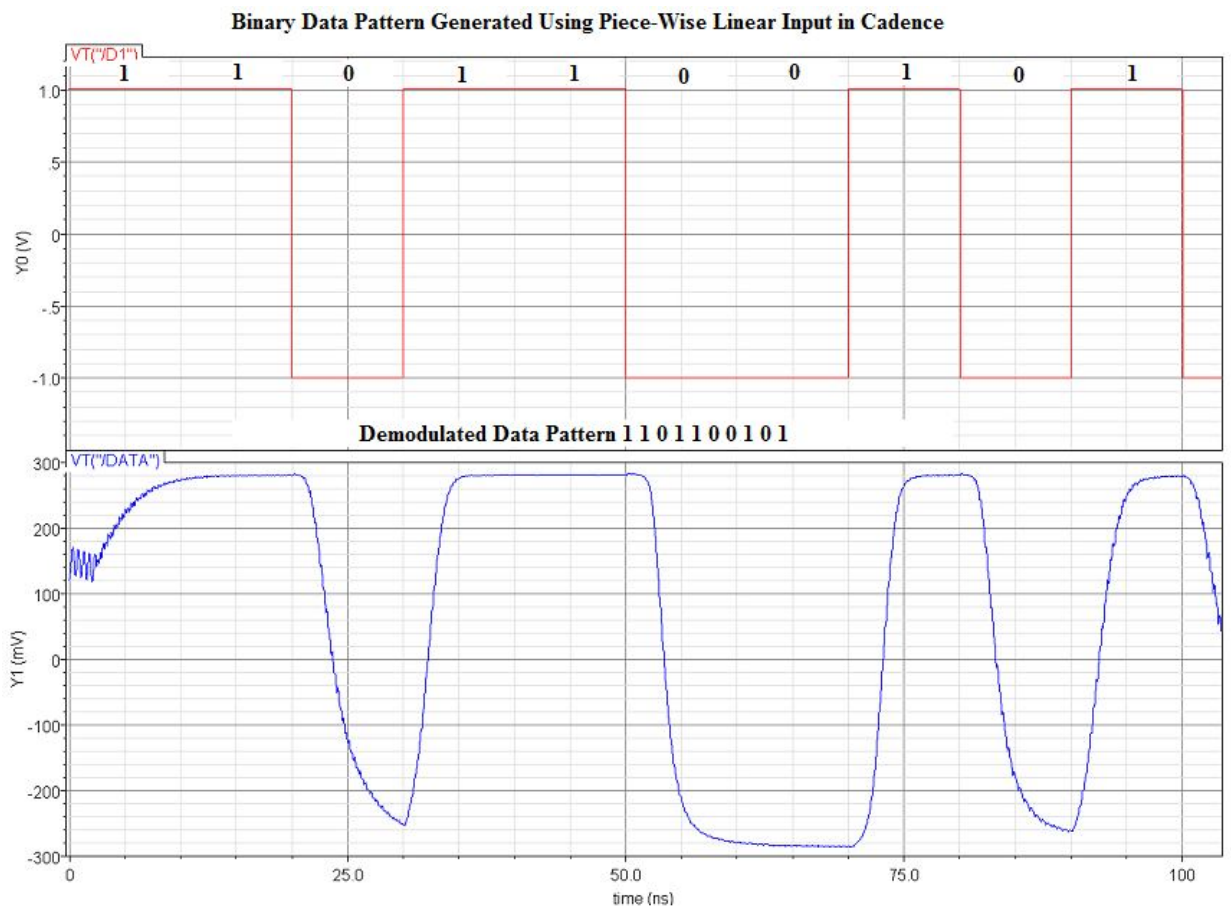
Figure 4.1: Simulation results of Costas PLL BPSK Detector detecting the pattern

1101100101

The binary sequence 1101100101 was generated using the piece-wise linear function available in cadence. This data pattern is the input to the BPSK modulator. This low frequency data signal running at 50MHz will modulate the other high frequency carrier signal at 2GHz input to the modulator. The generated BPSK signal is then given as an input the demodulator.

Figure 4.2 shows the demodulated binary data stream 00100110101

Binary Data Pattern Generated Using Piece-Wise Linear Input in Cadence

Demodulated Data Pattern 0 0 1 0 0 1 1 0 1 0 1
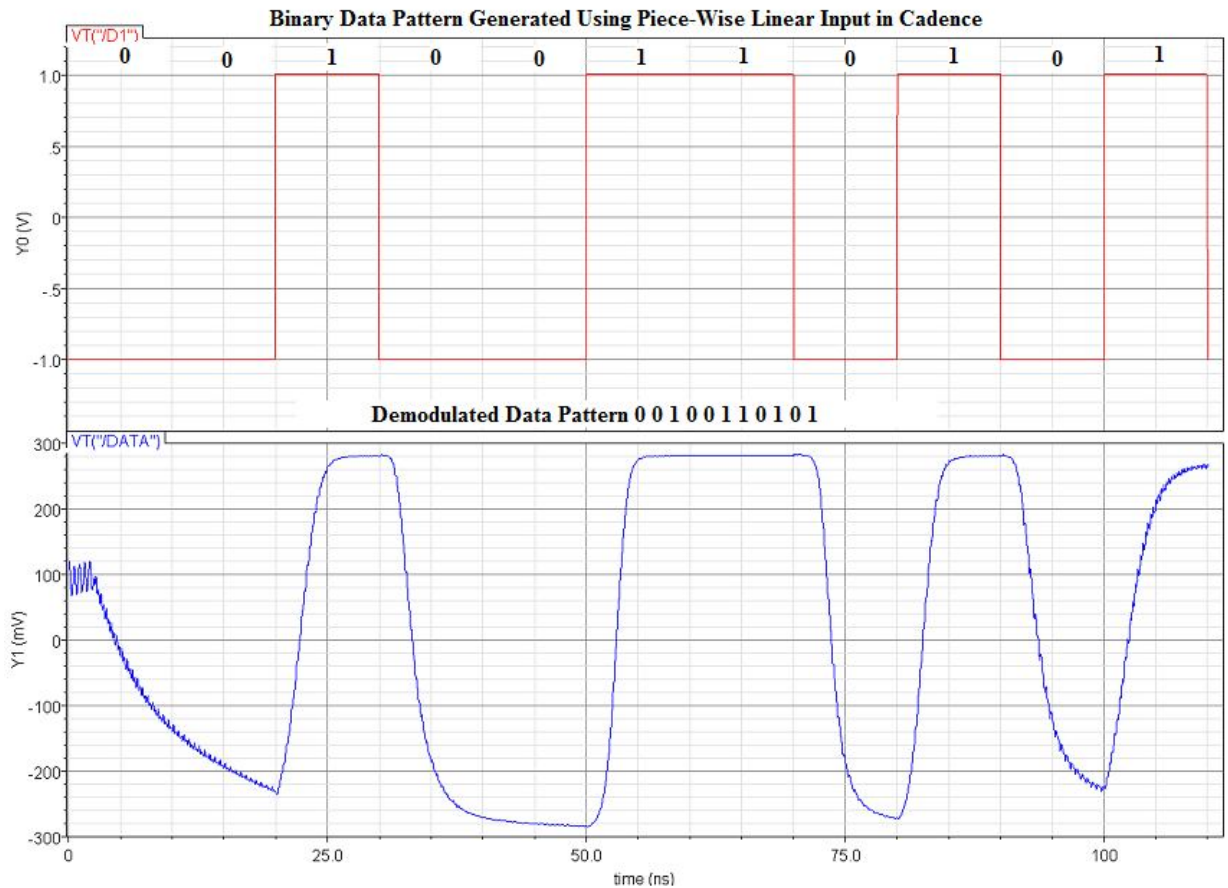
Figure 4.2: Simulation results of Costas PLL BPSK Detector detecting the pattern 00100110101

Thus the binary data 00100110101 is successfully detected and demodulated. This entire pattern can be made repetitious by just repeating the same sequence meaning by just making it periodic in the piece-wise linear input function. The designed Costas Loop BPSK detector can detect and demodulate any binary data stream at the data rate up to 50Mbps.

4.2   Summary

Table 4.1 summarizes the measured specifications of the Costas PLL BPSK detector.

Lock Range   : 1.99- 2.01GHz

Power Dissipation of BPSK Modulator   : 37.092μw

Power Dissipation of PLL   : 144.926mw

Power Dissipation of PFD   : 12.093mw

Power Dissipation of VCO @ 2GHz   :   4.8256mw

 Supply Voltage VDD!   : +/-0.9v

CONCLUSION & FUTURE WORK

A Costas PLL Loop for BPSK detection was successfully implemented using 0.18µm technology in cadence. The first and foremost requirement of this design was to generate or recover a carrier frequency at 2GHz at the receiver and then matching that with the phase/frequency of the incoming BPSK signal. This was achieved with the help of a ring oscillator which is a current starved VCO in configuration for this demodulator design. In this design a first order loop filter was scaled to an incoming data rate. Here first order was chosen considering the effects of VCO input gate capacitance. Filters need to be optimized such that its bandwidth is wide enough to minimize ISI and narrow enough to minimize noise. This Costas loop can see incoming signal phases of $0°$ and $180°$ and demodulate the data stream up to 50Mbps. The Costas PLL BPSK Detector consumes 144mw of power.

The design can be implemented with higher order loop filter for better response with the trade-off on chip area and cost. A coherent BPSK demodulator using anti-parallel synchronization loop could be implemented which uses differential VCO instead of a quadrature VCO. This will considerably reduce the chip area and improve the performance.

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