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Design of a Low Power and Area Efficient Digital Down Converter and SINC Filter in CMOS 90-nm Technology

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Design of a Low Power and Area Efficient Digital Down
Converter and SINC Filter in CMOS 90-nm Technology

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Engineering

By

Steven John Billman
B.S., Cedarville University, 2009

2011
Wright State University

WRIGHT STATE UNIVERSITY
SCHOOL OF GRADUATE STUDIES

Jun 10, 2011

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Steven Billman ENTITLED Design of a Low Power and Area Efficient Digital Down Converter and SINC Filter In CMOS 90nm Technology BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering

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2011

ABSTRACT

Billman, Steven John. M.S.Egr. , Department of Electrical Engineering, Wright State University, 2011. Design of a Low Power and Area Efficient Digital Down Converter and SINC Filter in CMOS 90-nm Technology.

A digital down converter (DDC) typically receives a digital input that has been generated by an analog to digital converter (ADC) operating at intermediate frequency (IF) in an RF receiver chain. The function of the DDC is to down convert the IF signal to baseband in phase (I) and quadrature (Q) signals and is a very important component in wireless receivers. A Digital Down Converter (DDC) is developed based on square wave local oscillators facilitating a multiplier-less implementation with no constraints on the sampling frequency. The DDC includes a pseudo multi-rate SINC low pass filter which exhibits better performance compared to the standard multi-stage SINC filter. The pseudo multi-rate SINC filter can be implemented with a unique cascaded integrator comb (CIC) filter to obtain the same improved performance. A 90nm CMOS design takes 8 bit inputs centered at 25 MHz with a bandwidth of 30 MHz and is clocked at 400MHz. The design demonstrates a flexible, very low power/size DDC architecture for single chip digital receiver applications. The layout area is 333.485um x 617.6um and the power consumption is 12.54mW when clocked at 400MHz.

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1 Introduction

An RF receiver chain is comprised of many subcomponents. The standard chain starts with the antenna and then is connected to a band pass filter (BPF) to filter out the noise not located within the bandwidth of the signal. The signal is then passed through a low noise amplifier (LNA) in order to boost the signal while limiting the noise output. Next the RF signal is multiplied by a local oscillator (LO) to down convert the signal to an intermediate frequency (IF). The signal is then sent through another band pass filter which filters out the higher frequency caused by the multiplication of the RF frequency. Once the frequency has been reduced to this lower IF frequency, an analog to digital converter (ADC) can accurately convert the IF analog signal into a digital signal. This IF signal is passed through a digital down converter (DDC) which converts the IF signal to baseband. The complex output which contains the in phase (I) and quadrature (Q) signals is then passed through a digital low pass filter which will filter out the high frequency caused by the DDC and leave only the baseband signal. The block diagram of this design can be seen in Figure 1.1 [12].

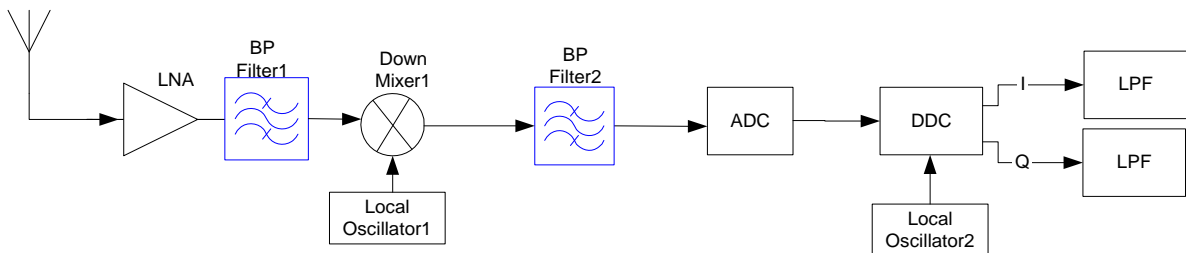


Figure 1.1 RF Receiver Chain

Technology has advanced enough to have the f_{IF} signal converted to a digital signal using an ADC. Using a DDC to take the f_{IF} digital signal and convert it to

baseband allows for low powered and highly accurate designs to be implemented. Eventually the goal is to take the analog f_{RF} coming in from the antenna and convert it directly to a digital signal using software in order to save space and power. In this case, the entire transceiver would be digital. However, current speeds restrict us to using analog designs to bring f_{RF} down to f_{IF} and then converting the signal to digital [7].

A DDC typically receives a digital input that has been generated by an ADC operating at an IF in an RF receiver chain. The function of the DDC is to down convert the IF signal to baseband in phase (I) and quadrature (Q) signals as shown in the block diagram in Figure 1.2 [1,2,3,4,5]. This is accomplished by multiplying the incoming IF signal centered at f_{IF} by in phase and quadrature sinusoid oscillator signals with frequency equal to f_{IF} . The outputs of the complex multiplier are I and Q signals centered at DC and at $2f_{IF}$. The DDC includes low pass filters in the I and Q output paths to reject the signal centered at $2f_{IF}$ and pass the signal centered at DC with the desired bandwidth.

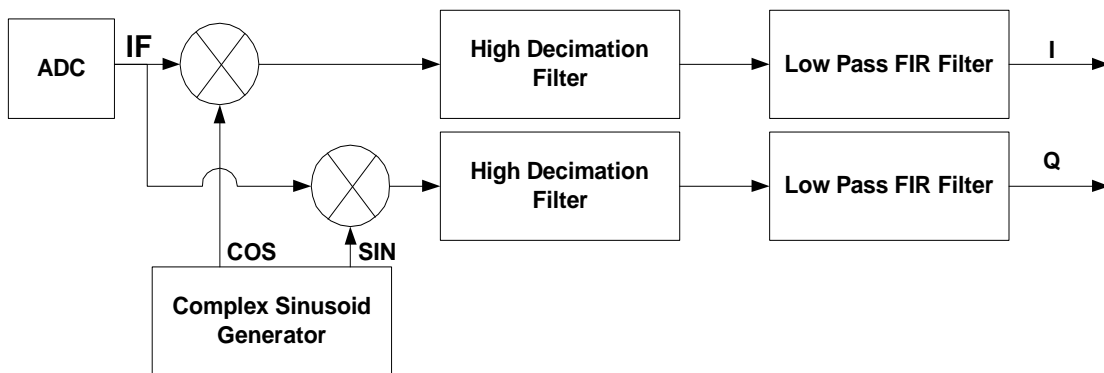


Figure 1.2 A DDC showing the IF signal coming out of the ADC being multiplied by the Complex Sinusoid Generator and passed through the High Decimation Filters and the Low Pass FIR Filters resulting in the I and Q output.

There are numerous applications for DDCs including software radios, smart antennas, cellular base stations, channelized receivers, and spectrum analysis [1,2,3,4].

Sophisticated single chip DDC implementations are available which include complex signal synthesizers to generate the I and Q local oscillator (LO) signals in continuous wave (CW), frequency hopped, and chirped formats [3,4]. These commercially available chips provide the flexibility and processing power to meet a variety of applications; however, they are not suited for embedding in single chip solutions such as single chip software receiver or in an integrated single chip multichannel smart antenna receiver.

FPGA designs of DDCs have the advantage of being reprogrammable and have the ease of designs being relatively uncomplicated to implement. However, FPGAs require a large amount of power and space for their designs. Some designs operate around 400mW [8]. This is not ideal for a very low powered chip design. So for small designs that require a very low power, the FPGA approach for the DDC is not recommended.

A common approach for filter design is to design the filter in Matlab and multiply the signal by coefficients given. However, multiplication is a very expensive resource when it comes to power and area in a digital design. Because of this, there has been a lot of research done on how to make the multipliers smaller or how to approach the multiplication differently. Below in Figure 1.3, is the design of a DDC that uses coefficients as a filter. The design requires n multipliers for n coefficients.

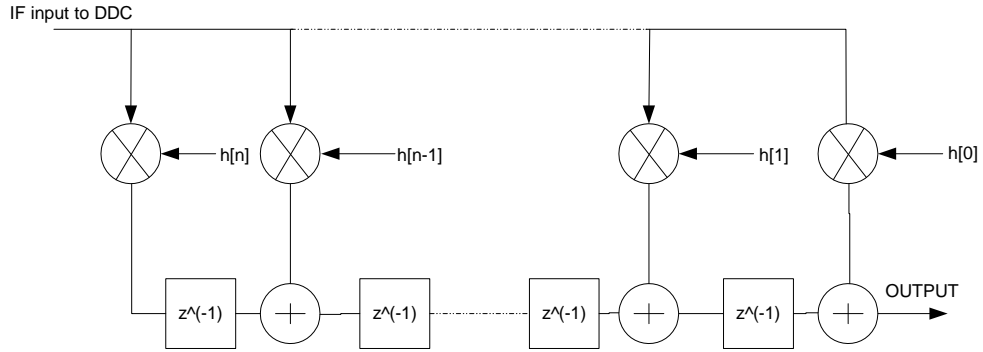


Figure 1.3 Low pass FIR Filter using coefficients

Much discussion has been made on how to optimize the design of multiplier blocks for the coefficients of FIR filters. This has really advanced the size and speed of designing FIR filters using coefficients. [9]

One approach to using coefficients for a FIR filter is to take the multiplication blocks and create one block and optimize it using graph representation. Graph representation starts with a one on the left hand side and uses vectors with associated positive or negative powers of two to calculate the desired integer. There can be multiple integers between the one located on the left hand side and the final value on the right hand side. The number associated with each vector is multiplied by the integer the vector is coming from. The integers throughout the graph, including the final value are the sum of the product of the end points of the vectors. Figure 1.4 shows an example of calculating 35 using graph representation. [10] This paper introduces the Bull-Horrocks algorithm which is used to reduce the complexity of the multiplier block. Another common type of algorithm used to simplify the multiplexer block is the n-dimensional reduced adder graph (RAGn) [9].

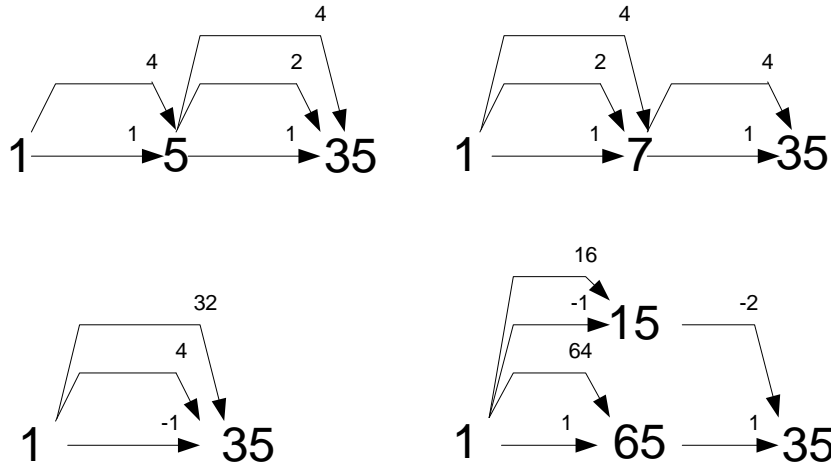


Figure 1.4 Graph Representation example for calculating 35

Another way to optimize coefficients is to represent them using canonical signed digits (CSD). This representation uses 33% more zeros than two's complement or binary and therefore requires much less addition than the standard two's complement or binary representation of numbers. CSD uses a ternary system. The three values a digit can have are 1, 0, or -1. Also, a zero has to follow any non-zero number. This results in many more zeros representing the values. This brings obvious advantages when multiplying since a multiplication by zero doesn't have to be done. One of the disadvantages to CSD is that one more bit is required to represent a number than standard binary. For example, if 7 were to be represented in binary, only three bits would be needed (111). However, if 7 were to be represented in CSD, four bits would be required since consecutive 1s are not allowed. So using CSD seven would be 100-1 ($2^3 + 0 + 0 - 2^0$) which only has two nonzero values associated with it, compared to the three nonzero values used in binary,

but requires four bits to represent the number instead of three. Below in Table 1 is the comparison between binary and CSD values with their corresponding decimal values

Table 1 Table showing binary and CSD values

Dec and Bin		CSD and Dec	
7	111	100-1	7
6	110	10-10	6
5	101	0101	5
4	100	0100	4
3	011	010-1	3
2	010	0010	2
1	001	0001	1
0	000	0000	0

Using Canonic signed Digit representation, an N-tap filter can be designed by using powers of two for the taps of the filter. This requires no multiplication and only requires additions, subtractions, and bit shifts. In this paper [11] 36 adders and 24 delay blocks were required for the 25-tap filter. 116 adders and 59 delay blocks were required for the 60 tap filter. The design discussed in this thesis uses 28 adders and 30 delay blocks for the equivalent of a 25 tap filter. The paper discusses how to faster search for optimal CSD values and compares them to the ideal values. The CSD values that the algorithm finds has minimal losses in performance for fewer adders required in the design. One of the problems with using CSD for filters is that due to the amount of shifting required, the bit size of the signals has to drastically increase in order to fully support the design. This is easily implemented when using an FPGA or a software based design, however implementing this in schematic or on an ASIC is difficult. An increase in bits by a factor of three for a signal can cause a significant increase in size and can increase the complexity of routing.

Cascaded integrator comb (CIC) filters use delays and multi-rate processing to create a low pass filter. The CIC filter does not require any multipliers which is very beneficial in keeping the design low powered and small. The design of a CIC filter has two sections, comb stages and integrator stages. The order of the two stages does not matter. Each comb stage takes a previously delayed signal and subtracts it from the current signal. There are N stages in the comb section. The N comb stages have a sample frequency of $\frac{f_s}{R}$. For each integrator stage, the signal is summed by the delay of the previous sum. As with the comb section, there are N stages of the integrator section. The sample rate of the integrator stages is f_s . The design of the CIC filter can be seen in Figure 1.5 where the integrator section comes before the comb section and it is a 4 stage filter. A CIC filter design has a frequency response that resembles a sinc function as seen in Figure 1.6. CIC filters have specific roll off responses for the pass band. This can be a disadvantage compared to other filters, since other FIR filters can be designed to have any roll off that is necessary. Also, CIC filters have high peaks after the initial drop off in the frequency response which causes the higher frequencies to not be filtered out as well as seen in Figure 1.6. Cascading this design makes the stop band lower since the high frequency peaks are lowered, but it decreases the pass band since the roll off is steeper. A SINC filter has the same frequency response as a CIC filter but a SINC filter averages inputs instead of decimating the sample rate. Since it can be difficult to decimate sampling frequency to certain values, a SINC filter can be valuable. By cascading SINC filters each with different design values, a more ideal filter with less peaks at high frequencies and a better roll off can be designed and is discussed and implemented in this thesis.

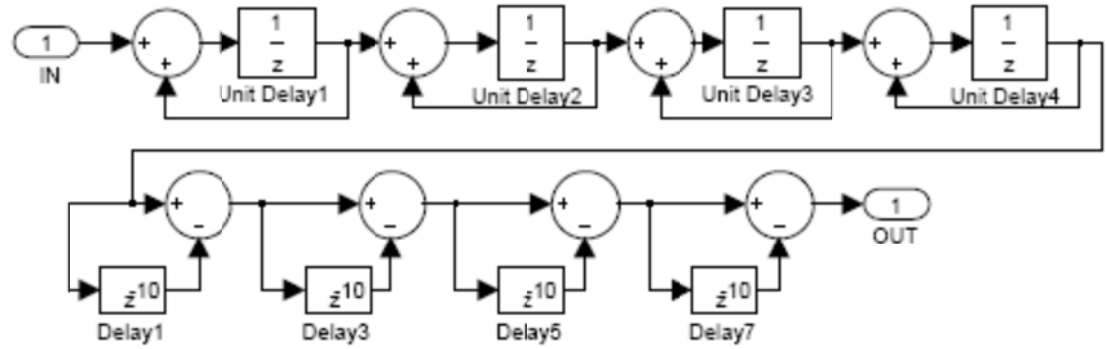


Figure 1.5 CIC filter design.

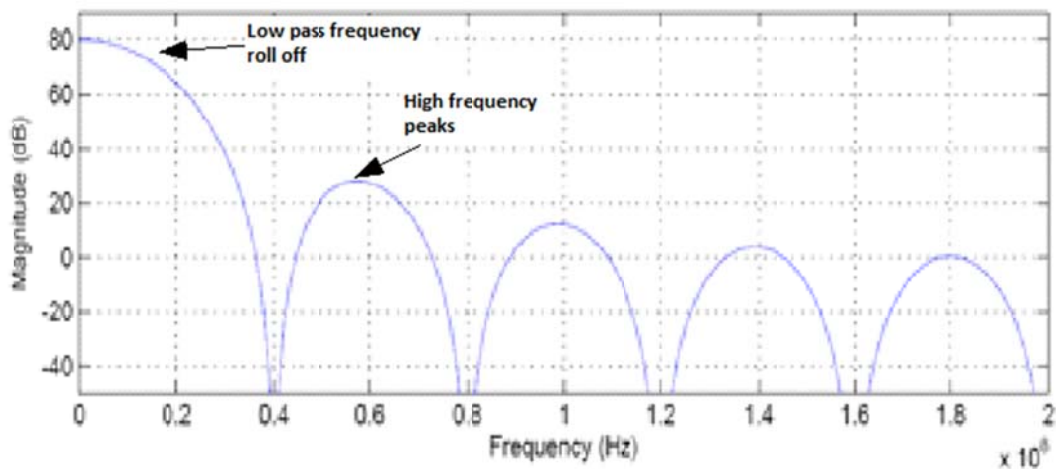


Figure 1.6 Frequency response of a CIC filter

1.1 Motivation

This Thesis presents a very low power area efficient CMOS DDC that is intended for applications where the ADC and the DDC are integrated with receiver chain digital processing hardware on a single chip. This Thesis details the design of a multiplier-less DDC with no constraints on the sampling frequency f_s . Previous implementations of multiplier-less DDCs require the DDC sampling frequency to be set at $4f_{IF}$ so the LO sinusoidal inputs have values of 1,0,-1,0 for each cycle [2]. The sampling frequency for this implementation can be set to any value up to the maximum sampling frequency of

the ADC which provides flexibility for meeting bandwidth and filtering requirements for various embedded applications.

The design in this thesis also includes a unique pseudo multi-rate SINC filter that has better performance than the standard cascaded multi-stage SINC filter [5]. Other filter designs that use coefficients are not optimal for a low power and space ASIC design. These filters rely on large bit shifts not being costly in order to work well in design which is not necessarily the case on an ASIC. The unique pseudo multi-rate SINC filter in this thesis builds upon the design of the cascaded SINC filter and optimizes it using very low power and low area. It is designed and implemented in CMOS 90-nm technology.

2 Digital Frequency Down Converter

2.1 Architecture

The block diagram of the multiplier-less DDC architecture is shown in Figure 2.1. As can be seen, the LO sinusoidal generator is replaced by a square wave LO. If the LO is a sine wave, then restricting the sampling frequency to be $4f_{IF}$ results in a cycle of the I and Q LO signals being represented by 1,0,-1,0 and 0,1,0,-1 respectively. This design is shown in Figure 2.2. If higher sampling frequencies are desired, the values of the I and Q LO signals must be generated with a sinusoidal synthesizer to produce the required values at the sample times and the DDC must execute complex multiplies. For this implementation, the LO signals are square waves, so if the sampling frequency is $4f_{IF}$, then one cycle of the I and Q LO signals are represented by 1,1,0,0 and 1,0,0,1 respectively. If it is desired to have a sampling frequency equal to $16f_{IF}$, then one cycle of the I and Q LO signals are represented by 1,1,1,1,1,1,1,0,0,0,0,0,0, 0 and 1,1,1,1,0,0,0,0,0,0,0,0,0,1,1,1,1. Thus, the sampling frequency of the DDC can be increased relative to the IF frequency while performing the DDC operation with only inverters and multiplexers.

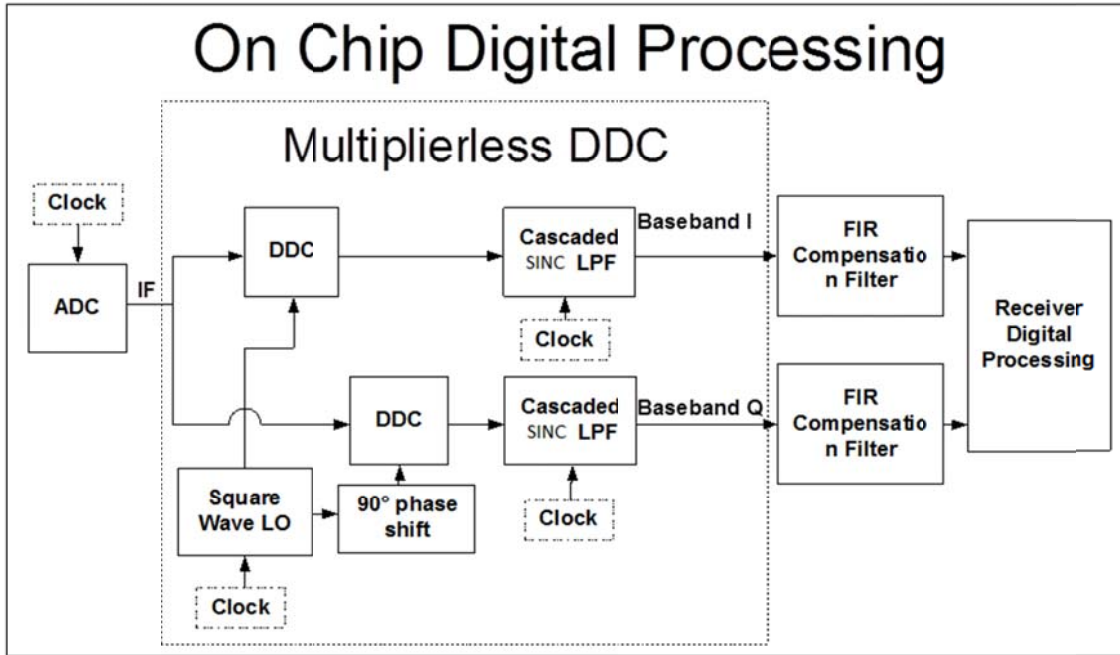


Figure 2.1 A block diagram showing a multiplier-less DDC.

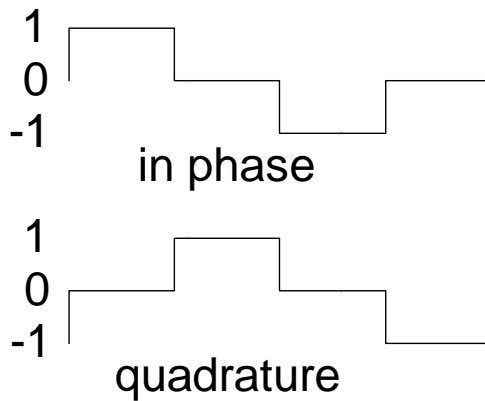


Figure 2.2 Design of an in phase and quadrature $4f_{IF}$ signal

For the square wave LO, the DDC multiplication is performed by inverters and multiplexers even for the higher sampling rates. The pure sine wave LO results in the DDC outputs having only the sum and difference frequency components centered at $f_{IF}-f_{LO}$ and $f_{IF}+f_{LO}$, with an information bandwidth equal to the f_{bw} . This can be seen in the following equation.

$$\sin((\omega_{IF})t) * \sin((\omega_{LO})t) = \sin((\omega_{IF} + \omega_{LO})t) + \sin((\omega_{IF} - \omega_{LO})t) \quad (1)$$

A square wave of frequency F has frequency components located at F, 3F, 5F, 7F, ... with magnitudes of B, B/3, B/5, B/7,... .For the square wave LO, the output of the digital mixer will have frequency components centered at $f_{LO}-f_{IF}$, $f_{LO}+f_{IF}$, $3f_{LO}-f_{IF}$, $3f_{LO}+f_{IF}$, $5f_{LO}-f_{IF}$, $5f_{LO}+f_{IF}$, ..., due to the harmonics of the square wave at $3f_{LO}$, $5f_{LO}$, ... So if $f_{IF} = f_{LO}$, then for the sine wave LO, the DDC output is the desired baseband signal centered at DC and the sum component centered at $2f_{IF}$. However, for the square wave LO, the DDC output signals are centered at baseband DC, $2f_{IF}$, $4f_{IF}$, $6f_{IF}$, ..., with the baseband signal bandwidth of f_{bw} .

2.2 Testing

2.2.1 Matlab

Figure 2.3 shows the DDC designed by having the f_{IF} signal multiplied by the LO. The figure has been designed in Matlab and is used to simulate the DDC. Since f_{IF} is located at 25MHz with a bandwidth of +/- 15MHz, the lowest possible input frequency to the DDC is 10 MHz and it is the first frequency simulated. The time domain results can be seen in Figure 2.4 and the frequency domain results can be seen in Figure 2.5. From the time domain, it is difficult to tell what has happened to the signal. However, looking at the frequency domain it is clear that there is a strong signal at 15MHz, which is the difference between the 25MHz local oscillator and 10MHz input frequency, and at 35MHz, which is the sum of the 25MHz oscillator and the 10MHz input frequency. This is the worst case scenario for the DDC and filter due to the fact that it has useful information located at 15MHz and has to get rid of the signal only 20MHz higher at 35MHz.

Figure 2.6 and Figure 2.7 are the time and frequency domain of the digital frequency down converter with a 25MHz input respectively. The output of these signals is located at 0Hz and 50MHz along with residual higher frequencies. However, it can be seen in the frequency response in Figure 2.7 that the power in at 0Hz is very low. The time domain in Figure 2.6 shows that the signal is only oscillating between 1 and 0. The input signal is from 1 to -1 so the output should also be from 1 to -1, similar to both Figure 2.4 and Figure 2.8. The reason it only oscillates from 1 to 0 is because there is a 0Hz frequency in the signal that does not bring the higher frequency down to -1, instead the signal stays at a constant oscillation from 1 to 0. Since FFTs do not check whether or not a signal goes from 1 to -1 and only determines the oscillation of a signal, the frequency response does not show the full power located at 0Hz. The filter will easily filter out the signal at 50MHz since the stop band is at 35MHz. This will result in a DC signal being output from the filter.

Figure 2.8 and Figure 2.9 show the time and frequency domain of the DDC with a 40 MHz input. This simulates the highest input frequency ($25\text{MHz} + 15\text{MHz} = 40\text{MHz}$). The results show this also pushes the boundaries of the pass band for the filter, but the spike at 35MHz is a residual frequency due to the square wave LO and actually comes from the $3f_{\text{LO}} - f_{\text{IR}}$ ($75\text{MHz} - 40\text{MHz}$) = 35MHz and is therefore smaller than the 35 MHz that needs to be filtered with a 10 MHz input. The sum of the 40 MHz input and 25 MHz oscillator is located at 65 MHz and will easily be filtered out since it is well above the stop band. The useful information is located at $40\text{MHz} - 25\text{MHz} = 15\text{MHz}$.

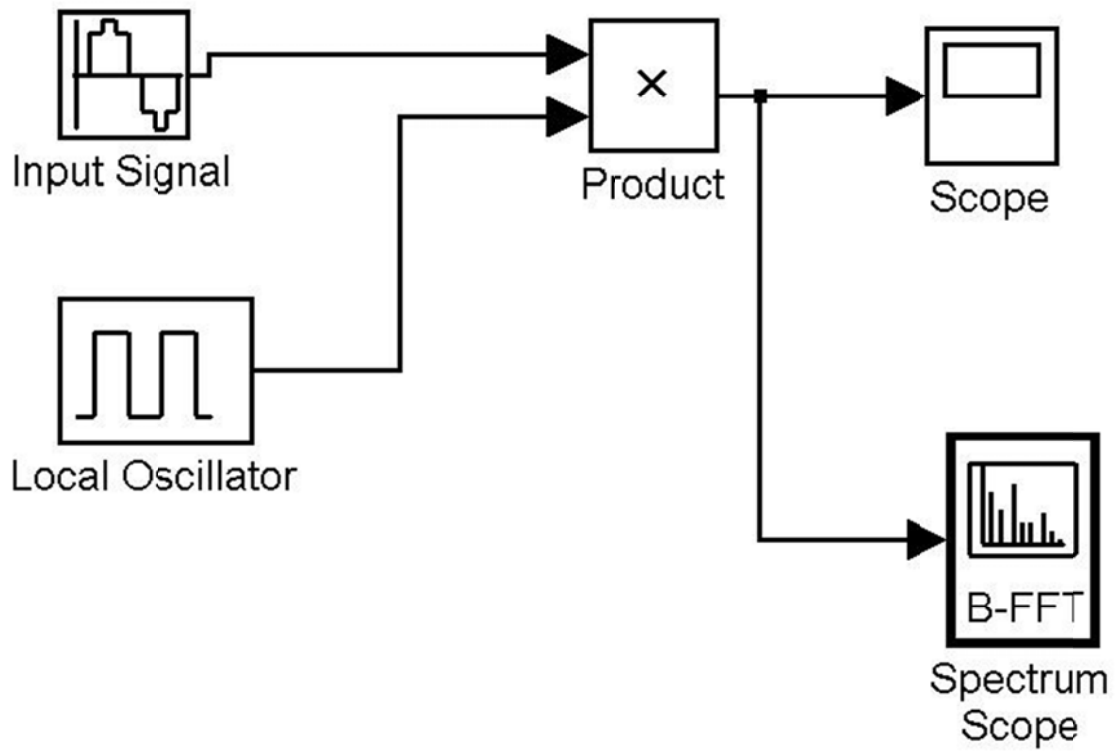


Figure 2.3 Matlab design for Digital Frequency Down Converter

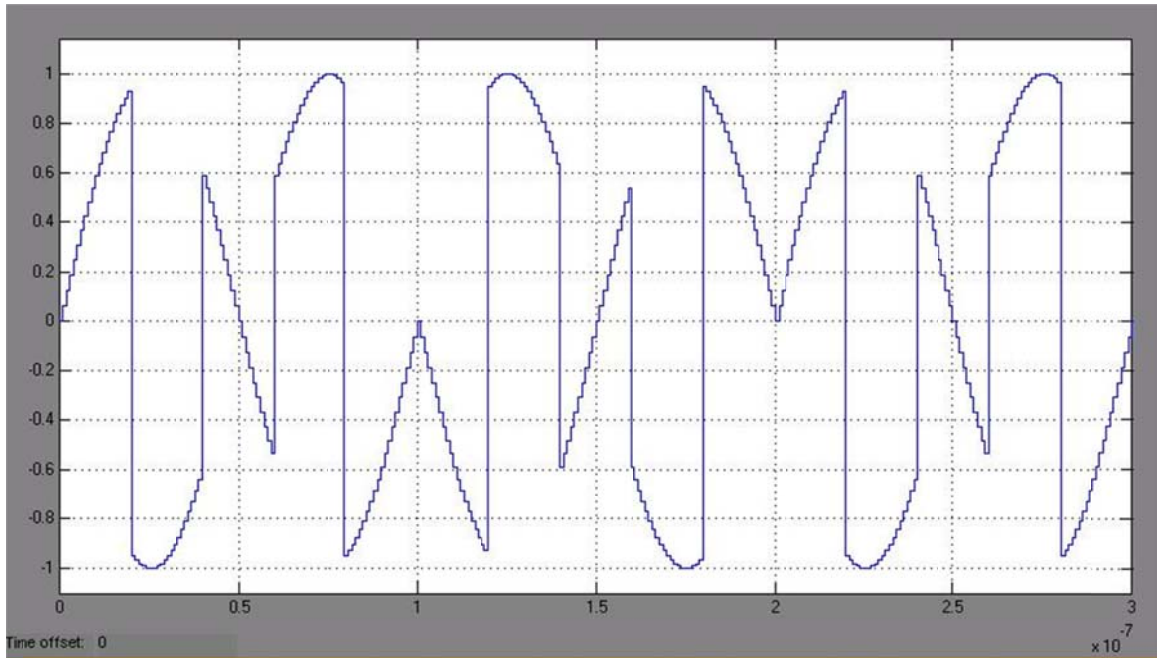


Figure 2.4 Time domain of the digital frequency down converter with a 10 MHz input in Matlab.

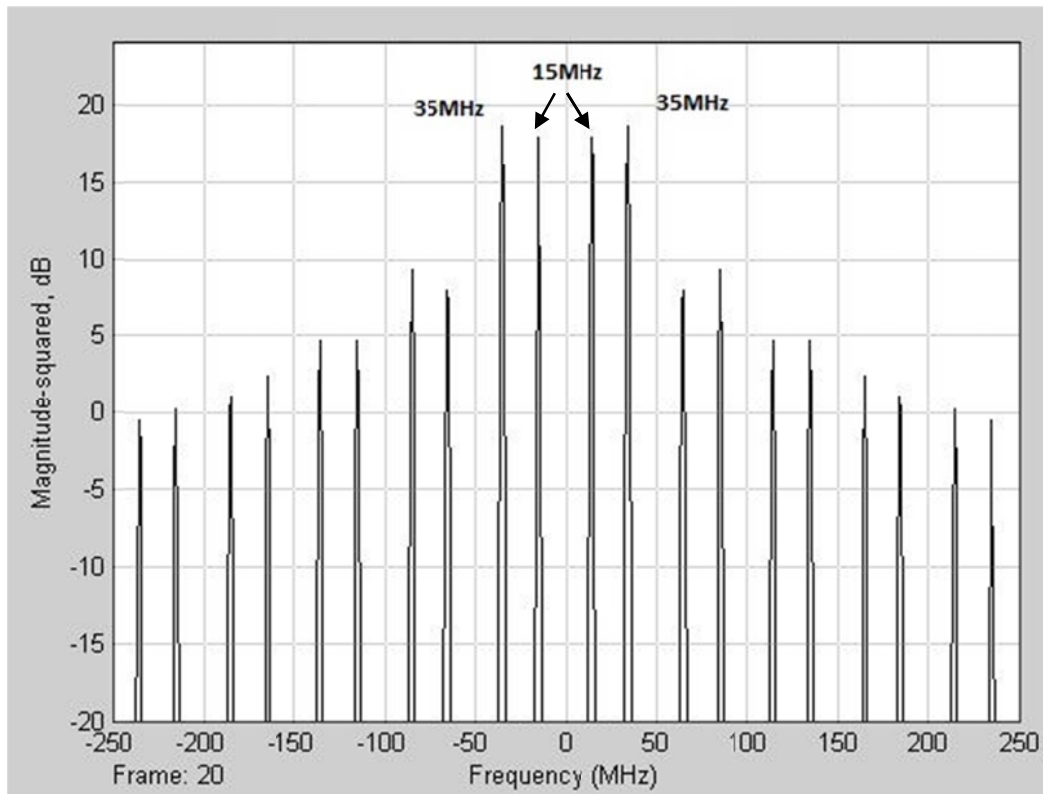


Figure 2.5 Frequency domain of the digital frequency down converter with a 10 MHz input in Matlab.

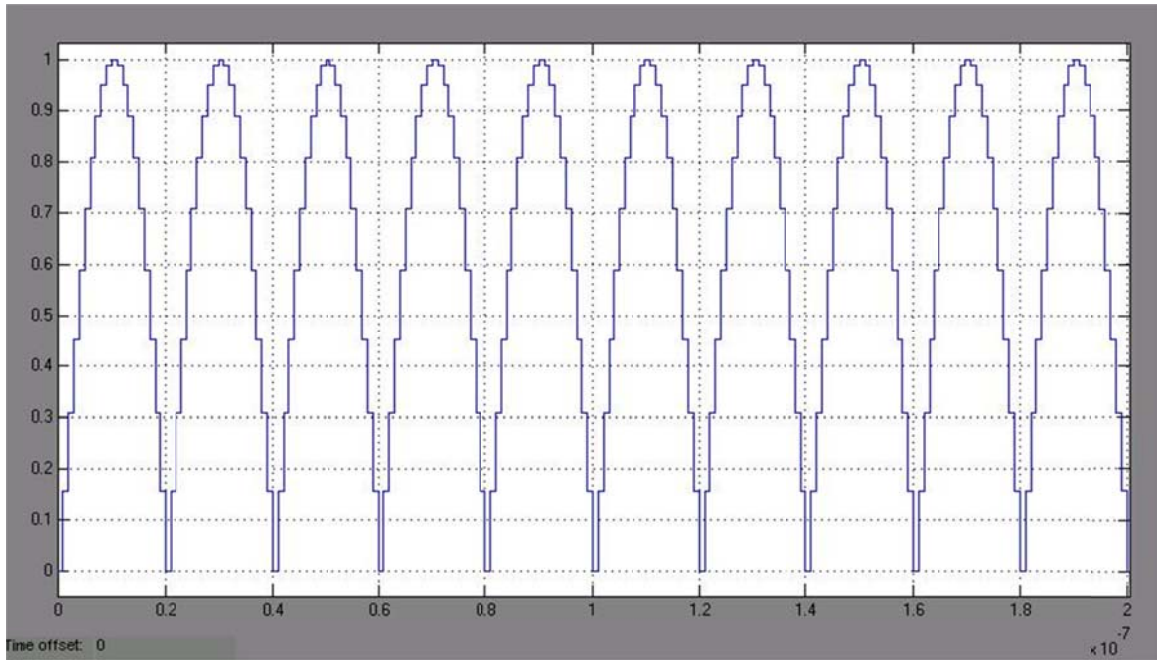


Figure 2.6 Time domain of the digital frequency down converter with a 25 MHz input in Matlab.

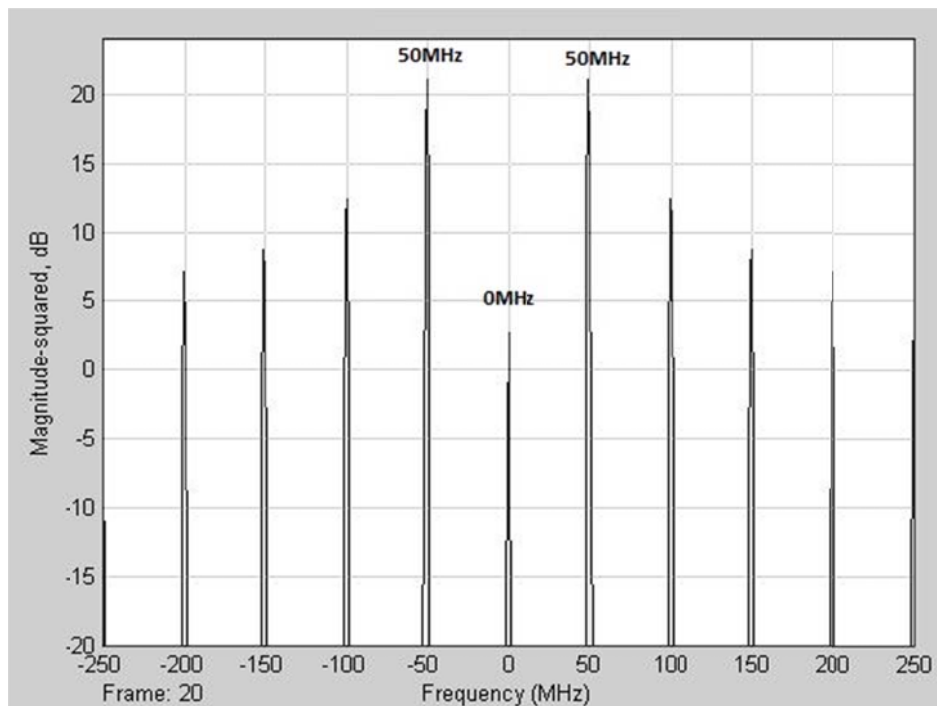


Figure 2.7 Frequency domain of the digital frequency down converter with a 25 MHz input in Matlab.

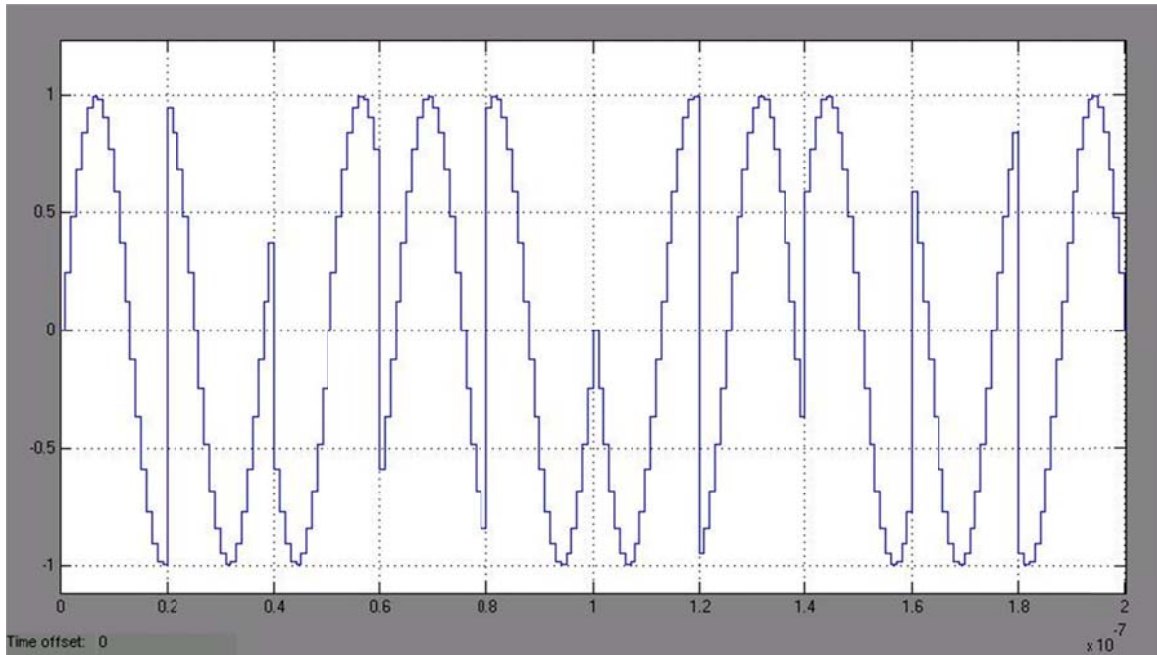


Figure 2.8 Time domain of the digital frequency down converter with a 40 MHz input in Matlab.

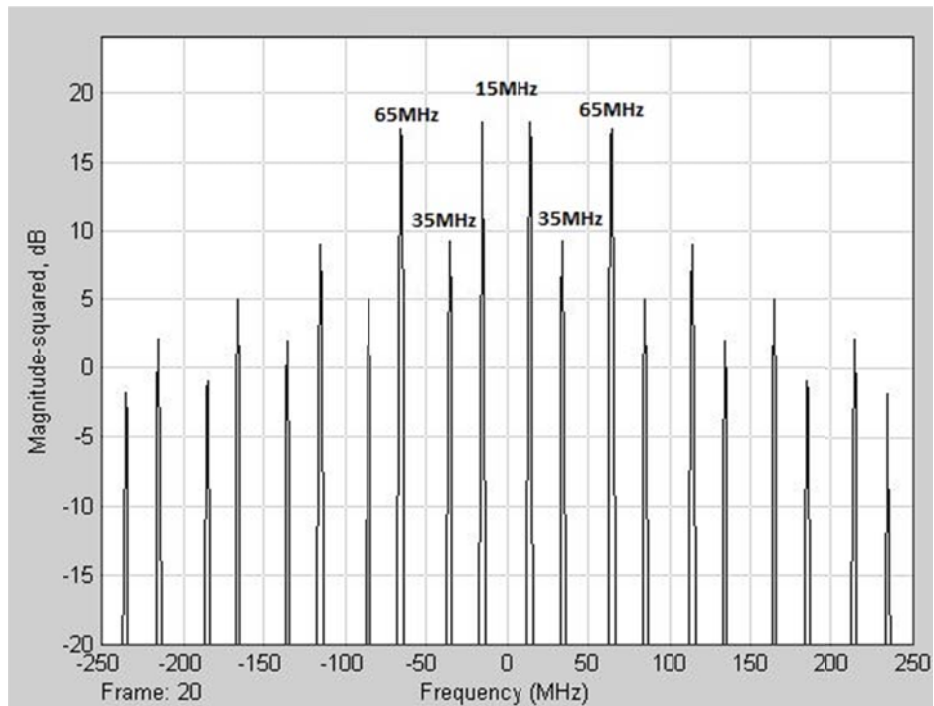


Figure 2.9 Frequency domain of the digital frequency down converter with a 40 MHz input in Matlab.

2.2.2 Schematic

With the simulations complete in Matlab, the DDC is designed as a schematic in Cadence by using CMOS 90m technology. The input signal has eight bits, and is standard binary, however the output is converted to two's complement before it is passed through the filter, the reason for this will be discussed later in the thesis. The DDC is designed to invert the input signal or let the input signal pass through, based on the state of the 25 MHz clock that is used. Since the input signal is centered or offset at 128 out of 256 on the incoming 8 bits, inverting all of the bits will simply flip or invert the incoming signal around the offset. Using a multiplexer and connecting the 25 MHz clock to the select pin of the multiplexer, a system can be designed for each bit where either the bit is passed through the multiplexer which in essence multiplies the bit by one, or it inverts the bit first and then passes the bit through the multiplexer which multiplies the bit by -1. The top level schematic design for this 8 bit DDC is given in Figure 2.10 which includes two 8 to four multiplexers and eight inverters. The two select signals come from the same source which is a 25 MHz square wave.

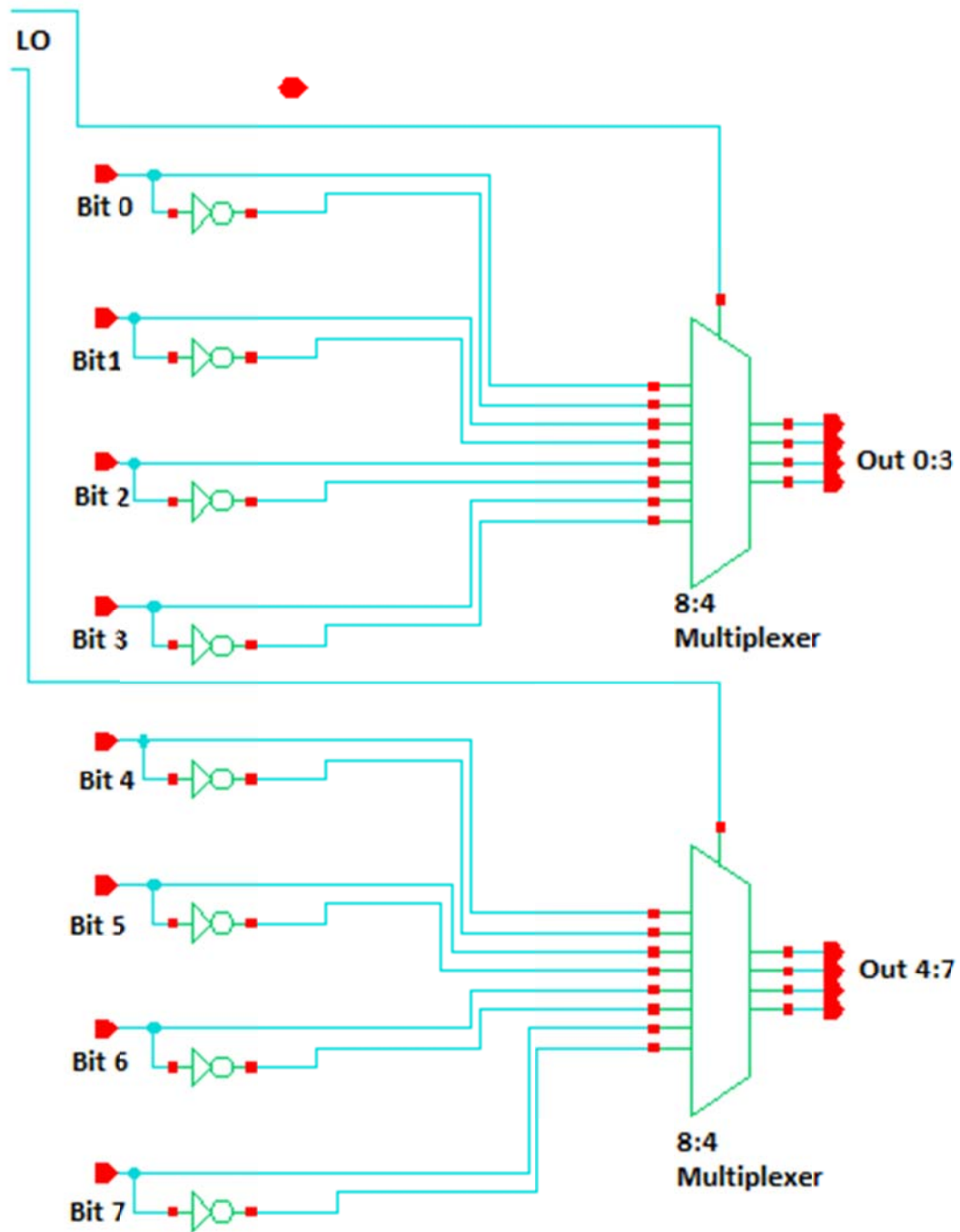


Figure 2.10 8-bit digital frequency down converter.

In order to make sure the design works like the model in Matlab, the same frequencies that were previously tested are input into the system. The input to this

system requires 8 bits instead of a single analog signal, so a simple sine wave input that is typically used in Cadence does not work. 10 MHz, 25 MHz, and 40 MHz signals are generated by Matlab and converted into eight txt files where each file represents each bit.. Figure 2.11 and Figure 2.12 show the time and frequency domain of the schematic with an input of 10MHz. Figure 2.11 and Figure 2.12 demonstrate that both the schematic and layout simulations are very accurate compared to the Matlab simulations. The next two figures, Figure 2.13 and Figure 2.14 show the results for the layout designs of the DDC with the same 10MHz input. Since the layout design is also digital, very similar results to the schematic design is expected and achieved. Figure 2.15through Figure 2.22 show the time and frequency domains of the output when the schematic and layout have an input of 25MHz and 40MHz. These results also coincide with the results from Matlab.

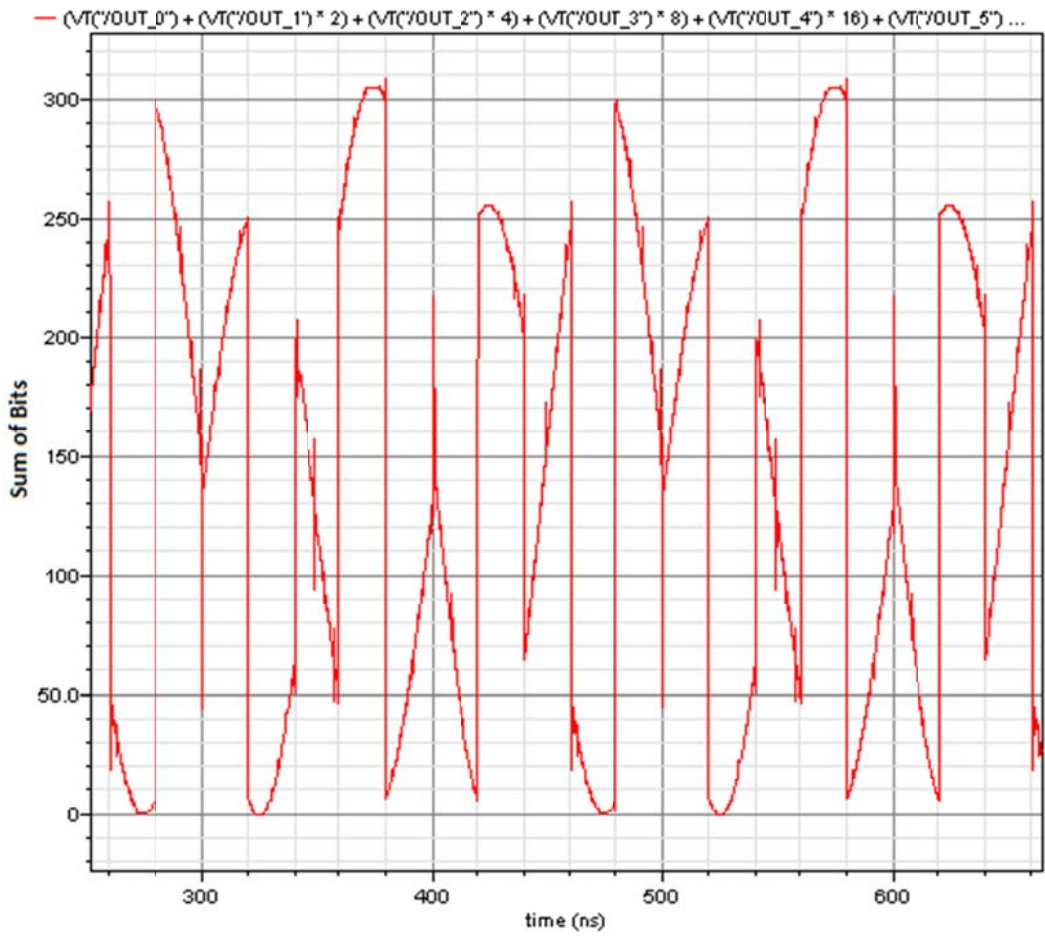


Figure 2.11 Time domain of the digital frequency down converter with a 10 MHz input from schematic.

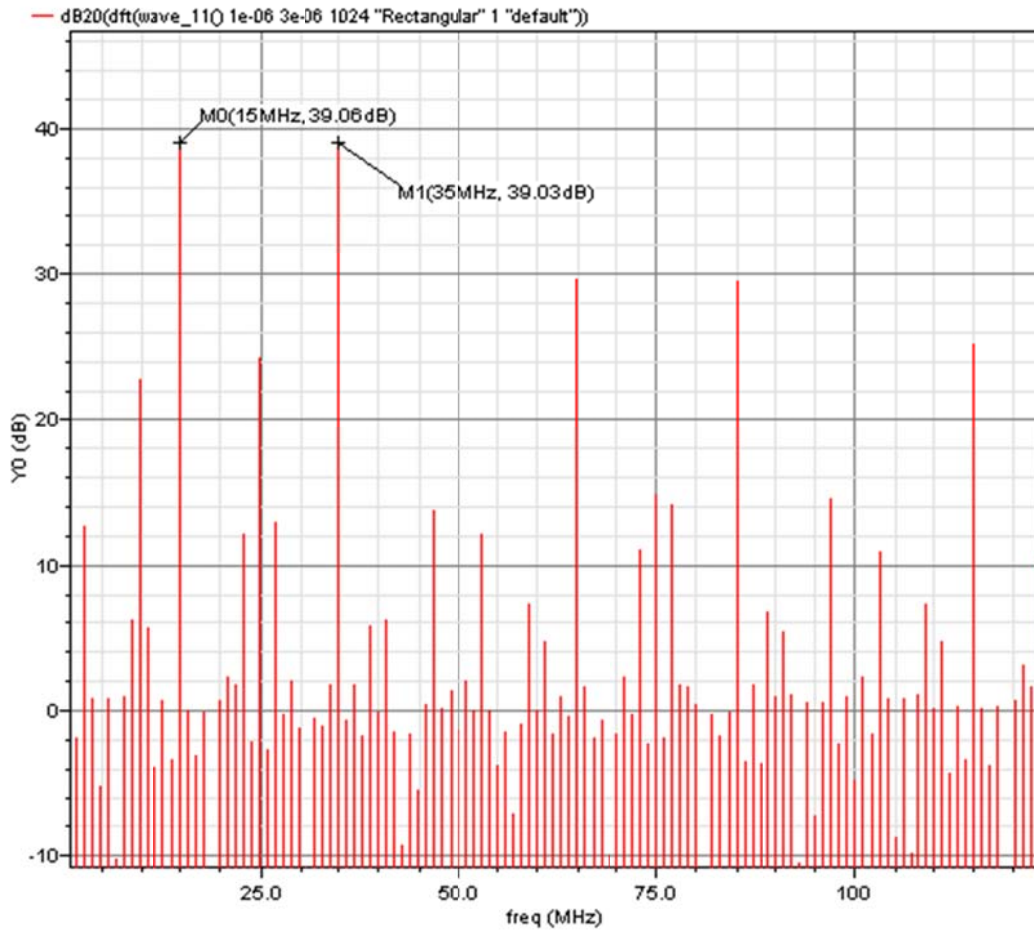


Figure 2.12 Frequency domain of the digital frequency down converter with a 10 MHz input from schematic.

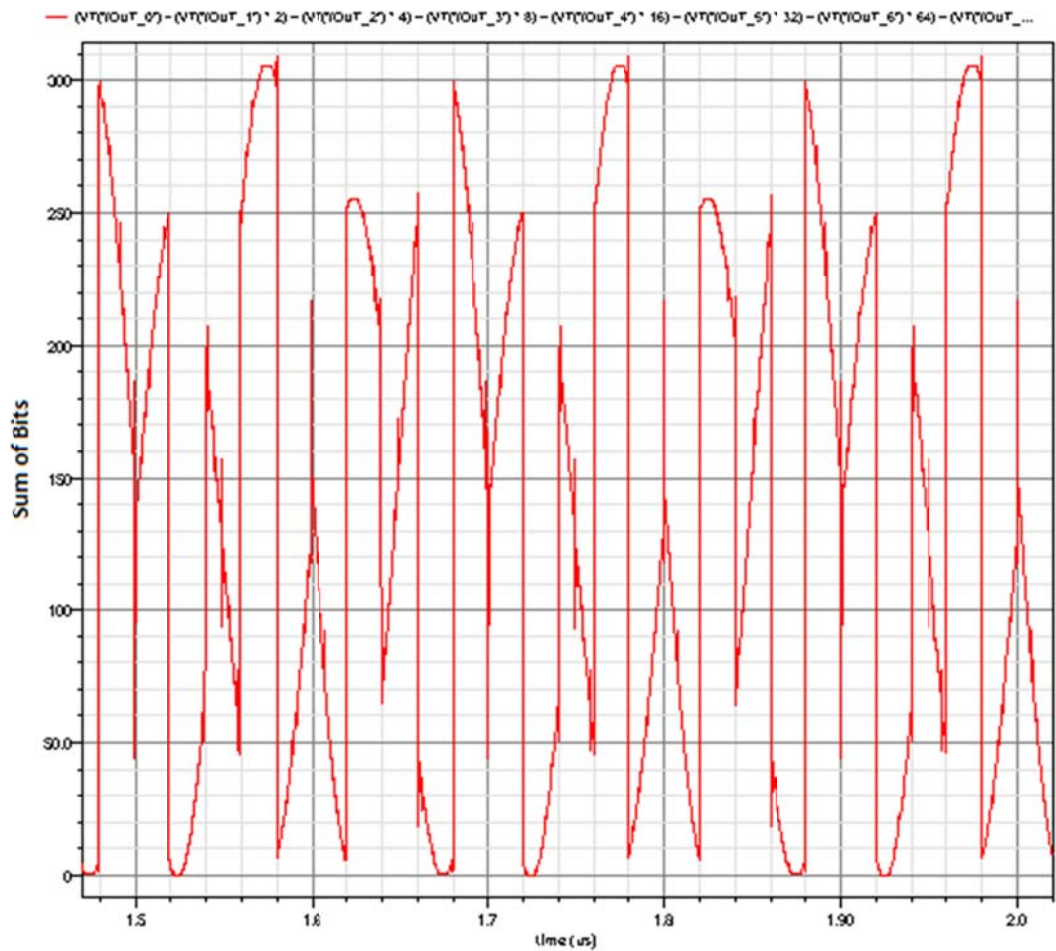


Figure 2.13 Time domain of the digital frequency down converter with a 10 MHz input from layout.

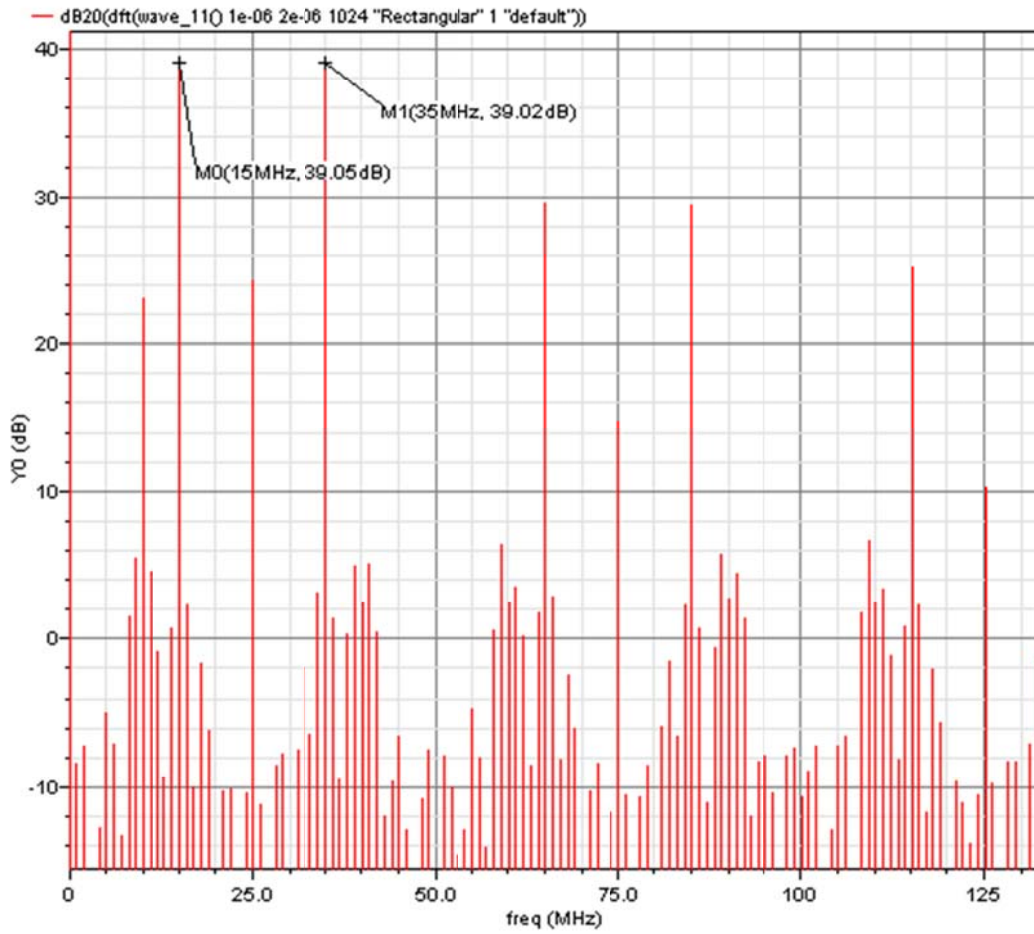


Figure 2.14 Frequency domain of the digital frequency down converter with a 10 MHz input from layout.

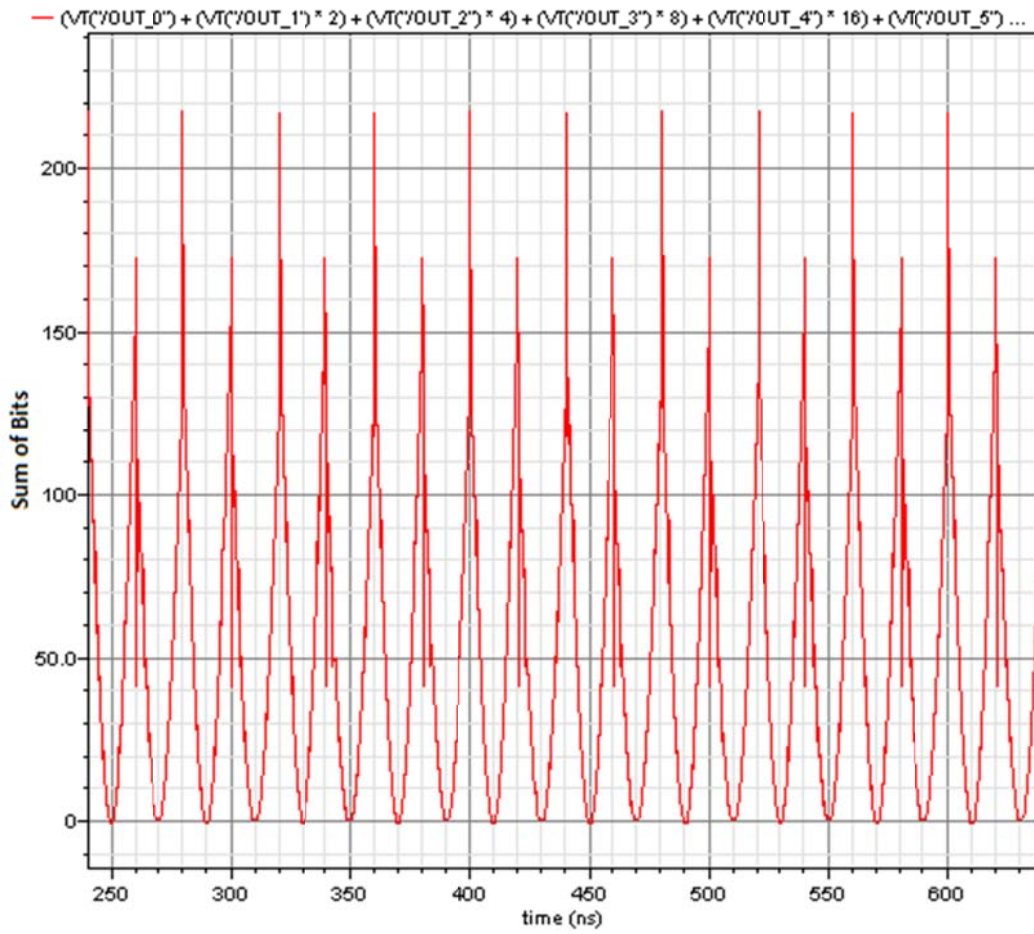


Figure 2.15 Time domain of the digital frequency down converter with a 25 MHz input from schematic.

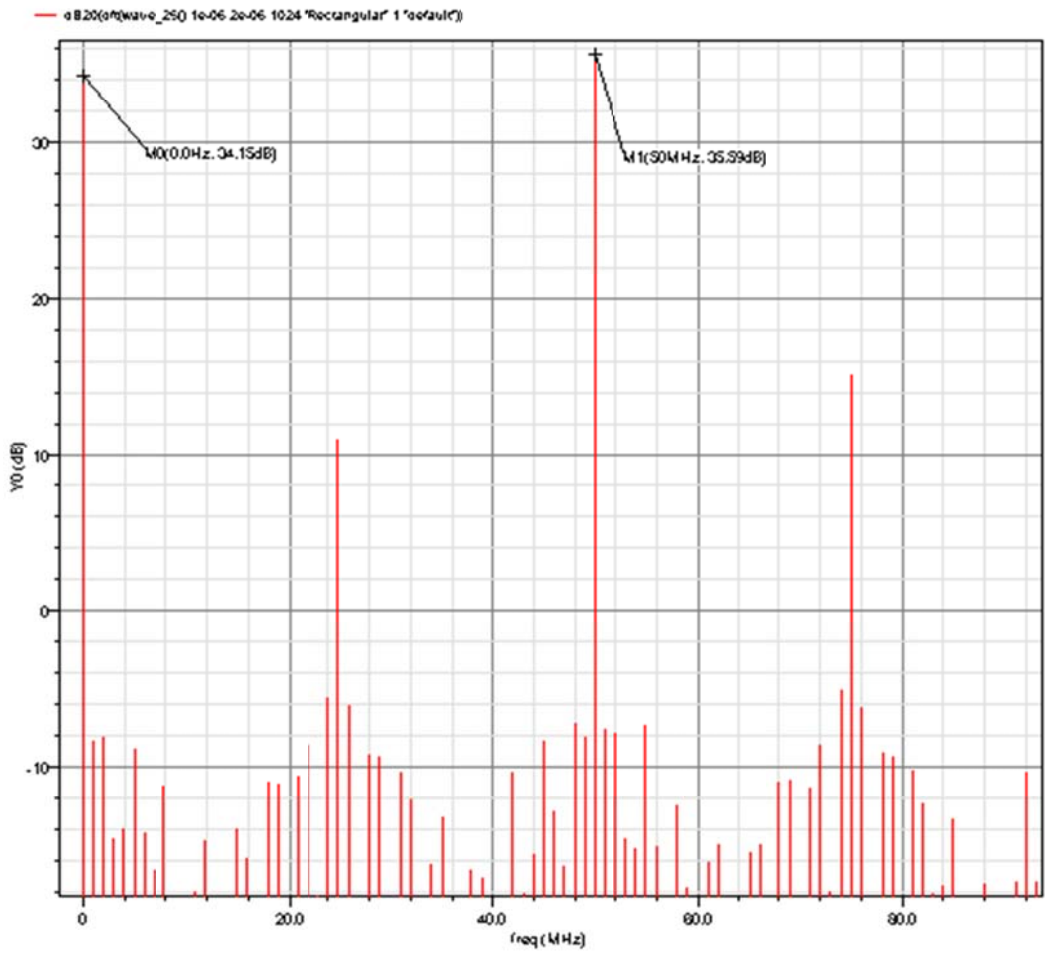


Figure 2.16 Frequency domain of the digital frequency down converter with a 25 MHz input from schematic.

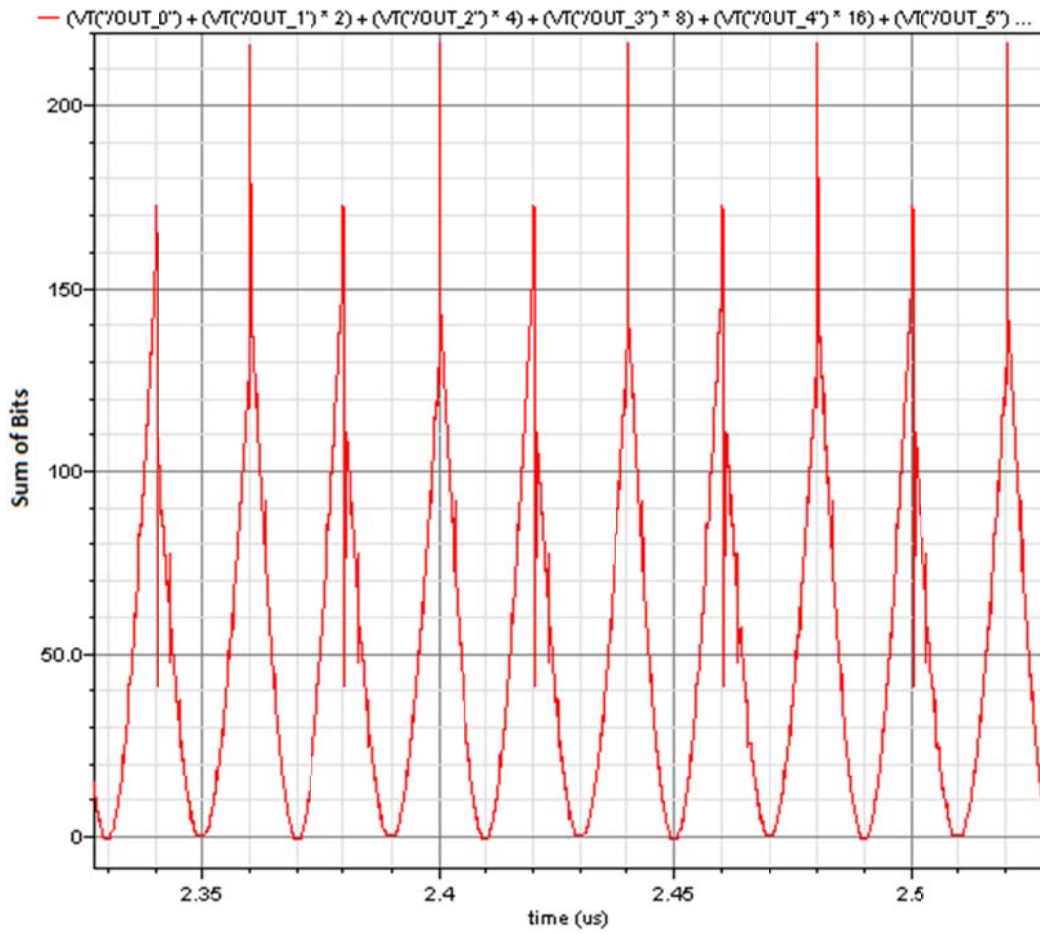


Figure 2.17 Time domain of the digital frequency down converter with a 25 MHz input from layout

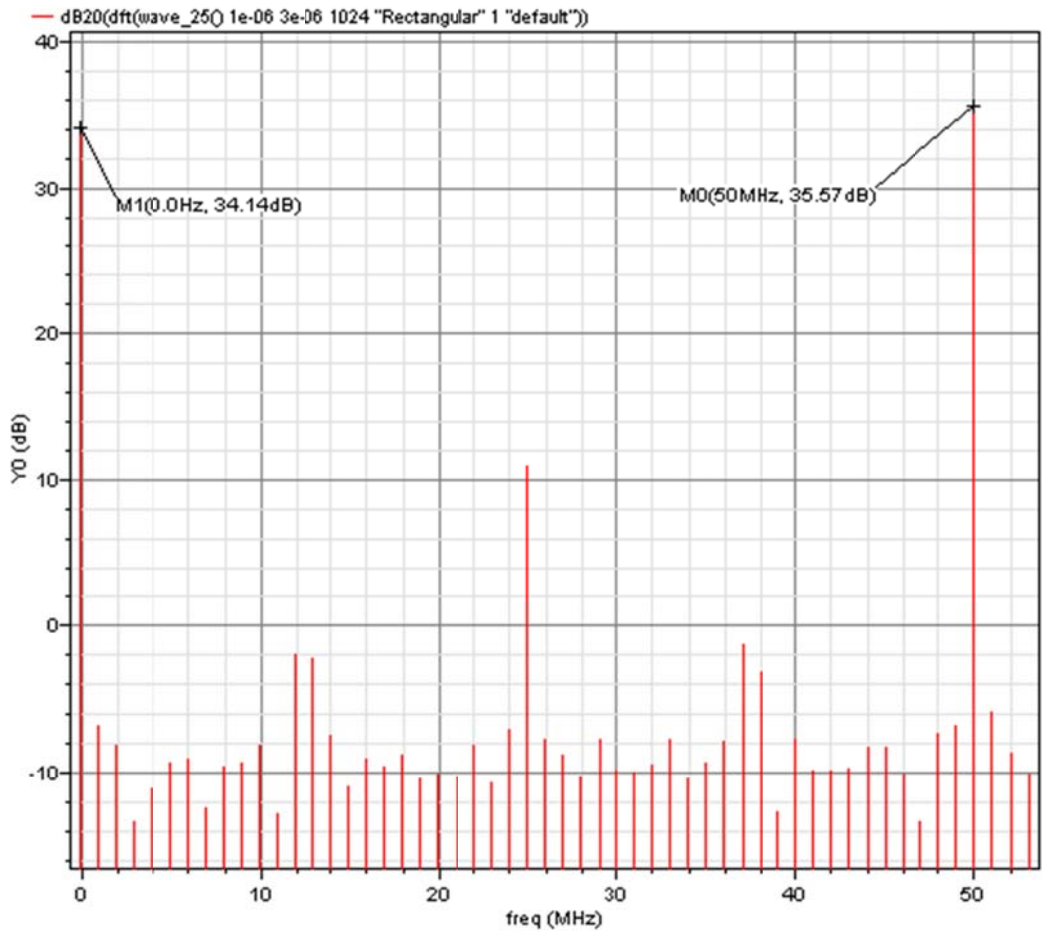


Figure 2.18 Frequency domain of the digital frequency down converter with a 25 MHz input from layout.

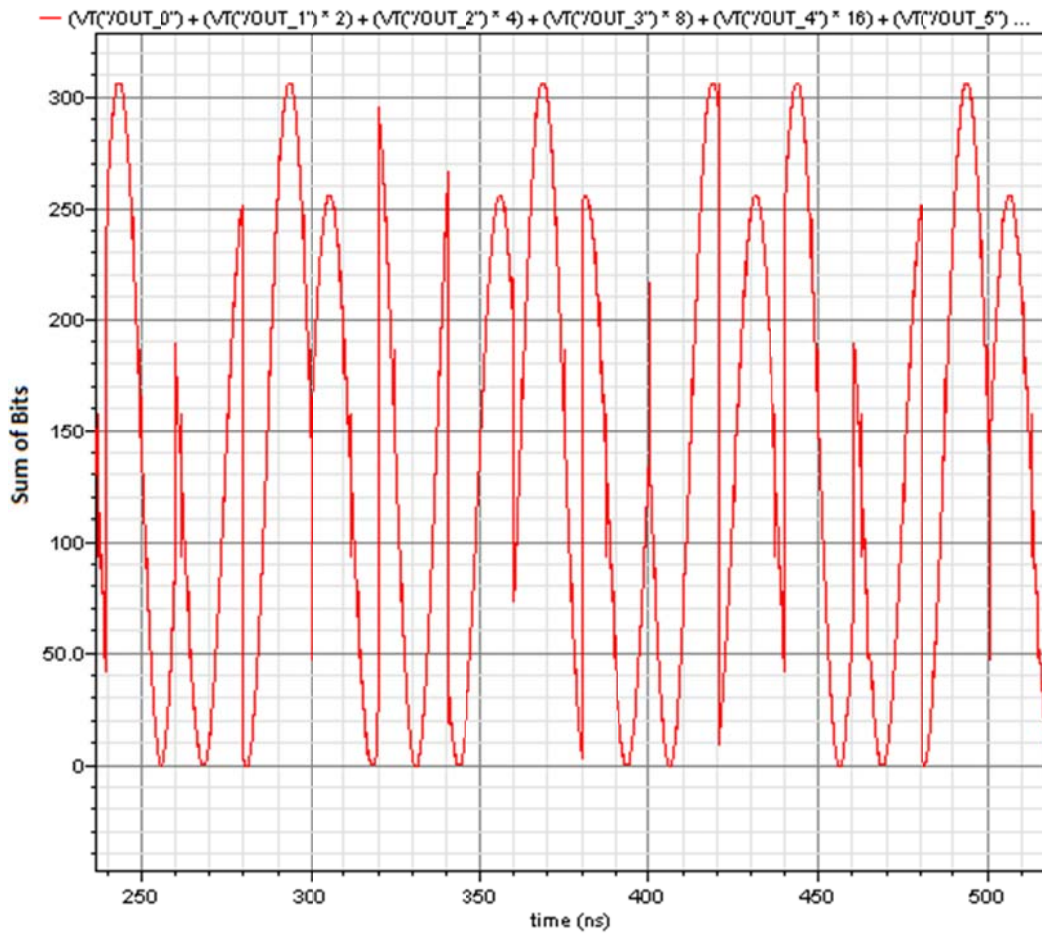


Figure 2.19 Time domain of the digital frequency down converter with a 40 MHz input from schematic.

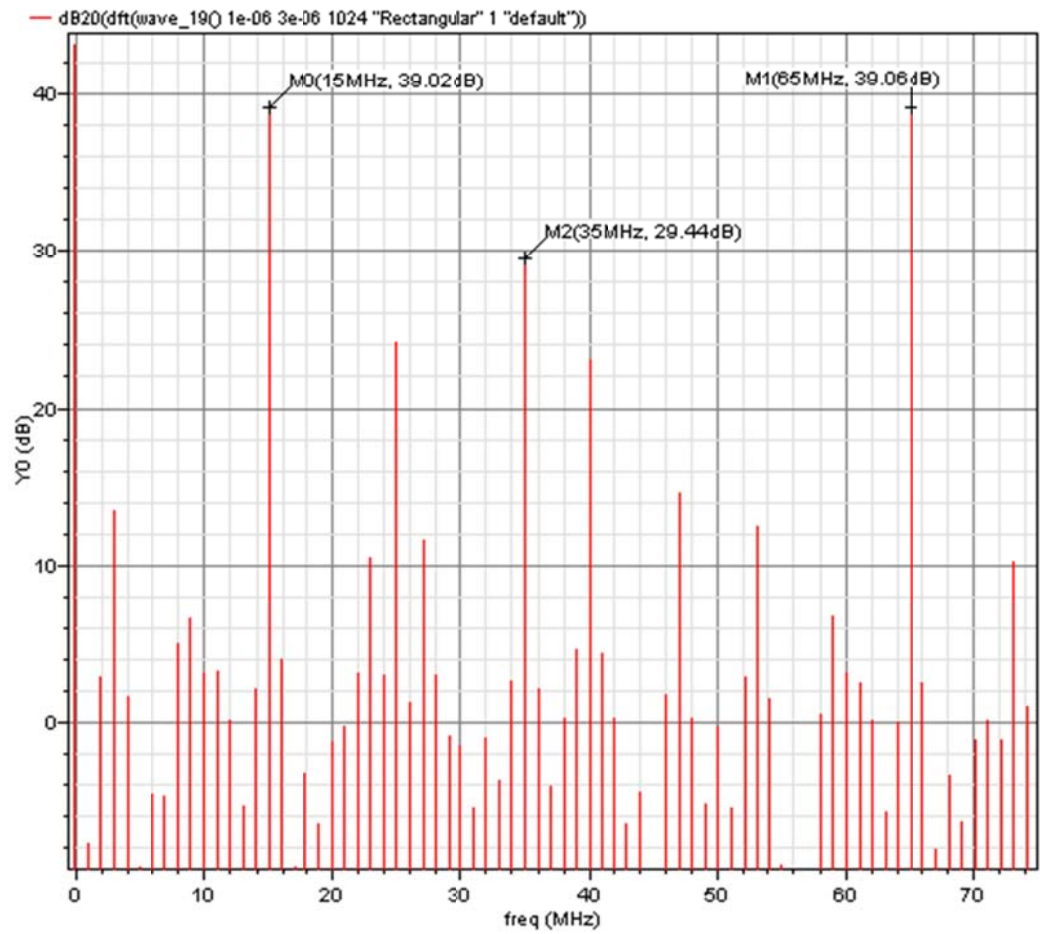


Figure 2.20 Frequency domain of the digital frequency down converter with a 40 MHz input from schematic.

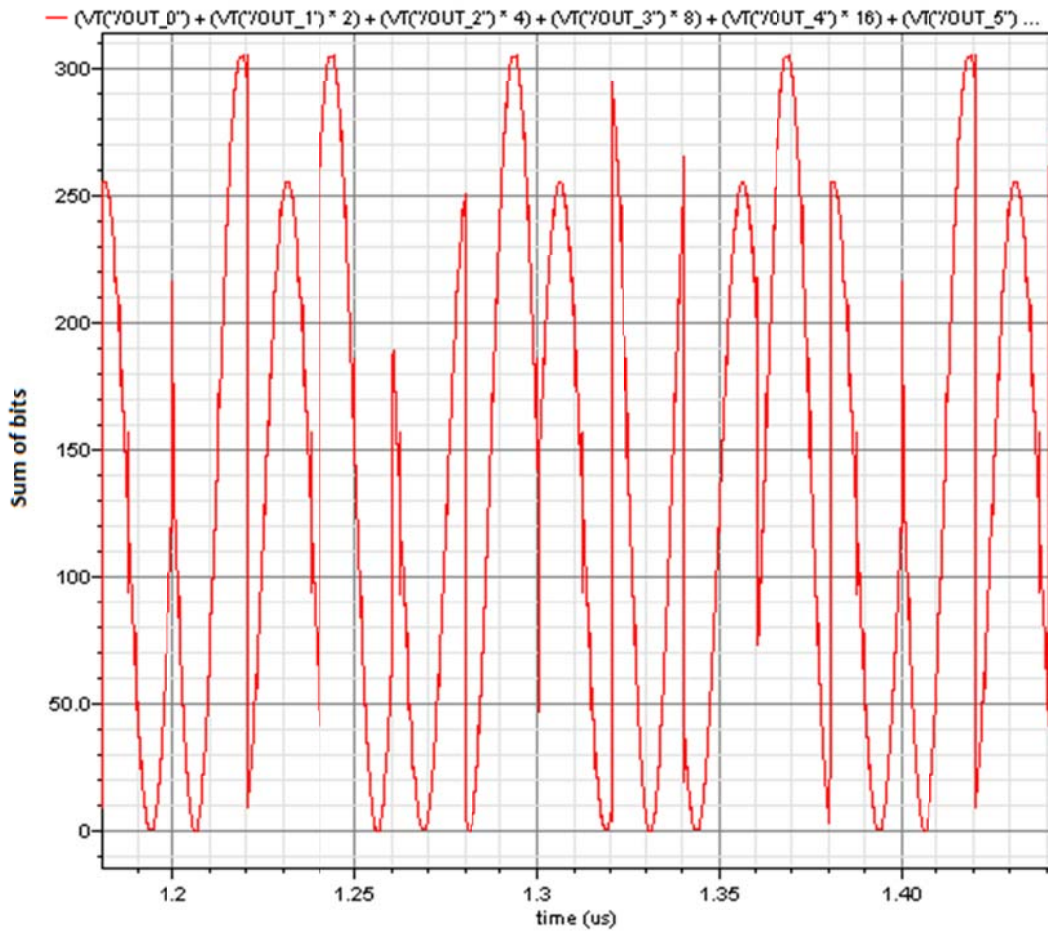


Figure 2.21 Time domain of the digital frequency down converter with a 40 MHz input from layout

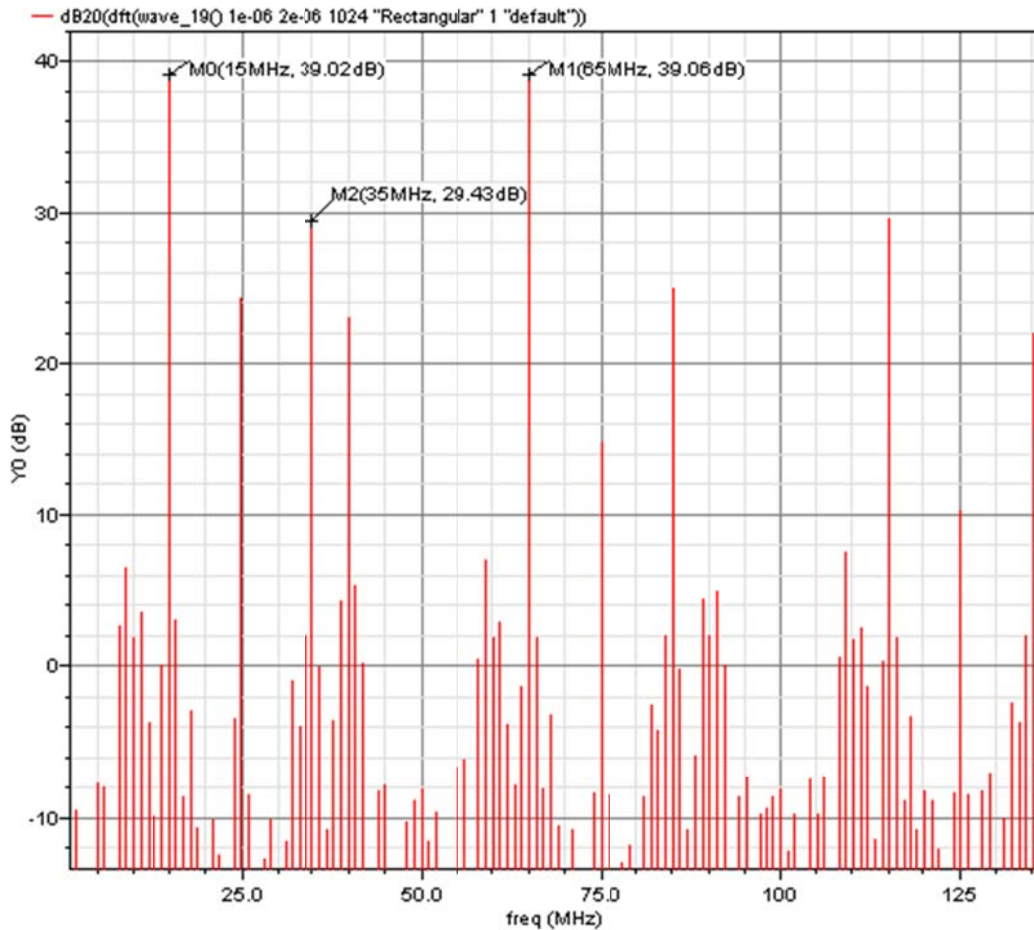


Figure 2.22 Frequency domain of the digital frequency down converter with a 40 MHz input from layout.

The design also requires both an I and a Q signal coming out of the DDC. In order to do this, two DDCs are used. The first DDC operates exactly like what has been discussed previously and will output the I signal. In order to get the Q signal, the output of the second DDC needs to be the same as the I signal but shifted 90 degrees. The 25MHz signal that is used as the LO comes from a 400MHz clock. Since the 400MHz frequency can be divided to get the 25MHz LO, a 50MHz signal can also be divided from the 400MHz clock frequency. In order to shift the frequency by 90 degrees, the 50MHz

signal and the 25MHz signal are input into an XOR gate and the output is a 25MHz signal with a 90 degree phase shift. Figure 2.23 shows the result of the XOR of the 50 MHz signal and 25 MHz signal. Later on in the thesis the output for the full DDC and SINC Filter are shown with both the I and Q output signals. The XOR Q signal is used as the LO for the DDC with the Q output.

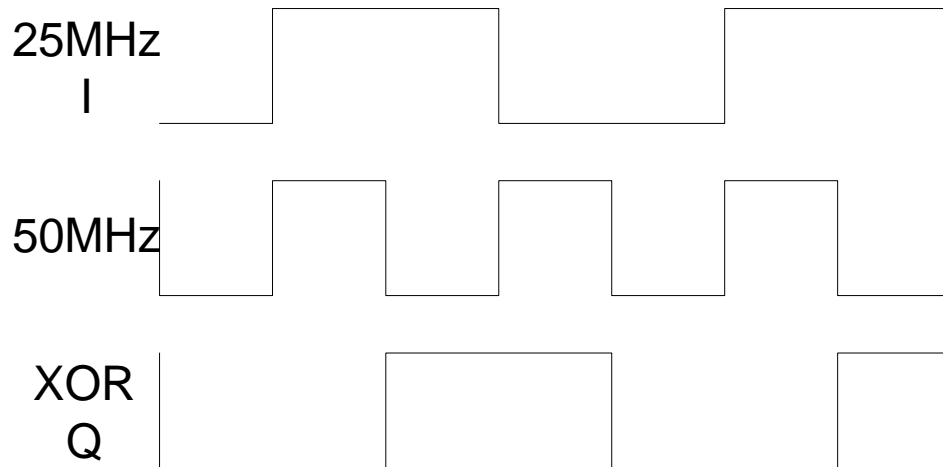


Figure 2.23 Design to use f_{LO} and have create the Q values. The XOR is the same frequency as the 25MHz I signal but it is shifted 90 degrees to give the Q signal.

2.3 Layout

The layout for the DDC has a very small area, since the DDC is a combination of only inverters and multiplexers that down converts the frequency of the incoming signal. The layout is designed to have the inputs on the left and the outputs on the right for easy data flow from left to right. The power consumption of the DDC with the clock frequency at 25MHz and the input frequency operating at 400MHz is 4.57uW. The size of the layout for the digital mixer is 3.735um x 118.745um. The elements for the DDC also were designed so that the vdd and vss lines are compatible with the layout elements of the low pass filter.



Figure 2.24 Layout of the digital frequency down converter after a 90 degree rotation

The design for the DDC uses the 8 to 4 multiplexer shown in Figure 3.21.

3 Digital Filter

3.1 Requirements

The low pass digital filter is designed to allow the signal at baseband to pass through but to stop the higher frequencies. In this design, a specific implementation for a smart antenna requires $f_{IF}=25\text{MHz}$ with a signal bandwidth of $\pm 15\text{MHz}$ (30MHz). The worst case input signal is when the input is 10MHz (25MHz–15MHz). This results in an output signal with frequencies located at 15MHz (25MHz–10MHz) and 35MHz (25MHz+10MHz). The f_{IF} signal has a bandwidth of 30MHz so the pass band is at 15MHz and a stop band at 35MHz. This allows for the baseband signal to pass through without any losses and eliminates all of the high frequency signals created by the DDC that will be present in the down converted signal.

3.2 Design

With a square wave LO, we would expect to see the digital outputs centered at DC, 50MHz, 100MHz, 150MHz, ... with bandwidths of $\pm 15\text{MHz}$. If we give an IF input of 10MHz we can expect a spectrum with outputs at 15MHz, 35MHz, 65MHz, 85MHz, 115MHz, ... with the baseband signal at 15MHz. The 15MHz IF input results in the undesired harmonic having the lowest frequency of 35MHz, so the stop band frequency for the low pass filter design is set at 35MHz for this example. The pass band frequency is set at 15MHz to give the desired bandwidth of 30MHz centered at DC. For this application, the sampling frequency is set at $16f_{IF}$; however, with the square wave oscillator, the sampling frequency can be set to any value up to the maximum frequency of the ADC. As will be discussed below, if the sampling frequency is constrained to $4f_{IF}$,

then the desired stop band frequency of 35MHz can not be met with the use of multiplier-less cascaded integrator comb (CIC) or FIR SINC filters.

For this implementation, we need a LPF with pass band of 15MHz and stop band at 35MHz with stop band attenuation of at least 30dB. The low pass filter is typically implemented with a CIC filter or cascaded FIR SINC averaging filter [3]. A four stage CIC filter and four stage FIR averaging filter are shown in Figure 3.1 and Figure 3.2. The transfer function for both filters is given by

$$H(z) = \frac{(1-z^{-D})^N}{(1-z^{-1})^N} = (\sum_{k=0}^{D-1} z^{-k})^N \quad (2)$$

In Equation 2, D represents the decimation of the sampling frequency for a CIC filter or the number of delays in a SINC filter. N represents the number of stages of the filter. The filters in Figure 3.1 and Figure 3.2 have N=4 and D=10. The CIC filter in Figure 3.1 does not decimate the sampling frequency after the integrator stages on top and prior to the comb stages on the bottom since the application required no decimation. The CIC filter can be implemented with a decimation of f_s/D for the combs. The magnitude of the frequency response for both filters is given by

$$|H(f)| = \left| \frac{\sin(\pi Df)}{\sin(\pi f)} \right|^N \quad (3)$$

Both filters have nulls at each multiple of f_s/D . For our implementation example, we desire a stop band frequency of 35MHz, so with a sampling frequency of 400MHz, we could implement a filter with D=10 to give a first null at 40MHz. With N=4, then the frequency response that is obtained is shown in Figure 3.3. If the sampling frequency was constrained to $4f_{IF}$ (100MHz), the filters would have nulls at $100\text{MHz}/D$, which does not

permit a stop band frequency of 40MHz. So these filters have to be designed for specific sampling frequencies.

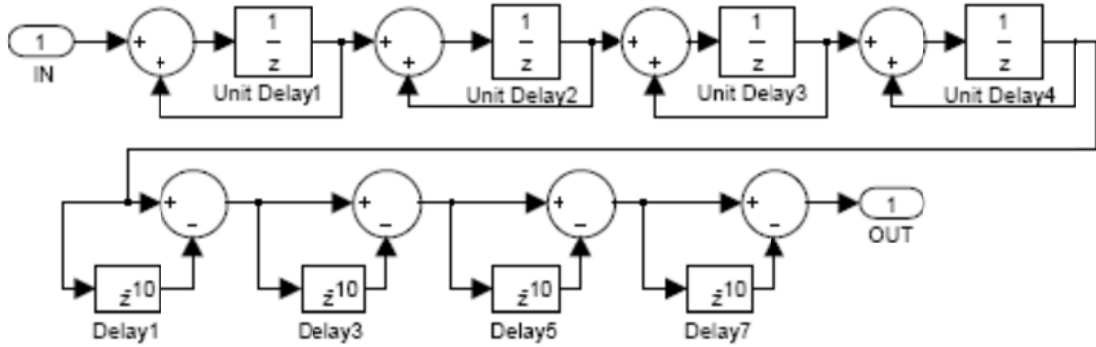


Figure 3.1 Four stage Cascaded Integrated Comb (CIC) Filter.

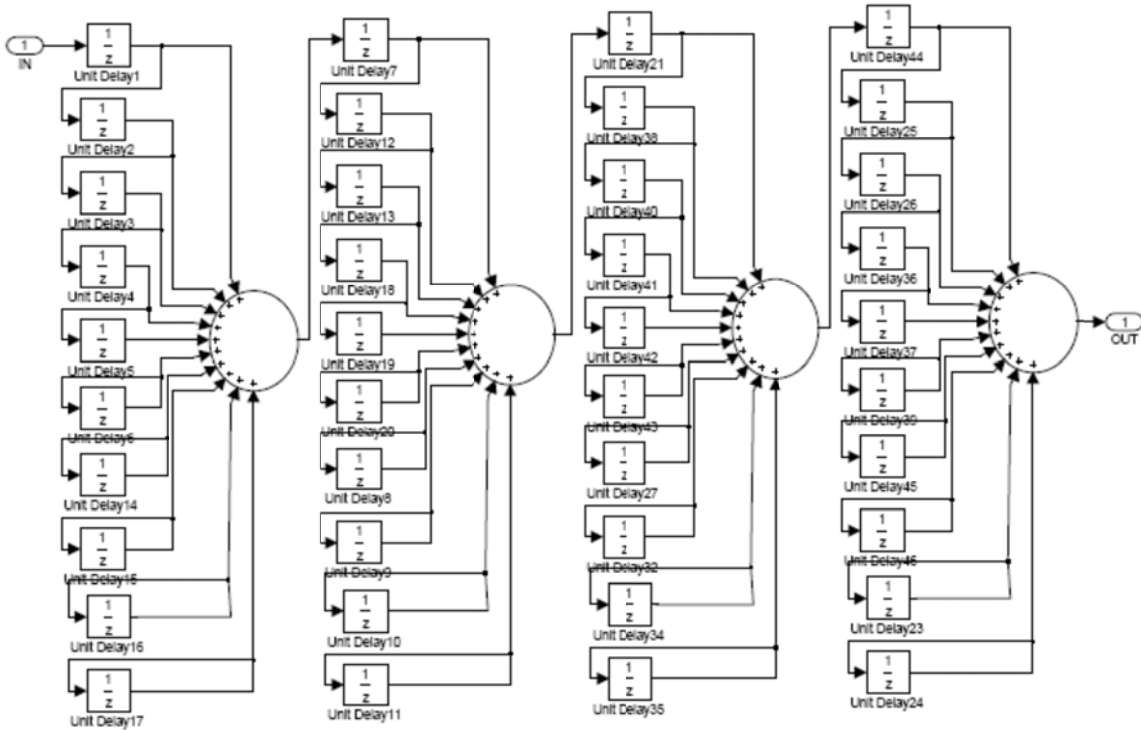


Figure 3.2 Four stage FIR SINC averaging filter.

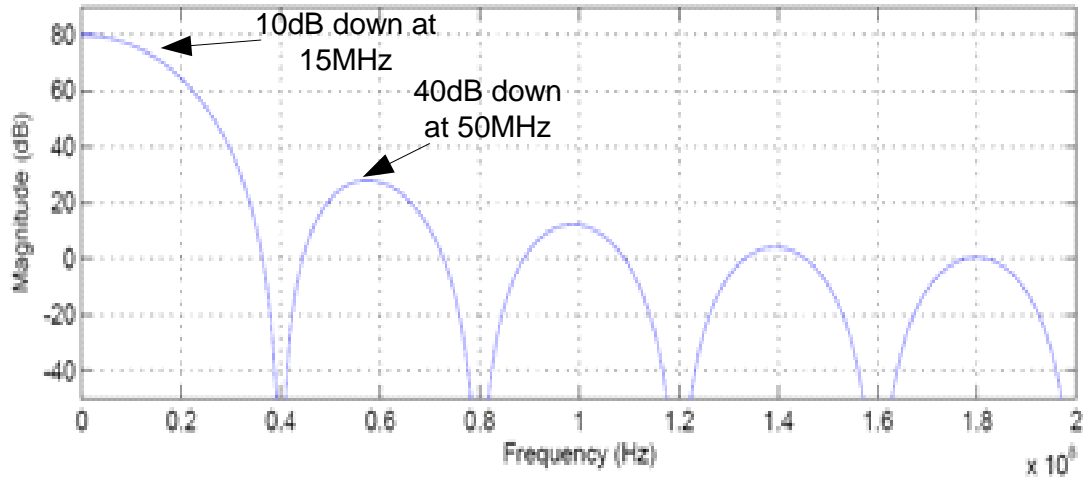


Figure 3.3 Frequency Response for CIC or FIR SINC Filter (D=10 and N=4)

It is noted from Figure 3.3 that the stop band attenuation does not reach the desired 35dB for this case (e.g. 50MHz). Instead it has a stop band of (40dB-10dB) 30dB. The response can be improved by implementing a pseudo multi-rate CIC or FIR averaging filter with four cascaded sections with D1=10, D2=9, D3=7, and D4=6. The transfer function is given by

$$H(z) = \left[\frac{(1-z^{-D_1})}{(1-z^{-1})} \right] \left[\frac{(1-z^{-D_2})}{(1-z^{-1})} \right] \left[\frac{(1-z^{-D_3})}{(1-z^{-1})} \right] \left[\frac{(1-z^{-D_4})}{(1-z^{-1})} \right] \quad (4)$$

The magnitude frequency response is

$$|H(z)| = \left[\frac{\sin(\pi D_1 f)}{\sin(\pi f)} \right] \left[\frac{\sin(\pi D_2 f)}{\sin(\pi f)} \right] \left[\frac{\sin(\pi D_3 f)}{\sin(\pi f)} \right] \left[\frac{\sin(\pi D_4 f)}{\sin(\pi f)} \right] \quad (5)$$

Changing the values of D for each comb of the CIC filter or for each stage of the FIR filter changes the null frequencies to f_s/D_1 , f_s/D_2 , f_s/D_3 , and f_s/D_4 , which has the effect of changing the sampling frequency. The frequency response obtained for the modified filters is shown in Figure 3.4.

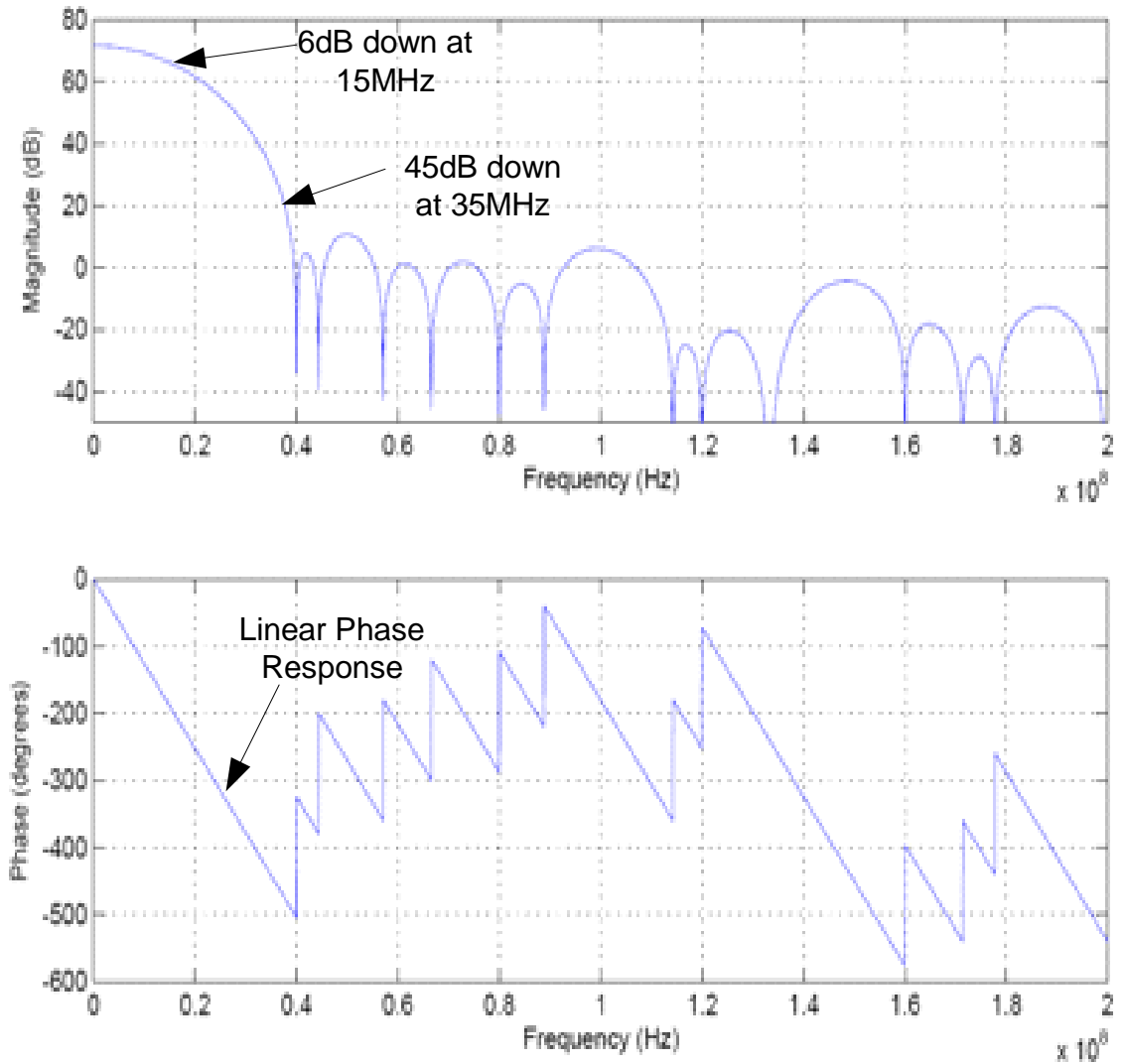


Figure 3.4 Frequency Response (top) and phase (bottom) for Pseudo Multi-rate SINC Filter with Four Cascaded Sections

It is seen from Figure 3.4(top) that the desired stop band attenuation of about 39dB is obtained and also that the linear phase response (bottom) is maintained in the pass band and even just past the stop band (40MHz). It is noted that the droop in the pass band of 15MHz is 6dB for the Pseudo Multi-rate SINC Filter Figure 3.4 compared to 10dB for the standard CIC Figure 3.3 or standard SINC averaging filter with $D=10$ and $N=4$. Thus the FIR compensation filter, which would be added for most applications to

reduce the pass band droop to the desired value, would be less demanding for the modified filters.

Figure 3.5 shows the MATLAB simulation result of the multiplier-less DDC with the square wave LO and either the pseudo multi-rate CIC or FIR SINC filter with an IF input of 10MHz. It is noted in Figure 3.5 that the worst case baseband input of 10MHz results in all harmonics being suppressed by at least 35dB below the passband. Figure 3.5 also shows that the harmonics associated with the square wave LO are completely suppressed except for the 35MHz harmonic.

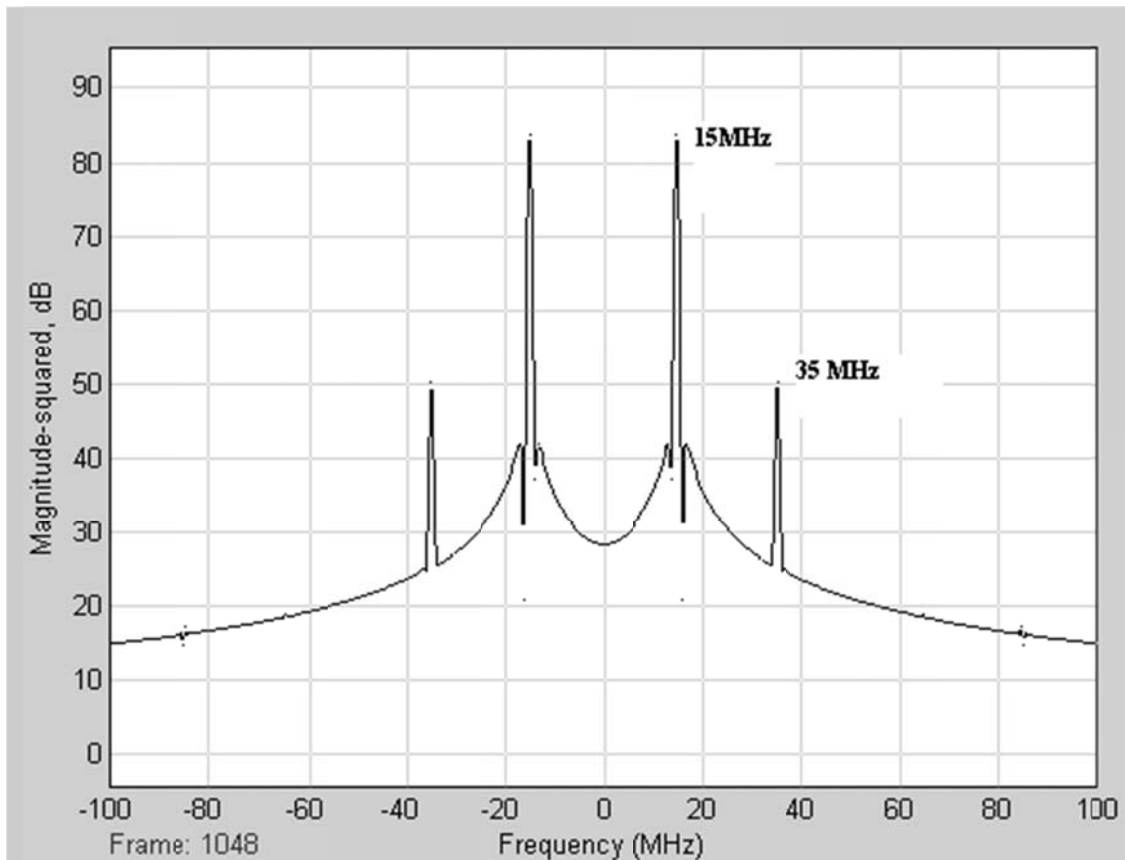


Figure 3.5 Matlab frequency response of the DDC and SINC Filter with a 10 MHz input.

3.3 Testing

3.3.1 Matlab

One of the strategies in picking the D values for the SINC filters is to try to eliminate the stop band peaks from the previous filter by choosing a D value that has zeros where the previous filter had peaks. From Figure 3.6 it can be seen that the 10 delay filter is a pass filter for 15MHz but once it gets to 35MHz filter it has gotten close to the null located at $f_s/D = 400\text{MHz}/10 = 40\text{MHz}$ in the frequency response. The next filter in Figure 3.7 has 9 delays and has a larger pass band than the first filter. This is not a problem because the 10 delay filter will filter out the stop band. The second filter's null position is located at $400\text{MHz}/9 = 44.44\text{MHz}$ which is slightly higher than the null of the first filter and works to cancel out part of the peaks of the first filter. Figure 3.8 shows the 7 delay SINC filter. It has a higher frequency for its first null than the 9 delay filter located at $400\text{MHz}/7 = 57.14\text{MHz}$ which contributes to canceling out the peaks in the first filter. Figure 3.9 shows the frequency response of the final filter of the four cascaded SINC filters, the 6 delay SINC filter. This filter has a higher frequency for its first null than the first two filters, yet is still at a lower frequency than the second null of the first 10 delay filter. The first null of the 6 delay filter is located at $400\text{MHz}/6 = 66.7\text{MHz}$. These filters combine together to get rid of all of the resonating peaks in the filters besides the main low pass area. The final filter response in Matlab shown in Figure 3.10 makes it clear that the residual peaks in the SINC filters have been flattened out and that the pass band and stop band are close to 50 dB apart.

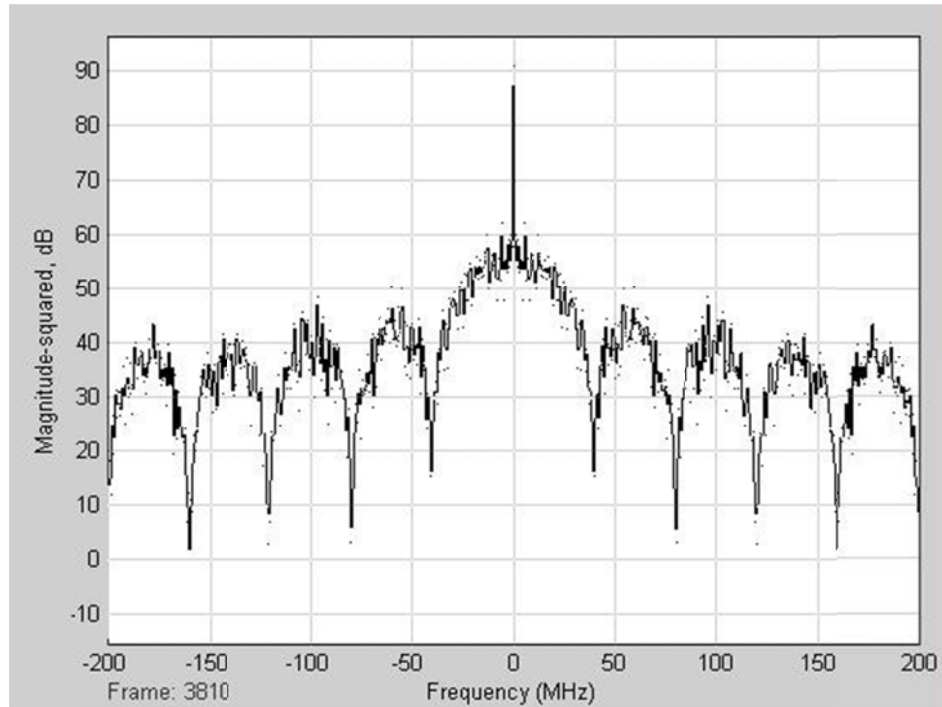


Figure 3.6 Frequency response of the 10 delay SINC Filter. The first null is located at 40MHz.

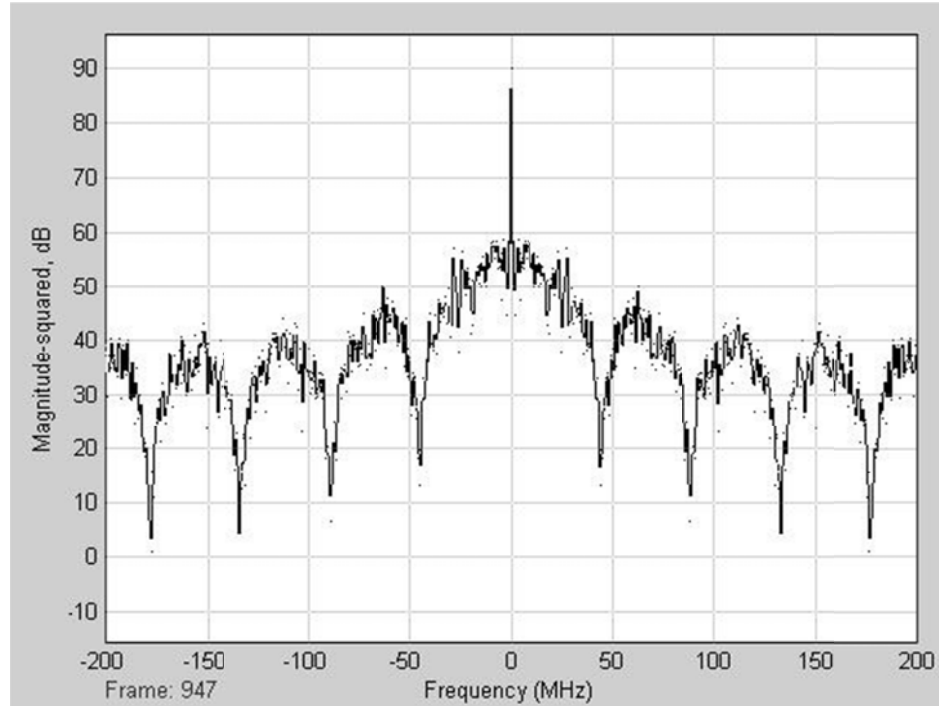


Figure 3.7 Frequency response of the 9 delay SINC Filter. The first null is located at 44.44MHz.

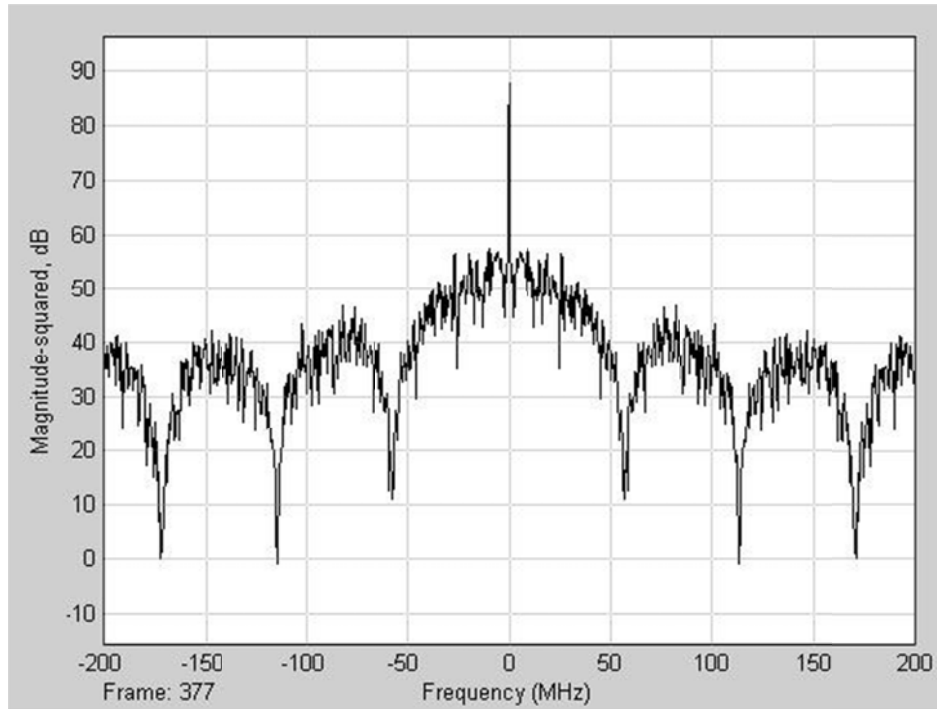


Figure 3.8 Frequency response of the 7 delay SINC Filter. The first null is located at **57.14MHz.**

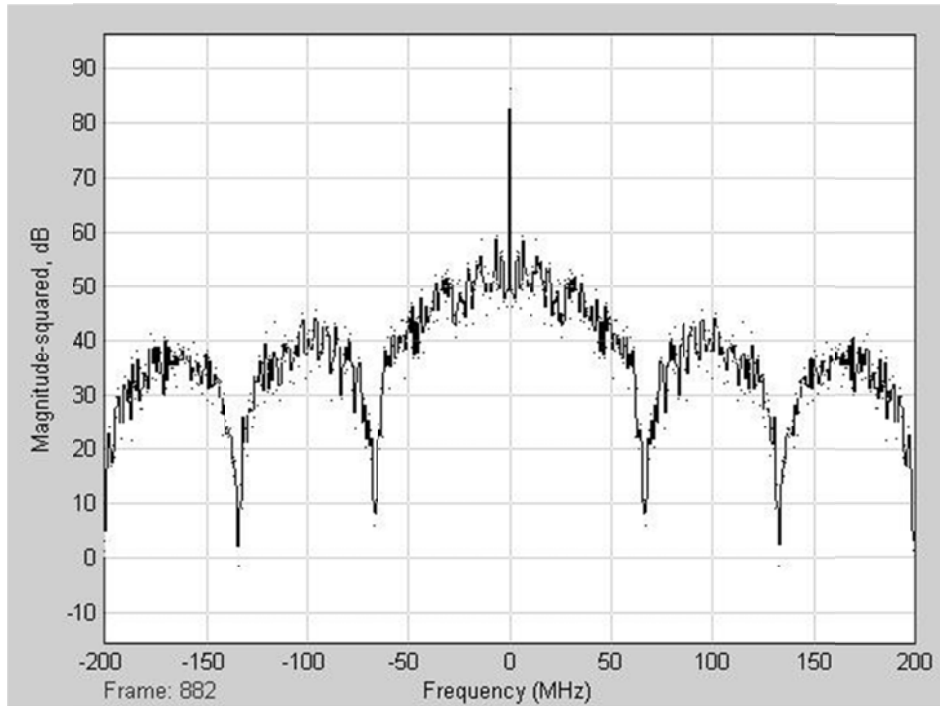


Figure 3.9 Frequency response of the 6 delay SINC Filter. The first null is located at **66.7MHz.**

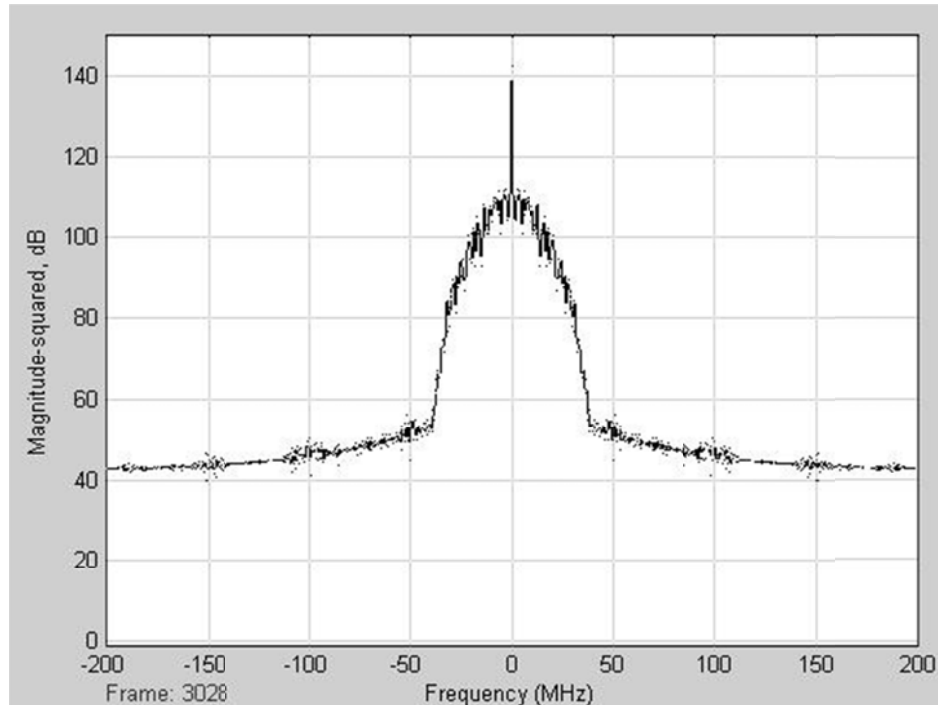


Figure 3.10 Frequency response of the previous 4 SINC filters cascaded together.

3.3.2 Schematic

When implementing the cascaded SINC filter in Cadence using CMOS 90nm technology, the main blocks used are registers and full adders. These are the basic building blocks of the system and are used to design 8 bit versions that are required for the final design. The incoming signal goes through a selected number D of delay blocks and then the outputs of each delay block are summed together. This summing process requires many adder blocks when designed in schematic and layout. When summing two eight bit signals together there is a carry out bit that makes the output nine bits in length. However, the output desired at the end of the system is an eight bit output. In order to satisfy this condition and save space, the connection of bits is designed so that the least significant bit is dropped in order to make sure none of the most significant bits are lost and the system maintains eight bits.

In order to get the calculations to the speed of the 400MHz clock, the 8-bit adder needed to be optimized. The Carry Select Adder is used to divide the time of calculations in half. The first 4-bit adder adds the first four bits with a carry out. The two other 4-bit adders add the four most significant bits. One of these 4-bit adders has a carry in set to 1 and the other has its carry in bit set as 0. The two 4-bit adders go through a 10:5 multiplexer that has its selection bit attached to the carry out of the first 4-bit adder. The result is nearly twice as fast since all of the adders can start instantly and do not have to wait for a carry bit. The design of the Carry Select Adder can be seen in Figure 3.11.

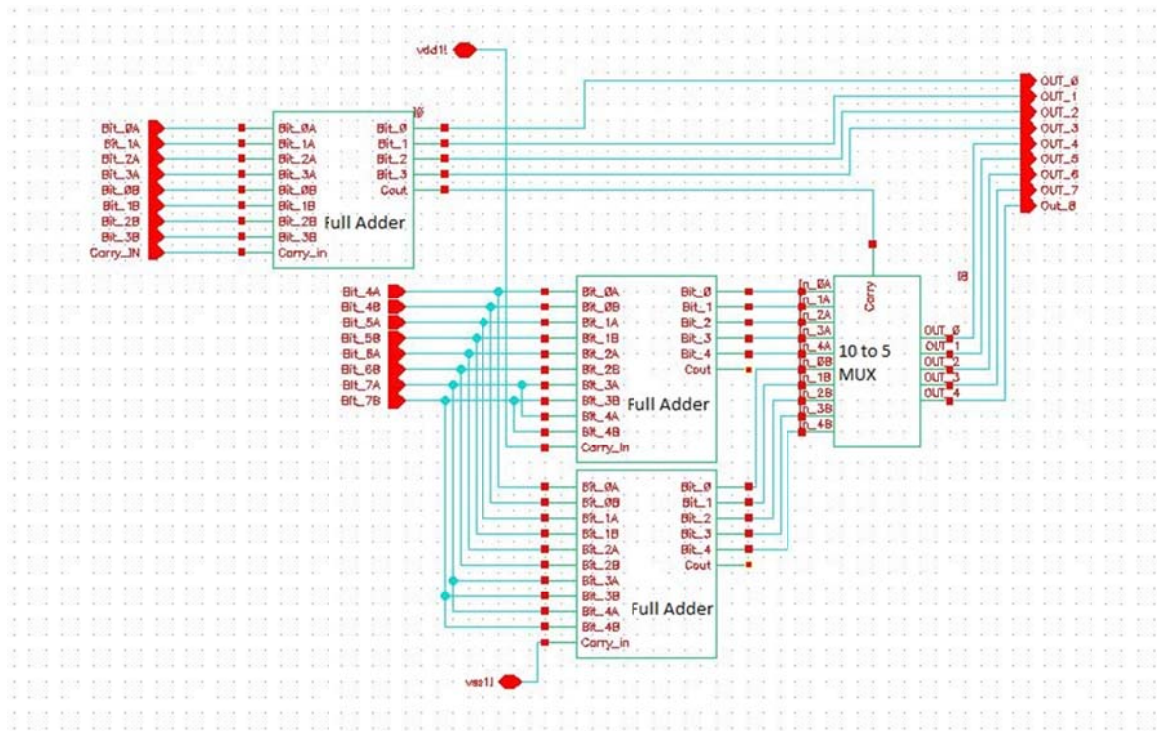


Figure 3.11 Carry Select Adder design

The registers used in the filter design are standard D-flip-flops with two inputs Clock and D, and two outputs q and \bar{q} not. This block was used as the delay for the SINC filters. The registers are also used for pipelining the signal from the adders, since the

system is not fast enough for the signal to propagate through the entire system in one clock cycle. The registers in the design cause an output delay of 46 clock cycles. However, the minimum amount of delay, assuming that the signal took no time to propagate through the adders, would be 32 since the SINC filter requires delays in order to operate. So pipelining the system introduces a delay in the system by 14 clock cycles which is 35ns with the 400MHz clock.

The filter design uses two's complement to represent the signal. Using two's complement instead of standard binary, where all values are positive numbers, allows division or multiplication while keeping the center of the signal constant. If all positive bits are used, there is an arbitrary offset of the signal. This causes a division or multiplication to also divide or multiply the offset of the signal and thus moves the signal. However, when two's complement is used, the signal is centered at zero and a divide or multiply does not move the signal's offset, it only affects the size of the signal. The input bits come in as standard binary and have to be converted to two's complement. In order to do this, the most significant bit is flipped. Table 2 is a three bit example of both binary numbers and two's complement numbers with the associated decimal representation. As can be seen by referencing Table 2, when the MSB of a binary bit is flipped and the number is then represented in two's complement, zero is then moved to the middle of the numbers represented. Since the amount of numbers represented by bits is always even, (2, 4, 8, 16....) zero is actually half a bit higher than the middle of the bits represented. This is not a problem with eight bits since a half bit shift is only 0.2% of the 256 bits represented.

Table 2 Representation of Binary and Two's complement compared by flipping the MSB of the binary bit.

Dec and Bin		Two's and Dec	
7	111	011	3
6	110	010	2
5	101	001	1
4	100	000	0
3	011	111	-1
2	010	110	-2
1	001	101	-3
0	000	100	-4

A clock tree was designed so that the clock does not have a significant load on it. This was done by having an inverter drive four inverters and have the size of the inverters increase throughout the fan out. The inverters were spread out to drive equal loads as well as to have similar distance from the origin of the clock signal in order to maintain a consistent clock signal throughout the design.

Testing the schematic to see the frequency response is very difficult due to the fact that the design uses an 8 bit input. Standard procedures for testing the frequency response in cadence use analog signals. Because of this there is no frequency response plot for the filter design in schematic. Instead the 10MHz frequency that was passed through the DDC is used to test the filter. The design used can be seen in Figure 3.12 which is also the final schematic design of the system shown later in Figure 3.35. This will show the worst case scenario for the DDC and SINC filter combination since the two strongest frequencies that are output from the DDC are 15MHz and 35MHz. The 15MHz is on the edge of the pass band of the filter and the 35MHz is right at the stop band for the filter. The time domain result can be seen in Figure 3.13. A clear sine wave can be seen

in the time domain. The filter does a good job filtering out the 35MHz with a 34 dB difference between the 35MHz and the 15MHz outputs which is very close to the simulation results from Matlab. The Frequency domain results can be seen in Figure 3.14.

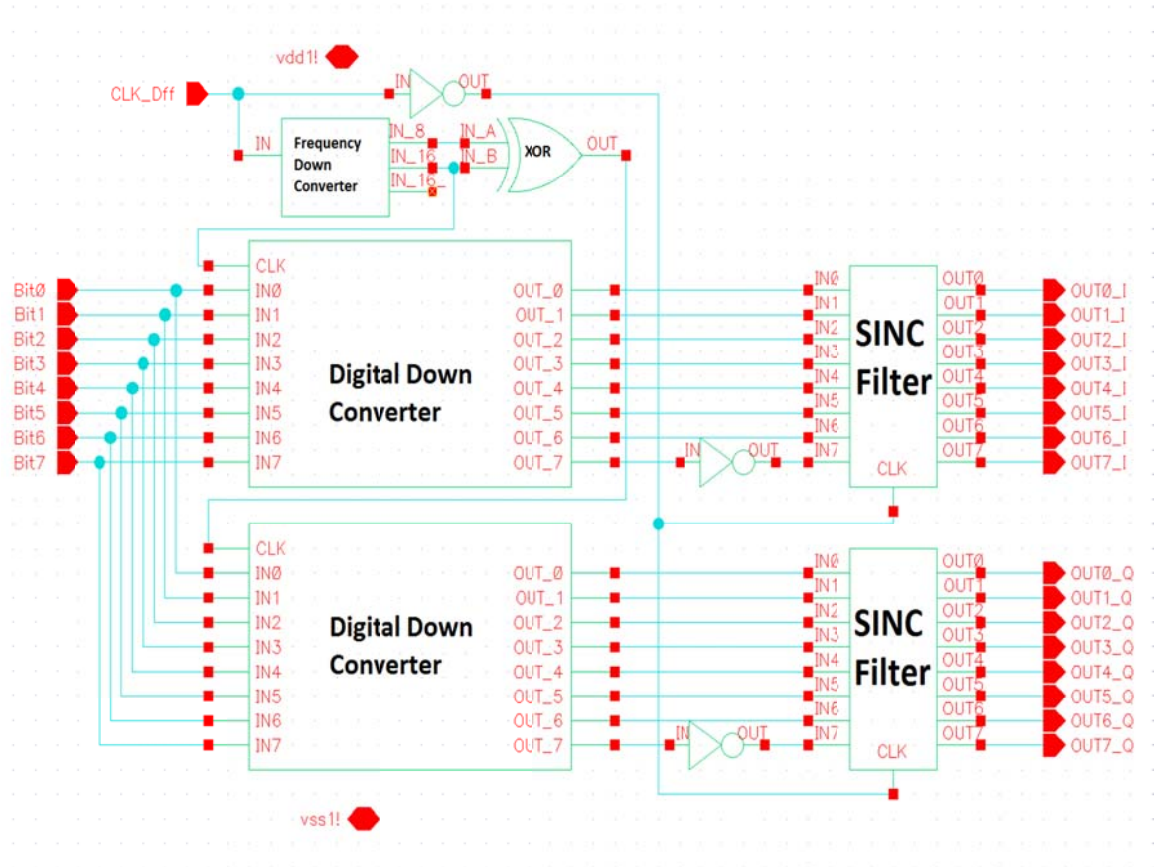


Figure 3.12 Schematic design of the DDC and filter used to demonstrate the filter is working correctly

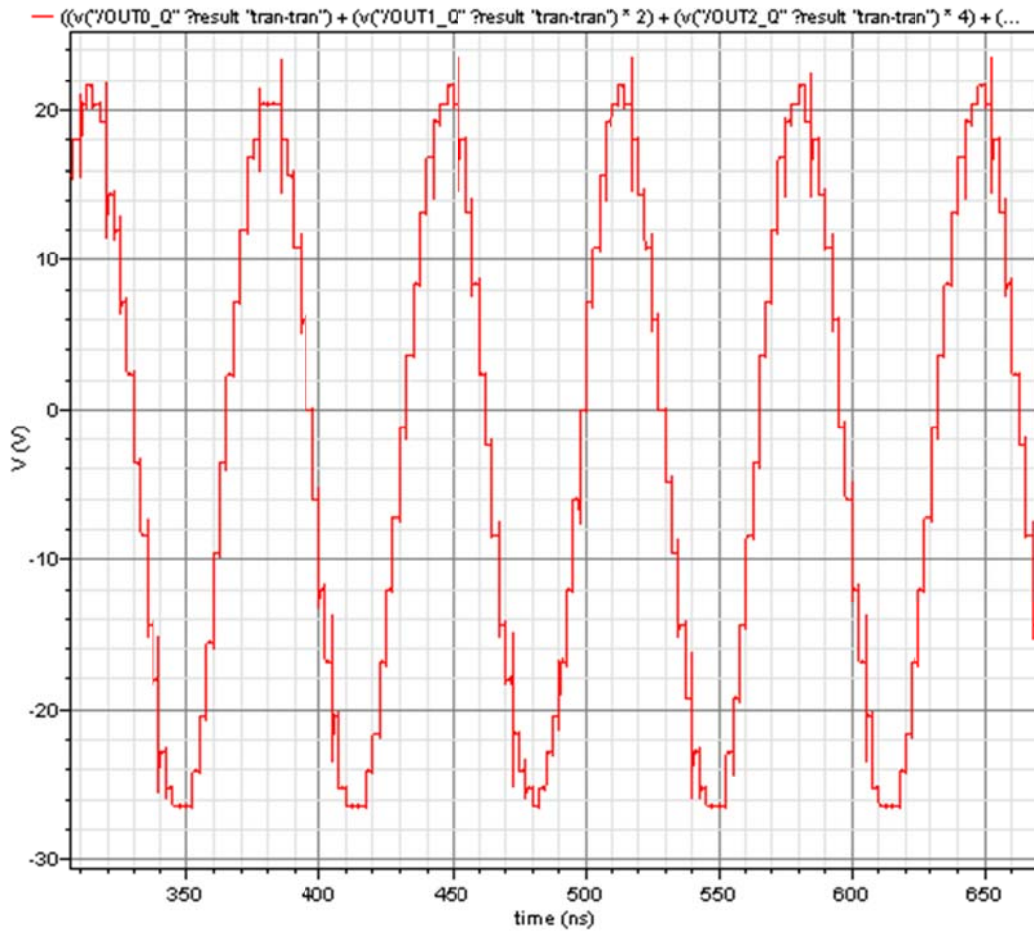


Figure 3.13 Time domain results of a 10MHz input into the DDC and SINC filter schematic design.

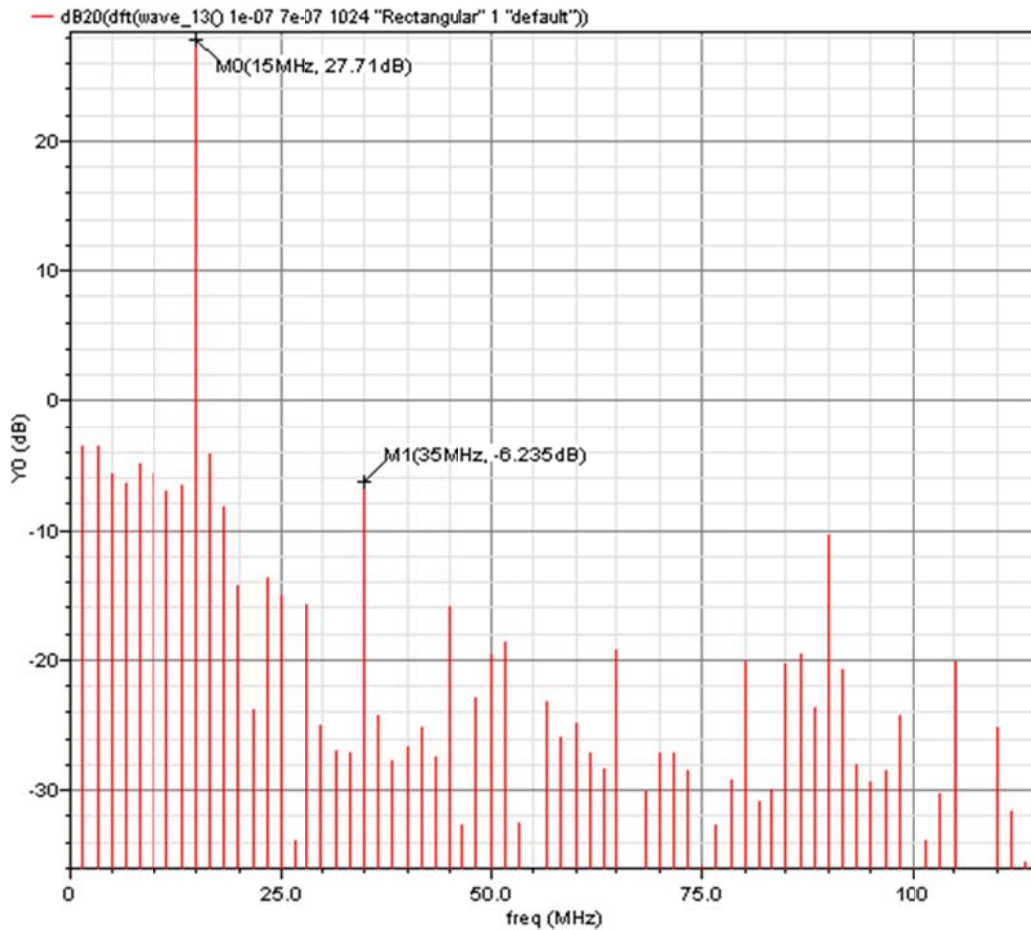


Figure 3.14 Frequency domain results of a 10MHz signal input to the DDC and SINC filter schematic design.

The design also requires both an I and Q signal to be output. The simulation was run using the schematic in Figure 3.12 and the results for this can be seen in Figure 3.15. It is clear from the figure that the Q signal has been shifted by 90 degrees from the original I signal. The shift is caused by the design of the LO which uses the XOR gate to shift the LO by 90 degrees. The figure represents the two outputs, one with the I LO and one with the Q LO.

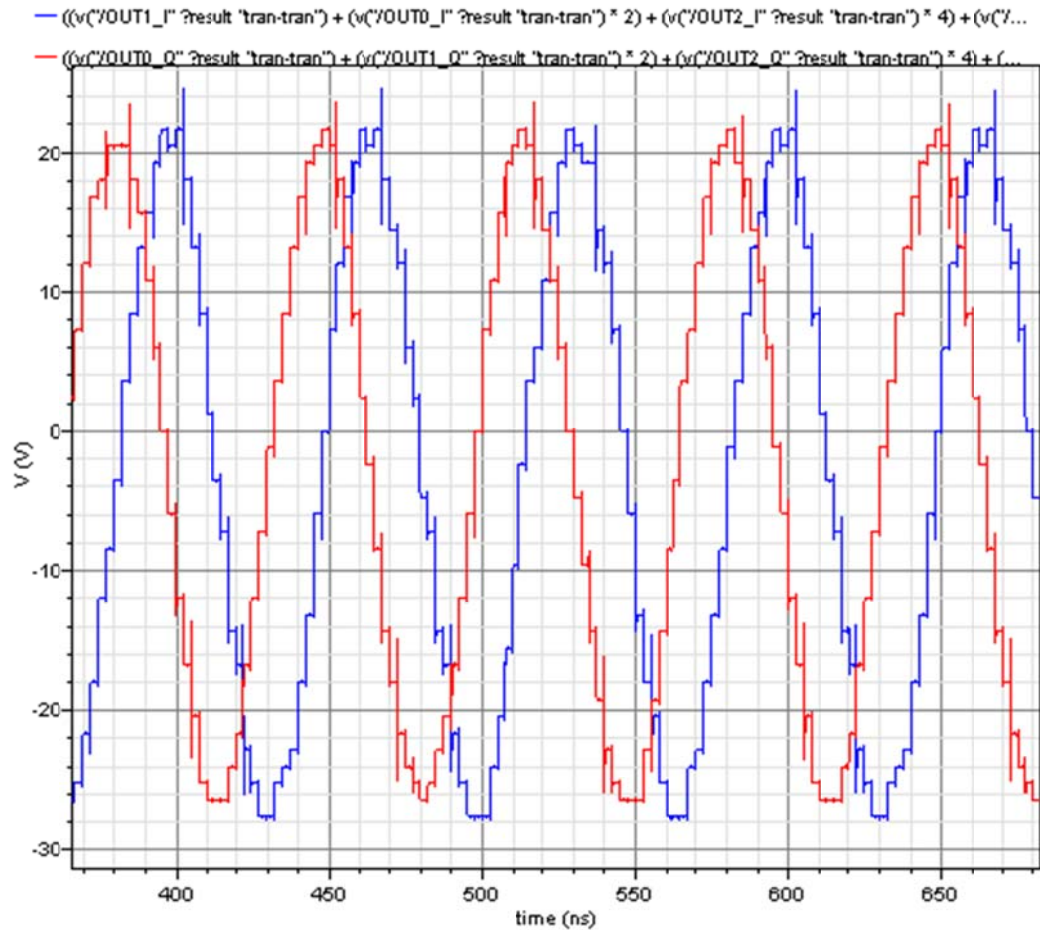


Figure 3.15 I and Q results for an input of 10MHz into the DDC and SINC Filter schematic design.

3.3.3 Physical Layout

The design of the DDC and SINC Filter requires many basic design subcomponents. The three main subcomponents used for the layout and schematic design are registers, full adders, and multiplexers. The floor plan for the layout is defined by finding the height of the largest block and the rest of the layout blocks are sized to match that height in order to make sure that all the blocks fit together well. The height chosen for this design is 5.285um from the top of vdd to the bottom of vss. Once these

subcomponents are designed at the transistor level in schematic, the layout is designed and compared to the schematic to make sure they operate correctly. The schematic and layout blocks are designed at the transistor level and then these blocks are used to design larger blocks in the hierarchy of the DDC and SINC Filter system. Each layout block is designed with the idea of data flowing from left to right.

The register design uses 11 transistors, has the inputs Clock and D, and has outputs Q and Q_. With a clock frequency of 400MHz the design operates using 9.4uW of power. The size of the layout of the register is 5.18um x 7.075um. The Layout and schematic for the register can be seen in Figure 3.16 and Figure 3.17.

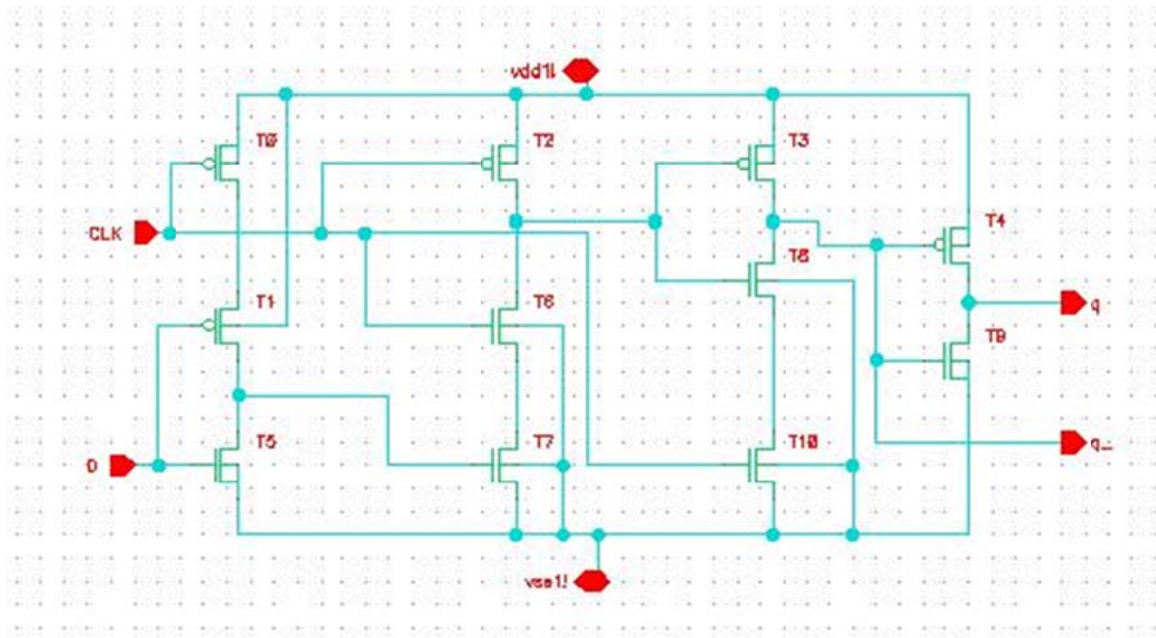


Figure 3.16 Schematic of the register

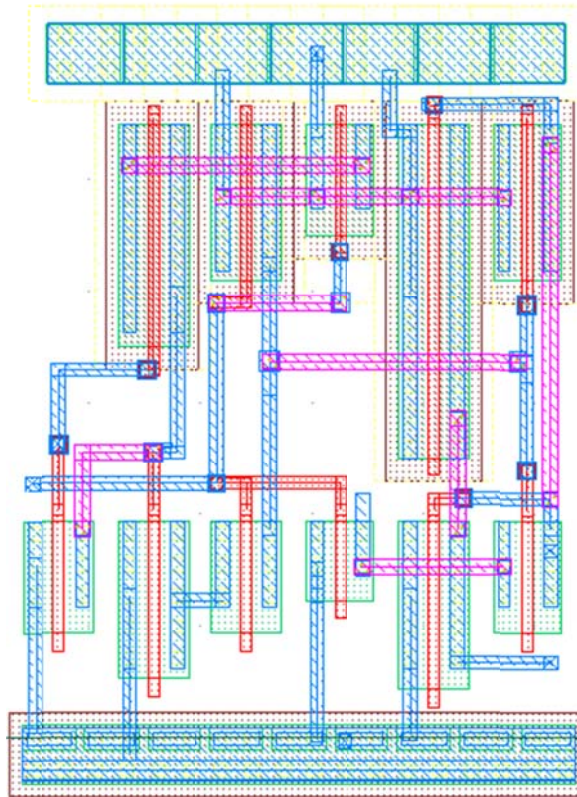


Figure 3.17 Layout of a Register

The design of the full adder uses 16 transistors and has inputs A, B, and C with the outputs sum and co. When inputs are operating at 400MHz the full adder uses 10.77uW of power. The size of the layout of the full adder is 7.075um x 6.400um. The schematic and layout of the full adder is shown in Figure 3.18 and Figure 3.19.

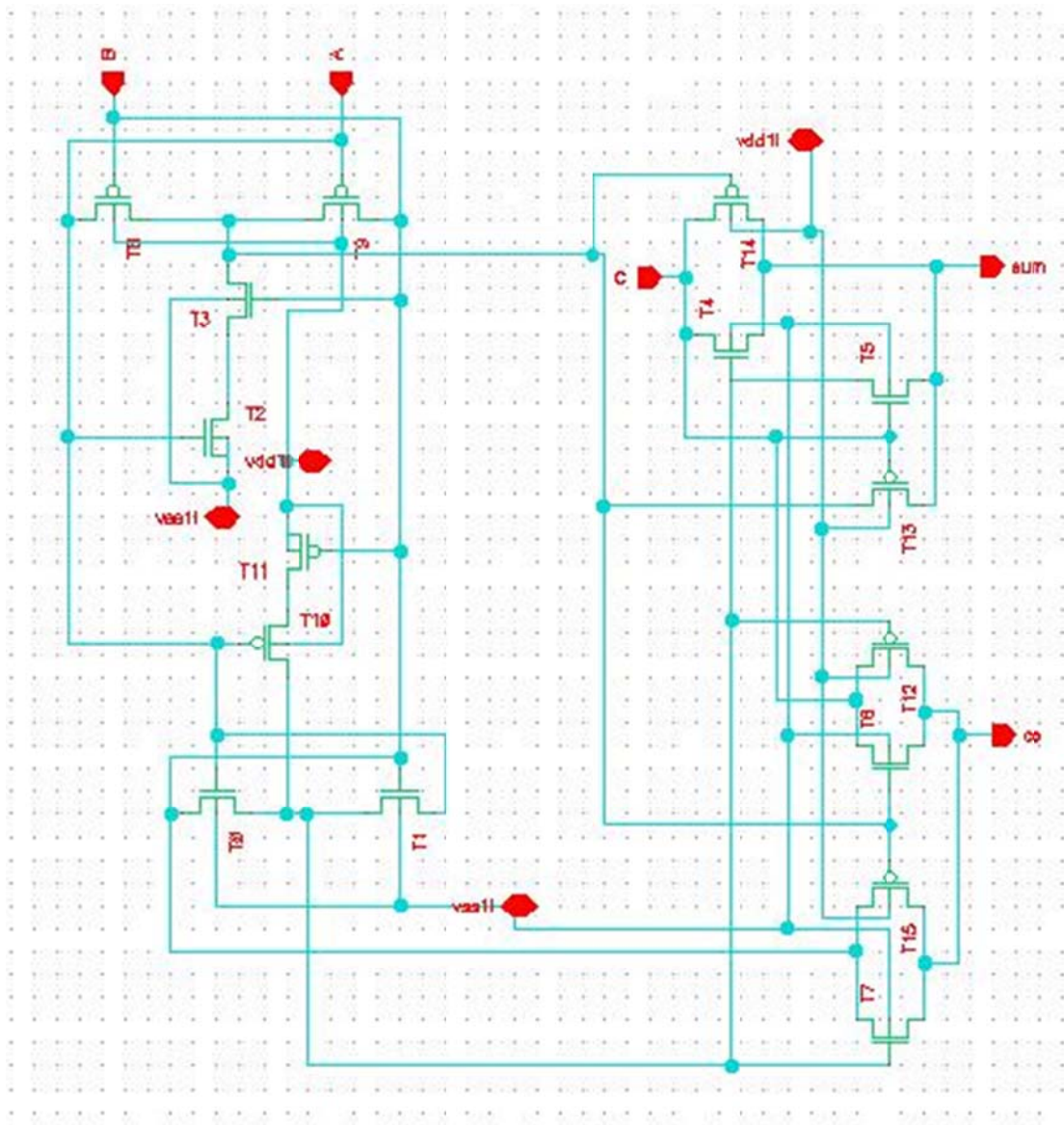


Figure 3.18 Schematic for the Full Adder.

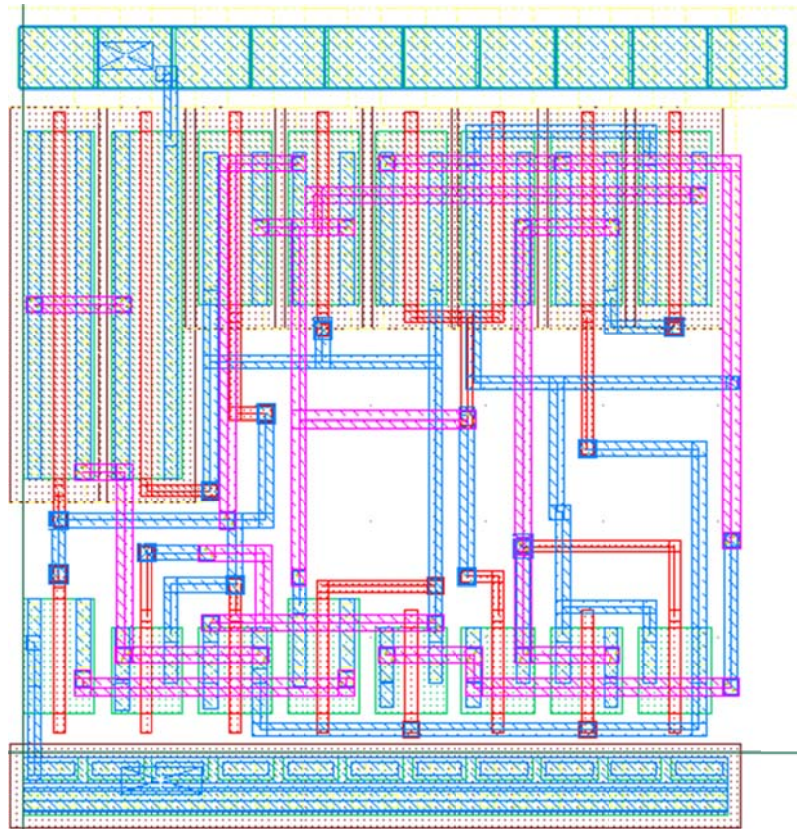


Figure 3.19 Layout of a Full Adder

The 8 to 4 multiplexers and 10 to 5 multiplexers use 2 to 1 multiplexers that are stacked. These multiplexers use 18 and 22 transistors respectively. The 8 to 4 multiplexer has 8 data inputs and a clock input and 4 outputs, while the 10 to 5 multiplexer has 10 data inputs and a clock input with 5 outputs. The inputs are all placed on the left hand side with the outputs on the right hand side for consistent left to right data flow. When the multiplexers are operating at 400MHz, the 8 to 4 multiplexer uses 14.6uW of power and the 10 to 5 multiplexer uses 14.6uW of power. The layout and schematic for the two multiplexers can be seen in Figure 3.20 and Figure 3.21 but they have been resized so that they appear to be the same size, this however is not the case. The 10 to 5 multiplexer is larger than the 8 to 4 multiplexer.

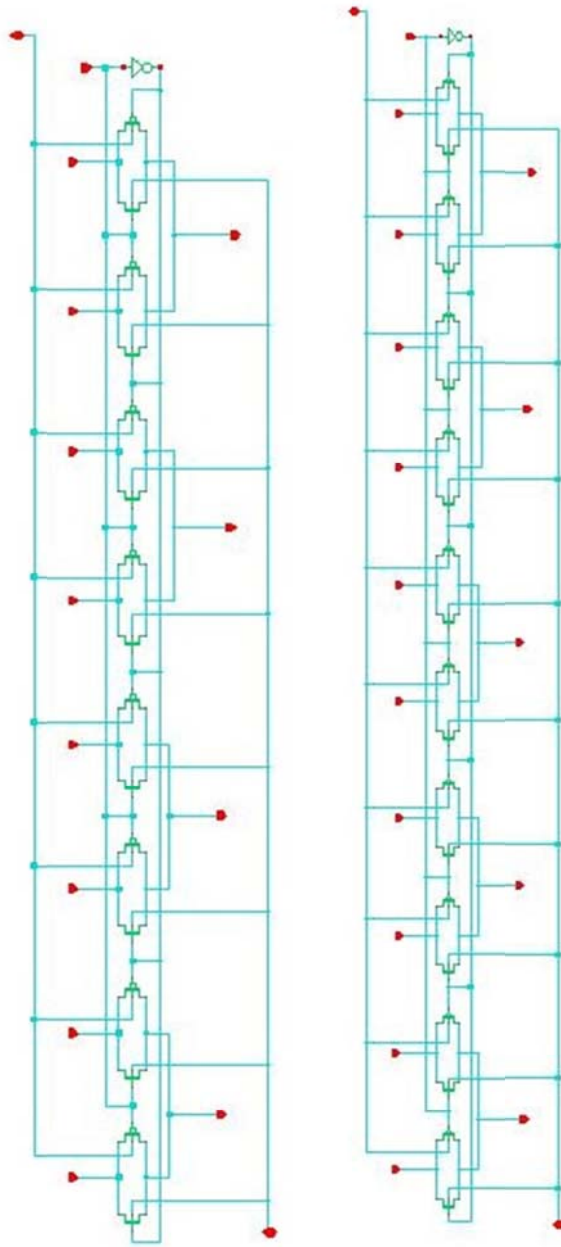


Figure 3.20 Schematic for the 8 to 4 Multiplexer and 10 to 5 Multiplexer

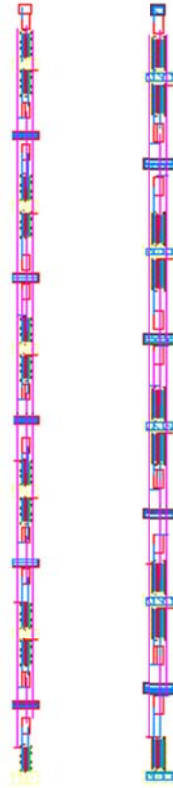


Figure 3.21 10 to 5 Multiplexer and 8 to 4 Multiplexer

The layouts of the register, full adder, and multiplexers are used to design the higher level blocks in layout. The delay blocks, 8-bit register, 4-bit adder, 5-bit adder, and carry select adder blocks are the higher level blocks that are designed. These blocks are designed to operate at 400MHz in a pipelined system.

There are 4 different delay blocks for the SINC Filter design. The different delays that the blocks have are 10, 9, 7, and 6. The delay blocks are created using registers and connecting the output of one register to the input of the next register. Each delay block has the same amount of registers and outputs as it has delays, so the 10 delay block has 10 registers and 10 outputs while the 6 delay block has 6 registers and 10 outputs. However, all the delay blocks have only one input. In order to stay consistent with the left

to right data flow the input is on the left and all of the outputs are on the right. This is done by stacking all of the register blocks vertically. The size of the 10 delay block in layout is 5.18um x 63.77um. The size of the 9 delay block is 5.18um x 57.435um. The size of the 7 delay block is 5.18um x 44.845um. The size of the 6 delay block is 5.18um x 38.59um. The Schematic and layouts of the delay blocks can be seen in Figure 3.22 and Figure 3.23.

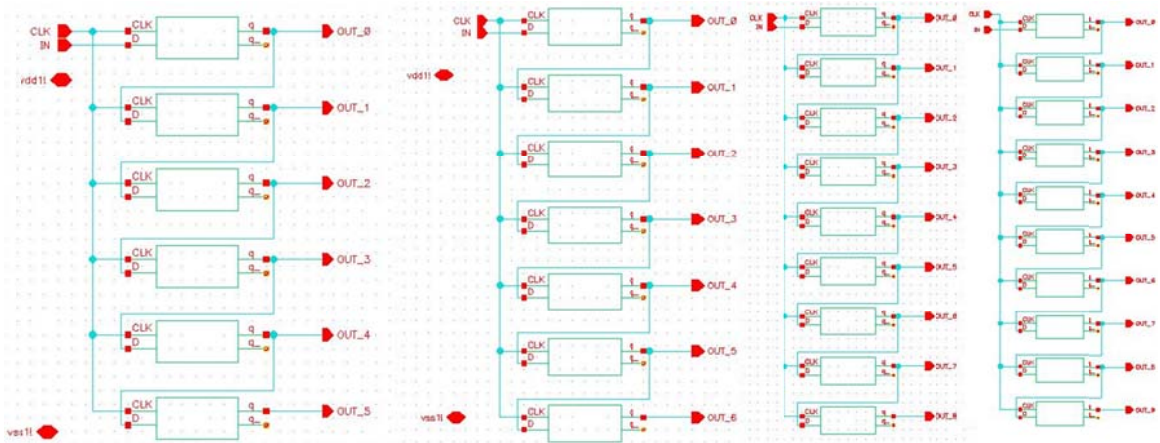


Figure 3.22 Schematic of blocks delay 6, delay 7, delay 9, and delay 10

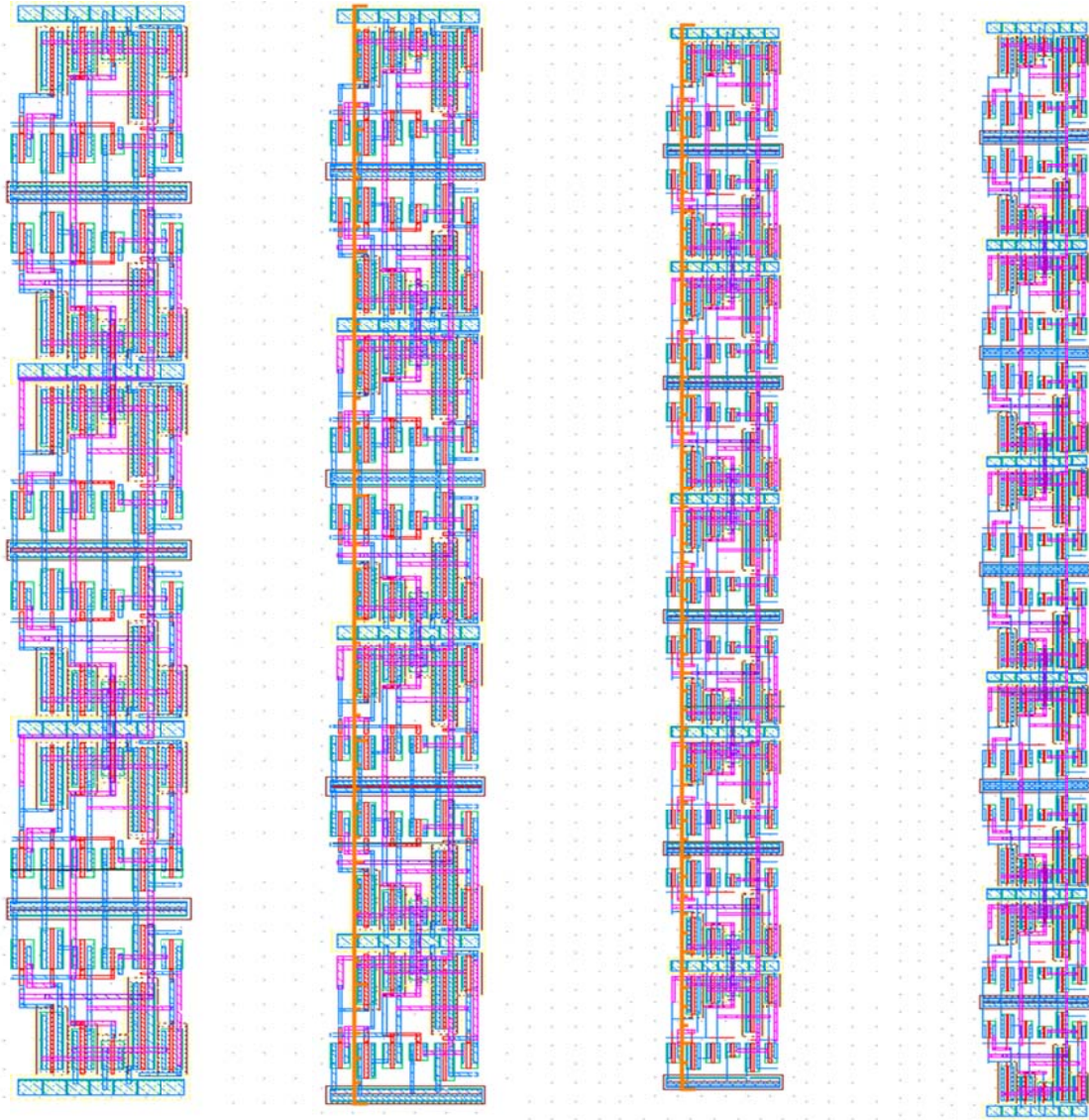


Figure 3.23 The layout of the Delay 6, Delay 7, Delay 9, Delay 10

The 8-bit register is eight registers stacked vertically in order to have a good left to right data flow. Also, all of the clock pins have been connected. The size of the layout for the 8-bit register is 5.18um x 51.18um. The power consumption is 22.4uW. The schematic and layout of the 8-bit register can be seen in Figure 3.24 and Figure 3.25.

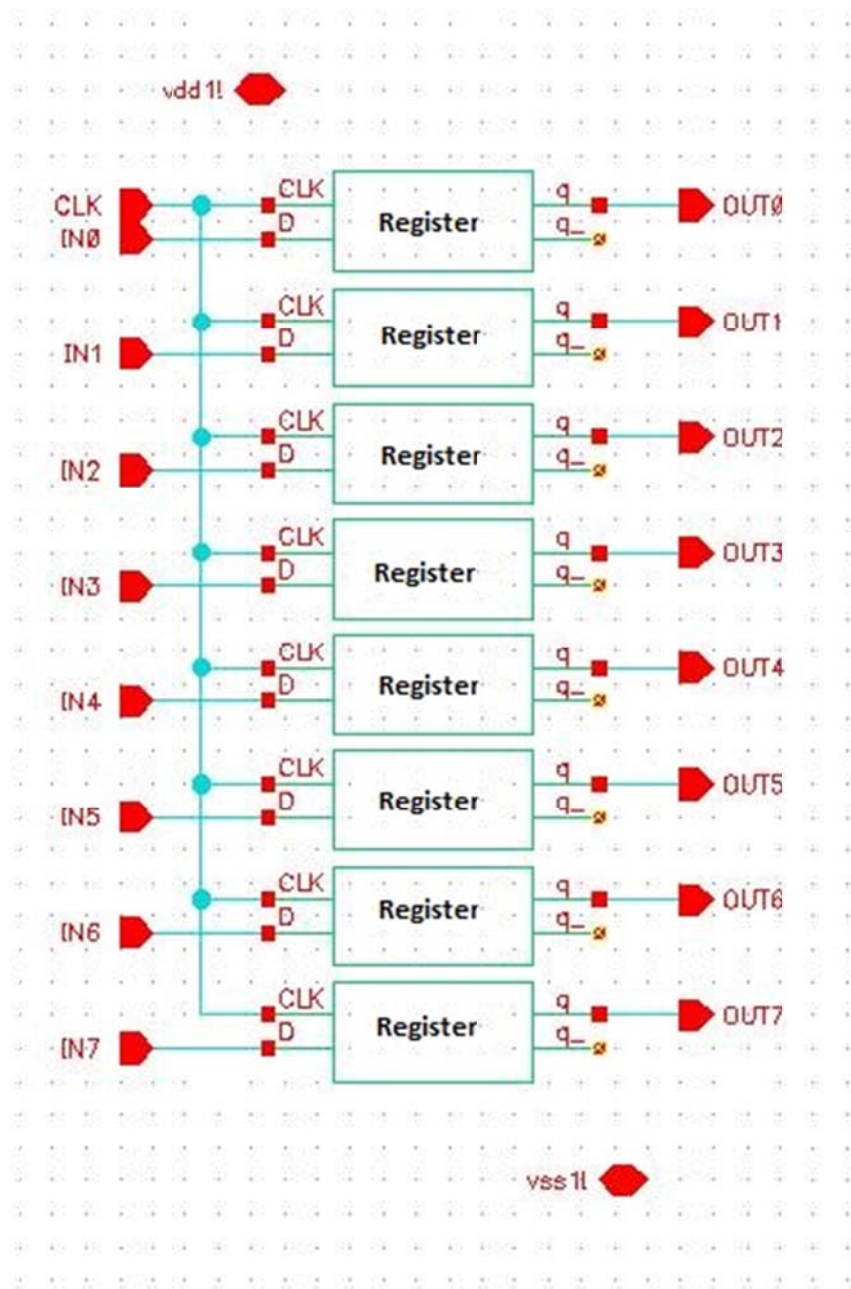


Figure 3.24 Schematic of the 8-bit register.

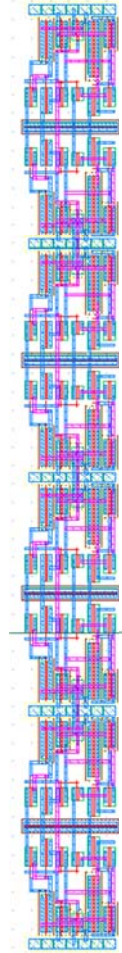


Figure 3.25 The layout for the 8-bit register

The 4-bit adder and 5-bit adder are subcomponents of the carry select adder block. They consist of 4 or 5 full adders that are connected vertically to allow for the input on the left and the output on the right for consistency in the left to right flow of data in the design. The power consumption of these are either 4 or 5 times the consumption of a single full adder, therefore the power of the 4-bit adder is 43.08uW and the power of the 5-bit adder is 53.85uW. The size of the layout for the 4-bit adder is 6.4um x 26um. The size of the 5-bit adder is 6.4um x 32.255um. The schematic and layout designs for the 4-bit adder and 5-bit adder can be seen in Figure 3.26 and Figure 3.27.

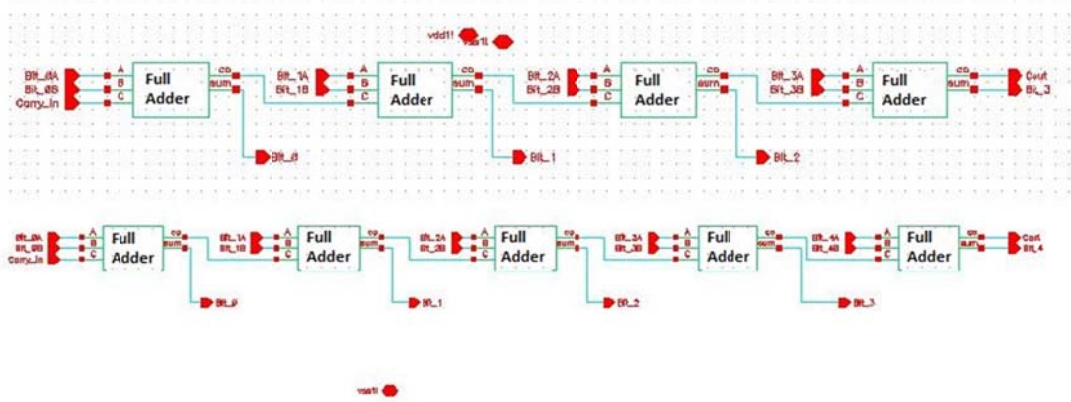


Figure 3.26 4-bit and 5-bit full adders

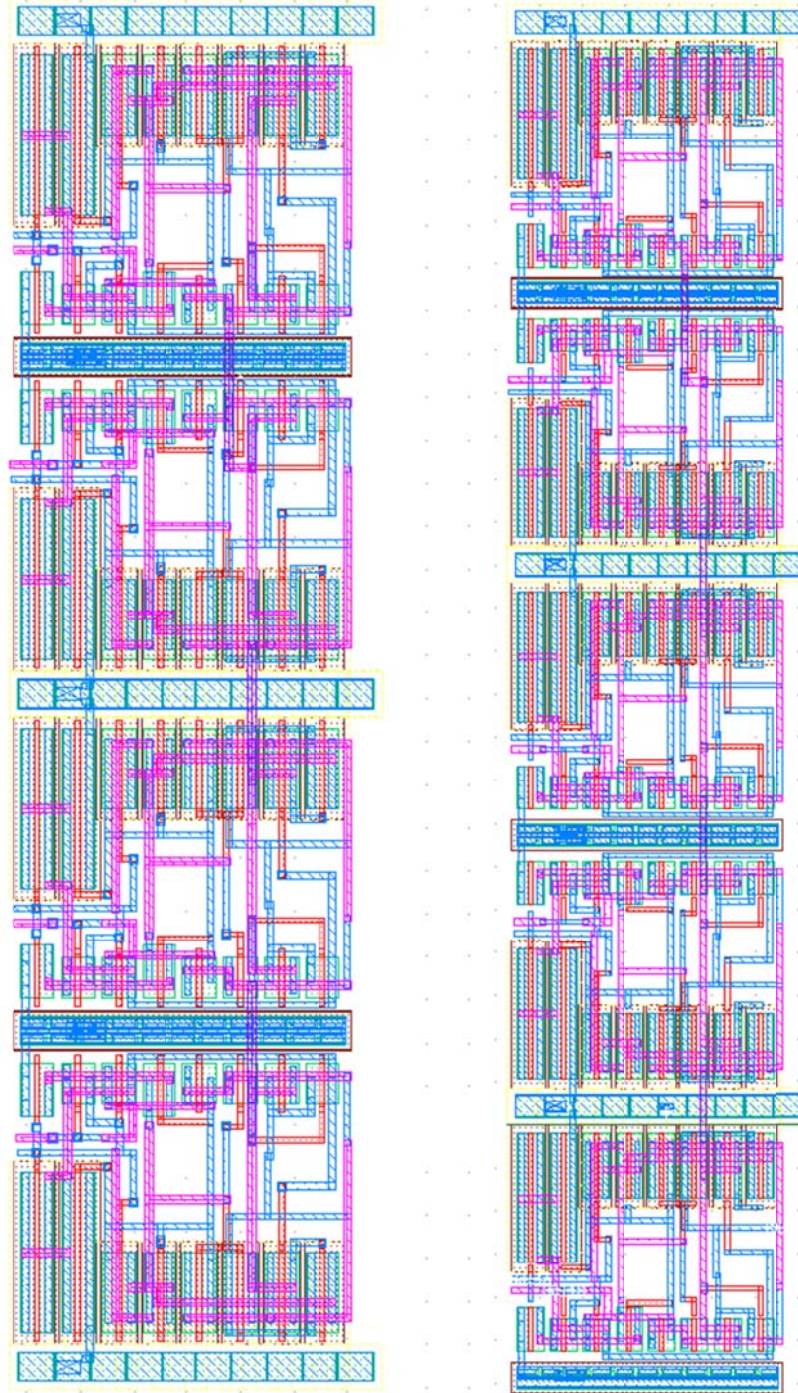


Figure 3.27 Layout of the 4 bit adder and the 5 bit adder

The design of the layout for the carry select adder uses the one 4-bit adder, two 5-bit adders, and one 10 to 5 multiplexer. In order to have left to right data flow and bits increasing from top to bottom, the 4-bit adder is placed on the top of the design, with the two 5-bit adders below and stacked vertically. The 10 to 5 multiplexer is then positioned to the right of the two 5-bit adders in order to continue the left to right data flow. The size of this block is 10.48um x 95.205um. The schematic and layout designs can be seen in Figure 3.28 and Figure 3.29.

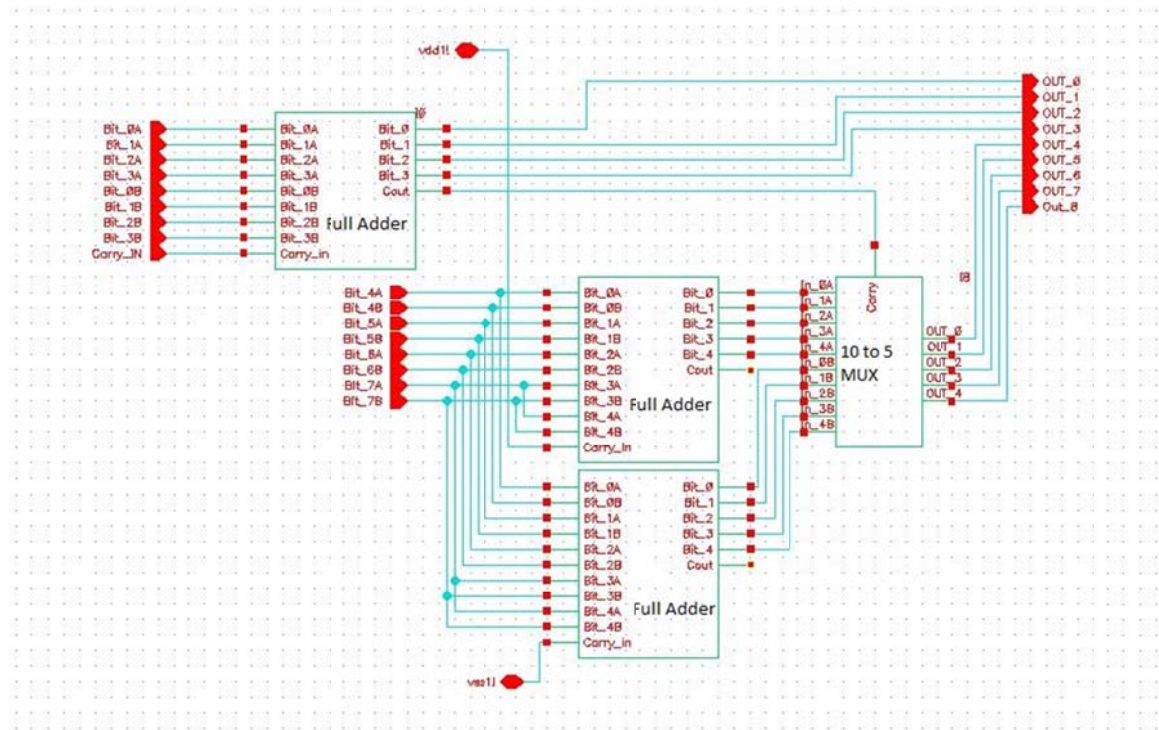


Figure 3.28 Schematic of the Carry Select Adder



Figure 3.29 Layout of the Carry Select Adder

The layouts of each of the four filters are designed similarly. The main idea is to have all the delay blocks on the left, stacked vertically. This allows for the data to easily flow in a left to right direction. The filters with the 10, 9, and 7 delay blocks have two vertical stacks of the delay blocks in order to make the final design not be too tall. The 6 delay blocks are small enough that they can be condensed into one vertical stack. Following the delay blocks, the data flows into the 8 bit carry select adders that are stacked vertically as much as possible, with the 8-bit register blocks set up behind the adders for easy data flow. The final 8-bit register in each of the filter blocks is positioned all the way on the right of the design so that the 8 output bits can easily be connected to the next block in the design. Due to the blocks being designed individually and not perfectly rectangle there are spaces throughout the design. This allows for the clock tree

to be inserted throughout each of the filters. The clock drivers are placed close to the location of the blocks which they need to drive. The size of the 10-delay filter is 82.325um x 296.645um. The size of the 9-delay filter is 65.93um x 296.645um. The size of the 7-delay filter is 54.635um x 296.645um. The size of the 6-delay filter is 52.93um x 302.98um. The schematic and layout of each of the SINC filters can be seen in Figure 3.30 through Figure 3.34. The schematic designs are all individual figures while the layouts have been all placed side by side in one figure. The placement of the blocks in the layout is similar to where they are placed in the schematic design.

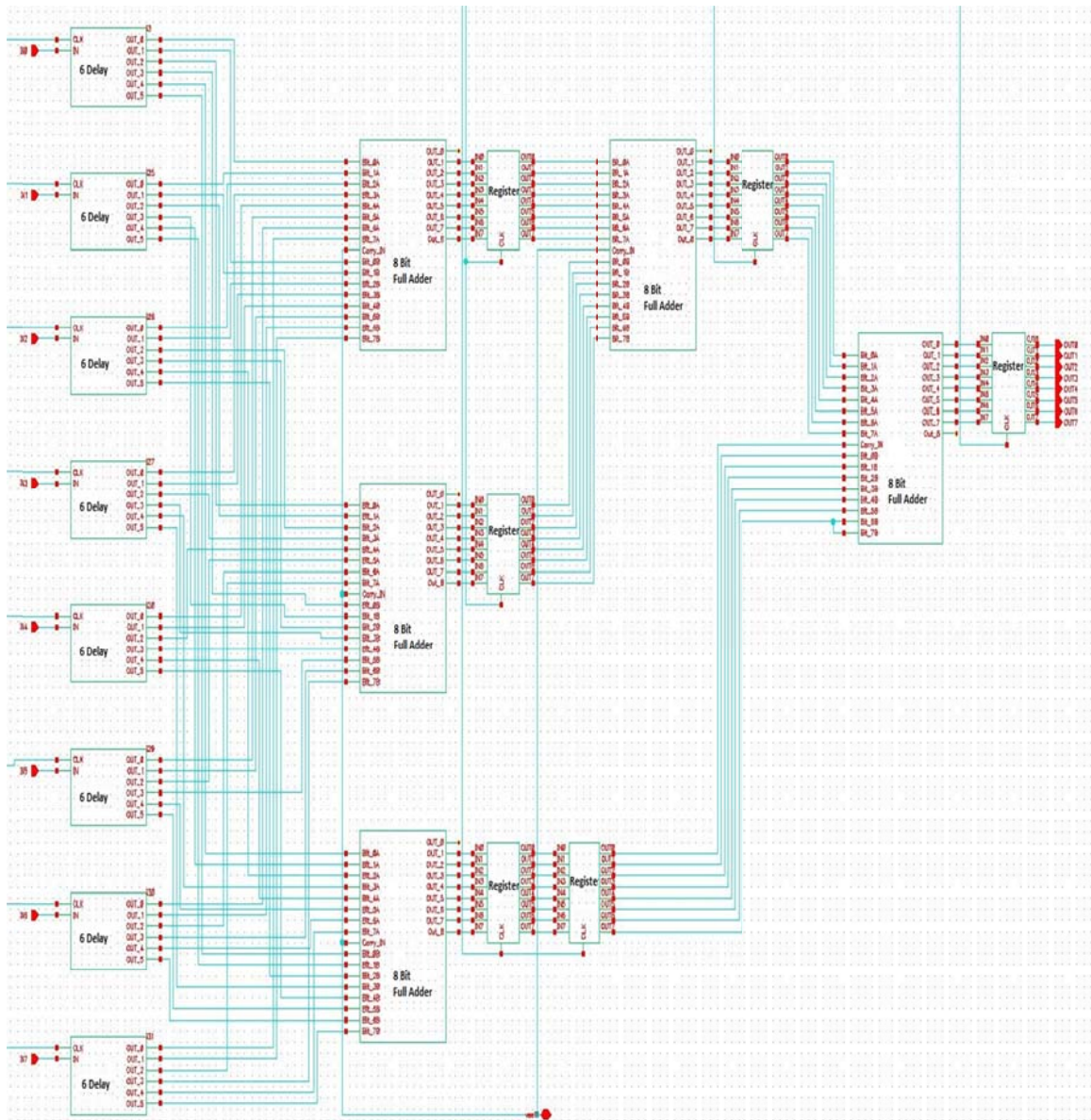


Figure 3.30 Schematic for the 6 delay SINC filter. The eight input bits go into the 6 delay blocks then the bits are summed together.

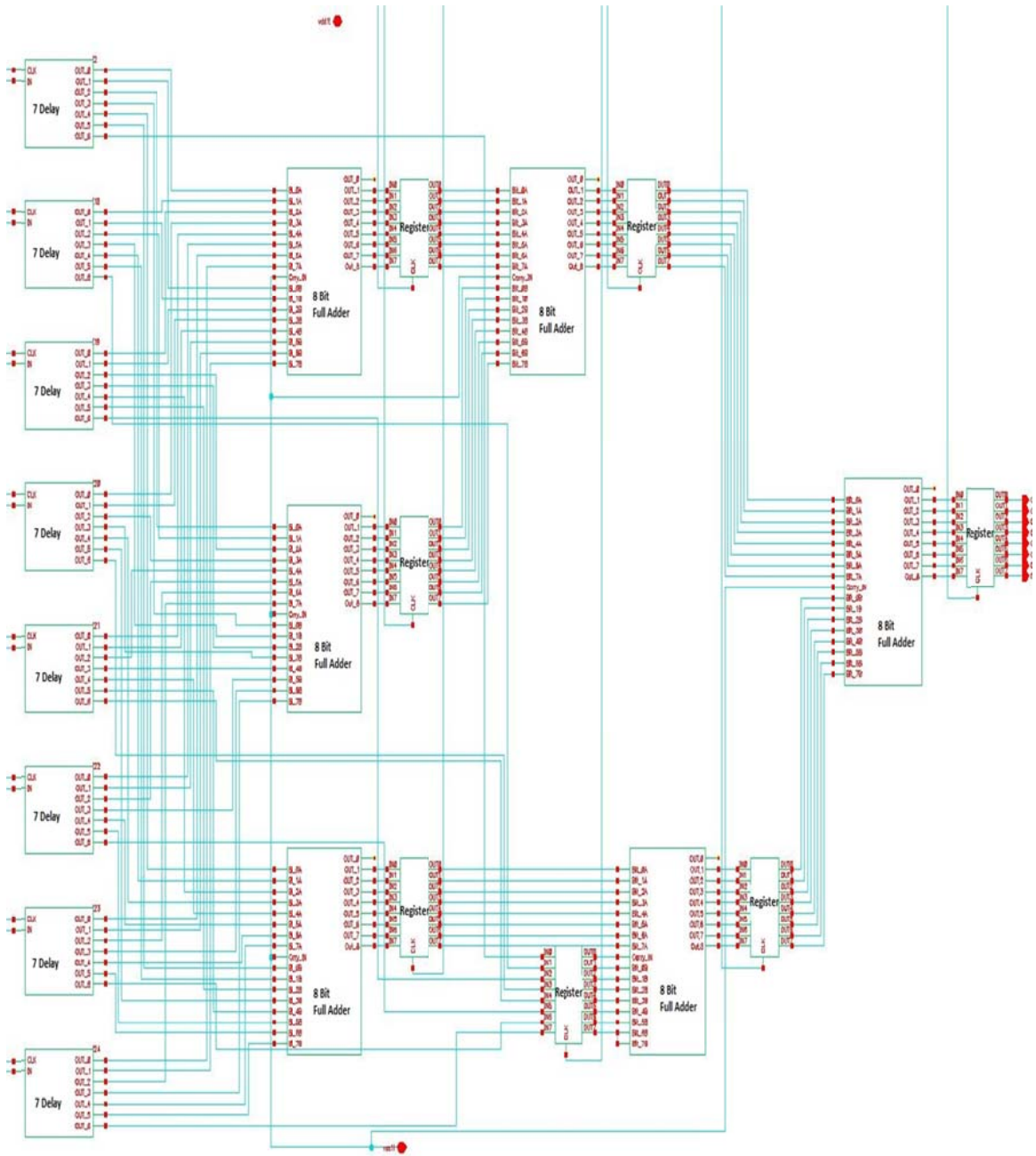


Figure 3.31 Schematic for the 7 delay SINC filter. The eight input bits go into the 7 delay blocks then the bits are summed together.

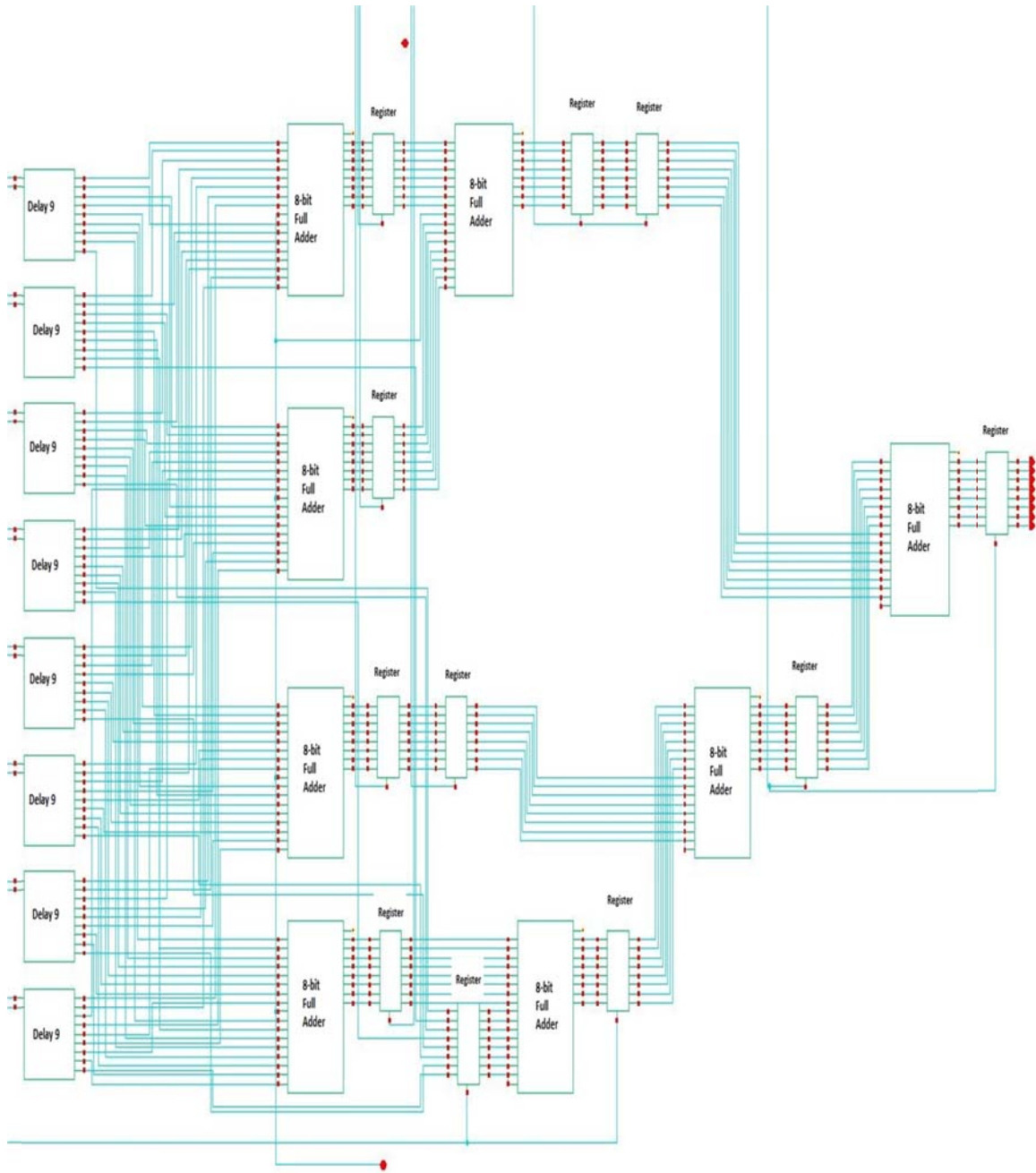


Figure 3.32 Schematic for the 9 delay SINC filter. The eight input bits go into the 9 delay blocks then the bits are summed together.

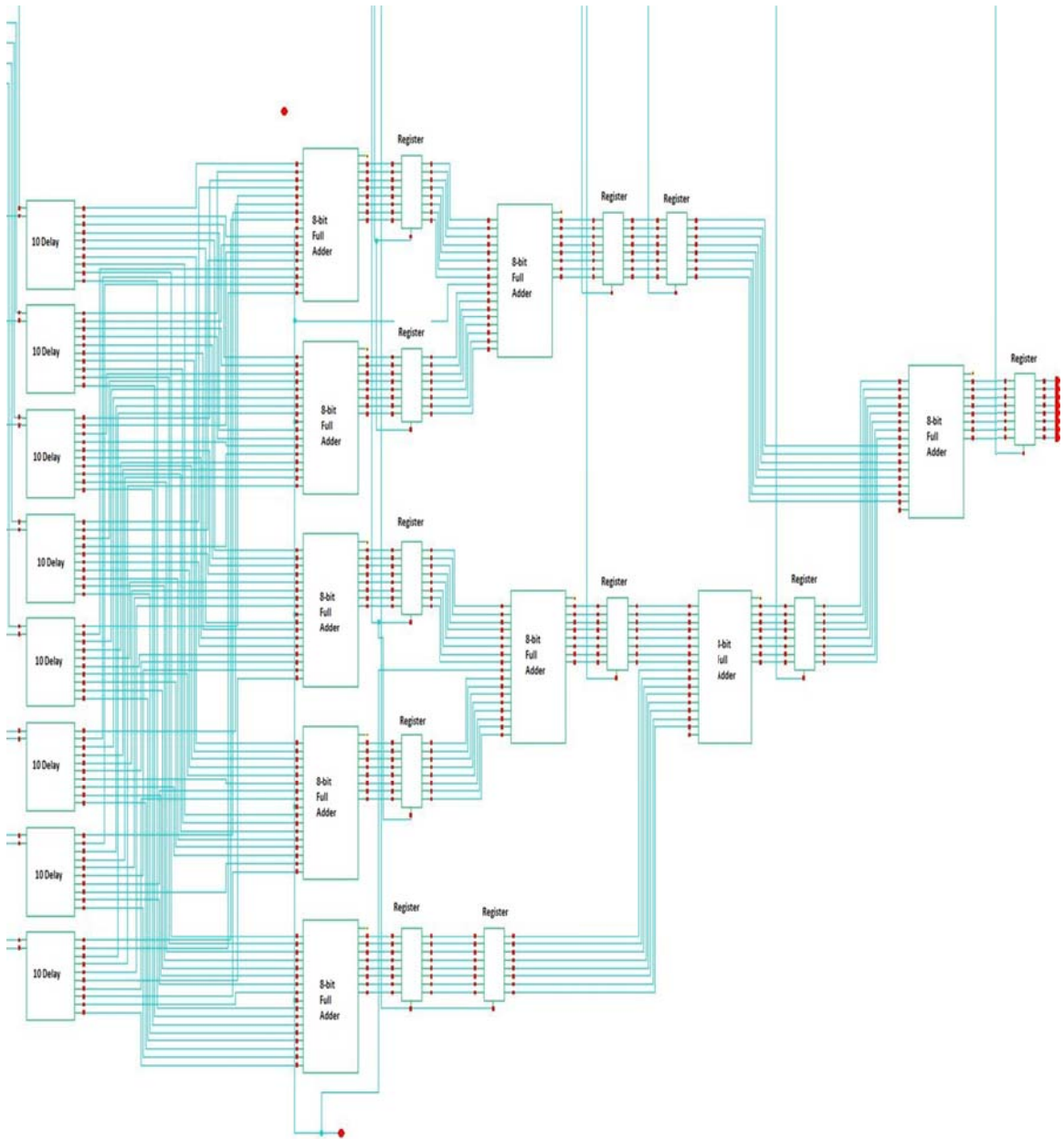


Figure 3.33 Schematic for the 10 delay SINC filter. The eight input bits go into the 10 delay blocks then the bits are summed together.

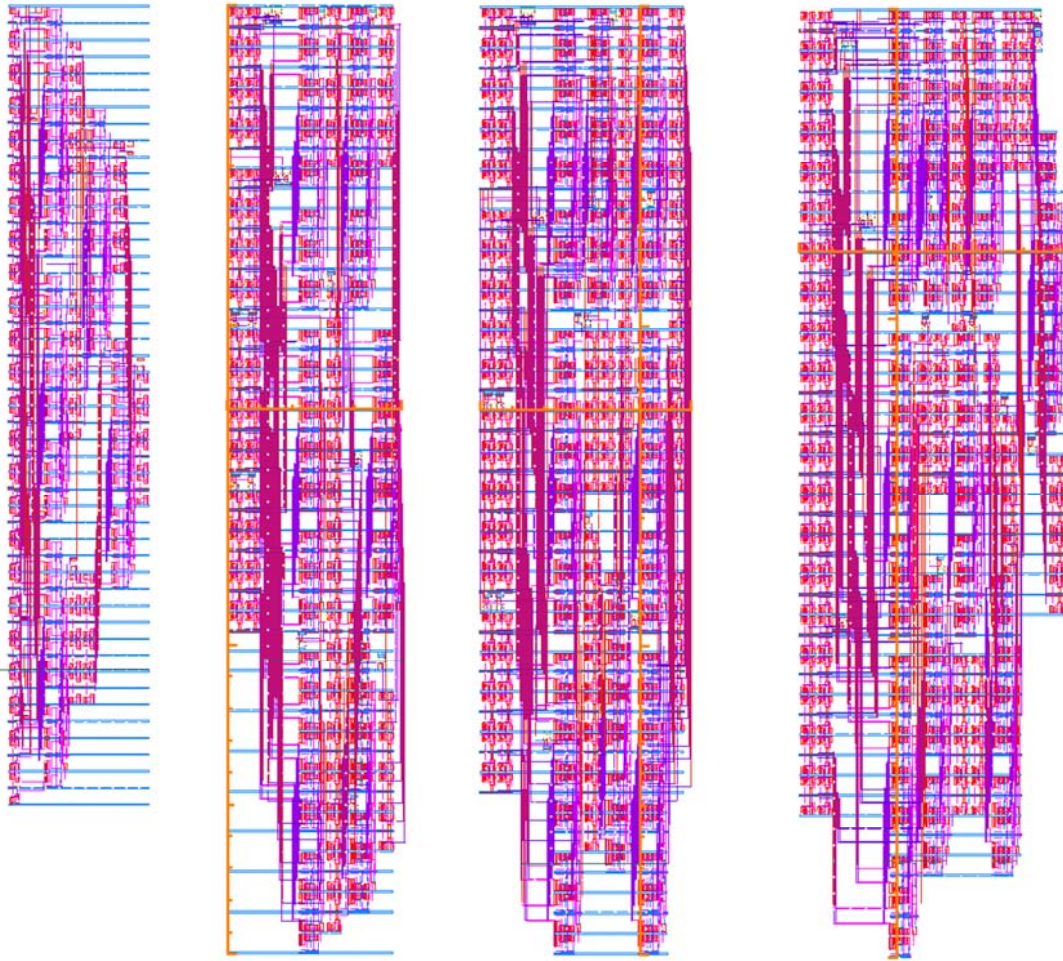


Figure 3.34 Layout of the 6 delay SINC filter, 7 delay SINC filter, 9 delay SINC filter, and 10 delay SINC filter

Next, all four filters are placed together horizontally, preceded by the mixer. This creates either the I or the Q design for the system depending on which frequency divided clock is brought into the mixer. The final design is both the I and Q designed stacked vertically, with 8 inputs connecting to both the I and the Q design. The power design used is an H design where the power and ground are vertical on both sides of the layout and carried into the design through horizontal metals. Placing the power and ground vertically on both the left and the right of the layout allows for current to flow from both the left and the right of the layout in order to reduce the maximum current of the horizontal

metals in half. The power and ground are connected to the multiple power and grounds that are running horizontally through the layout. The final size of the design is 333.485um x 617.6um. The final power dissipation of the I and Q DDC and Filter is 12.54mW. The schematic and the layout for the full design of the DDC and SINC filter can be seen in Figure 3.35 and Figure 3.37. Simulation results of both the layout and schematic version of the DDC and SINC filter can be seen in Figure 3.36 and Figure 3.38. The input to the simulation is a 10MHz sine wave, which as discussed before is the worst case scenario for the system. The results show both the I and Q signals are clear and have a 90 degree phase difference.

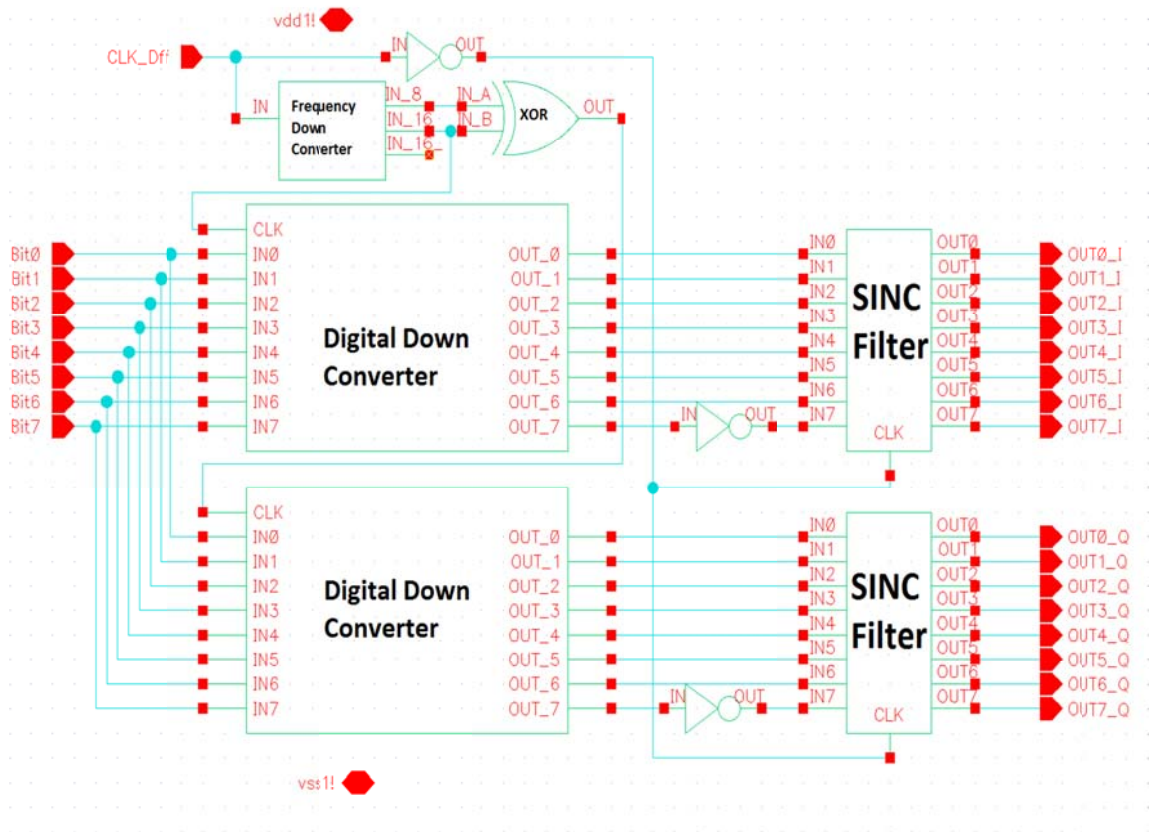


Figure 3.35 Schematic of the Inphase and Quadrature design of the Digital Down Converter and Cascaded SINC Filter

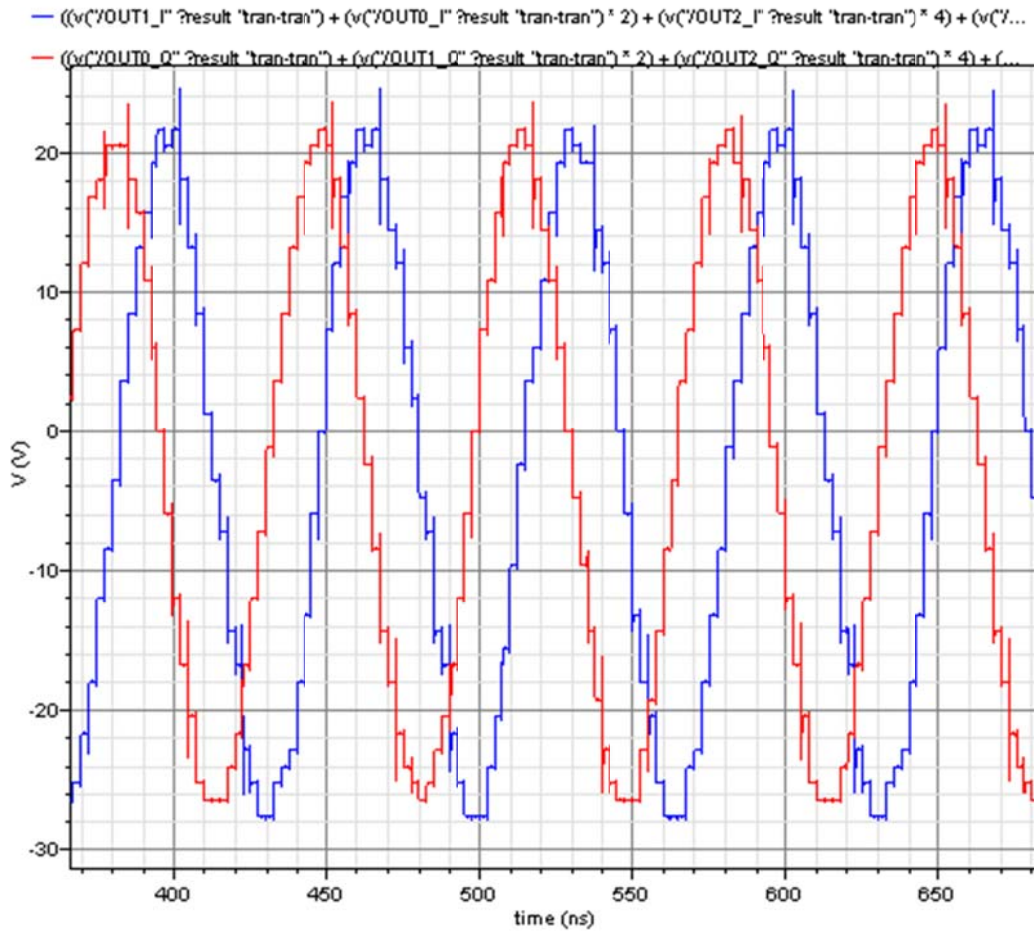


Figure 3.36 Schematic design results of the DDC and SINC filter with a 10MHz input. The results show the I and Q outputs which have a 90 degree phase difference.

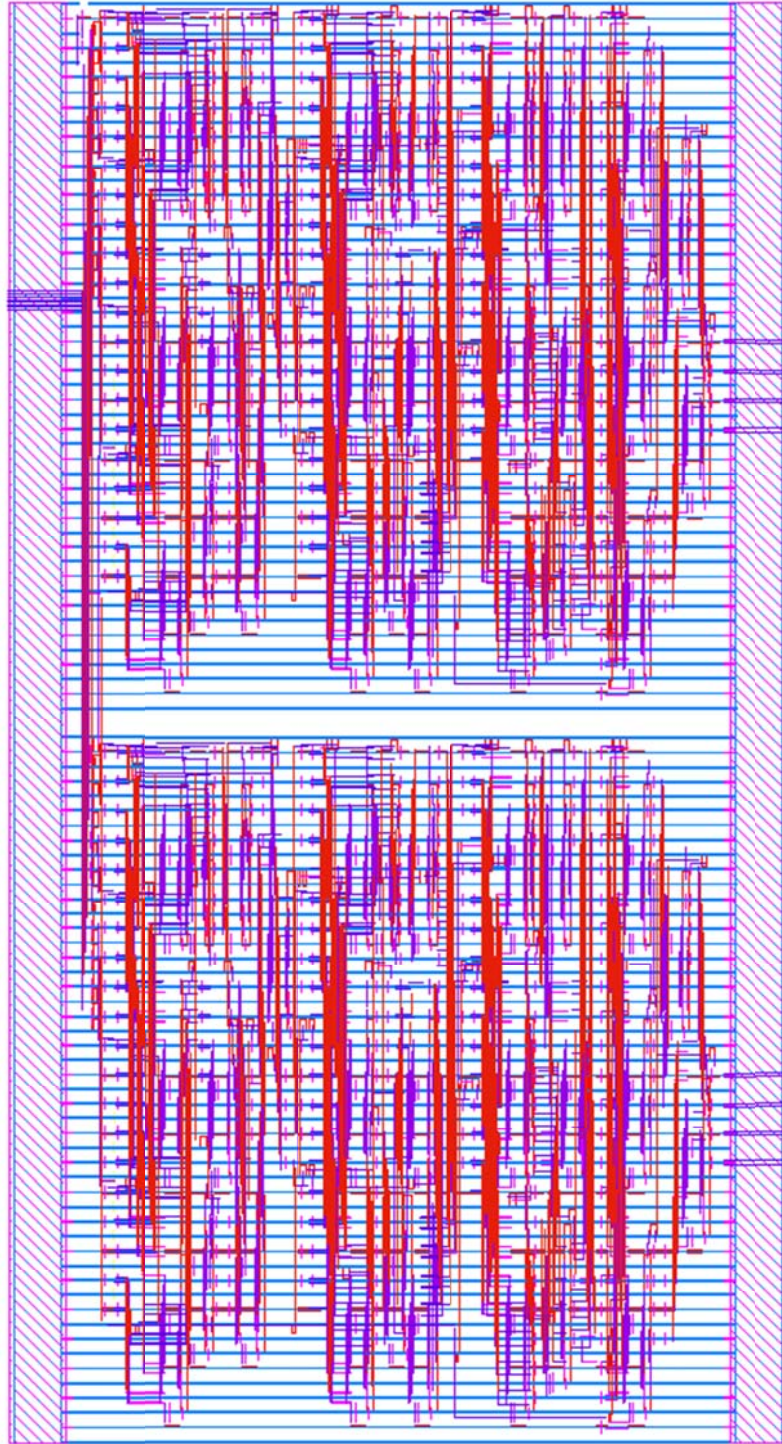


Figure 3.37 Layout of the Inphase and Quadrature design of the Digital Down Converter and Cascaded SINC Filter

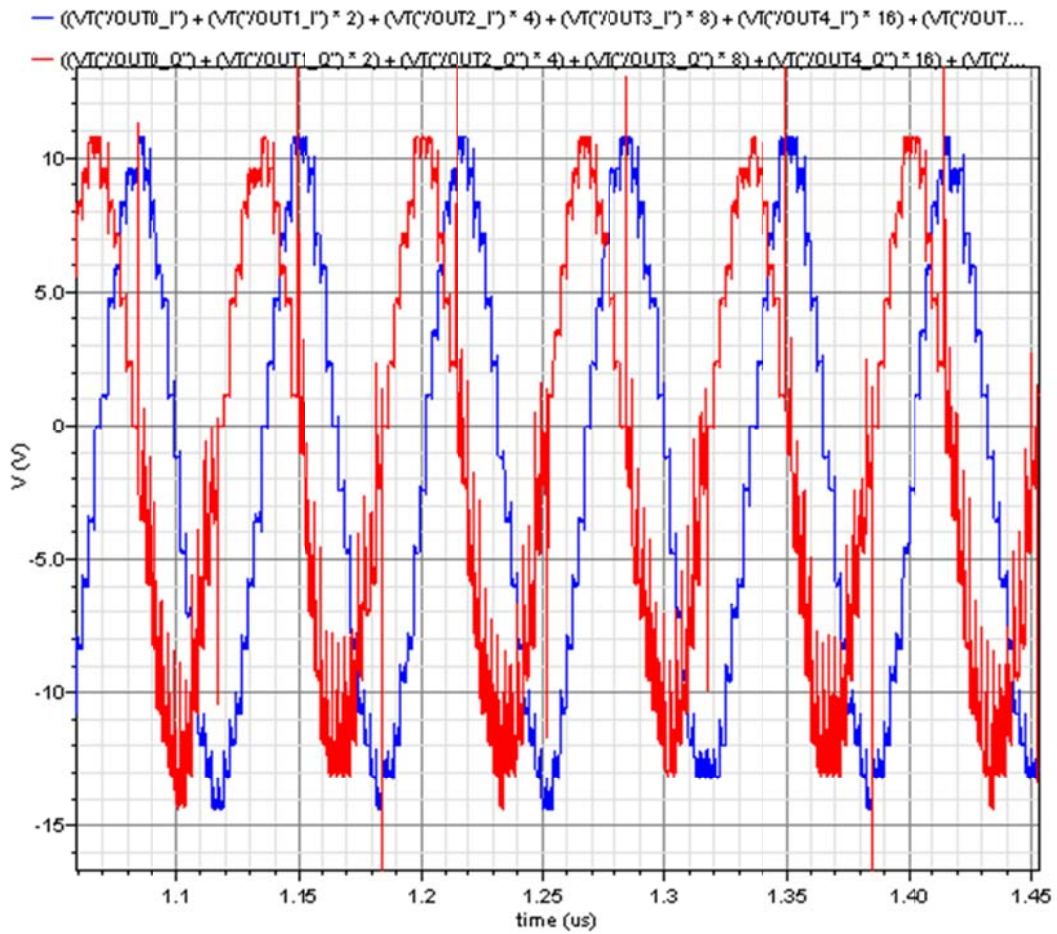


Figure 3.38 Layout design results of the DDC and SINC filter with a 10MHz input. The results show the I and Q outputs which have a 90 degree phase difference.

4 System Analysis

The SINC filter uses fewer adders and delay blocks than other designs such as a FIR filter using coefficients. When using Matlab's filter design tool to create coefficients, the SINC filter discussed in this thesis would require 25 taps if it were a coefficient filter. An FIR filter using coefficients with 25 taps represented by CSD was discussed in the introduction and required 36 adders and 24 delay blocks (registers). The SINC filter designed in this thesis uses 28 adders and 30 registers. Since registers and adders require nearly the same amount of power and area they can be counted as an equal expense and the SINC filter requires two less blocks than the coefficient design. Also, the SINC filter does not have any complex routing compared to large shifts required in filters using coefficients. The ability to have such a low power, small area filter, allows the filter to be implemented on any ASIC chip without having space or heat be an issue is very useful. This design is very specific to its pass band and stop band using the 400MHz sampling frequency. However, the same idea for the design can be easily implemented for other filter specifications.

Most filters are designed to have the pass band only down 3dB and the stop band down closer to 60dB. One of the reasons that this filter does not have ideal pass band or stop band results is because the original design was for an input with a 24MHz bandwidth instead of a 30MHz bandwidth. With these specifications the filter performs optimally and has a 3dB pass band and a 60dB stop band when simulated in Matlab. If the filter in this thesis was redesigned specifically for the current specifications required, there would

probably be a different number of stages and each stage would have different values in order to have the stop band and pass band be more ideal.

The schematic frequency response for the filter gives a dynamic range of 34dB while the ideal case shown in the Matlab design shows a dynamic range of 39dB. The change in dynamic range can be attributed to two things. The simulation in Matlab uses an ideal sine wave to represent the IF signal. The actual implementation in Cadence uses an 8-bit wave. The other reason there is a difference in the dynamic range is because of the truncation of the LSB throughout the filter implementation. The value is not being represented as a bit value in Matlab so it does not need to truncate any values when adding to keep an 8-bit system throughout the design. The combination of these two differences between the Matlab and Cadence design account for the difference in the dynamic range of the signals.

5 Conclusion

In any modern RF receiver chain, a DDC and digital low pass filter are necessary. Designing these systems to be low powered and low area is important in advancing technology. The DDC design described in this thesis uses a square wave as the LO in order to minimize power and area. Using a square wave in the design also gives the advantage of easily producing an I and Q signal by delaying the square wave by 90 degrees. The characteristic of a DDC produce high frequency outputs that need to be filtered out. This means a low pass filter is required. Low pass filters commonly use multipliers which are a very expensive. The design of the SINC filter in this thesis is based off of a CIC filter is multiplier-less. The cascaded SINC filter uses only adders and registers and is specifically designed so that each stage of the filter compliments the other stages. The combination of both the DDC and SINC filter is used to take the digital IF signal from the ADC and produce two baseband signals, I and Q.

The design and implementation of the efficient DDC and SINC filter discussed in this thesis consumes very low power, 12.54mW at 400MHz and has a total area of 333.485um x 617.6um. The combination of these two convert the IF signal to a baseband signal and stop any higher frequencies from being output. The layout of the design is small and can be easily implemented behind an ADC in an RF receiver chain. The ability to have such a low power and small area DDC and filter design allows for an ASIC to contain a significant portion of the RF receiver chain all on one chip.

The DDC is extremely small 3.735um x 118.745um. The implementation is also very dynamic, since the design can use any frequency up to the sampling frequency of the system as its local oscillator. The square wave design does not inhibit the application at

all since all of the harmonics that come from the square wave are located outside of the stop band of the filter. Also, the square wave design makes the I and Q signals very easy to generate.

The design of both the DDC and SINC filter is not only limited to ASIC implementations but also can be implemented both in FPGAs and in software designs as well. The low power and small area implementation of the DDC and SINC filter is very useful as it is an important component in any RF receiver chain.

6 Future Work

The SINC filter designed in this thesis is very specific to the requirements needed in the design. An algorithm could be designed to calculate what specific values and what order of filter are needed to match the requirements for a different system. This algorithm would be able to take in pass band, stop band, and sample frequency in order to calculate the filter values needed for the design.

A compensation filter could be designed to raise the pass band to the standard 3dB instead of the 6dB that the current filter has.

The entire design has been implemented in layout using CMOS 90nm technology and fabricated. However, since the DDC and filter design is part of a larger system the DDC and filter responses can not be tested directly. Future work could include fabricating a chip that only contains the DDC and filter on it in order to be able to test the design.

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