8-1-2008

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(Received 12 May 2008; accepted 25 July 2008; published online 29 August 2008)

Low defect AlN/GaN high electron mobility transistor (HEMT) structures, with very high values of electron mobility (>1800 $cm^2/V\,s$) and sheet charge density ($>3\times10^{13}$ cm^{-2}), were grown by rf plasma-assisted molecular beam epitaxy (MBE) on sapphire and SiC, resulting in sheet resistivity values down to ~100 $\Omega/\square$ at room temperature. Fabricated 1.2 μm gate devices showed excellent current-voltage characteristics, including a zero gate saturation current density of ~1.3 A/mm and a peak transconductance of ~260 mS/mm. Here, an all MBE growth of optimized AlN/GaN HEMT structures plus the results of thin-film characterizations and device measurements are presented. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2970991]

High electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures have been extensively studied for their potential application in high power, high frequency, and high temperature amplifiers.[1] However, as the device dimensions are being reduced, a number of issues including rf current collapse, leakage currents, and short channel effects have severely hindered the progress.[2] Variations in the basic structure, including indium-containing HEMTs such as AlGaN/InGaN/GaN (Ref. 3) and AlInN/GaN,[4] have also been investigated in response to theoretical predictions of higher performance devices.[5,6] Recently, the insertion of a thin (~1 ML) film of AlN in the HEMT structure has been shown to improve the device performance by increasing the two dimensional electron gas (2DEG) confinement and reducing alloy scattering.[7–9] However, much less work has been done on AlN/GaN heterostructure for HEMT devices mainly due to the difficulty in growing high-quality AlN barrier layers on GaN by either metal organic chemical vapor deposition[10] (MOCVD) or molecular beam epitaxy (MBE).[11–13] Nonetheless, the expected reduction in short channel effects and lower threshold voltages, using ultrathin AlN barrier layers, makes these structures of great interest for very high frequency and high power applications.

Previous attempts to grow AlN/GaN HEMTs directly on sapphire substrates have produced structures with limited room-temperature (RT) 2DEG mobility ($\mu_{RT}<500$ $cm^2/V\,s$), which resulted in high values of sheet resistance, ρ_s, in spite of very large 2DEG densities ($n_s>2\times10^{13}$ cm^{-2}).[10,12] To date, the best ρ_s values for AlN/GaN HEMTs have been demonstrated by rf plasma-assisted MBE on thick MOCVD grown templates that contain a low density of threading dislocations (TDs).[11,13] Based on these results, it may be concluded that the quality of the 2DEG, generated by strong polarization fields at the AlN/GaN interface, can be severely degraded by a number of factors including a high density of TDs, interface roughness, and/or cracking of the highly strained AlN layer. On one hand, for high-quality AlN/GaN HEMTs the AlN barrier should be thick enough to provide both a high density of carriers and good confinement of 2DEG. On the other hand, the critical thickness for dislocation formation in the AlN barrier layer, with about 2.4% lattice mismatch on GaN, can be as small as 3 nm depending on growth conditions and interface quality.[14,15] In this work we demonstrate that AlN/GaN HEMT structures, directly grown on sapphire and SiC under optimized conditions, can show both very high values of μ_{RT} and n_s, resulting in record low values of ρ_s in III-nitride HEMTs. We will also present the results of dc and pulsed device characterization on these structures.

AlN/GaN HEMT structures were grown on *c*-plane sapphire and semi-insulating 6H-SiC in a MBE system equipped with a rf nitrogen plasma source from SVT Associates (SVTA-RF45). During growth, reflection high-energy electron diffraction was used to monitor surface morphology. Other *in situ* measurements, including emissivity-corrected surface temperature, thin film growth rate, and III/V flux ratio were performed by a combination of pyrometry and two-color reflectometry (SVTA-IS4000). The growth process started with surface preparation at high temperatures by either removing the surface oxides, in the case of SiC, or nitridation using rf plasma source, in the case of sapphire, followed by the growth of a thin AlN nucleation layer. Next, a 2–3 μm low-defect GaN buffer was grown. A relatively low TD density ($<1\times10^8$ cm^{-2}) in these films was confirmed by both etch pit density measurements, using atomic force microscopy (AFM), and by transmission electron microscopy (TEM). Finally, the AlN/GaN active layer was formed by growing a thin (<5 nm) AlN layer at about 700 °C. To protect the AlN layer, ~1 nm of undoped GaN cap layer was grown on some samples. For comparison, a number of conventional AlGaN/GaN HEMT structures were also grown on sapphire and SiC. The optical and electrical properties of the samples were characterized by cathodoluminescence, Hall, and capacitance-voltage measurements. The thin film quality and surface roughness were studied by x-ray diffraction, TEM, and AFM.

Some of the AlN/GaN structures were processed using standard photolithography to fabricate metal oxide semiconductor (MOS) HEMTs for device measurements. The device

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TABLE I. Results of RT Hall measurements for several AlN/GaN and A1GaN/GaN HEMTs grown on sapphire and SiC.

Sample	n_s (cm^{-2})	μ_{RT} ($cm^2/V\ s$)	ρ_s ($\Omega/\square$)	HEMT structure	Substrate
1	5.47×10^{12}	1220	937	1 nm GaN / 2.0 nm AlN/3.0 μm GaN	Al_2O_3
2	1.83×10^{13}	1610	213	1 nm GaN / 3.0 nm AlN/3.0 μm GaN	Al_2O_3
3	2.50×10^{13}	1780	140	1 nm GaN / 3.5 nm AlN/3.0 μm GaN	Al_2O_3
4	3.27×10^{13}	1130	170	1 nm GaN / 4.0 nm AlN/3.0 μm GaN	Al_2O_3
5	4.10×10^{13}	110	1390	1 nm GaN / 5.0 nm AlN/3.0 μm GaN	Al_2O_3
6	1.68×10^{13}	1630	228	2 nm GaN / 3 nm AlN/3.0 μm GaN	Al_2O_3
7	2.30×10^{13}	1460	185	1 nm GaN / 3.5 nm AlN/2.0 μm GaN	6H-SiC
8	1.05×10^{13}	1830	325	2 nm GaN / 20 nm $Al_2Ga_{0.8}N$/3.0 μm GaN (reference)	Al_2O_3
9	9.60×10^{12}	1990	327	2 nm GaN / 20 nm $Al_2Ga_{0.8}N$/2.0 μm GaN (reference)	6H-SiC

fabrication included the addition of up to 30 nm of Al_2O_3 oxide layer by atomic layer deposition (ALD), followed by reactive ion etching of the oxide layer in the source and drain regions and deposition of a Ti/Al/Ni/Au metal stack to form Ohmic contacts. A contact resistivity $\rho_c \sim 5\times10^{-6}\ \Omega\ cm^2$ was obtained using rapid thermal annealing in nitrogen at 800 °C for 30 s. The metal gate was formed by depositing Ti/Au on top of the Al_2O_3 layer. The ρ_c and ρ_s values were measured using transmission line method (TLM). Device measurements including dc and pulsed *I-V* measurements were performed using an Accent Diva-D225 dynamic *I-V* analyzer.

Table I shows the Hall measurements, averaged over the 2 in. wafer, for a number of AlN/GaN HEMT structures grown on sapphire and SiC. Samples 1–5 in this table show that both μ_{RT} and n_s values are strongly affected by small changes in the thickness of the AlN layer. On the low-defect GaN buffers grown by MBE in this work, the optimum AlN thickness of 3.5 nm produced the lowest as-grown RT ρ_s of $\sim140\ \Omega/\square$ (sample 3). This is about twice the channel conductivity of typical high-quality AlGaN/GaN HEMTs grown on sapphire or SiC (reference samples 8 and 9). To date, the highest RT and 77 K electron mobility values that we have measured on AlN/GaN HEMT wafers are 1850 and 6530 $cm^2/V\ s$, respectively, at a relatively constant n_s value of $\sim1.6\times10^{13}\ cm^{-2}$. Temperature-dependent Hall measurements, performed on samples with n_s as high as $3\times10^{13}\ cm^{-2}$, also showed a constant n_s from RT down to ~10 K (as shown in Fig. 1). Kuzmik *et al.*[9] recently reported a ρ_s of 237 $\Omega/\square$ for an as-grown InAlN/AlN/GaN structure by MOCVD, which could be reduced to as low as 110 $\Omega/\square$ by depositing a thin ZrO_2 layer. We have observed similar improvements in channel conductivity using a thin Al_2O_3 layers formed by ALD on the AlN/GaN HEMTs. In one example, the as-grown average ρ_s of ~259 $\Omega/\square$ on a 2 in. AlN/GaN HEMT dropped to an average of 156 $\Omega/\square$ after depositing 15 nm of Al_2O_3 , as measured by TLM. On the same wafers, we measured local ρ_s values down to ~100 $\Omega/\square$. This is the lowest RT sheet resistivity reported for any III-N based HEMT structure to date. Although the mechanism for such enhancement is not very well understood, these results point to the possibility of even higher channel conductivity in HEMTs with lower as-grown ρ_s values (e.g., sample 3), which is currently being investigated.

Samples with thicker AlN barrier layers (e.g., 4 nm in sample 4) showed a large drop in μ_{RT}, which resulted in a lower channel conductivity in spite of a substantially higher n_s. This might correspond to the onset of dislocation formation in the highly strained AlN layer, which has been reported to depend strongly on a number of extrinsic factors including starting density of TDs, growth conditions, and interface roughness.[14,15] As the AlN layer thickness was further increased to 5 nm or more (sample 5), much higher n_s values ($>4\times10^{13}\ cm^{-2}$) with lower values of μ_{RT} ($<500\ cm^2/V\ s$) were obtained. We note that n_s values $\sim6\times10^{13}\ cm^{-2}$ have been theoretically predicted for these structures.[16] The lower values of μ_{RT} coincide with the formation of a network of microcracks in the highly strained AlN layer, as shown in the AFM images of Figs. 2(a) and 2(b). In addition to a crack-free surface morphology, high mobility samples were found to have atomically abrupt AlN/GaN interface, as imaged by high resolution cross-sectional TEM, shown in Fig. 2(c). Figure 2(c) also shows the importance of growing these structures on low-defect GaN buffer

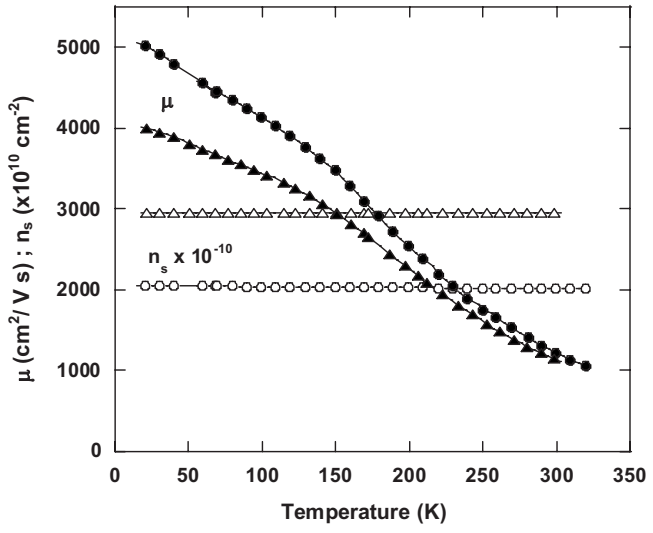

FIG. 1. Temperature dependent Hall measurements on two AlN/GaN HEMT samples (circle and triangle symbols) showing higher 2DEG mobility (closed symbols) with a fixed sheet carrier density (open symbols) at lower temperatures.

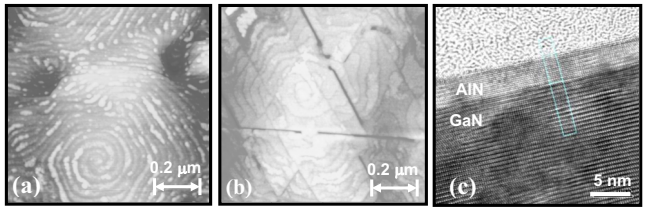

FIG. 2. (Color online) AFM images of (a) 4 nm and (b) 7 nm AlN layer grown on GaN and (c) TEM image of an AlN/GaN HEMT structure.

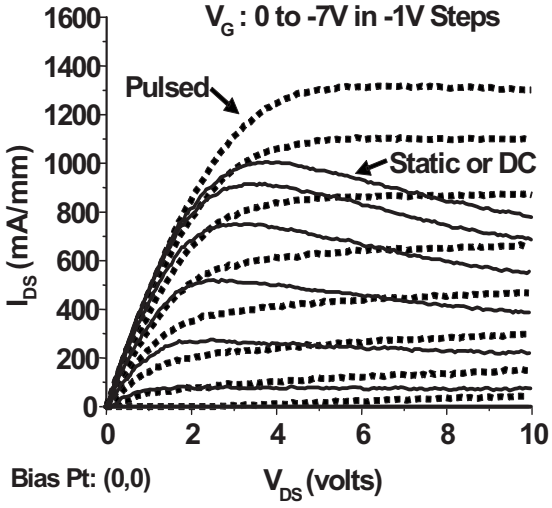

FIG. 3. Characteristic dc (solid lines) and pulsed (dotted lines) *I-V* curves of an AlN/GaN MOS-HEMT, with a gate length of 1.2 μm and source-drain separation of 4.5 μm.

layers in order to obtain smooth AlN/GaN interface for high μ_{RT} values. Though the Coulomb scattering of 2DEG from the charged dislocation lines is expected to be well screened for $n_s > 10^{12}$ cm^{-2}, a large density of TDs can still reduce the mobility by scattering due to both strain variations across the interface, which results in a nonuniform polarization field, and increased surface roughness (e.g., by hillock formation).[17] This is also indicated in recent calculations of Bulashevich *et al.*[18] showing the effect of the interface rms roughness, Δ resulting from TDs at a density of N_{TD}, on the low-temperature mobility as $\mu^{-1} \propto \Delta^2 (n_s N_{TD})^{1/2}$. Finally, a comparison of samples 2 and 6 in Table I shows that to a lesser extent the thickness of the GaN cap layer can also affect n_s which could be caused by modifying the strain and/or the density of surface states.

Lastly, we examined the device performance of the AlN/GaN structures by measuring the dc and pulsed *I-V* characteristics of MOS-HEMTs fabricated in this work. Figure 3 shows the dc (solid line) and pulsed (dotted line) *I-V* characteristics of a device grown on sapphire. The source-drain separation of the device was 4.5 μm. The gate length and width sizes were ~1.2 and 200 μm, respectively. The gate bias V_G was changed from 0 to –7 V in 1 V steps. The pulse length used was 1 μs. The pulse separation was 2 ms. The initial bias point for each pulse was zero gate and drain voltages. This bias point was chosen to highlight the effect of self-heating, which is seen as a drop in dc source-drain current I_{DS} at higher source-drain voltages V_{DS}. As expected from very low ρ_s values, and considering the device dimensions used here, we obtained very high values of zero gate bias I_{DS} ~1.3 A/mm (Fig. 3) and peak transconductance g_m, ~260 mS/mm at a gate bias voltage of about –3 V. However, these low ρ_s values also point to the need for further reduction in contact resistance in order to obtain higher currents. These results are consistent with recent measurements on AlN/GaN HEMTs grown on MOCVD GaN templates, showing very high current densities as the device dimensions are reduced,[19] and point to the great potential of these HEMTs for very high-frequency and high-power applications.

In summary, we have demonstrated high-quality AlN/GaN HEMT structures directly grown on sapphire and SiC by rf plasma-assisted MBE. The strong confinement of the 2DEG and the reduction in roughness and alloy scattering in these structures resulted in both very high μ_{RT} and n_s values. The observed RT sheet resistivity of 100 $\Omega/\square$, on an AlN/GaN structure covered by a thin protective Al_2O_3 layer, is the best reported value for a III-nitride HEMT to date. Based on the *I-V* characteristics of the MOS-HEMTs, with device dimensions used in this work, we expect record high dc and rf device performance for the short channel (<0.25 μm gate length) AlN/GaN HEMTs on SiC, which are currently being studied.

We would like to acknowledge the valuable help from Dr. Ilesanmi Adesida and Dr. Liang Wang at the University of Illinois, Urbana-Champaign, on TEM characterization, and Danh Nguyen at Lehighton Electronics, Inc., for non-contact sheet resistivity measurements. This work was partially supported by the Department of Defense Grant No. W911QX-06-C-0083, monitored by Dr. Pankaj Shah, and Grant No. W911NF-06-C-0190, monitored by Dr. Dwight Woolard.

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