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Electron and hole traps in N-doped ZnO grown on p-type Si by metalorganic chemical vapor deposition

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Electron and hole traps in N-doped ZnO grown on *p*-type Si by metalorganic chemical vapor deposition

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Electron and hole traps in N-doped ZnO were investigated using a structure of n^+-ZnO:Al/*i*-ZnO/ZnO:N grown on a *p*-Si substrate by metalorganic chemical vapor deposition (for growth of the ZnO:N layer) and sputtering deposition (for growth of the *i*-ZnO and n^+-ZnO:Al layers). Current-voltage and capacitance-voltage characteristics measured at temperatures from 200 to 400 K show that the structure is an abrupt n^+-p diode with very low leakage currents. By using deep level transient spectroscopy, two hole traps, H3 (0.35 eV) and H4 (0.48 eV), are found in the *p*-Si substrate, while one electron trap E3 (0.29 eV) and one hole trap H5 (0.9 eV) are observed in the thin ZnO:N layer. Similarities to traps reported in the literature are discussed. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2759181]

I. INTRODUCTION

Among possible acceptor dopants in ZnO, nitrogen has been predicted to be the best candidate because it is about the same size as oxygen and thus should substitute easily without adding much strain.[1,2] However, it has been very challenging to prepare *p*-type nitrogen doped ZnO (ZnO:N), and most attempts, even successful ones, produce low hole concentrations and mobilities, and sometimes even instability.[2,3] In fact, ZnO:N will exhibit *n*-type conductivity when the growth conditions are not precisely controlled. For example, ZnO:N films grown by metalorganic chemical vapor deposition (MOCVD) are *p* type only if deposited at ~400 °C, and higher or lower growth temperatures lead to *n*-type material.[4] Various growth conditions also can influence the presence of midgap impurities and point defects and such deep centers can produce undesired trapping and carrier recombination. In past years, deep level transient spectroscopy (DLTS) has been used to study traps (mainly electron traps) in *n*-type bulk ZnO grown by the hydrothermal,[5] vapor-phase,[6] and pressurized melt growth[7] methods. In most of these cases, the DLTS test structures were Schottky-barrier diodes. A recent DLTS study has revealed deep acceptor states (hole traps) in ZnO single crystals using a novel $p-n$ junction formed by N^+ implantation.[8] In that study, an N^+-implanted *p*-ZnO layer was employed for injecting holes. Here, we present a DLTS investigation of a ZnO:N thin film incorporated into a $p-n$ junction diode. The structure of our $p-n$ diode is composed of n^+-ZnO:Al/*i*-ZnO/ZnO:N layers grown onto a *p*-Si substrate.[9] Although $p-n$ diodes are usually more difficult to fabricate than Schottky diodes, they have one big advantage for DLTS, namely, they allow observation of both hole and electron traps.

II. EXPERIMENTS

The growth procedure is detailed later. First of all, a nitrogen-doped ZnO thin layer, ~270-nm thick, was grown onto a *p*-Si substrate by low-pressure MOCVD.[9] The precursors used in the growth were DEZ $[(C_2H_5)_2Zn]$, oxygen, and dilute NO gas (2 wt % NO/Ar). The carrier for all the precursors was N_2 gas and the deposition temperature was ~400 °C. Next, a bilayer structure of ~100-nm-thick undoped *i*-ZnO layer and a similar thickness of n^+-ZnO:Al layer, with an electron concentration of $\sim 6\times 10^{16}$ cm^{-3} and of $\sim 4\times 10^{20}$ cm^{-3}, respectively, were grown on the ZnO:N layer by sputtering deposition. Ohmic contacts of Ni/Al and Al were then fabricated on the n^+-ZnO and Si substrate, respectively. The contact resistance for the Ni/Al should be very small, because of high-doping in the n^+-ZnO:Al layer. By using the two-terminal method on two contacts (area of ~4 mm^2) with a spacing of 0.5 mm, we checked the total resistance for the Al on Si, which consists of the resistance of the Si substrate and the contact resistance. The total resistance decreases from 80 Ω at 300 K to 52.5 Ω at 150 K, which means a negligible contact resistance, since the decrease of the total resistance is mainly due to the temperature dependence of the electrical properties of the Si substrate. Mesa $n-p$ diodes, each with a junction area of 2 mm^2, were formed by wet etching. In spite of careful wet etching of the Si substrate, a thin SiO_2 layer will be formed at the interface of the ZnO:N/*p*-Si. The formation of SiO_2 at the interface was tested by x-ray diffraction (XRD) on a sample with a

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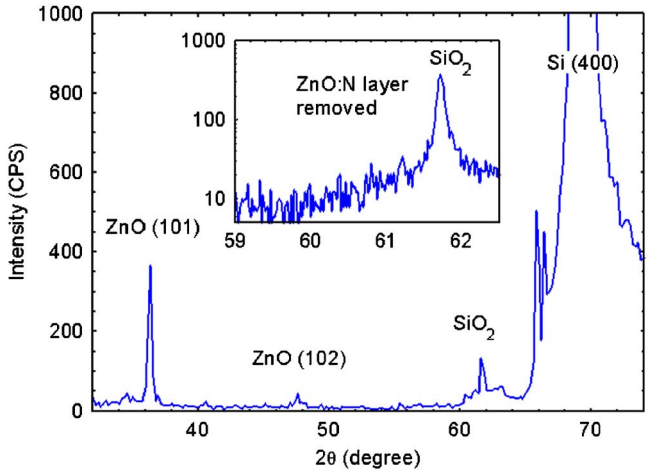

FIG. 1. XRD data of ZnO:N on p-Si. The inset shows existence of SiO_2 feature after removing the ZnO:N layer.

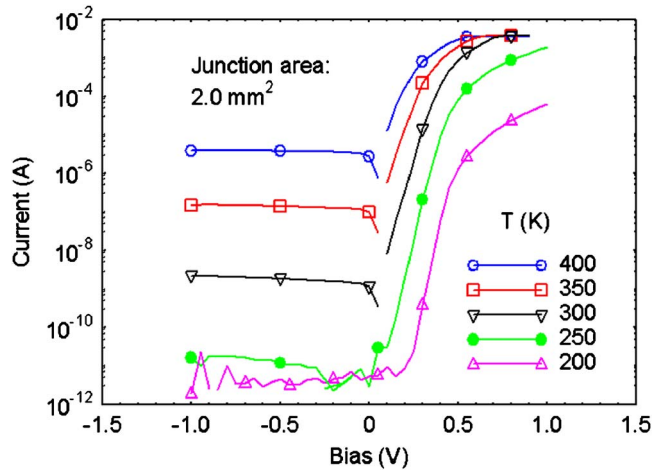

FIG. 2. Temperature-dependent $I-V$ characteristics on a n^+-p junction diode of structure n^+-ZnO:Al/i-ZnO/ZnO:N/p-Si.

ZnO:N layer on p-Si. As shown in Fig. 1, in addition to peaks related to ZnO (101), ZnO (102), and Si (400), we find a peak at $2\theta=61.7°$. According to the Joint Committee on Powder Diffraction Standards card number 14–0654, the peak is ascribed to SiO_2 structure. After removing the ZnO:N layer, the peak remains, as shown in the inset of Fig. 1. As previously reported through measurements of x-ray photoelectron spectroscopy,[10] the thickness of SiO_2 at the n-ZnO/p-Si interface was about 3 nm at a deposition temperature of 480 °C. Thus, we have good evidence for the existence of a thin SiO_2 layer at the ZnO:N/p-Si interface during MOCVD growth at 400 °C; however, it is clear that the thin SiO_2 layer did not cause a problem in obtaining $n-p$ diodes with reasonably good electrical characteristics for the DLTS tests. Current-voltage ($I-V$), capacitance-voltage ($C-V$), and DLTS measurements were measured using a digital Accent DL8000 spectrometer, with 1-MHz and 100-mV test signals, and a Keithley 617 programmable electrometer. The DLTS spectra were obtained from Fourier transforms of the capacitance transients recorded as a function of temperature. The carrier concentration profile was derived from the $C-V$ data.

III. RESULTS AND DISCUSSION

To avoid possible persistent photoconductivity (PPC) induced by room light during sample mounting, the $n-p$-diode sample was kept in the dark for a few hours before the measurements.[11] Actually, unlike the case of bare ZnO samples, the mesa $n-p$ diodes with Ni/Al Ohmic contacts on top of the ZnO:Al layer do not show serious PPC at room temperature. Typical $I-V$ characteristics of the $n-p$ diodes, measured at temperatures from 200 to 400 K, are shown in Fig. 2. The reverse current shows significant temperature dependence, indicating that thermionic emission is the dominant conduction mechanism. At 300 K, the reverse current can be as low as 2×10^{-9} A at a bias of $U_R=-1$ V, which is much lower than that reported for a Pd-Schottky diode sample [cf. sample A, Fig. 1(a), Ref. 8]. At these temperatures, the forward current at low bias ($U_R<0.5$ V) can be well described by $I_F=I_0[\exp(qV/nkT)-1]$, where I_0 is the reverse saturation current and n is the ideality factor (close to unity). From thermionic emission theory, I_0 is given by $I_0=SA^*T^2\exp(-\Phi_b/kT)$, where S is the diode area, A^* is the effective Richardson constant, and Φ_b is the potential barrier height. Thus, an Arrhenius plot of I_0/ST^2 vs $1/T$ can be used to yield Φ_b and A^*. By applying such an analysis for the exponential portion of the forward currents, it is found that $\Phi_b=0.73$ eV and $A^*=1.3$ A cm^{-2} K^{-2}. The value of Φ_b is close to values of built-in potential reported on an n-ZnO/p-Si heterojunction prepared by chemical spray pyrolysis.[12] This value of A^* is much smaller than the theoretical value of 32 A cm^{-2} K^{-2} calculated for ZnO under the assumption that $m_e^*=0.27\ m_0$, where m_0 is the electron mass. The significant difference could be due to the existence of a very thin SiO_2 barrier at the ZnO:N/p-Si interface, through which the electrons must tunnel, as discussed by Hacke *et al.* in connection with the much lower value of A^* found on n-GaN Schottky barrier diodes.[13] Interestingly, the forward current at higher biases, where the current is limited by series resistance, decreases as temperature decreases. The reason may well involve carrier freeze-out in the ZnO:N layer, which has been confirmed by temperature-dependent measurements of dark current in a ZnO:N layer grown on sapphire in a separate run. The dark current for the ZnO:N/sapphire sample, measured under a bias of 1 V from 400 to 100 K, was found to decrease by about two orders of magnitude. Although the ZnO:N layer grown on glass was reported to be p type with a hole concentration of $\sim10^{14}$ cm^{-3},[9] the ZnO:N/sapphire sample exhibits n-type behavior with a sheet concentration of 2×10^{13} cm^{-2} at 300 K. We are not sure of the exact electrical nature of the ZnO:N layer in the n^+-ZnO:Al/i-ZnO/ZnO:N/p-Si structure.

Typical $C-V$ characteristics of the $n-p$ diodes, measured at temperatures from 200 to 400 K, are shown in Fig. 3. The inset in Fig. 3 shows the carrier concentration profile at 300 K. From the inset, we see that: (i) in the region from 0.6 μm up to more than 2 μm, which is in the p-Si substrate, the carrier profile is almost flat ($p\sim1\times10^{15}$ cm^{-3}) and (ii) there is a clear increase of carrier concentration up to

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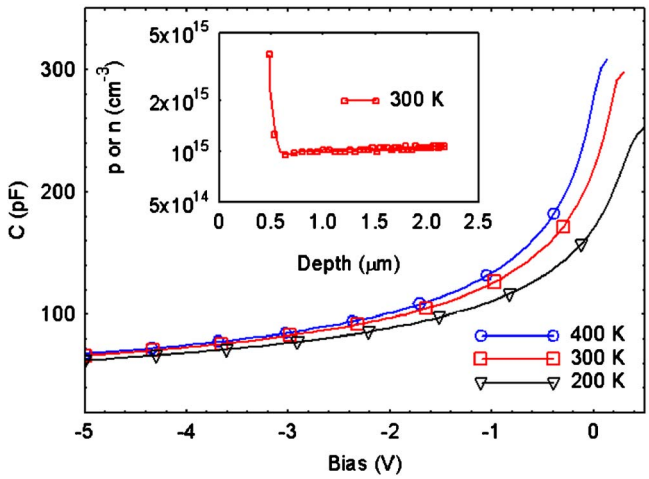

FIG. 3. Temperature-dependent $C-V$ characteristics on the n^+-p diode. The inset shows carrier concentration profile at 300 K.

mid-10^{15} cm^{-3} at a depth of about 0.5 μm, which roughly corresponds to the interface between the ZnO:N and the p-Si. Thus, we speculate that the ZnO:N layer in the structure might be n type; otherwise we would see a profile related to the ~0.3-μm-thick p-type ZnO:N layer at depths of around 0.5 μm, before approaching the n-type i-ZnO layer. The $C-V$ characteristics show significant temperature dependence of the capacitance (i.e., decrease of capacitance with decreasing temperature) at biases close to zero voltage (both above and below), which likely indicates a decreasing contribution to the capacitance from the depletion region in the ZnO:N layer due to carrier freeze-out. The potential barrier at the junction can also be measured by $C-V$ characteristics, since an approximately linear relationship of $1/C^2$ vs U_R was obtained at temperatures from 200 to 400 K (not shown here). At 300 K, the intercept with the x axis at $1/C^2=0$ is 0.5 V, from which a barrier height of 0.76 eV is obtained. These results indicate that the diode is an abrupt n^+-p junction, with the depletion region mainly in the p-Si substrate.

In the n^+-p diode, the n-region (including both n^+-ZnO:Al and i-ZnO thin layers) has a higher carrier concentration than the p region (consisting mainly of the p-Si substrate). The ZnO:N layer, which seems to be n type, serves as a transition region. Detection of hole traps in the p-Si region can be accomplished by setting a reverse bias (U_R) and limiting the filling pulse height (U_P) to values near zero, while detection of electron traps in the ZnO:N region is carried out by keeping a fixed reverse bias and then increasing the filling pulse height to forward voltages (i.e., above zero). DLTS spectra, using fixed $U_R=-3$ V and changing U_P from −0.8 to 0 V or from 0.2 to 0.55 V, are pictured in Figs. 4(a) and 4(b), respectively. As seen in Fig. 4(a), two hole traps (H3 and H4) can be observed when U_P is set at −0.8 and −0.4 V, which corresponds to a trap-detection region within the p-Si substrate. However, when U_P is set to 0 V, a third trap (H5) appears, and H3 and H4 become more prominent because of a larger detection region. Evidently, H3 and H4 are produced by hole traps located in the p-Si region, while H5 arises from a trap located in the transition region, i.e., in the ZnO:N layer. When the forward filling pulses are

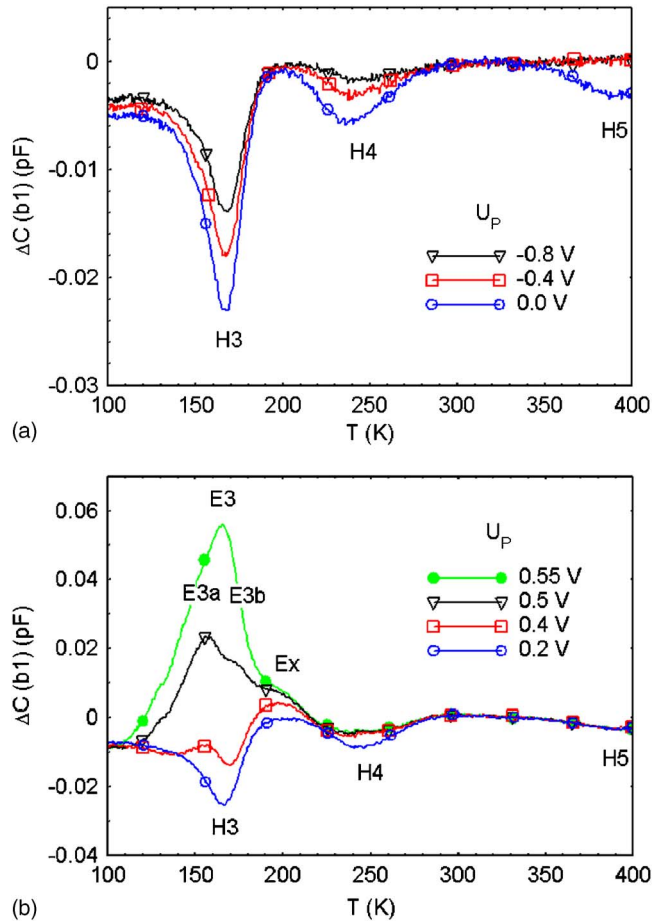

FIG. 4. DLTS spectra for the n^+-p diode, measured with constant reverse bias $U_R=-3$ V, and (a) negative filling pulse heights (U_P's) for hole injection and (b) positive filling pulse heights for electron injection. The other parameters were: filling pulse length $t_P=1$ ms and measurement period $T_W=20.48$ ms.

kept in the range 0.2–0.55 V, where the forward current increases exponentially, electron injection from the n-ZnO region is realized. As seen in Fig. 4(b), as U_P is gradually increased and more electrons are injected, an electron trap (E3) with a shoulder feature (Ex) can be clearly observed. Obviously, E3 consists of two components, E3a and E3b, as seen from the spectrum measured at $U_P=0.5$ V.

Since the thin ZnO:N layer was grown on the p-Si substrate, it can be seen as a "surface layer" on the p-Si. Thus, we can apply a technique, which was developed to judge whether traps are distributed through out the depletion region (bulk-like) or are concentrated near the "surface."[14] The DLTS peak height for a given trap is measured as a function of applied bias, while keeping the filling pulse height constant. With increasing U_R, a bulk trap signal will increase and a surface trap signal will decrease. DLTS spectra, measured under different biases, keeping $U_P=0$ V (to observe hole traps) or $U_P=0.55$ V (to observe both electron and hole traps), are presented in Figs. 5(a) and 5(b). In Fig. 5(a), we see that with increasing U_R, the trap signals of H3 and H4 increase and the trap signal of H5 decreases, which suggests that H3 and H4 are bulk traps in the p-Si, and trap H5, has a surface nature, i.e., is located in the ZnO:N layer. From Fig. 5(b), we find that electron trap E3, composed of E3a and

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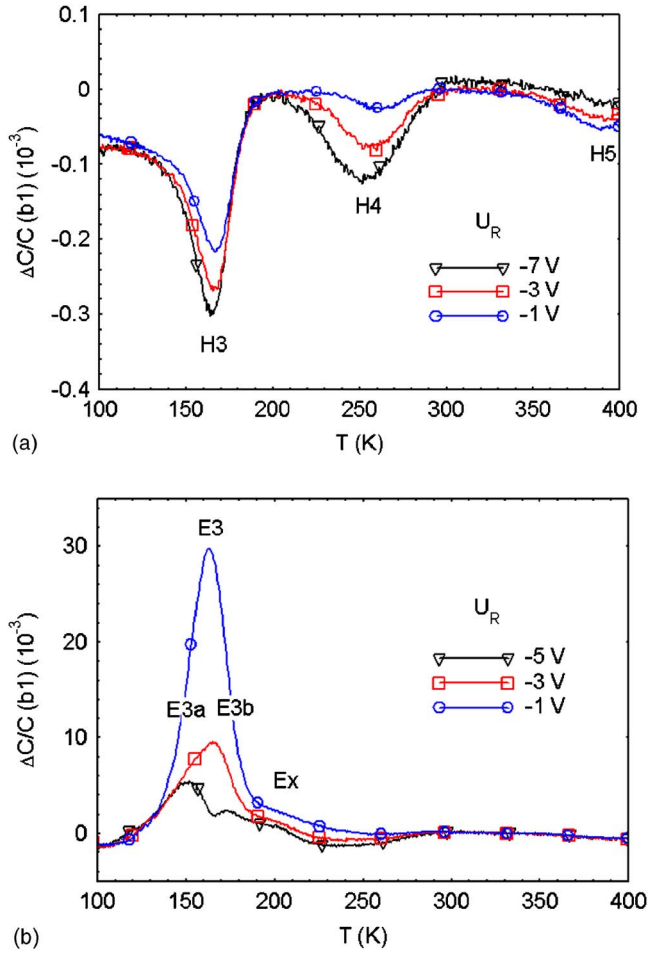

FIG. 5. DLTS spectra for the n^+-p diode, measured with (a) $U_P=0$ and variable U_R; and (b) $U_P=0.55$ V and variable U_R. The other parameters were: $t_P=1$ ms, and $T_W=20.48$ ms.

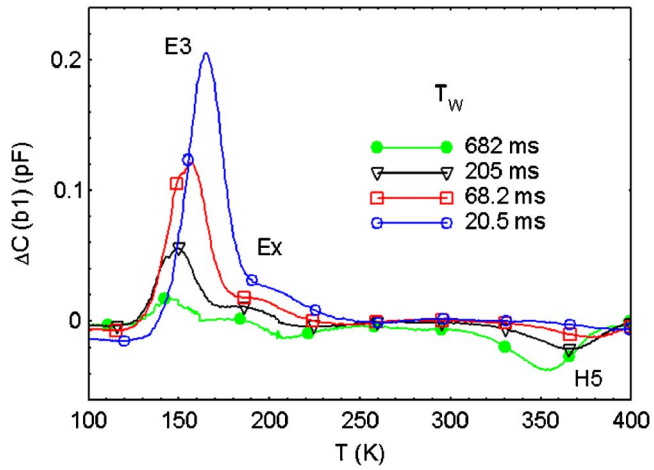

FIG. 6. DLTS spectra for the n^+-p diode as a function of measurement period T_W. The other parameters were: $U_R=-1$ V, $U_P=0.5$ V, $t_P=1$ ms, and $T_W=20.48$ ms.

E3b, decreases when U_R increases, which implies that this trap is also located in the thin ZnO:N layer. It appears that E3a has a larger capture cross section than E3b, when a higher bias (or electric field) is applied.

By using "maximum evaluation," a software designed for analysis of trap parameters, the activation energy and apparent capture cross section for the major DLTS traps are determined to be: 0.29 eV and 4.4×10^{-16} cm^2 for E3; 0.35 eV and 7.4×10^{-14} cm^2 for H3; 0.48 eV and 2.9×10^{-15} cm^2 for H4; and 0.9 eV and 4×10^{-14} cm^2 for H5, respectively. The electron trap E3, with an activation energy of 0.29–0.30 eV, has been previously reported for all bulk ZnO (Refs. 5–7) and is thought to be related to oxygen vacancies, V_O. Actually, the presence of two components in the trap E3 has been clearly revealed by high-resolution Laplace DLTS characterization.[7] However, in vapor transport grown ZnO bulk crystals, a deep center E4 at 0.53 eV below the conduction band was found to decrease after oxygen annealing and thus has been assigned to V_O.[15] On the other hand, in a recent study of as-grown and N$^+$-implanted ZnO single crystals, E3 has been assigned to Zn_i.[16] The hole trap H3, with activation energy of 0.35 eV, could be related to transition metals in the *p*-Si, or Zn that might have diffused into the *p*-Si during growth of the ZnO films.[17] It should also be mentioned that a Li-acceptor-related hole trap A_3, with activation energy of 0.28 eV and capture cross section of $\sim10^{-16}$ cm^2, was reported in pressurized melt-grown ZnO using a $p-n$ junction diode formed by N$^+$-implantation;[8] on the other hand, we have no evidence for Li in our sample. The hole trap H4, with an activation energy of 0.48 eV, could also be due to transition metals in *p*-Si.[17] However, a further understanding of H3 and H4 will require a DLTS study of the *p*-Si substrate itself. A preliminary measurement, which was performed on a *p*-Si Schottky diode (with the ZnO:N layer removed), shows the existence of H3. The hole trap H5, with an activation energy of 0.9 eV, has been observed in the ZnO:N layer. The 0.9-eV hole trap was reported in vapor transport grown bulk ZnO, for both a virgin sample and a sample implanted with 100-keV protons.[18] In Ref. 18, the authors invoked an early review that related these centers to oxygen vacancies. In contrast to the behavior of the other traps, the DLTS signal of H5 shows an anomalous increase as the measurement period T_W increases (or the "rate window" decreases), as shown in Fig. 6. Sometimes a decrease of the DLTS signal with decreasing rate window is observed and this effect is usually attributed to a capture barrier, such as might be associated with threading dislocations.[19] Further DLTS investigations will be needed to understand the peculiar capture behavior of trap H5.

IV. CONCLUSIONS

A n^+-p diode, consisting of *n*+-ZnO:Al/*i*-ZnO/ZnO:N layer grown on *p*-Si, has been used to investigate electron and hole traps in the ZnO:N layer. The temperature-dependent $I-V$ and $C-V$ characteristics show that the diode has an abrupt junction with a potential barrier of 0.75 eV. When holes are injected by reverse biasing the diode, three hole traps, H3 (0.35 eV), H4 (0.48 eV), and H5 (0.9 eV), are observed; also, one electron trap E3 (0.29 eV) is revealed by injecting electrons. Following the results of previous studies, E3 could be related to oxygen vacancies or zinc interstitials, while H3 and H4 could

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be due to impurities in the *p*-Si. A hole trap, H5 (0.9 eV), is observed in the ZnO:N layer; however, it displays a peculiar capture behavior.

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