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Weatherford, T.R.

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Effects of Low-Temperature Buffer-Layer Thickness and Growth Temperature on the SEE Sensitivity of GaAs HIGFET Circuits

T. R. Weatherford[1], *Member, IEEE,* P.W. Marshall[2,3], *Member, IEEE,* C.J. Marshall[2], D. J. Fouts[1], *Member, IEEE,* B. Mathes[4] and M. LaMacchia[4]

[1]Naval Postgraduate School, Code EC, Monterey, CA 93943

[2]Naval Research Laboratory, 4555 Overlook Avenue SW, Washington DC 20375

[3]SFA, Inc., 1401 McCormick Avenue, Largo, MD 24033

[4]Motorola Government Systems, Scottsdale, AZ

Abstract

Heavy-ion Single Event Effects (SEE) test results reveal the roles of growth temperature and buffer layer thickness in the use of a low-temperature grown GaAs (LT GaAs) buffer layer for suppressing SEE sensitivity in GaAs HIGFET circuits.

I. INTRODUCTION

FET-based GaAs ICs have shown excellent immunity to Total Ionizing Dose (TID) and single event latchup effects [1]. However, FET-based GaAs digital ICs are severely limited in space-based applications due to the susceptibility of the technology to Single-Event Upset (SEU). Our research has addressed the implementation of a LT GaAs buffer layer under GaAs FET circuits to dramatically improve their SEU performance. Specifically, we have studied growth temperature and geometry effects on LT GaAs buffer layer parameters in the Motorola C-GaAs™ IC process [2].

Digital GaAs ICs are attractive for high-speed digital applications due to their low dynamic power dissipation [3]. GaAs FET-based ICs provide some of the highest packing densities for digital circuits operating above 500 MHz. A disadvantage associated with GaAs digital Metal-Semiconductor FET (MESFET) ICs is their high static power dissipation. The Motorola C-GaAs™ process utilizes a Heterostructure Insulated Gate FET (HIGFET) to substantially reduce gate leakage. This process has evolved from the delta-doped C-HIGFET process licensed to Motorola by Honeywell. Static power dissipation is reduced by 3 or more orders of magnitude over digital MESFET ICs [2]. Vulnerability to SEU effects is reduced from 10^{-3} errors/bit-day to approximately 10^{-5} to 10^{-6} errors/bit-day for the complementary HIGFET IC process as compared to the MESFET technology [4]. However, even the later SEU rate is still not acceptable for most space-based applications.

Circuit techniques to reduce SEU have shown some promise but require compromises in design and layout [5]. Designing an epitaxial wafer with LT GaAs buffer layers can reduce SEE without compromising previous circuit or mask designs. Only a modification of the structure of the Molecular Beam Epitaxy (MBE) wafer needs to be implemented. The purpose of this work is to determine the optimal parameters for obtaining SEU-immune circuits in the Motorola C-GaAs™ process. The goal is the ability to manufacture the LT GaAs wafer in a manner to be transparent to the baseline fabrication process. The LT GaAs has a potential to enhance yield and performance [6].

FET-based GaAs ICs have a disadvantage compared to Si MOSFET technology because the FET gate leakage current increases static power consumption. The use of heterojunctions to increase gate barrier heights has lead to improvements in power-speed products and the SEU performance as shown in Figure 1 [2]. E/D MESFET or Direct Coupled FET Logic (DCFL) and the complementary, single-ended logic, HIGFET families (n-channel and p-channel, C-HIGFET) are further hardened against SEU because of the larger noise margins that result from reduced gate leakage.

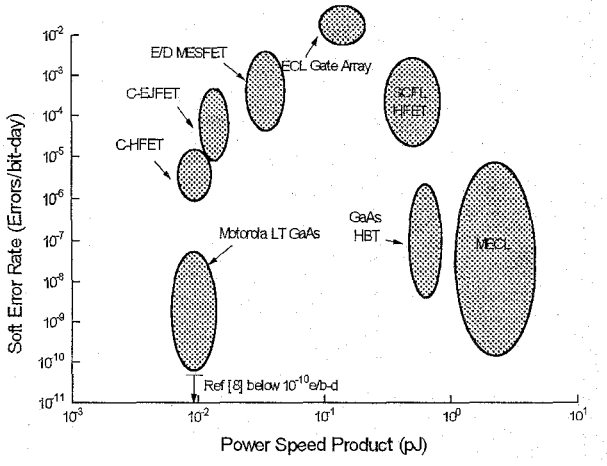

Figure 1: Speed-power vs SEU rate for several digital GaAs IC technologies. Error rates are estimated from LET and saturated cross sections from static tests for heavy ion upset in geosynchronous orbits [6].

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Even with heterostructure gates, differential logic families such as Emitter-Coupled Logic (ECL Gate Array), Source-Coupled FET Logic (SCFL), and Current Mode Logic (CML) are much more sensitive to SEU when power speed products are reduced unlike complementary logic.

Cutchin et al. [7] reported on the proton and heavy ion SEU characteristics of a GaAs (C-HIGFET) 1k x 1 SRAM fabricated in GaAs. They performed static (no clocking) measurements and observed SEU upset cross-sections for C-HIGFET devices of 1 to 2 orders of magnitude lower, compared to alternative ECL gate arrays or E/D MESFET technologies. Reference [4] explored the SEU sensitivity of SCFL fabricated using HIGFETs and extended the results in [7] to cover a range of clocking speeds using a serial shift register structure. Two key findings were that the SEE sensitivity of the SCFL approach was higher than that of the complementary structure. More importantly, the SEE cross sections measured at high data transfer rates increased dramatically with clock speed. Utilizing LT GaAs buffers to limit charge collection should provide SEU-hard SCFL and CML circuits for applications above 1 GHz clock speeds.

In a separate study, the efficiency of a low temperature (LT) GaAs buffer layer for mitigating SEE sensitivity in C-HIGFET structures was examined [8]. That work extended the results of static SEU tests on the 1.0 micron feature size SRAM [7] by evaluating dynamic SEU characteristics on a 0.7 micron feature-size shift register. It also compared the SEU response of the shift register as fabricated on conventional semi-insulating starting material with that of otherwise identical devices fabricated on a LT GaAs buffer layer. For the complementary logic family, the LT approach provided virtual immunity to particles with LET values as high as 90 MeV/mg/cm^2.

There are two key aspects to the present study. First, we have extended the previous body of work to include the application of a LT buffer layer to mitigate SEE in the more vulnerable high speed CML and SCFL HIGFET families, and have evaluated their SEE performance during high speed operation where vulnerabilities are greatest [8],[9]. Second and most importantly, these experiments demonstrate the roles of two key growth parameters in the MBE process by which the LT GaAs buffer is grown. These are the temperature at which the layer is grown and the thickness of the deposited layer. The experimental approach presented here is augmented by modeling and computer simulations aimed at a more detailed understanding of the interaction of the LT GaAs buffer to device performance [10],[11].

In contrast to silicon-on-insulator (SOI) where an oxide acts as a coulombic barrier to block ionized charge in the substrate, the basic principle behind LT GaAs buffers is to utilize improved recombination properties to remove free charge before it reaches the device's contacts. Hence, it is essential to optimize recombination in the LT GaAs material.

II. Low-Temperature Grown GaAs

The beneficial properties of LT GaAs include high resistivity and very short carrier lifetimes [12],[13]. These characteristics are due to a high density (~10^{18}/cm3) of As anti-sites and Ga vacancies in the semiconductor [14]. The use of low temperatures (190°C to 400°C) in the growth of the MBE epitaxial GaAs is to increase the excess concentration of As to approximately 1 to 2%. In this work, buffers were grown at 220°C, 280°C and 350°C. The combination of As overpressure and low temperature MBE growth places As interstitially in the lattice. At this stage, the GaAs lattice is expanded due to the interstitual As. Following the low temperature growth, the sample is annealed at higher temperatures. During the anneal the As coalesces into precipitates or else moves to Ga sites developing As antisites and Ga vacancies. This allows the lattice constant to return to the normal GaAs lattice spacing and the resulting high density of defects shortens the carrier lifetimes to below 1 picosecond [13].

At higher GaAs growth temperatures, less excess As is introduced into the crystal so there are fewer defects present after annealing. The reduced defect density provides longer mean free paths between trap centers, i.e. longer carrier lifetimes as compared to material grown at lower temperatures. Larger buffers provide more recombination centers and it is expected that within reasonable constraints, the thickest buffer grown at the lowest temperature will prove to be superior for charge recombination and elimination of SEEs in nearby circuits.

Figure 2 is a transmission electron microscopy (TEM) image of a GaAs epitaxial structure above a LT GaAs buffer.

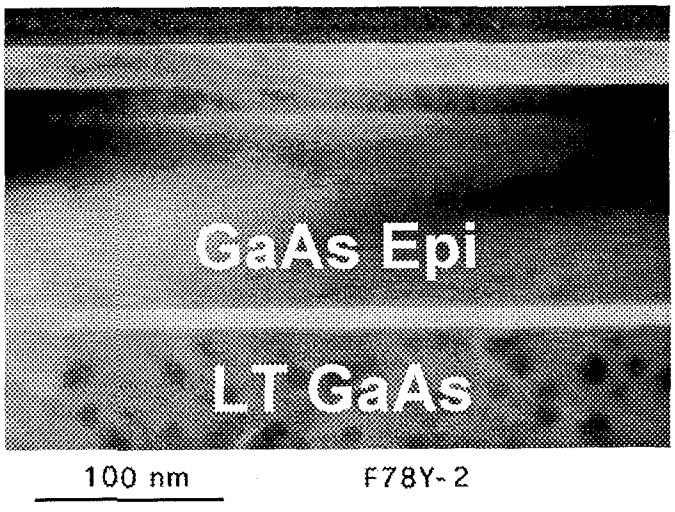

Figure 2: A transmission electron microscopy image of the LT GaAs buffer layer. Regions where the precipitates exist is the LT GaAs buffer region.

Separating these regions is an AlAs diffusion barrier which acts to prevent As from migrating outside of the buffer. This is important since As outdiffusion from the buffer during the annealing process has two detrimental effects. First, the reduced defect density increases the carrier lifetime thereby compromising carrier recombination in the buffer. Secondly, we have observed a degradation in FET transconductance which may be caused by As related traps in the channel region.

III. Motorola C-GaAs™ Process

The MBE wafer/LT GaAs buffer structures grown in this study were fabricated in the Motorola 0.7 micron C-GaAs™ process without any modifications to implants or anneals in the baseline process.

The MBE epitaxial layers are grown on bulk GaAs wafers. The IC process utilizes an AlGaAs-InGaAs heterostructure channel in the fabrication of an Insulated Gate FET (IGFET). Ohmic implants are used for the source and drain contacts, whereas an undoped Schottky contact is used for the gate. Because the C-GaAs™ process already employs MBE epitaxial layers grown on bulk GaAs, the cost impact of growing the MBE LT GaAs buffer is minimal.

Fortunately, the C-GaAs™ process uses Rapid Thermal Anneals (RTAs) which are advantageous compared to furnace anneals, because the RTAs cause significantly less degradation to the recombination properties of the LT GaAs buffer layer. This is important because after the buffer is produced, it is annealed during the MBE epi-layer growth and once again after the implantation to form the ohmic contacts. We note that the annealing procedure used in this work is not changed from the baseline C-GaAs™ process.

The process control monitor structures were evaluated at Motorola. The most significant change in the FET parameters compared to the conventional process, was a 50 to 100% increase in the ohmic-implant sheet resistance seen on all five of the wafers tested. We believe that the increase in sheet resistance resulted from reduced activation of the N-implant near the LT-grown buffer layer but this issue is still under study. Subsequent fabrications using Schottky-based resistors, as opposed to ion implanted ones, have not exhibited this problem. Because of the effect of the implant activation problem on the source follower feedback resistors, the bandwidths of these parts were considerably below the design goal of ~ 1.2 Gbps. However, all other process parameters were within the process windows. Specifically, device thresholds were unaffected by the implant activation problem because of the existence of a delta-doped layer in the HIGFET structure, which partially shields the InGaAs from the resulting fermi level shift. [10]. In summary, the first attempt to incorporate LT GaAs buffers in the C-GaAs™ process was successful even though further optimization is required.

IV. Test Devices

Figure 3 shows the HIGFET device structure. The matrix of starting wafers was supplied by Picogiga Inc. and includes three growth temperatures for two different thicknesses of the LT GaAs layer, as shown in Table 1. These parameters were selected based on the expected likelihood of growing high quality epitaxial material above the LT GaAs layer, the insights provided by computer simulations of the HIGFET structure [11], and what was understood from our previous work [8] and the LT GaAs literature [11],[12],[13]. All of the LT GaAs starting wafers were grown consecutively at Picogiga Inc. As illustrated in Figure 3, a 100 A thick AlAs diffusion barrier was grown above the LT GaAs buffer, but no diffusion barrier exists below the LT buffer.

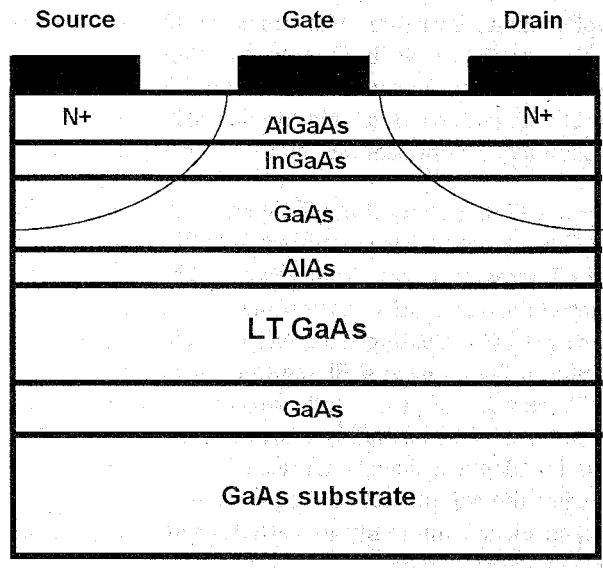

Figure 3: Cross sectional view representative of a C-GaAs HIGFET placed on a LT GaAs buffer with an AlAs diffusion barrier.

One of each of the six types of wafers listed in Table 1 was processed at Motorola. Some of the duplicate wafers were utilized for various material characterization studies. An existing mask set was used which included the same 32-bit serial shift register studied in our earlier work and allows a comparison to the conventional technology [8]. Shift registers from each wafer, except number 5 which was damaged during processing, were packaged. Functional testing was performed to select the best parts for SEE testing. The dicing of test structures from wafer number 4 for other projects prevented us from obtaining the shift registers on that die for SEE testing.

In addition to the wafers described in Table 1, we tested identical shift registers from a separate wafer lot that were processed similarly except that a 5000 A buffer layer was grown at 200°C and the diffusion layer was composed of AlGaAs instead of AlAs.

VI. Test Setup

The ion test setup was similar to that described in [8]. A commercially-available bit error rate test set (BERT) provided differential ECL level data and clock to the serial shift registers. As shown in Figure 4, data was clocked through the DUT while exposed to ions in the Brookhaven National Laboratory heavy ion test chamber. Clock recovery was accomplished in the BERT receiver or, alternatively, the clock was passed directly to the BERT receiver and to the DUT. A pseudo random bit sequence, (2^7-1) in length, was used throughout the tests.

Table 1.
Wafer growth parameters.

Wafer Number	Quantity	LT Layer Thickness (A)	Growth Temperature (°C)
1	2	4000	220
2	2	4000	280
3	2	4000	350
4	2	6000	220
5	2	6000	280
6	2	6000	350

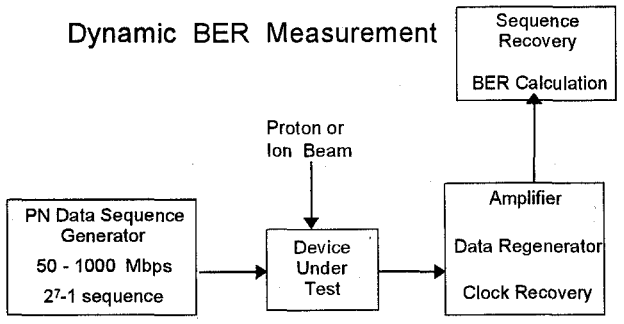

Figure 4: Pseudorandom data is clocked through the shift register DUT at high data rates during exposure.

VII. Test Results

A total of seven CML and SCFL shift registers from 5 wafers were tested with heavy ions. All data was obtained with a clock frequency of 200 MHz unless otherwise noted. The SEE error cross sections were measured at room temperature with normal biasing on each part using at least 5 ions with LETS ranging from 3.6 MeV/mg/cm^2 (Fl-19 at 140 MeV) to 110 MeV/mg/cm^2 (Au-197 incident at 60° at 350 MeV).

Figure 5 compares the LET curves for the conventional CML technology and two LT GaAs CML cases, specifically the 4000 A / 220°C LT GaAs buffer and the 6000 A / 350°C buffer. (In this abbreviated description of the various wafers, the first number refers to the thickness of the LT buffer, and the second number gives the growth temperature.) The improvement in saturated upset cross section is approximately 4 orders of magnitude compared to the conventional technology. The LET threshold increased from below 1 MeV/mg/cm^2 to 28 MeV/mg/cm^2, which is greater than 1 order of magnitude improvement.

The temperature dependence of the SEE saturated error cross sections per bit and LET thresholds (10% of saturated cross section) for the 4000 A and 6000 A CML devices is illustrated in Figure 6. The improvement in both the saturation cross section and threshold LET are clearly shown in the data as the buffer growth temperature is lowered. At 350°C we note that the increased buffer layer thickness accounts for an order of magnitude decrease in cross section.

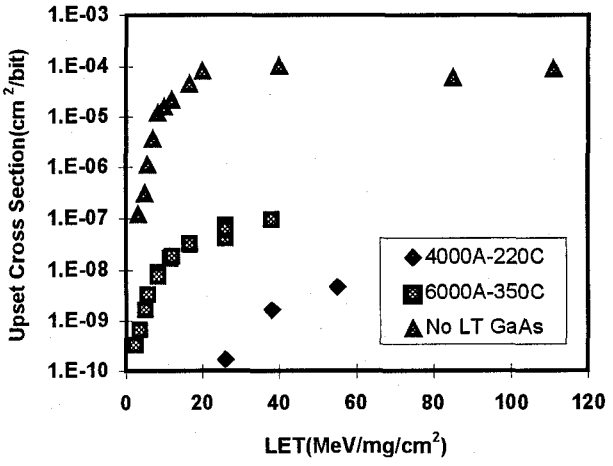

Figure 5: SEE cross sections for the CML devices with 4000A / 220°C, 6000A / 350°C LT GaAs buffer layers are compared with those for the conventional technology.

Improvements in the SCFL devices are less than those observed for the CML. Conventional SCFL saturated cross cross sections of 1e-4 cm^2/bit and threshold LETs of <1 MeV/mg/cm^2 have been reported [8].

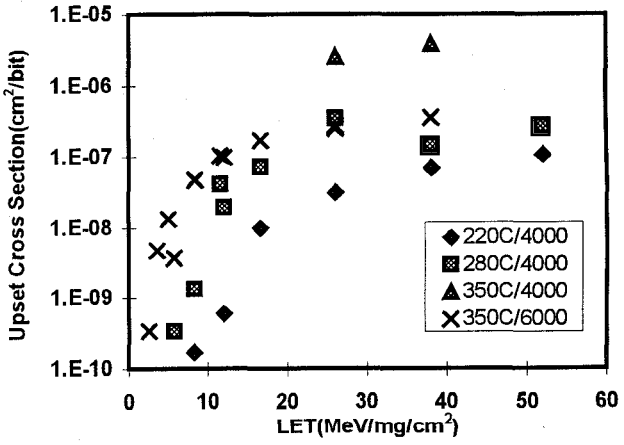

Figure 6: SCFL device cross section curves for 4000 A thick LT GaAs buffers grown at 220°C, 280°C and 350°C, and a 6000A buffer grown at 350°C.

Figure 6 shows SEE sections curves for SCFL devices grown with various LT GaAs buffer layers. The saturated cross sections range from 3.84e-6 cm2/bit (4000A / 350oC) to 1.07e-7 cm2/bit (4000A / 220oC), which is a factor of 36. As compared to the conventional SCFL technology, the saturated SEE cross section for the 4000A / 220oC case is reduced by three orders of magnitude and the LET threshold is increased by one order of magnitude.

Increasing the buffer layer from 4000 A to 6000 A in the 350°C case reduces the SCFL cross section by a factor of 11, which is similar to the results for the CML devices. The threshold LET cannot be determined from the 200 MHz data, however the analysis obtained at other frequencies and operating biases suggests that the LET threshold may have been reduced by a factor between 2 to 10 for thicker buffer layer.

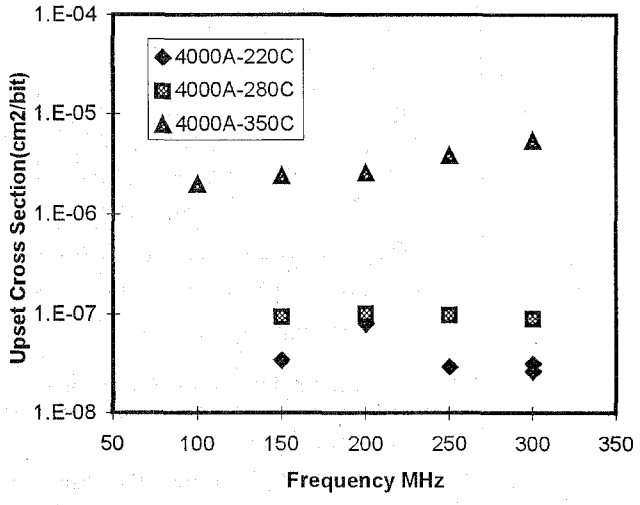

Figure 7: Upset cross sections for CML shift registers verses clock frequency.

The data rate dependence of the cross section is shown in Figure 7 for the CML devices with the 4000 A thick buffers. The SEU sensitivity increases above 200 MHz for the 220°C and 280°C cases. However, the SEU cross sections (irrespective of LT growth temperature), are within an order of magnitude at 300 MHz. In contrast, the SCFL SEU cross sections are independent of frequency (up to 300 MHz) for devices regardless of LT growth temperature as shown in Figure 8.

VIII. Discussion

The previous tests [8] demonstrated extraordinary SEE hardening achieved using a Honeywell-grown LT layer underneath C-HIGFET shift registers and flip-flops. Although no upsets were observed for LETs as high as 90 MeV/mg/cm^2, we note that only 1 shift register and 1 flip flop

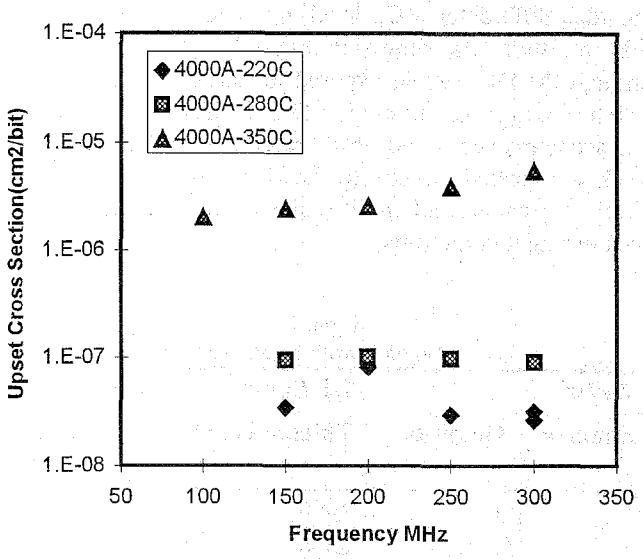

Figure 8: Upset cross sections for SCFL shift registers verses clock frequency.

from a single lot that we tested. The results in this paper are from the first water lot of LT GaAs devices and further optimization of the buffer structure and growth parameters is required. The first devices have lower LET thresholds (26 MeV/mg/cm^2) as compared to the Honeywell devices in [8]. However, we note that the complementary logic of the later devices is more readily hardened than the differential pair logic evaluated in the present study. (Previous measurements [4] showed an order of magnitude difference in the cross sections of these technologies.) Also, the clock rate employed in the testing of the Honeywell devices [8] was significantly lower than those in the current work. Even so, we observe upset cross sections improved by as much as 4 orders of magnitude over equivalent non LT devices. It is also very significant that the thicker buffers comprised of LT grown at lower temperatures demonstrated enhanced SEE hardness as expected.

As indicated by Figure 9, out diffusion of As from the LT GaAs buffer layer may have compromised the SEE hardness of the present devices. Notice the change in defect density from the top to the bottom of the buffer layer shown in the TEM. A critical density of interstitial As is required to form the defects responsible for the picosecond carrier lifetimes that result in SEE hardness. A second diffusion layer beneath the LT buffer layer might prevent As outdiffusion and further improve the SEE response of this technology.

Devices fabricated on the 5000 A / 200°C wafer were much more SEU sensitive than any of the other parts. TEMs on this wafer reveal a poor interface between the AlGaAs

diffusion barrier and upper GaAs epitaxy. Since this problem has not been observed on subsequent wafers which have AlGaAs diffusion barriers, the epitaxial quality is not expected to be impacted by the use of AlGaAs versus AlAs diffusion barriers. The quality of the epitaxial layer itself may be the most critical of issue.

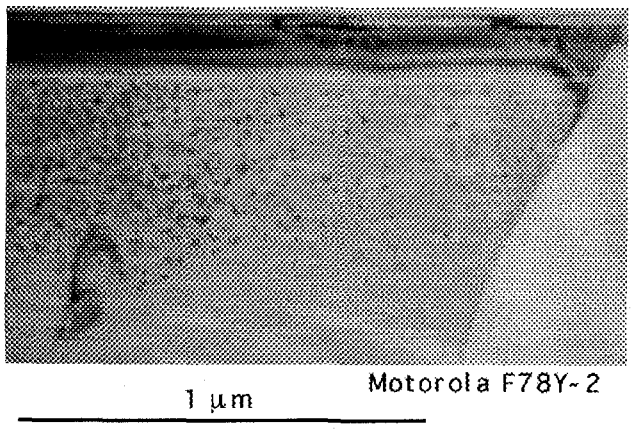

Figure 9: A post fabrication TEM image of an LT GaAs buffer grown at 220°C.

CML is identical to Si ECL except that CML utilizes FETs. SCFL utilizes a differential type gate, but with leveling shifting. Power consumption and currents are higher in SCFL and these differences are observed in the SEU results. The differences in hardening due to the LT GaAs buffer layer may be less in the SCFL due to the susceptibility of the level shift diode. Noise margins are small in both logic families but the higher power-speed product in the SCFL follows the trend in Figure 1.

Figures 10 and 11 summarize the dependence of upset cross section and threshold LET on CML and SCFL respectively. The upset cross sections for both technologies are observed to have the same dependence of the LT GaAs growth temperature. The dependence between SCFL and CML thresholds can not be directly compared because of differences in critical charges.

We observed that reducing the LT GaAs buffer growth temperature from 350°C to 220°C was more effective at SEU hardening that increasing the LT buffer from 4000 to 6000 A. Growth temperature and buffer thickness control carrier lifetime and transit times through the buffer respectively. For the buffer to prevent free charge from collecting at the FET terminals, carrier lifetimes must be much shorter than the transit time through the buffer. Thus the maximum SEU hardness would be expected from a combination of the lowest possible LT GaAs growth temperature and the thickest buffer layer. Growth temperatures above about 200°C are the best to obtain crystalline LT GaAs material. Also, a buffer thickness in excess of about 1 μm can result in stacking faults that adversely impact the subsequent epi growth.

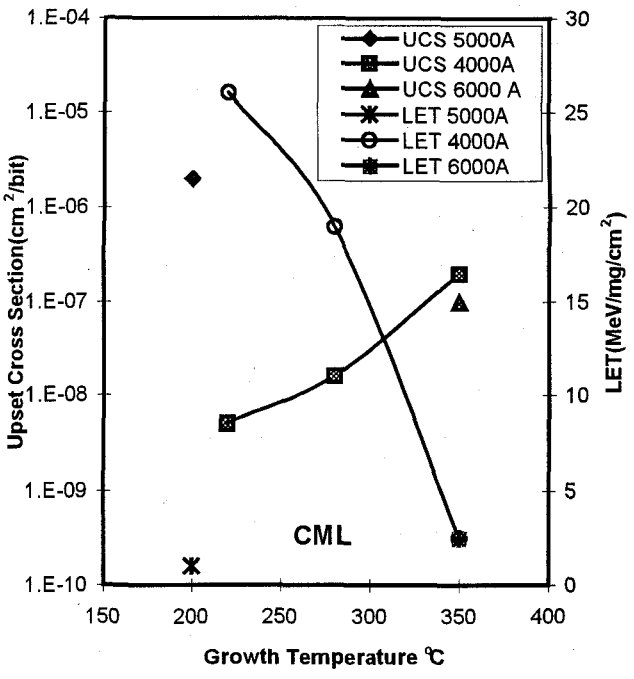

Figure 10: LET threshold and upset cross section versus LT growth temperature for various buffer thickness from CML.

The frequency dependence of the cross section also merits discussion. In Figure 7, the two lower growth temperature CML cases showed a strong dependence on increasing clock frequency, as opposed to the 350°C data which showed no frequency dependence. As discussed

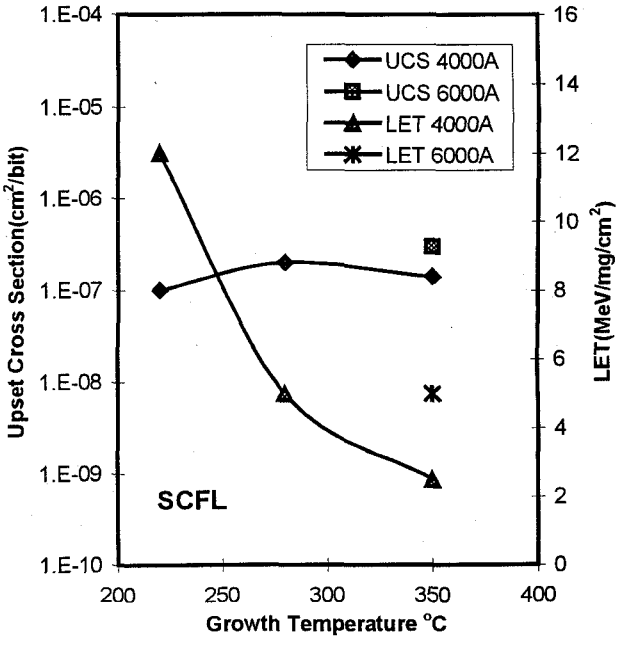

Figure 11: Saturated cross section and threshold LET versus LT growth temperature for various buffer thicknesses in SCFL.

earlier, all the processed wafers showed similar increases in sheet resistively of the implanted resistors. Therefore the frequency dependence may be related to charge collection and not a circuit limitation (i.e. noise margin lost at high frequencies). We also note that the increase in upset cross section starts at 250 MHz (4ns), which is close to hole lifetime in the GaAs. This may suggest part of the upset mechanism in the CML devices is related to hole dominated collection mechanisms. The SCFL data shows no degradation up to 300 MHz, suggesting that a 3.3 ns clock is not limited by either a critical path to latch data or charge collection mechanisms.

For comparison, in figures 9 and 10, cross sections were measured at ~70% of the maximum operating frequency for each device. Not all devices had the same bandwidth, thus the maximum test frequencies varied. This criteria is due to previous observations in conducting high data rate SEU experiments [4,8].

IX. Conclusions

We are reporting substantial progress in understanding and implementing the use of an LT buffer layer to solve the SEE problem in GaAs HIGFET devices. This advance is gained through a systematic investigation using a matrix of buffer materials which are evaluated using electrical measurements, ion-induced SEE measurements, and TEM studies.

The first iteration of this research offers promise that SEE sensitivity in MBE-based GaAs FET logic can be dramatically reduced. The improvements suggest that SCFL logic soft error rates can be reduced by 5 orders of magnitude, and the CML soft errors could be reduced by 6 or more orders of magnitude. The resulting SER levels should be below 10^{-10} errors/bit-day for geosynchrous orbit, which is sufficient to satisfy most applications. It should be noted that all these estimates are for circuits operating at a 200 MHz clock rate.

The data obtained for clock-rate dependence show the LT GaAs buffers can increase the unstable bandwidth of digital GaAs FET circuits in an SEU environment. However, the improvement is dependent on the logic family, and it is not presently clear whether the sensitivity is due to circuit delays or charge collection mechanisms.

Process yield does not appear to be strongly impacted when LT GaAs buffers are utilized in an MBE process. Although further refinements are needed, this first iteration has shown considerable improvement in SEU hardness.

Utilization of this technique provides a cost-effective SEU solution for digital GaAs FET integrated circuits because no re-engineering or mask costs are required once a baseline process is established

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