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A high level noise blanker RF amplifier system for the UHF band

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NAVAL POSTGRADUATE SCHOOL

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A HIGH LEVEL NOISE BLANKER AND RF AMPLIFIER SYSTEM FOR THE UHF BAND

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ABSTRACT

The design and construction of a high level noise blanker and RF amplifier system as used in RFI measurement work is presented. This RFI work is part of the "Shipboard RFI in UHF Satcom" project sponsored by Naval Electronic Systems Command. The system requirements are discussed providing a basis for deriving the system specifications. The design of the solid state blanker is presented in detail along with tests performed on the completed system. Electromagnetic compatibility of the unit with the working environment is considered in the design and in the special construction techniques employed.

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The design and construction of a high level noise blanker and RF amplifier system as used in RFI measurement work is presented. This RFI work is part of the "Shipboard RFI in UHF SATCOM" project sponsored by Naval Electronic Systems Command. The system requirements are discussed providing a basis for deriving the system specifications. The design of the solid state blanker is presented in detail, along with

tests performed on the completed system. Electromagnetic compatibility of the unit with the working environment is considered in the design and in the special construction techniques employed.

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I. INTRODUCTION

In July 1975, the Naval Postgraduate School in Monterey, California received a charter from PME 106 of the Naval Electronics Systems Command in Washington, D. C. to investigate and report on "Shipboard RFI in UHF Satcom." This project was headed by Associate Professor John E. Ohlson in the Department of Electrical Engineering.

The project was prompted by a need to have a definitive study made on the UHF electromagnetic environment aboard surface ships of the U.S. Navy. The charter specifically included the frequency bands expected to be used by the Fleet Satellite Communications System, when that system became operational.

Upon receipt of the charter to investigate shipboard RFI, no knowledge existed among the interested parties as to whether similar studies had been previously conducted at UHF. It was also apparent that "RFI" had to be defined for the purpose of the investigation. RFI, Radio Frequency Interference was defined as interference from any of the following phenomena:

a. Interference from high powered radars or communications transmitters transmitting on the same band of frequencies.

b. Broadband noise such as noise from motors or industrial noise observed within the UHF Spectrum.

c. Harmonic distortion with the UHF Band

$$F_{harm} = n\ F_{fund}\ ;\ n=1,2,...$$

d. Intermodulation Product Distortion

$$F_{imp} = m\ F_{fund_1} \pm n\ F_{fund_2}\ ;\ n,m = 1,2,...$$

Once RFI was defined, literature searches were undertaken to determine to what extent the UHF environment aboard surface ships had been characterized. Although several studies [Refs. 1,2,3] indicated that the HF environment was well documented and could be analyzed, little information was found concerning the specifics of the UHF environment.

The conclusion was reached that no studies existed which adequately characterized the UHF environment aboard surface ships. This conclusion indicated that to accomplish the project charter some method of documenting the UHF electromagnetic environment was necessary. Specifically, a knowledge of noise power as a function of frequency was needed. Additionally, knowledge of the characteristics of the noise would be required. This knowledge would enable investigators to recommend some solution to overcome deleterious RFI, if such RFI existed. Several forms of documentation would be desirabl for analysis and correlation. These decisions led to the design of the instrumentation package as shown in Fig. 1-1.

The test instrumentation consists of a superhet receiver with high level noise blanking in the RF section of the receiver. The following discussion is made in reference to Fig. 1.1.

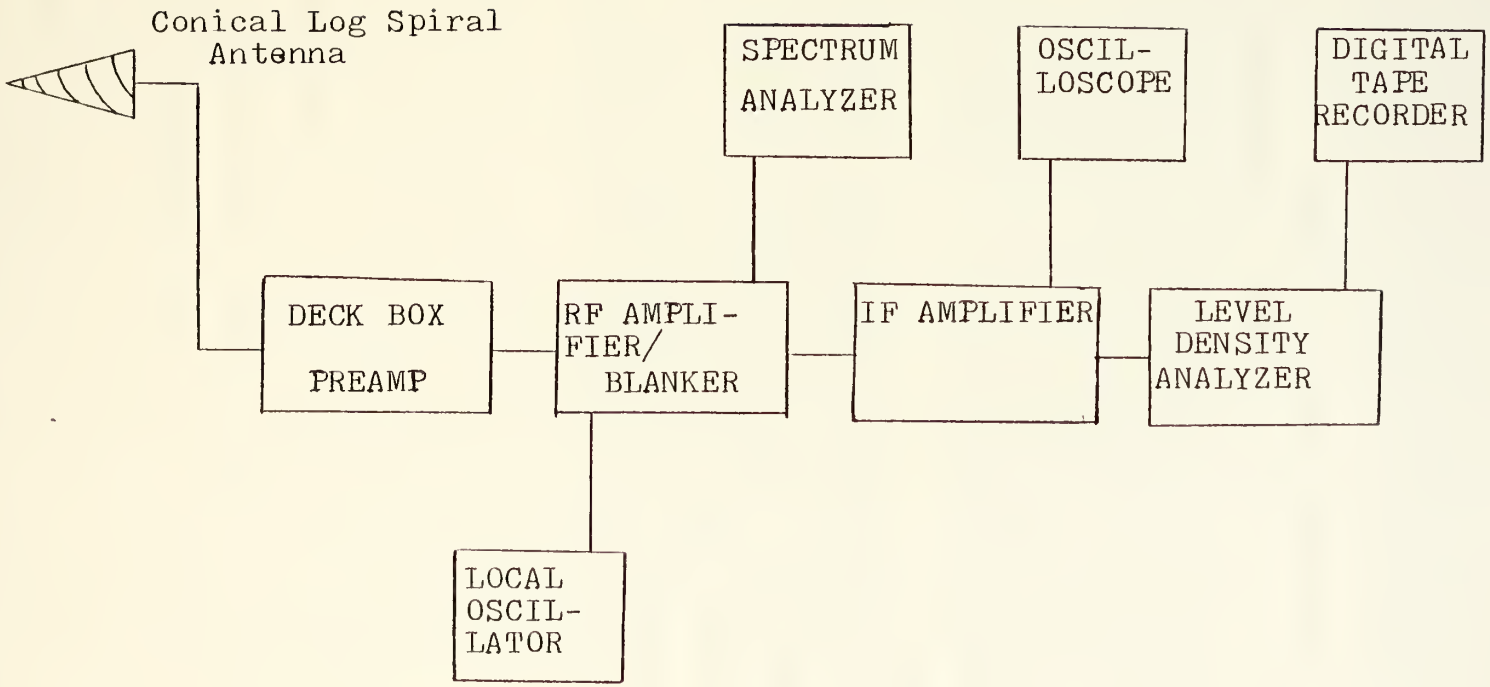


Figure 1.1. RFI Measurement Test Instrumentation Package Block Diagram

The UHF environment is sampled through a conical logarithm spiral antenna. The electromagnetic energy intercepted is preamplified in the Deck Box and transmitted via coaxial cable to the RF Amplifier/Blanker Unit. The RF energy is down converted to a signal with center frequency of 30 MHz. The 30 MHz signal can be further filtered by narrow band filters in the IF Amplifier. The signal is also converted to a video signal and supplied to various output devices. The methods of documenting the UHF environment are by photos of time based and frequency based displays. Digital tapes of the probability density of noise power vs. frequency are also produced.

The RF Amplifier/Blanker Unit had to be compatible with the other units in the instrumentation package. This paper constitutes the documentation of the work performed in designing the RF Amplifier/Blanker Unit. Included also are the construction, testing, and calibration phases.

II. GENERAL RF AMPLIFIER/BLANKER SPECIFICATIONS

This chapter presents the preliminary analysis leading to formulating the general specifications of the RF Amplifier/Blanker Unit.

A. FUNCTION OF BLANKERS

Preliminary analysis of the expected environment aboard a surface ship indicated the following. The UHF environment could be expected to be very noisy in terms of harmonics and intermodulation products. Noise was defined as the amount of noise power present that would interfere with a communications signal received from a synchronous orbit satellite transmitting in the UHF band being monitored. The interfering noise power could be expected to be in some direct proportion to the power emitting capabilities of the transmitters on board a ship under test. Noise power could also be expected to vary directly with the power of the emitters on nearby ships that were illuminating the ship under test.

Knowledge of the existence of the interference in terms of absolute noise power, relative power with respect to the ambient noise, and spectral content would be desirable. The receiver system that would process the information had limits in its dynamic range. If the receiver was made sensitive enough to "look" at low power interfering signals than "high power" interfering signals would cause receiver saturation or

overload. Saturation lockup would prevent gaining present information and would, in addition, distort the information gained. It was decided that a circuit that would eliminate or blank the high level noise before it could cause saturation would be desirable.

B. BLANKER DESIGN CONSIDERATIONS

The design of the blanker circuitry required consideration of the following questions.

1. Several radars contain "pretrigger" circuitry for blanking receivers. Would these circuits serve for blanking the test instrumentation?
2. If pretrigger blanking was not desirable, how fast could blanking be effected?
3. What level must be exceeded before blanking should be initiated?
4. In what section of the receiver should the blanking be accomplished?
5. What should the bandwidth of the noise be that require blanking?
6. How much attenuation of the high level signals would be accomplished by blanking?
7. What external controls of the blanker would be necessary to make the blanker useful?

The use of pretrigger circuits was considered impractical for the following reasons. High powered radars all have some form of pretrigger pulse for blanking applications; however, the format of the pretrigger would probably not be standard

among the different radar types. Pretrigger outputs would contain no information concerning some emitters that might cause saturation, e.g., a nearby ship illuminating the test ship. The pretrigger output might not be accessible at the location of the test instrumentation during testing.

The decision to not attempt to use pretrigger circuits for blanking led to analysis of how fast blanking could be accomplished and how much energy would be detrimental to test results. Blanking speed would be a function of the response of the blanking control circuit. Utilizing TTL integrated circuits would enable the control circuit to have a response of nanoseconds. Use of a delay network would provide a means of delaying high level noise energy from reaching the IF Amplifier section until blanking could be effected.

It has long been accepted that high Q circuits have a tendency to ring when pulsed with high level noise pulses or spikes. These pulses or spikes are wide band and when mixed with a local oscillator for down conversion to IF create additional noise in the IF Amplifier. For these reasons blanking would be more efficient in the wide band front end of the RF Amplifier section.

The noise power expected in the front of the system could range from -90 dBm in a quiet environment to as much as +10 dBm in a noisy environment. This range obviously exceeded the dynamic range of the receiver system. Rather

than establish one power level that would initiate blanking, it was recognized that the blanking threshold should be variabl

The receiver bandwith would be variable, depending on the operating mode. In some modes of operation the RF Amplifier bandwidth would be as much as 170 MHz centered about 320 MHz. In other modes, the bandwidth would be narrowed to 32 MHz with a center frequency ranging across the UHF band from 240 MHz to 405 MHz. The blanking channel was designed to work with either a 10 MHz or a 1 MHz frequency bandwidth. If the noise power in that bandwidth exceeded the level that was predetermined to be detrimental to test results, blanking would be initiated.

The ambient noise could be expected to be as low as -90 dBm and the receiver's dynamic range to be about 60 dB. The preamplification of approximately 30 dB in the Deck Box (see Fig. 1.1) placed the operating range of the receiver from -90 dBm to -30 dBm. The blanker would need to be designed to operate on signals within 10 dB of the receivers' sensitivity. If the interference from high powered sources could expectably exceed 10 dBm the blanker must attenuate by at least 40 dB to stay within the limits of the receivers range.

The above answers to the initial questions gave some indications to what controls would be required for viable operation of the blanker system. External control of the blanking threshold, noise power bandwidth, and some disabling control would be required. Additionally it was decided that

some form of an inverting circuit would be useful. The inverting circuit would cause the blanker to blank the receiver until the noise exceeded a predetermined threshold. Knowledge of the duty cycle of the blanker would be useful in determining what coding schemes might be used to combat RFI. It was also decided to count the number of times the blanker blanked during a selectable time period.

C. BLANKER DESIGN SPECIFICATIONS

The considerations of the previous section led to the following general specifications for the design of the blanker.

Specification I

The blanker must have a variable threshold blanking level ranging from +10 dBm to -80 dBm as seen at the input of the RF Amplifier.

Specification II

There will be enough blanking delay in the RF Channel so that the blanking occurs before the high level RF signal reaches the IF Amplifier.

Specification III

The Blanking Channel will have a selectable bandwidth and this will be tunable over the UHF range of 240 MHz to 405 MHz.

Specification IV

Blanking is to be accomplished by attenuating the RF signal or noise by a minimum of 80 dB.

III. BLANKER SYSTEM BLOCK DIAGRAM AND DISCUSSION

Chapter three is a discussion of electronic blankers in general followed by a discussion of the RF Amplifier/Blanker Unit. This Unit is discussed under two sections. One section is a discussion of the RF channel. This channel is in series with the electronic switches used to blank high level noise signals. The other section concerning the RF Amplifier/ Blanker Unit discusses the Blanking Channel. The Blanking Channel processes the high level noise and provides control of the electronic switch in the RF Channel.

A. ELECTRONIC BLANKERS

Electronic blankers may be operated at RF or IF. The same principles apply in either portion of the receiver. Two paths exist for electromagnetic energy to follow. One path, the RF signal path, may consist of some amplification and some delay and an electronic switch. The other path consists of circuitry for processing a signal, making a decision based on the level of the signal, and control of the electronic switch that is in the RF signal path.

Refer to Fig. 3.1 for the following discussion. RF energy coming into the system is split into two channels. The RF Amplifier provides gain and improves the noise figure of the system. The Delay Line has a delay of τ seconds which correspond to the delay experienced in the overall alternate channel. The Blanking Channel has some selective

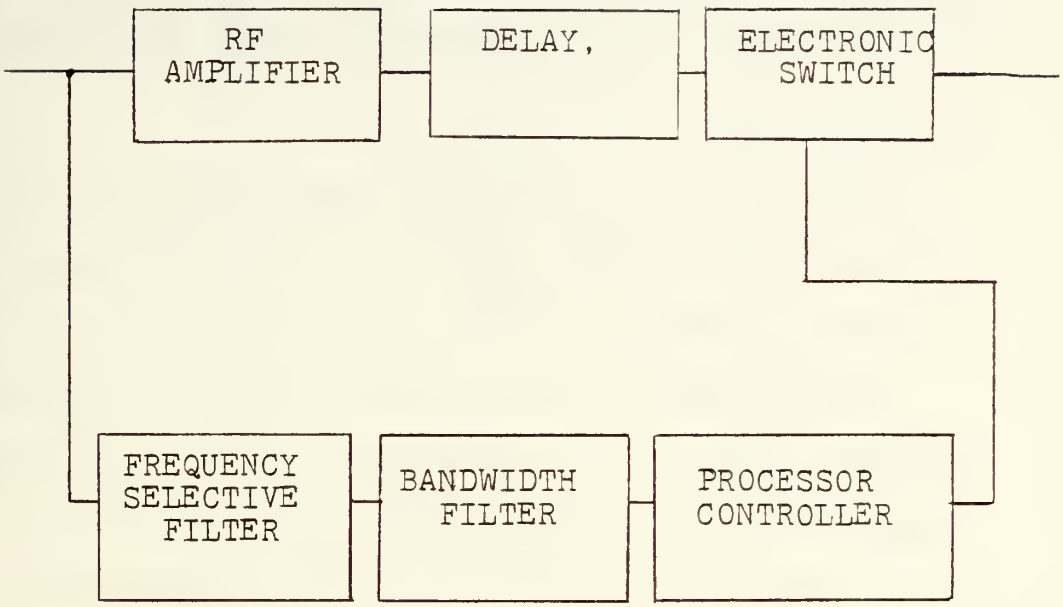


Figure 3.1. Blanker Configuration

filtering. It also has some processing circuitry. The circuitry determines the status of the electronic switch. The electronic switch provides either a continuous path for the RF energy, or an interrupted path, thus blanking the system

B. RF CHANNEL

Figure 3.2 is an accurate representation of the RF Channel of the RF Amplifier/Blanker Unit. The following discussion is made in reference to Fig. 3.2.

The RF input to the unit can be applied directly to a bandpass filter or can be preamplified in a 10 dB gain amplifier. The bandpass filter has a bandwidth of 195 MHz and a center frequency of 320 MHz. Immediately following the filter is a +20 dBm limiter. This limiter is a safety measure used to protect against extreme transients in power that may be experienced. A variable attenuator calibrated in 10 dB steps provide some control over the RF signal levels which are next incident upon a power splitter. The RF Channel goes from the power splitter through a series of amplifiers and delay lines to a pair of coaxial switches. These coaxial switches are connected together as a double pole double throw switch. The proper amount of amplification and delay are switched into the RF Channel to correspond with the different bandwidths of the Blanker Channel.

The delay lines are used for timing. The series amplifiers are used to keep the noise figure low while maximizing the dynamic range of the channel. The delay line consists of coiled coaxial cable, RG223. This coaxial cable has a

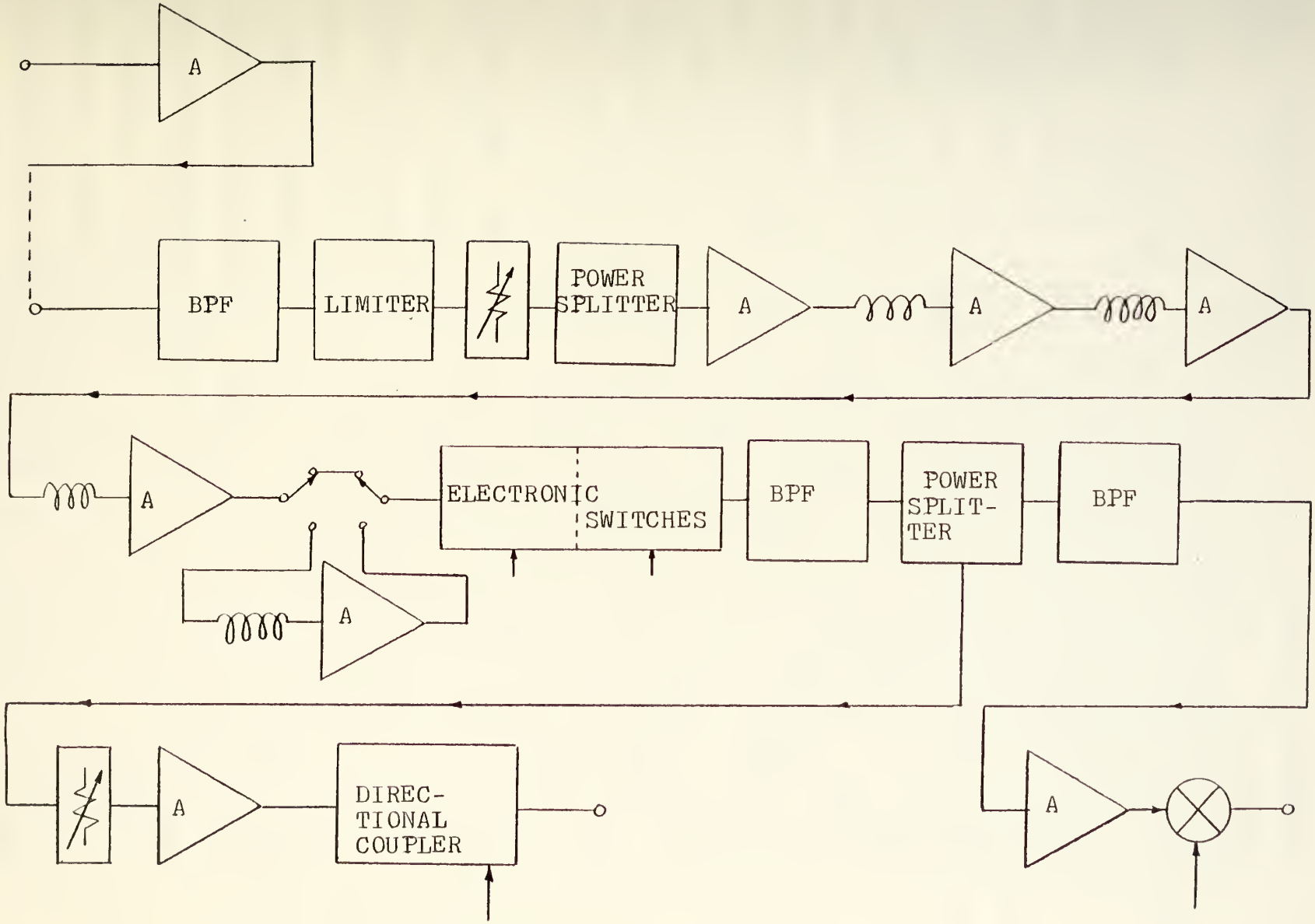


Figure 3.2. RF Channel

propagation constant of 0.714 x c, or a delay of about 142 nsec/100 ft. Calculations in Appendix A show the amount of delay necessary for the system.

Following the coaxial switches, the RF Channel is connected to the electronic switches, MS1 and MS2. If these two switches are both closed the RF Channel is completed through to another bandpass filter and to a power splitter. When blanking is occurring, the two switches MS1 and MS2 are considered to be open. In actuality the RF Channel is being attenuated by 106 dB. The bandpass filter following the electronic switches has a bandwidth of 182 MHz and a center frequency of 320 MHz. It is to provide filtering against the possibility of noise pick up through the control circuit for the blanker switches.

Coming out of the second power splitter the RF Channel diverges. One path is through another variable attenuator, a 28 dB gain amplifier, a directional coupler and to a test point. This test point allows access to the RF spectrum for display on a spectrum analyzer or oscilloscope.

The other RF Channel from the power splitter goes through another bandpass filter with a center frequency of 320 MHz and a bandwidth of 195 MHz. This filter keeps spurious harmonics of the local oscillator from reaching the test point discussed above. The RF Channel then goes through a 12 dB gain amplifier to a mixer. The local oscillator input to the mixer is 30 MHz lower in frequency than the frequency that will be analyzed in the IF Amplifier. The difference frequency of 30 MHz is taken from the mixer and connected to the IF Amplifier Unit.

C. BLANKING CHANNEL

Refer to Fig. 3.3 for the following discussion of the Blanking Channel. The RF energy comes from the power splitter in the front end of the RF Amplifier Unit through a 10 dB gain amplifier. This amplifier is used to obtain amplification and to isolate the RF Channel from the local oscillator. The RF is then applied to a mixer with the local oscillator input frequency 30 MHz lower than the frequency of interest in analysis. The Blanking Channel is tuned to a center frequency of 30 MHz. The channel has a bandwidth of either 10 MHz or 1 MHz depending on operation of an external switch. The RF signal, now down converted to 30 MHz, is bandpass filtered through a 10 MHz bandwidth filter, then is amplified in a 9.5 dB gain amplifier and applied to the coaxial transfer switch. The transfer switch allows the selection of additional selectivity in the noise bandwidth. A 1 MHz bandwidth filter may be inserted in series with the attenuator which then connects to the logarithmic amplifier.

The two choices of bandwidth in this channel also introduce the possibility of two different time delays being necessary in the RF Channel. The time response of a filter is approximated by the reciprocal of the bandwidth of the filter. A 10 MHz filter has a time response of about 100 nsecs. A 1 MHz filter has a time response of about 1 microsec.

The logarithmic amplifier has the characteristic that the output of the amplifier varies with the logarithm of the input. This characteristic provides the capability of

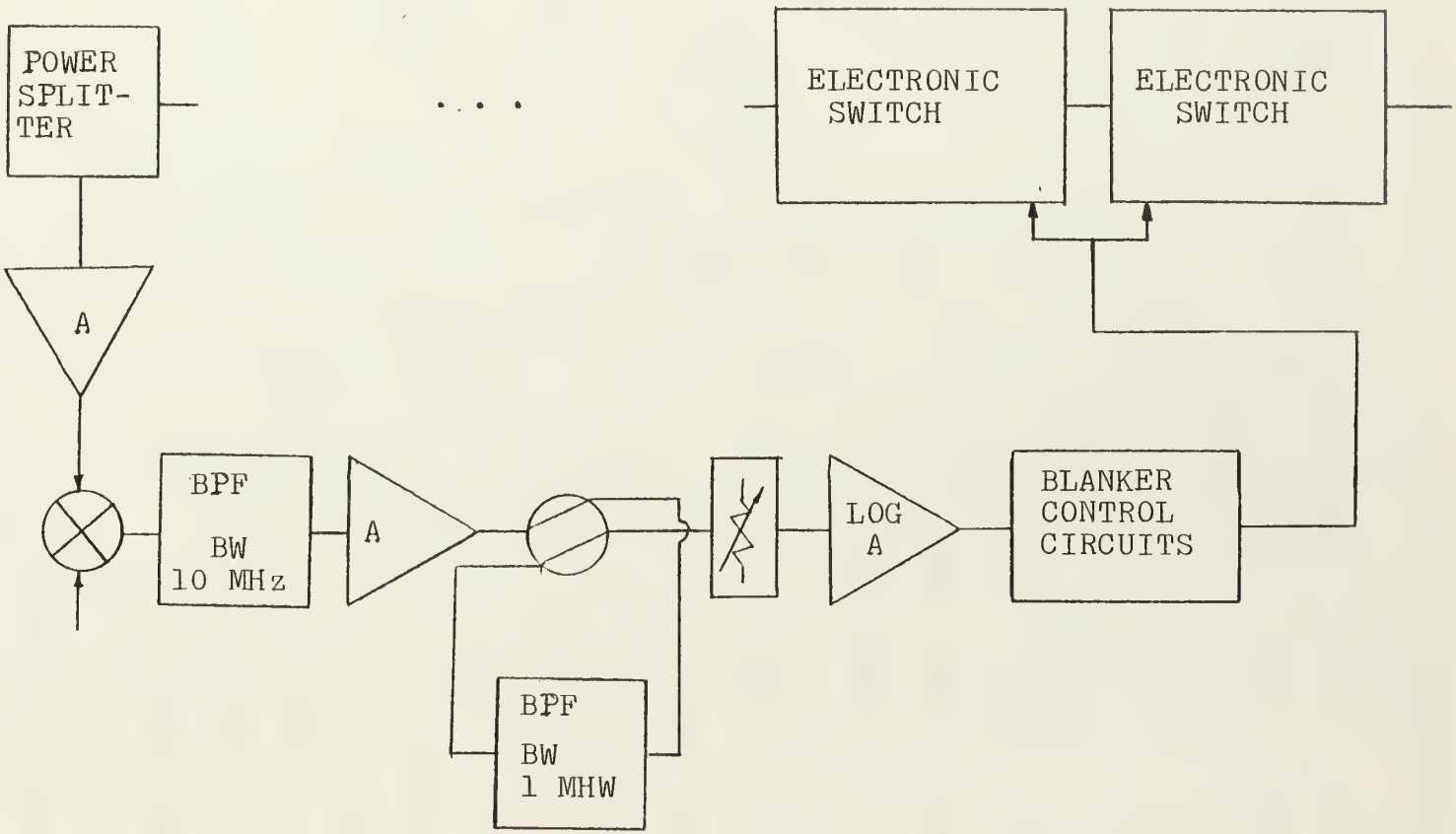


Figure 3.3. Blanking Channel

$$V_{out} = K_1 + K_2 \log V_{in}$$

extending the range of operation of the amplifier. The output of the logarithmic amplifier is taken from the video output and is applied to the Threshold Comparator Circuit.

The Threshold Comparator, some pulse shaping circuits, and driver circuits then control the status of the electronic switches, MS1 and MS2. The discussion of these circuits is the subject of Chapter 4.

Figure 3.4 is included here as a comprehensive view of the entire RF Amplifier/Blanker Unit in block diagram form.

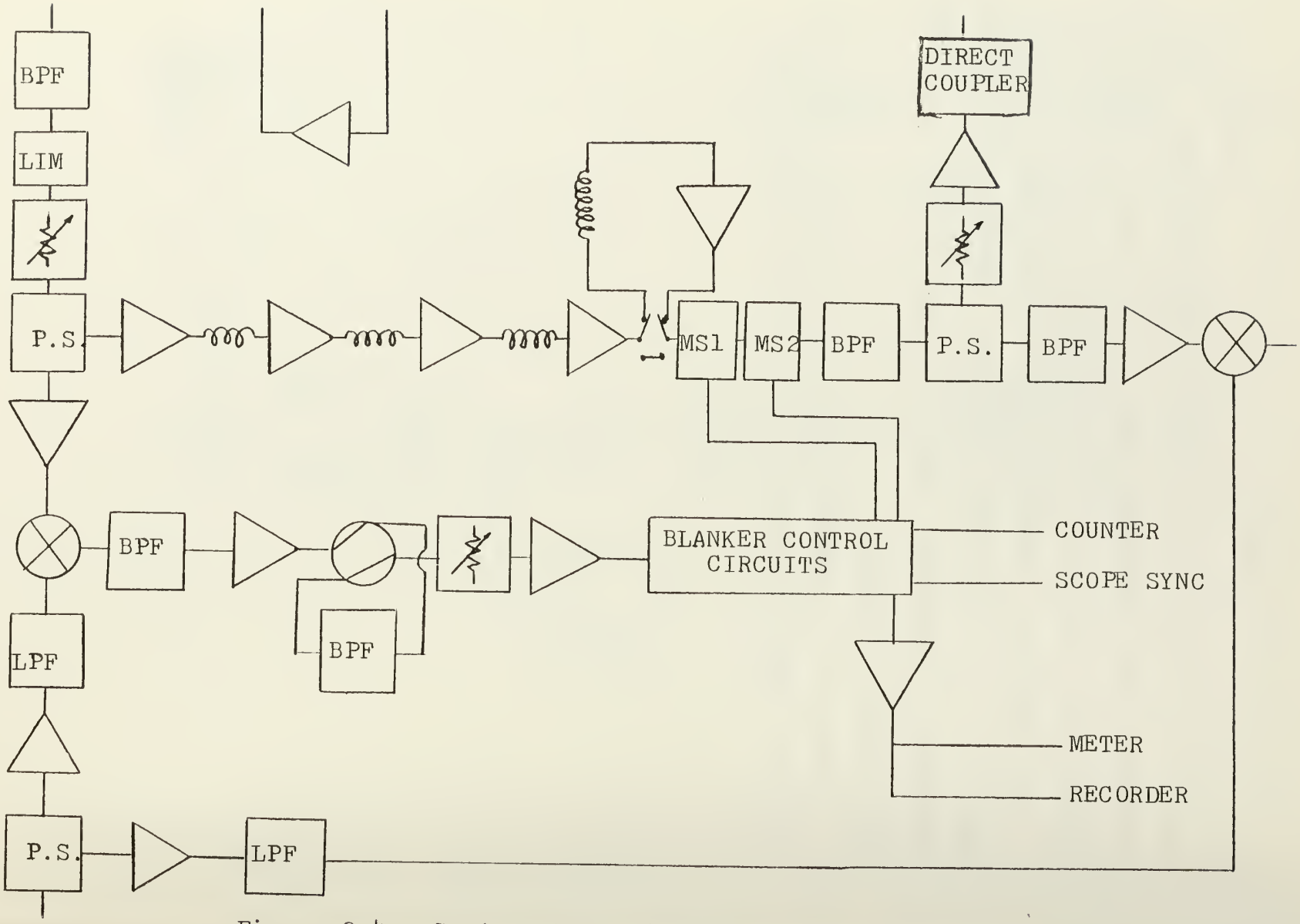


Figure 3.4. System Block Diagram

IV. BLANKER CONTROL CIRCUITRY

The Blanker control circuitry consists of several individual integrated circuits cascaded together on one printed circuit board. The individual circuits are listed below:

1. Threshold Comparator
2. Pulse Width and Shaping Circuit
3. Inverting Gate and Duty Cycle Averager
4. Dual Line Blanking Drivers
5. Counter and Sync Pulse Driver

These circuits are discussed under their respective sections. Appendix D provides a comprehensive view of the Logic from input to output of the control circuitry. Included also is a discussion of the double balanced mixers used as electronic switches for blanking. The photograph in Fig. 4.12 may be referred to for an understanding of the integration of the above circuits.

A. THRESHOLD COMPARATOR

The Threshold Comparator is designed about a Signetics 527 Analog Voltage Comparator [Ref. 4]. The circuit produces a rapid transition from the 0 to 1 state or the 1 to 0 state when the analog input varies about a preselected comparison level. Transition time is less than 20 nsec. The circuit has an "in phase" and a reversed phase" output polarity voltage. The Threshold Comparator is shown in Fig. 4.1.

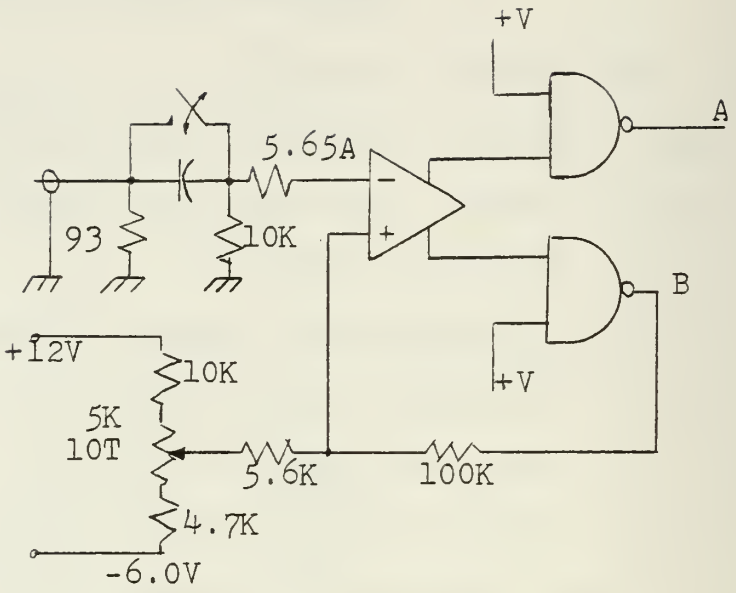


Figure 4.1. Threshold Comparator

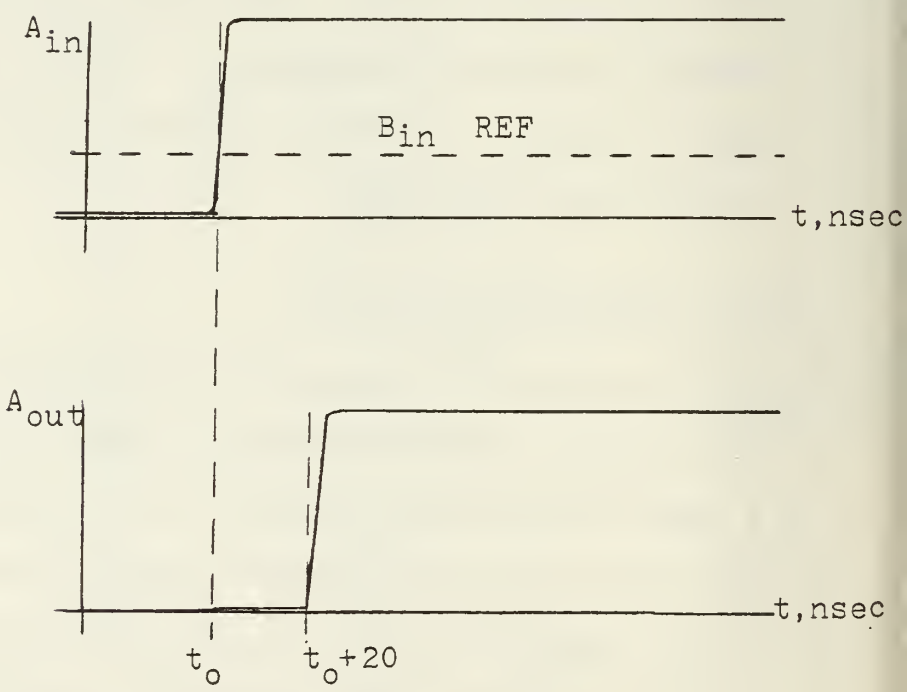


Figure 4.2. Comparator Waveforms

The Blanker Level Adjust potentiometer is located externally to the RF Amplifier/Blanker Unit for accessibility. It is a 10 turn, 5Kohm, precision potentiometer. A voltage divider network is employed to set the voltages at either end of the potentiometer to +2.86v and -1.7v. The voltage on the wiper of the potentiometer is the input comparison voltage to the inverting input of the IC circuit. This input is modified by the hysteresis feedback discussed on page 32. The other input to the comparator is the video output from the logarithmic amplifier discussed in Chapter 3. The video signal input voltage is variable between 0v and 2.2v at a rate of 28mv/dB. The "A" output of the comparator follows the "A" input if the reference voltage, the "B" input is exceeded. Refer to Figs. 4.2, 4.3, and 4.4.

The "B" output is the reversed phase of the "A" input. The comparator is operated as a high gain circuit that is in either of two states, logical Zero, "0" - 0.5v or logical one, "1" - 3.0v.

The following paragraphs are used to describe the hysteresis feedback utilized for noise immunity in the Threshold Comparator. The Blanker Level Adjust is set to some arbitrary reference voltage, V_{ref}, that corresponds to some noise level, L_{dBm}. Table IV provides the necessary information to determine what setting is required to blank any arbitrary noise level. If $V_{Ain} > V_{Bin}$ blanking is initiated.

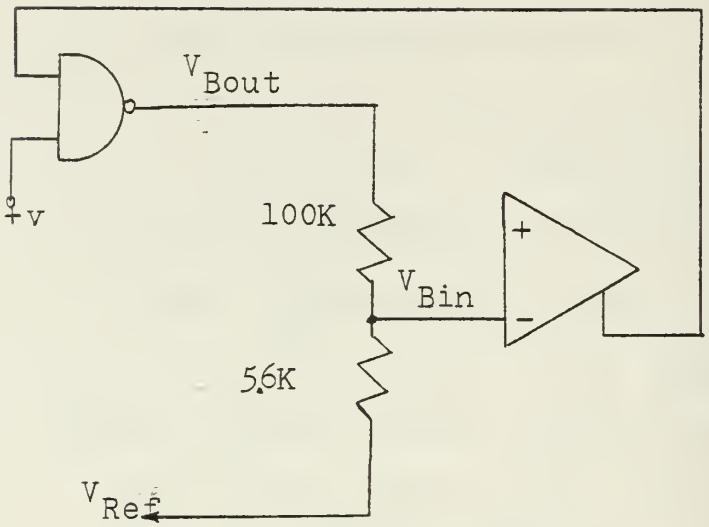


Figure 4.3. Hysteresis Feedback

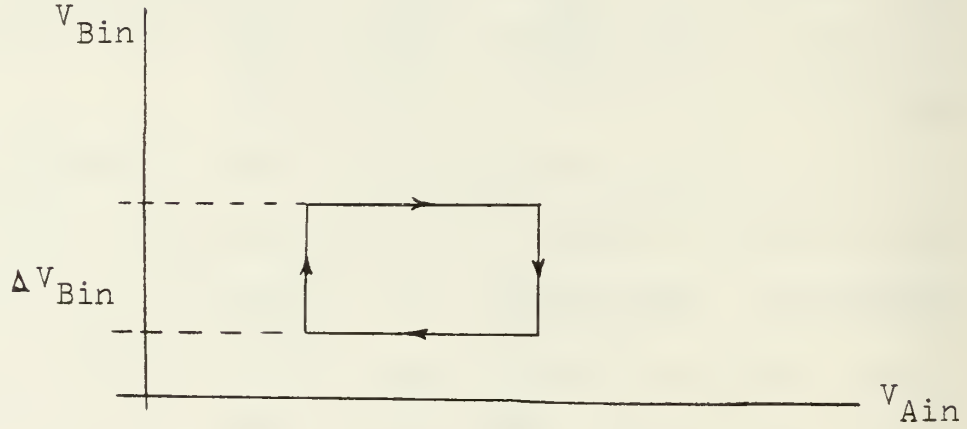


Figure 4.4. Hysteresis Loop

To prevent minute changes in V_{Ain} from causing changes in the blanking, noise immunity is provided [Ref. 5].

$$V_{Bin} = (V_{Bout} - V_{Ref})(5.6K\ )/(100K\ + 5.6K\ )$$

$$V_{Bin} = 0.053\ (V_{Bout} - V_{Ref})$$

If $V_{Ain} > V_{Bin}$ then V_{Bout} transistions from "1" to "0" and

$$\Delta V_{Bin} = V_{Bin}\text{"1"} - V_{Bin}\text{"0"}$$

$$= 0.053\ \ (V_{Bout}\text{"1"} - V_{Ref}) - (V_{Bout}\text{"0"} - V_{Ref})$$

$$= 0.053\ \Delta V_{Bout}$$

$$= 0.053\ (3.0-0.5) = 0.132v$$

The output of the logarithmic amplifier is 28mv/dB of input. Therefore 0.132v corresponds to 4.7dB of hysteresis.

The "A" output is directly connected to the input of two OR gates for pulse width and pulse shaping control.

B. PULSE WIDTH AND SHAPING CIRCUIT

The analog comparator circuit connects directly into the Pulse Width control circuit. The Pulse Width Control circuit is an OR gate whose output is connected to an RC network and switch as shown in Fig. 4.5.

The OR gate is a Signetics 7432 quad OR gate. Logical one, "1," is 3.0v, and logical zero, "0," is 0.2v [Ref. 4].

The pulse width control's purpose is to extend the blanking pulse to keep the blanker engaged for the entire time a

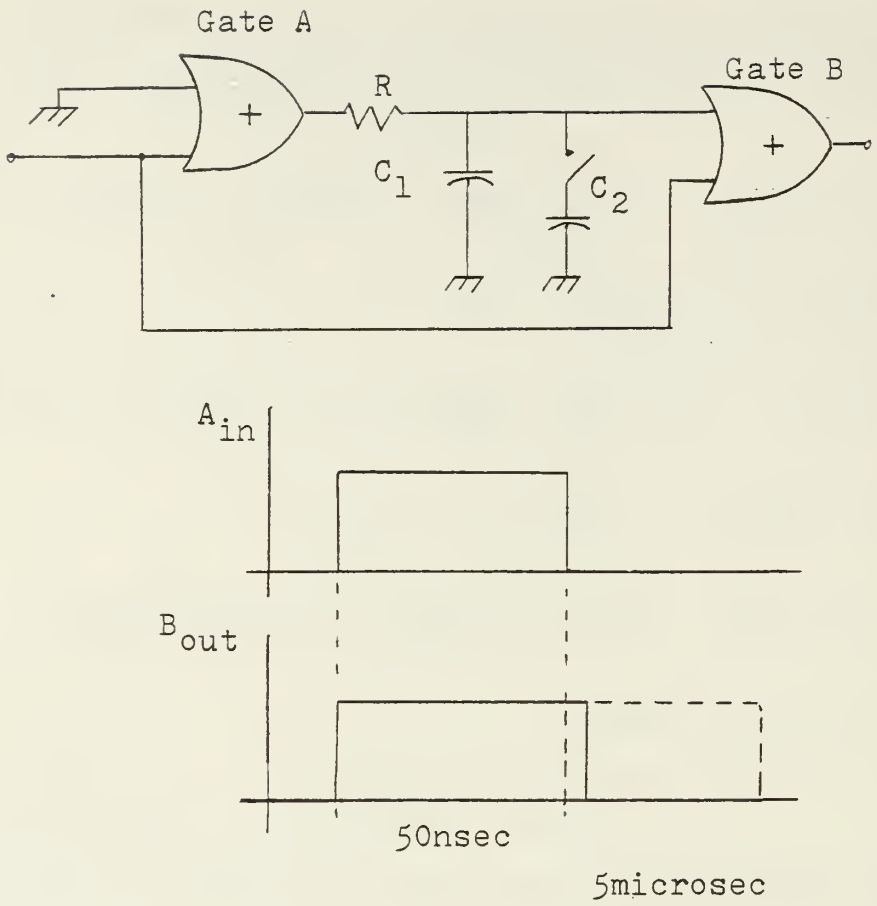
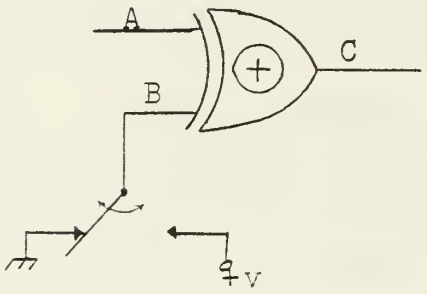


Figure 4.5. Pulse Width and Shaping Circuit



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Figure 4.6. Inverting Circuit

high level noise exists. Due to expected inaccuracies in tabulated time delays or small changes in the characteristics of the Blanking Channel, the Blanker timing may not be completely accurate. This circuit extends the time of blanking and allows for the different responses of the 10 MHz and 1 MHz filters. Refer to Figure 4.5 for the following discussion.

Gate B will transition from an output "0" state to the "1" state if either input voltage V_{Bin} 0.8v. V_{Bin} will be greater than 0.8v as long as the Threshold comparator has a "1" output state. Additionally, Gate A causes capacitor C_1 (and C_2 if selected) to charge to V_{out} of 3.0v. When the Threshold Comparator output goes to "0," V_{out} of Gate A switches to 0.2v.

The following equations are given to show the time delay created by the RC network.

$$V_c(t) = 3.0 \exp\left(-\frac{t}{RC}\right)$$

$$V_c(t_1 = 0.8v) = 3.0 \exp\left(-\frac{t}{RC}\right)$$

$$t_1 = RC \ \ln 3 - \ln 0.8$$

$$t_1 = 1.32\ RC$$

Choose R = 390 ohms, C_1 = 100 pf, and C_2 = .01μf and the two time extensions of the blanking pulse are t_1 = 50nsec and t_2 = 5.6 microsec.

Gate A is used to isolate the RC network from the Threshold Comparator. Gate B provides logic, "1", when either input or both inputs are greater than 0.8v.

C. INVERTING CIRCUIT AND DUTY CYCLE AVERAGER

The function of the inverting circuit is twofold. The double balanced modulators used as blanking switches use negative logic. They require 0 v to blank and 3.5v to not blank. The Pulse Width circuit and Threshold Comparator are designed around positive logic. Therefore, the first function of the Inverting Circuit is to invert the logic. An output of 3.0v corresponds to a nonblanking condition. The second function of the inverter is to provide a means of changing the logic externally upon command. In this instance, a time period corresponding to a nonblanking period becomes a time period when the receiver is blanked. This option is provided so that the blanker will not always eliminate the large signals. The choice may be made to analyze the noise created while the large signals are present.

The inverting is done through the use of Exclusive OR Logic. One fourth of a quad Ex-OR Signetics 7486 is utilized [Ref. 4]. Referring to the truth table in Fig. 4.6 it is obvious that the proper switch assignment is all that is necessary for the logic choice desired.

The Duty Cycle Averager is constructed from 1/4 of the 7486 IC used as the Inverting Circuit. The capacitor charges

to the average value of the output of the Ex OR Gate IC used to isolate the Averaging Circuit from the Blanker Drivers. (Figure 4.7 refers).

D. BLANKER DRIVER CIRCUITS

The driving circuits for the double balanced modulators consist of Signetics 8T23B Dual Line Drivers. The drivers are connected into a resistive network which serve as impedance matching and current limiting networks. Refer to Fig. 4.8 for the following discussion.

The 8T23B Driver consists of a dual input AND Gate and a quad input AND gate internally connected into an OR gate (Dot-OR Logic). The output of the IC is 3.5v at 69ma into a 50 ohm load, or 0.15v at -240 microamps in the low state [Ref. 4].

The normal nonblanking condition is with the output at 3.5v forward biasing the diodes in the modulators so that RF coupling between input and output ports exists. This condition is obtained by connecting the dual input and gate to chassis ground through an external panel switch. The output of the Inverting Circuit provides a logical 1 into the quad input AND gate. The output of the Driver is a logical 1 or +3.5v. Removal of the logical 1 input causes the output to go to essentially 0v and blanking occurs. The blanker is disabled (will not blank) by switching the input of the dual input AND gate to a +5.0v supply. This voltage keeps the diodes in the blanker forward biased and blanking will not occur.

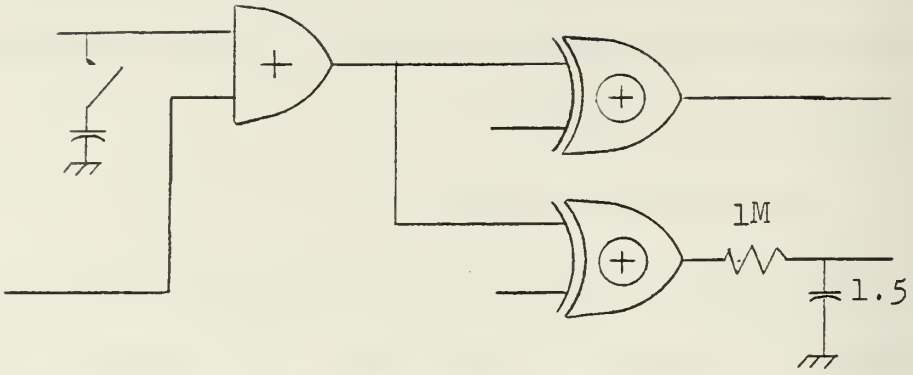


Figure 4.7. Averaging Circuit

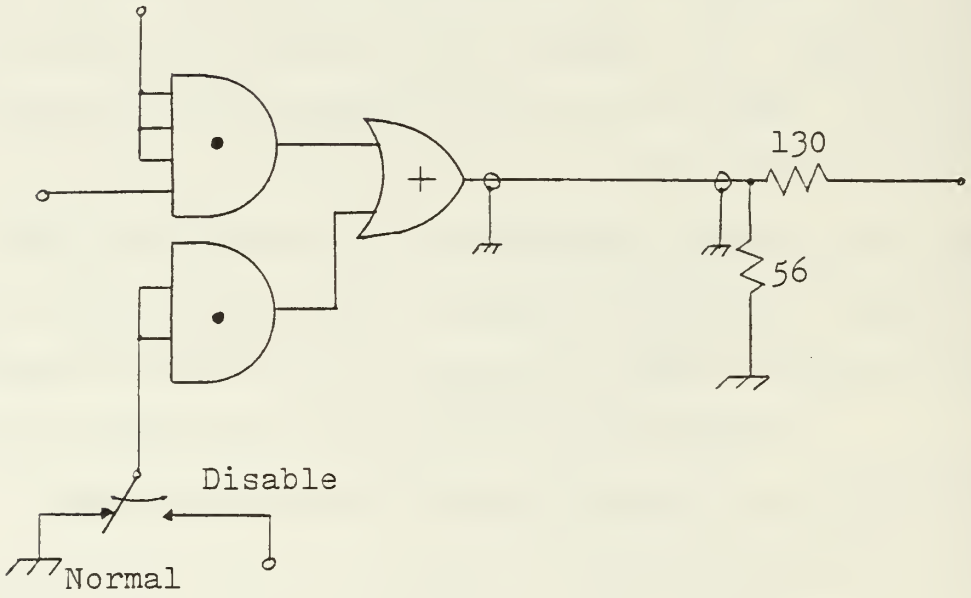


Figure 4.8. Blanker Driver and Disable Switch

The drivers are connected to the two modulator/mixers in the following configuration of Fig. 4.9.

E. ELECTRONIC BLANKING SWITCHES

The two modulators used as switches are connected into the RF Channel in series and are controlled in parallel. Figure 4.10 schematically represents the electronic configuration of one of the mixers used as a switch.

The RF input is applied to the "L" port of the mixer and the output is taken from the "R" port. The control or driving voltage is applied to the "I" port. Referring to Figure 4.10, a control voltage of 0v allows no RF path from "L" to "R." The attenuation at UHF is about 55dB for a typical modulator of the ZLW-1WH model used in the RF Amplifier/Blanker Unit. The application of a positive voltage forward biases the diodes and RF is coupled across from "L" to "R." With a control voltage of 3.5v applied to the resistive network the current flowing in the diode circuit is about 10 ma. The attenuation under this condition is 4.5 dB insertion loss.

F. COUNTER AND SYNC PULSE DRIVER

The usage of a sync pulse was anticipated to synchronize an oscilloscope presentation to the blanking pulse. The ability of being able to count the blanking pulses also seemed desirable.

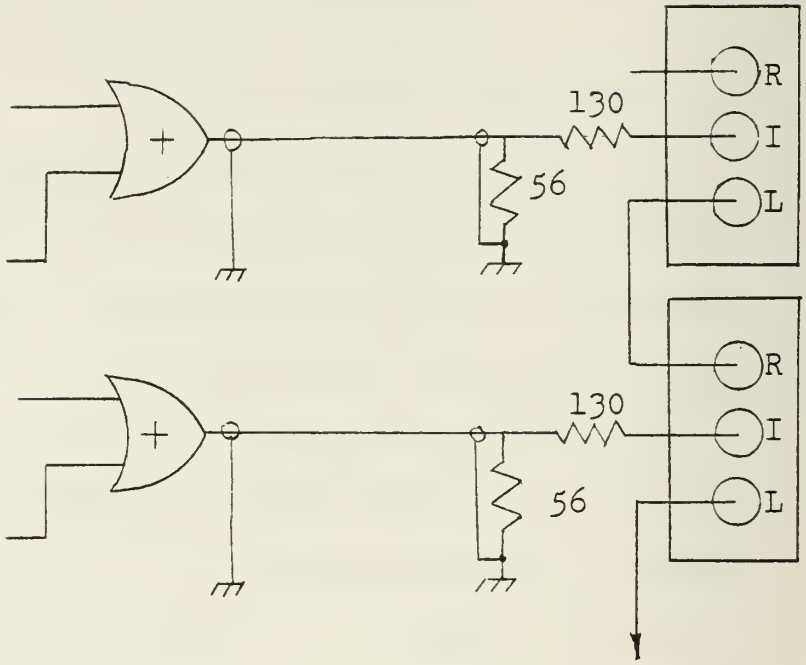


Figure 4.9. Blanker Switch--Driver Interconnections

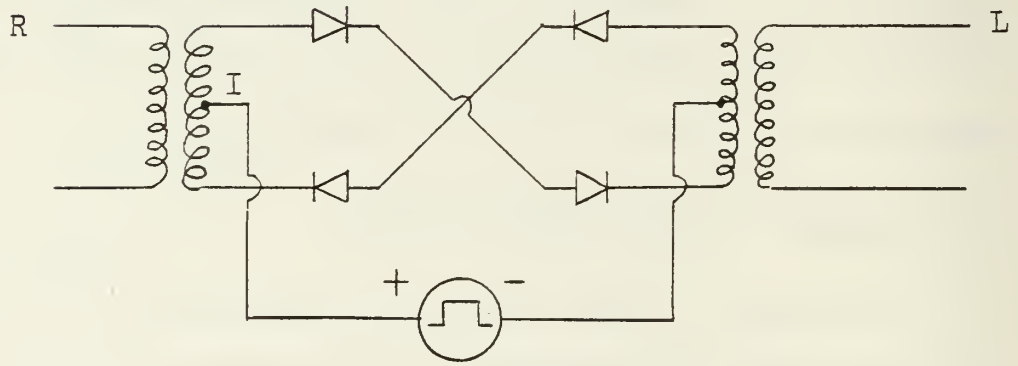


Figure 4.10. Blanker Switch

The counter was already constructed in the Level Density Analyzer but was constructed from CMOS circuitry. This required a counting pulse greater than 6v to trigger the CMOS counter. The Signetics 8T15 Dual Line Driver was chosen for both functions. The 8T15 output is one of two states. One state is +12v output and the other is -12v output. Refer to Fig. 4.11 for the following discussion.

During the time the blanker is not normally activated, the input to the NAND gate is a logical 1. The output of the NAND inverter is also a "1" or +12v. This is the input to the oscilloscope sync circuit as well as into the second NAND gate. The output of the second NAND gate is also a "1." When the blanking pulse occurs, the cascaded NAND gates change states. This provides a negative sync pulse and a negative pulse to the CMOS counter. A diode protection circuit is across the counter to short the negative output from reaching the counter. When the blanking pulse terminates, the transition back to a positive output from the drivers capacitively couples a positive count pulse to the counter. Therefore the counter counts at the end of each blanking period. The sync pulse can be used to sync on either the start or the end of a blanking period.

Figure 4.12 may be referred to as a summary view of the circuitry discussed above.

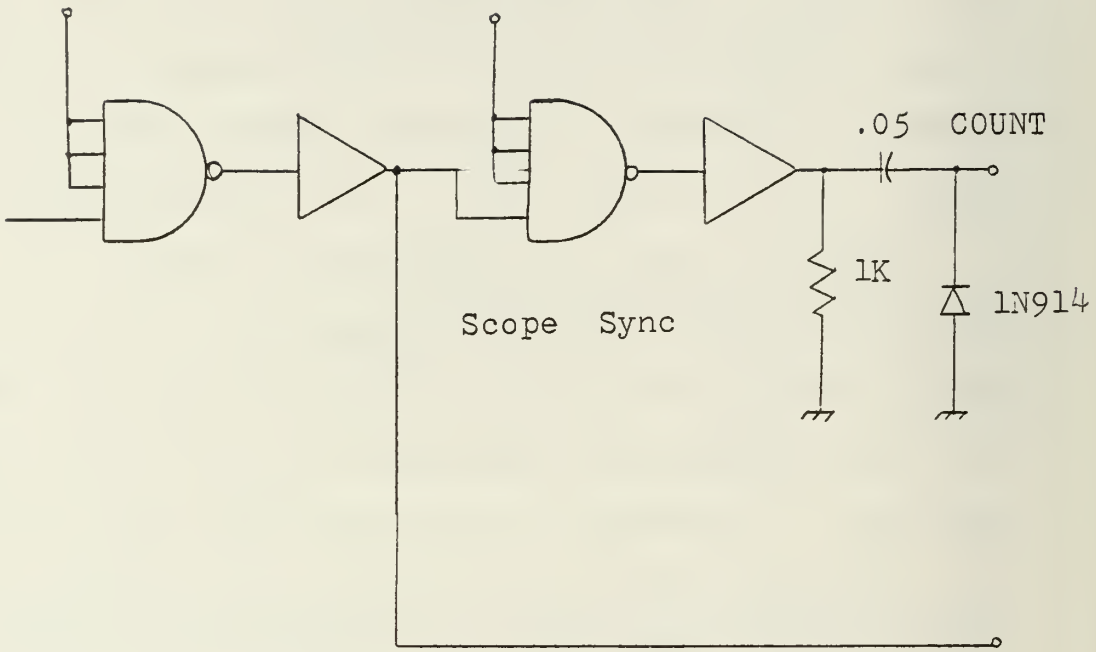


Figure 4.11. Counter and Sync Pulse Driver

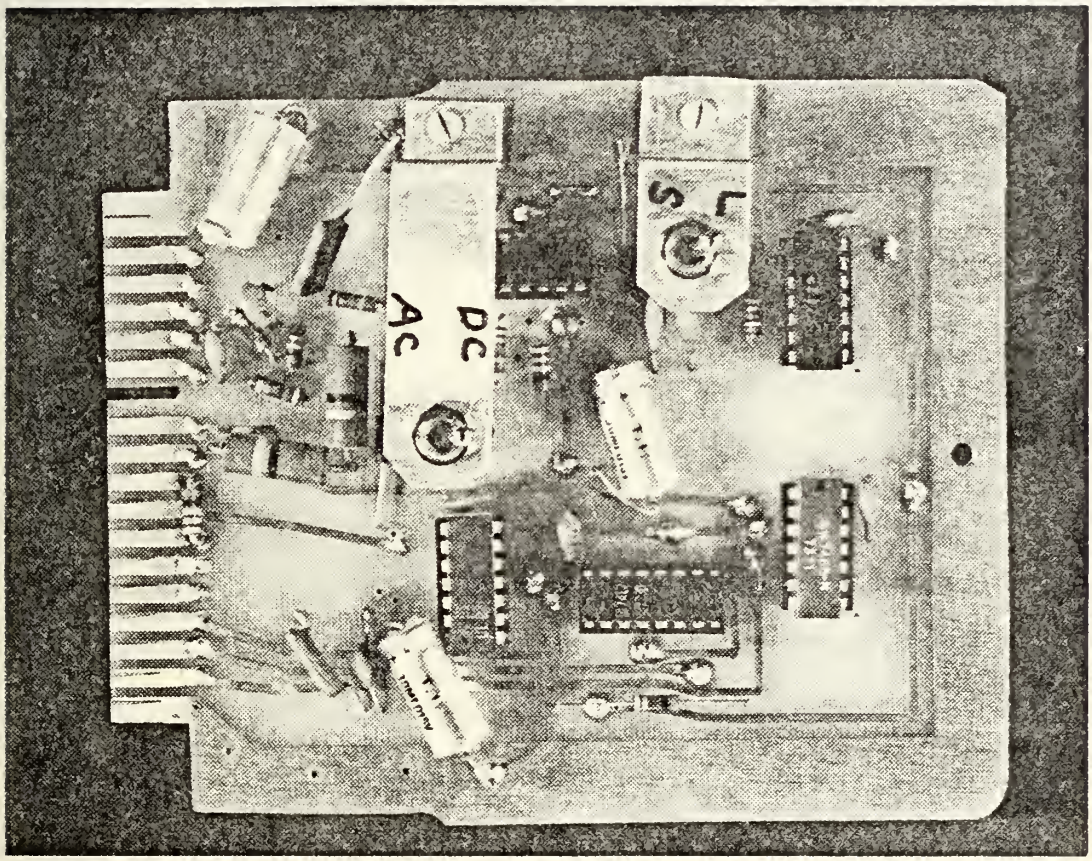


Figure 4.12. Photograph of Blanker Control Circuits. A8B1 Contents

V. DUTY CYCLE CIRCUIT

A typical radar could be expected to produce RFI at a periodic rate up to 300 Hz. These RFI signals could be expected to have a pulse width of 200 microsecs or less. With these known characteristics it appears logical to assume that a blanker operating on these signals would have similar characteristics. Knowledge of the Off-On interval of the blanker was considered essential if accurate data was to be obtained.

A 200 microsec pulse occurring at a rate of 300 Hz has a duty cycle of 200 microsec/(1/300) sec x 100% = 6%. Most radars have somewhat smaller duty cycle and could normally be expected to be operating between 0.1% and 10.0%.

The Duty Cycle Circuit discussed in this chapter is designe to provide a visual display of the blanking circuit's duty cycle on a meter. A voltage output is also available for connection to a strip chart recorder for a more permanent record of the duty cycle.

A. DUTY CYCLE AMPLIFIER

It was decided most adequate to build a circuit that had three ranges of operation. One range would give an output proportional to 10% to 100% duty cycle. Another range would be between 1% and 10%. The third range would be between 0.1% and 1%.

The circuit of Fig. 5.1 is a selectable gain dc amplifier. The output voltage is applied across a microammeter in series with a current limiting resistor. The amplifier is calibrated so that when the input range is exceeded the amplifier reaches saturation. The limiting resistor sets the current through the meter to cause full scale deflection as the amplifier reaches saturation.

The amplifier consists of two stages of LM308 op amps cascaded together as a dc amplifier. The overall gain is 5, 50, or 500, depending on the position of switch A6S4. The three positions of A6S4 are 100%, 10%, 1% full scale deflection. The input to the circuit is 2.4v when the blanker is blanking and about 0v when it is not blanking.

In the 100% full scale deflection position, A6S4 connects the inverting input of A6A1A2 to ground through a 100 Kohm resistor. The second stage, A6A1A2, is operating as a fixed gain amplifier. The overall system gain is adjusted by A6A1R1. These adjustments are considered in more detail in Chapter 8 under Calibrations.

In the 10% full scale position A6S4 connects the inverting input of A6A1A2 to ground through a 2 Kohm trimmer potentiometer. The first stage gain has been set in the 100% full scale deflection position. The resistor A6A1A2 is adjusted for full scale deflection in the 10% position.

Similarly, the resistor A6A1R3 is adjusted to cause full scale deflection when A6S4 is set to the 1% full scale position.

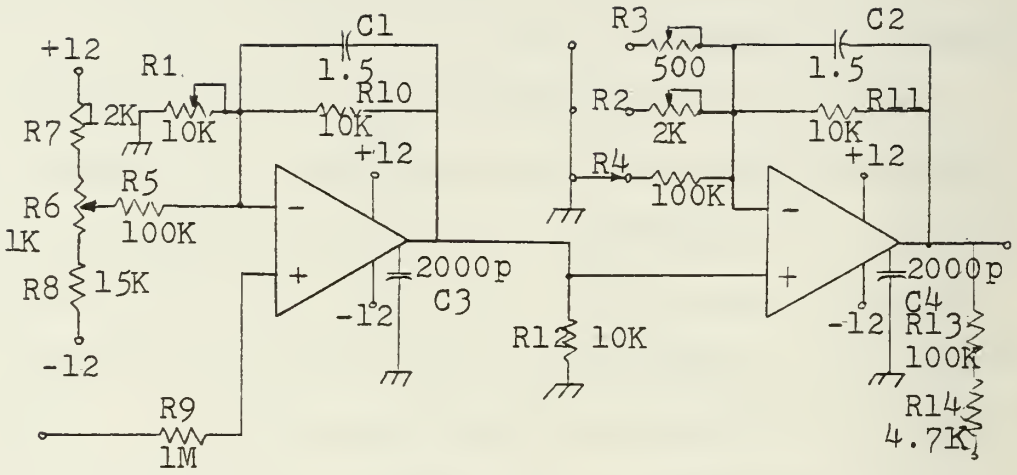


Figure 5.1. Duty Cycle Amplifier

The divider network A6A1R6, A6A1R7 and A6A1R8 are used for zero adjustment. This adjustment is made when the input to the amplifier corresponds to a no-blanking signal.

B. METER AND RECORDER OUTPUT CIRCUITS

Figure 5.1 showed the output of the amplifier connected to a microammeter. The maximum voltage output from A6A1A2 is +12v. A6A1R13 is used to set the saturation current through the meter to cause full scale deflection. The metering circuit is shown in Fig. 5.2.

The voltage output of A6A1A2 is also taken directly from the amplifier to an output jack in the rear of the RF Amplifier/Blanker Unit. This provides an external output for use with a strip chart recorder.

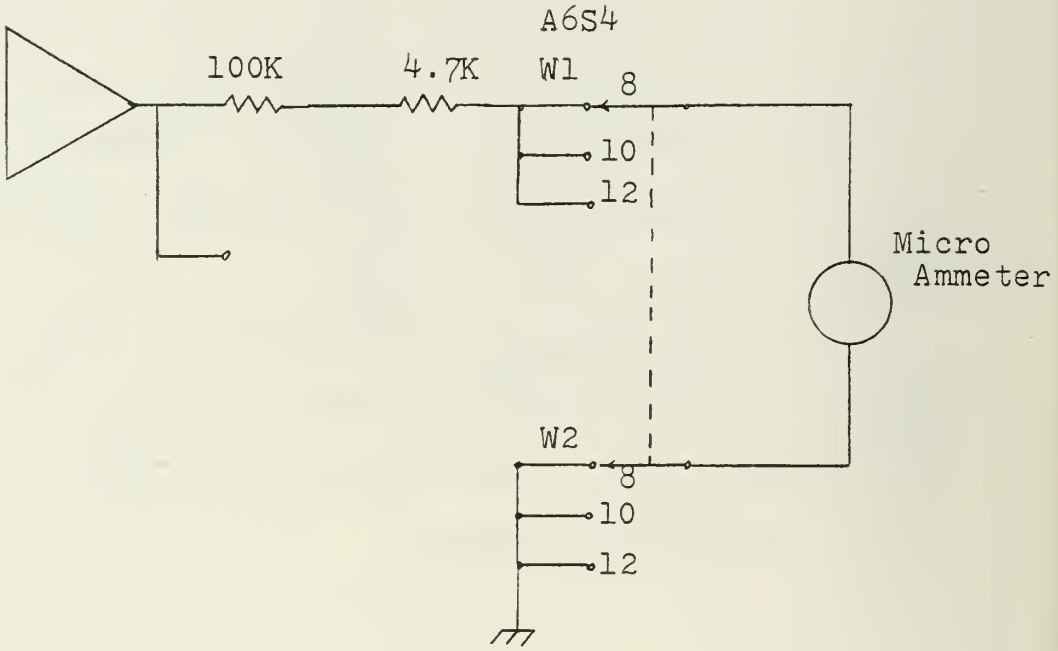


Figure 5.2. Meter and Recorder Output

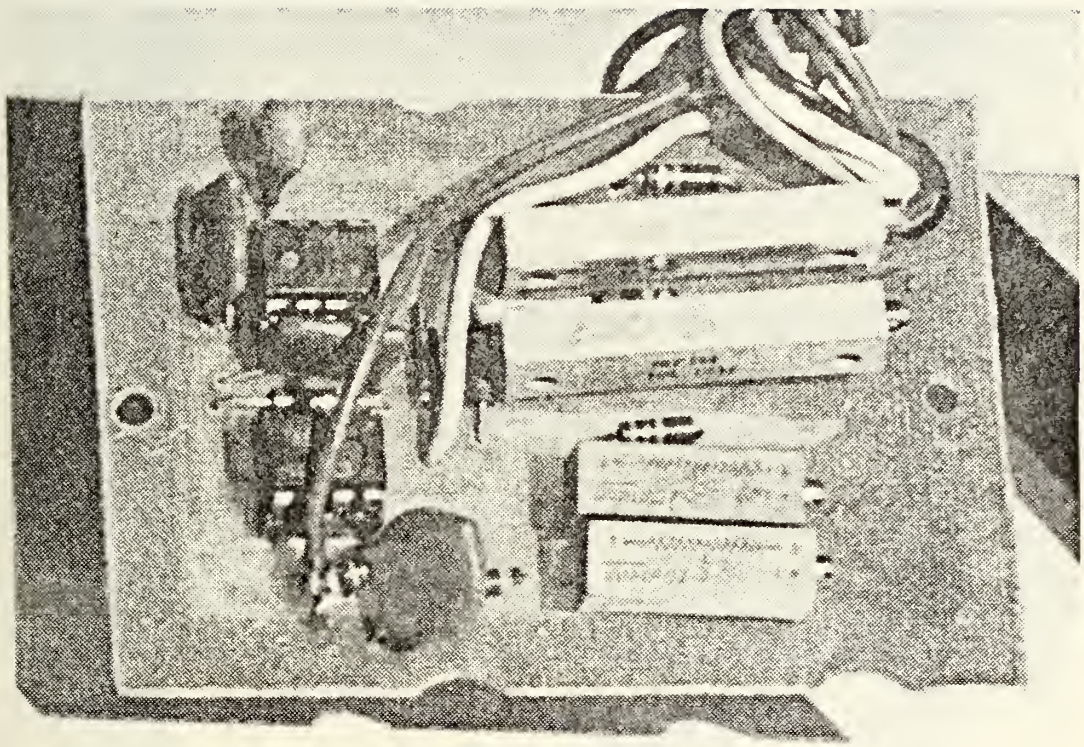


Figure 5.3. Photograph of Printed Circuit and Components, A6A1

VI. ELECTROMAGNETIC COMPATIBILITY

The purpose of building the test instrumentation was to enable investigators to characterize the UHF environment. This UHF characterization would be constructed from the data collected. The test equipment must not distort the data unnecessarily, and any distortion must be recognized as such.

The subject of Electromagnetic compatibility is too lengthy to discuss here. This chapter is devoted to stating those construction techniques employed to combat distortion due to incompatibility of the equipment in the environment.

A. ELECTROMAGNETIC SHIELDING

The RF Amplifier/Blanker Unit was encased in an aluminum equipment case. This case was not completely RFI shielded as the panels that mounted on a frame were not gasketed, or constructed of finger stock. There existed a certain amount of shielding however and care was taken to not violate that amount. All access holes through the exterior were shielded on the inside by use of smaller aluminum boxes. Because exterior wiring could act as an antenna at the UHF frequencies all wiring was decoupled by passing through RFI feedthrough capacitors at the metal interface. Refer to Fig. 6.1 for shielding of the DC power cable.

Electromagnetic shielding was considered in purchase of all modular components. Manufacturer specifications were

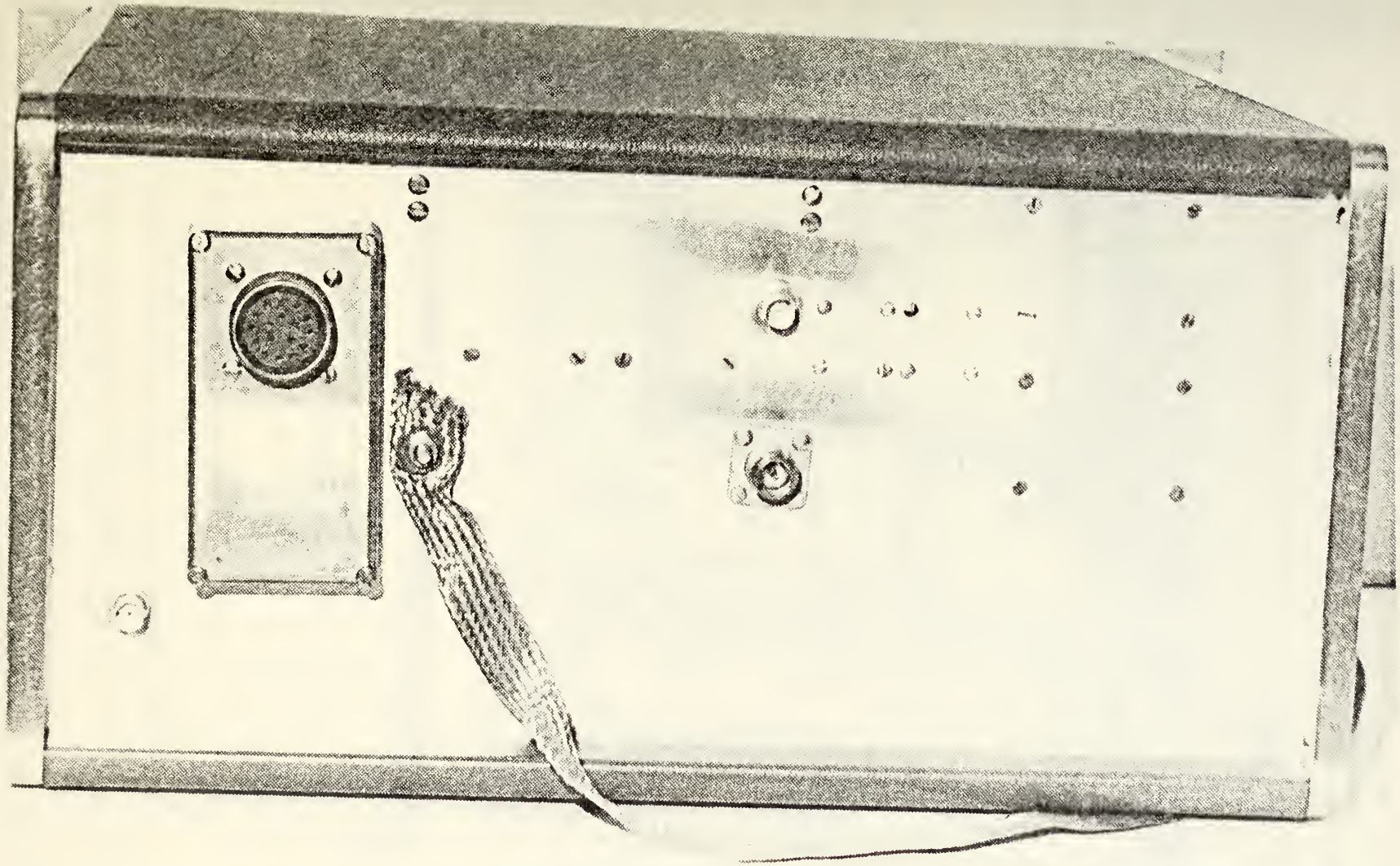


Figure 6.1. Rearview of RF Amplifier/Blanker Unit Showing Bonding and Shielding Techniques

referred to when making component choices. The RF signal path was constructed from semi-rigid 0.141 coaxial cable. The coaxial cable is constructed from tinned copper and is soldered at the coaxial fittings. The solid shielded line placed a near perfect ground around the RF path which made it theoretically almost free from RFI except at the input or output ports of the shielded system. Figure 6.2 shows the RF path as semi-rigid coax connecting modules which are also shielded by the manufacturer, usually in aluminum.

The delay line consisted of 510 feet of coiled RG 223. To further maximize the shielding of the delay line, aluminum foil was wrapped around every 100 feet of cable as it was placed on the containing reel. This double shielded, woven strand cable was tested for crosstalk prior to its use. The output of a signal generator was set for +20 dBm output at 300 MHz, and connected to several coils of RG 223. The other end of the coiled cable was left as an open circuit to create standing waves. Another piece of RG 223 was connected to a spectrum analyzer through about 40 dB of amplification. This cable was positioned about the coiled cable for a maximum of crosstalk which was then observed to be 150 dB lower then the transmitted power.

All logic circuitry was encased in an aluminum box of 0.1875 inches thickness. This accomplished at least 90 dB of attenuation on any radiating transients caused by the fast switching circuits. This calculation is shown in Appendix E.

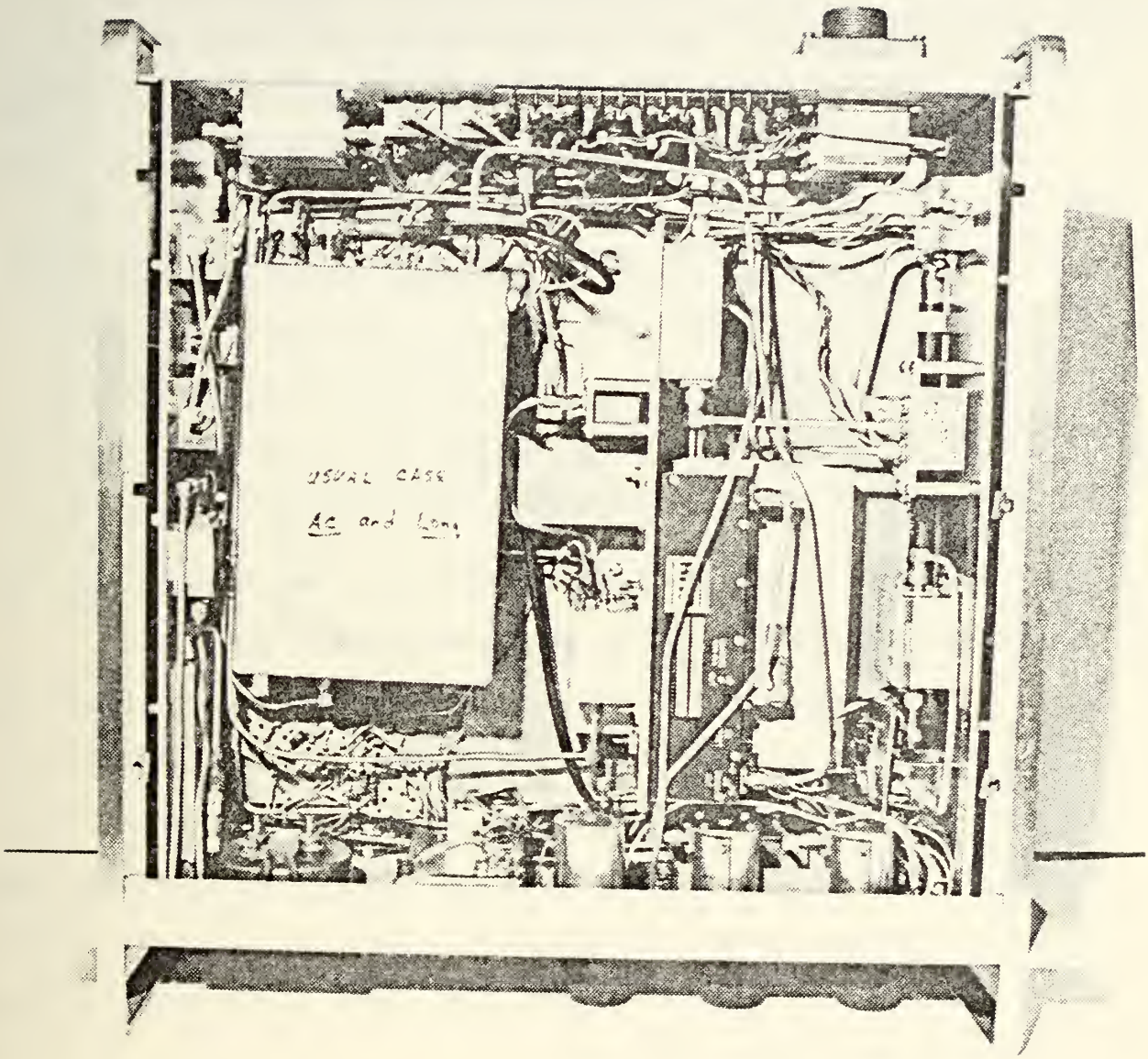


Figure 6.2. Internal Shielding Techniques

B. FILTERING

The DC power supplies were physically located in the IF Amplifier Unit. The interconnecting cable was shielded and connected to the RF Amplifier/Blanker Unit by a screw-type Cannon Plug. The individual wires each connected to a section of a 12 section RFI filter capacitor.

The operator controlled switches mounted on the front panel were connected to power supply wires in the same manner. The small box containing the RFI capacitor was mounted over the switch and bolted onto the inside of the exterior panel. The RFI capacitor acted to decouple any UHF from entering into the interior of the Unit as well as decoupling any RFI being generated inside the box.

The printed circuit boards had several large valued capacitors connected to the current sources. These capacitors served to prevent large amounts of transient current from being forced to flow in the power cables, which would appear as antennas at these frequencies. Each IC also had decoupling capacitors mounted physically close to the chip to decoupl RF from the power sources.

All DC connections to the Blanker Control circuitry were made through RFI feedthrough capacitors. Ferrite toroidal beads were placed on the wires at the metal interfaces to act inductively against transients. The ferrite beads were also placed over the power cables to the individual active modules, i.e. amplifiers.

C. GROUNDING AND BONDING

The circuitry of the RF Amplifier/Blanker was referenced to chassis ground. This ground was connected to system ground. Ground loops were avoided where possible by using a single ground as reference point. All other grounds were then connected to this ground at 5TB1. The printed circuit boards had ground planes about 1/2 inches wide for accessibility. The RF Amplifier/Blanker Unit was bonded to the other pieces of test equipment by a 1 inch braided strap. This strap was then connected to the system ground which was the ships' hull in those instances where measurements were aboard ship.

VII. CONSTRUCTION

This chapter is meant as a technical guide to the physical construction of the RF Amplifier/Blanker Unit. It consists mainly of diagrams, photographs, and schematic representations This Unit has been modularized and each component is identifie by its modular identification.

A. BREADBOARD MODEL

The RF Amplifier/Blanker was breadboarded together in essentially the same configuration as the completed version. The breadboard model was not encased in a box but was mounted on a plywood base for mechanical rigidity. RF signal connections were made utilizing RG223 with crimp-on connectors of SMA type. Teflon coated wires were used to make the DC power connections. A front control panel similar to the final panel was constructed of aluminum. Preliminary testing and operatin experiments showed the design to be sound with one major exception. Originally, the blanker switches were designed as PIN Diode Switches manufactured by General Microwave Corp. This choice was made because these switches had a response of 20 nsec and attenuation of about 40dB each at the UHF under investigation. Operation of the switches exhibited cross-talk between the control input and the RF signal input that was unacceptable. A 3.0v control pulse capacitively coupled into the RF line as a 3.0v spike of short duration. Refer to Fig. 7.1.

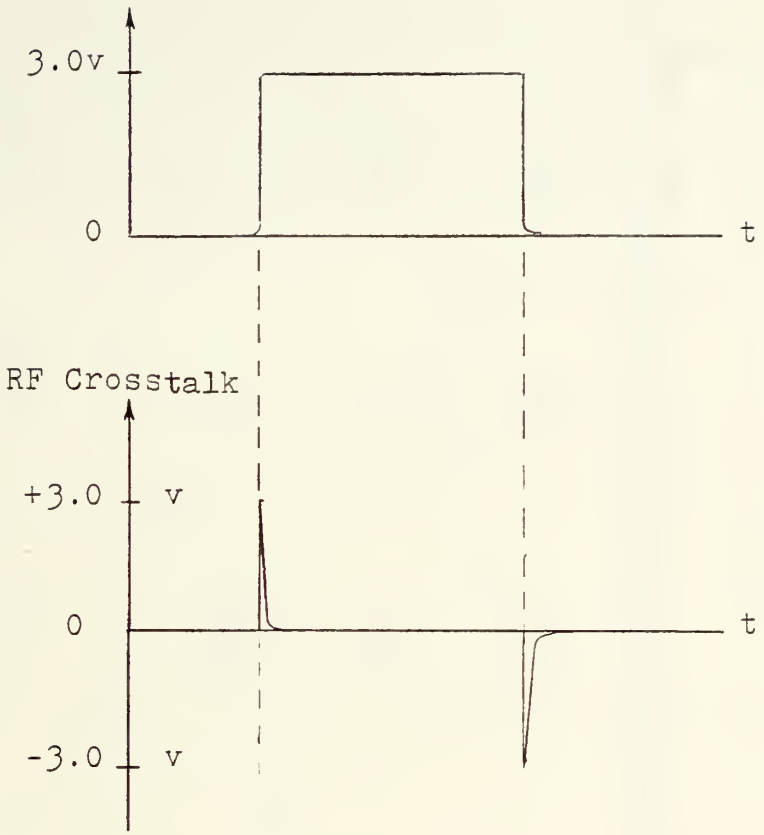


Figure 7.1. RF Crosstalk from Control Voltage

This crosstalk constituted obvious distortion and so a substitution was made with double balanced modulators Model ZLW-1WH manufactured by Mini Circuits Lab. This substitution resulted in almost eliminating crosstalk. The use of ZLW-1WH modulators provided a signficant cost reduction, as well as increased blanking attenuation when blanking.

B. COMPLETED UNIT

The breadboard model was dismantled and reconfigured in the equipment case as the final version of the unit. Figures 7.2 and 7.3 show the Unit in a manner that demonstrate physic layout as well as some of the construction techniques.

The RF signal connections are shielded coaxial 0.141 cabl as discussed in Chapter 6. The component layout was made with accessibility of the components as a primary considerati The components could have been packed more compactly with a loss in the accessibility. The component locations can be readily identified using Appendix F in conjunction with Appendix E.

The top of the delay line serves as the base plate to mount modules A2, A3, and A8B1. Module A1 is located on the inside of the frame on the right side when facing the rear. Module A4 is mounted similarly on the left side and A5 is mounted along the rear panel. The inside of the front panel is designated A6. Module A7 is on an aluminum sheet attached to the under side of the delay line, module A8.

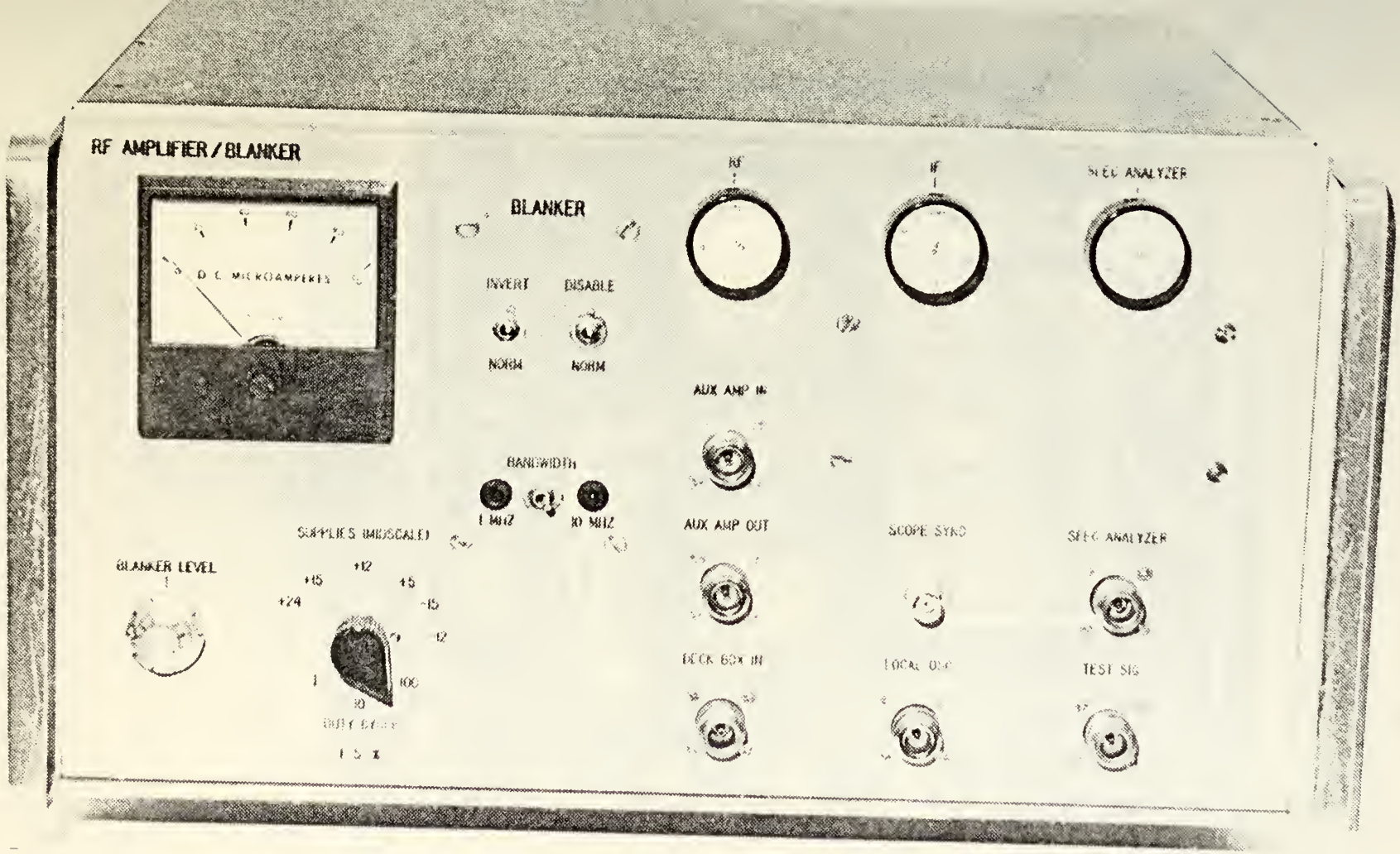


Figure 7.2. Front View of RF Amplifier/Blanker Unit

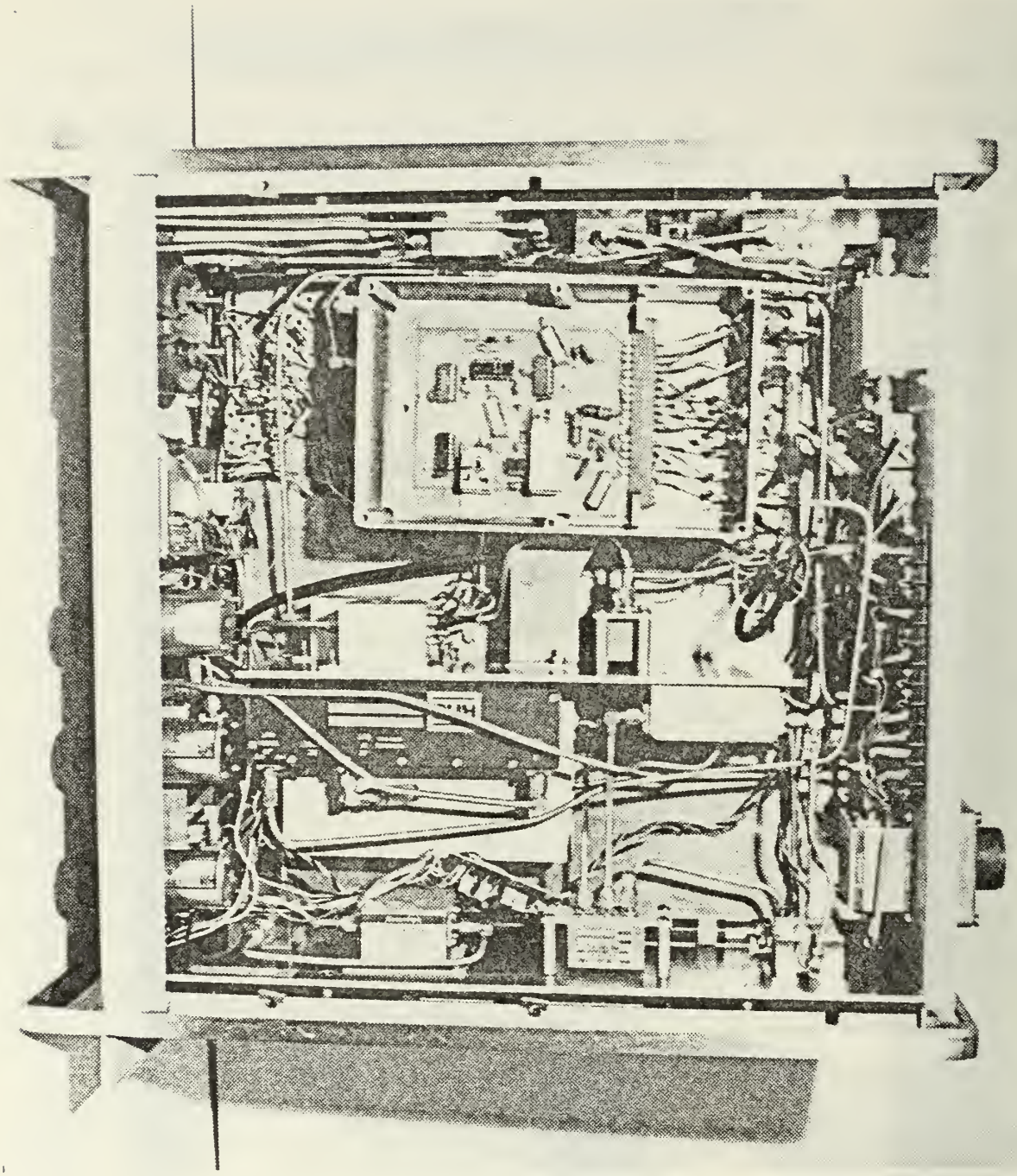


Figure 7.3. Photo Top-Front With Cover Off

The wiring interconnections for the Blanker Control Circuit box (A8B1), the duty cycle circuit (A6A1), the Blanker Bandwidth Switch (A6S3) and the mode selector switches (A6S1, A6S2) and the Indicator Circuits are in Appendix G.

VIII. TESTS AND CALIBRATIONS

This chapter contains some of the characteristics of the RF Amplifier/Blanker Unit. Several tests were made upon completion of construction. These tests are covered in their respective sections.

The calibrations included in this chapter are those calibrations that must be performed after corrective maintenance. These calibrations are not normally a part of the daily routine of data collecting.

A. RF CHANNEL GAIN AND FREQUENCY RESPONSE

The RF Channel gain is tabulated by component in Table I. These tabulated values are only valid at the specified frequency of 320 MHz. The test points listed in Table I.a. may be associated with physically accessible component interconnections by using Appendices D and F. The RF Channel gain was measured from the Deck Box Input (A6J3) to either of two outputs. Test point 26 is the Spectrum Analyzer Output (A6J6) Test point 22 is the IF Amplifier Output (A5J1). To obtain the gain at Test Point 22 the local oscillator was operated at a frequency of 290 MHz with a power output of +9 dBm into Local Oscillator Input (A6J5). Figures 8.1 and 8.2 show the transfer characteristics of the RF Channel.

Note that the gain decreases with an increase in frequency This decrease is due to the attenuation characteristic of the

TABLE I.a. TEST POINTS/GAIN TABULATIONS
FOR RF CHANNEL

This Table may be used in conjunction with Appendices D and F for trouble shooting the RF Amplifier system.

Test Pt.	Gain from previous TP	Accumulative 1 MHz BW Gain	Accumulative 10 MHz BW Gain	Remarks
Input				-50dBm/320 MHz
2	- 0.6	- 0.6	0.6	
3	- 0.5	- 1.1	- 1.1	
4	Variable	--	--	
5	- 3.5	- 4.6	- 4.6	
6	+12.0	7.4	7.4	
7	- 8.0	- 0.6	- 0.6	100ft delay line
8	+12.0	11.4	11.4	
9	- 9.0	2.4	2.4	119ft delay line
10	+10.0	12.4	12.4	
11	- 8.0	4.4	4.4	100ft delay line
12	+10.0	14.4	14.4	
13	- 8.0	6.4	--	100ft delay line
14	- 8.0	- 1.6	--	91ft delay line
15	+12.0	10.4	--	
16	- 0.1	10.3	14.3	
17	- 8.0	2.3	6.3	
18	- 0.5	1.8	5.8	
19	- 3.5	- 1.7	2.3	
20	- 0.5	- 2.2	1.8	
21	+12.0	9.8	13.8	
22	- 5.0	4.8	8.8	IF Output, A5J1
23	- 3.5	1.3	5.3	
24	Variable	--	--	
25	+28.0	29.3	33.3	
26	- 0.1	29.2	33.2	Spectrum Analyzer A6J6

CONDITIONS:

LO Input: 8.5dBm so TPA has +17 dBm for proper mixer level input

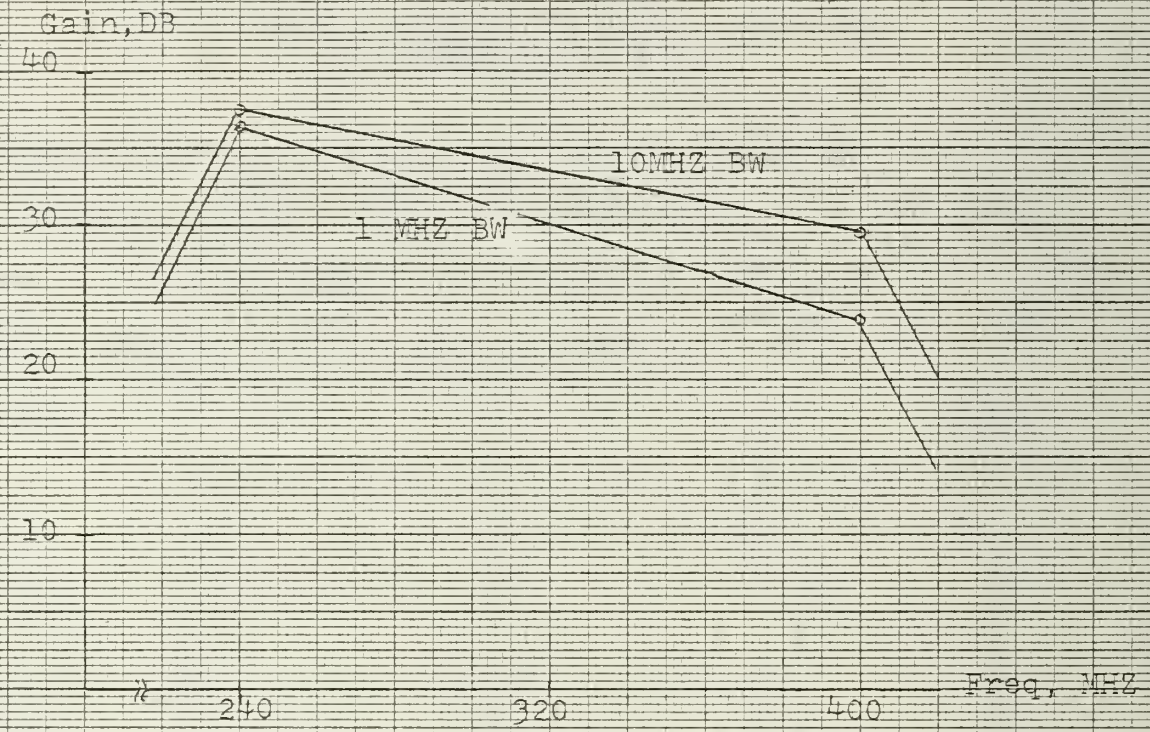


Figure 8.1. RF Channel Gain at TP26 vs. Frequency

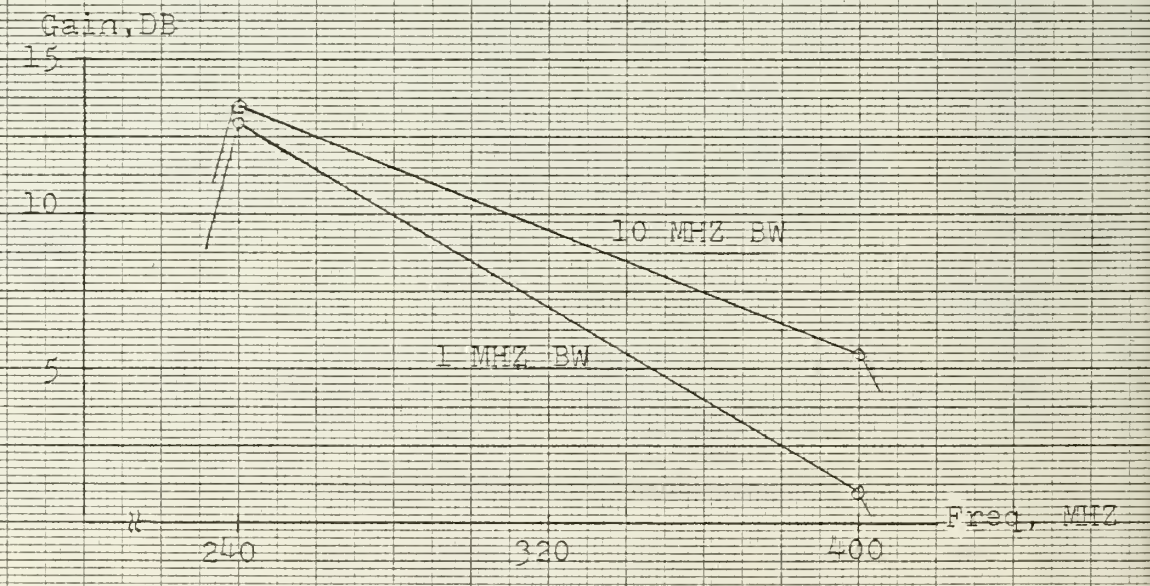


Figure 8.2. RF Channel Gain at TP22 vs. Frequency

RG 223 coaxial cable. Table II gives the loss per 100 feet as a function of frequency. Table III gives the RF gain at the UHF band edges as a function of frequency and Blanking Channel Bandwidth.

B. BLANKER CHANNEL GAIN AND FREQUENCY RESPONSE

The Blanking Channel gain is shown in Fig. 8.3 and is tabulated in Table I.b. The gain difference of 4 dB is due to the added insertion loss of the 1 MHz bandpass filter. The frequency response is the response of the RF portion of the channel prior to the mixer. The remainder of the channel is maintained at a 30 MHz frequency.

The power gain of the Blanking Channel is shown in Fig. 8.4. The linear portion of the curve can be moved downward (or right) if desired by adding attenuation at the RF Attenuator (A6R1). This has the effect of moving the curve to the right 10 dB with every 10 dB of attenuation added. These two gain measurements were made from the Deck Box Input (A6J3) to the Logarithmic Amplifier (A3A1).

C. BLANKING CHANNEL PERFORMANCE TEST

The following test procedure was developed to be used as a performance test of the Blanking Channel. The test does not require any equipment that is not a part of the test instrumentation package. Any deviation from the standard set herein indicates some change within the system between the Deck Box Input (A6J3) and the output of the Blanker Drivers located inside A8B1.

TABLE I.b. TEST POINTS/GAIN TABULATIONS FOR BLANKING CHANNEL AND LO INPUTS

This table may be used in conjunction with Appendices D and F for Trouble Shooting the Blanking Channel, Local Osc. Input Channel.

TP	Gain from previous TP	Accumulative 1 MHz BW Gain	Accumulative 10 MHz BW Gain	Remarks
Input of -50 dBm input power at 320 MHz Frequency				
2	- 0.5	- 0.5	- 0.5	
3	- 0.6	- 1.1	- 1.1	
4	Variable	- 1.1	- 1.1	
30	6.5	5.4	5.4	
31	- 8.0	- 2.6	- 2.6	
32	+10.0	7.4	7.4	
33	(-4)1MHz	7.4	3.4	
34	28mv/dB			
A6J5	Input Level Required = +9 dBm			
B	- 3.5	5.5dBm	5.5dBm	
A	+11.5	+17 dBm	+17 dBm	

TABLE II. RG 223 LOSS VS. FREQUENCY

Attenuation/100 ft.	Frequency
6.7 dB	200 MHz
8.0 dB	300 MHz
10.0 dB	400 MHz

TABLE III. GAIN VS. FREQUENCY AND BLANKING BANDWIDTH

Freq=240 MHz		Gain at	Freq=400 MHz	
Blanking Bandwidth		Test Point	Blanking Bandwidth	
10 MHz	1 MHz	TP 26 (A6J6)	10 MHz	1 MHz
37.5 dB	36.5 dB		29.5 dB	24.0 dB
		TP 22 (A5J1)		
13.5 dB	13.0 dB		5.5 dB	1.0 dB

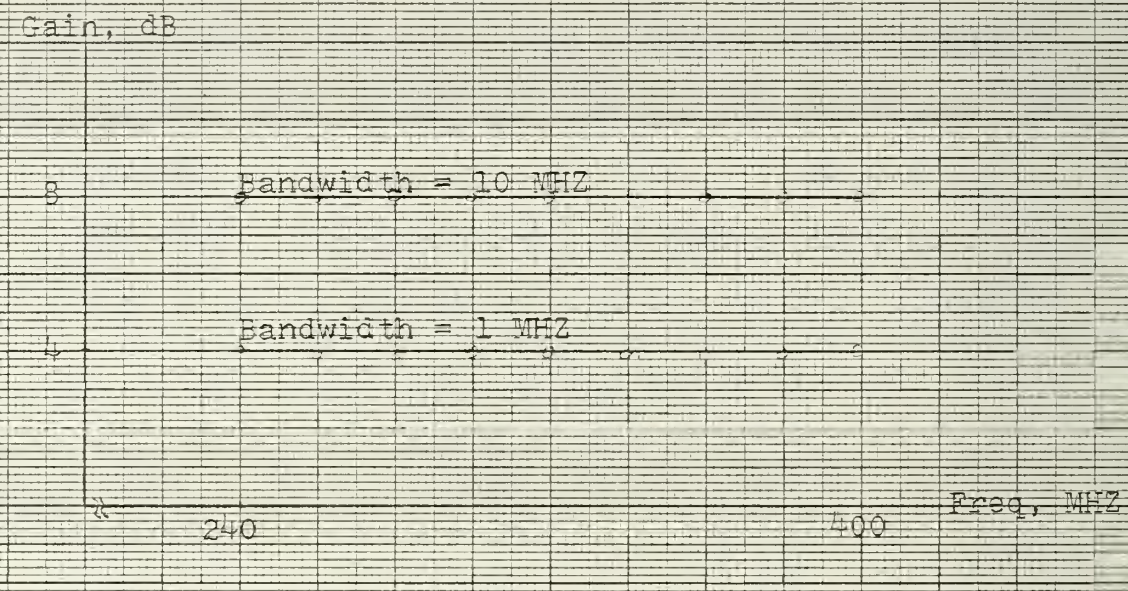


Figure 8.3. Blanker Channel Gain vs. Frequency

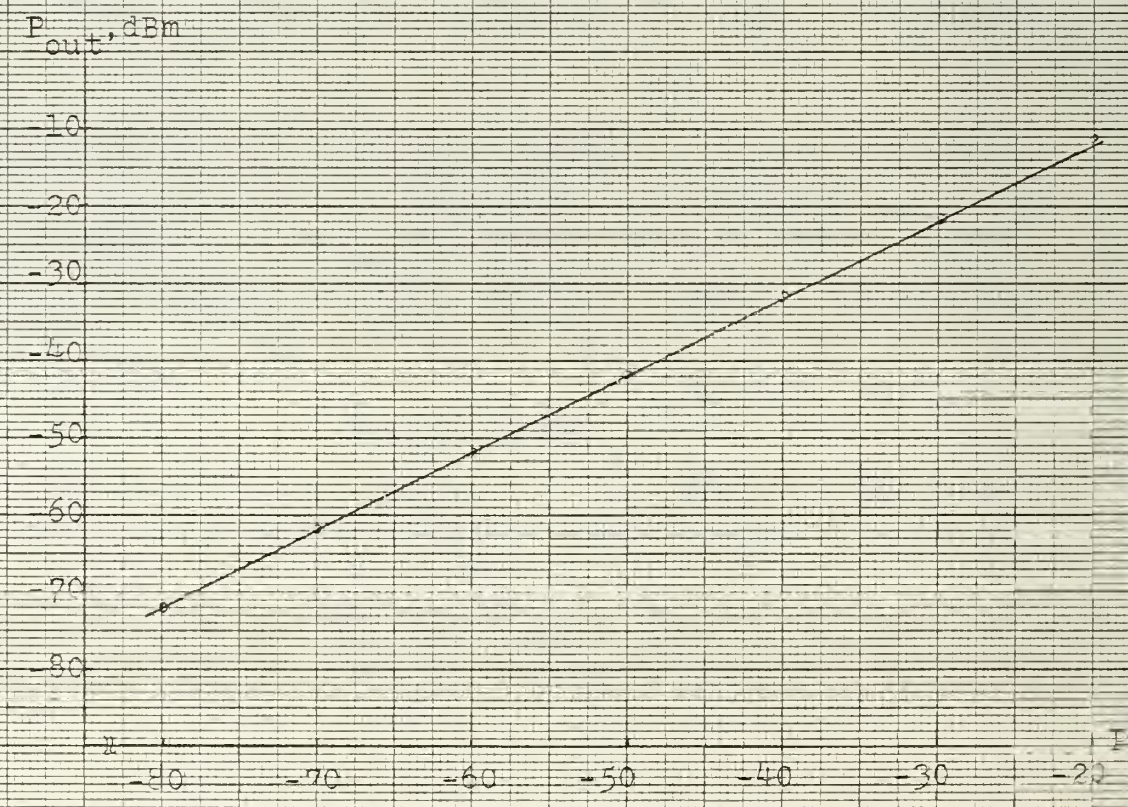


Figure 8.4. Blanker Channel Power Gain

The following controls were set as follows prior to testing.

1. IF Amplifier Unit
    a. Zero attenuation
    b. 10 MHz filters
    c. Additional Gain Out
    d. Scope-Level Analyzer to Scope
    e. The scope output was connected to the oscilloscope.
2. RF Amplifier/Blanker Unit
    a. Zero attenuation
    b. Bandwidth switch to 10 MHz
    c. Switches inside A8B1 set to AC and Long (Normal)

The RF Signal Generator HP 8640 was used to insert a test signal into the Deck Box Input (A6J3). The test signal was a 320 MHz signal modulation at 1 KHz with 100% modulation. The output level was -70 dBm. The Local Oscillator input was set for 290 MHz at +9 dBm.

The Blanker Level Adjust was adjusted for blanking the modulated signal for 50% of the modulated waveform. The dial readings of the Blanker Level Adjust were recorded and are given below as a standard to compare any repetition of the performance test. Variations from these standard reading are to be interpreted as degradation of the Blanking System.

STANDARD: 10 MHz BW

Duty Cycle Meter	50%
Blanker Level Adjust	3.1

D. BLANKER ATTENUATION TESTS

The purpose of this test was to measure the attenuation of the Electronic Switches used for blanking. The measurement was made as follows.

1. A Signal source was connected into the Deck Box In (A6J3)
2. A Spectrum Analyzer was connected to TP 26.
3. The signal source output level was set to -13 dBm at 240 MHz in a CW mode.
4. The Spectrum Analyzer Attenuator (A6R3) was set to 30 dB of attenuation.
5. The power out of TP26 was then observed on the Spectru Analyzer to be -9 dBm with the Blanker Off.
6. The power was then observed with the Blanker On to be -85 dBm, with the Attenuator (A6R3) set to 0 dB.
7. The attenuator of the Blanker was calculated as follo

Attenuation = -85dBm + 9dBm - 30dB = 106dB

E. ONE DB COMPRESSION POINT

The one dB compression point serves as a bench mark of the upper power limit of the linear region of an amplifier. The power level input that causes one dB less gain than any lower power level input is the one dB compression input power The power out when the input is the one dB compression input power is the one dB compression output power.

The measurements were made at TP 22. This point was chosen as the more interesting as it led directly to further signal processing. The output at TP 26 could be controlled for display purposes by use of A6R3 the Spectrum Analyzer Attenuator. The measurement of the one dB point was made as follows.

1. A variable level, calibrated signal source was connected to A6J3.
2. The output at A5J1 was observed using the Spectrum Analyzer.
3. The input power was increased through the linear region of the RF Channel until the gain decreased by one dB.

Table IV gives a tabulation of the one dB compression point as a function of the high and low frequencies of the system and also the Blanker Bandwidth.

F. LOGARITHMIC AMPLIFIER CALIBRATION

The logarithmic amplifier video output varies as the logarithm of the input at a rate of 28mv/dB. The manufacturer's specification sheet shows that this is a linear rate over the input range of -75 dBm to +5 dBm. The output voltage varies from 0v to 2.24v for this input. The amplifier has a Zero Adjustment located at the top of the unit. This adjustment was calibrated as follows.

1. A calibrated, variable level signal source was connected to the Deck Box Input (A6J3) and set for an output power of -80 dBm at 300 MHz in CW mode.

TABLE IV. INPUT POWER FOR ONE DB COMPRESSION OUTPUT POWER

The output power at the one dB compression point is equal to the system gain minus 1 dB.

	10 MHz Bandwidth	1 MHz Bandwidth
240 MHz		
Input Power	-13 dBm	-10 dBm
400 MHz		
Input Power	- 7 dBm	- 2 dBm

When these input power conditions are exceeded, the GAIN as seen at the IF Amplifier Output (A5J1), TP 22 is compressed by at least 1 dB.

2. The local oscillator was set for +9 dBm output and 270 MHz.
3. The Bandwidth Switch was set to 1 MHz bandwidth.
4. A high impedance oscilloscope was connected to the video output which was also terminated in 93 ohms.
5. The screwdriver adjustment was then adjusted for an average of 0v output.
6. As a check, the signal source power was decreased below -80 dBm and the output of the logarithmic amplifier was observed to undergo little change.

This calibration also leads to the conclusion that the minimum input signal that can be used to detect and blank is -80 dBm. The Blanker does operate when lower input power is being supplied into A6J3, however the Blanker is blanking on the noise of the logarithmic amplifier only.

G. DUTY CYCLE CIRCUIT CALIBRATION

The duty cycle circuit was designed to provide an output that is proportional to the duty cycle of the blanker circuit when operating in the normal mode. The output may be a voltage output taken from A5J4 or a visual display on the meter (A6MT). The meter circuit was designed such that the duty cycle in percentage of time may be read directly from the meter after multiplying the meter indication by the position of the switch, (A6S4).

There are four calibrations that must be accomplished in this circuit.

1. Zero Adjustment

   a. Switches A6S1 and A6S2 were set to NORMAL.

   b. The Blanker Level Adjust (A6R4) was set so no blanking pulse was generated.

   c. Switch A6S4 was set for 100% FULL SCALE.

   d. Resistor A6A1R6 was adjusted for 0% meter display.

2. Gain Adjustments

   a. A pulsed signal source of known duty cycle was connected to the Signal Input of the Blanker Control Box (A8B1). The Blanker Level Adjust was set so the blanker activated on the positive pulse

   b. An oscilloscope was connected to the output of the 7486 IC connecting to the Duty Cycle Averaging Circuit, and the duty cycle was observed.

   c. Resistor A6A1R1 was adjusted to display the same duty cycle on the meter that was observed on the oscilloscope.

   d. The Switch A6S4 was then changed to the 10% FULL SCALE position and step b, c were repeated by adjusting A6A1R2. (The duty cycle had to be set within the limits of the switch position.)

   e. The 1% FULL SCALE position calibration was made in similar fashion adjusting A6A1R3.

IX. OPERATING CONTROLS

The operating controls discussed in this chapter are for the most part located on the front panel. Two switches, the pulse width and AC coupling are mounted internally in the Blanker Control Box. The purpose of this was to anticipate being able to eliminate them after enough operating conditions had indicated that only one position of either switch was used.

A. BLANKER LEVEL ADJUST (A6R4)

The Blanker Level Adjust is a 10 Turn, 5 Kohm potentiometer with an exterior ring calibrated in 1/100 digits. The use of Figure 9.1.a and 9.1.b in conjunction with this control allows an operator to select the amount of noise power level that will be blanked.

B. METER SELECTOR SWITCH (A6S4)

The meter selector switch is used to select the inputs to the meter to be monitored. The top five positions are used to monitor power supplies. If these positions are selected, the meter deflects to about mid scale to give an indication that power is available.

The bottom positions are used to display the duty cycle of the blanker when it is operating. The duty cycle is the result of the meter reading multiplied by the switch position.

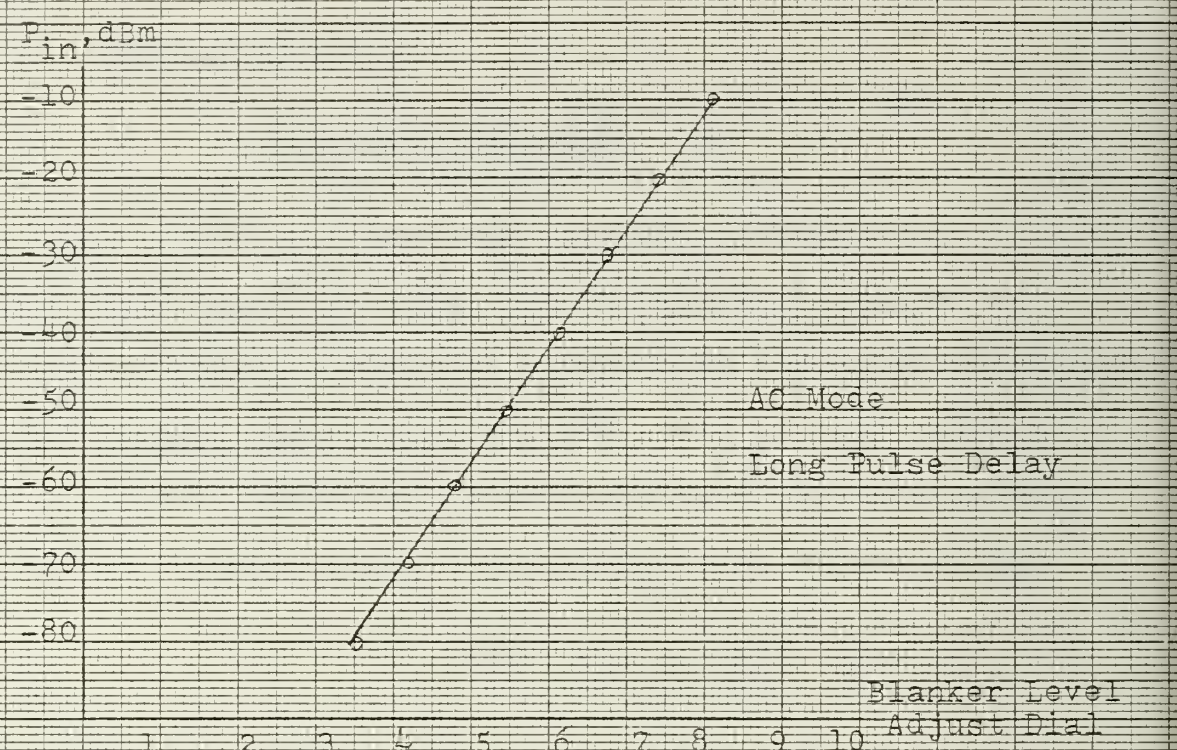


Figure 9.1.a. P_{in} vs. Dial Setting in 1 MHz BW

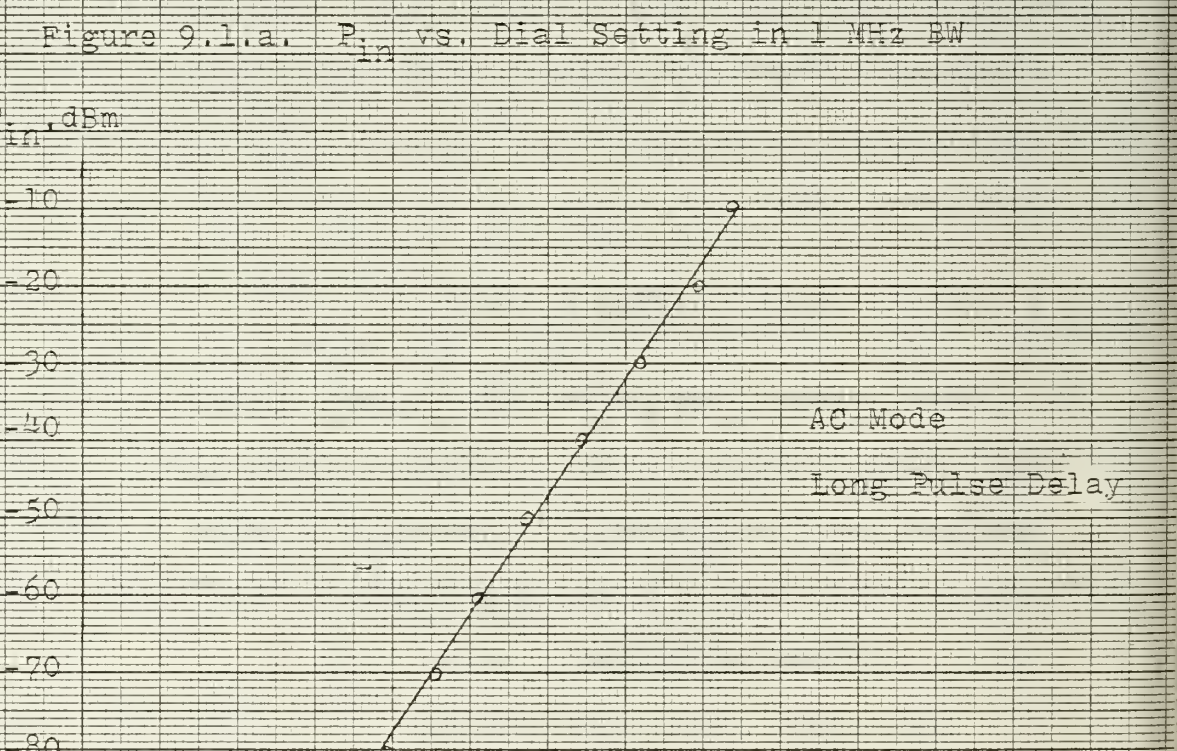


Figure 9.1.b. P_{in} vs. Dial Setting in 10 MHz BW

C. BANDWIDTH SWITCH (A6S3)

The Bandwidth Switch is a two position switch. In the 10 MHz position this switch applies DC voltage to the two coaxial switches that switch the extra delay line out of the RF signal path. Simultaneously it switches the DC voltage that allows the 1 MHz filter in the Blanker Channel to be bypassed. When the switch is in the 1 MHz position the extra delay line is inserted in the RF Channel, and the 1 MHz filter is in the Blanker Channel.

Mounted along the sides of the switch are two LEDs. These LEDs are used to indicate that the remotely controlled coaxial switches and the transfer relay are in agreement with the switch command.

D. INVERT-NORMAL SWITCH (A6S1)

The Inverting switch is a two position switch. Normal operation requires the NORMAL position. The INVERT position is used to blank all signals below a selected power level.

E. DISABLE-NORMAL SWITCH (A6S2)

The Disable switch is a two position switch. The NORMAL position is used if the blanker is going to be used (in either INVERT or NORMAL position of A6S1). Only the blanking switches are disabled with this switch. All other circuits on the Blanker Control Circuit Board function as designed.

F. RF ATTENUATOR (A6R1)

The RF Attenuator is a calibrated 100 dB step attenuator (10 dB/step). It may be used to control the input power when it exceeds the 1 dB compression input power so that the system remains in a linear region.

G. IF ATTENUATOR (A6R2)

The IF Attenuator is a calibrated 100 dB step attenuator (10 dB/step). It may be used to control the input power to the logarithmic amplifier in the Blanker Channel. When the attenuator is used in any position other than 0 dB the calibration curve for the Blanker Level Adjust must be compensated

H. SPECTRUM ANALYZER ATTENUATOR (A6R3)

The Spectrum Analyzer Attenuator is a calibrated 100 dB step attenuator (10 dB/step). The attenuator is in the RF Channel leading to the output jack for the Spectrum Analyzer. It is not in the RF Channel leading to the IF Amplifier outpu.

X. CONCLUSIONS AND RECOMMENDATIONS

This chapter contains the conclusions reached concerning the design and construction of the RF Amplifier/Blanker Unit. Some of the circuitry built has proven to be superfluous. Some of the components are placed in inconvenient locations for ready access. These facts are given notice with recommendations for improvement. Included also are recommendations for future work in RF Blankers as they relate to the frequency band of interest in this project.

A. CONCLUSIONS

The RF Amplifier/Blanker Unit meets all the specifications as set forth in Chapter II. A few other characteristics of the system are presented here as a summary of the system. The dynamic range of the Blanking Channel exceeds 70 dB. The sensitivity of the Blanking Channel is in excess of -80 dBm. The blanker eliminates high level noise by attenuating the RF Channel by 106 dB. The Unit has been made compatible with the UHF environment that is being tested through use of shielding and filtering.

The Unit has several characteristics that are minor inconveniences that do not affect the performance adversely. The RF Channel gain is not uniformly flat over the band. This requires using a graph or calculations to determine system gain for the overall test package, or to determine if the

gain has degenerated at any particular frequency other than the center frequency, which is tabulated in Table I.

The unit is bulky and heavy. This requires extra work in transporting the equipment aboard ship. The size is due to the desire to be able to remove components quickly in case of failure or design re-configuration. Component reliability and design suitability have proven that a compact configuration could be as acceptable. The weight could be reduced by lighter gauge metal panels and by using a different delay line subsystem.

The Blanking Control Circuits received the greatest number design modifications. The printed circuit board was not chang with each modification. The Counter Driver and Sync Pulse Driver are not used enough to warrant the space provided for them on the board. The location of the Duty Cycle Amplifier (A6A1) is most inaccessible. It requires dismantling the Blanking Channel to remove the board from its' electromagnetic shield for calibration. A recommendation for a future generation unit would be to eliminate the Counter and Sync Pulse Driver Circuit and reorganize the printed circuit board so that the Duty Cycle Amplifier can be included on the same board with all other integrated circuitry. This provides accessibility, compactness, and makes calibration easier to perform if necessary.

A final change would also be recommended. The Duty Cycle Amplifier is a two stage amplifier using only none inverting amplification stages. This was designed in this manner to

provide the different gains through switching in or out the second stage as the situation demanded. This design was modified to include both stages in cascade at all times. The design could have then been changed to using the inverting inputs of the operational amplifiers, with a positive output voltage still as required. This was not done, consequently the gain of the amplifier is not as stable as might be accomplished.

B. RECOMMENDATIONS FOR FUTURE WORK

The physical demands expected of the test package were considered when choosing a delay line. The need exists for a wide band, lightweight delay line that has a flat frequency response over the band from 240 MHz to 400 MHz. This delay line must be durable to accommodate frequent movement and vibration with the ability to accept some shock. It should be adjustable in terms of tens of nsecs. Compactness and size are also important as well as its compatibility with its environment. The crosstalk from input to output should be in excess of -100 dB. It remains unlikely that a more economic delay line exists than coaxial cable for UHF delay lines as other delay lines experience large insertion losses.

APPENDIX A DELAY LINE CALCULATIONS

The delay line must delay the RF signal in the RF Channel until blanking can be initiated. Too long a delay will result in the RF pulse being present after blanking has occurred.

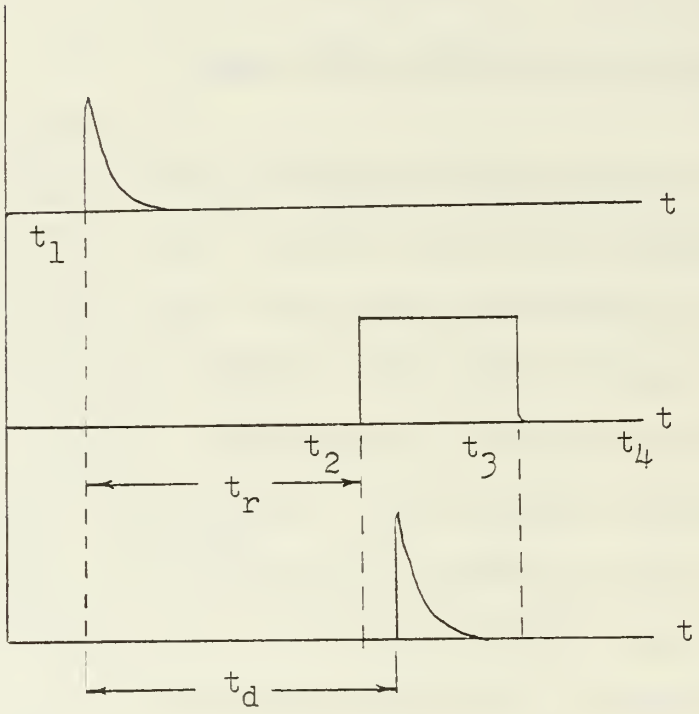


Figure A-1. Delay Times

t_1 = a pulse occurs at power splitter, A7PS1.

t_2 = blanking is initiated.

t_3 = blanking is terminated.

t_d = delay caused by delay line

t_r = response time of Blanker Channel

For effective blanking: $(t_2 - t_1) < t_d < (t_3 - t_1)$

Table V lists the components that cause the time response to be of finite length. The total delay is 379 nsecs in the 10 MHz bandwidth mode, and 1.379 microsec in 1 MHz.

These calculations are based on the typical values of propagation delay as given by the manufacturer. Addition of a 5% error factor appears reasonable to account for small errors due to interconnections etc. Therefore the Blanker Channel is considered to have a delay of about 400 nsecs.

Utilizing RG 223 coaxial cable as a delay line provides a delay of 142 nsec/100 ft.

Velocity of propagation = 0.714c

$= 7.027 \times 10^8$ ft/nsec

Delay/100 ft $= 100/7.027 \times 10^8$

= 142.3 nsec/100 ft

The above calculations show that 400 nsec delay requires at least 281 ft. of RG 223. The actual delay line consists of two lengths of 100 ft. each and one length of 119 ft., for a delay of 454 nsec. This ensures that the blanker is fully activated before the pulse to be blanked can arrive at the blanker switches.

The trailing edge of a high level pulse would arrive at the blanking switches about 50 nsec after the blanking had been terminated except for the action of the Pulse Width Circuit. In the 10 MHz blanking bandwidth mode this extra delay is 50 nsec.

The delay line consists of an optional delay of 725 nsec when the blanker bandwidth of 1 MHz is selected. Theoretically

TABLE V. COMPONENT DELAYS

Component	Identification	Response Time
Amplifier	A4A2	-
Mixer	A1M1	-
Filter	A2F1	100 nsec
Amplifier	A1A2	-
Coaxial Switch	A2CS1	-
Filter (optional)	A2F2	(1 microsec)
Attenuator	A6R2	-
Logarithmic Amp	A2A1	200 nsec
Threshold Comparator	A8B1A1	15 nsec
Pulse Width Ckt.	A8B1A2	22 nsec
Inverter	A8B1A3	22 nsec
Blanker Drivers	A8B1A4	20 nsec
Total		379 nsec (1379 n

NOTE: The pulse width circuit provides an optional delay at the end of the blanking pulse of either 50 or 5600 nsec

this is not enough to compensate for the addition of the 1 MHz filter that is inserted into the Blanker Channel. Actual observations indicated that most if not all noise above the desired level is effectively blanked. The trailing edge of the pulse would be blanked by the effect of the slower response of the Blanker Channel. The addition of an option to extend the Pulse Width by 5 microsec allows blanking to be maintained in those instances where the trailing edge of the pulse is ragged or varying in amplitude.

APPENDIX B BLANKER CHANNEL NOISE POWER

Below are the figures and calculations for the system noise temperature. These temperatures are then converted to the noise power as seen at the system input, when terminated in its' characteristic impedance.

Component	Loss,dB	Noise Fig.,dB	T_n, K	T_{sys}, K
Filter	0.6	0.6	39.2	39.2
Limiter	0.5	0.5	35.4	40.6
Power Splitter	3.5	3.5	359.2	462.7
Amplifier	-12.0	10.5	2963.8	8566.0
Mixer	8.5	9.0	1539.8	280.2
Filter	2.0	2.0	169.6	218.5
Amplifier	-9.5	5.2	670.2	1370.7
Coaxial Switch	0.2	0.2	13.7	3.1
Filter	3.0	3.0	288.6	69.3
Logarthmic Amplifier	28mv/dB	10.0	2610.0	1252.3 627.4*

$$T_{sys} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \cdots \frac{T_k}{G_1 G_2 \cdots G_{k-1}}$$

$T_n = 290^{\circ}K(NF-1)$ or $T_p(L-1)$ where T_p is assumed = $300^{\circ}K$

$T_{sys} = 12,302.6^{\circ}K$ for 1 MHz BW

$T_{sys}^{*} = 11,608.4^{\circ}K$ for 10 MHz BW

The interfering noise input to the RF Amplifier Unit must exceed P_{noise} before the Blanker can discriminate between the signal and system noise.

$$P_{noise} = k\ T_{sys}\ \text{Bandwidth}$$

$$P_{noise}\ (1\ \text{MHz}) = -198.6\ \text{dBm} + 40.9\ \text{dB} + 60\ \text{dB}$$
$$= -97.7\ \text{dBm}$$

$$P_{noise}(10\ \text{MHz}) = -198.6\ \text{dBm} + 40.6\ \text{dB} + 70\ \text{dB}$$
$$= -\ 88.0\ \text{dBm}$$

The Blanking Channel has a linear sensitivity for signals greater than (-75 dBm - Gain in dB). This results in -83 dBm for a bandwidth of 10 MHz and -79 dBm for bandwidth of 1 MHz. P_{noise} is less than this linear sensitivity measure and therefore does not degrade the system performance.

APPENDIX C POWER REQUIREMENTS

A1A1	120 ma/+12v
A1A2	60 ma/-15v
A2A1	70 ma/+12v, 70 ma/-12v
A3A1	120 ma/+12v
A3A2	110 ma/+15v
A4A1	135 ma/+15v
A4A2	110 ma/+15v
A5A1	120 ma/+12v
A5A2	120 ma/+12v
A5A3	110 ma/+15v
A5A4	110 ma/+15v
A5A5	110 ma/+15v
A6A1	1 ma/+12v, 1 ma/-12v
A7A1	110 ma/+15v
A8B1	16 ma/+15v, 28 ma/-15v, 83 ma/-5v, 20 ma/-5v
A2CS1	120 ma/+28v
A5C1	120 ma/+28v
A5C2	120 ma/+28v

Total:	550 ma/+12v, 70 ma/-12v
	800 ma/+15v, 89 ma/-15v
	83 ma/+5v, 20 ma/-5v
	360 ma/+28v

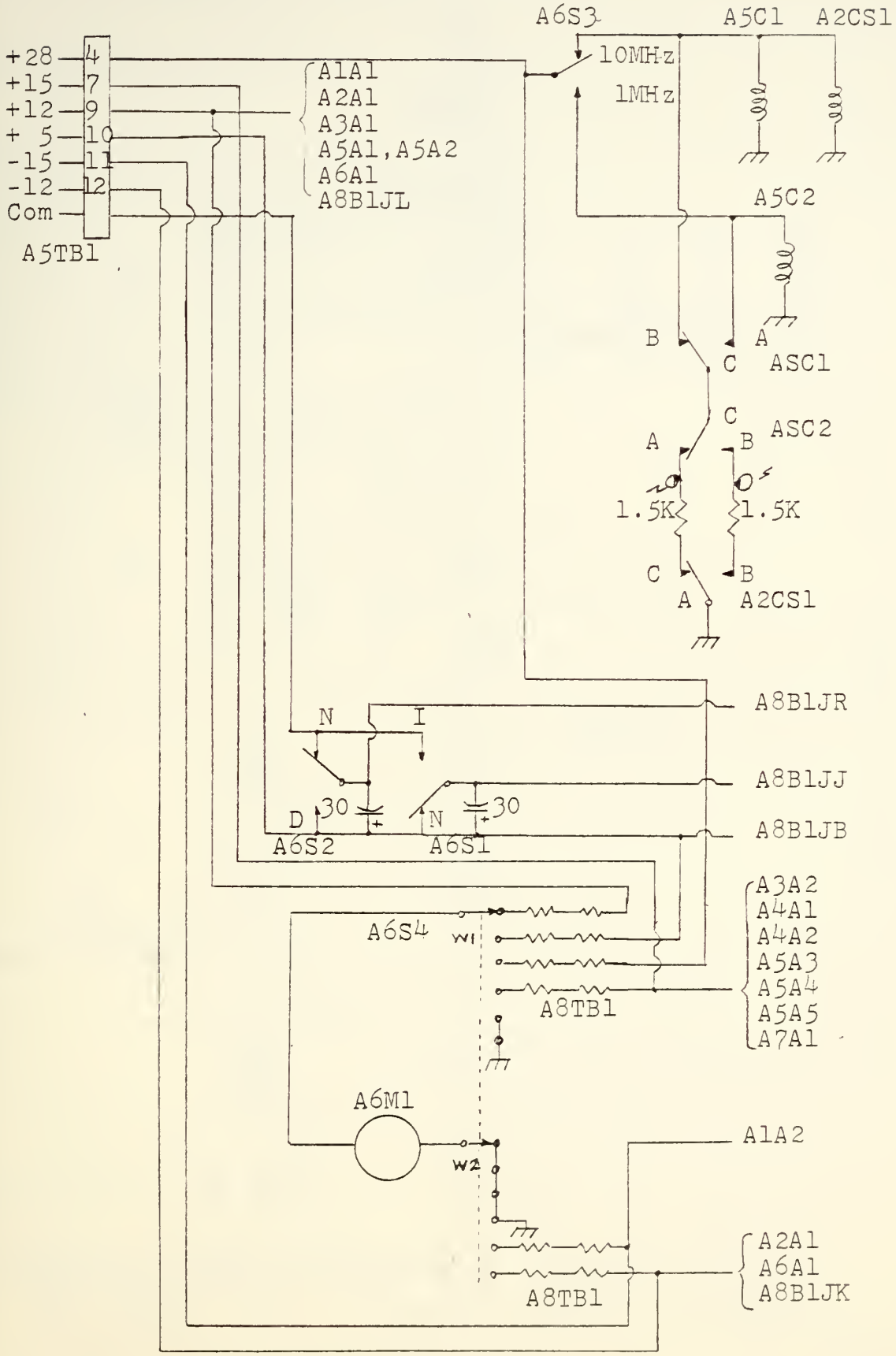


Figure D.1. DC Power Distribution

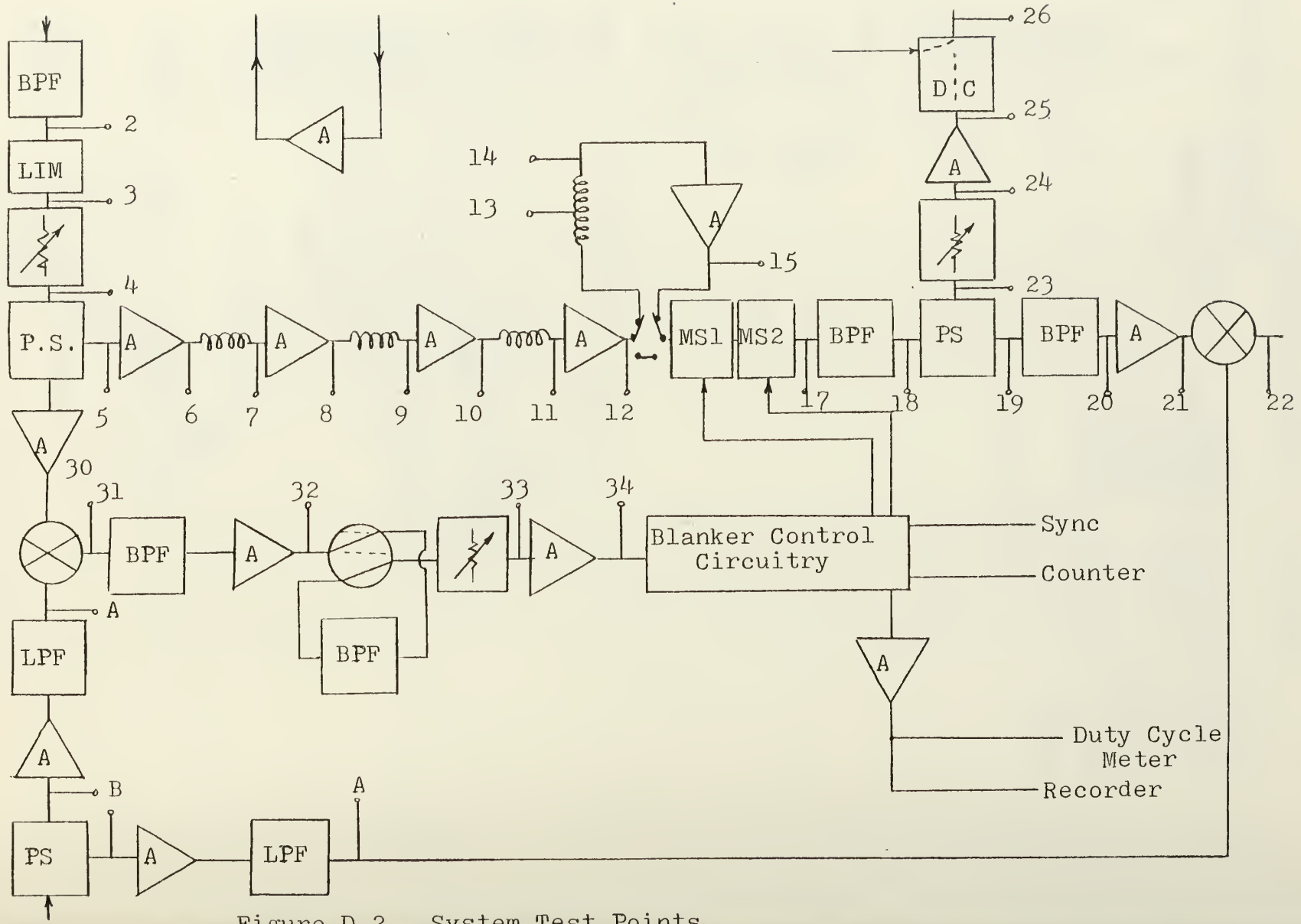


Figure D.2. System Test Points

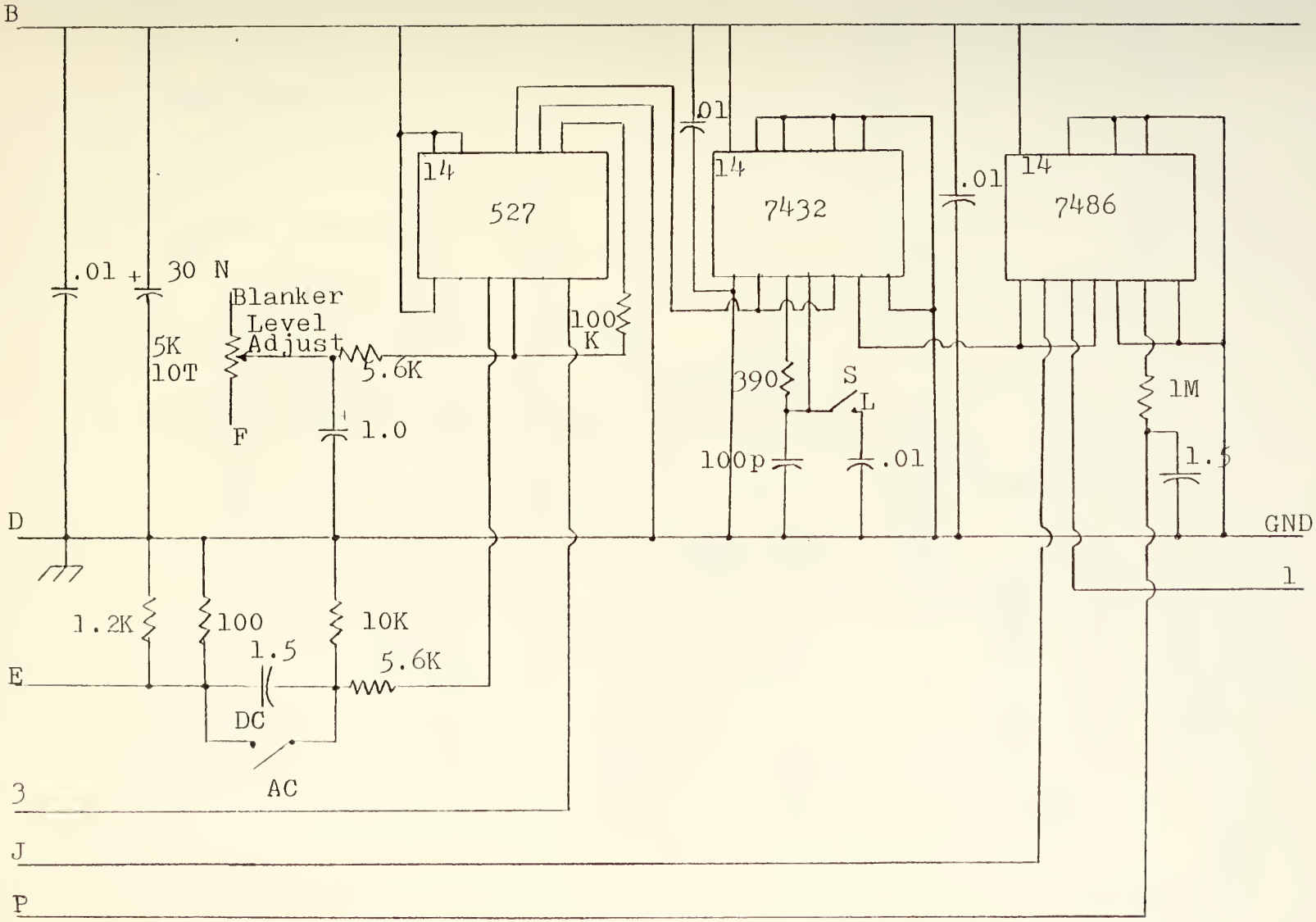


Figure D.3. Threshold Comparator, Pulse Width, Shaper, Inverter, Averager Circuits

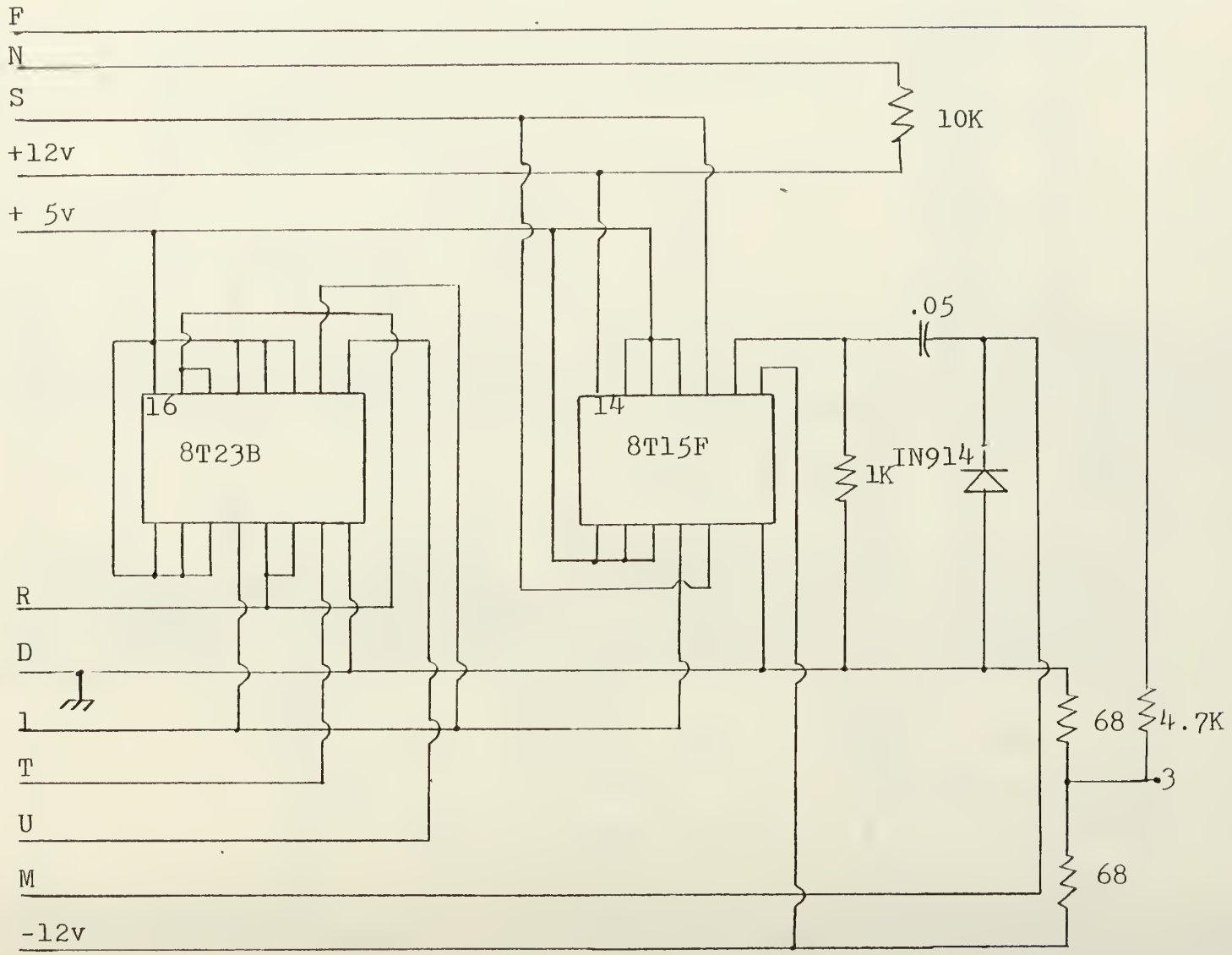


Figure D.4. Blanker Drivers, Counter and Sync Pulse Driver Circuits

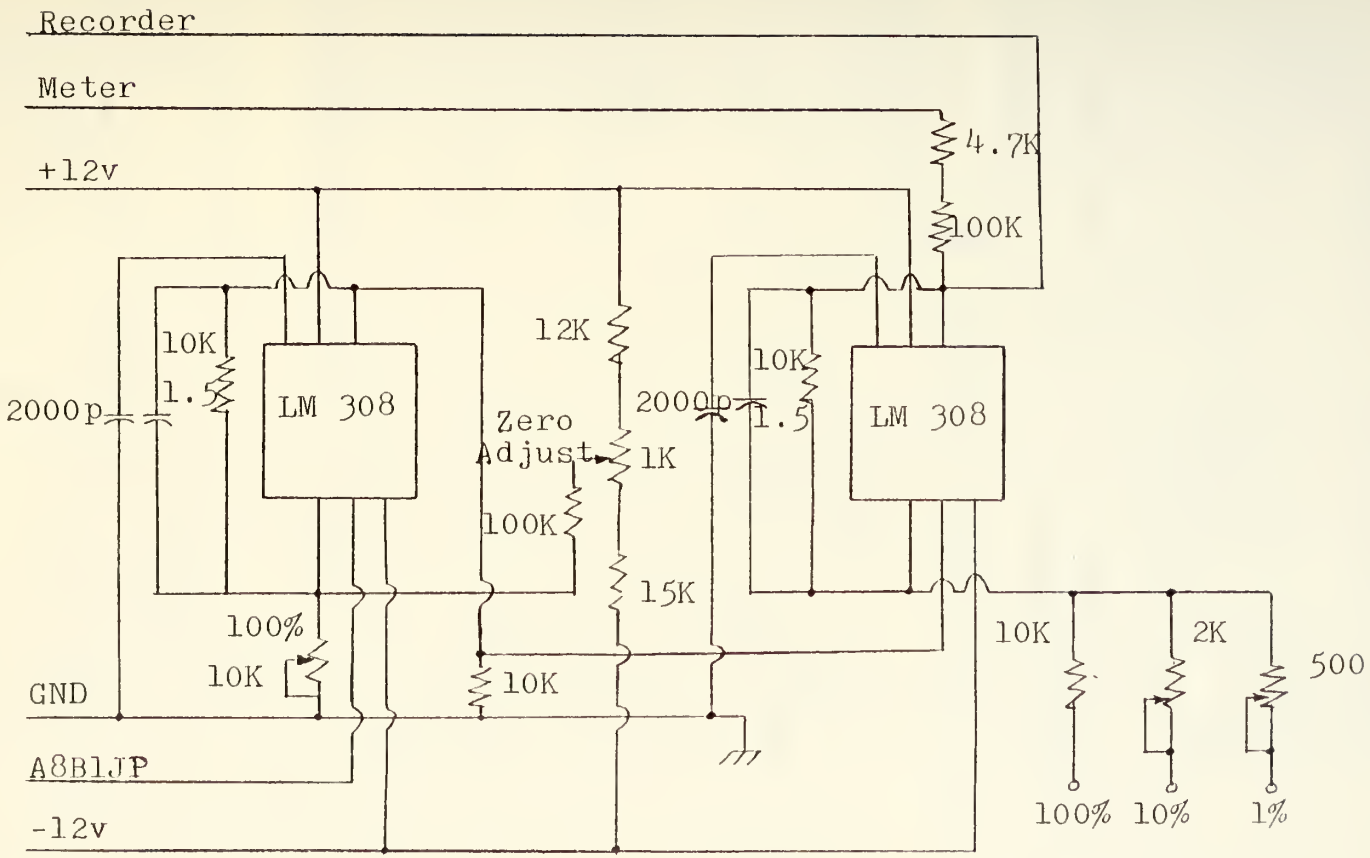
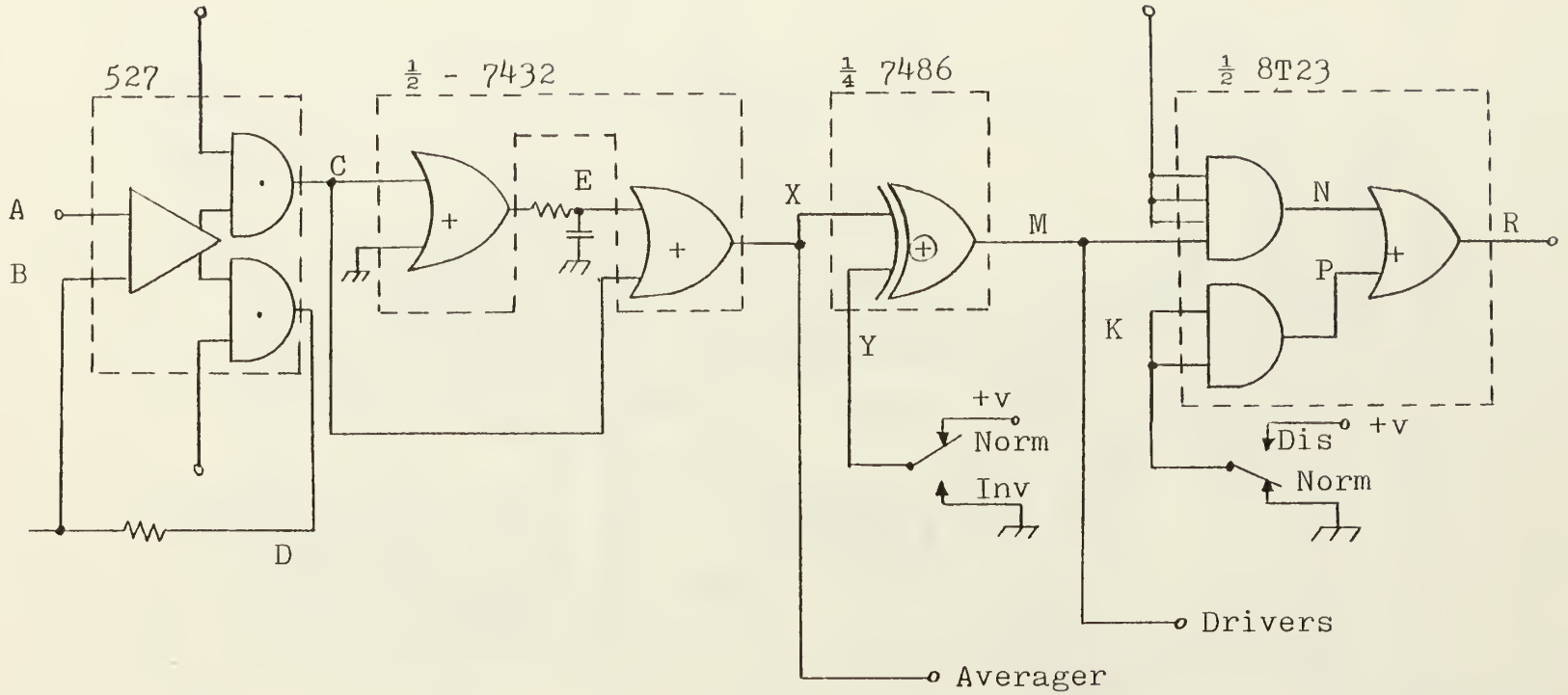


Figure D.5. Duty Cycle Amplifier Circuit



A	B	C	D	
B	A	1	0	Blank
B	A	0	1	Not Blank

C	E	X	
0	0.8	0	No Blanking
0	0.8	1	Terminating
1	0.8	1	Initiated
1	0.8	1	Blanking

X	Y	M
0	1	1
1	0	1
0	0	0
1	1	0

K	L	M	N	P	R	
0	1	0	0	0	0	Blanking
0	1	1	1	0	1	No Blanking
1	1	0	0	1	1	Disabled
1	1	1	1	1	1	Disabled

Figure D,6. Blanker Control Logic

APPENDIX E CALCULATIONS FOR EMC

Switching time of a 7486 IC is about 5 nsecs. This corresponds to a fundamental frequency of 200 MHz. The IC may be considered a current source. This implies that the main RFI in the near field is magnetic. Magnetic shielding is accomplished by enclosing the IC inside an Aluminum box, with thickness of 187.5 mils. The reflection loss of the magnetic field may be calculated [Ref. 4].

$$R_h = 20 \log \left[\frac{0.462}{D} \sqrt{\frac{\mu}{F\sigma}} + (0.136)(D) \sqrt{\frac{F\sigma}{\mu}} + 0.354 \right]$$

F in Hz

D in inches

$$\frac{\sigma}{\mu} = 0.55$$

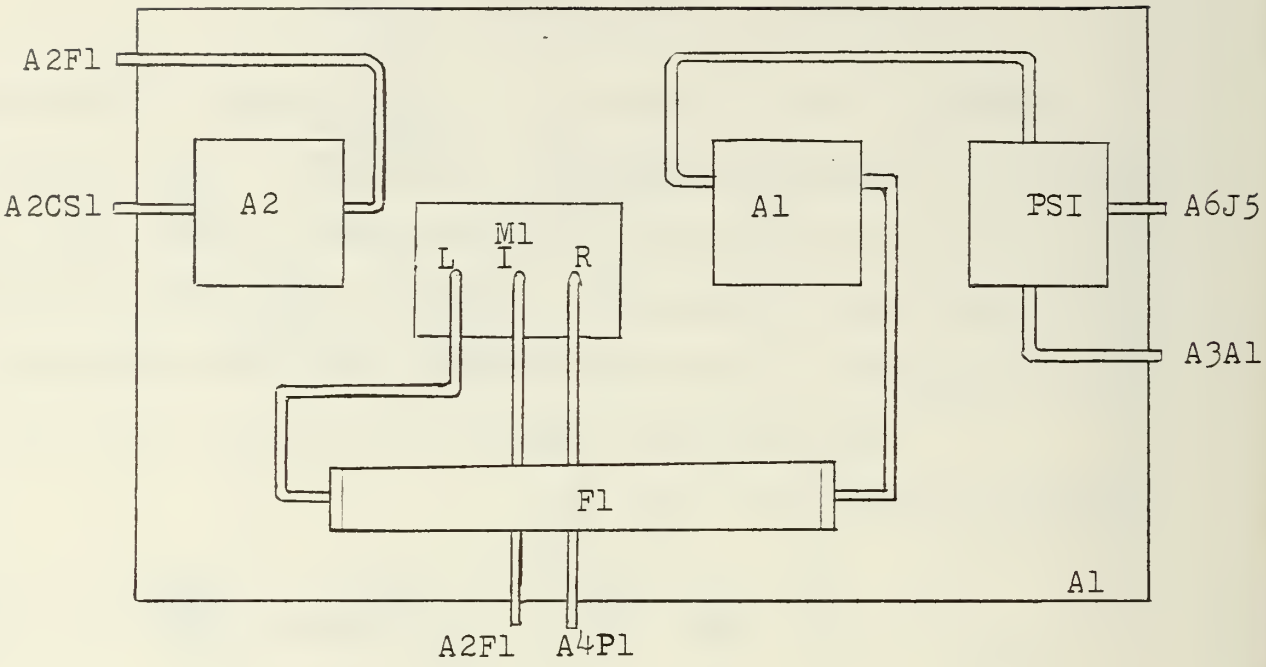
$$R_x = 20 \log \left[\frac{0.462}{2} \sqrt{\frac{1.8}{2x10^8}} + (1.36)(2) \sqrt{2x10^8 x.55} \right.$$

$$\left. +0.354 \right]$$

$$= 20 \log \ 2.852 \times 10^3$$

$$R_h = 91 \text{ dB}$$

APPENDIX F MODULAR LOCATION OF COMPONENTS



A1 - Right Side Panel

A1A1 - Avantek Amplifier

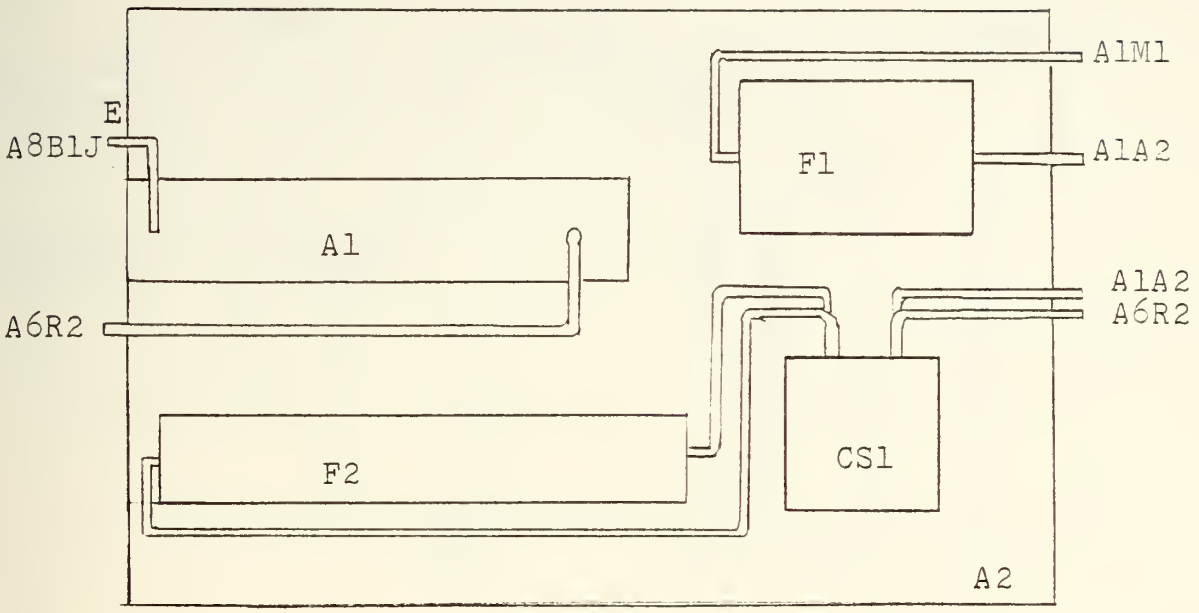
A1A2 - Anzac Amplifier

A1F1 - K & L Low Pass Filter

A1M1 - Minicircuits Mixer

A1PS1 - Anzac Power Splitter

Figure F.1. Right Side Panel



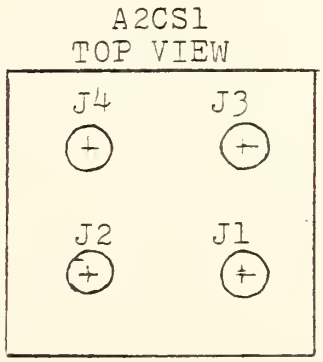
A2 - Center Panel - Right Side

A2A1 - RHG Logarithmic Amplifier

A2F1 - K & L 10 MHz BW Filter

A2F2 - K & L 1 MHz BW Filter

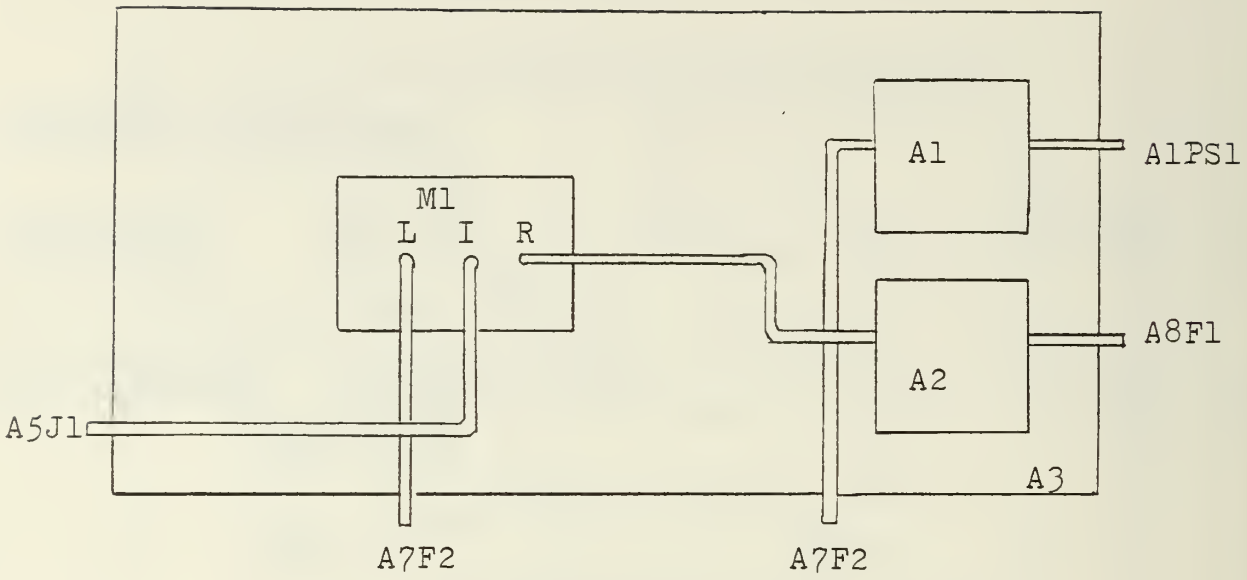
A2CS1 - Transfer Switch



10 MHz BW Makes
J1-J3, J2-J4

1 MHz BW Makes
J1-J2, J3-J4

Figure F.2. Center Panel Right Side



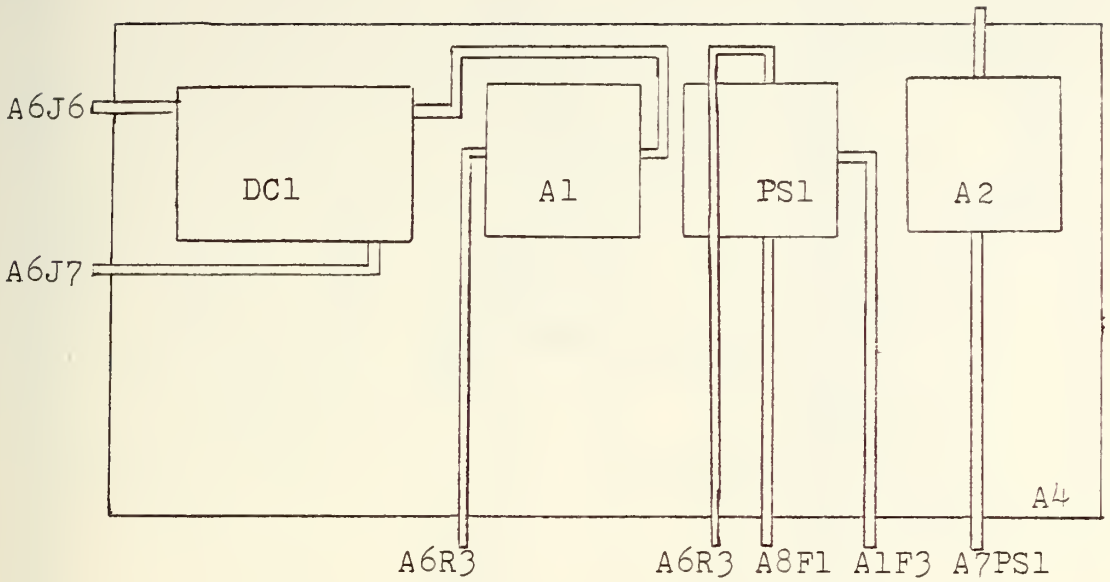
A3 - Center Panel - Left Side

A3A1 - Avantek Amplifier

A3A2 - Avantek Amplifier

A3M1 - Minicircuits Mixer

Figure F.3. Center Panel, Left Side



A4 - Left Side Panel

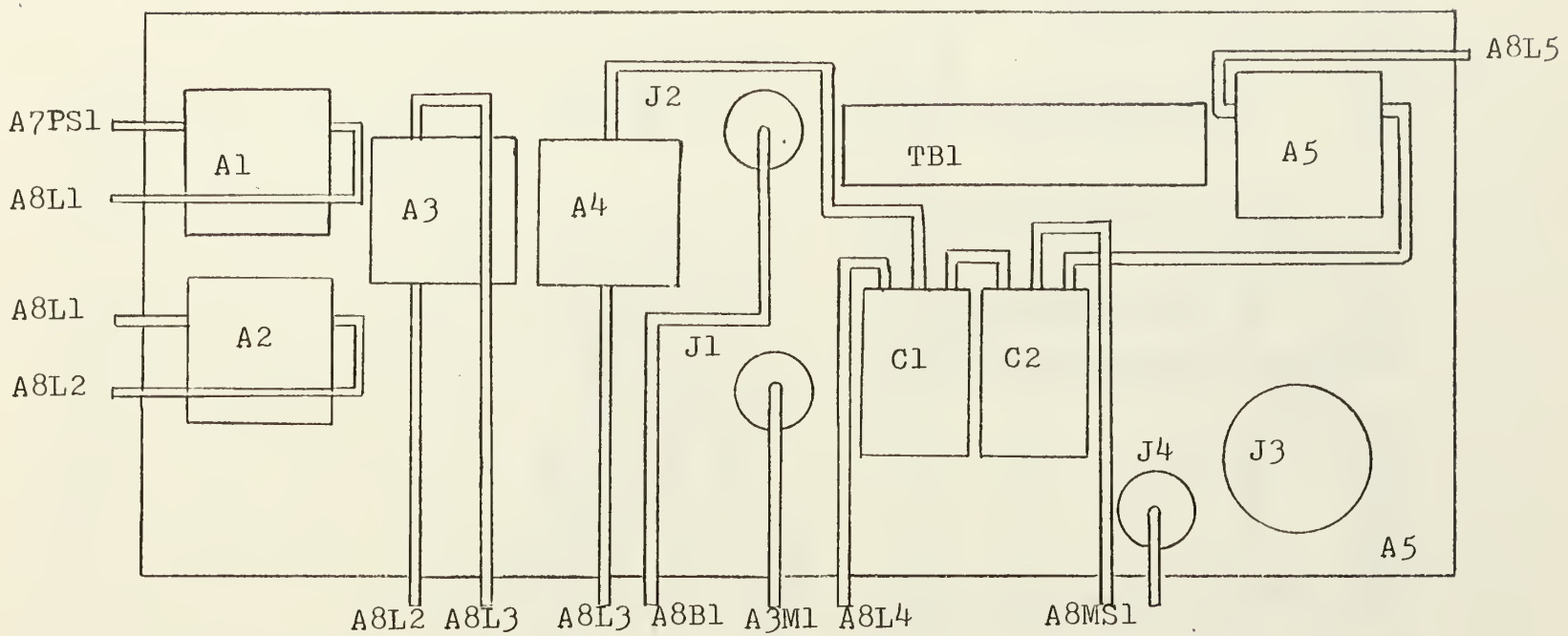
A4A1 - Watkins-Johnson Amplifier

A4A2 - Watkins-Johnson Amplifier

A4DC1 - Engelman Directional Coupler

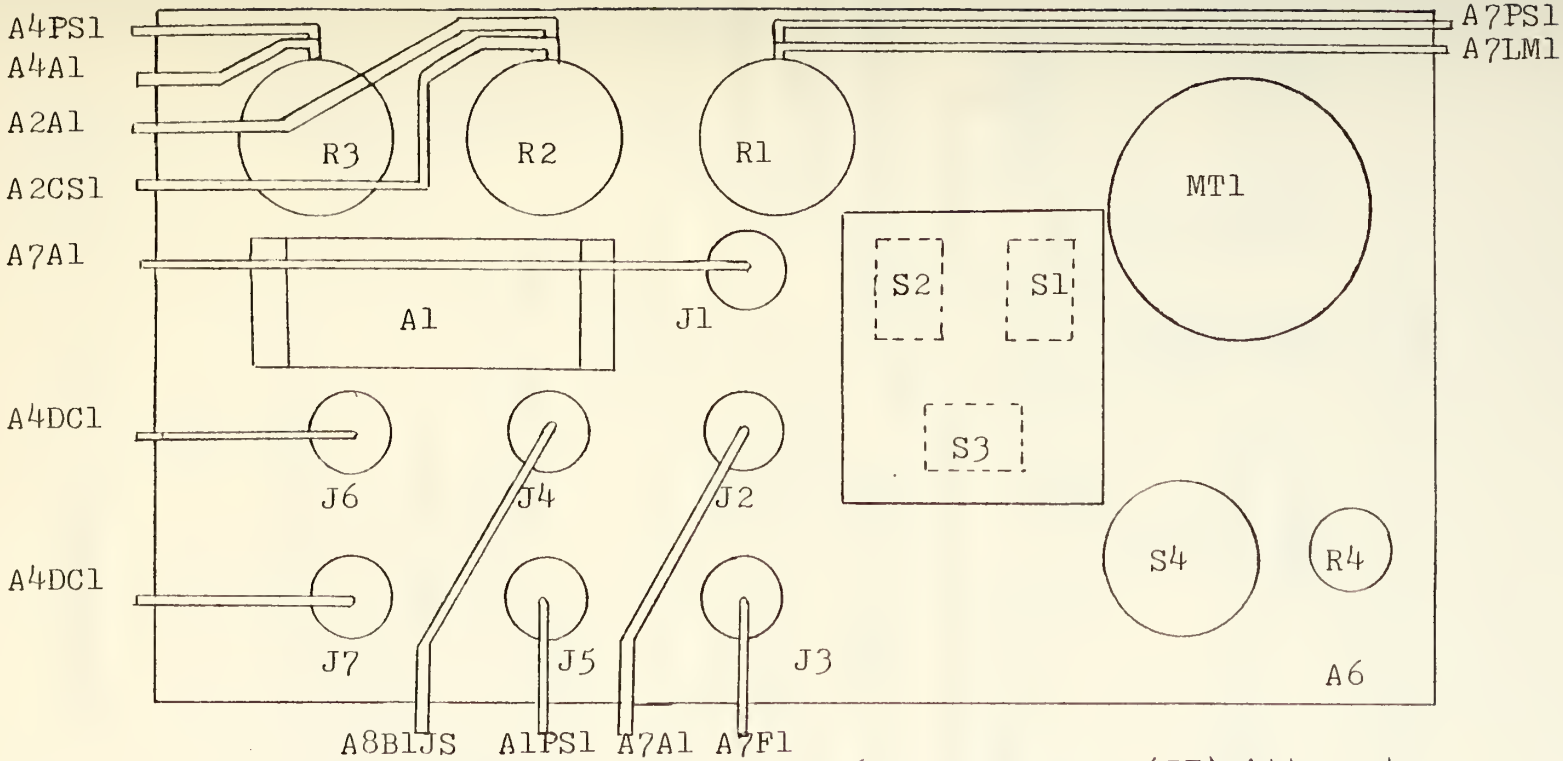
A4PS1 - Anzac Power Splitter

Figure F.4. Left Side Panel



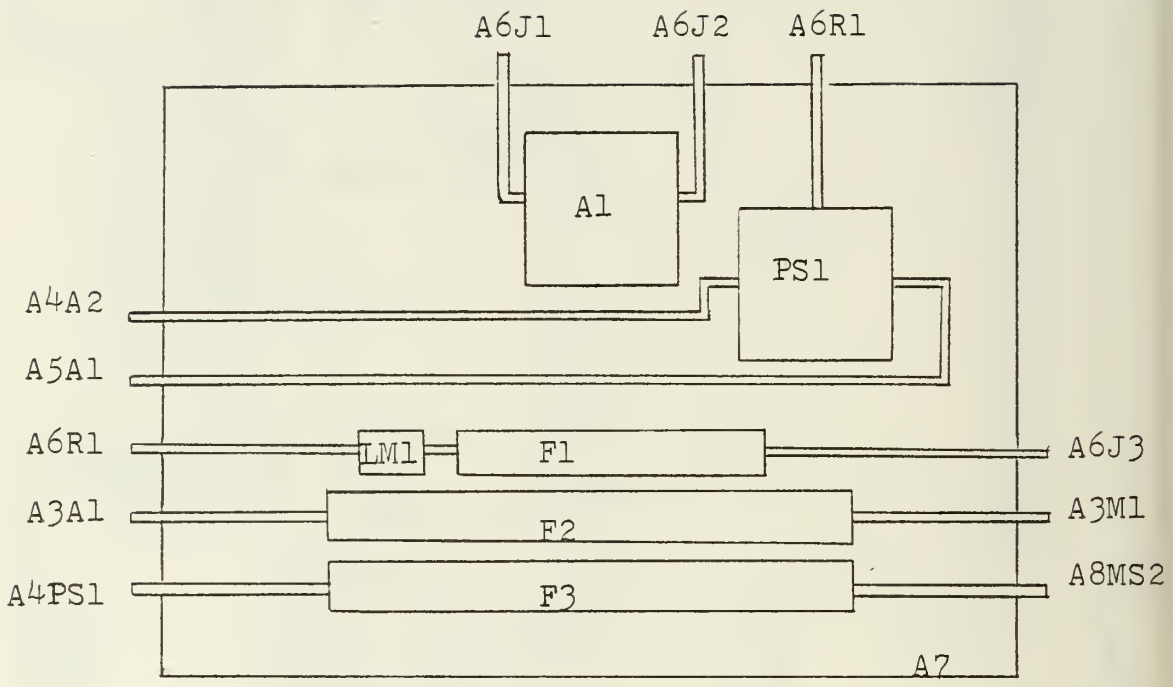
A5 - Rear Panel
A5A1 - Avantek Amplifier
A5A2 - Avantek Amplifier
A5A3 - Watkins Johnson Amplifier
A5A4 - Watkins Johnson Amplifier
A5A5 - Avantek Amplifier
A5C1 - Coaxial Switch
A5C2 - Coaxial Switch
A5J1 - IF Output Jack
A5J2 - Blanker Counter Output Jack
A5J3 - DC Power Input Jack
A5J4 - Duty Cycle Output Jack

Figure F.5. Rear Panel



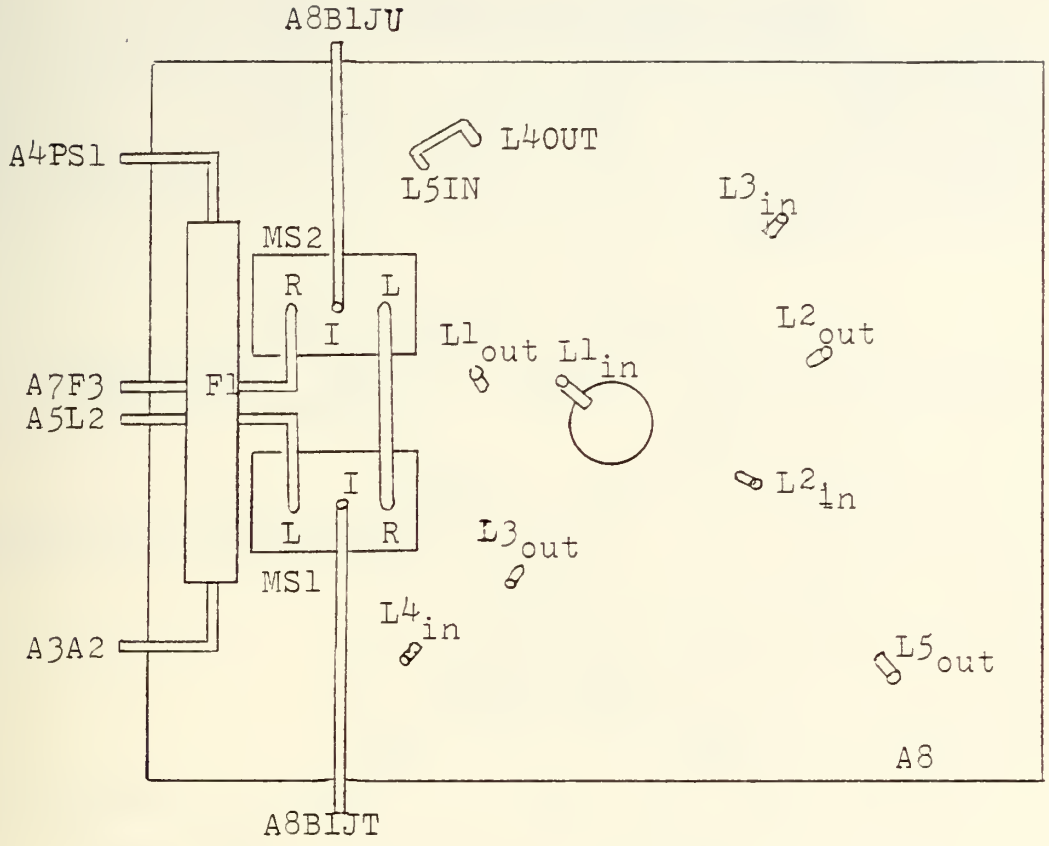
A6 - Inside Front Panel
A6A1 - Duty Cycle Circuit
A6J1 - Aux. Amp. Input Jack
A6J2 - Aux. Amp. Output Jack
A6J3 - Deck Box Input Jack
A6J4 - Scope Output Jack
A6J5 - Local Oscillator Input Jack
A6J6 - Spectrum Analyzer Output Jack
A6J7 - Test Signal Input Jack
A6MT1 - DC Microammeter
A6R1 - RF Amplifier Attenuator
R6R2 - Blanker (IF) Attenuator
R6R3 - Spectrum Analyzer Attenuator
A6R4 - Blanker Level Adjust
A6S1 - Inverter Switch
A6S2 - Disable Switch
A6S3 - Bandwidth Switch

Figure F.6. Inside Front Panel



A7 - Bottom Panel
A7A1 - Watkins-Johnson Aux. Amplifier
A7F1 - Texscan BP Filter
A7F2 - K & L Low Pass Filter
A7F3 - Texscan BP Filter
A7LM1 - AEL Limiter
A7PS1 - Anzac Power Splitter

Figure F.7. Bottom Panel



A8 - Delay Line Case
A8F1 - Texscan BP Filter
A8L1-L5-Delay Line Segments
A8MS1 - Minicircuits Mixer-Blanker Switch
A8MS2 - Minicircuits Mixer-Blanker Switch
A8B1 is suspended above A8

Figure F.8. Delay Line, Top Side

APPENDIX G WIRING DIAGRAMS

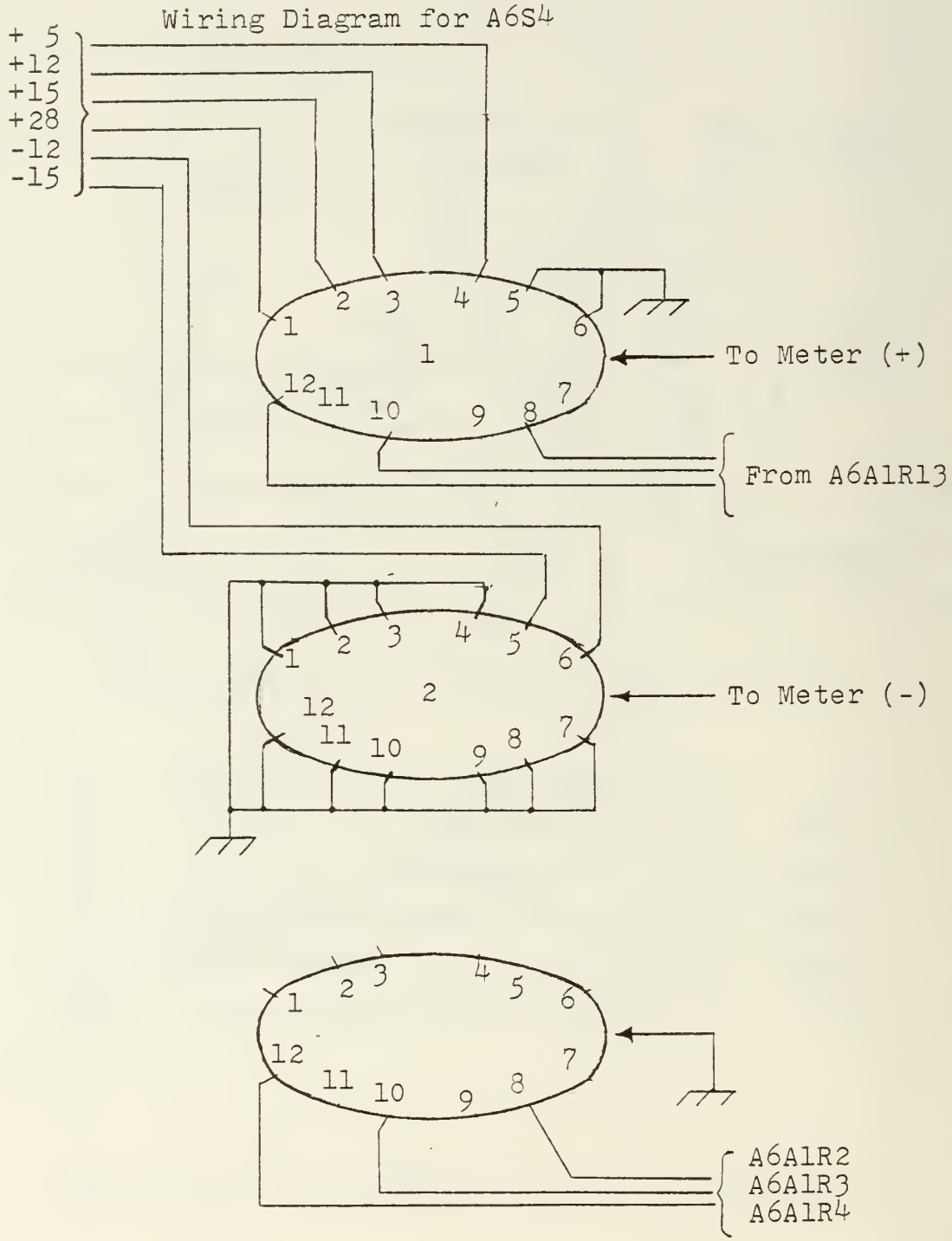


Figure G.1. Meter Selector Switch
A6S4 Wiring Connections

Switches and Indicator Circuits

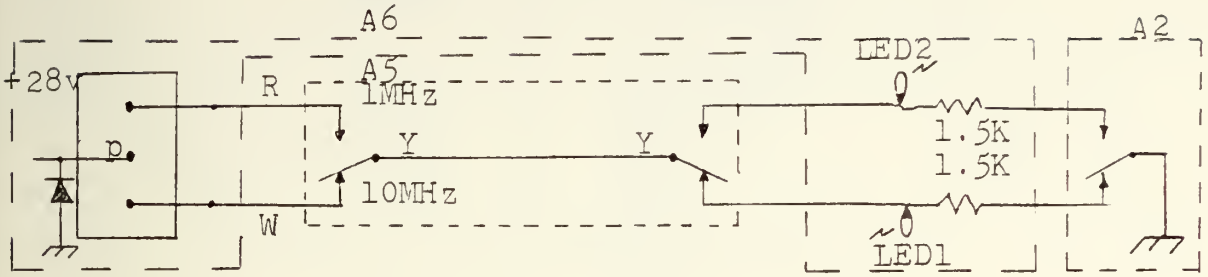
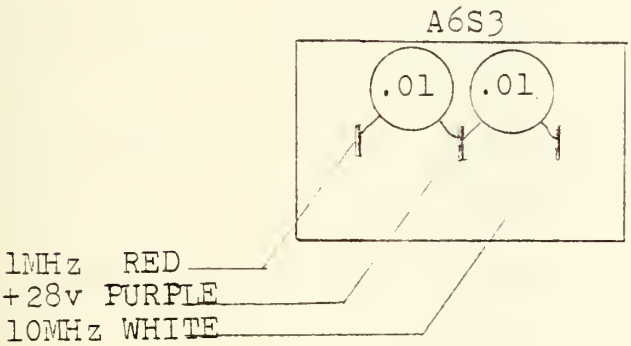


Figure G.2. Bandwidth Indicator Circuit Wiring Connections



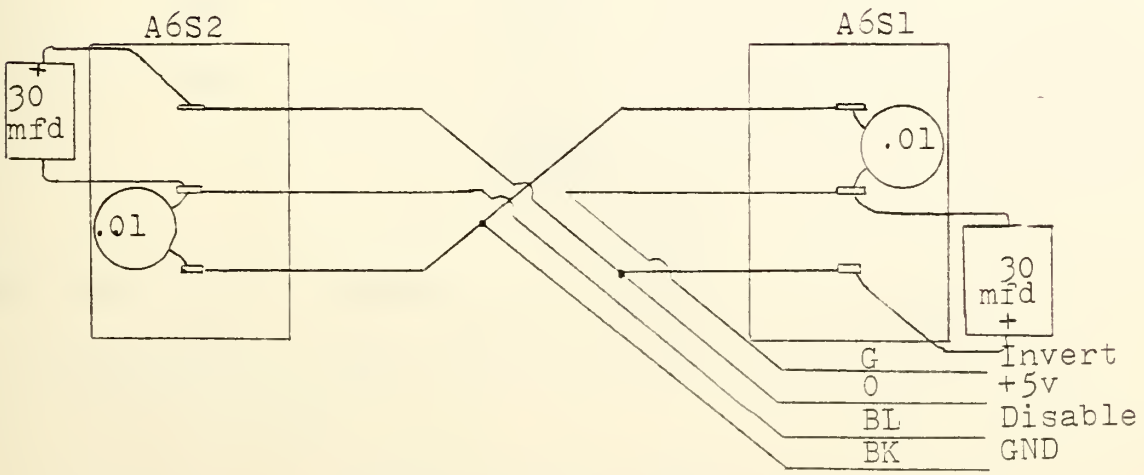


Figure G.3. Inversion and Disable Switches (Inside RFI Shield)

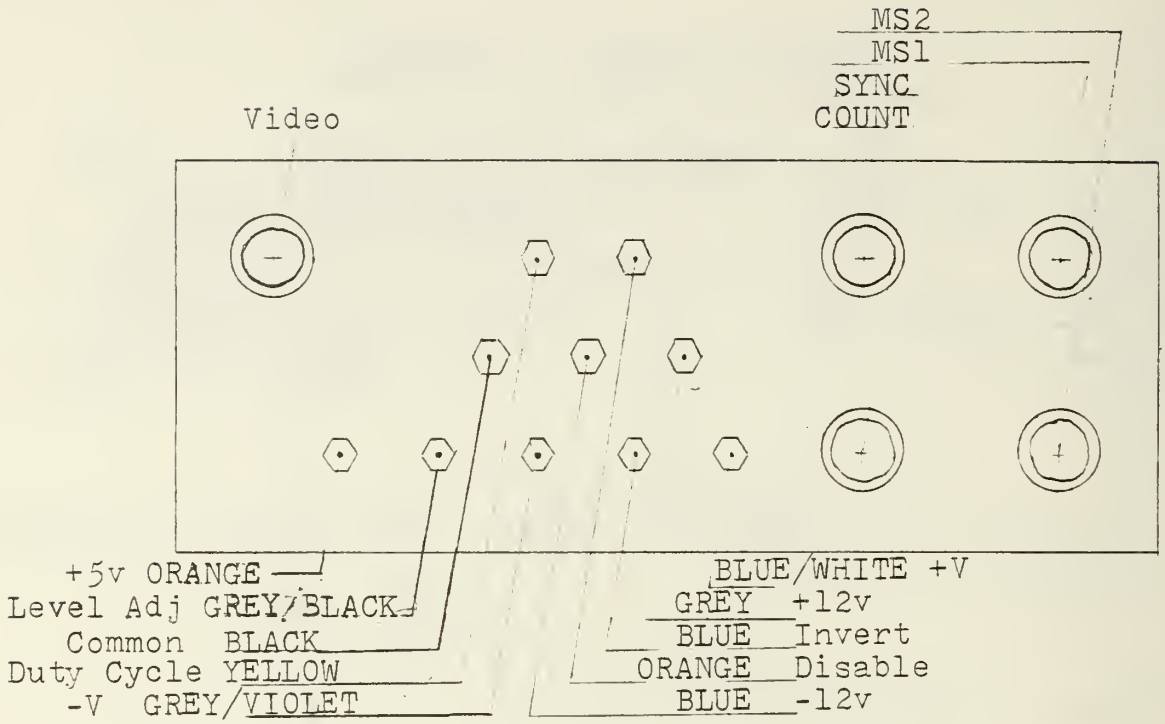


Figure G.4. Blanker Box External Wiring Connections

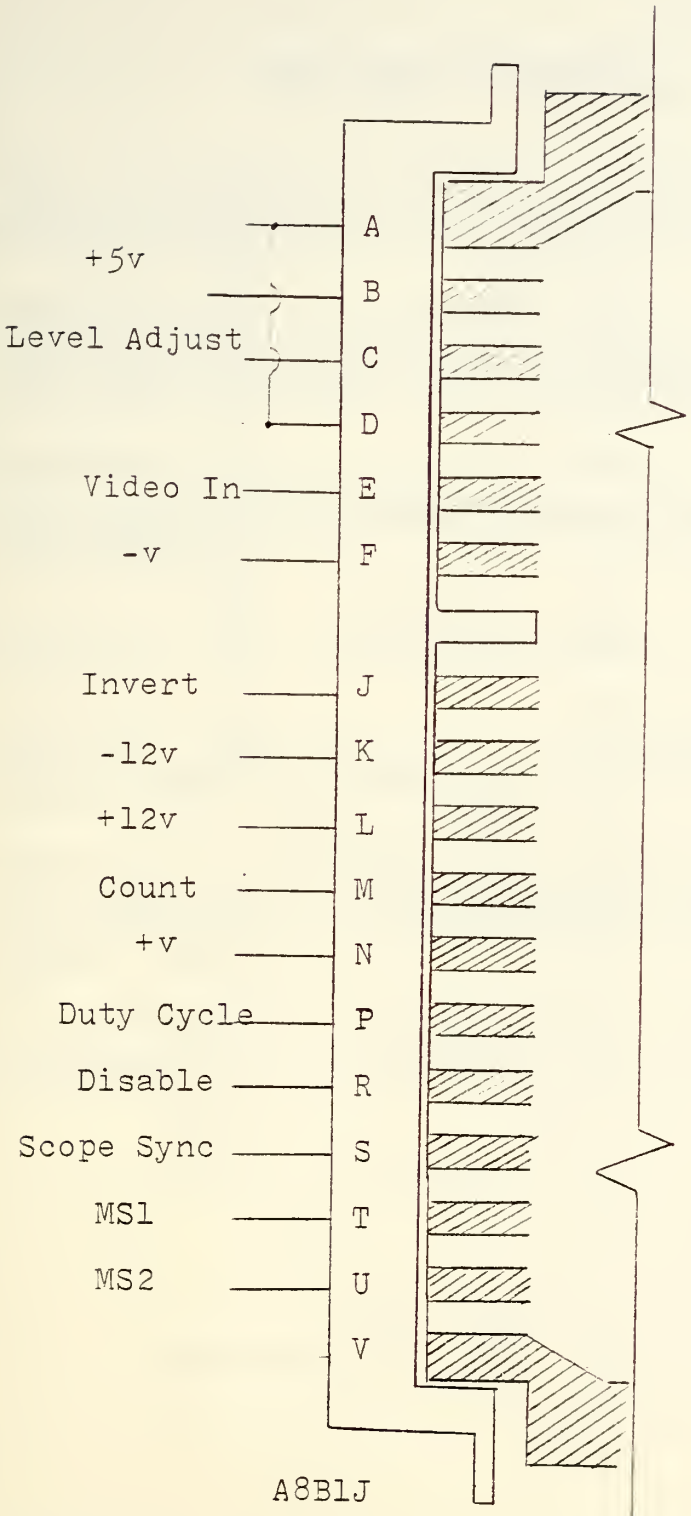


Figure G.5. Blanker Box Internal Wiring Connections

APPENDIX H PARTS LIST

Manufacturers	Component	Model	Quantity
Texscan	A1F3,A8F1	8BB 320/195	2
K&L	A1F1,A7F2	12L120-320-0/0	2
K&L	A2F1	6B 10-30-0/0	1
K&L	A2F2	8B 1-30-0/0	1
K&L	A7F1	12B 120-370-0/0	
Watkins Johnson	A5A3,A5A4,A7A1	6200-303	3
Watkins Johnson	A4A1	6200-352	1
Avantek	A3A1,A3A2,A4A2 A5A1,A5A2,A5A5	9662	6
Anzac	A1A2	102	1
RHG	A2A1	LLT 3010	1
Teleonic	A6R1,A6R2,A6R3	8120S	3
Anzac	A1PS1,A4PS1,A7PS1	T-1000	3
Mini-circuits	A1M1,A3M1 A8MS1,A8MS2	ZLW-1WHB	4
Simpson	A8MT1	3323	1
Signetics	A8B1A1,A8B1A2	527,7432	1 ea
	A8B1A3,A8B1A4	7486,8T23	1 ea
	A8B1A5	8T15	1
National	A6A1A1,A6A1A2	LM308	2
Belden	RG 223		520 f
	0.141		100 f
AMERICON	SMA/SMA, SMA/N BNC, SMA Solder Fittings		
Engelmans Microwave	A4DC1		1

Miscellaneous

Resistors, Capacitors, Terminal Boards, several spools of #22 wire, RFI Capacitors, RFI Inductive Ferrite Beads #10-32 screws, #8-32 screws, #4-40 screws

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5. Milman, J. and Halkias, C. C., Integrated Electronics: Analog and Digital Circuits and Systems, p. 583-584, McGraw-Hill, 1972.

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