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EVALUATION OF FERROELECTRIC MATERIALS FOR MEMORY APPLICATIONS

by

Carl Elof Josefson

June 1990

Thesis Advisor: R. Panholzer

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Ferroelectric materials have wide application in areas such as piezoelectric transducers, pyroelectric detectors, and electro-optics, and now thin-film ferroelectric mateials are being integrated with conventional semiconductor processes to produce memory devices. Memories based on this technology potentially offer nonvolatile data storage and extended read-write endurance in comparison with EEPROMs, without speed or power penalties. These memories are also radiation hard. Considerable interest in ferroelectric memory exists in the Department of Defense (DOD) because of these characteristics. However, several problems remain unsolved and no memory devices have been produced as yet. The physical mechanisms (as they are understood) are discussed, the claims made for the technology are examined, and the potential roadblocks, such as: cycle dependent fatigue, time dependent degradation of memory retention, and fabrication problems are evaluated.

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Evaluation of Ferroelectric Materials for Memory Applications

by

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Commander, United States Navy
B.S., United States Naval Academy, 1971

Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

The technical literature on ferroelectric materials and memory devices was reviewed to evaluate the potential for ferroelectric data storage systems in military applications. This thesis discusses the physical mechanisms and examines the claims made for the technology. The potential roadblocks, such as cycle dependent fatigue, time dependent degradation of memory retention, and fabrication problems are evaluated in terms of the impact on memory devices. This thesis describes the proposed designs and weighs their relative advantages. There are numerous applications for ferroelectric memories as the obstacles to full production are eliminated. A joint NPS/industry space evaluation of engineering prototype devices outlined will provide qualification data for applications requiring radiation tolerance.

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I. INTRODUCTION

An exciting new memory technology, using ferroelectric materials, offers the potential for the "ideal" semiconductor memory. This new technology has a tantalizing array of capabilities: nonvolatility, radiation-hardness, low power, increased density, and high speed. With the read/write speeds and operating life predicted by its advocates, ferroelectric memories will be stiff competition for EPROMs and EEPROMs, and further development could bring their cost-per-bit down and performance up until they are direct competition for DRAMs [Ref. 1: p. 12]. In the longer term, by providing nonvolatility without sacrificing performance, ferroelectric memories could replace several currently used memory devices, thus greatly simplifying system architectures.

A. FERROELECTRIC MATERIALS

This new memory concept exploits a unique characteristic of ferroelectric materials, the ability to store binary data in the state of the material itself. Under the influence of an external electric field ferroelectric materials exhibit a spontaneous electric polarization which remains after the electric field is removed. Reversal of the electric field causes polarization in the opposite direction. A plot of the polarization P versus applied field E, as shown in Figure 1, results in a characteristic hysteresis curve analogous to ferromagnetic hysteresis. In fact, the name "ferroelectrics" is derived from this analogy, although none of the materials of current interest are ferrous. Ferroelectric materials can thus be modeled as bistable capacitors with two distinct polarization thresholds. The significant detail is that no external electric field or current is required to maintain the polarization; a finite value of polarization exists at zero applied field and will remain until switched by an applied electric field. The memory devices under development use this bistable polarization of ferroelectric

materials to store binary data. The state of polarization is read by measuring displacement current versus direction of applied electric field. The characteristics of ferroelectric materials are well known, but have not previously been exploited for memory applications because of limitations in thin film deposition and memory design.

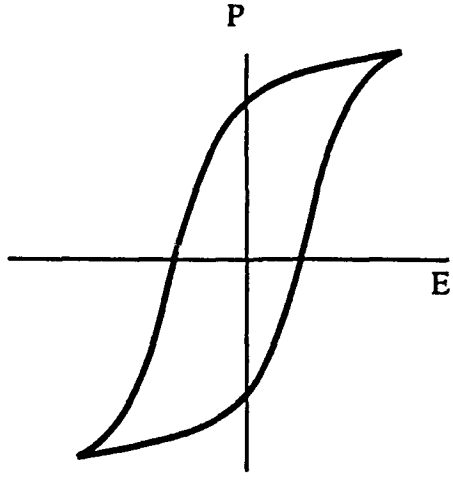

Figure 1. Polarization versus Applied Electric Field

B. PREVIOUS RESEARCH

This is not the first time the potential of ferroelectric materials for memory applications has been recognized. Over twenty years ago there were several corporate and university programs attempting to exploit the ferroelectric effect to produce a memory device. These earlier efforts focused on thick-film or bulk ferroelectrics, which required external electric fields in excess of 40 v, well above semiconductor voltage requirements. These thick-films were also very slow to switch polarization states, making them uncompetitive with existing technologies. Additionally, the coercive voltage for most ferroelectrics is not well defined, but depends both on the level of the field and the duration of application, which made the historical approach to design of a ferroelectric memory susceptible to "half select" or

integration problems [Ref. 2: p. 65]. Also, in many ferroelectrics previously tested, it is difficult to detect the polarization reversal. Most significantly for current design efforts, many ferroelectric materials exhibited polarization-reversal-dependent material degradation (fatigue) and data retention problems, such as time-dependent signal loss (aging) and a tendency to return to a previous state after polarization, which even today have not been completely eliminated.

These and other problems, apparently inherent in the materials being evaluated, led to the termination of research efforts. IBM, as a typical example, ended its effort in 1973 because of seemingly insurmountable difficulties with read/write cycle material degradation and retention of data [Ref. 3: p. 2]. Ferroelectrics have proven to be practical in other areas, such as piezoelectric transducers, pyroelectric detectors, and electro-optics, but ferroelectric memories are still under development.

In the past fifteen years much progress has been made in the fabrication of thin-film materials, and recent breakthroughs might bring ferroelectric memories into commercial reality. Most of the memory devices under development are based on conventional CMOS circuitry and will be completely compatible with existing designs and fabrication procedures. At the present time several companies (McDonnell-Douglas, Raytheon, Westinghouse, National Semiconductor, Ramtron, TRW, and Harris, among others) are engaged in developing memories based on ferroelectric materials. The reason for this interest is clear; the potential applications of a nonvolatile semiconductor memory device require no great imagination.

C. ADVANTAGES OF FERROELECTRIC MATERIALS

In addition to non-volatility, ferroelectric memories offer other advantages as well: radiation hardness, low power, high bit density, high speed, and compatibility with silicon (Si) and gallium arsenide (GaAs) fabrication.

Since the polarization state is not affected by radiation, the ferroelectric memory is inherently radiation-hard. Gamma radiation, high energy particles, or neutrons must physically displace ions in the crystal lattice to impact the polarization state. Ferroelectric materials have exhibited tolerance of more than $5x10^6$ rad (Si) of high-energy x-rays/cm^2 with a dose rate 10^{11} rad/cm^2s, and 10^{14} 1-Mev neutrons/cm^2 without performance degradation [Ref. 4: p. 1400]. Basically, the radiation hardness of a ferroelectric memory device is determined by the hardness of the underlying control circuitry.

The potential for higher bit densities results from the relatively large signal, or charge density differential between the switched and unswitched state, available for the read process. The charge density differential for Lead-Zirconate-Titanate (PZT) films is approximately 8-15 $\mu C/cm^2$ [Ref. 3: p. 6, Ref. 5: p. 31, Ref. 6: p. 213], which is more than 100 times that of DRAMS, with a typical 0.1 $\mu C/cm^2$ charge. This allows higher bit densities since the ferroelectric capacitors can potentially be made much smaller than DRAM cells.

Ferroelectric materials also promise low power and high speed. Ferroelectric memories are voltage driven (magnetic materials are current driven) which allows the use of high impedance, low power circuitry. Compared with EEPROMs, with millisecond write times, ferroelectric memories have achieved write times of 20-60 nanoseconds [Ref. 3: p. 7, Ref. 7: p. 220, Ref. 8: p. 130, Ref. 9: p. 1440, Ref. 10: p. 5470] and have the potential for more speed [Ref. 6: p. 213, Ref. 11: p. 211, Ref. 12: p.1, Ref. 13], which will make them competitive with DRAMs. They also promise extended read/write endurance with 10^{12} read/write cycles [Ref. 3: p.67, Ref. 5: p. 31, Ref. 11: p. 213, Ref. 12: p. 3], while EEPROMs typically wear out after 10^5 cycles [Ref. 14: p. 32].

II. BASIC PHYSICAL MECHANISM IN FERROELECTRIC MATERIALS

A. DEFINITION OF FERROELECTRICITY

Before continuing with discussions of applications, definitions for important parameters of ferroelectric materials will be developed and the physical mechanisms of these materials explored. The fundamental characteristic of ferroelectric materials, which differentiates them from the larger class of dielectric materials, is a spontaneous electric polarization (measured as charge per unit area) that can be reoriented by the application of an external electric field [Ref. 15: p. 9].

B. CHARACTERISTICS OF FERROELECTRIC MATERIALS

All dielectric materials exhibit a polarization when an external electric field is applied, but it is not permanent; when the electric field is removed, the polarization disappears. Those dielectric materials whose crystal structure lacks a center of symmetry can exhibit piezoelectricity; that is, application of mechanical stress will induce an electric charge and, inversely, application of an electric field will produce proportional strain. A smaller subgroup of these piezoelectric materials have a unique polar axis in the unstrained condition, that is, the unit cells are aligned such that the dipole moments produce a finite and permanent polarization. The resultant electric dipole moment changes in magnitude when the material is uniformly heated or cooled, generating an electric charge at the surface of the material as the polarization changes. This effect is termed pyroelectricity. All ferroelectrics are both piezoelectric and pyroelectric, but they are unique in that they

possess a spontaneous polarization which can be reversed with the application of an external electric field.

1. Crystal Structure

This reversible polarization is the result of the structure of the ferroelectric atom. Figure 2 is a representation of the unit cell of an ABO_3 perovskite, typical of most of the ferroelectric materials of interest. The A cation at the corners of the unit cell has a large atomic radius, while the B cation is relatively small. The oxygen atoms positioned at the face centers have the largest atomic radius. In a ferroelectric material the structure is polar, usually tetragonal, orthorhombic, or rhombohedral [Ref. 16: p.17]. M· `of the materials of interest for memory applications are tetragonal, with the exception of potassium nitrate (KNO_3). With tetgragonal structure, a cubic cell is stretched along one axis and shrunk along the two others. The longer axis is referred as the *a* axis and the shorter are called the *c* axes. The asymmetric position of the B ion, resulting from a difference between the center of positive and the center of negative charge, gives the unit cell its electric dipole. The external charge resulting from the dipole is the polarization, expressed in $\mu C/cm^2$. It can be seen from the figure how the new polarization of the cell is "locked in" by the attractive-repulsive forces in the unit cell until an external field moves the B ion either from the lower to the upper position or vice versa. In lead zirconate titanate (PZT), the A ions are primarily lead, with some of the lead replaced by zirconium, and the B ions are titanium. Ferroelectric materials are characteristically formed from ions with certain valance relations and atomic size ratios and it is possible to generate a list of candidate materials with specific characteristics using these two criteria [Ref. 17].

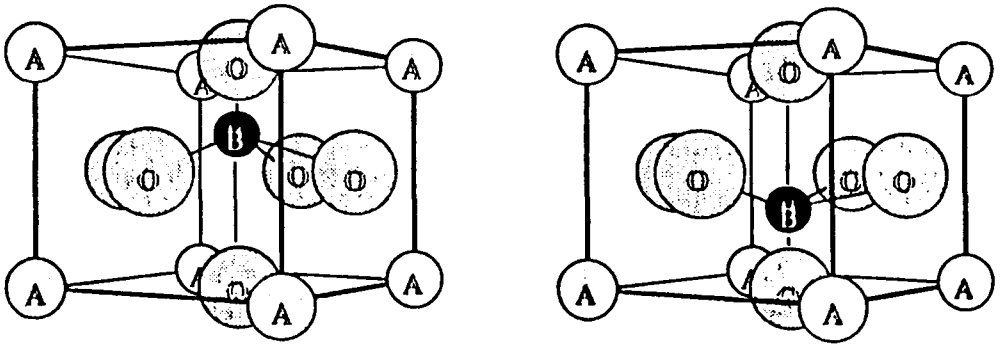

Figure 2. ABO_3 Unit Cell

The switchability of polarization implies that the energy "hump" between directional states is relatively low. It further implies that the nonpolar state is only slightly less stable, so increasing the temperature will cause the material to become nonpolar [Ref. 16: pp. 11-12]. In fact, ferroelectric materials have a particular temperature at which there is a transformation to a nonpolar (cubic) structure and the spontaneous polarization disappears. This transformation temperature is called the Curie point (T_c); above the Curie point the material is said to be in a paraelectric phase. In the paraelectric phase, the dielectric permittivity follows Curie-Weiss behavior; that is, the dielectric permittivity is inversely proportional to the difference between the temperature of the material and the Curie temperature

$$K = C/(T - T_c) \qquad (1)$$

where K is the relative dielectric constant, C is the Curie constant, and T_c is the Curie temperature. [Ref. 16: p. 13] There is generally a substantial discontinuity of the electrical, optical, mechanical and thermal properties of a ferroelectric material near T_c. In PZT T_c is

approximately 360°C and it exceeds 250°C in the other materials of interest for memory applications.

2. Polarization

As a sample of ferroelectric material is brought from the high-temperature paraelectric state through T_c to the ferroelectric state, it develops the polar, or asymmetric crystal lattice, structure. This polar structure displaces the ionic and electronic charges within the unit cell, resulting in a microscopic electric dipole moment. In ferroelectric materials, the unit cells cooperatively align parallel with neighboring cells within a region called a domain, a homogeneous region where there is a common orientation of the dipole, resulting in a uniform spontaneous polarization. Since separate domains are randomly polarized, the electric dipole moments will tend to cancel each other and there may be no net macroscopic polarization.

To achieve a macroscopic polarization of the ferroelectric material so there is a net remanent polarization, it is "poled". Poling is the application of a dc electric field to reorient the polar axis of the domains in a common direction [Ref. 15: p. 13]. Since the field required to reorient the domains is usually a minimum at T_c, poling is commonly accomplished by cooling through T_c with an applied electric field. Poling at relatively high temperatures is recommended to improve the fatigue resistance of the sample [Ref. 3: p. 3]. The magnitude and duration of poling required varies from material to material.

As previously noted, the unique characteristic of a ferroelectric material is the polarization response of the material to an applied electric field. After the poling electric field is removed, the material will retain a net polarization which is defined as the remanent polarization (P_r). When a voltage is applied in the opposite direction, the polarization will switch directions to the opposite sign. The reversal of an electric field applied to a linear

dielectric results in the response curve of Figure 3a, while the distinctive hysteresis loop characteristic of ferroelectric materials under the same conditions is shown in Figure 3b.

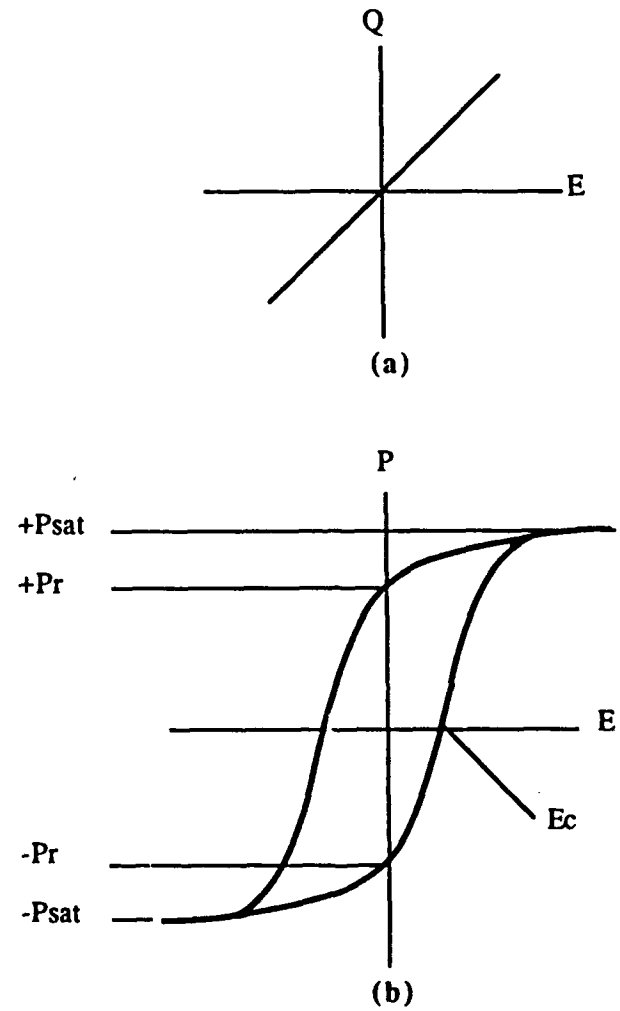

Figure 3. Linear Dielectric and Ferroelectric Capacitive Response Curve (After Ref. 15)

Measurement of the polarization response versus applied electric field can be done using a Sawyer-Tower circuit as shown in Figure 4 [Ref. 18: p. 270]. A large integrating capacitor is placed in series with the sample so that most of the voltage drop in the circuit is across the sample. Thus, V1 is a close approximation of the voltage across the ferroelectric

sample, and V2 is proportional to the charge (q) flowing through the material. The polarization (P) in $\mu C/cm^2$ is calculated from

$$P = q/A \tag{2}$$

where A is the electroded area of the ferroelectric material. The polarization can reach values as high as 500 $\mu C/cm^2$, although it is more typically 10-38 $\mu C/cm^2$ for the materials of interest for memory applications [Ref. 19: p.122]. The electric field (E) is calculated from

$$E = V/d \tag{3}$$

where d is the thickness of the sample [Ref. 20: p.3].

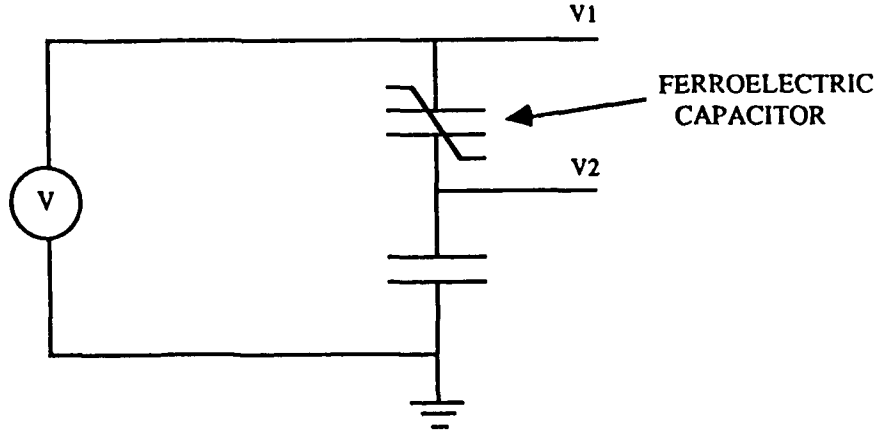

Figure 4. Sawyer-Tower Circuit (After Ref. 18)

A ferroelectric memory capacitor is written to by the application of an electric field which orients all the dipoles in a common direction. To "read" the device, an electric field is again applied to the capacitor. If the dipoles are in the direction of the applied field, a current pulse corresponding to the charging current of the capacitor is generated. This current can be considered proportional to the linear dielectric of the capacitor. If, however,

the dipoles are oriented in the opposite direction, a larger current pulse forms, consisting of the capacitor charging current and the switching current caused by the switch in polarity of the dipoles. The "read" operation in most memory designs under consideration involves detecting the difference between the two output signals to determine whether a "one" or a "zero" was stored. It is important to note that when the "read" operation requires polarization reversal, it is destructive; the data must be rewritten to the memory cell following the "read". Figure 5 shows the current response as a function of time for each of the four read situations: negative voltage pulse followed by a positive voltage pulse (P), two consecutive positive pulses (U), positive pulse followed by negative pulse (N), and two consecutive negative pulses (D). The difference between P and U, or N and D, is the signal charge, and is 13.8 $\mu C/cm^2$ in this example [Ref. 6: p. 213]. This large signal makes the technology highly scalable; a 1x1 μm capacitor will provide approximately 200 mv differential in-line voltage.

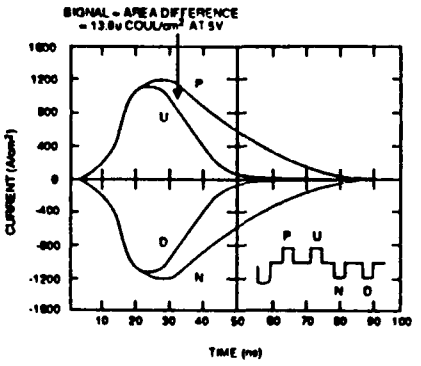

Figure 5. Switching Current versus Time for a Ferroelectric Capacitor (From Ref. 6)

This hysteresis loop response of polarization to the applied electric field defines three parameters which are useful for the classification of ferroelectrics: remanent

polarization (previously defined), coercive field, and saturation polarization. These parameters are also labeled on Figure 3b.

The electric field required to reverse the polarity from +Pr to zero is defined as the coercive field (E_c). For memory applications the coercive field is the digital switching voltage of the memory cell. As an electric field larger than E_c is applied, the polarization will continue to increase (although at a slower rate) until all domains are aligned in the new direction; at this point the P versus E curve becomes linear. Extrapolation of the linear extreme of the plot is defined as the saturation polarization (P_{sat}). For typical measurement of P_{sat}, the polarization at $3*E_c$ is used.[Ref. 20: p. 39]

The hysteresis loop is generally symmetrical about the origin ($+E_c = -E_c$, $+P_r = -P_r$). However, mechanical clamping, doping, radiation treatment [Ref. 20: p. 40], and space charge shielding [Ref. 21: p. 1242] can cause asymmetry or distortion of the loop. The loop parameters are functions of the dimensions and treatment of the specimen, temperature, pressure, type of electrodes, magnitude and frequency of the applied switching field, and the material's electrical and thermal history [Ref. 20: p. 40, Ref. 22: p. 3]. Generally, higher frequencies and temperatures decrease the values of P_r and P_{sat}. The coercive field increases as a function of the rate of polarization reversal [Ref. 15: p. 14].

The actual mechanism of polarization reorientation is a sequential process which begins with the nucleation, or reorientation, of small regions. After these regions, usually near the surface, reach a critical size, their growth rate becomes approximately exponential. The time to reach the critical size is termed nucleation time and is on the order of one nanosecond for barium titanate ($BaTiO_3$) and KNO_3. [Ref. 11: p. 209]

The sequence continues with the growth of domains in the direction of the applied field. These domains can usually be considered to grow at the speed of sound in solids, or approximately one km/sec in the materials of interest. Thus, for a one micron film, the

forward growth time is comparable to the nucleation time. The process of switching is complete when the needle-like domains begin to spread laterally until the entire sample has switched to the opposite polarization. In most ferroelectrics, the time for lateral growth is the dominant factor in switching time and is strongly affected by the applied electric field; larger fields reduce the switching time (Figure 6) [Ref. 15: p. 14]. The circuitry used and the size of the cell also influence the switching speed, with smaller size and lower load resistances decreasing switching time. In KNO_3 the switching times vary between 11 nsec and 10 μsec, depending on the applied field, external circuit, and cell size as shown in Figure 7 [Ref. 11: p. 211].

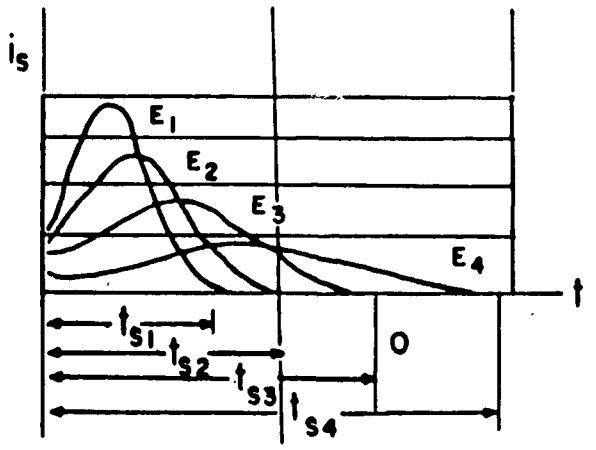

Figure 6. Switching Time versus Applied Electric Field ($E_1>E_2>E_3>E_4$) (From Ref. 15)

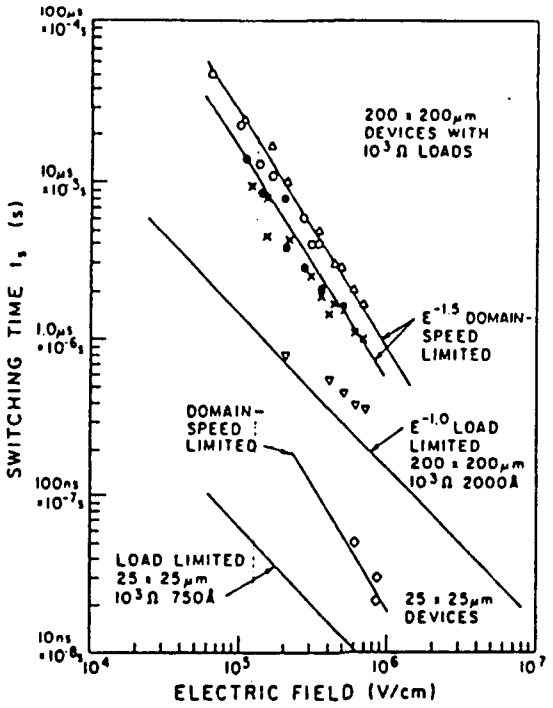

Figure 7. Switching Time versus Cell Size, External Resistance, and Applied Electric Field (From Ref. 11)

3. Other Properties of Ferroelectric Materials

Another distinction shared by ferroelectric materials is the possession of anomalously high values for dielectric permittivity, ε. Ferroelectric materials have values of ε in the range of 100-20,000, much higher than the values of 1-10 normally associated with nonpolar dielectrics [Ref. 16: p. 8, Ref. 20: p. 360, Ref. 23: p. 266]. This is commonly referred to as the dielectric constant, but since it is not constant, but a function of both electric field and temperature in ferroelectric materials, dielectric permittivity is more appropriate. The dielectric permittivity is a nonlinear function of the electric field and is nearly proportional to the slope of the P-E curve [Ref. 24: p. 19]. The curves in Figure 8 illustrate the typical temperature dependency for ferroelectrics, with a large discontinuity at the Curie point, above which the dielectric permittivity conforms with the Curie-Weiss Law [Ref. 20: p. 36, fig. 3.1]. It should also be noted that the dielectric permittivity is

different for each axis of the basic crystal structure [Ref. 20: p. 36]. The dielectric permittivity is also a function of material composition and structure, frequency of the applied electric field, and time. The capacitance of the ferroelectric capacitor is calculated from

$$C = \varepsilon_r \varepsilon_0 A/d \tag{4}$$

where C is the capacitance in Farads, ε_r is the relative permittivity, ε_0 is the permittivity of free space, A is the area of the capacitor, and d is the distance between plates. As shown in equation (4), the capacitance is a function of the dielectric permittivity. Since most memory sense circuits are based on the Sawyer-Tower circuit, the capacitance of the ferroelectric memory capacitor must be fixed relative to the sense capacitor. Thus, a ferroelectric material used for memory applications must have a dielectric permittivity that is relatively stable over a wide range of temperatures.

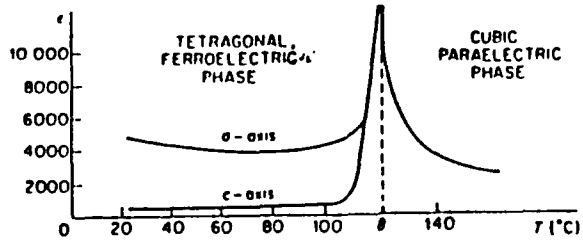

Figure 8. Dielectric Permittivity versus Temperature (From Ref. 20)

3. DESIGN AND ENVIRONMENTAL INFLUENCES

1. Electric Field/Film Thickness

Remanent polarization, switching speed, aging, and fatigue are all dependent on the external electric field applied to the ferroelectric memory capacitor . Since the applied

electric field is a function of the circuit voltage (which is fixed if the device is to be compatible with existing logic levels) and film thickness, as shown in equation (3), the parameters listed above are also functions of film thickness. With larger applied electric fields remanent polarization, switching speed, and aging rate increase [Ref. 25: p. 569, Ref. 26: p. 170, Ref. 27: p. 4]. However, larger applied fields appear to reduce the rate of fatigue, although from the published data it is difficult to determine if the fatigue rate actually decreases, or if the larger field, by increasing the remanent polarization, is masking the effect of fatigue [Ref. 3: p. 6]. If the initial remanent polarization is large enough to provide sufficient aging margin, a larger field will give improved speed performance and greater readable signal.

Independent of the expected relationship between applied voltage, film thickness, and resulting electric field, film thickness influences the dielectric permittivity, remanent polarization, and coercive field [Ref. 28: p. 2717, Ref. 29: p. 788]. Figure 9 shows a plot of the coercive field versus film thickness for KNO_3 [Ref. 26: p. 168]. The dependencies of E_c and switching speed on film thickness support theories of three-dimensional domain switching, where the lateral domain wall velocities are the rate-limiting factor in polarization switching [Ref. 26: p. 170].

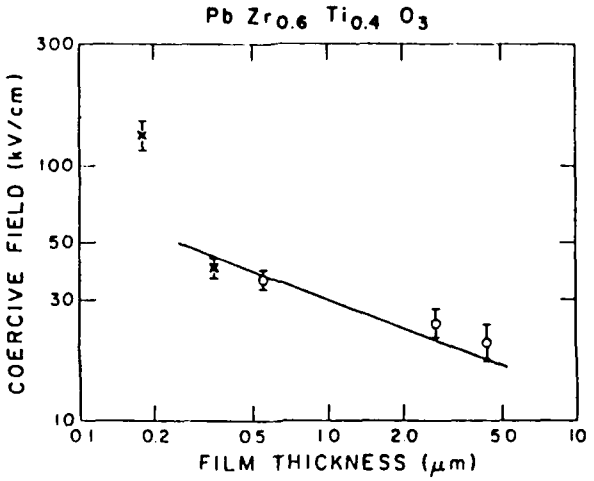

Figure 9. Coercive Field versus Film Thickness (From Ref. 29)

The effects of electric field and film thickness are competing factors in the design of an integrated memory cell. Faster operation requires thinner films, but, as the film thickness is reduced, E_c increases. Since the device operating voltage is fixed by standard semiconductor voltages, the increase in E_c sets a minimum thickness of 100-400 nm for KNO_3 [Ref. 11: p. 209, Ref. 25: p. 569].

2. Temperature

As previously mentioned, the properties of ferroelectric materials are functions of temperature. This includes the remanent polarization of the material, one of the critical parameters for memory applications, which decreases as temperature increases until the Curie temperature is reached. The reduction is relatively gradual at lower temperatures, but becomes more dramatic as the Curie temperature is approached, at which point the material enters the paraelectric phase and the material loses its capability to switch polarization and retain a set state (Figure 10) [Ref. 20: p. 40]. For memory applications this temperature dependence must be considered in the design process when establishing the required minimum levels of initial remanent polarization. This dependence on

temperature also limits the materials useful for memory applications to those with Curie temperatures significantly above the maximum military specification of 125°C.

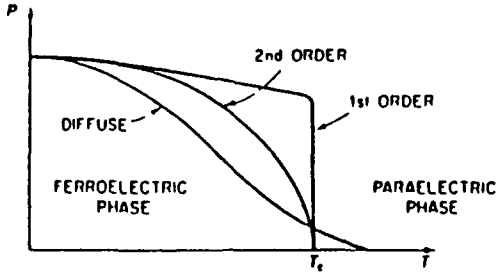

Figure 10. Remanent Polarization versus Temperature (From Ref. 20)

Switching time is also a function of temperature. As temperature increases toward T_C, the switching speed of the material increases. Switching time extrapolates to zero as the temperature goes to T_C [Ref. 29: p. 790]. Figure 11 shows this relationship for PZT thin-films [Ref. 29: p. 790, Fig. 6].

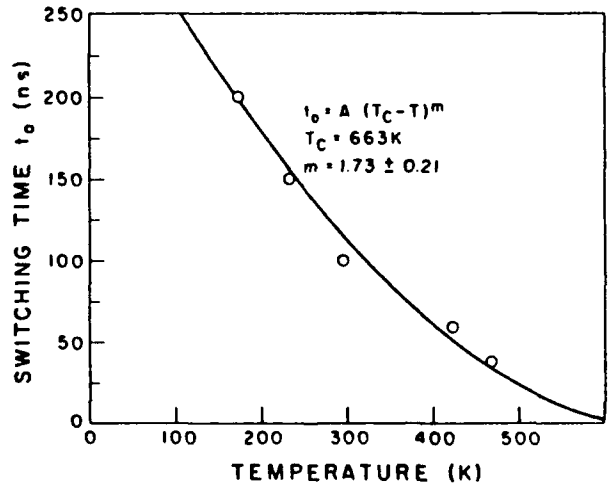

Figure 11. Switching Time versus Temperature (From Ref. 29)

Increased temperature while cycling polarization states can also act as an aging and fatigue accelerator. Operation of a ferroelectric capacitor at high temperature--above

approximately 85° C--increases the effect of polarization cycling and reduces the signal retention time by increasing the aging rate [Ref 27: p.4]. Increased temperature also increases the nonswitching response, which further complicates sensing the stored state in memory applications since the switched and unswitched signal are usually compared in a complementary fashion [Ref. 27: p. 4, Ref. 29: p. 790]. The increased nonswitching response is probably due to domain wall contribution to ε [Ref. 29: p. 790]. This acceleration begins at approximately 85° C and grows as temperature increases. The effect on data retention at the high end of the military operating range (125°C) can be significant, and must be considered in memory cell design and establishing retention/fatigue specifications.

3. Radiation Effects

Ferroelectric materials are extremely tolerant of radiation exposure. The function of the material as a memory relies on the "permanence" of the polarization and its ability to switch states with an applied electric field, and neither the polarization nor the switchability of the material is easily affected by low doses of radiation. For example, $BaTiO_3$ was exposed to up to 10^{12} neutrons/cm^2 with no effect on the ferroelectric properties of the material. Exposure to a greater flux of 10^{13} - 10^{16} neutrons/cm^2 caused reduction in the coercive field and remanent polarization, while 10^{17} - 10^{20} neutrons/cm^2 caused continued degradation of the material until samples subjected to doses above 10^{20} neutrons/cm^2 lost all ferroelectric properties [Ref. 16: p. 90, Ref. 30: p. 116]. Other tests have shown that exposure to x-ray, gamma-ray, neutrons, and electrons can also produce asymmetries in the hysteresis loop and structural changes in the material, but that relatively high levels of exposure are required [Ref. 20: p. 39-40].

Radiation tests conducted by the Naval Surface Weapons Center and Raytheon Corporation on PZT test devices produced by Krysalis Corp. demonstrated that

ferroelectric capacitors are radiation-hard with respect to total dose, dose rate, neutrons, and single event upset [Ref. 12: p. 3, Ref. 31: p. 1, Ref. 32: p. 2]. Test devices were exposed to the following radiation environment: dose rate of 10^{11} rad(Si)/s, total dose of $5x10^6$ rad(Si), and $6x10^6/cm^2$ heavy ion fission fragments from a californium-252 fission process with approximately 200 MeV of energy without significant degradation to the hysteresis loop characteristics [Ref. 31: p. E-16]. In a second, more exhaustive, test the ferroelectric test capacitors were exposed to 1 Mev equivalent neutrons under two conditions, 10^{14} neutrons/cm^2 while reading the polarization state and static exposure to 10^{15} neutrons/cm^2 followed by device characterization. The capacitors retained the programmed polarization state and hysteresis loop characteristics. [Ref. 32: p. 2]

Test capacitors and the Krysalis 512-bit UniRAM were evaluated for radiation effects from a 30 nsec x-ray pulse of $1.2x10^{11}$ rads/sec. The ferroelectric capacitors demonstrated no susceptibility to high transient dose rate errors. The 512-bit memory showed no increase in errors resulting from the x-ray pulse. Total dose gamma radiation tests were conducted by Sandia National Laboratories, Raytheon, and the Naval Surface Warfare Center and the ferroelectric devices were exposed to 14 MRads from a Cobalt 60 radiation source with no apparent effect on the material or the stored data. Additionally, there was no damage evident when the parts were electrically stressed during exposure to $4.8x10^6$ rads from the Cobalt 60 source. [Ref. 32: p. 2]

Tests of potassium nitrate (KNO_3) demonstrated tolerance of $4x10^{12}$ to $4x10^{13}$ 1 MeV neutrons/cm^2 without memory degradation [Ref. 11: p. 212], although other tests of KNO_3 memories indicates some susceptibility to gamma-ray damage. Four packaged memory devices were subjected to $0.5x10^6$ rad of 1.17 MeV gamma-rays from a Cobalt 60 radiation source, with mixed results. One of the devices retained full function, a second suffered non-radiation related failure, and two had severe polarization loss indicative of

radiation damage. It was theorized that the irradiated parts failed due to development of bias voltages from the radiation-produced charge defects. Data concerning the underlying circuitry is not available, so the effect of the radiation on the non-ferroelectric portions of the memory cannot be determined [Ref. 33: p. 1].

The switching characteristics of PZT-based packaged memories were evaluated by Scott, et al., which indicated that under some bias conditions radiation damage may occur with lower total dose exposure levels. Five packaged devices with a total of 18 PZT capacitors were divided into three groups which were exposed to 5.04 MRad total dose under three voltage conditions: 5.0 v dc bias, open circuit, and short circuit conditions. Some impact from the radiation exposure was evident but the memories remained functional. The performance of the devices with a 5.0 v dc bias and the open circuit condition actually improved following irradiation. Two of the eight capacitors exposed under short-circuit conditions lost sufficient polarization to preclude detection of a "one" or "zero" condition. It is proposed that this is the result of space-charge accumulation at the electrode interface during irradiation [Ref. 34: p. 1446].

In addition to total dose evaluation, tests with high dose rate x-ray pulses were conducted. The nine packaged parts containing 25 PZT capacitors were again divided into three lots and exposed to 2.6×10^{11} rad (LiF)/s, 10 nsec pulses under the same voltage conditions as the previous experiment. There were no retention failures following irradiation; in fact, total switched charge and state discrimination improved for those samples under a 5.0 v bias [Ref. 34: pp. 1450].

Radiation tests on PZT capacitors conducted by Sandia National Laboratory have also shown that radiation effects are dependent on any applied bias voltage. Parts tested with a -5.0 v bias voltage demonstrated increased the post irradiation P_r until the total dose exceeded 1×10^6 rad (Si), at which point P_r began to drop as a function of increased

radiation. However, a similar effect on device performance was not noted for parts in either the open or short circuit condition, which demonstrated degradation without the initial improvement in performance characteristics. Following irradiation, application of a dc or ac voltage restored the material characteristics. In the case of those parts exposed under a bias voltage, the subsequent application of a 10 v dc anneal resulted in over 150% improvement in P_r [Ref. 35]. The nature of these effects and the subsequent anneal indicate that the radiation impact may be primarily at the ferroelectric-electrode interface. If possible, further testing should be structured to eliminate these effects.

Theoretical analysis of the physics and circuit design requirements provides an upper limit to the radiation tolerance and extrapolates the dosages required to cause significant degradation of the ferroelectric material. An estimate of the neutron fluence required to cause sufficient displacement damage to effect the material is 6.4×10^{17} neutrons/cm^2. It is expected that other effects, such as changes in the lattice constant of the material, would predominate at this level of irradiation. Assuming a 0.1% change in the lattice will cause a significant degradation in the hysteresis loop, the damage threshold becomes 5×10^{16} neutrons/cm^2, still well above military requirements. Other estimates of radiation damage thresholds are total dose from high-energy gamma-rays greater than 10^8 rads (Si), ionizing dose of 2.5×10^{13} rads (Si)/s, and no sensitivity to single event upset (SEU) until the cell sizes reach 0.8 um by 0.8 um. [Ref. 36: p. 5]

Although the tests cited above appear to support the claims of radiation hardness made for ferroelectric materials, they are not conclusive. Additional testing is required to provide better understanding of the impact of irradiation on the ferroelectric material and the interface effects.

4. Grain Size

The grain size of the ferroelectric material can have a significant effect on coercive field, Curie temperature, remanent polarization, aging rate, and resistance to fatigue (aging and fatigue will be discussed in more detail in Chapter III). Coercive field, aging rate, fatigue rate, and Curie temperature are inversely related to grain size, while remanent polarization is directly related [Ref. 19: p. 122, Ref. 37: p. 86, Ref. 38: p. 4410, Ref. 39: p. 408]. These effects are apparently the result of a space charge field which builds up inside the material domains and shields the domains from the applied electric field [Ref. 21: p. 1245, Ref. 37: p. 85-86]. Polarization switching time is also reported to increase as grain size decreases [Ref. 40: pp 490-493, Ref. 41: pp. 154-155].

These relationships between the critical ferroelectric properties and grain size may be an important factor when considering which of the available deposition techniques to use, since each method produces a typical range of grain sizes. In considering the advantages and disadvantages of each method, the performance of the resulting thin-film is the ultimate performance criteria.

5. Selection of Materials for Memory Applications

All of the ferroelectric properties discussed above can vary quite widely with different materials, and since several of the materials are "solid solutions" with continuously variable compositions, even with changes to the same material. Ferroelectric materials chosen for memory applications must have several characteristics for successful device design/manufacture: adequate remanent polarization, high switching speed, acceptable rates of fatigue and aging, CMOS-compatible coercive field, sufficient operating temperature range, and compatibility with IC fabrication methods. These criteria have narrowed the list of materials being actively evaluated for memory applications to PZT, $BaTiO_3$, lead germanate ($Pb_5Ge_3O_{11}$), barium manganese fluoride ($BaMgF_4$), and lithium

niobate ($LiNbO_3$), with PZT as the current favorite. Although KNO_3 has many desirable properties and has been extensively studied, it is also extremely hygroscopic and has proven too difficult to integrate into semiconductor fabrication processes. With over 1400 other ferroelectric materials to evaluate, others may be discovered with even better memory properties.

III. DEGRADATION MECHANISMS IN FERROELECTRIC MATERIALS

There are three degradation effects in ferroelectric materials which are of interest in memory applications. The first of these is commonly called aging and refers to the time-dependent degradation of the material with no polarization switches, or in the case of a memory, no reads or writes. The important feature is the passive nature of aging. The second mechanism of interest, fatigue, is the result of repeated polarization reversals. Thus fatigue is dependent on the number of read-write cycles the material has experienced. The third degradation mechanism is referred to as "waiting time" and is the inclination of some materials to switch back to a preferred state, following domain reorientation due to an external electric field.

These terms, although commonly used, are not standard, and a great deal of confusion exists on proper terminology. Aging and fatigue are frequently used to refer to the same phenomena and other terms, such as retention and endurance, are occasionally used in the literature. A standardization effort was initiated at the Ferroelectric Materials Tutorial (28-29 March 1989) sponsored by the Naval Postgraduate School and led to the creation of the IEEE Thin-film Standards Committee.

In the absence of a standard definition, aging will be defined as the loss of remanent polarization that occurs with no external electric field applied to the material. The loss is not recovered by the application of an electric field which causes a single polarization switch; however, the sample may be "de-aged" by extended polarization cycling (10^3 cycles). Fatigue will be defined as the loss of remanent polarization that occurs when the material is subjected to an external electric field which either switches the polarization state

or reinforces the existing state by driving the polarization from $\pm P_r$ to $\pm P_{sat}$. Waiting time will be defined as the spontaneous reorientation of the material to a preferred state.

A. AGING

Aging decreases the dielectric permittivity, remanent polarization, and coercive field. Saturation polarization (P_{sat}) may also decrease, but this is not evident in all materials. The hysteresis loop changes shape and/or shifts along the abcissa as a result of the degraded polarization. Figure 12 shows examples of typical effects on an aged sample. Aging effects are not exponential, but occur linearly with the logarithm of time [Ref. 16: p. 28, Ref. 42: p. 3, Ref. 43: p. 725, Ref. 44: p.57, Fig.1].

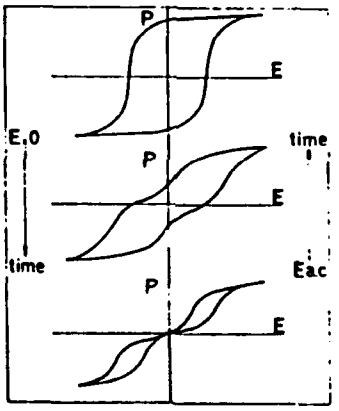

Figure 12. Aging Effects on the Hyteresis Loop (From Ref. 44)

A word of caution is appropriate here: The research cited here dated prior to 1986 is predominantly of thick-film ferroelectric materials. Search of the literature shows relatively little evaluation of the aging process in thin-film materials.

It is generally accepted that aging is a result of stabilization of the domain pattern in the ferroelectric material [Ref. 44: p. 57]. However, the mechanism at work is not fully understood. One of the theoretical explanations of the aging phenomena is the relaxation of

the domain structures into more stable, lower stress configurations [Ref. 16: p.28 & 84, Ref. 42: p. 10, Ref. 43: p. 725, Ref. 45: p. 199].

Most of the ferroelectric materials of interest (BaTiO3, PZT) are cubic in the paraelectric phase and tetragonal in the ferroelectric phase (below the Curie Temperature). As the unit cell stretches from the cubic to the tetragonal structure, internal strain is created since the change in structure cannot be accommodated without deformation of the unit cell if material continuity is to be maintained. Additionally, when the material cools through the Curie temperature, the nucleating domains are randomly oriented. Because of this random orientation, the sample will not be in the most stable or lowest energy state [Ref. 43: p. 725]. Over time the domain structure will move toward a more stable state (lower stress), causing the material characteristics to change. In a tetragonal crystal structure this results in domains oriented with lattice axes 90° apart. The reorientation of domains to 90°-domains has been observed by electron microscope by Ikagama and Ueda and, separately, by Brandt and Ansell, who also noted that the change tended to occur at a rate equal to the aging rate of the material [Ref. 43: p. 728, Ref. 45: p. 196]. As the domains reorient they become trapped or "clamped" in the new configuration and so the ability of the material to switch polarization is reduced.

The rate of aging is strongly correlated with the degree of tetragonality in the sample crystal structure [Ref. 42: p. 5, Ref. 43: p. 725]. The rate of aging appears to decrease with increasing tetragonality, which is supported by the aging rates in different materials with differing degrees of tetragonality. Also the aging rate decreases as the material is brought toward the transition temperature from below and the ratio of the *c* axes (shorter axes) to the *a* axes (longer axes) decreases in a given material as the temperature increases toward the transition temperature.

Another theory of the cause of the aging effect in ferroelectric materials is that it depends on the distribution and mobility of space charge in the material [Ref. 21: p. 1236, Ref. 37: p. 82, Ref. 46: p. 1551, Ref. 47: p. 403, Ref. 48: p. 145, Ref. 49: p. 96]. M. Takahashi noted that domain switching is largely the result of shielding by an internal space charge field accumulating at domain boundaries. This space charge is ionic in nature and may result from dopants, impurities, or vacancies [Ref. 47: p. 403]. The effects of this space charge as proposed by Takahashi are explained below.

In a ferroelectric film subjected to an external electric field, E_{ext}, the domains will align in the direction of the applied field, developing spontaneous polarization, P_S. Following removal of the field, space charge will collect at the domain wall to counteract the field produced by P_S. Thus the space charge field will be oriented in the same direction as the previously applied electric field, as shown in Figure 13a.

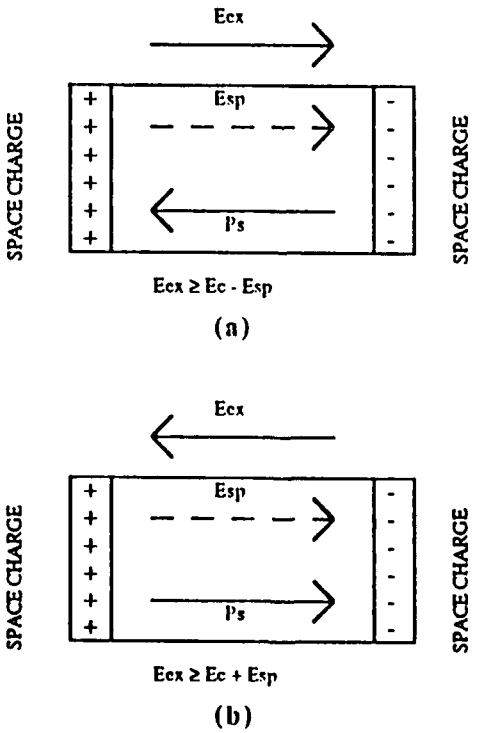

Figure 13. Space Charge Field (From Ref. 21)

To reverse the polarization, the applied electric field must be large enough to overcome the space charge field, i.e., $E_{ext} > E_{sp}+E_c$. Returning the polarization to the original direction requires an external field (E_{ext}) greater than the difference of the space charge field and E_c, as shown in Figure 13b.

Because of the presence of the space charge field, the external field required for polarization switching is dependent on direction and the hysteresis loop is no longer symmetric ($+E_c = -E_c$ and $+P_r = -P_r$), but is shifted horizontally along the E axis. The magnitude of the space charge field, E_{sp}, increases with increased aging time at both 35°C and 80°C as shown in Figure 14 [Ref. 21: p. 2145, Ref. 37: p. 84 and Fig. 7a, Ref. 41: p. 154, Fig. 2, Ref. 49: p. 96]. The shift of the hysteresis loop may result in a read error since the charge differential has been reduced for the storage of either a "one" or a "zero", depending on the storage convention selected. It has been reported that the polarization switching time also becomes dependent on direction as the material ages [Ref. 41: pp. 154-155, Fig. 3]. As is shown in Figure 15, the switching time is faster when the applied electric field is in the same direction as the space charge field.

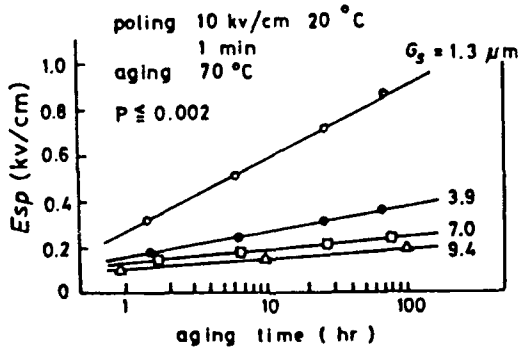

Figure 14. Space Charge Field versus Time (From Ref. 41)

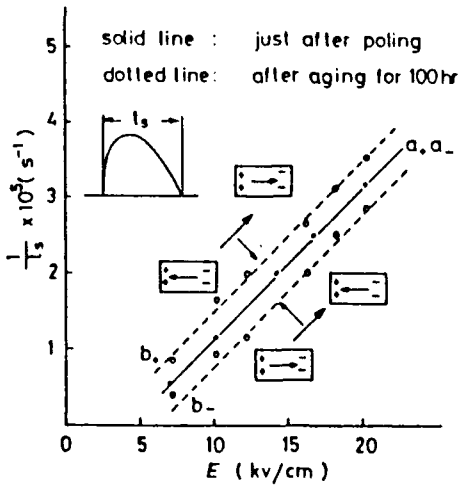

Figure 15. Switching Time versus Direction of Applied Electric Field (From Ref. 41)

When the polarization is reversed several times the hysteresis loop is restored to a symmetric shape, suggesting dispersal of the space charge. It has also been noted that the larger the resistivity of the material, the more slowly the space charge relaxes [Ref. 21: p. 1243]. Donor doping of the material significantly increases the resistivity [Ref. 49: p. 100] and thus increases the number of polarizations required to restore symmetry to the hysteresis loop. In some materials the space charge is quite stable and may require up to 10^5 polarization reversals before loop symmetry is achieved [Ref. 37: p. 84, Fig. 7b].

The correlation of aging rate with the addition of dopants has been reported by others. The general tendency is consistent, but the degree of the effect is not consistent throughout the literature. It has been reported that doping PZT with donor impurities lowers the aging rate, while acceptor dopants have little effect on the aging rate [Ref. 20: p. 37, Ref. 42: p. 22]. Others have reported that acceptor doping strengthens the internal bias field, i.e., increases the aging rate, and that donor doping has little effect on the bias field or stabilizing the polarization [Ref. 49: p. 100]. Although these reports are not entirely in agreement, the implications support the same theory of space charge generation. Doping

with donors or acceptors is thought to reduce or increase oxygen vacancies in the material, in turn reducing or increasing the electrolytic migration of the vacancies which may also contribute to the aging process [Ref. 20: p. 37, Ref. 49: p. 100]. The pinning of the domain walls is a result of the accumulation of defects, such as oxygen vacancies, at the walls [Ref. 16: p. 845].

As previously discussed, the space charge field is also affected by grain size and porosity of the material. A decrease in grain size results in an increase in the space charge field as shown in Figure 16 [Ref. 37: p. 83].

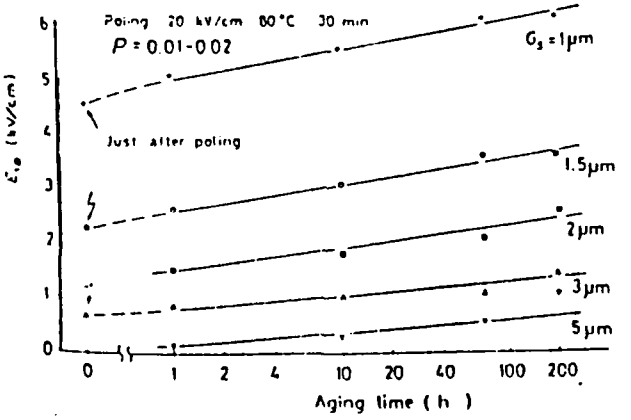

Figure 16. Aging Rate versus Grain Size (From Ref. 37)

The aged material can be restored to its original condition by heating the sample above the transition temperature (Figure 17)[Ref. 37: p.84 and Fig. 8, Ref. 42: p.4]. With $BaTiO_3$, PLZT, KNO_3 and PZT, the restoration is complete and the aging begins again at the original rate . [Ref. 20: p. 37, Ref. 37: p. 84 and Fig. 8, Ref. 48: p. 4, Ref. 50: p. 1]. The aged material can also be restored or de-aged by the application of strong ac fields for up to 10^5 [Ref. 44: p. 57]. With KNO_3 the sample dielectric permittivity, remanent polarization, and coercive field are restored, but the sample now ages at a higher rate,

indicating some form of permanent damage [Ref. 27: p. 4, Ref. 46: p. 1550]. It would appear that these restore methods support the existence of an internal biasing field.

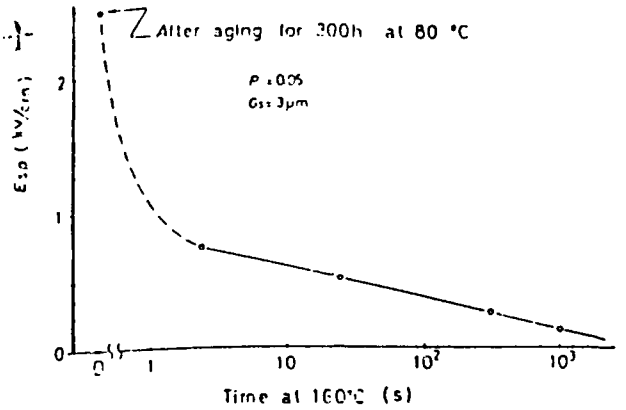

Figure 17. De-aging Effect of Temperature (From Ref. 37)

There are other theories of aging related to domain changes or reorientation. Rapoport and Dontsova state that the decrease in dielectric permittivity and remanent polarization is due to the decrease in the number of domains and therefore the area of the domain walls and a decrease in the mobility of the domain walls [Ref. 51: p. 328].

B. FATIGUE

The other major degradation effect of concern in ferroelectric memory applications is commonly termed fatigue. As a sample fatigues, the remanent and maximum polarization (P_r and P_{sat}) decrease, the coercive field (E_c) increases, the switching time (t_s) decreases, the hysteresis loop becomes less square, and microcracks and dendritic growths may appear [Ref. 46: p. 1550, Ref. 50: p. 1, Ref. 52: p. 202, Ref. 53: p. 100].

Fatigue results from repeated switching of the polarization state by cycling of the applied electric field. The rate of fatigue is a function of the material, but in materials being considered for memory applications the point of fatigue "failure" is on the order of 10^9 to 10^{12}. Failure of a memory cell is obviously a function of both the materials and the

memory cell design. The degradation effects begin after a characteristic number of cycles and then continue logarithmically.

As is the case with aging, the mechanism which causes fatigue is not fully understood. The inability of the material to switch has been generally attributed to electro-migration of ions and charge defects or the pinning of domain walls [Ref. 46: p. 1547, Ref. 54: p. 4513] although Salaneck suggests the fatigue mechanism is the appearance of microcracks in the material [Ref. 53: p. 100].

Microcracks are commonly reported after repeated cycling, but it is unclear whether they cause the electrical properties to change or are simply another symptom of material degradation. The microcracking is an inherent effect of the mechanical coupling of the piezoelectric materials, and Salaneck attributes the increase in coercive field to the impact of the microcracks near the electrode [Ref. 53: p. 97 and 101]. However, Stewart and Consentino demonstrated that the samples could be "de-fatigued" by heating or cycling at high temperature without "healing" of the microcracks or any substantial change in their distribution [Ref. 55: p. 164-165].

Scott has reported on a Soviet theory of mobile ion diffusion causing an accumulation of space charge along domain walls. The data supporting this theory implies an activation energy typical of ion hopping in a polar crystal. This activation energy is consistent with the results of other researchers [Ref. 3: p. 5]. The Soviet work is also noteworthy for the observation that fatigue is reduced at higher temperatures. The degradation in switched charge is described by the relationship:

$$dQ/dn = A*e^{(-b/kT)} \qquad (5)$$

where Q is the switched charge; n, the number of cycles; T, temperature; and b, an activation energy of 0.7 eV.

A proposed model of the fatigue process is the growth of an inactive surface along the electrode-ferroelectric interface. The existence of a planar inactive surface, or forming layer, along the interface has been proposed by Zheludev [Ref. 56: p. 474-486]. This model suggests the accumulation of free charge at the interface between the two materials which results in a discrete capacitance and a residual resistance at the interface which affects the switched charge. It also provides an explanation for the decrease in switching time as a sample fatigues.

Another model of inactive surface formation proposed by Duiker, Beale, and Scott is the dendritic growth of oxygen deficient filaments from the electrode interface. [Ref. 50: p.l]. They report that Plumlee visually detected the growth of dendritic filaments from the electrodes in fatigued samples of PZT. They propose that ions freed by the degradation of a unit cell move through the lattice until they touch the top or bottom of the lattice, at which point a dendrite begins to form. Subsequent free ions build on the growth until the dendrite shorts the sample and the material becomes conducting. As the dendrite grows, the field in the center of the lattice becomes stronger, which makes the cell near the end of the dendrite more likely to degrade. It also results in faster switching times, since the switching time in ferroelectric materials is dependent on the field strength. Cells below the end of the dendritic growth will experience a reduced field, and are therefore less likely to switch polarization, reducing P_s. This model is disputed by others who have not detected dendritic growth in fatigued ferroelectric materials.

Stewart and Consentino found that fine grained samples fatigue faster than large grained samples [Ref. 55: p. 166]. Scott has suggested that this will be true in all materials since the accumulation of space charge occurs at grain boundaries [Ref. 3: p. 3]. If this is true, fabrication processes which result in particularly fine-grained specimens, such as sol-

gel, could be expected to suffer more from rapid fatigue, but there is little information to confirm this hypothesis.

The electrode material used for ferroelectric memory device is also crucial. Fraser and Maldonado [Ref. 57: p. 2172] systematically evaluated several materials for electrodes and found a significant difference in the fatigue rate for the various materials. Electrode materials will be discussed in more detail in Chapter IV.

Fatigue and aging can be improved by an order of magnitude or more by poling at high temperatures. Over 100% improvement has been shown when the initial poling is done at 200° C, compared with ambient temperature. These results are linear, with .05% improvement for each additional degree. High temperature operation will also improve fatigue rates [Ref. 3: p. 2].

It is important to note that the fatigue proceeds more slowly with a higher field; the fatigue limits can change by a factor of 10^6 depending on whether the applied field is well above the coercive voltage or near the coercive field threshold [Ref. 3: p. 4, Ref. 55: p. 165]. The reason is that the coercive field gradually creeps up as a result of fatigue, causing less and less charge to be switched for an established voltage level [Ref. 20: p. 48, Fig. 3.12]. If operations are near the threshold, this is a very large effect relative to the applied field; if the external electric field is well above the coercive field, it becomes negligible. This effect is vividly demonstrated in Figure 18. Obviously, it is extremely important to specify the applied field used to determine the fatigue rate. A test near the breakdown voltage for that particular material may achieve 10^{12} polarization reversals, while one at 5 v may result in only 10^5 reversals before the switched charge is reduced by half [Ref. 3: p. 4].

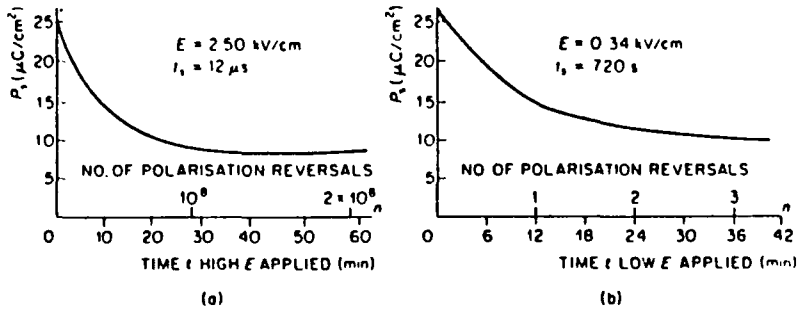

Figure 18. Fatigue Characteristics versus Electric Field (From Ref. 20)

C. WAITING TIME

There is another effect which can cause loss of data through the spontaneous polarization switch of a ferroelectric memory cell. This effect is generally termed "waiting time" and is the result of the establishment of a preferred polarization direction in the material. Some ferroelectric materials, e.g., KNO_3, develop a memory of the existing polarization state over the time they are exposed to a dc bias field and the time at zero bias as it "waits" to be switched [Ref. 54: p. 4512]. This preferred direction may be the direction of original poling, or it may be the result of space charge buildup at the electrode/material interface [Ref. 34: p. 1446, Ref. 54: p. 4512]. The result of the waiting time effect is an asymmetry in the switched polarization which is dependent on the length of time the cell has been held in either the $+P_S$ or $-P_S$ state, i.e., the longer the cell has been in one state the less polarization is switched [Ref. 46: p. 1550]. This effect has been related to reduction in the polarization switching due to the specific resistivity (Ω–cm) of the material and is similar to the previously discussed space charge driven theory of aging [Ref. 21: p. 1241]. As the resistivity increases, the migration of the space charge produced by impurities is suppressed [Ref. 21: p. 1242]. These results can be particularly acute

when the cell is irradiated in the short-circuited condition [Ref. 34: p. 1448]. To minimize this effect, acceptor atoms should be avoided and care must be taken to eliminate impurities.

D. EFFECTS ON DEVICE PERFORMANCE

The important criteria of performance for a nonvolatile memory is the capability to correctly recall the set device state after a given time interval, i.e., retain the data. Retention, defined as a performance parameter, has units of time and measures the performance of both the material and the underlying circuitry. Obviously, when the previously discussed material degradation mechanisms affect retention by reducing P_r, the readable signal available to the sensing circuitry is also reduced. For a given material, fatigue, aging, and waiting time are dependent on the processing techniques used, since the deposition method, etching, electrodes, film thickness, etc., can all impact the ability of the packaged device to retain data over a specified period. However, the operating profile of the device (average retention interval and access frequency, operating temperature, and radiation environment) also have retention impact.

Aging and fatigue are the primary problems. Although several researchers have reported acceptable fatigue rates, these reports also indicate an increase in aging rate as a result of repeated cycling of the material. This inter-relationship between aging rate and extensive cycling of the material prevents treating these as independent problems, to be solved separately. The reported data also seems to indicate that several mechanisms, some of which may be independent, contribute to changes in material properties.

Unfortunately, at the present time there is no theore ical model which allows the prediction of results when the material composition, processing procedures, metal interconnect system, or electric field design parameters are changed. Thus, when changes are made, the effect on device parameters such as output signal, aging, and fatigue can be

determined only by test of devices produced under those conditions. Conversely, when a desired characteristic fails to meet specifications the questions of which variable to change and by how much are also answered only by device testing. The number of variables is daunting; as previously discussed, hysteresis loop parameters are dependent on the magnitude and frequency of the applied electric field, impurities in the material, film thickness, grain size, electrode metal, and temperature. Only with a better theoretical understanding of the phenomena can integration of ferroelectric materials into existing semiconductor processing be done efficiently. In addition to the factors discussed above, testing procedures (to be discussed in greater detail below) can have significant impact on the results obtained. The complexity of the inter-relationships and lack of standards contributes to a lack of consistency in results reported in the literature, further weakening acceptance of the technology. The present situation not only complicates the fabrication of working devices, it also undermines the customer acceptance of the technology since it is difficult to be confident of the quality and reliability claims when there is no theoretical support for limited empirical results.

IV. FABRICATION OF FERROELECTRIC MEMORY DEVICES

A. THIN-FILM DEPOSITION METHODS

Successful ferroelectric memories require fabrication methods which consistently produce high quality thin-films. These methods must be capable of precisely controlling the stoichiometry, since ferroelectric material properties are so strongly dependent on any impurities which may be used to dope the material. The process must also produce phenomena comparable to the bulk material, proper cystallinity, and good interface properites. The memory-critical characteristics of ferroelectric materials, such as resistivity, remanent and spontaneous polarization, dielectric permittivity, and coercive field may be degraded if process parameters are not be precisely controlled. Difficulties with "narrow" or constricted hysteresis loops, compositional control, non-uniformity in thickness, and cracking may also be encountered with deposition of thin-films [Ref. 28: p. 2717, Ref. 58: p. 189, Ref. 59: p. 2]. Additionally, although part of the solution to previously discussed degradation problems lies in improved understanding of the physical mechanisms of aging and in materials selection, empirical optimization of the processing of integrated ferroelectric memories can also provide solutions.

Any technique employed must also be compatible with the existing semiconductor processes and provide reliability, reproducibility, and low cost if it is to be effective in manufacturing. Several techniques meet these requirements and will be discussed in more detail. Ferroelectric thin-films have been produced by molecular beam epitaxy (MBE), flash or electron beam evaporation, rf diode sputtering, ion beam deposition, chemical vapor deposition, and sol-gel or metal organic decomposition deposition methods, and each

has its unique advantages and disadvantages [Ref. 20: p. 23-28, Ref. 58: p. 189, Ref. 60: p. 595, Ref. 61: p. 6601, Ref. 62: p. L655]. It is worth noting that the results given for any of these deposition methods is highly dependent on the material composition. The specific problems reported can frequently be alleviated or eliminated by changing the composition of the target or precursor, atmospheric mixture, or temperature. For example, it has been reported both that sputtered and sol-gel deposited ferroelectric thin-films suffer from acute retention loss and that they have good retention characteristics [Ref. 3: p. 3, Ref. 34: p. 1452]. Therefore, the method selected for use will depend heavily on prior experience, the specific materials used, and the fabrication steps required for the device under consideration. Deposition techniques can be divided into two major classes, physical vapor deposition (rf, ion beam, and dc magnetron sputtering and flash/electron beam evaporation) and chemical methods (CVD, MOCVD, and sol-gel)

1. Physical Vapor Deposition

a. Sputtering

Sputtering is a physical vapor deposition process in which an electrical discharge is set up between two plates in the presence of a low-pressure inert gas such as argon. The ionized gas atoms are accelerated by the electric field toward the "target" material from which the thin-film is to be formed. Atoms of the target material are knocked free and diffuse to the substrate. The target can be a compound of the material to be deposited, or an active gas, such as oxygen, water, or hydrogen sulfide can be introduced to reactively sputter a new compound [Ref. 63: p.242]. Multiple targets can also be used to control stoichiometry. Sputtering can be applied to nearly all materials of interest in semiconductor manufacturing and is used for approximately 70% of the metallization processes [Ref. 64: p.329].

Ion beam, rf diode, and rf planar magnetron sputtering have been employed successfully to deposit ferroelectric thin-films with desirable properties, although these results are not always reproducible. The substrate is usually heated, with substrate temperatures above 500° C generally required for perovskite crystal structure [Ref. 61: p. 6601, Ref. 65: p.244, Ref. 66: p. 4495, Ref. 67: p. 2]. The properties of films deposited at lower temperatures improve after annealing at 400-900° C. Rf planar magnetron sputtering provides reasonable deposition rates over relatively large surface areas and meets the requirement for fabrication temperatures compatible with integrated circuit technologies, although precise control is required of the deposition conditions [Ref. 61: p. 6601]. It has shown higher deposition rates than conventional sputtering or ion-beam deposition [Ref. 61: p. 6602], although problems with producing consistent compositions have been reported [Ref. 68: p. 606].

The temperature required for deposition of high quality crystalline films with good ferroelectric properties is the biggest drawback to the sputtering method. Use of reactive sputtering of multi-element metallic targets with an rf magnetron system, rf sputtering with a dc bias applied to the substrate, or ion beam sputtering may allow lower temperatures [Ref. 38: p.4406, Ref. 61: p. 6602, Ref. 68: p. 606, Ref. 69: p. 18, Ref. 70: p. 3]. These techniques may also improve compositional control, although cracking and adhesion problems have been reported [Ref. 38: p. 4407, Ref. 69: p. 20].

In addition to the problems with stoichiometric control mentioned above, sputtering has two other drawbacks: damage to the substrate material through impact of high-energy atoms, electrons, and molecules, and roughness of the deposited surface [Ref. 62: p. L655]. Despite these disadvantages, familiarity with the technique and equipment availability has made it the choice of several firms developing ferroelectric memories.

b. Flash/electron Beam Evaporation

In flash evaporation the ferroelectric material is evaporated by dropping individual grains of the source material onto a filament heated to a temperature of approximately 2000° C. The material thickness is built up on the heated substrate in small increments. The crystal structure of the resultant thin-film depends on the substrate material. When metallic substrates, such as platinum, are used the film is polycrystalline, with properties closer to ceramics than single crystals [Ref. 20: p. 27].

Deposition of materials with ferroelectric properties directly on silicon is difficult. Successful electron beam evaporation of $BaTiO_3$ onto a silicc substrate at only 120° C has been reported. The thin films of between 100 and 500 nm exhibited ferroelectric behavior, although the remanent polarization and coercive field were not reported [Ref. 71: p. 155]. If these results are reproducible, this method may gain in popularity, but presently no one is using evaporation techniques in a production setting.

2. Chemical Methods

a. Chemical Vapor Deposition (CVD)

Chemical vapor deposition (CVD) employs the decomposition of a gaseous precursor to produce a solid thin film. Inert carrier gases, such as argon, transport the reagent vapors to the substrate. The substrate is heated to catalyze the process. Thin film growth rates are controlled by the temperature used for source decomposition and carrier gas flow rate [Ref. 72: pp. 98-101]. Temperature, precursor gas flow rate, and pressure must be precisely controlled for reproducible production of uniformly high quality materials with the desired ferroelectric properties. CVD is widely used in semiconductor device fabrication because it is a simple technique with considerable versatility.

CVD has been used with some success to fabricate ferroelectric thin films and eliminates most of the disadvantages suffered by sputtering, but produces films with

lower values for remanent polarization [Ref. 62: p. L655, Ref. 73]. Values of remanent polarization and coercive field of 0.16 $\mu C/cm^2$ and 14.5 kV/cm have been achieved [Ref. 62: p. L656]. These values do not compare well those generally obtained by sputtering, indicating that further process refinement is necessary before this is the fabrication method of choice.

b. Sol-gel

The sol-gel method is a relatively new ceramic processing technique which has been used to prepare highly homogeneous thin-films at temperatures significantly lower than several of the other methods (300-700° C). Sol-gel processing of ceramics involves a non-aqueous solution of metal alkoxide precursors. The metal oxides are mixed in the proper stoichiometry and partially hydrolized with a solvent-water solution. The film thickness can be adjusted by varying the viscosity of the solution. The resulting "sol" of the hydrolized alkoxide is placed on the desired substrate by spin-coating, spraying, or dipping. Following drying, the "gel" is densified by heat treatment. Multiple coats of the gel are used to increase the film thickness if necessary. Sol-gel thin-films have been fabricated on various substrates: Si, Pt, Au, Al-Cu alloy, SiO_2, Al_2O_3, $SrTiO_3$, and silicon-nitrited GaAs. In addition to low processing temperatures and compatibility with a large variety of substrates, this method has several other advantages: excellent compositional control, high degree of homogeneity and film thickness, ease of application over large areas, relatively inexpensive equipment, and rapid turn-around time for new compositions [Ref. 28: p. 2717, Ref. 58: p. 189 and 191, Ref. 59: p. 2, Ref. 74: p. 177, Ref. 75: p. 186].

Poor adhesion between the substrate and the film may result in cracking. Selection of a solvent with a high boiling point and latent heat of vaporization and increasing the firing temperature will significantly reduce the tendency to crack. Firing of

the films by placing the substrate on a hot plate also reduces cracking in comparison to oven firing [Ref. 28: p. 2719].

Following firing, films are frequently amorphous and annealing is required to achieve crystallization [Ref. 28: p. 2719, Ref. 59: p. 3, Ref. 74: p. 180-181]. Following annealing the sol-gel thin-films have crystal structure close to those for bulk materials [Ref. 28: p. 2720].

The electrical characteristics of the resulting thin-film depend on the ferroelectric material, the number of layers deposited, firing process and temperature used, annealing time and temperature, and the substrate used [Ref. 28: p. 2719-2723, Ref. 59: p. 5-6, Ref. 74: p. 179-183]. The remanent polarization is frequently smaller than that for bulk materials, while the coercive field (E_c) is larger. This is generally attributed to the smaller grain size in sol-gel thin-films [Ref. 28: p. 2721, Ref. 37: p. 85-86, Ref. 58: p. 191, Ref. 75: p. 186-187]. Values of remanent polarization of 36.0 $\mu C/cm^2$ have been achieved [Ref. 76: p. 80].

As previously noted, smaller grain size has been associated with higher rates of fatigue and aging [Ref. 3: p. 3, Ref. 37: p. 83, Ref. 46: p. 1550]. This would seem to indicate that sol-gel thin-films should exhibit higher rates of fatigue and aging, but little evidence has been reported in the literature. Space charge effects in the form of asymmetric hysteresis loops have been reported in sol-gel thin-films. The direction of asymmetry depends on whether the substrate is n- or p-type semiconductor. Films deposited on p-type substrate have a cut-off where the external field switches sign from positive to negative, while films on an n-type substrate display the same form of cut-off when the voltage switches from negative to positive. This is attributed to the buildup of a compensating space charge at the semiconductor-ferroelectric interface. Electrons are attracted to the semiconductor surface when polarization is toward the interface, and holes are attracted

when polarization is reversed. Thus, either a charge depletion region or a charge accumulation region is created depending on the type of semiconductor and direction of polarization [Ref. 75: p. 187].

Other researchers have reported very good fatigue results from sol-gel fabricated ferroelectric thin-films. Figure 19 shows the endurance achieved with PZT thin-films on platinum substrate. The reported $2x10^{11}$ reversals compares well with those achieved with other forms of fabrication [Ref. 58: p. 191, Fig. 4]. The positive slope of this curve varies from the fatigue curve usually displayed but is not inconsistent with results reported by others for sol-gel films [Ref. 27: pp. 3-4]. These results, when coupled with the other advantages of this technique seem to make sol-gel deposition the preferable method.

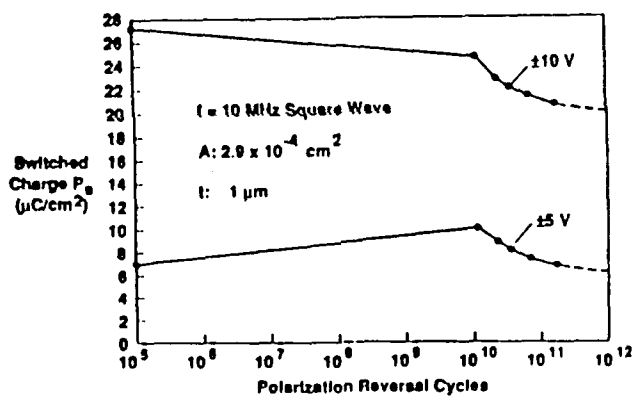

Figure 19. Endurance with Sol-gel Deposition (From Ref. 58)

B. DEVICE PATTERNING/ETCHING

The processes used for device patterning, etching, and cleaning must be compatible with the ferroelectric material so that an otherwise acceptable thin-film is not degraded by the subsequent processing. The temperature used for the etch process or for removing the photoresist can have detrimental effects on the remanent polarization, causing the hysteresis

loop to narrow as the remaining process steps are completed until there is insufficient signal for memory operation. Ferroelectric materials have environmental stability and temperature requirements which are generally compatible with existing IC manufacture, but adding new materials to the fabrication process may narrow the window of acceptable parameters to the point where acceptable yields are difficult to maintain. An additional complication arises when one considers there is no complete model for the effect of temperature, deposition technique, and stoichiometry on the characteristics of ferroelectric materials; a workable process is developed by a trial and error process--sometimes with more error than we would wish.

C. ELECTRODE MATERIALS

Electrode materials have significant impact on the performance of the ferroelectric memory, and several electrode materials have been evaluated with differing degrees of success. Compatibility problems occur if a high temperature anneal is required for acceptable ferroelectric behavior, since the standard IC inter-connect metal systems, such as Al, Au, and Cu, are incompatible with high temperatures because of their relatively low melting points. The solution to this problem is development of a fabrication process which is carried out at lower temperatures, such as sol-gel or MOD, or the use of other metal systems, such as platinum and titanium. [Ref. 77: p. 4]

As mentioned previously, the choice of electrode metal has significant impact on the aging and fatigue rates of the ferroelectric material. The analysis by Fraser and Maldonado indicate that electrodes of indium provided the best characteristics, while gold and silver accelerated the degradation process [Ref. 57: p. 2174]. Platinum was not included in their study, but has been evaluated by others [Ref. 78: p. 69] and has found wide use with ferroelectric memories in laboratory evaluation, although there are some problems with

adhesion using standard IC processes. There are other materials, not yet evaluated in the open literature, which may provide IC process compatibility and acceptable ferroelectric properties, such as the transition metals and their oxides [Ref. 64: p. 438, Ref. 80].

D. TESTING STANDARDS

The market for ferroelectric memories depends on extending the retention limitations resulting from fatigue and aging. Although claims are made for ten years and 10^{12} read/write cycles before loss of data retention, these claims are not supported by adequate test data. In the absence of a substantive theory of the signal degradation mechanisms, empirical data is essential to improved performance and validation of product specifications. To accomplish this end, proper testing procedures which provide the necessary information to the design engineer, process engineer, and customer need to be established. Since the critical parameters of ferroelectric memories are dependent on the test conditions (e.g., magnitude and frequency of the applied electric field) and the history of the device, test condition changes allow the tester to "tailor" the results to meet the specifications. In fact, the test may itself alter the material under test. Thus, it is hard to make comparisons of results from different researchers or manufacturers. Recognition of these problems led to the creation of a Test Chip Working Group at the first Government /Industry Ferroelectric Memory Review in September 1988. The progress has been hampered by protection of proprietary information, but Harris is designing a test chip which meets the preliminary requirements established by the Test Chip Working Group in November 1988. The IEEE standardization effort also includes a test and measurement subcommittee.

Considerable government sponsored research is being done and there is coordination of these efforts to reduce duplication. Measures should also be taken to provide consistency in the analysis and reporting of the results, to further enhance the effectiveness

of the research. At a minimum, government contracts should require a standard set of tests, which allow for the integration of results.

The test standards established must provide for two test requirements, material evaluation and device characterization. By providing standards for the evaluation of material properties, deposition techniques, electrode options, and operating environment impacts, real progress can be made in optimizing material composition, deposition methods, electrode materials, and read/write designs. The other test regime is device testing, which must be structured to provide the closest correlation to the expected use of the part. Access frequency, retention requirements, and operating env ɔnment must be considered. The inter-relationships between these competing requirements must be understood so the results are not biased by compensating effects.

1. Materials Characterization

There are six tests typically used to characterize ferroelectric materials: hysteresis (P-E), pulse (I-t), capacitance-voltage (C-V), current-voltage (I-V), conductance-voltage (G-V), and dielectric permittivity [Ref. 80: p. 1756, Ref. 81]. The standard test setup for ferroelectric materials is the previously discussed Sawyer-Tower circuit [Ref. 15: p.4, Ref. 18, pp. 269-273]. It is the basis for the hysteresis, current-voltage, and pulse test techniques.

The Sawyer-Tower circuit was first used to measure polarization versus electrical field, producing the hysteresis loop characteristic of ferroelectric materials. It will also provide a measurement of dielectric permittivity. The circuit may be modified to compensate for conduction through the capacitor under test and to reduce the sense capacitor distortion [Ref. 82: p.217]. The capacitor conductance compensation uses an adjustable resistor and an adjustable linear capacitor in parallel with the device being tested. This simulates the linear components of the test capacitor signal, which are then subtracted

to produce a "pure" ferroelectric hysteresis loop. It must be noted that this technique may hide distortions which appear to be linear. If compensation is used, the values for the compensating resistor and capacitor should be reported with the test results. The second modification to the basic Sawyer-Tower circuit is the addition of an operational amplifier to create a virtual ground between the ferroelectric capacitor and the sense capacitor, eliminating the distortion caused by the sense capacitor.

Substitution of a resistor for the sense capacitor is done for current-voltage and current-time measurements. The circuit is driven with a voltage pulse and the resulting current waveform is observed. The results may provide insight to the switching process of the material. The switching time of the capacitor tested is not a material characteristic, but is dependent on the resistance value [Ref. 80: p. 1757]. High speed measurements require the use of very small capacitors.

A second form of pulse measurement utilizes the Sawyer-Tower circuit driven with a series of relatively slow voltage pulses. Measurements are taken at $\pm P_{sat}$ (while the voltage is applied) and $\pm P_r$ (after removal of the voltage), providing digital reconstruction of the hysteresis loop.

The capacitance-voltage measurement method was originally used to determine the interface trap charge in silicon metal-oxide-semiconductor (MOS) devices. Polarization switching causes a variation in capacitance and the coercive field (E_c) can be estimated from the data. The capacitance-voltage technique may be useful to detect the presense of defects such as impurity ions [Ref. 80: pp.1756-1758]. As previously discussed, the presense of mobile ions may cause fatigue problems.

The same test setup can be used for conductance-voltage measurements and generates information on coercive field, switching symmetry, and mobile ion concentration and effects [Ref. 83: p. 342].

The final test method is the determination of the dielectric permittivity. An impedance meter measures the dielectric permittivity with a small ac signal while a dc bias is applied to the sample. The dielectric permittivity is plotted as a function of dc bias. This method provides information for the study of contact and space charge effects [Ref. 81].

All of the techniques discussed provide important data for the characterization of ferroelectric materials. Care must be taken to avoid introducing measurement errors by failing to consider the properites of ferroelectric materials (fatigue and aging) or the parameters of the electrical circuit (RC time constant and test frequency). The test conditions and electrical parameters should be reported to aid in reproducing the test data.

2. Device Characterization

Device characterization requires evaluating every aspect of the memory's performance, i.e., retention, speed, operating voltage parameters, timing, bit error rates, and temperature range. The test programs used during the development phase of the device must provide feedback to the design and process engineers so problems in design and fabrication can be pinpointed. This testing will initially be done on small lots of wafers as the design and process are evaluated. As development is completed, the device will be subjected to a sequence of tests designed to verify that the device meets operating specifications, and following development, testing will be done to screen defective parts. Because of the dependence of material performance on test parameters, it is important to structure the test procedures to reflect the expected usage of the device and ensure that inadvertent "best case" scenarios are not used.

Because of the interrelation of fatigue and aging, and the test duration required for testing to failure, testing retention is the most difficult aspect of ferroelectric memory evaluation. It seems to be generally accepted that a nonvolatile memory should provide 10^{12} read/write cycles and ten year data retention following the last write. Although no

systems design evaluation of these requirements has been reported, these are de facto standards which present problems to the test engineer as well as the design engineer. Obviously, waiting weeks to test a device to failure due to fatigue or ten years to conclude a ten year retention test is not practical. Therefore, accelerating mechanisms must be found that will allow short-duration evaluation of performance through margin testing. Discovery and validation of these accelerating mechanisms will require extensive materials characterization, providing manufacturer and customer confidence in their predictive ability. An iterative process results, with better testing providing a more complete understanding of the basic physics of ferroelectric materials, which in turn will improve test procedures and give greater assurance of device performance.

V. FERROELECTRIC RANDOM ACCESS MEMORY (RAM) DESIGN

A. GENERIC TWO-TRANSISTOR DESIGN

The circuitry for memory cells in a ferroelectric RAM is virtually indistinguishable from that in a standard DRAM., utilizing pass transistors and ferroelectric capacitors in a matrix of bit and word lines. Figure 20 shows a concept of a memory layout with two transistors in each memory cell. Two transistors are used in this more conservative approach to shield the ferroelectric capacitor from capacitive feedthrough when the word line is taken high, so there is no unintentional disturbance of the capacitor. If the ferroelectric capacitor is resistant to disturbance problems, the transistor on the drive line can be eliminated. In this example, the bit, word, and drive lines are held at ground when none of the cells are being written or read, isolating the ferroelectric capacitors. Only when the word line is high does the status of the bit or drive lines affect the capacitors. The WRITE operation is initiated by taking the word line high, connecting the bit and drive lines to all the capacitors in that row. Then either the bit or drive line for the cell to be written is taken high to write a "one" or "zero". Following the WRITE operation the lines brought high are returned to ground.

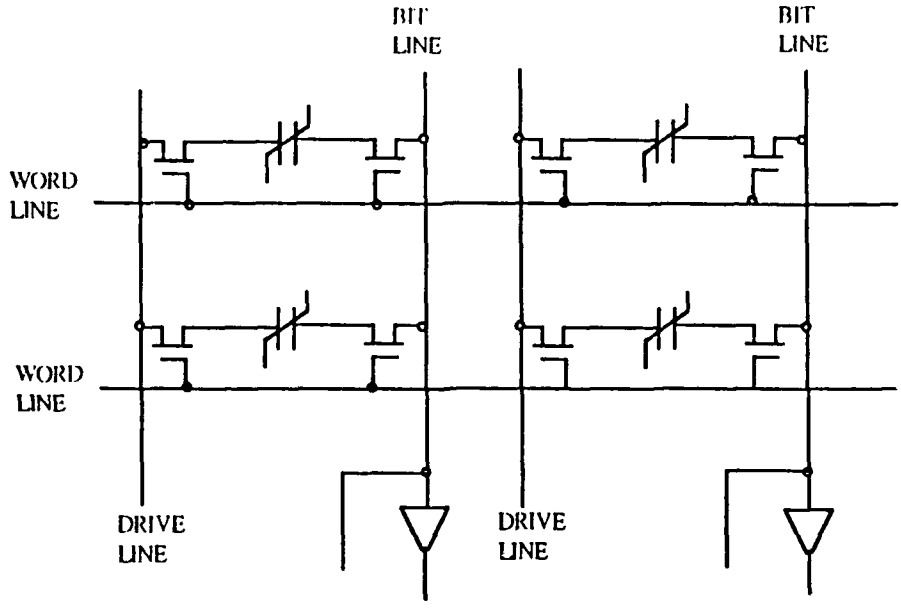

Figure 20. Two-Transistor Memory Cell (After Ref. 84)

Reading a cell follows a similar process. First the word line of the appropriate row is brought high, then the drive line in the cell column is "pulsed" or taken high for a short time. If the polarity of the capacitor does not switch, that is, the polarization is already oriented to the zero state, the bit line will stay below an established voltage threshold. However, if the capacitor polarization switches (from "one" to "zero"), the output of a noninverting amplifier on the bit line will go high as the bit line voltage exceeds the threshold. To restore the original state the output is fed back to the bit line rewriting a "one" in the cell; the drive line has returned to low at this time. All lines taken high are returned to ground to complete the READ operation. Figure 21 illustrates the concept of the read and write process [Ref. 84: p. 265, Fig. 2].

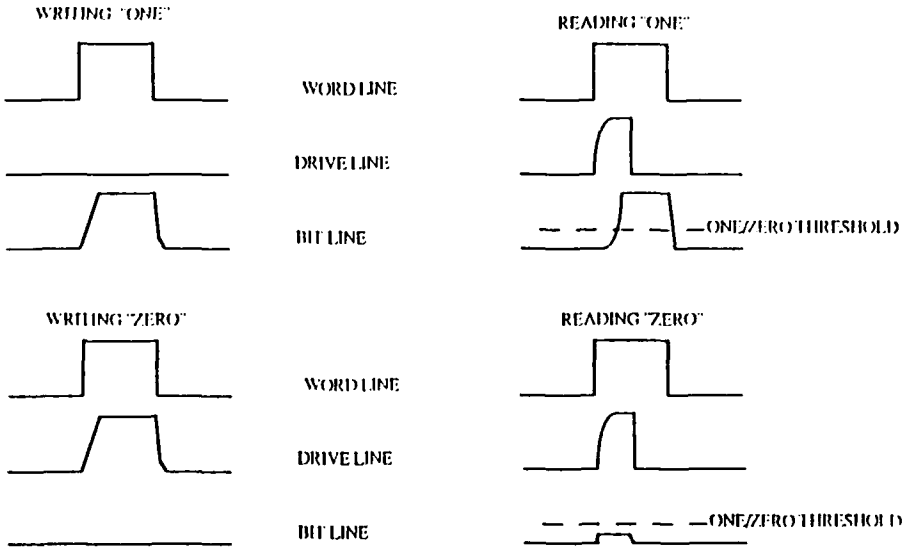

Figure 21. Read/Write Operation (After Ref. 84)

It is important to note that this process cannot be interrupted until the restore is complete without losing the data. As a result the device will have a cycle time that is different than either the read or write time. Memory design must ensure that the restore cycle is completed before lockout occurs on power down. Care must also be taken to protect code intended to be read-only so that it is not inadvertently destroyed by an erroneous signal from external control logic.

B. DIFFERENTIAL-READ CELL

The circuit in Figure 22 provides a larger signal differential through the use of a paired, complementary oriented, cell structure. A second ferroelectric capacitor and a bit line (complement) are added to the previous circuit. To write to a memory cell, the appropriate word line is brought high and the sense amp is set to the desired state, driving

BL and BL (complement) to opposite voltages of ground and V_{drive}. The drive line is then brought high, writing a "zero" to the capacitor at ground. As the drive returns to ground the second, complementary, capacitor is written with a "one". The state of the capacitor controlled by BL represents the stored datum.

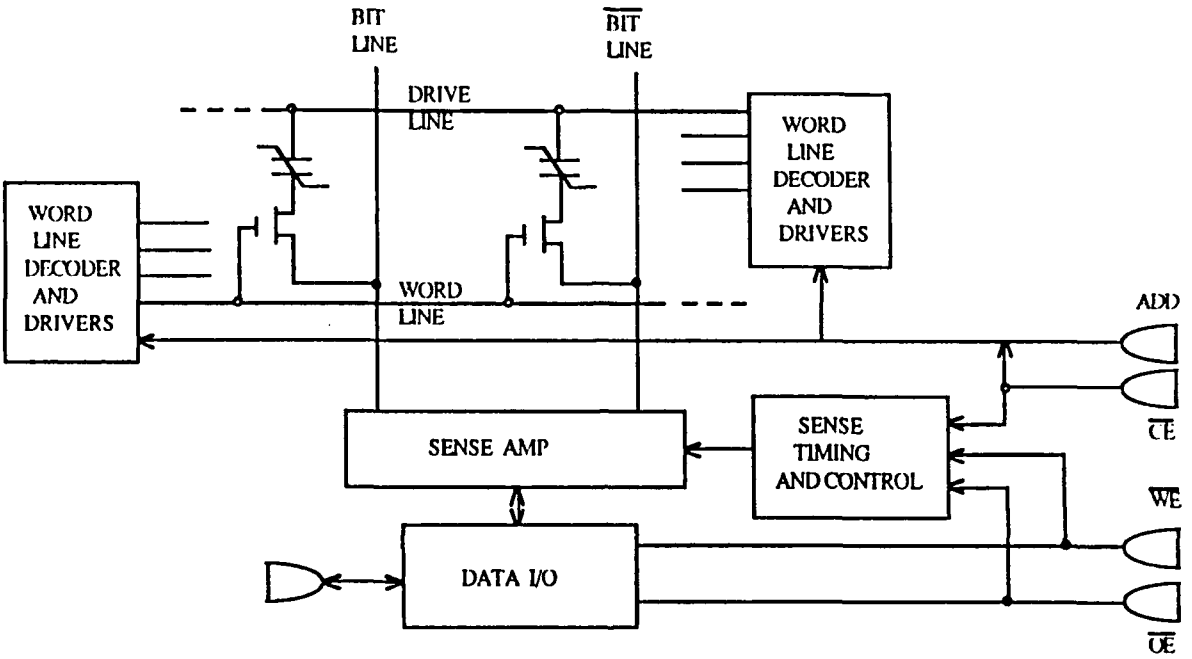

Figure 22. Differential Read Memory Cell (After Ref. 85)

For the READ operation the sense amplifier is off, the word line is brought high for the appropriate row, and the drive line is taken high. Since the paired capacitors are in opposite states, BL and BL (complement) will have different voltages as shown in Figure 23 [Ref. 85: p. 1172]. The bit line with the higher voltage (the cell whose polarity switched) will go high as the sense amplifier turns on, while the other will be forced to ground, recreating the original write condition.

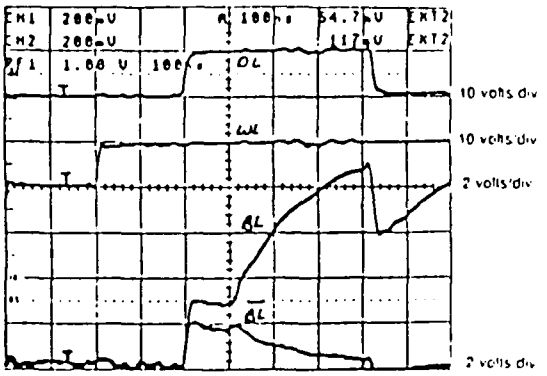

Fig. 5. 512 FCD bit-line voltages during READ

Figure 23. Output Voltages (After Ref. 85)

C. "SHADOW" RAM

Ramtron has designed a combination of an SRAM and a ferroelectric memory, called a FRAM, which provides data protection in case of power failure. As shown in Figure 24, the ferroelectric memory acts as a "shadow" to the SRAM through the use of control transistors which connect the ferroelectric capacitors to the SRAM cell and deselect the device to avoid data contamination when a power interrupt occurs. When the control transistors are turned on, the ferroelectric capacitors are polarized to the appropriate state within approximately 20 nsec, well before the SRAM portion of the devices loses its data due to power drop [Ref. 86: p. 93]. When the control transistors are off the FRAM acts as a standard SRAM. After the data is stored in the ferroelectric array it can be recalled when power is restored, or new data can be loaded into the SRAM cell while the old information is left in the ferroelectric array for later use. This design avoids the problem of fatigue since the ferroelectric capacitors are switched only when power is interrupted. Further detail of this design is provided in Appendix A.

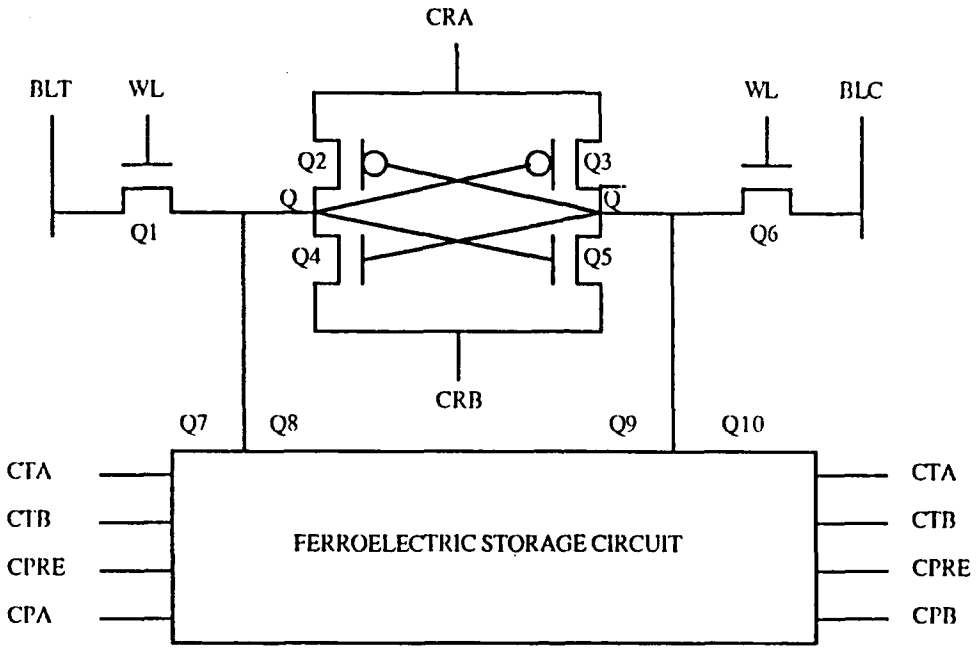

Figure 24. FRAM Cell Schematic (After Ref. 86)

D. FERROELECTRIC FET

The simplest design for a memory based on ferroelectric materials is a field effect transistor (FET) with the ferroelectric material used to regulate the conductivity of the semiconductor channel between the source and drain. With the gate oxide replaced by ferroelectric material, the polarization state of the ferroelectric will change the electron population at the interface. If the semiconductor is p-type, a negative polarization will decrease the electron concentration and increase conduction, while a positive polarization will increase the electron concentration and decrease conduction. Thus the polarization state turns the FET "on" or "off" [Ref. 65: p. 246, Ref. 87: pp. 17-18].

This implementation offers two very significant advantages. Since the polarization state is not altered to do a "read", this is a non-destructive method of storing and retrieving

data, which offers extended operating life and improved radiation hardness. Additionally, with only one FET per memory cell, this memory implementation has potential for very high densities. However, this design has several problems: it is difficult to fabricate the low resistance electrodes needed to get low voltage operation, it is difficult to deposit the ferroelectric film directly on silicon, and movement of compensation charge through the ferroelectric film reduces the difference between the "one" and "zero" voltages [Ref. 71: p. 156, Ref. 88: p. 10, Ref. 89: p. 580].

Despite the drawbacks, the inherent simplicity and desirable characteristics of this design keep interest high. Westinghouse Electronics System Grou is developing a variation of this technology, using $BaMgF_4$ to replace the gate dielectric. $BaMgF_4$ has good fatigue characteristics and also sublimes as a molecule, eliminating stoichiometry problems. The resulting device is referred to as a ferroelectric FET (FEMFET) [Ref. 5: p. 5, Ref. 90].

E. OTHER MEMORY DESIGN CONCEPTS

1. Bipolar Memory

The previous memories discussed are based on CMOS technology. Raytheon is developing a ferroelectric memory based on bipolar rather than CMOS technology because they feel there are advantages in design and fabrication. Since bipolar devices are current-driven rather than voltage-driven, the switching current can be directly sensed without conversion to voltage, which may provide better detection threshold values, although higher power will be required. Bipolar device fabrication can tolerate high-temperature procedures which may be required to achieve optimum ferroelectric properties. Sintering at high temperatures (550° C to 1000° C) is done to obtain the desired crystal structure [Ref. 20: p. 40, Ref. 28: p. 2719, Ref. 74: p. 179, Ref. 91: p. 12]. Bipolar circuitry is also less

sensitive to total dose ionizing radiation. Evaluation of the design under a U. S. Army Strategic Defense Command contract is underway. [Ref. 79]

2. Latch

Krysalis has developed a non-volatile octal D-type flip-flop with non-volatile recall of stored data after power off. The device functions as a standard 8-bit latch with the added feature of non-volatile data storage on each positive clock transition, providing automatic data protection in case of power loss. It is being evaluated for applications such as automobile odometers, access counters, and flight time recorders. Detailed product information is provided in Appendix A.

3. Optical Read

Ferroelectric materials have a variety of interesting optical properties, including changes in birefringence, refractive index, and transparency with changes in the electrical polarization of the material [Ref. 30: p. 579]. These changes in the optical properties can be used for memory applications, with data storage done by setting the desired polarization state with an applied electric field and optical data recovery. The immediate advantage of this electronic write and optical read is that the read does not destroy the data, so this technology offers potential for non-destructive read out (NDRO), which will be discussed further.

The simplest form of optical memory is an electrically controlled light valve. With incident light propagating along the *b* axis, the polarization of the *c* axis only is reversed by the application of an electric field. In $BaTiO_3$ this results in rotation of the optical indicatrix through 50° [Ref. 30: p. 580-581]. With proper alignment of an optical polarizer at the input and an analyzer at the output the electrical-dipole polarization state of the sample can be determined by the magnitude of transmitted light.

Another form of light valve can be created with polarizers oriented 90° apart, a quarter-wave plate and a electrically switchable ferroelectric quarter-wave plate, formed from gadolinium molybdate, which provides sufficient change in birefringence with an applied external electric field. As the total retardation is switched from zero to $\pi/2$, the transmission is switched off and on.

4. Non-destructive Read Out (NDRO)

Strategic and SDI applications generally require non-destructive readout (NDRO) of the stored data [Ref. 36: p. 1]. Although there may be alternatives which will provide the same practical level of data protection, the established requirements generally dictate NDRO for strategic system memories. Several possible NDRO techniques are being explored.

a. Partial Switching

If a ferroelectric material is subjected to an electric field E which is less than E_C, a partially switched, or minor, hysteresis loop as shown in Figure 25 will result. The shape and stability of the minor loop are dependent on the material characteristics and the frequency and magnitude of the applied field [Ref. 20: p. 41, Fig. 3.7]. If the material provides a stable minor loop (as shown in Figure 25), the polarization state could be determined without traversing the complete hysteresis loop. This switching behavior may be exploited for an NDRO design by using circuit voltage levels such that the remanent polarization is moved from $-P_R$ to $-P_A$, but not switched, for the read operation. The normal process could then be used to restore the memory capacitor to $-P_R$. If the restore process were interrupted by a radiation pulse, the remaining polarization ($-P_A$) would provide sufficient signal for a subsequent read. This technique would provide data integrity unless the memory were to be hit by pulses on two succeeding attempts to access the same memory capacitor, an event of vanishingly small probability.

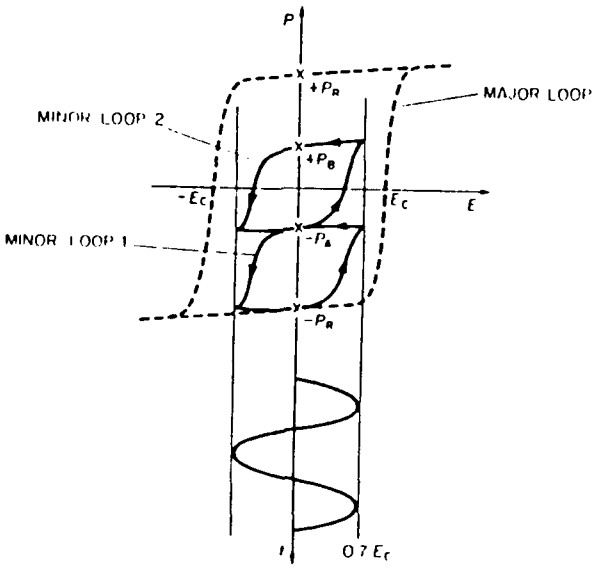

Figure 25. Minor Hysteresis Loop (From Ref. 20)

A potential drawback to this NDRO technique is that partial switching of the memory capacitor has been shown to have detrimental effects on data retention. Switching to intermediate states which are less than half of P_{sat} sharply decreases the retention of the material in samples 2 to 7 μm thick [Ref. 78: p. 73]. This may not be a factor in thinner films in the range of 70-500 nm, but must be evaluated.

b. Polarization-controlled Current Flow

The bipolar device under development by Raytheon may offer NDRO through polarization-controlled variation in conductance in the ferroelectric material. The conductance of the ferroelectric material differs depending on the orientation of the current flow in relation with the remanent polarization, ie, parallel or antiparallel. Evaluation of this concept in hardware will require further effort to discover alternate electrode materials which will not mask the small polarization-controlled changes in current. If the current flow changes can be measured this will provide another NDRO technique [Ref. 79, Ref. 94].

c. Piezoelectric Effect

Another idea for NDRO uses the piezoelectric effect which is found in ferroelectric materials [Ref. 20: p. 299-300, Ref. 93: pp.51-52]. A high frequency sine wave is applied to the electrode for the central area, which piezoelectrically excites radial mechanical vibration. Measurements of phase change compared to the driving voltage (which acts as a standard) are used to determine the orientation of polarization in one of the outer electroded areas, with the change in phase proportional to the polarization. The phase change can be used to store binary data or, by using partial switching, to store any value between $+P_r$ and $-P_r$ [Ref. 93: pp.51-52]. A prototype low-capacity NDRO memory using this idea has been developed, but because of large size (>0.38 cm diameter, 76 μm thick) it is unlikely to be used in production memories and is mentioned here primarily for completeness [Ref. 20: p. 299-300].

d. Anomalous Photovoltaic Effect

A unique idea for NDRO recovery of data uses an anomalous photovoltaic effect present in many ferroelectric ceramics. Relatively large photovoltages can be generated by uniform illumination of the ferroelectric material and the direction of the photo-emf flow can be regulated by changing the electrical polarization of the memory element. The circuit is biased so that a field effect transistor is turned on or off depending on the polarized state of the memory cell. Thus a "write" is done by switching the polarization state and a "read" is achieved by applying a read pulse to the input and observing the resulting voltage across the transistor [Ref. 94: p. 153-154]. The critical point of interest is that the polarization state is not changed by the read operation, so the stored data is not altered by the read. This technique offers intriguing possibilities, but the present design is too large (13 by 1750 μm cell) to be utilized in an operational device.

Other ferroelectric-photoconductor memory devices have been proposed, but are generally too slow and require destructive readout [Ref. 95: p. 426-427].

F. NON-MEMORY DRAM APPLICATIONS

As DRAM density increases to 4 Mbit and beyond, the required charge density cannot be achieved with planar nitride-oxide capacitors. The 4-Mbit and 16-Mbit devices are designed with either trench or stacked capacitors to get the necessary charge storage while consuming less die area. It may be possible to develop a 64-Mbit part using a nitride-oxide dielectric by design innovations which further reduce capacitor footprint, but to realize additional gains a material must be found which provides a substantially higher dielectric constant. As mentioned previously, ferroelectric materials possess very large dielectric permittivities and are being evaluated for use in high density DRAMs [Ref. 24: p. 17]. Although this work is preliminary, it appears that ferroelectric capacitors could provide sufficient charge storage density to support 256-Mbit DRAMs. Although a nonvolatile memory application, it is significant because it will spur further experimental evaluation of ferroelectric materials and their integration into semiconductors by an even wider circle of manufacturers. For example the work cited here is supported by Semitech, the semiconductor research consortium.

VI. FERROELECTRIC MEMORY APPLICATIONS

Ferroelectric memories will first be used in niches where the application-specific capabilities outweigh the initially higher price. For applications where nonvolatility is required, ferroelectric memories have advantages over other technologies, such as EPROMs, EEPROMs, SRAMs with battery backup, magnetic bubbles, and magnetic core. These advantages will be exploited by system designers to solve particular problems and provide the initial market. Ferroelectric memories will find another niche in designs where radiation hardness is critical. After introduction in these applications the new technology will proceed along the learning curve, costs will begin to fall, and further product improvements will be made [Ref. 1: pp. 6-8]. As this process continues, ferroelectric memories offer the potential to successively displace other memory technologies and perhaps even become competitive with DRAMs as device densities increase beyond the point where DRAMs are scalable.

Before ferroelectric memories can seriously compete with any of the existing technologies, manufacturers must prove that claims made by proponents have not been exaggerated. Since the early development efforts have been made by startup companies, there has been pressure to produce immediate results and this pressure has resulted in several premature product announcements. The optimism is probably not misplaced, but has made many potential users skeptical of the technology.

A. NONVOLATILE MEMORY REPLACEMENT

In the past, nonvolatility has always come with a complication; changing the stored information was difficult at best. As the systems in which non-volatile memories are used become more complex, the likelihood of changes to improve operation or exploit new

developments increases proportionately. This makes a re-programable non-volatile semiconductor memory ever more important. In general, ferroelectric memories could be used to replace any of the above memory technologies, and in fact the first designs presented have been compatible with existing EEPROM pin-outs, allowing the utilization of ferroelectric memories in existing designs.

Ferroelectric memories offer advantages over each of the other non-volatile memory technologies available. ROM and PROM offer excellent endurance and non-volatility but by definition are not reprogrammable, which severely restricts flexibility and makes error correction difficult. Magnetic core is non-volatile and offers radiation tolerance but is slow, bulky, and power hungry. Magnetic bubble memory is an improvement, but still requires more space and power than semiconductor memory technologies. EPROM can be erased and reprogrammed, but not in any real time fashion. Exposure to UV restricts mounting options and usually requires at least partial disassembly of the system. EEPROM provides in place reprogramming of selected portions of the memory, but is still relatively slow. Additionally, rewrites are limited to less than 10^5. SRAM with battery backup is fast, but the battery makes the package relatively large in comparison to the ferroelectric memory, require routine maintenance and introduce another failure mode. The typical SRAM design uses six transistors, so the densities projected for the ferroelectric RAM should far exceed those achievable with SRAM. Thus the first ferroelectric products will compete well against EEPROMs, offering better endurance and higher speed. They also compare well with SRAM with battery backup, although slightly slower and more expensive. As operating speeds increase and the technology progresses down the learning curve it will begin to displace battery-backed SRAMs as well.

The programs for embedded controllers, such as those increasingly used in automobiles, are kept in nonvolatile memory. The ability to efficiently correct errors or

adapt to changes in fuel specifications make ferroelectric memories candidates for use. Automated production equipment, which require frequent changes to manufacturing instructions, would also benefit from the higher speeds and greater cycle endurance available with ferroelectric memories.

The military applications are almost too numerous to list: missile navigation and targeting information, "smart" mines and torpedoes, airborne mission data storage, weapon system loadout information, electronic warfare suite setup parameters, maintenance records of inflight aircraft system parameters, remote-site inventory data collection and storage for supply records, weapons guidance/search parameter tailoring, and recording of built-in-test results. The demands of shorter development times and more rigorous operational test and evaluation for military systems make the flexibility of ferroelectric memories particularly important. As performance problems are discovered or system requirements change in the development and production cycle, retrofitting the improvements and corrections requires only reprogramming, without disassembly or hardware changes.

Ferroelectric memories could be used to replace ROM, SRAM with battery backup, or EEPROMs used in PCs for bootstrap memory, firmware device drivers, and lookup tables. The use of ferroelectric memories would allow fast, simple changes to the stored programs without the size and complexity of an SRAM and provide greater speed and endurance than the EEPROM. [Ref. 96: p. 44]

Ferroelectric memories can be used for aircraft communications system and field radio encryption devices, providing both nonvolatility and extended endurance for frequent changes to key lists.

Ferroelectric memories used with a microprocessor such as the F68HC11 used in the Naval Postgraduate School ferroelectric satellite experiment discussed in Appendix A would provide a system for performing remote-site supply inventories and maintenance

record keeping [Ref. 97: p. 32]. Similar systems with EEPROMs have been utilized for medical record keeping but the EEPROM wears out too quickly for applications requiring frequent data change and higher read/write speeds.

The combination of non-volatility and radiation hardness provided by ferroelectric memories make it an obvious choice to replace magnetic core memory. The Space Shuttle and F-16 both still rely on this 30-year old technology because it provides reliable non-volatility. The B-2 also uses core memory, but may switch to semiconductor memory technology in a tradeoff for more computing speed and power. EEPROMs, with write times on the order of 0.5-10 msec and limited endurance of approximately 10^5 writes, cannot provide the performance required. SRAM with battery backup has the necessary speed, but it comes with size, complexity, and reliability penalties. Ferroelectric memories can give extended endurance, SRAM-like speeds, and reduce bulk and complexity. Magnetic core providing 32 Mbit of memory occupies 6600 in^2, while an equivalent memory composed of 4 Kbit ferroelectric devices would occupy only 330 in^2. The savings in power consumption is even more dramatic; the core memory requires 700 W while the ferroelectric memory needs only 4 W. [Ref. 98: p.79]

B. RADIATION HARD APPLICATIONS

The radiation tolerance of ferroelectric memories discussed earlier also makes the technology attractive for space applications. Since the 1962 radiation-caused failure of the Telstar I communications satellite, spacecraft designers have used a variety of techniques to ensure the operation of spacecraft systems at the high radiation dosages encountered in space. The radiation testing done on ferroelectric devices demonstrate radiation hardness equal to any projected space missions. The radiation of greatest interest is primarily electrically charged particles trapped in the Earth's magnetosphere and, less prevalent, high-energy cosmic rays [Ref. 99: p. 445]. Trapped electrons have a maximum energy of

5 MeV and protons generally have energies of 1-10 MeV [Ref. 100: pp. 460-461]. Ferroelectric materials have exhibited radiation hardness in excess of these levels in the experiments previously cited. Ferroelectric memories could finally provide a semiconductor replacement for spaceborne tape recorders and will be particularly useful for long-duration space missions, such as the Voyager probe, because reprogrammable non-volatility will allow adjustments to the mission profile as dictated by post-launch discoveries/equipment failures.

Ferroelectric memories may be exploited in some space or strategic systems applications without significant modification of the underlying CMOS circuitry. As stated earlier, NDRO is considered essential to hardened military and strategic system applications, but there are design schemes using error detection and correction (EDAC) software which could achieve the desired reliability goals with ferroelectric memories with destructive read out. A design developed by the Jet Propulsion Laboratory incorporates a Hamming error-correcting code in the DRAM layout [Ref. 101: p. 30]. This form of on-chip error-correction provides faster detection and correction with lower overhead in hardware and software. The code corrects for only one error per word, but the DRAM can be protected for single-event upsets by separating the memory locations for each word. If the memory cells are beyond the damage area for charge tracks from incident ions, a single hit will not cause more than one error per word.

Other alternatives could be used to make the read cycle tolerant of radiation pulse damage. The read/restore sequence can be done bit-by-bit with a Hamming code or parity bit technique used to cue resets, if necessary. The total would be complete within about 50 nsec and the probability of two successive radiation pulse hits within 50 nsec is practically zero. [Ref. 36: pp.1-6] The use of partial read NDRO for ferroelectric memories discussed

earlier would of course eliminate the requirement for EDAC software, but EDAC may be the simplest approach and provide practically the same radiation hardness.

Since CMOS radiation tolerance is dependent on the bias condition, it may be possible to use the combination of ferroelectric material and CMOS as an "on only when accessed" memory, which would provide improved radiation hardness. This technique would obviously not be workable for all memory applications, but provides another alternative for systems where fast access times are not critical. Also, significant improvements in CMOS radiation tolerance are being made which will make this less of a handicap [Ref. 102].

The Strategic Defense Initiative Office is interested in non-volatile semiconductor memories to replace magnetic tape storage systems currently used on most satellite systems. Although attention is focused on silicon oxide/nitride oxide semiconductor (SONOS) technology, ferroelectric memories are also candidates for this application. [Ref. 99: p. 79]

C. ARCHITECTURE SIMPLIFICATION

In the longer term, if all the potentials of ferroelectric memories are realized and they become competitive with DRAMs on a cost and density basis, the benefits of speed and nonvolatility will be exploited to simplify computer system memory architectures. When all levels of the existing memory hierarchy can be nonvolatile the functional division shown in Figure 26 is no longer required and the new architecture shown in Figure 27 will become possible, bringing with it improvements in programming flexibility and operating speed.

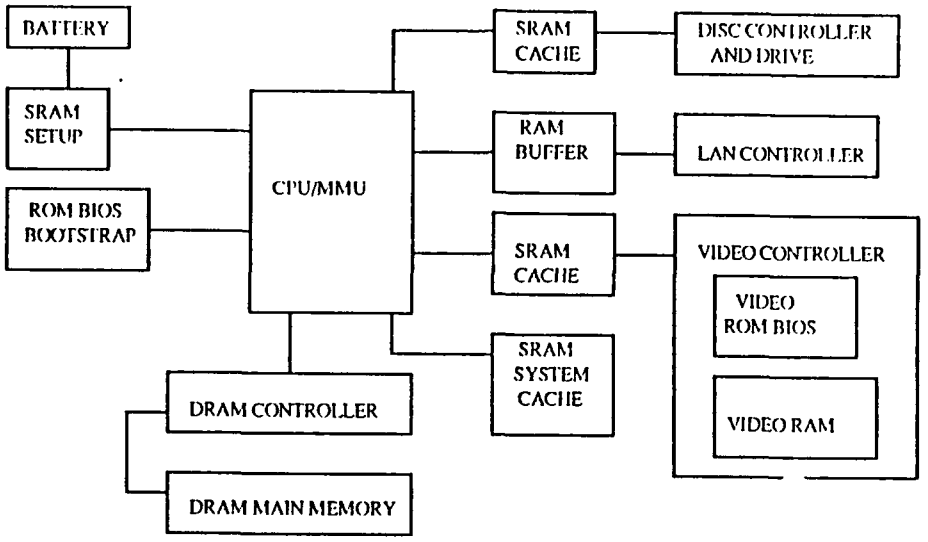

Figure 26. Current Computer Memory Architecture

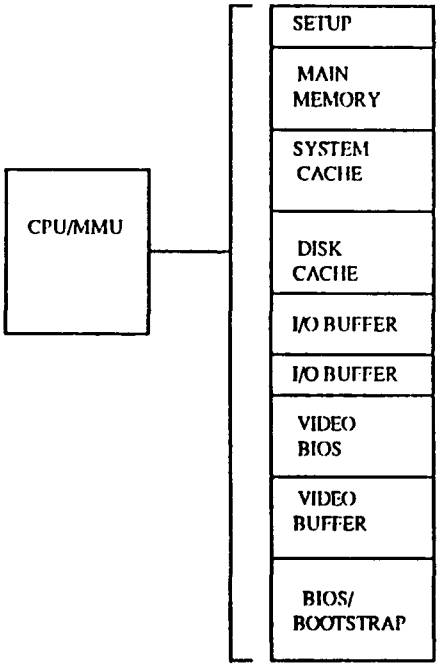

Figure 27. Computer Memory Architecture with Ferroelectric Memory

VII. SUMMARY/CONCLUSIONS

The properties of ferroelectric materials make them a natural candidate for memory applications. Successful integration with conventional semiconductor technology and processes will provide the memory system designer a high speed, nonvolatile, memory option. The feasibility of the basic concept is not at issue; memories based on ferroelectric materials have been fabricated and demonstrate the potential of ferroelectric-based memories. However, two significant hurdles remain, eliminating the problem of signal degradation and complete integration of the ferroelectric material into full-scale commercial manufacturing processes with acceptable production yields.

Signal degradation due to fatigue and aging is the major factor limiting application of ferroelectric materials; in this regard nothing has changed since the previous efforts were aborted two decades ago. However, progress has been made. As discussed previously, the fatigue characteristics of several materials now exceed the accepted requirement of 10^{12} cycles, and reports indicate acceptable aging rates have been achieved, at least at the commercial temperature specification (85° C). Further progress will come as a better understanding of the physical mechanisms develops from additional research.

Integration of ferreoelectric materials into semiconductor fabrication processes is not a trivial problem. It could be considered equivalent to empirically maximizing an unknown equation with an unknown number of variables without complete data on which variables have changed from trial to trial. Standard semiconductor processes, although within specification for other devices, can cause failure of ferroelectric memories through degradation of initial remanent polarization. They can also produce accelerated rates of aging or fatigue, or otherwise lower yields to unacceptable levels. Thus new process specifications have to be developed so commercially viable yield levels are achieved and

maintained. Although development efforts can be sustained with low yields, the potential customer will not pay prohibitively high prices for ferroelectric memories, even with truly exceptional performance characteristics.

Solution of these problems will require extensive research into optimization of material composition, deposition techniques, electrode materials, process integration, film thickness and grain size effects, write/read voltage levels and waveforms, temperature effects, and alternate designs. A great deal of research is already ongoing, but the analysis and reporting of the results is not consistent, hampering integration of data from two or more sources. The data reported frequently appears contradictory without definitions of the phenomena under study and standards for testing. This results in duplication of effort and undermines the reputation of the technology. It is recommended that government contracts require a standard set of tests, which would allow for meaningful integration of the results. Work must be continued to coordinate research activities to minimize duplication of effort.

As an unproven technology, ferroelectric memories face a "Catch-22" dilemma where designers are reluctant to use them because they have no reliability history, and they cannot generate a reliability history without increased use. The present lack of theoretical understanding further hinders acceptance. It is for this reason that thorough evaluation of materials, process integration, and degradation mechanisms and widespread dissemination of the results are essential.

Progress continues with minimizing the effects of fatigue and aging and integration of the ferroelectric material into standard semiconductor processes without degrading laboratory-attained material properties. Several workable memories have been made in small numbers, and efforts to integrate ferroelectric materials into standard IC processes are nearing fruition. Added impetus to integration efforts will be given by the cited interest in utilizing ferroelectric materials as high dielectric capacitors in conventional DRAMs. This

interest in higher density devices will mean that even those not interested in the unique memory properties of ferroelectric materials will be engaged in integration evaluation.

The memory market is growing rapidly, both in quantity and in performance requirements. Larger, faster memories with reduced power consumption are needed to support the faster, more powerful CPUs. Magnetic core and plated wire can no longer meet the system requirements and are being replaced with less robust technologies that can provide the needed speed. Ferroelectric memories are really the only candidate technology to replace these older systems, which provides significant impetus to research and development. This implies that support for ferroelectric memories is likely to be longterm.

However, the memory market is also extremely competitive and ferroelectric memories will be used by memory system designers only if they are convinced that the overall system operation, reliability, and cost effectiveness has improved by the incorporation of ferroelectric memory components. For example, if the application requires 10^4 read/write cycles, the memory system designer will not pay a premium for a ferroelectric memory device even if it provides 10^{12} read/write cycles. It is also important to note that initially ferroelectric memories will be competing for applications in designs optimized for the competing technology.

Ferroelectric memories can provide unique advantages for system designers. Initially, the applications will be in niche markets where the design problems demand innovative solutions. As larger memories are produced they will find expanded application as replacement for EEPROMs and SRAMs with battery backup, but still in relatively small numbers. Large scale production of 256-Kbit will be required before a major shift away from existing memory technologies will begin to occur. As successful applications increase, even with small memories, the product acceptance will begin to accelerate. The real breakthrough will be made when the new designs are optimized for ferroelectric

memory capabilities, rather than the other technologies' limitations. The first steps will begin with the release of the National Semiconductor eight-latch and the 4-Kbit memories from National Semiconductor and Ramtron projected for 1991.

APPENDIX A: NAVAL POSTGRADUATE SCHOOL SATELLITE ON-ORBIT MEMORY EXPERIMENT

As part of a cooperative effort with Orbital Sciences Corporation, the Naval Postgraduate School is conducting an experimental evaluation of two ferroelectric products, a eight-bit non-volatile latch and a 256x1 "shadow" ferroelectric random access memory. The experiment was severely constrained by power, weight, and volume restrictions, and also by the limited time for concept development and design. The two products and controlling circuitry have been installed in the Datasat-X satellite which was to be placed in a 500 km polar orbit by the first Pegasus launch. Unfortunately, due to growth in the weight and volume requirements of other systems, the Naval Postgraduate School ferroelectric experiment was not carried on the 5 April 1990 launch. However, planning continues for expanded experiments with launch support from the Space Test Program.

The experiment was intended to evaluate the performance of these parts in the space environment and provide information for the space qualification of integrated ferroelectric devices. Neither the parts nor the control circuitry is shielded from radiation effects, which are significant in a polar orbit, with annual dose rate of 1.63×10^{13} 1 MeV equivalent protons and 4.5×10^{11} 1 MeV equivalent electrons [Ref. 103: pp. 6-46 and 6-47]. The unshielded parts cannot be considered radiation hard since the underlying CMOS structure is not hardened, although the ferroelectric material should not be effected by the radiation levels expected.

The experiment consists of eight Ramtron FMx 801 Shadow RAMs, one National Semiconductor octal latch, and associated control and address circuitry. The experiment was limited to this configuration by the "not to interfere" basis of the original proposal.

The experiment is a single board which weighs 200 grams and dissipates less than 200 mW of power. A more detailed description of the ferroelectric products follows.

1. National Semiconductor (Krysalis) Octal Latch

The National Semiconductor (Krysalis) device is the octal latch described earlier, which provides non-volatile storage of data in the power off condition. The stored state is recalled to the output pins on the rising edge of the clock when recall input pin (RCL) is high. When powering up, the device protects stored data by ignoring clock inputs until a recall has been executed. The latch is fabricated with 2-micron CMOS technology, and provides TTL-level inputs and CMOS input impedance, output drive cai ›ility, and power consumption . The device is a 20-pin package compatible with bipolar and CMOS based logic circuits. The specification calls for more than one year of power-off data retention and typical propagation delays of 25 ns.

2. Ramtron 256-bit FRAM

The Ramtron FMx 801 256x1-bit nonvolatile static RAM (SRAM) utilizes the ferroelectric material to provide power-off protection to an otherwise conventional CMOS SRAM. The basic operation of the device was described above. The device operates with a 5 v supply, has equal 100 ns read and write times, is CMOS/TTL compatible, and is packaged as a standard 24 pin 600 mil ceramic dual in line (DIP) package. The FMx 801 was designed as a technology evaluation device, so direct access was provided to all ferroelectric control signals to allow complete device characterization. Two discrete ferroelectric capacitors are available, but were not used for this experiment. Figure 28 is a block diagram of the memory cell.

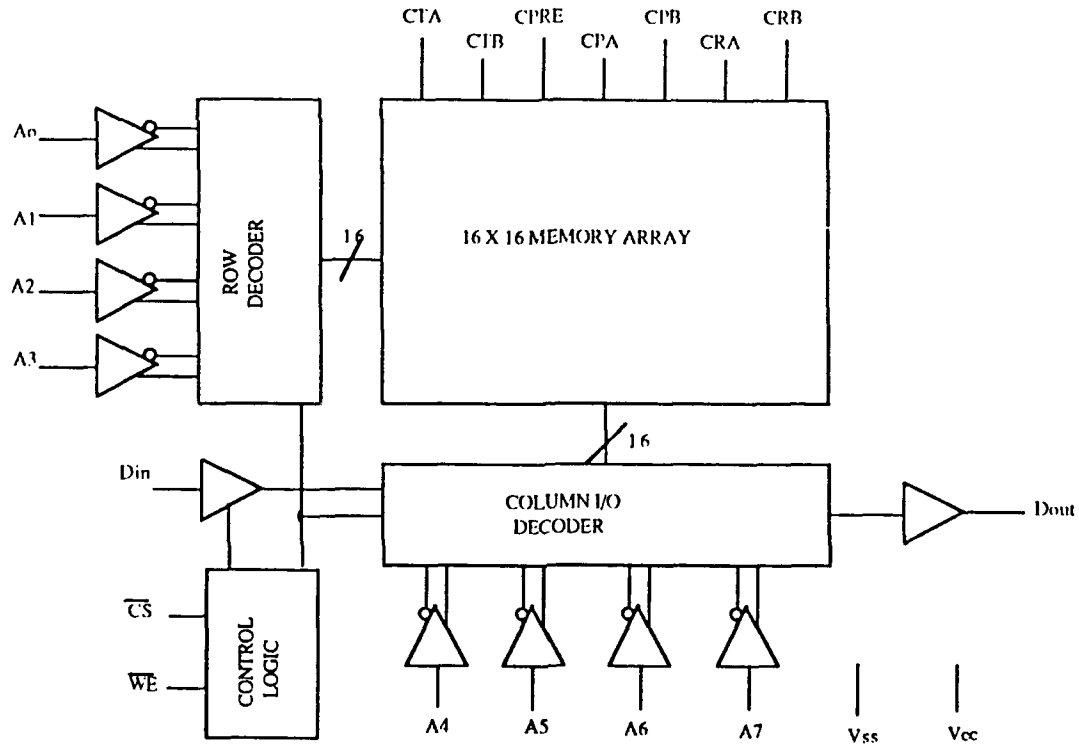

Figure 28. FMx 801 Memory Cell Block Diagram

Fourteen of the pins are used to operate the FMx 801 as a standard SRAM, and seven pins are used to control the store and recall operation of the ferroelectric non-volatile "shadow" memory. The seven ferroelectric pins are divided into two groups with pins CRA and CRB providing the power and ground to the SRAM cell during read/write and store/recall operations. The other five pins (CTA, CTB, CPA, CPB, CPRE) are control signals that either connect or isolate the ferroelectric capacitors as appropriate. For normal SRAM read/write operation all the ferroelectric control pins are held at DC levels as follows: CRA, CTA, and CPRE at Vcc, and CRB, CPA, CPB, and CTB at Vss. The CRA and CRB pins supply the current to all 256 static RAM cells and have the normal supply pin restrictions.

When storing data in the non-volatile part of the memory, reads or writes of the static RAM cells are avoided by deselecting the device with CS. Following deselect, the five control pins are used to write data to the ferroelectric capacitors. The recall operation can take place following restoration of power or during normal static read/write cycling. Care must be taken to avoid overwriting data by pulsing CPA or CPB, or destroying/altering data through failure to follow the prescribed read sequence. The detailed operation of the device, including operating conditions and restrictions, pin diagram, timing requirements, and switching waveforms, are contained in the Ramtron product specification.

3. Experimental Procedures

The experiment is designed to evaluate the retention of the Ramtron device and fatigue performance of the National device. The test structure was restricted by the power, volume, and weight limitations imposed by the launch proposal and the short fuse nature of the entire concept and design effort.

The objective of the experiment on the Ramtron parts is to evaluate their retention performance in the space environment. The eight devices will be driven simultaneously with a "surround," or checkerboard, pattern, which is moved across the memory cell matrix one cell per step. The pattern was chosen to provide the worst-case evaluation of the memory cells by maximizing the probability of adjacent cells impacting the polarization state. The stored data will be read at intervals which increases as the logarithm of time.

The National device is cycled continuously during the operational portion of the test and is otherwise powered down. A test cycle commences with a read of the data. Following verification of data retention, the part is cycled at 100 kHz until powered down. The final data state is stored by the test control circuitry for data verification on the next test cycle. Thus the device is tested for both fatigue and subsequent retention degradation.

The experimental setup does not have provision for determining the cause of device failure. When the data readout indicates a failure either the ferroelectric memory cell has been degraded beyond the point where the sense circuitry can determine the stored state or the sense circuit itself has failed due to the effects of the space environment. Later experiments, with less stringent weight, power, and volume constraints, will provide for failure mode analysis.

4. Control Circuitry

Control of the experiment is done with an F68HC11 microcontroller programmed in the Forth language. Communication is via two serial ports, one for receive and one for transmit. A version of the AX.25 communications protocol was used for compatibility with the Datasat-X system controller. The microcontroller and the interface with the Datasat-X control system provides for reprogramming of the experiment after launch. Experimental data is stored by the Datasat-X control system until queried by ground controllers.

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