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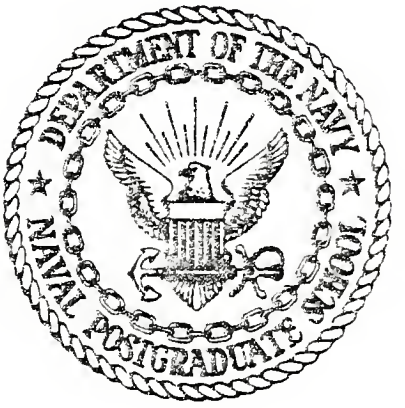
Kyriazanos, Michael D.

Monterey, California. Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL
Monterey, California



THESIS

OPERATION AND PERFORMANCE
OF A SINGLE CHANNEL PCM CODEC
VOICE TRANSMISSION SYSTEM

by

Michael D. Kyriazanos

December 1978

Thesis Advisor: Glen A. Myers

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Operation and Performance of a Single Channel PCM Codec Voice Transmission System

by

Michael D. Kyriazanos
Lieutenant, Hellenic Navy
B.S.E.E., Naval Postgraduate School, 1977

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ABSTRACT

A new monolithic LSI product has recently been developed for the telecommunications market. The device is a coding-decoding circuit called a codec that converts analog voice signals into digital bit streams and back to analog form. Its primary application is in telephone channel banks, where its low cost makes per channel coding and decoding of voice signals economically feasible.

In this work such a codec set is used in conjunction with two hybrid filters as the main components of a single channel voice transmission system. The operation and the performance of this system are presented.

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I. INTRODUCTION

Commercial telephone and military communications systems are being influenced by the revolution created by large scale integration (LSI) technology. Digital transmission of messages continues to gain in popularity. Digital data is relatively insensitive to noise, crosstalk and distortion while faded signals can be readily regenerated without cumulative degradation. Digital switching has such features as flexibility, higher speed, simple design, small size and low cost. Digital signaling can use error-control techniques to improve received message quality.

To realize the advantages of digital communications, signals such as voice need to be converted into digital form (bits) before they can be transmitted. The bit stream must then be converted to analog form in the receiver.

The circuit that contains all the elements needed to convert the analog signal (voice) into digital data for transmission is called the encoder or coder. The circuit that contains the elements needed to convert the digital data back to analog form is called the decoder. A popular technique used by coders and decoders at present is pulse code modulation (PCM).

In usual PCM transmission systems, the necessary conversions were performed by high-speed analog-to-digital (ADC) and digital-to-analog (DAC) converters shared by

many analog channels. In these systems analog sampling and multiplexing were performed before the ADC, and analog demultiplexing was done after the DAC. A typical PCM transmission system is shown in Fig. 1. Disadvantages of this approach include crosstalk between channels due to analog sampling and multiplexing, complex analog components such as samplers, multiplexers and demultiplexers, and loss of all channels when one ADC or DAC fails.

Recent advances in LSI have made it economically feasible to encode each channel with a single integrated circuit (IC) chip. Multiplexing then occurs after ADC. A transmission system using the per-channel approach is shown in Fig. 2. This per-channel approach is claimed to offer improved performance and reliability. Further, cross-talk between channels is eliminated. Switching and processing of individual signals with locic and/or microprocessor control is possible using a per-channel approach.

Many semiconductor manufacturers anticipate a considerable commercial and military market for these monolithic LSI coders and decoders which are now known as "codecs". The PCM codecs perform sampling at a standard 8 kHz rate, analog-to-digital and digital-to-analog conversion. These codecs meet telephone company companding and digital formatting specifications. At present, there are at least 15 semiconductor manufacturers worldwide supplying monolithic codecs. Consequently codecs come in various shapes

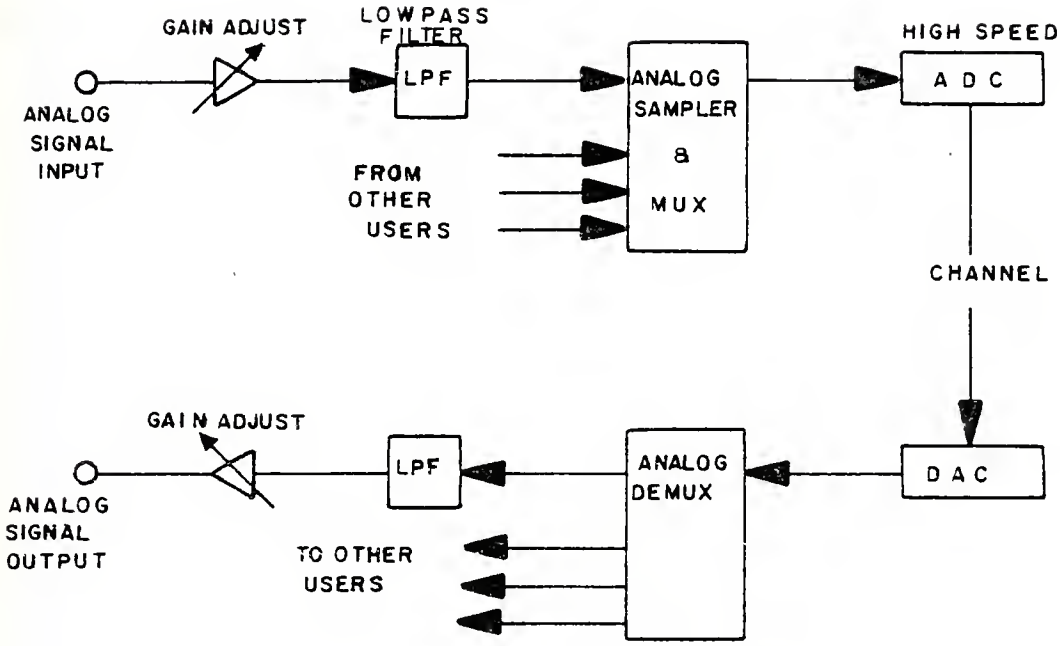


Fig.1 A usual PCM transmission system

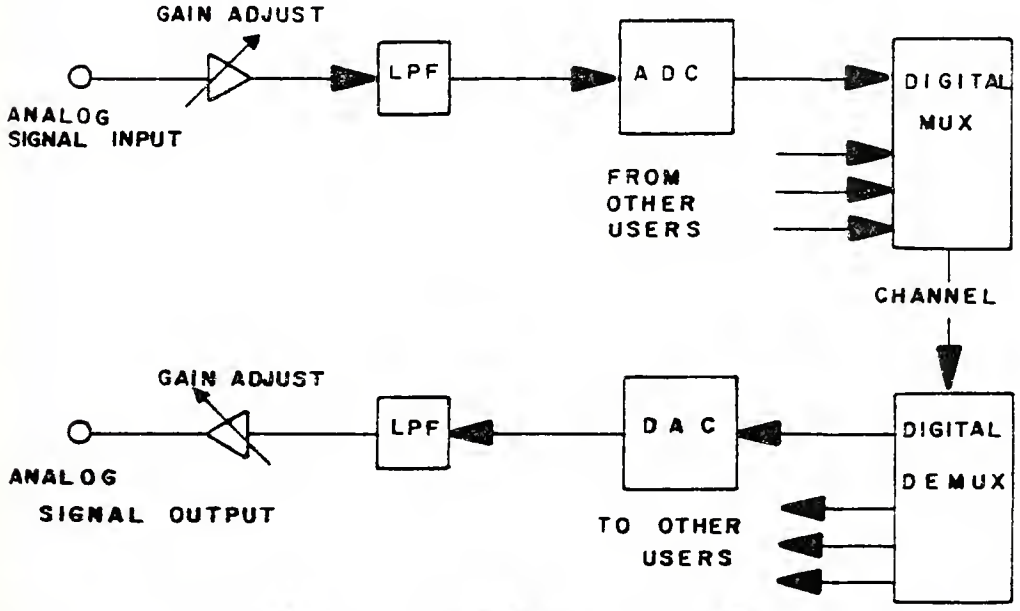


Fig.2 A PCM transmission system using per-channel approach

and sizes and employ differing techniques. There are one-chip, two-chip and totally discrete realizations available using n-channel, complementary MOS, integrated injection logic, and charge-coupled device technologies.

Whatever the design and make of a PCM codec, a lowpass or bandpass filter is required before encoding to prevent aliasing caused by sampling and to reject noise. A similar filter is needed in the receiver after decoding to remove the sampling frequency and to compensate for the frequency distortion caused by the decoder sample and hold circuit. The way that codec and filters are related in a typical PCM channel is shown in Fig. 3.

In voice transmission systems these filters have very rigid specifications such as very small passband ripple and sharp cut-off. At present filters which meet these requirements are realized with hybrid integrated circuits where features of both the monolithic and thick-film construction are used. However IC manufacturers indicate that cheaper, completely monolithic filters will soon be available.

In this particular work, a monolithic codec designed by Sliconix, Inc., in conjunction with transmit and receive hybrid lowpass filters designed by National Semiconductor Inc. is described and operated.

The Siliconix, Inc. DF331 coder and DF 332 decoder is a complete ADC and DAC intended for use in per-channel PCM

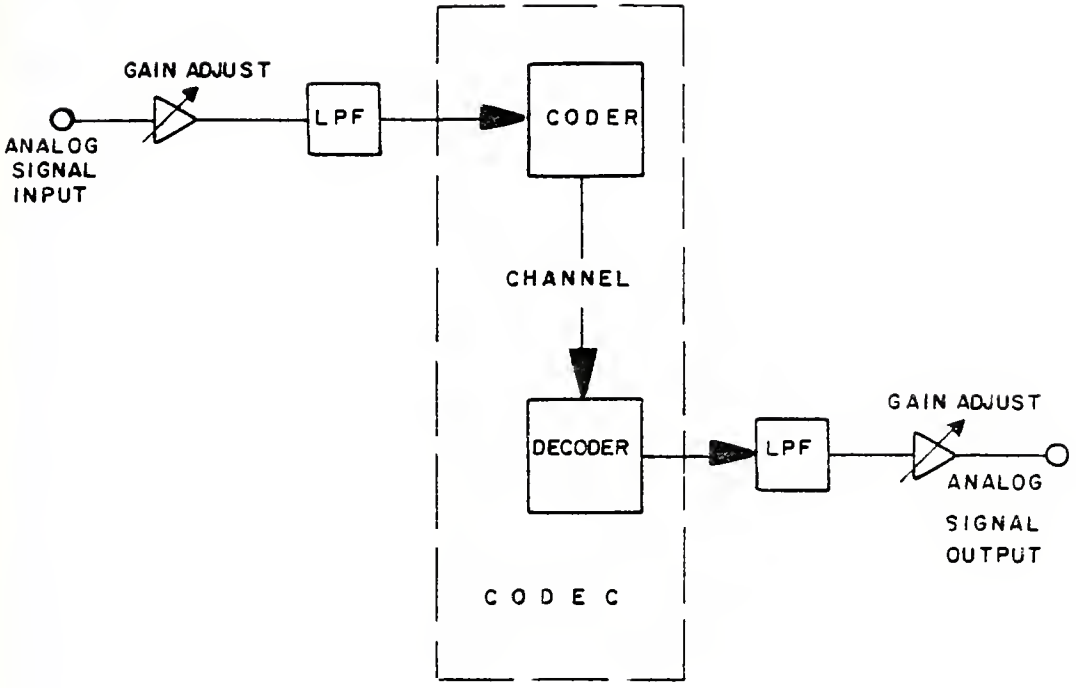


Fig. 3 A typical PCM codec channel

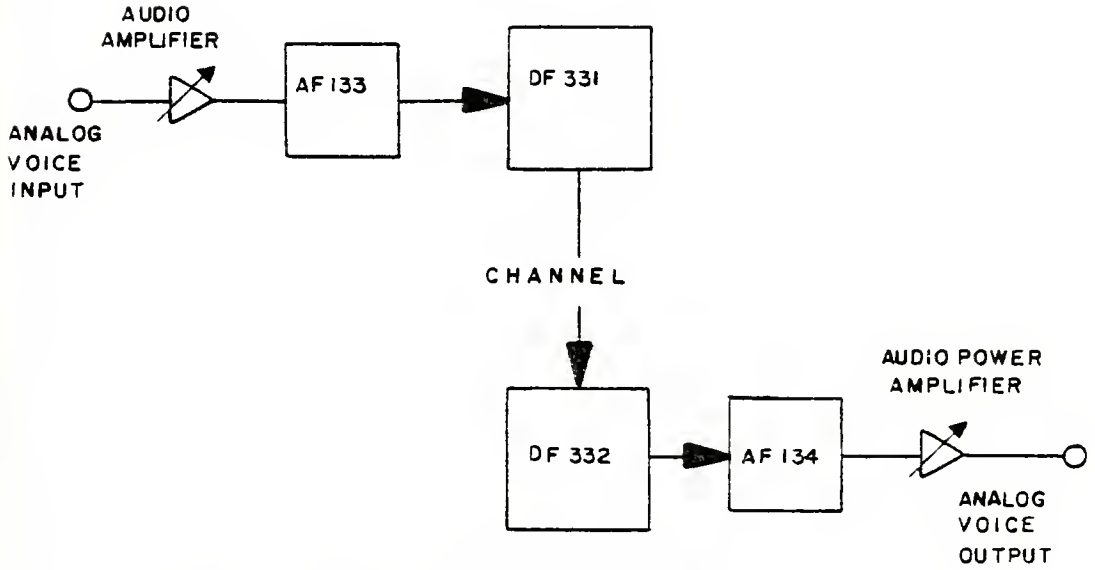


Fig. 4 A single voice transmission system

telephone systems. The DF331 converts up to a 4 kHz bandwidth signal into a high-speed serial digital format. The DF332 accepts high-speed serial digital signals and converts them back to audio signals. Together the two form a codec that is designed to meet the needs of the telecommunications industry for a PCM channel bank and private branch exchange (PBX) systems. The DF331 and DF332 transfer characteristics conform to the μ-255 companding law used by the telephone companies in the United States, Canada, Japan and some South American countries. In Europe and the rest of the world, A-law companding is used and the corresponding codecs are the DF341 and DF342.

National Semiconductor, Inc. markets two hybrid fifth-order elliptic filters for use with PCM codecs: the AF133 (transmit lowpass filter) and the AF134 (receive lowpass filter). The AF133 transmit filter is designed to provide a very flat band pass response from DC to 3.2 kHz, to attenuate signals at 4 kHz (half the sampling rate) by at least 16 dB, to prevent aliasing, and to attenuate signals above 4.5 kHz. The AF134 receive filter is designed to receive the sampled data from the decoder and reconstruct the original analog signal. The AF134 filter approximates an inverse $\frac{\sin x}{x}$ lowpass frequency function needed to compensate for attenuation of high frequency components caused by the decoder sample and hold operation.

A single voice transmission system using the codec pair DF331/DF332 and the transmit/receive filters

AF133/AF134 is shown in Fig. 4. Note the similarity between this circuit block diagram of Fig. 4 and the functional block diagram of Fig. 3. The principles of operation and the performance of the system of Fig. 4 are presented in this report.

Typical circuits required for single channel operation along with interfacing clocking and synchronizing circuitry needed are shown. The hybrid filters AF133/AF134 were not available early in this work. Consequently a filter design using the 741 linear integrated circuit is included. Experimental results are presented. Applications of this system are considered. Difficulties experienced are discussed.

II. OPERATION

In the typical PCM codec channel shown in Fig. 4, the input voice information is an analog time-varying signal. To convert this signal into a PCM pulse train, the coder performs sampling at an 8 kHz rate. This 8 kHz rate that all PCM codecs follow has been adopted by telephone companies. This permits transmission of voice frequency components up to 4 kHz which provides adequate fidelity for telephone conversations. Thus, the voice signal must be band-limited to 4 kHz before sampling to prevent aliasing. This band-limiting is done by the transmit lowpass filter.

In the coder, analog-to-digital conversion is achieved through the use of a successive approximation scheme implemented with a capacitive charge redistribution tech-nique. The block diagram of this ADC is shown in Fig. 5 where the required successive approximation register is represented by the control logic and switch driver block.

The most critical step in the process of forming the PCM bit stream is the assignment of a binary code to each sample. This is done by the elements shown in Fig. 5 in a nonlinear manner referred to as companding. Companding, a contraction of the words, compressing-expanding, is widely used in PCM coder-decoders. There are two parts of companding circuits as the name implies. A compressing part in the coder compresses the range of signal amplitude before

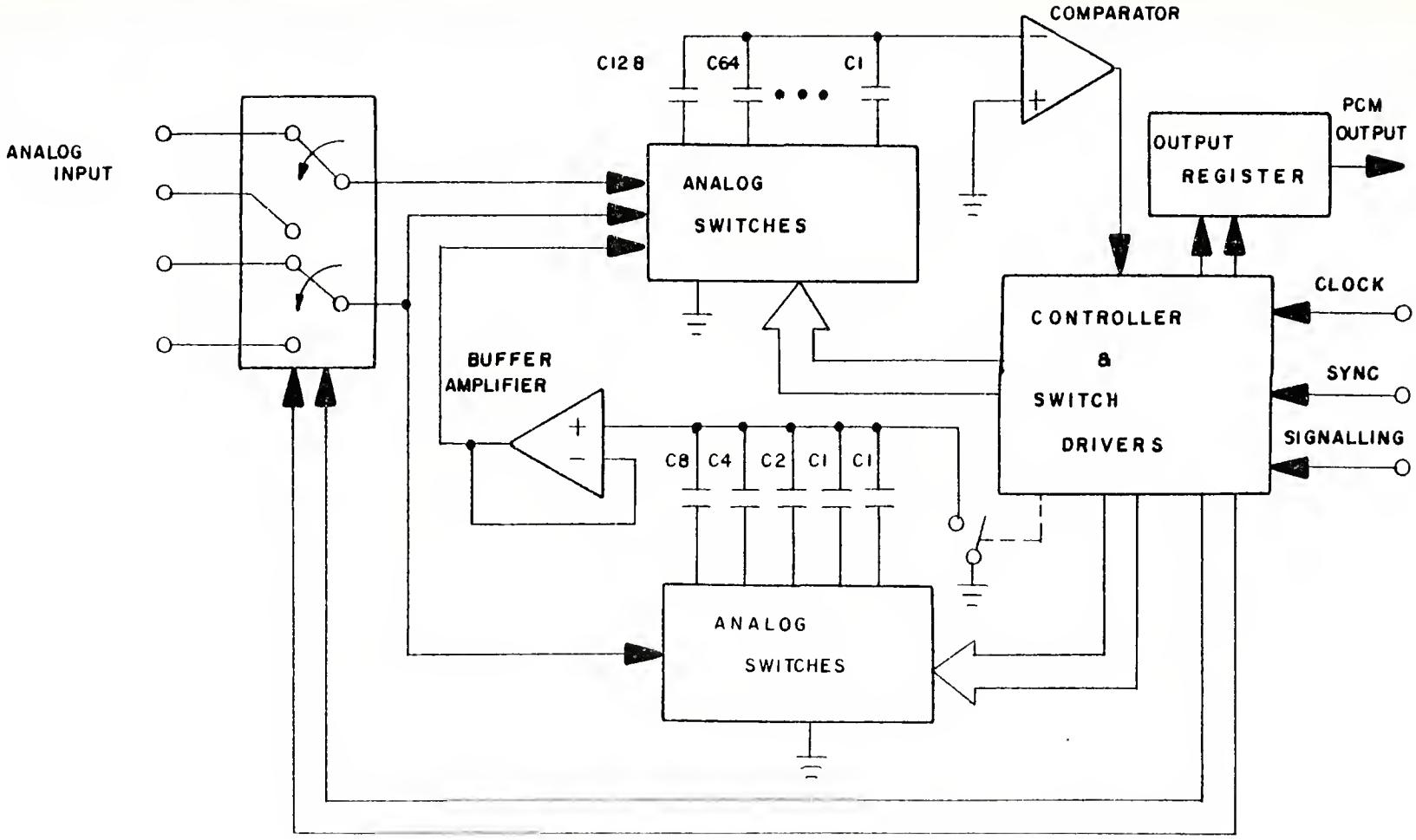


Fig.5 PCM coder DF331 block diogrom

quantizing while after transmission an expanding part in the decoder restores the amplitude to its former level. By this technique a preferential treatment is given to the weaker signals because their smaller amplitudes cover more quantization levels than they would otherwise. This is done at the expense of the large amplitude signals. However, since small amplitude values of speech occur more often than large amplitude values, the result is less quantizing error and higher signal-to-quantization noise ratio.

Two companding standards are internationally recognized, the μ-law and the A-law. The coder DF331 operates according to the μ-law for compression. The equation

$$F(x) = \text{Sgn}\ (x)\ \frac{\ln(1 + \mu|x|)}{\ln(1 + \mu)}\ ,$$

plotted as Fig. 6, defines the μ-law, where μ is a coefficient that determines the amount of compression. As shown in Fig. 6, the value $\mu = 0$ represents a linear conversion while increasing μ increases the converter's nonlinearity or compressing characteristics. The specific value of $\mu = 255$, adopted by the Bell telephone system, is used in μ-law PCM codecs.

The coder approximates the μ-255 law equation by a piecewise linear transfer characteristic as shown in Fig. 7.

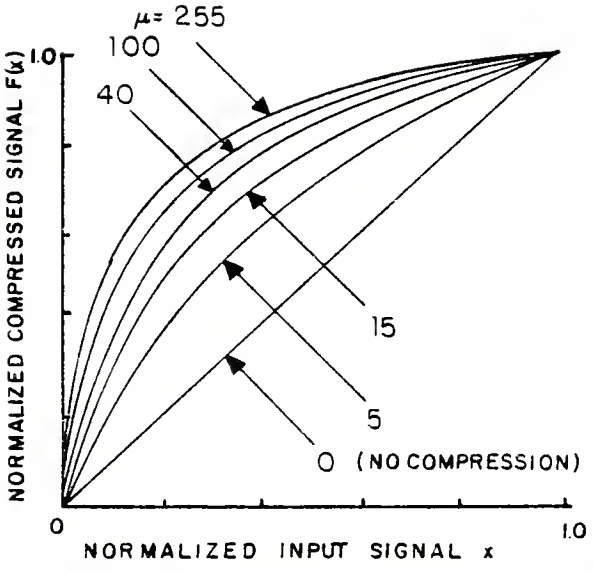


Fig. 6 Logarithmic compression characteristics for the μ-law equation

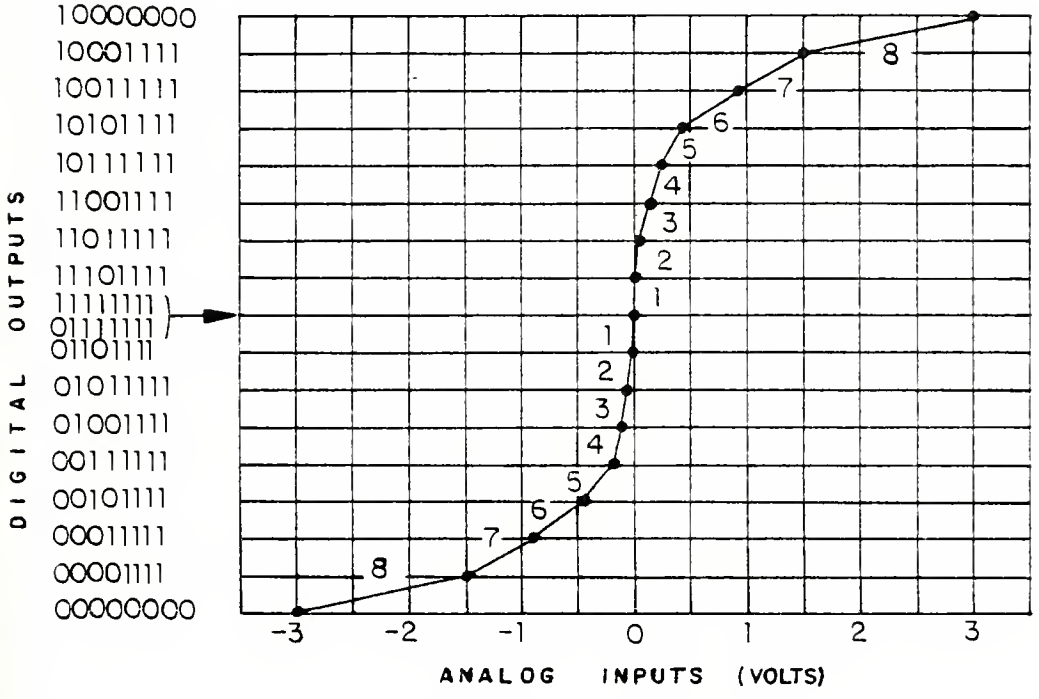


Fig. 7 Coder transfer characteristic

The binary codes in Fig. 7 represent the 8 bit words for the individual segments in the piecewise linear μ-255 law approximation. The first bit represents the sign of the sample taken. The next three bits represent the segment in which the sample lies. The last four bits represent the step within the segment. There is a total of 16 segments, 8 for each input polarity with each segment having 16 equal steps. The step size within each segment is constant but doubles in size from one segment to the next starting with the segment nearest the origin.

The coder operates as shown in Fig. 5. First the analog input voltage is sampled onto the lower plates of the capacitors that form the upper capacitor array. At the same time the upper nodes of both capacitor arrays are initialized. Next the sign of the sample is determined using the comparator by switching the lower plates in the upper capacitor array from input to ground. Then a successive approximation switching sequence is used to determine the segment of the μ-255 transfer characteristic within which the input sample lies. Finally the lower capacitor and switch array is used in a successive appproximation sequence to determine the step within the segment. One initialization cycle followed by eight comparator decision cycles are required.

When the proper binary code is determined, the eight bit word is loaded into the output shift register of the

coder. This register is unloaded at a fast clock rate upon receiving a synchronization (sync) pulse. The required fast clock rate is 1.544 MHz while the sync pulse occurs at an 8 kHz rate and is synchronized to the fast clock. The width of the sync pulse is 8 fast clock cycles. Both the fast clock pulses and the sync pulses are externally generated and directed to the corresponding coder inputs.

The fast clock is used for the high speed data transmission needed in multiplexed PCM channel bank systems and is internally divided to provide timing and control. The 1.544 MHz rate is standard in 24 channel PCM systems including the AT&T T1 system.

The sync pulse train is used to control the dumping of the output shift register in such a way that synchronized TDM transmission of many channels over a single line is possible. The 8 kHz sync pulse rate is exactly the sampling rate of the analog voice signal.

The digitally encoded information from the coder is transmitted in bit serial form at a 1.544 Megabits per second rate. The bit flow however is not continuous but occurs in 8 bit code words every 125 μsec because only one channel is processed and because the coder's output register unloads its contents at an 8 kHz rate. Consequently, the decoder at the receiving end accepts 8 bit code words every 125 μsec in synchronization with the coder's unloading. Thus the decoder needs the same clocking and synchronizing

circuitry for loading the 8 bit code words as the coder requires for unloading them. The decoder upon reception of the sync pulse loads its input register at the fast clock rate. The block diagram of the decoder is shown in Fig. 8.

A comparison of Fig. 8 with Fig. 5 indicates that there are many similarities between the encoder and decoder. Actually many internal circuits are of identical design. The decoder's DAC operates basically on the same capacitive ladder arrangement. The digital input is stored in the input register. Then each 8 bit code word controls the logic to the switch drivers. The switch drivers operate the analog switches which in turn switch the capacitors from the capacitor arrays to construct the corresponding analog output. A sample-and-hold circuit is included at the DAC output to facilitate the discharge of the capacitor arrays between decode operations.

The decoder operates according to the μ-255 law for expansion and thus approximates the inverse of the μ-255 law equation by a piecewise linear transfer characteristic as shown in Fig. 9. The analog output of the decoder is in the form of voltage pulses having the duration of a sync pulse and amplitude approximately equal to that of the encoded sample of the analog input signal.

To reconstruct the actual analog voice signal from these pulses a receive lowpass filter is needed. The

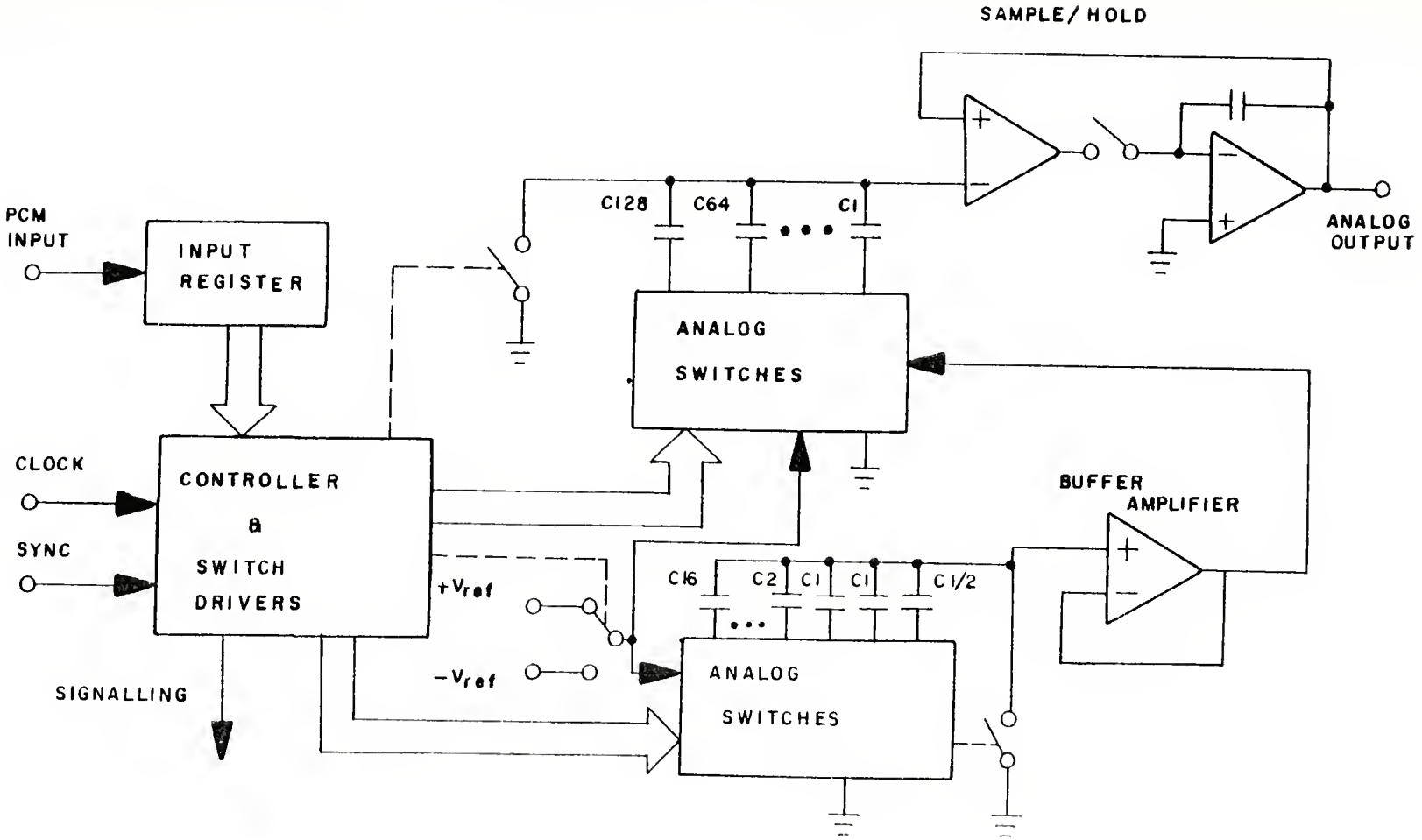


Fig. 8 PCM decoder DF332 block diagram

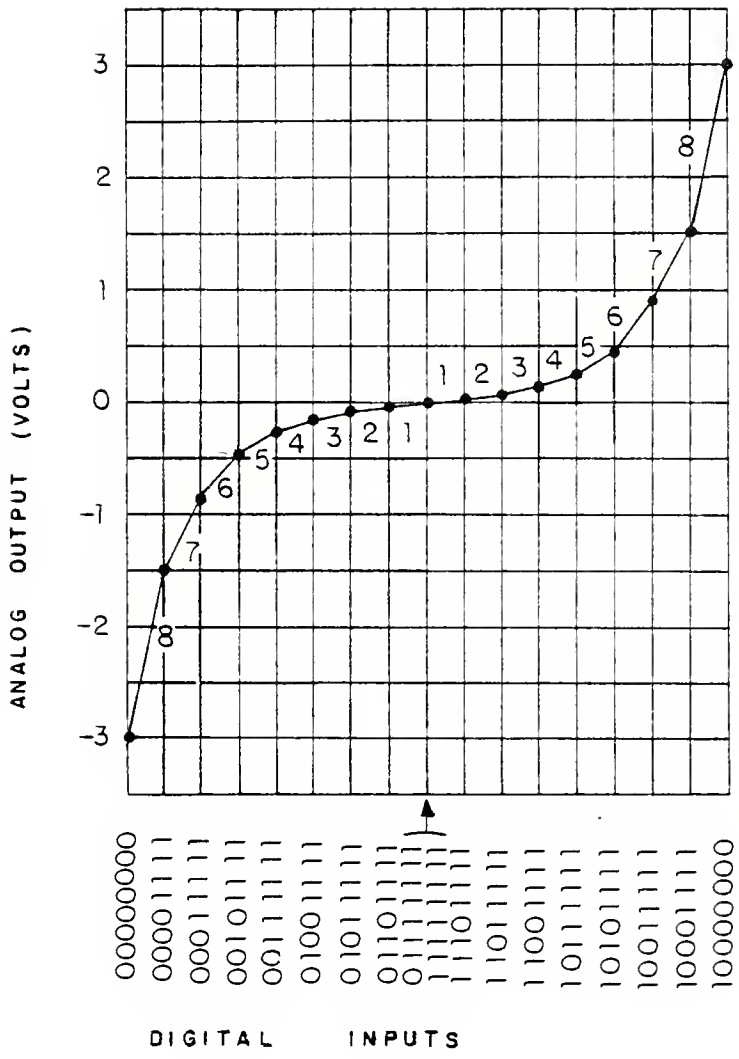


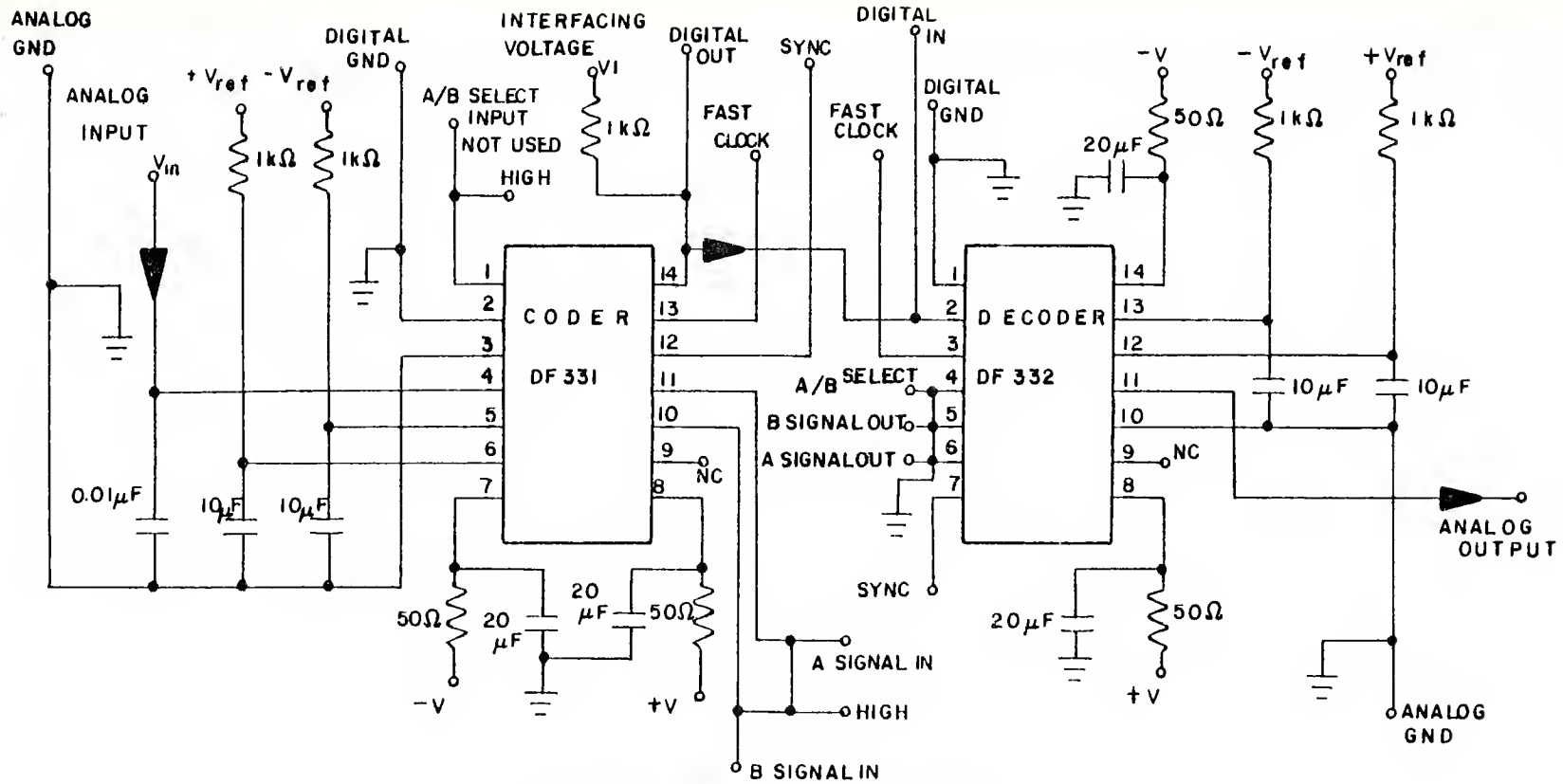
Fig. 9 Decoder transfer characteristic

receive filter has two functions. One function is to attenuate all frequencies above the usable voice band. The other function is to correct for the amplitude distortion introduced by the decoder sample-and-hold circuit.

III. TYPICAL CODEC PIN CONNECTIONS

To operate the codec pair DF331/DF332, circuitry like that shown in Fig. 10 is required. Fig. 10 also indicates voltage ranges and specific values used in this work.

In addition to typical pin connections, four items need special attention. First, the analog input voltages must be between the positive and negative reference voltages for accurate encoding. Second, there are separate analog and digital grounding pins to reduce system noise problems. Third, the digital output of the DF331 is an active low open drain output. This feature exists to allow easy interfacing to TTL and CMOS multiplexers when many such DF331 outputs are multiplexed in a PCM channel bank system by one multiplexer. Thus there is a need for a pull-up resistor and an interfacing voltage V_1 to be connected to this output, as shown in Fig. 10. Fourth, two signalling bit inputs A and B are provided on the DF331 to allow insertion of signalling information into the transmitted data stream. Signalling is a necessary process in telephony by which a caller on the transmitting end informs a particular party at the receiving end that a voice message is to be communicated. Signalling is also that supervisory information that lets the caller know that the called party is ready to talk, that his line is busy or that he has hung up. This information occurs as the least significant bit



Voltages	Ranges	Typical values
+V	$0 < +V < 11V$	+ 7.5 V
−V	$-11V < -V < 0$	− 7.5 V
+Vref	$0 < Vref < +V$	+ 3 V
−Vref	$-V < -Vref < 0$	− 3 V
VI	As required	+5V, +7.5V
Vin	$-Vref < Vin < +Vref$	$-3V < Vin < +3V$
LOGIC	0, +V	0, + 7.5 V

Fig. 10 Typical codec pin connections

(LSB) in the transmitted 8 bit code word. Therefore, when signalling is enabled by proper setting of the A/B select input on the DF331, each voice signal sample gets a seven bit code instead of an eight bit code because its LSB is stolen for signalling. In this particular work, this process is not needed and consequently all the inputs/outputs on the DF331/DF332 that provide signalling are connected either to high (+V) or to ground.

IV. CLOCKING AND SYNCHRONIZING CIRCUITRY

To operate the coder-decoder chips fast and in synchronization, a fast clock and a sync pulse must be externally provided. The fast clock and the sync pulses must be unipolar 0 to +7.5V. For the fast clock the value +7.5V is a necessary requirement, while for the sync pulse a value between +3.5 to +7.5V is acceptable. The fast clock and sync pulses must be free of overshoot and noise. The fast clock rate is 1.544 MHz while the sync pulse occurs at an 8 kHz rate. The sync pulse is synchronized to the fast clock. Its duration is 8 fast clock cycles or pulses. The fast clock and the sync pulses are shown in Fig. 11a and 11b respectively.

A pulse generator is used as the fast clock source in this experiment. The sync pulses are derived then from the fast clock by using a few medium scale integrated (MSI) circuits, as shown in Fig. 12. There are two binary counters (74161 divide by 16 counter) that are cascaded in such a way to provide frequency division by integers, from 1 through 256. These counters are set to divide by 193 by having their load inputs connected properly either to high or to ground. The required clock to operate the counters is the fast clock. As a result of their operation an output positive pulse is generated at the carry-out pin of the second counter. This pulse occurs at an 8 kHz rate since

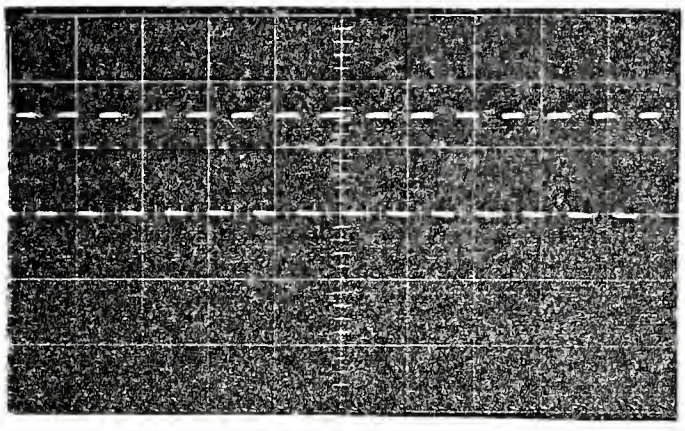


Fig. 11a. Fast clock 1.544 MHz, 1 μsec per horizontal division, 5 V per vertical

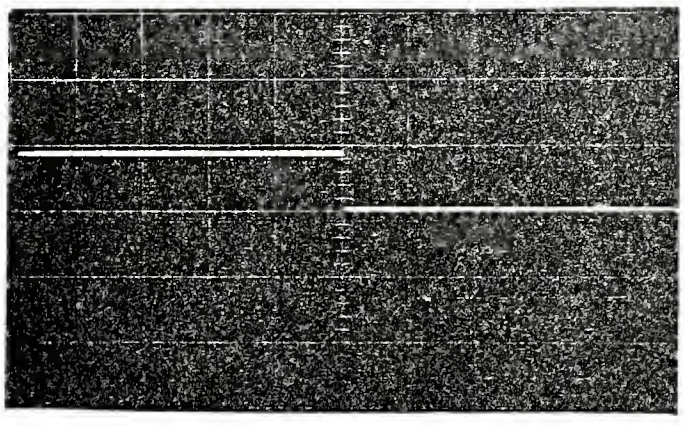


Fig. 11b. Sync Pulse 8 kHz, 1 μsec per horizontal division, 5 V per vertical

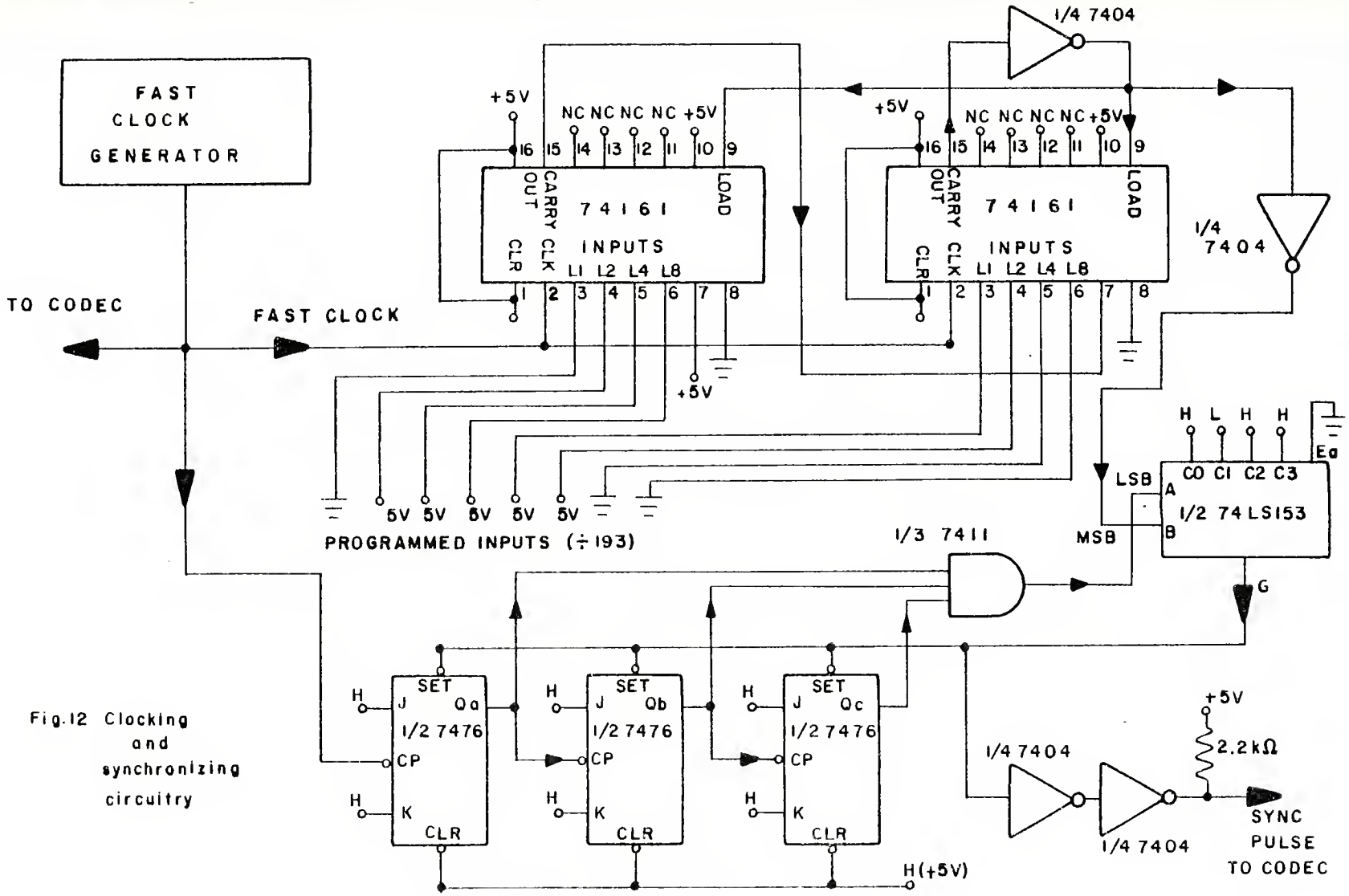


Fig.12 Clocking and synchronizing circuitry

1.544 MHz ÷ 193 = 8 kHz, and its duration is one fast clock cycle.

The inverter (7404) that is connected to the carry-out pin is used to bring the load pins of both counters low as specified. The second inverter is used to bring the output pulse back to positive polarity. This pulse is used then as the most significant address bit to a 1-of-4 multiplexer (74LS153) operating as a function generator. The least significant address bit to this multiplexer is provided by a three-bit counter and an AND gate. Three JK flip-flops (7476) are used to form the asynchronous three-bit binary counter. The required clock to the first flip-flop is again the fast clock. When this counter counts eight fast clock pulses, a binary 111 is generated at the flip-flop outputs and a positive pulse occurs at the output of the AND gate (7411). The counter is allowed to count every 125 μsec for a duration equal to 8 fast clock pulses. This is accomplished by the multiplexer output that sets the counter according to the required timing. Thus, when the three-bit counter is set as described and the ÷ 193 divider provides an output pulse waveform, the multiplexer select inputs A,B address one out of four multiplexer inputs $C_0C_1C_2C_3$, according to the truth table shown in Fig. 13.

As a result an output pulse train G is generated at the multiplexer output that meets the requirements of the

SELECT INPUTS		ADDRESSABLE INPUTS				OUTPUT
B	A	C0	C1	C2	C3	G
L	L	H	L	H	H	H
L	H	H	L	H	H	L
H	L	H	L	H	H	H
H	H	H	L	H	H	H

Fig. 13 Truth table for the generation of the sync pulse waveform

sync pulse waveform. The last two cascaded inverters form a noninverting buffer that improves the sync pulse rise time and interfaces the TTL logic circuits to the CMOS codec circuits.

V. THE SINGLE CHANNEL CODEC SYSTEM

The block diagram of the complete single channel codec system is shown in Fig. 14. For presentation purposes this diagram has been separated into three main sections: input, output, and codec. The codec section has already been discussed. The input and output sections are considered here.

A. THE INPUT SECTION

The input section consists of an analog signal source, an audio amplifier and a lowpass filter as shown in Fig. 15.

A function generator or a cassette recorder is used to provide the necessary analog input signals. An audio amplifier (380) is used then to provide gain adjustment. This initial stage of amplification and gain adjustment is required mainly for two reasons. First, the signal entering the lowpass filter must be strong enough to overcome the noise that is generated by the filter itself and by the rest of the system. Second, the input analog signal to the coder chip must be conditioned to a specific amplitude range for correct encoding.

The external circuitry and the pin connections that are needed for the operation of the amplifier are shown in Fig. 15. Features of the linear integrated amplifier 370 include, an internally fixed gain of 34 dB, a bandwidth

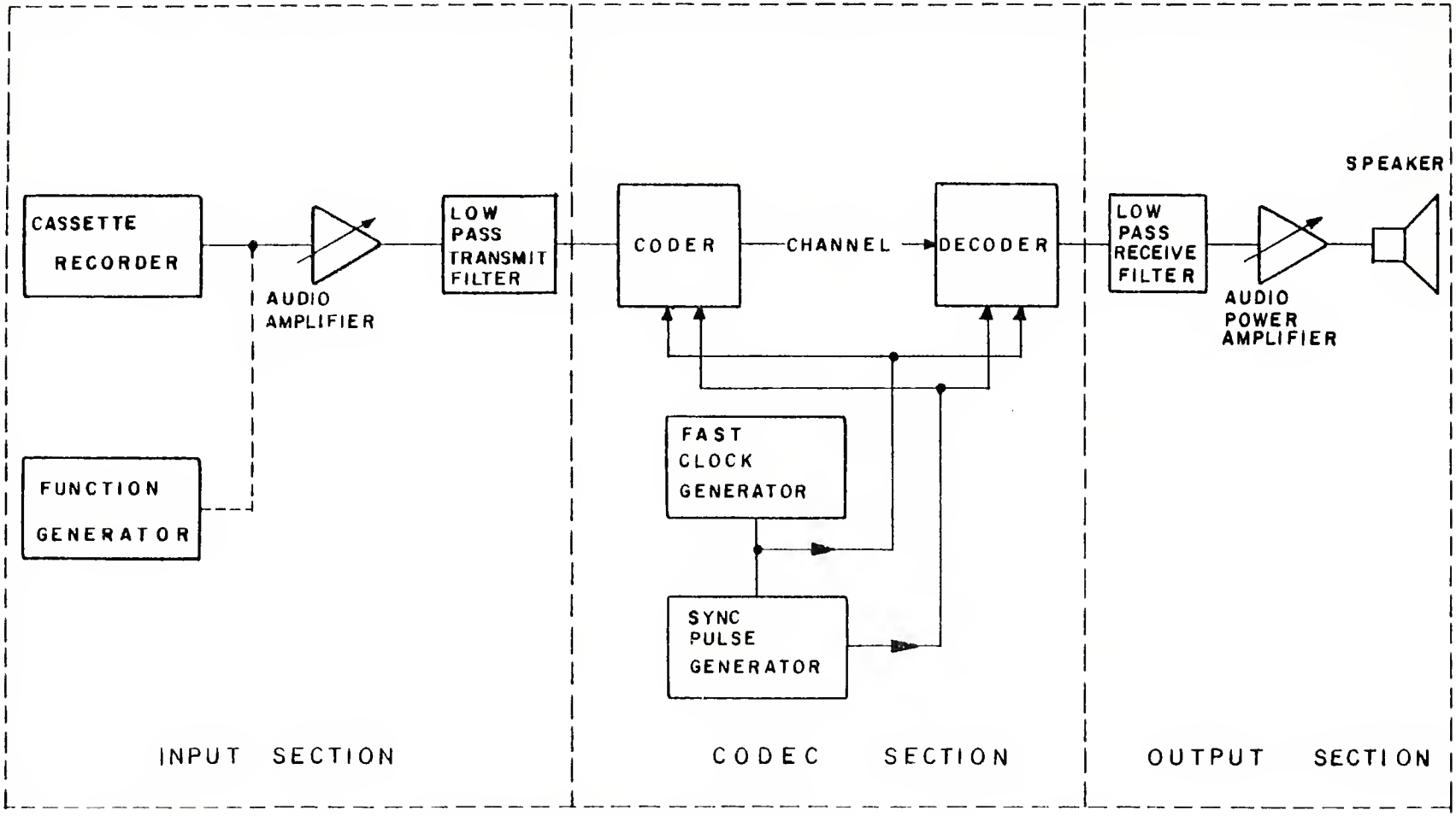


Fig.14 Block diagram of the single channel codec system

R1=10kΩ POT
R2=2.7Ω
R3=10kΩ
R4=392kΩ
R5=2.67kΩ
R6=22.6kΩ
R7=57.6kΩ

C1=5μF
C2=.1μF
C3=.0047μF
C4=500μF

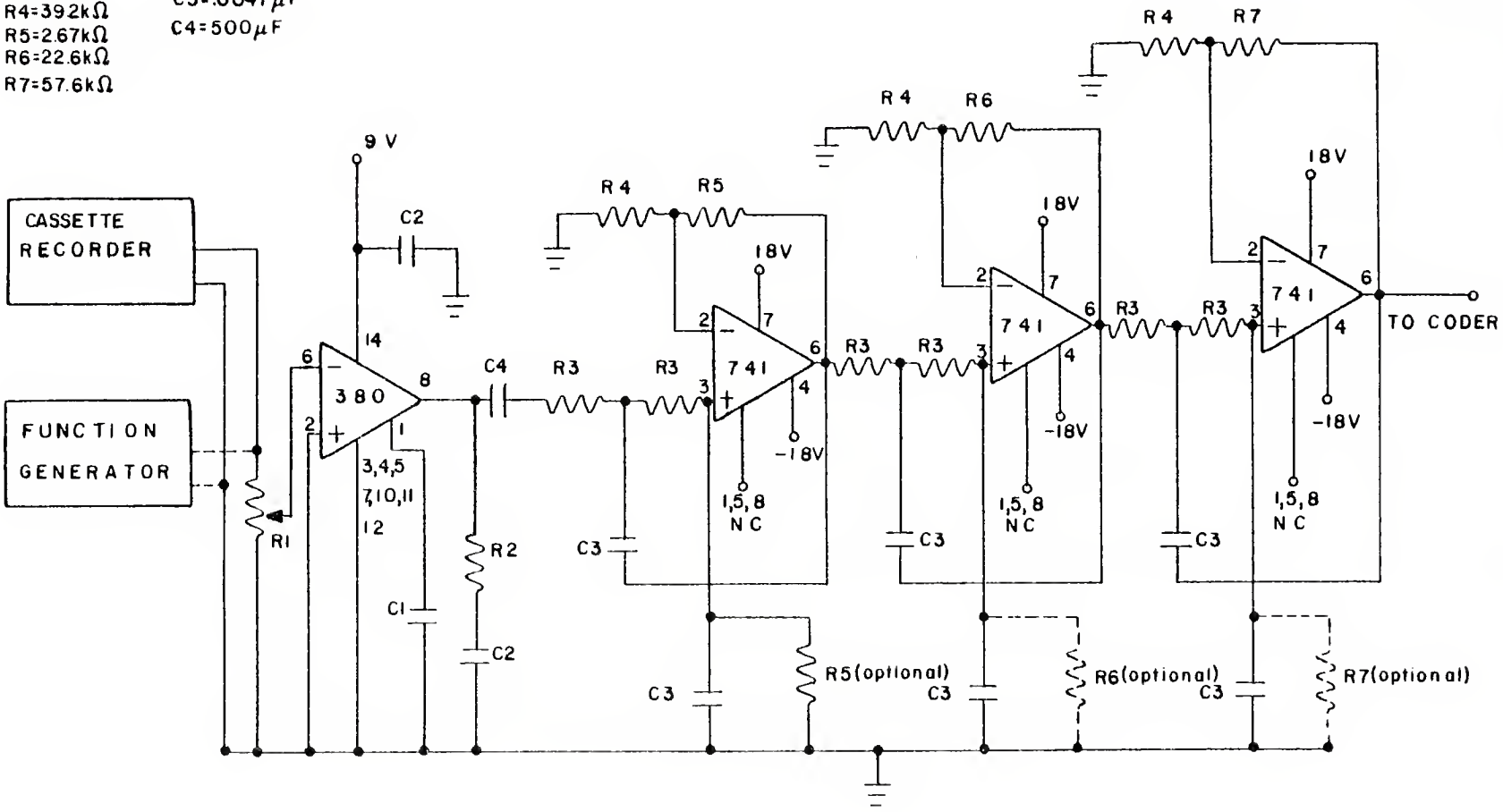


Fig 15 The original input section

of 100 kHz, an input stage that allows inputs to be ground referenced or AC coupled as required, and a wide range of supply voltages (9V to 22V).

An active lowpass filter implemented by three operational amplifiers (741) is shown next in Fig. 15. This is a typical Butterworth type lowpass filter. Its design is based upon the requirements for a fast fall off after 3.6 kHz and a relatively flat amplitude response from DC to 3.2 kHz. To meet these requirements, three second-order lowpass sections are cascaded. The values of the passive elements involved are specified by active filter handbook tables [Ref. 5] according to the imposed requirements. The net result is a sixth-order Butterworth lowpass filter providing a reasonable -36 dB/Octave roll off after 3.6 kHz and a tolerable amplitude and phase response as shown in Fig. 16a and 16b. Since this filter is used in a voice transmission system the small phase distortion is tolerable.

The gain of the filter can be set to a maximum of 12 dB, if all the optional resistors shown in Fig. 15 are removed. However, removal of these resistors that provide a DC path to ground can cause an offset voltage in the range of 2 to 3V to appear at the filter's output. Such an offset voltage is undesirable because it can restrict the dynamic range of the filter and consequently the range of the coder. Thus a 2.7 kΩ resistor is connected to the non-inverting input of the operational amplifier at the first

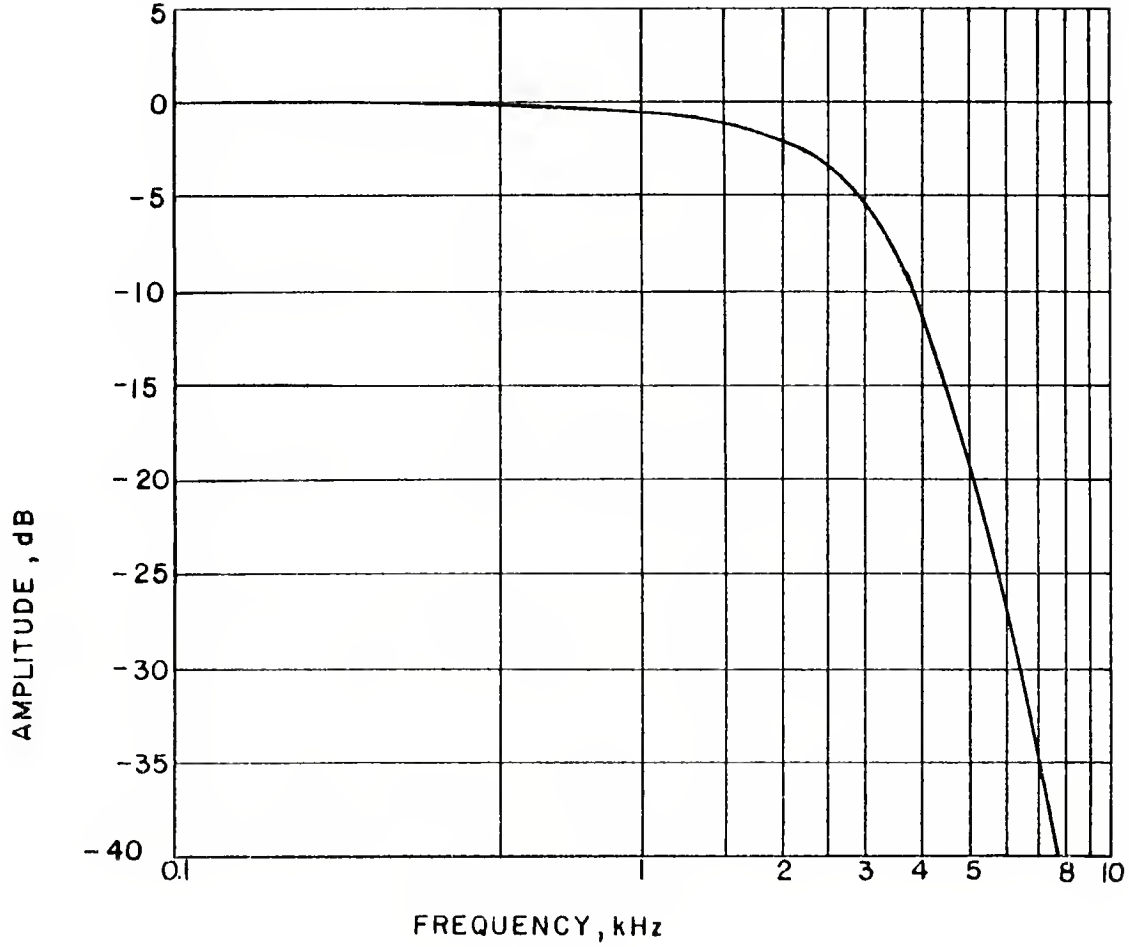


Fig.16a Amplitude response of the 6th order Butterworth filter

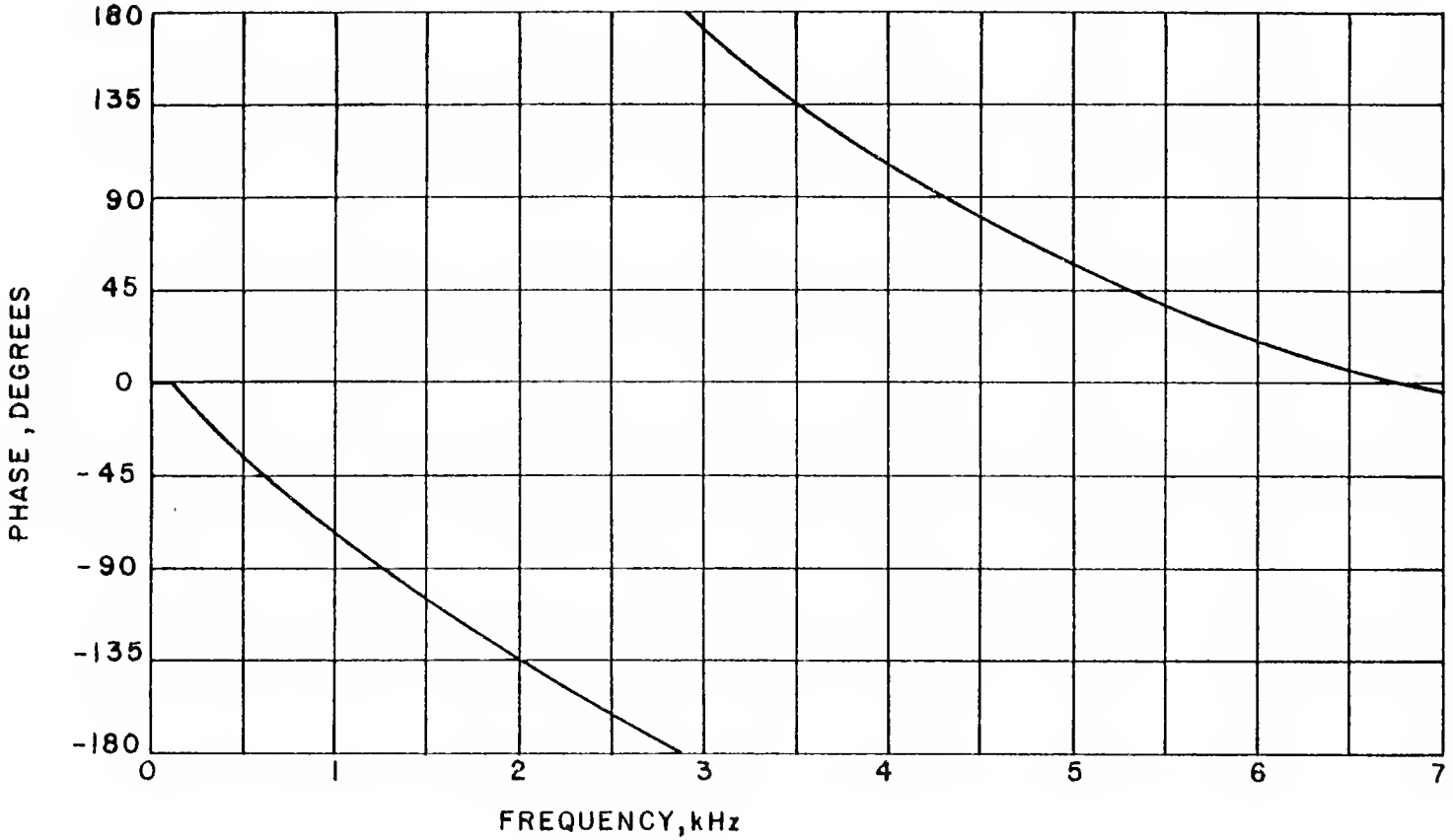


Fig.16b Phase response of the 6th order Butterworth filter

second-order section. With this resistor, offset voltages are reduced to less than 100 mV while the filter's gain is limited to 0 dB.

This filter was used successfully until the hybrid transmit filter AF133 was available. The final input section including the transmit filter AF133 is shown in Fig. 17. Detailed specifications of this fifth-order elliptic filter can be found in the manufacturer's report on the AF133/AF134 filters [Ref. 30].

The AF133 filter consists of two separate sections that are joined externally by connecting pin 5 to pin 8. Filter gain adjustment is desirable. An external resistor connected between pins 17 and 18 provides this gain adjustment and renders the filter operative. The nominal value of the resistor required is 133 kΩ for a 0 dB voltage gain. Unused pins have been left open in Fig. 17.

B. THE OUTPUT SECTION

The output section consists of a lowpass filter, an audio amplifier and a speaker, as shown in Fig. 18. A comparison of Fig. 18 with Fig. 15 indicates that originally the input section was identical to the output section. The same active filter scheme was used to implement both the transmit and receive filters. This filter scheme was used until the hybrid receive filter AF134 was obtained. The final output section using the AF134 filter is shown in Fig. 19.

R1=10kΩ POT
R2=2.7Ω
R8=100kΩ
R9=Not specified
R10=133kΩ

C1=5 μF
C2=.1μF
C4=500μF

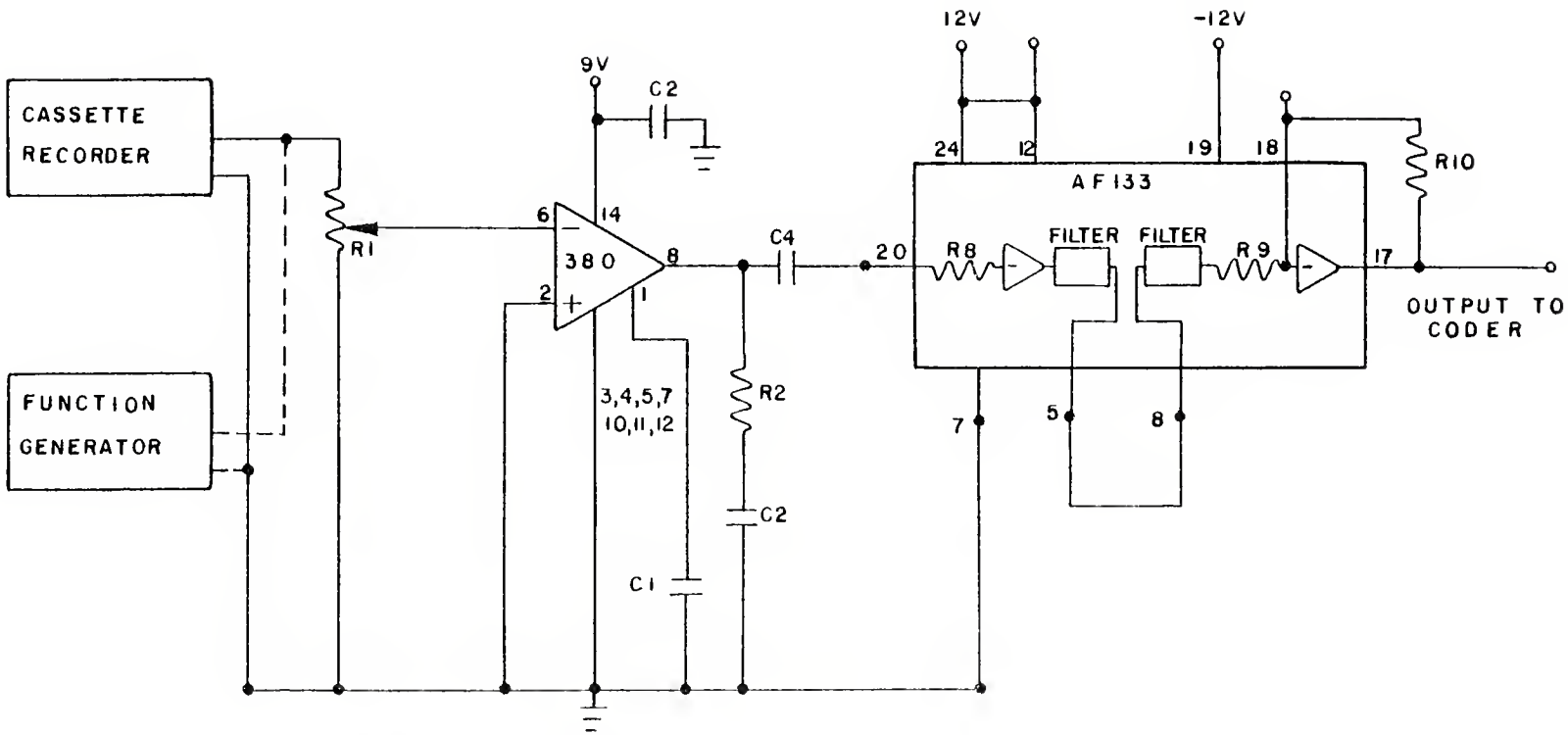


Fig. 17 The final input section

R3=10kΩ
R4=39.2kΩ
R5=2.67kΩ
R6=22.6kΩ
R7=57.6kΩ
RII=25kΩ POT
R2=2.7Ω

C1=5 μF
C2=.1μF
C3=.0047μF
C4=500 μF

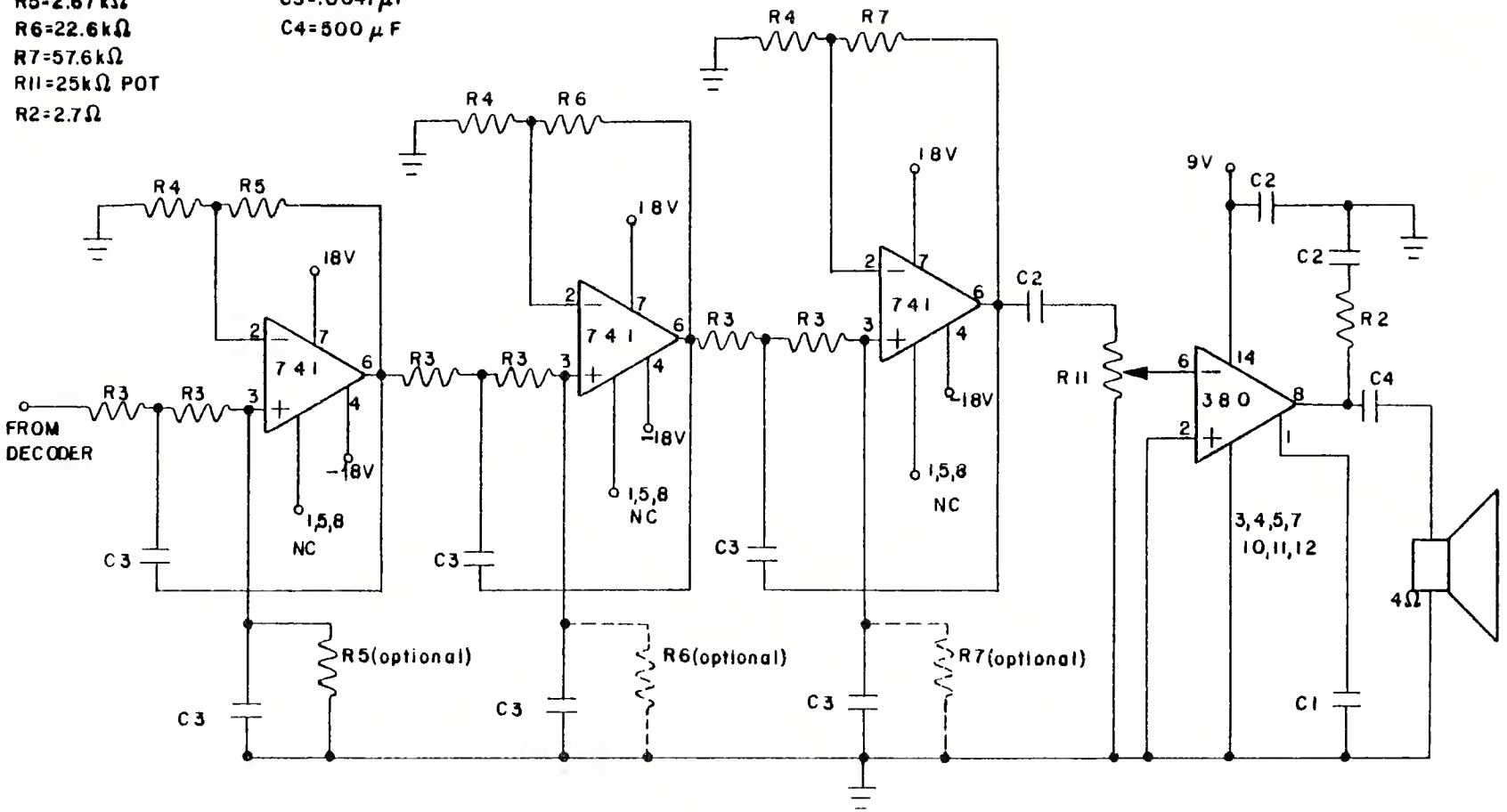


Fig.18 The original output section

R2=2.7Ω C1=5 μF
R8=100kΩ C2=.1 μF
R11=25kΩ POT C4=500 μF
R12=100kΩ POT

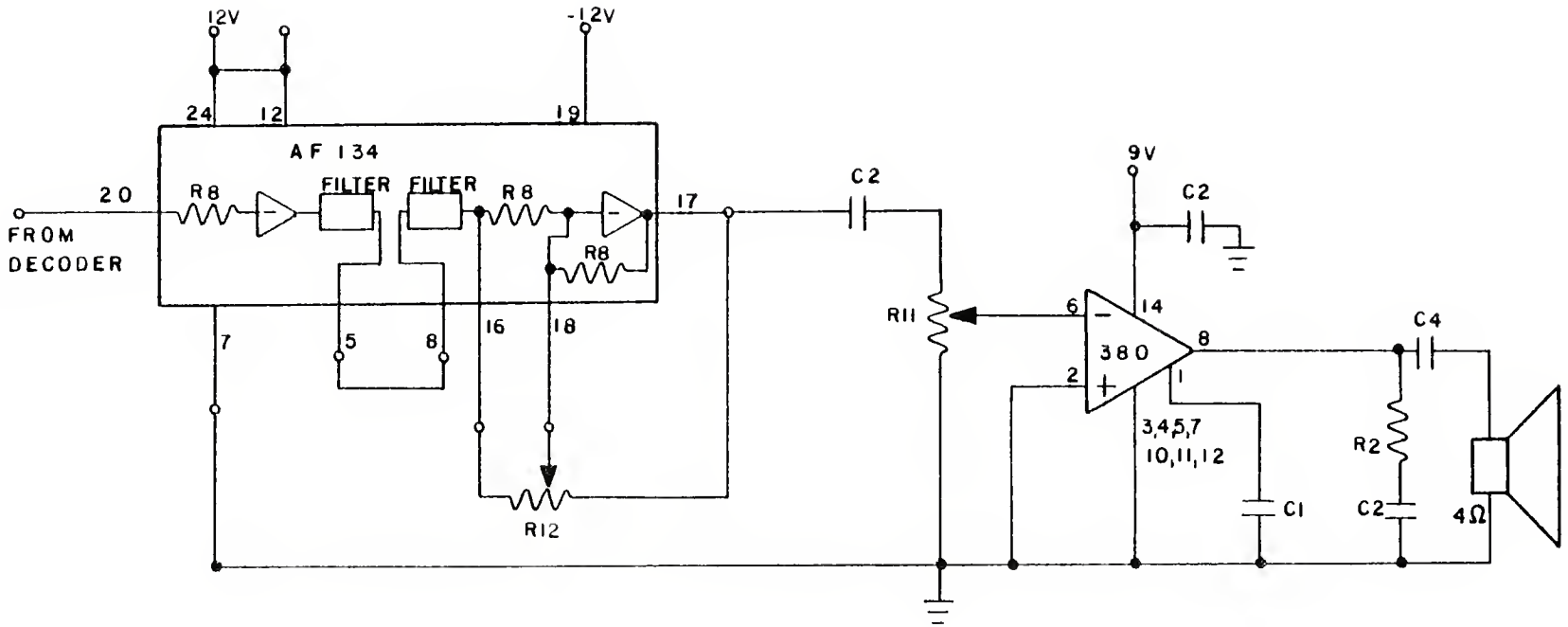


Fig.19 The final output section

The filter AF134, like the filter AF133, consists of two separate sections which must be connected together externally. Likewise, provision has been made to adjust the gain of the filter by a 100 kΩ single pot connected between pins 16 and 17 with the wiper arm tied to pin 18. Unused pins have been left open as specified.

Finally, an audio power amplifier similar to that used in the input section provides the power to drive a 4 Ohm speaker.

VI. CONTROLLED ERROR GENERATOR

There are many sources of errors in the data bits of an operating voice transmission system. These include natural noise, switching (impulse) noise, cross-talk, etc.

Noise may cause a transmitted "1" to be falsely received as a "0" and a transmitted "0" to be falsely received as a "1".

In this work we want to investigate the effects of bit errors in the 8-bit word used in voice transmission systems. So, we deliberately introduce errors in a controlled manner by using the MSI circuits shown in Fig. 20. We use a serial-in/parallel-out (SIPO) 8 bit shift register, an array of 8 Exclusive-OR (EX-OR) gates, a parallel-in/serial-out (PISO) 8 bit shift register, a programmable divider similar to that shown in Fig. 12, a delay circuit and a parallel loading enable pulse generation circuit.

The SIPO shift register is loaded serially with 8 bit data words every 125 μsec at the fast clock rate. Then each one of the 8 bits A through H is transferred in one of two ways. The first way is to be loaded undisturbed to its corresponding input of the PISO shift register. This is done by setting the R input of the EX-OR gate relative to that bit low. Thus in this case no error occurs in that bit. The second way is to be inverted by its relative EX-OR gate before it is loaded to the PISO shift register.

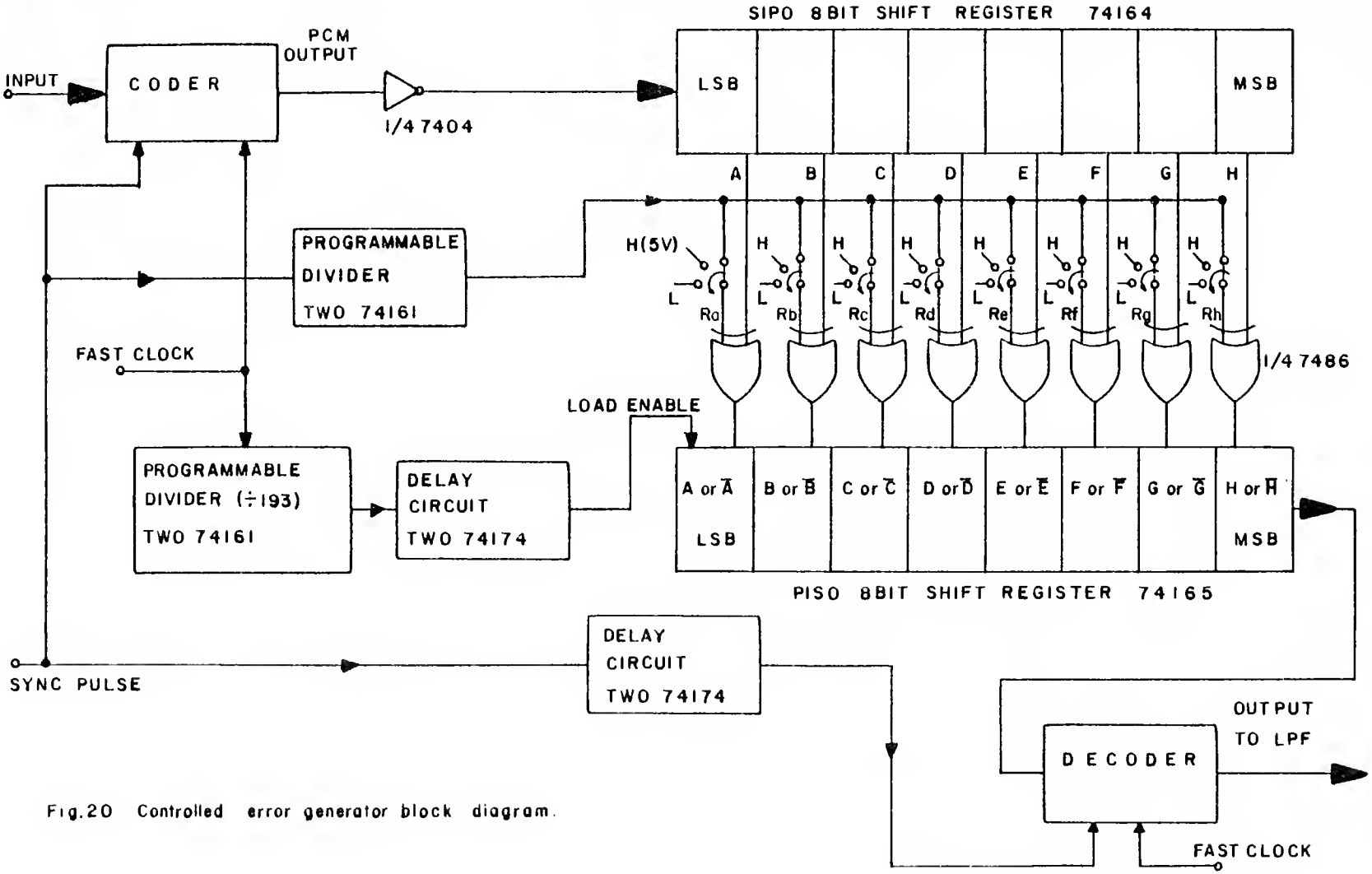


Fig.20 Controlled error generator block diagram.

This is accomplished by setting the R input of the EX-OR gate relative to that bit high. In the second case therefore an error occurs in a specified bit of that data word.

The PISO shift register is loaded simultaneously by the 8 bit word if and only if its load input becomes low. It is required also to load this register each time the SIPO shift register contains exactly an 8 bit word. This is accomplished by providing a loading enable pulse sequence to the load input of the PISO shift register. This pulse has a duration of one fast clock cycle, occurs every 125 μsec, and it is delayed in relation to the sync pulse or data group by 8 fast clock pulses. Thus, it occurs immediately after the loading of the SIPO shift register. When the PISO shift register is simultaneously loaded by the 8 bits of the data word, it starts to dump its content every 125 μsec at the fast clock rate.

To have the ability to control the number of errors in a certain number of transmitted data bits, any one of the R inputs to the EX-OR gates needs to be set high according to a specified rate and not continuously, because the latter results in an error in each 8 bit data word. Further, this rate must be easily changed to different values to ensure different error rates. This is accomplished by the programmable divider shown in Fig. 20. To obtain an error rate of 10^{-3} (1 error for each 1000 bits), this divider is set to divide by 125, and the sync pulses are used to clock it.

At this point note that the data bit stream (8 bits every 125μ sec) and the sync pulse train (pulses of 8 bit duration every 125μ sec) have the same rates. Thus the divider generates a pulse every 125 sync pulses or every 1000 (125 x 8) transmitted data bits. These pulses are used then to enable any R input high which in turn causes an error to occur at the specified rate. Meanwhile, all the other R inputs remain low. The net result of this operation is that an error occurs every 1000 transmitted data bits. Because the divider is programmable, and since there is a provision to alter any one bit or any combination of several bits in each 8 bit data word, any error pattern can be generated.

The SIPO and PISO shift registers as well as the EX-OR gates add a delay to the transmission of the data words. This delay equals or is greater than 8 fast clock pulses. Thus for proper codec operation the loading of the decoder's input shift register needs to be delayed by the same interval that the data words are delayed by the error generator circuit. Because the sync pulses determine when the decoder's input shift register must be loaded, it is these pulses that must be delayed. The circuit required for this operation is shown in Fig. 20. This delay circuit adds a delay to each sync pulse equal to 9 fast clock pulses, and it is implemented by 9 cascaded D flip-flops (two 74174 MSI circuits).

In addition to the delay circuit the fast clock rate needs to be adjusted to values greater than 1.544 MHz, namely to 2.5-2.8 MHz, to compensate for the delay introduced in the data path. Conseuqently, all the other pulse waveforms which are related to the fast clock change rates. These changes however do not affect codec operation or the error rates as long as the sync pulse duration remains eight fast clock pulses.

The circuitry required for the operation of the shift registers and the EX-OR gates is shown in Fig. 21. Fig. 21 also shows the parallel loading, enable pulse circuitry. Note that the divider (÷193) in Fig. 20 is that divider used previously in Fig. 12 for the generation of the sync pulse, and therefore, it is not included in Fig. 21. The other divider that controls the error rate in Fig. 20 has been implemented similarly using the circuitry shown in Fig. 12 (two 74161chips).

Division by 125 is accomplished by this divider when its L inputs are set as follows: first 74161 chip, L_1 = low, L_2 = high, L_4 = low and L_8 = low; second 74161 chip, L_1 = low, L_2 = low, L_4 = low and L_8 = high. In Reference 3 information is given for division by any other number between 1 and 256. The circuitry needed to delay the sync pulse is shown in Fig. 22.

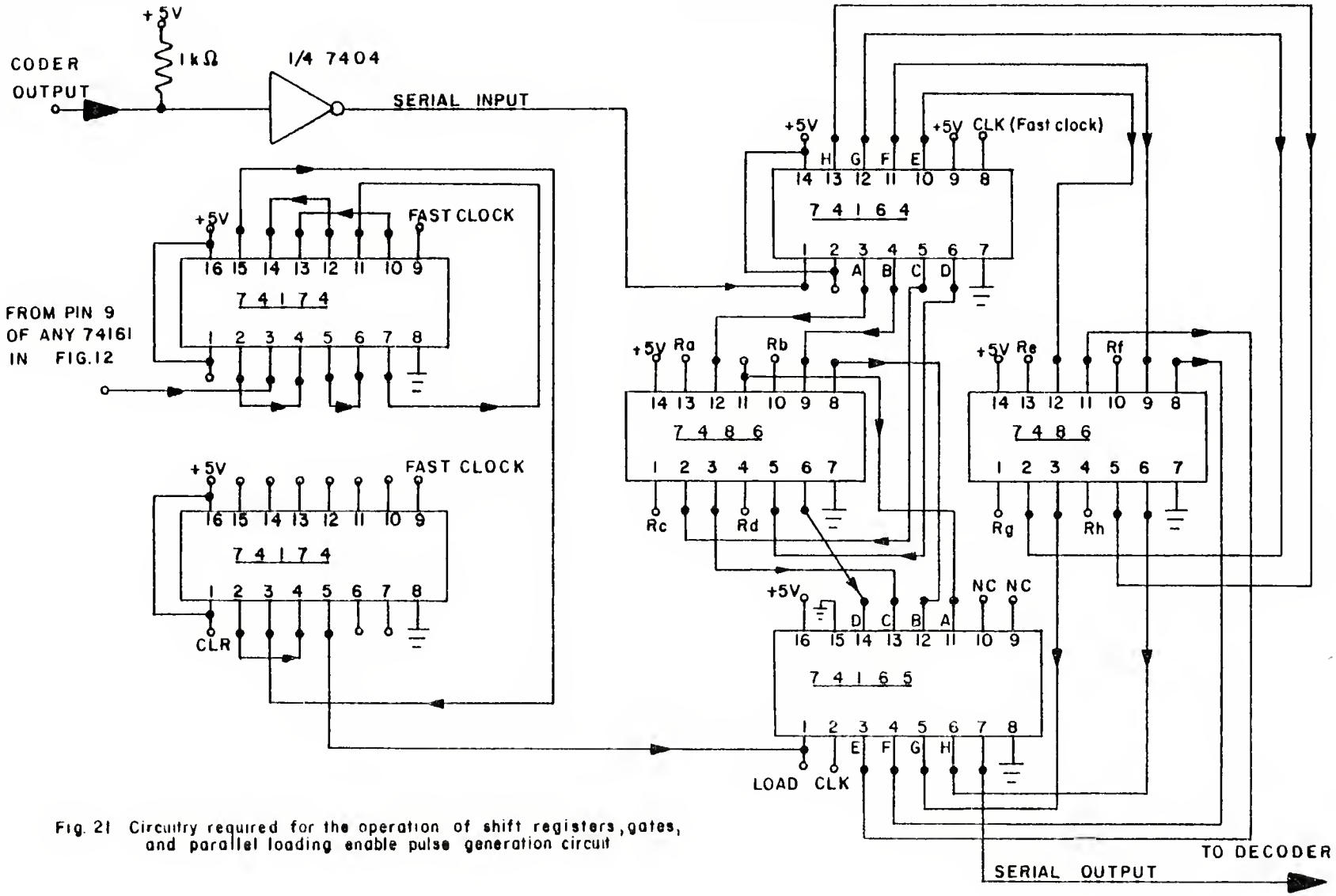


Fig. 21 Circuitry required for the operation of shift registers, gates, and parallel loading enable pulse generation circuit

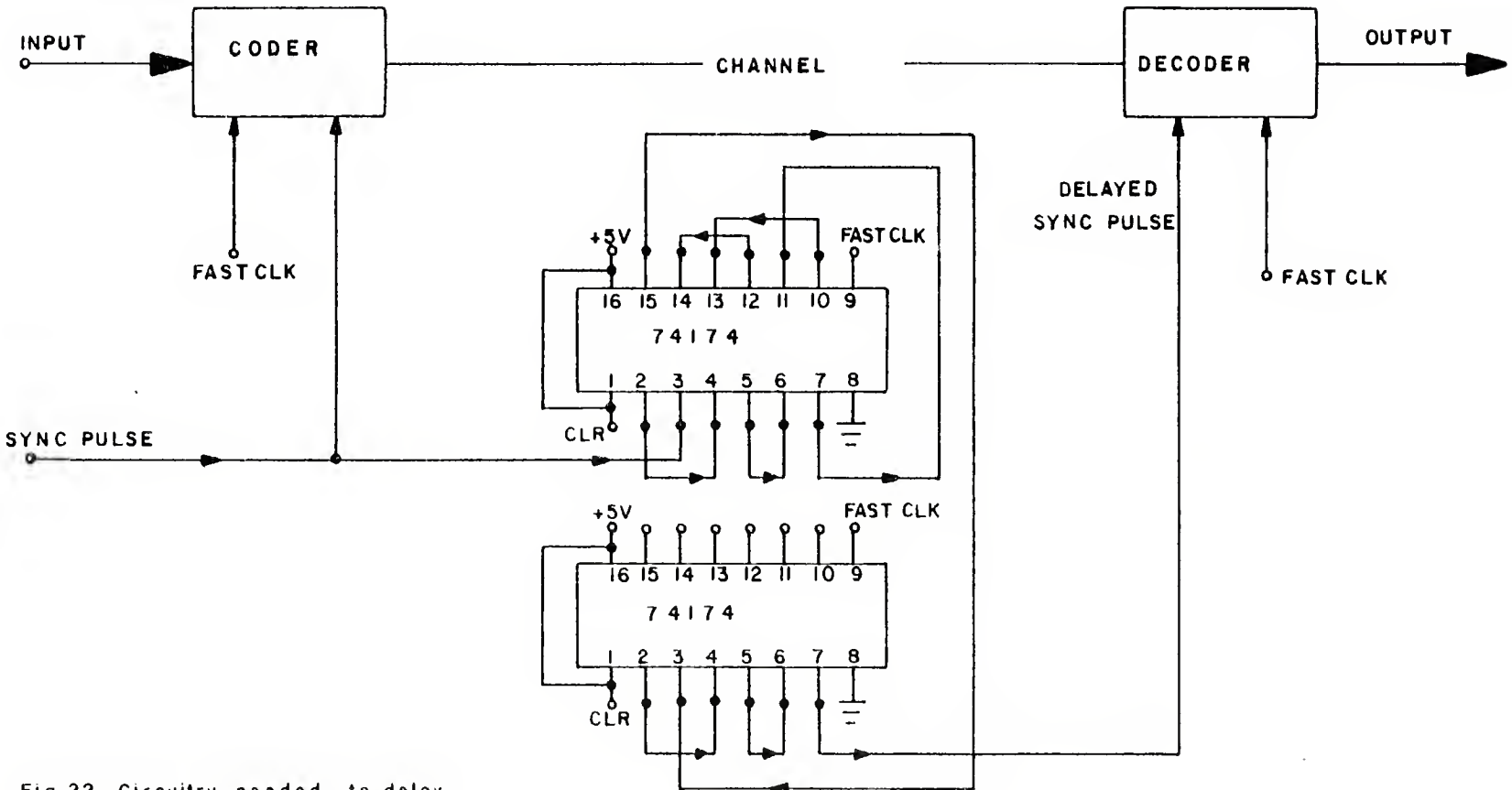


Fig. 22 Circuitry needed to delay the sync pulse.

VII. EXPERIMENTAL RESULTS

To evaluate the performance of the system, analog inputs of various forms and frequencies including DC were used first. Then, voice and music were applied to the system. Inputs such as DC, sinusoids, triangular waves and square waves were filtered, sampled, encoded and decoded by the system with results shown in Fig. 23 through 46.

Sine waves at audio frequenceis, 300 to 3300 Hz as well as DC voltages are processed by the system without detectable distortion. Triangular waves suffer some distortion by the transmit lowpass filter, while square waves are distorted more severely by the same filter. This distortion is expected since waveforms like triangular, square and pulse contain high frequency components that are not allowed to pass the transmit lowpass filter.

In any case the coder and the decoder follow the variations of the filtered input signal with great accuracy.

Voice and music were processed by the system without any apparent distortion. Voice signals especially, sounded by the speaker at the receiving end as clearly as the recorder could provide. Recall that this system is a companded PCM transmission system operating at 64 kBit per second data bit rate (8000 samples/second x 8 bits/sample) which is one of the highest bit rates in use in digitized voice transmission systems. Thus such a high output voice

quality is expected. The signal to noise ratio measured at the receive filter output is 41.5 dB.

Figs. 47 through 55 show cases where different error patterns are generated in the transmission channel. These include single errors in different bits in each 8 bit data word.

It was observed that if the MSB of each 8 bit data word is in error then the regenerated signal experiences the most severe distortion as shown in Fig. 48. On the contrary, if the LSB of each 8 bit data word is lost then the regenerated signal is almost the same as the error free signal, as shown in Fig. 55. This is why the LSB of each 8 bit data word is used for signaling in PCM telephone systems.

At this point recall that the first bit (MSB) represents the sign of the sample taken by the coder. The 2nd, 3rd and 4th bits represent the segment of the μ-law characteristic in which the sample lies and the 5th, 6th, 7th and 8th bits represent the step within the segment. Thus errors occuring in the last four bits are not so critical. And, as shown in Figs. 52, 53 and 54, if the 5th, 6th or 7th bit is lost then the regenerated signal experiences a small distortion. Errors in the 2nd, 3rd or 4th bit affect more or less the regeneration of the signal as shown in Figs. 49, 50 and 51.

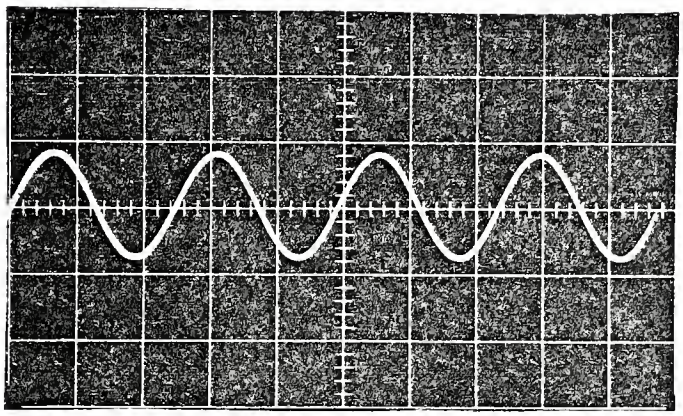


Fig. 23. 400 Hz sine wave input to the system, 1 msec per horizontal division, .2 V per vertical

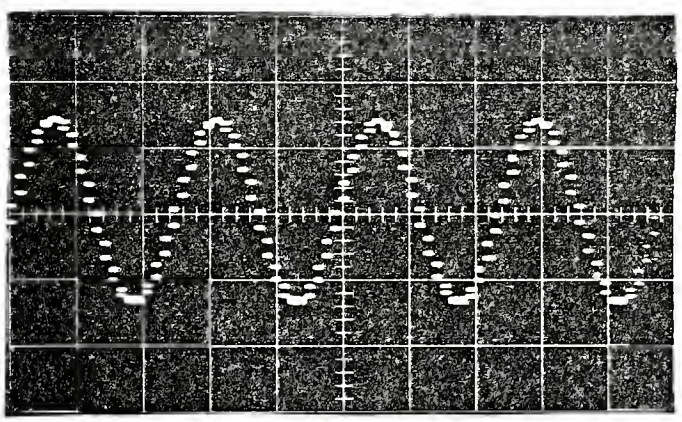


Fig. 24. 400 Hz sine wave decoder output, 1 msec per horizontal division, 2 V per vertical

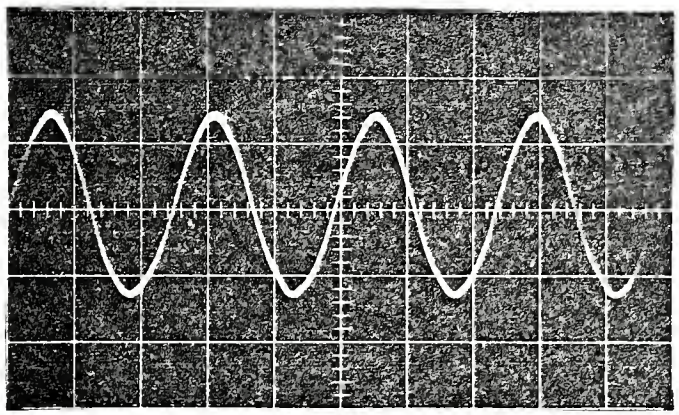


Fig. 25. 400 Hz sine wave receive filter output, 1 msec per horizontal division, 2 V per vertical

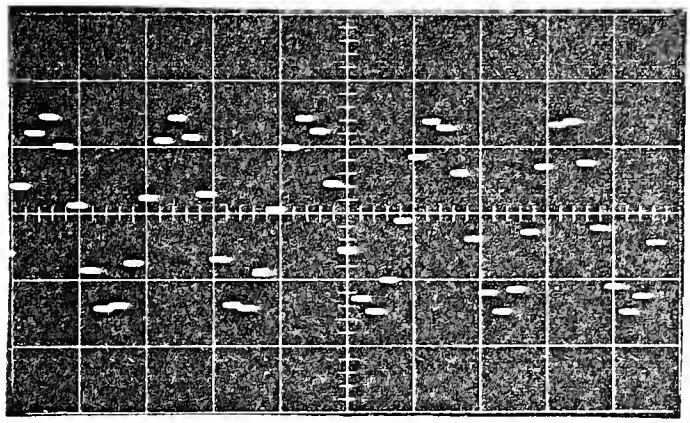


Fig. 26. 1 kHz sine wave decoder output, .5 msec per horizontal division, 1 V per vertical

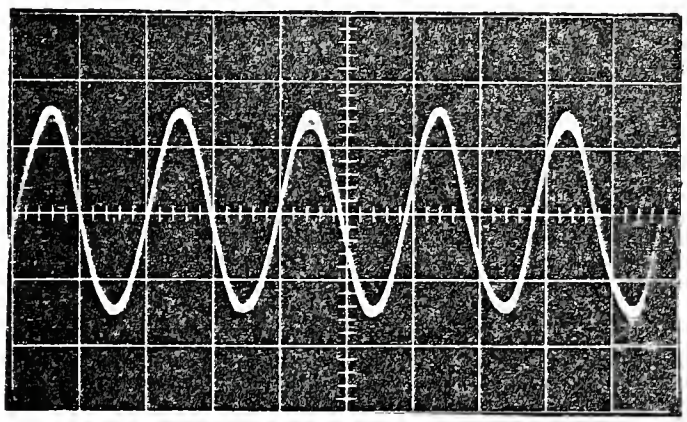


Fig. 27. 1 kHz sine wave receive filter output, .5 msec per horizontal division, 1 V per vertical

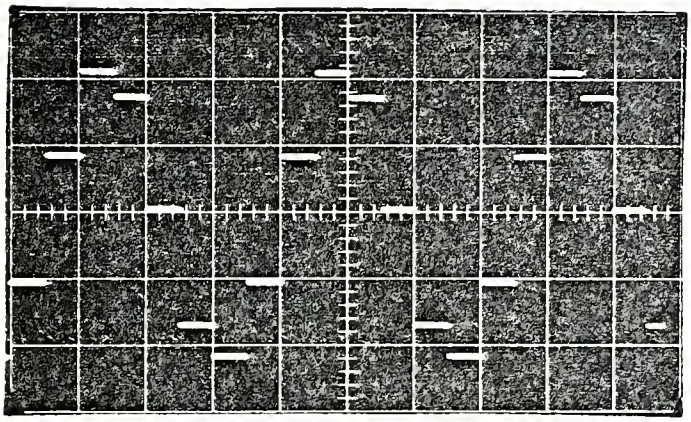


Fig. 28 1.5 kHz sine wave decoder output, .2 msec per horizontal division, .5 V per vertical

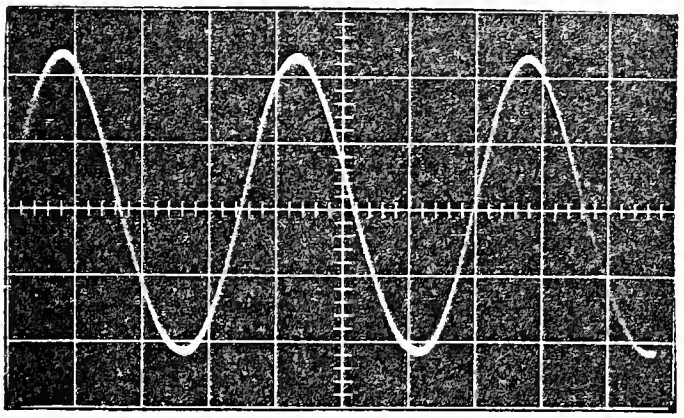


Fig. 29. 1.5 kHz sine wave receiver filter output, .2 msec per horizontal division, .5 V per vertical

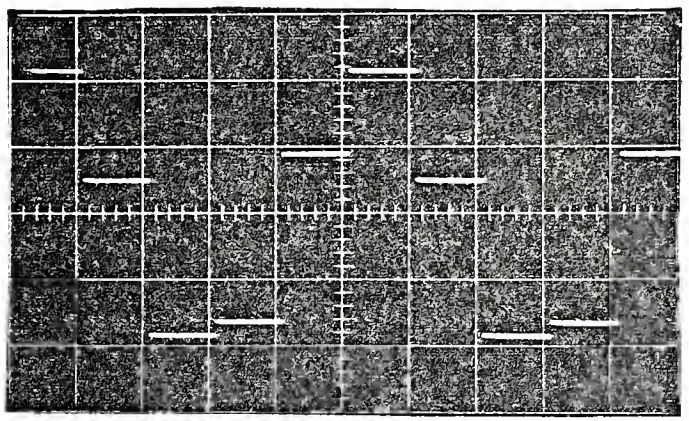


Fig. 30. 2 kHz sine wave decoder output, .1 msec per horizontal division, .5 V per vertical

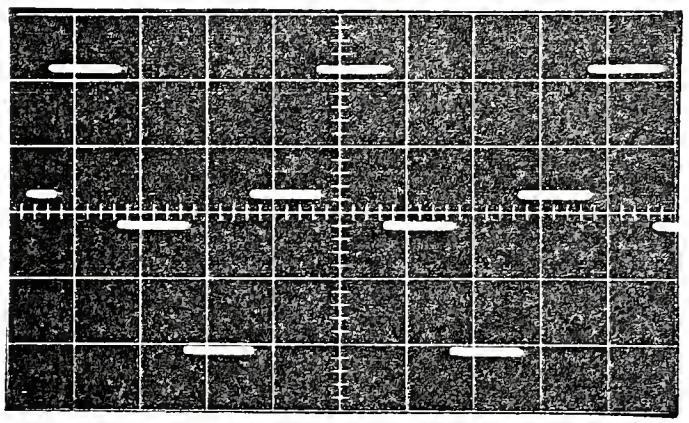


Fig. 31. 2.5 kHz sine wave decoder output, 1 msec per horizontal division, .5 V per vertical

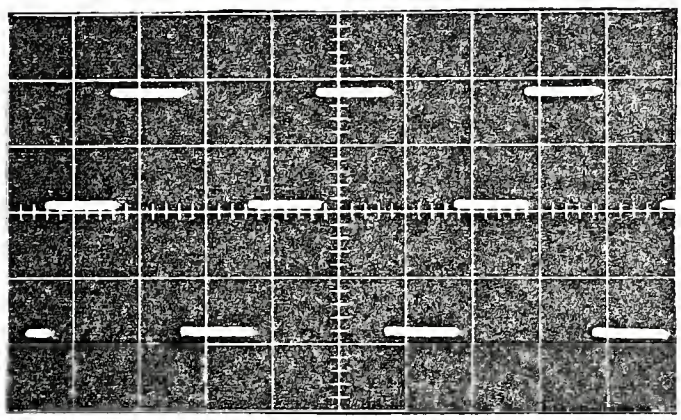


Fig. 32. 3.3 kHz sine wave decoder output, .1 msec per horizontal division, .5 V per vertical. Note the reduction of amplitude in relation with previous figures due to filtering.

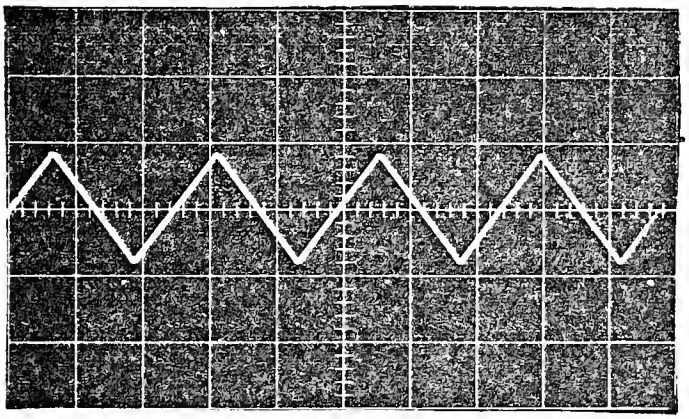


Fig. 33. 400 Hz Triangular wave input to the system, 1 msec per horizontal division, .2 V per vertical

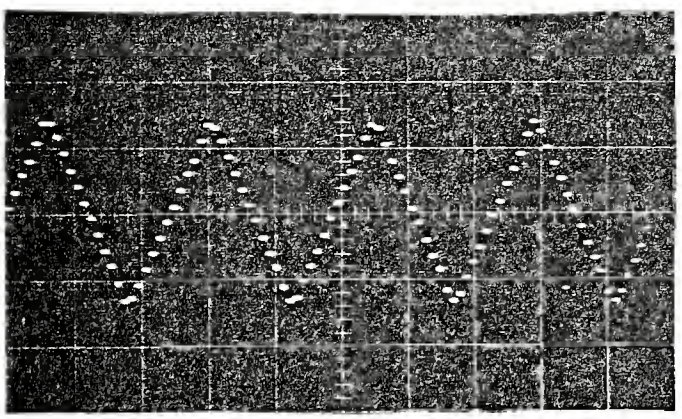


Fig. 34. 400 Hz Triangular wave decoder ouptut, 1 msec per horizontal division, 2 V per vertical

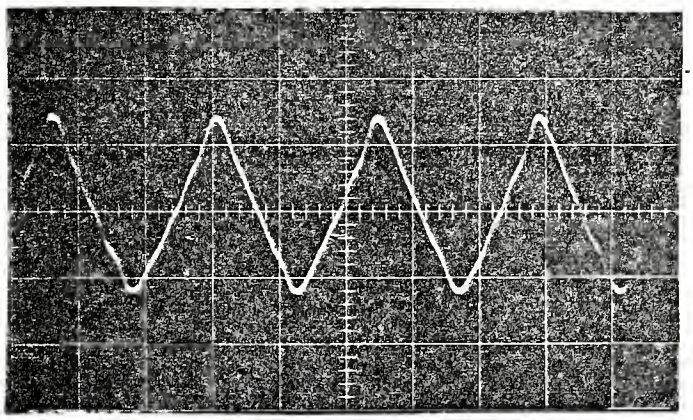


Fig. 35. 400 Hz Triangular wave receive filter output, 1 msec per horizontal division, 2V per vertical

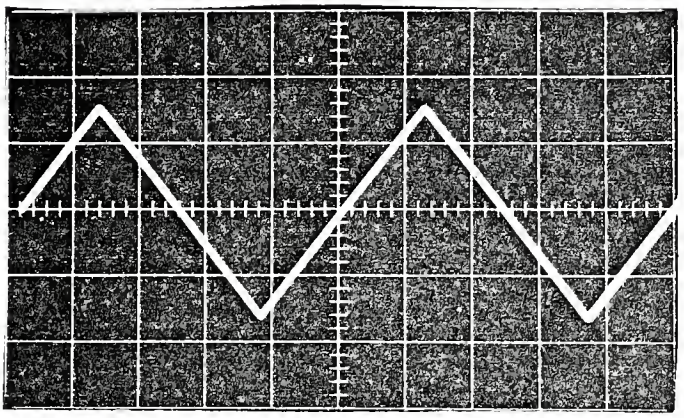


Fig. 36. 1 kHz triangular wave input to the system, .2 msec per horizontal division, .5 V per vertical

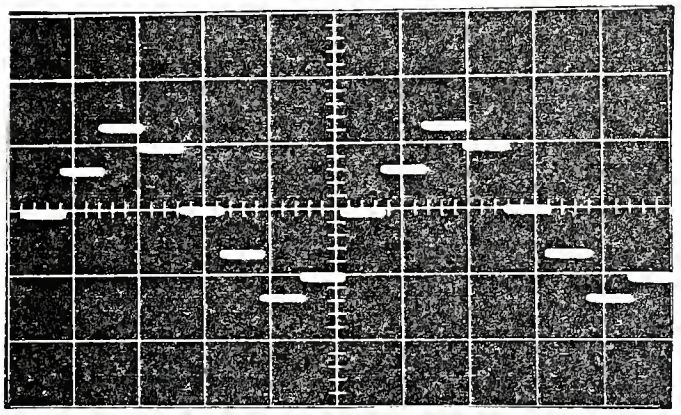


Fig. 37. 1 kHz triangular wave decoder output, .2 msec per horizontal division, .5 V per vertical. There are 8 samples per period since the sampling rate is 8000 samples per second and the period of this signal is 0.001 sec

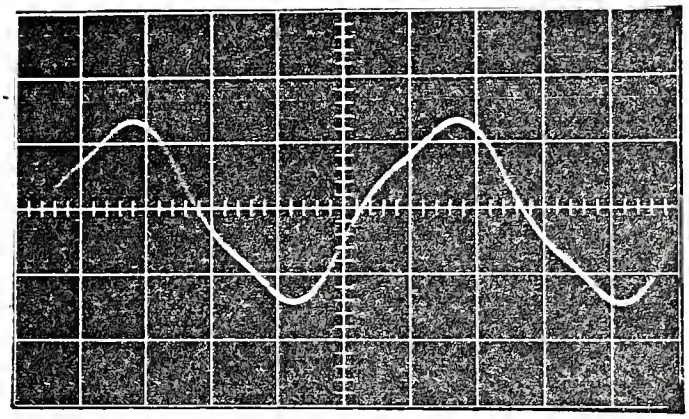


Fig. 38. 1 kHz triangular wave receive filter output, .2 msec per horizontal division, .5 V per vertical

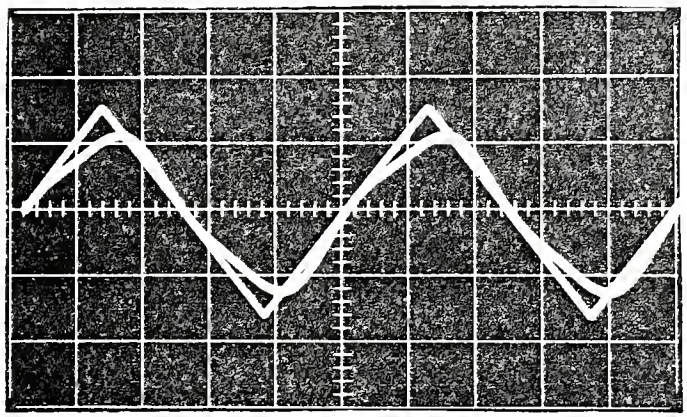


Fig. 39. 1 kHz triangular wave, comparison between input and output of the system with the gain set to 0. The distortion is due to the filtering prior to coding and not to the codec, 0.2 msec per horizontal division, 15 V per vertical

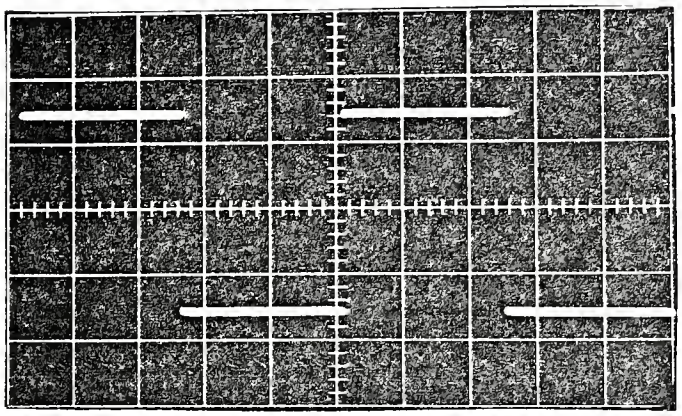


Fig. 40. 1 kHz square wave input to the system, .2 msec per horizontal division, .5 V per vertical

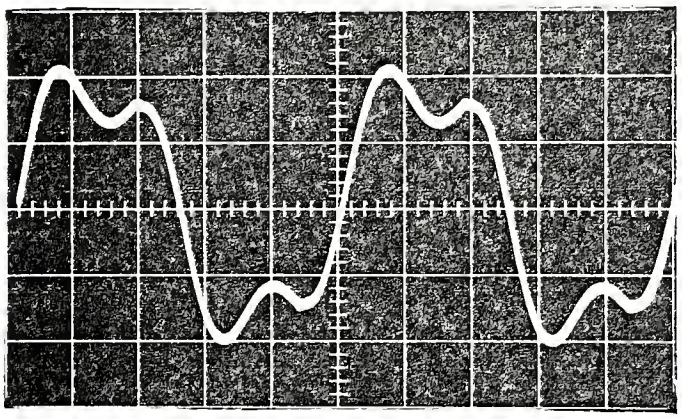


Fig. 41. 1 kHz square wave transmit filter output, .2 msec per horizontal division, .5 V per vertical. Note the distortion that the transmit low pass filter introduces.

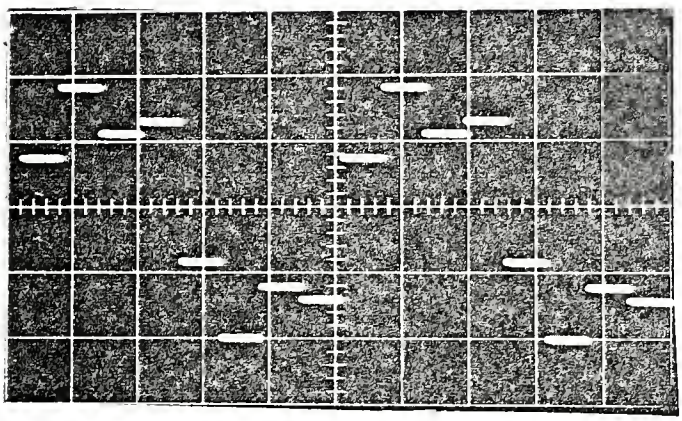


Fig. 42. 1 kHz square wave decoder output, .2 msec per horizontal division, .5 V per vertical

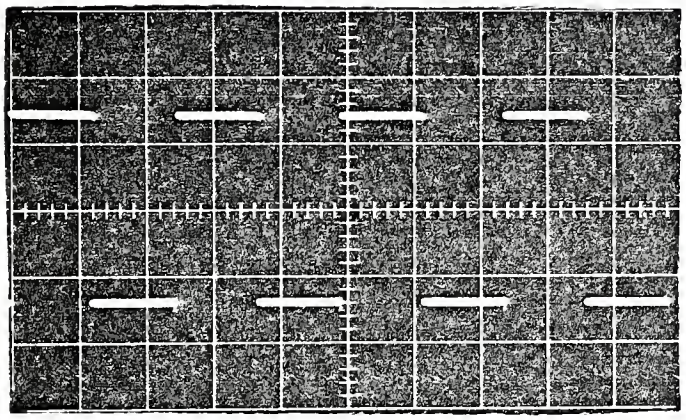


Fig. 43. 2 kHz square wave input to the system,
.2 msec per horizontal division,
.5 V per vertical

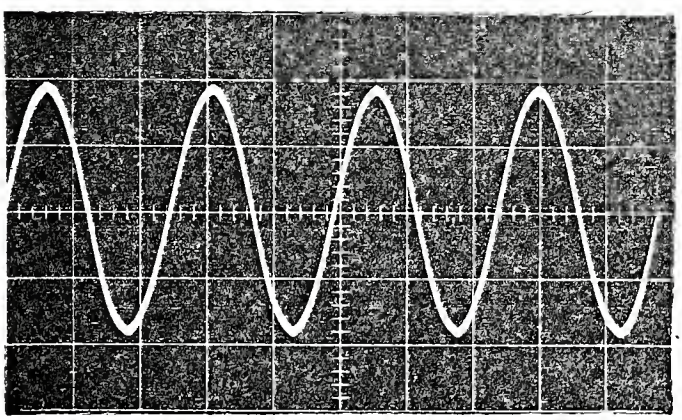


Fig. 44. 2 kHz square wave being distorted by
the transmit low pass filter,
.2 msec per horizontal division,
.5 V per vertical

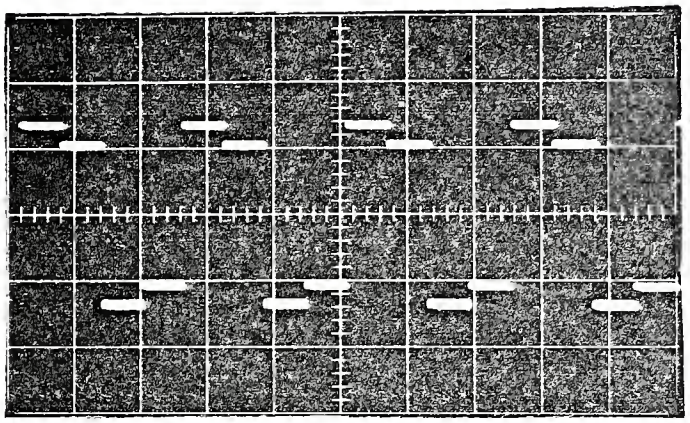


Fig. 45. 2 kHz square wave decoder output, .2 msec per horizontal division, .5 V per vertical

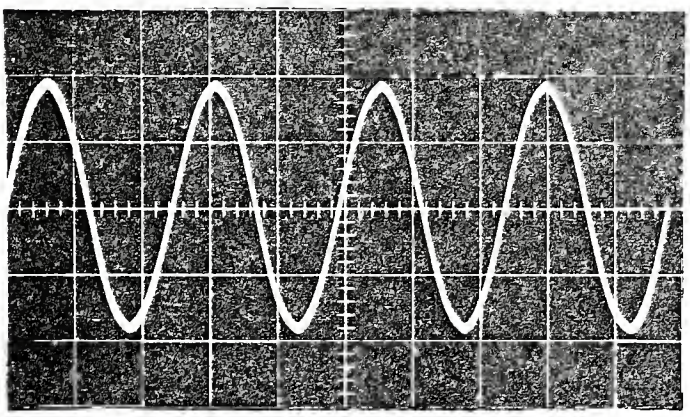


Fig. 46. The distorted 2 kHz square wave regenerated by the decoder and the receive filter, .2 msec per horizontal division, .5 V per vertical

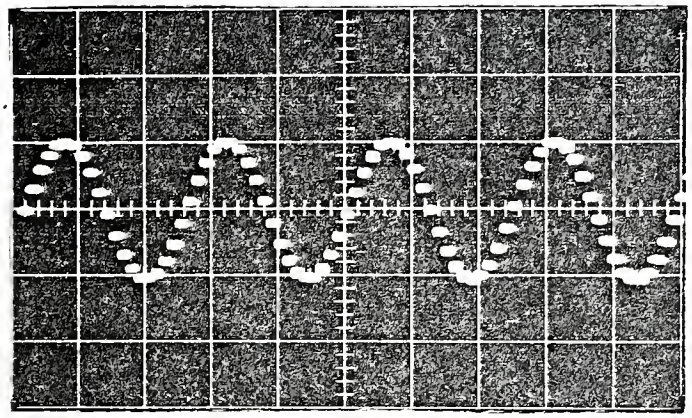


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

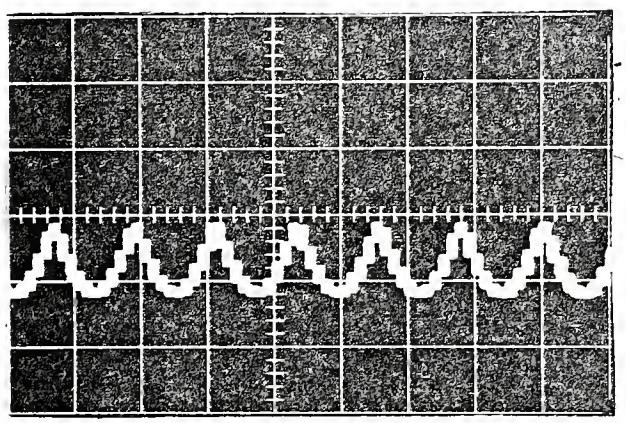


Fig. 48. Decoder output when the MSB (1st bit) of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

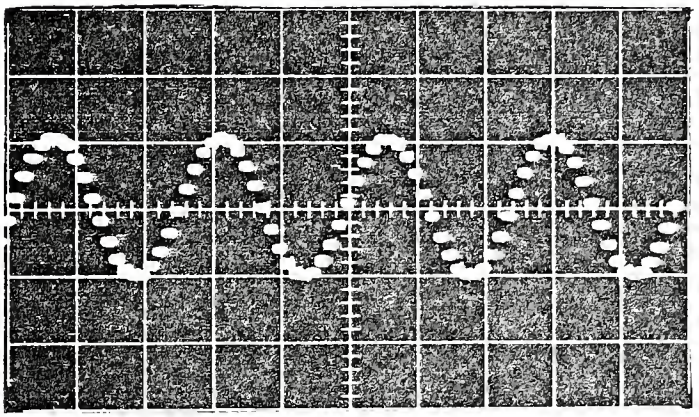


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

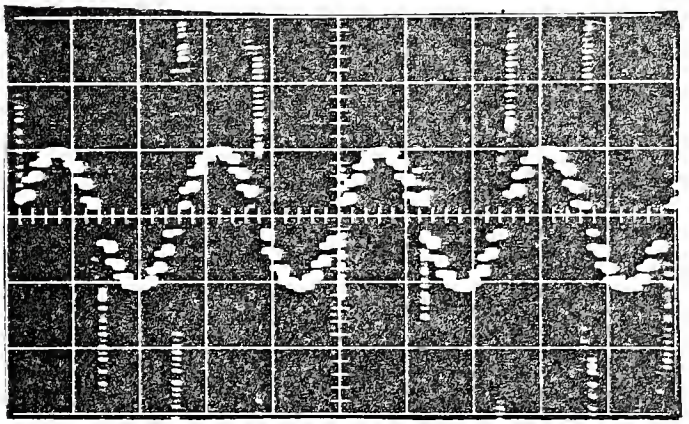


Fig. 49. Decoder output when the 2nd bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

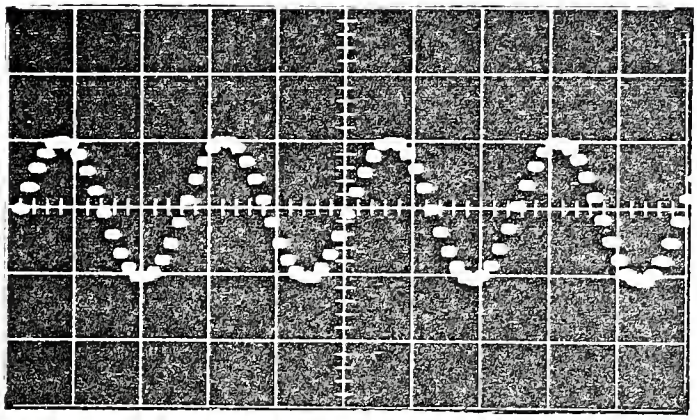


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

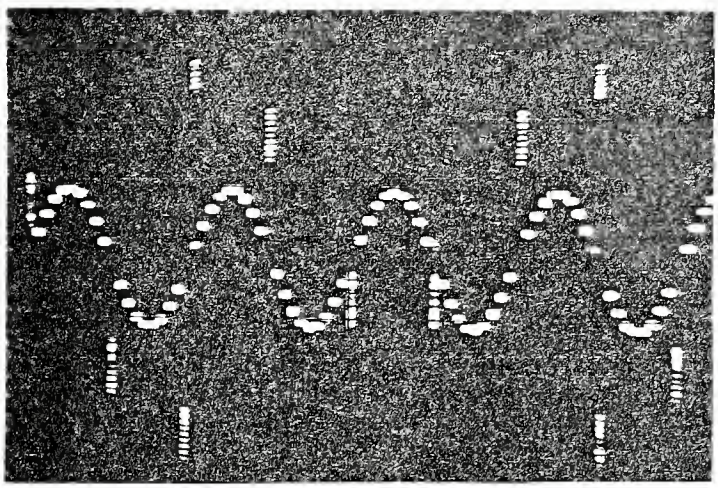


Fig. 49. Decoder output when the 2nd bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

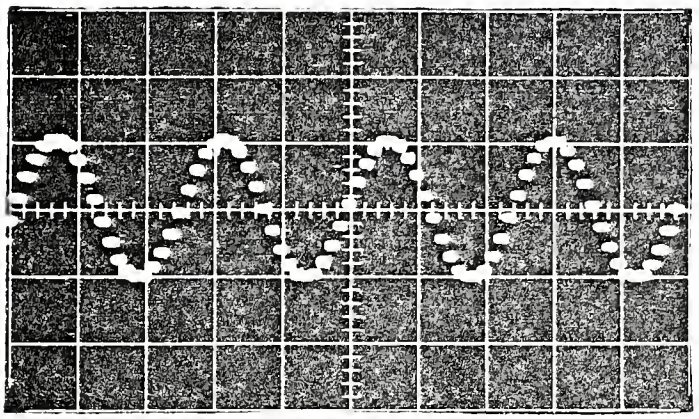


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

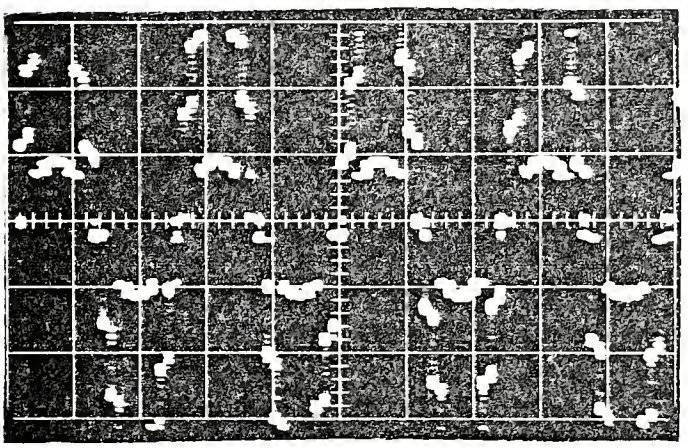


Fig. 50. Decoder output when the 3rd bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

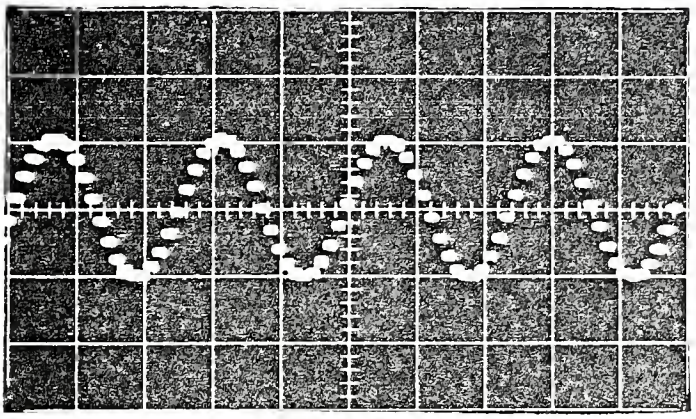


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

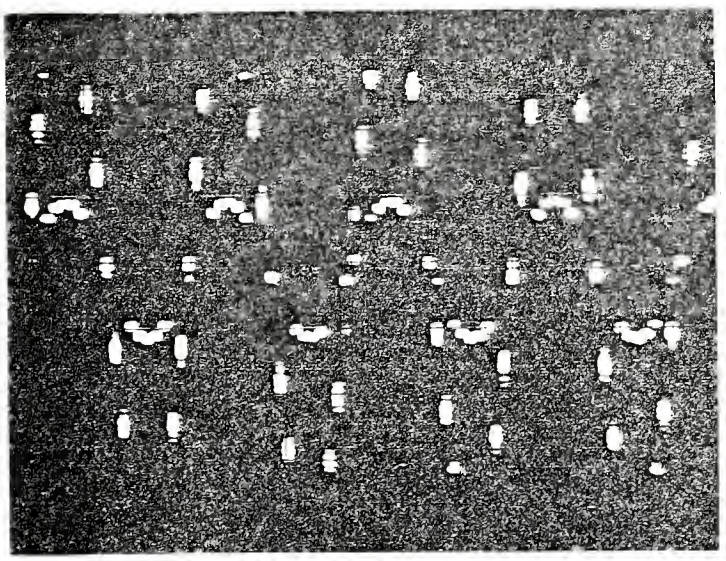


Fig. 50. Decoder output when the 3rd bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

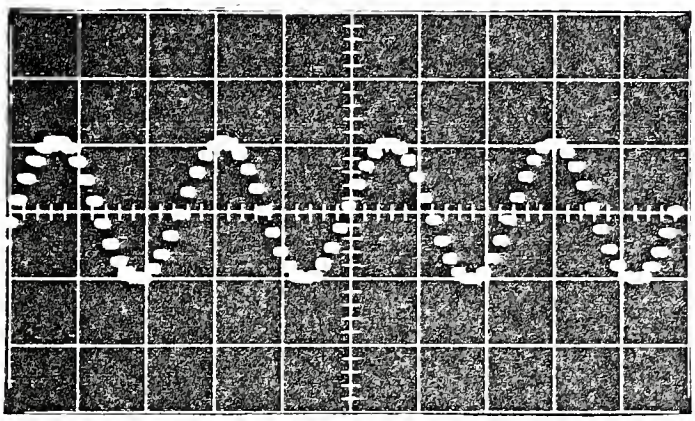


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

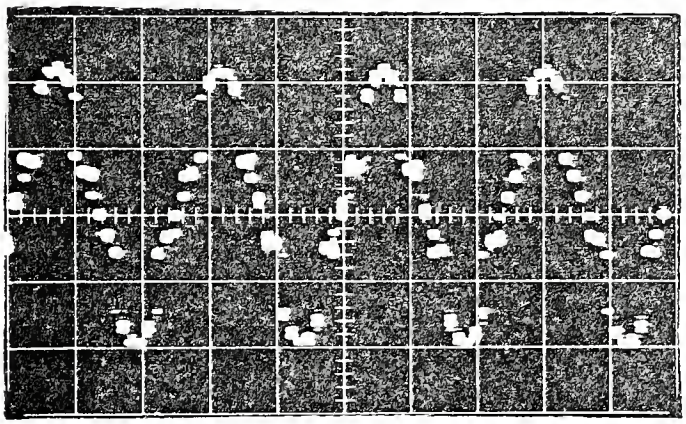


Fig. 51. Decoder output when the 4th bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

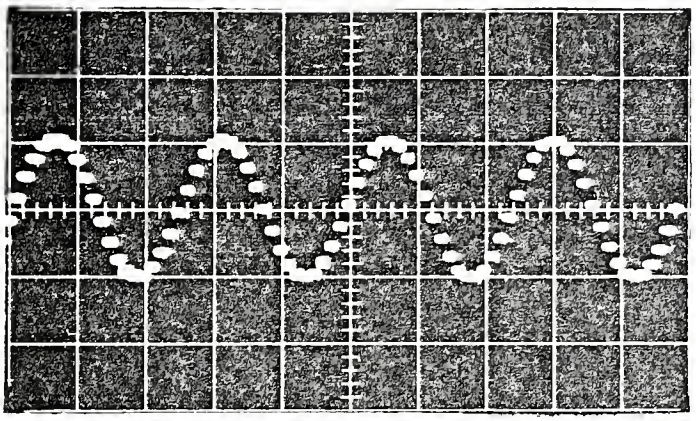


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

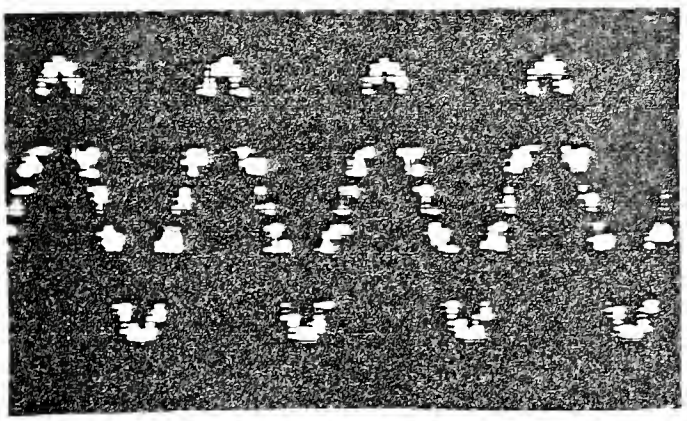


Fig. 51. Decoder output when the 4th bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

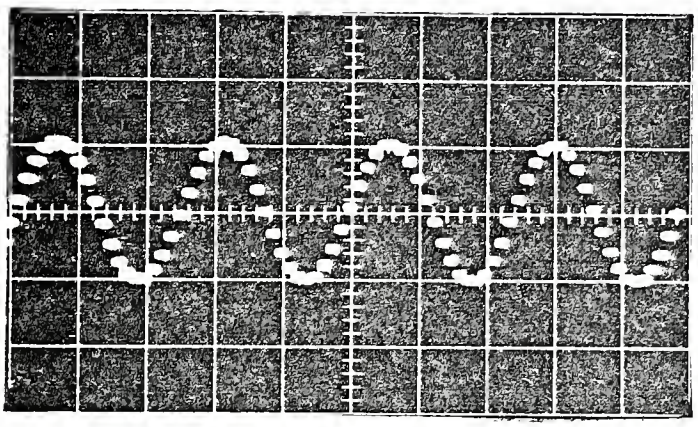


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

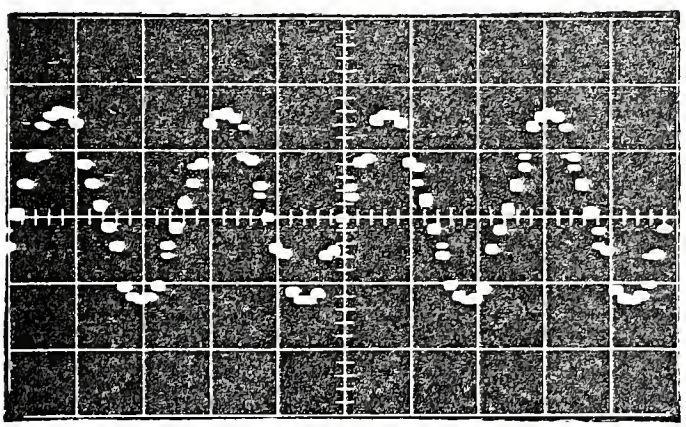


Fig. 52. Decoder output when the 5th bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

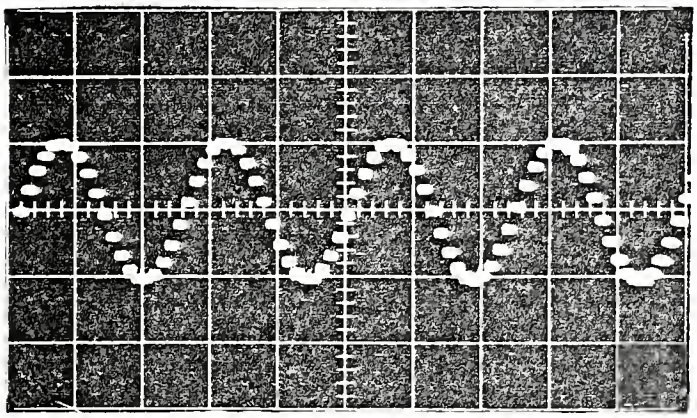


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

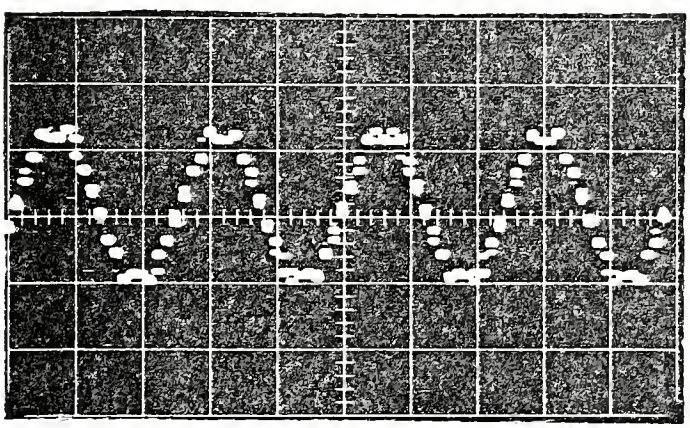


Fig. 53. Decoder output when the 6th bit of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

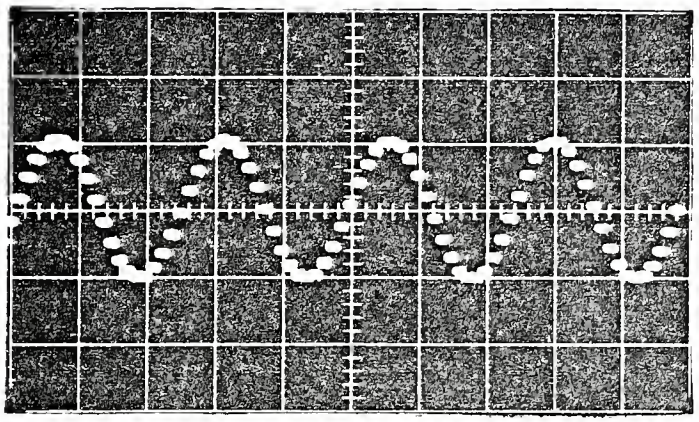


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

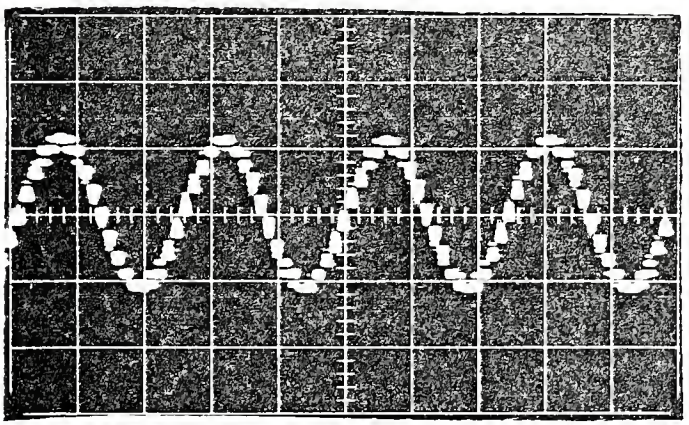


Fig. 54. Decoder output when the 7th bit of each 8 bit data word is lost in transmission of a coded 300 Hz sine wave. One volt per vertical division, .5 msec per horizontal

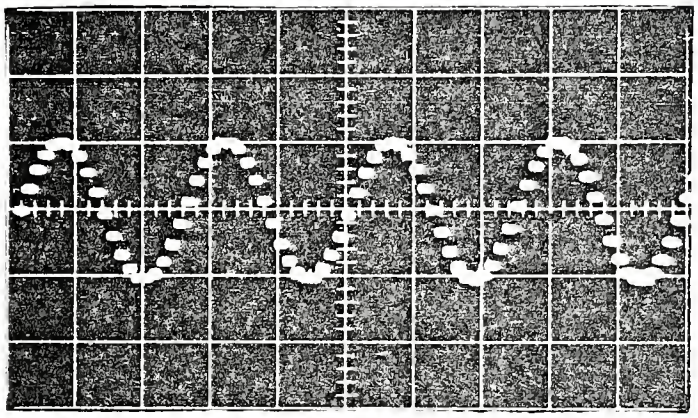


Fig. 47. Error free decoder output when a 800 Hz sine wave is used as input signal. One volt per vertical division, .5 msec per horizontal

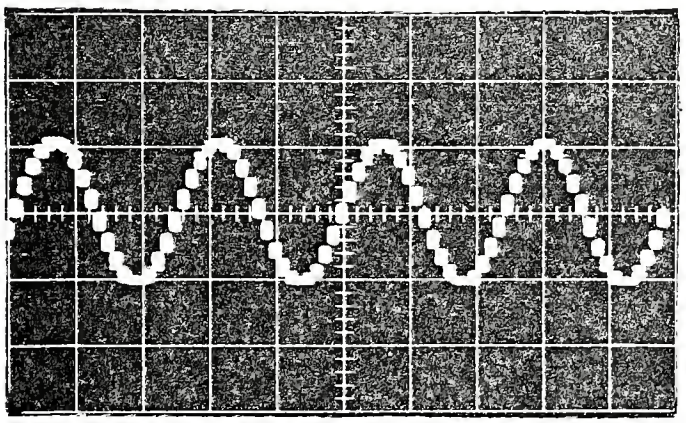


Fig. 55. Decoder output when the 8th bit (LSB) of each 8 bit data word is lost in transmission of a coded 800 Hz sine wave. One volt per vertical division, .5 msec per horizontal

VIII. APPLICATIONS

Codecs are primarily used in telephone channel banks. Actually today codecs are being shipped to telephone companies "by the thousands". However, it is believed that they will be used soon in other applications as well. These may include digital audio systems, telemetry, data acquisition, music, voice command systems, secure voice communications and the like.

It is claimed that the second major application for codecs in the near future will be in microprocessor-based voice command systems. In these systems encoded speech in binary format can be easily stored in a memory and used in a specified order to initiate certain processes. These processes may activate in turn proper transducers for a desirable output to be obtained.

As very large-scale integration (VLSI) technology grows and devices with unprecedented density and performance appear, it will not be a surprise to find a microprocessor and a codec residing on the same chip implementing such a voice command system.

IX. PROBLEMS, RECOMMENDATIONS AND CONCLUSIONS

In spite of the simplicity of the implemented system in this work the difficulties experienced were not few. First, the typical codec pin connections as shown in Fig. 10 and the interfacing between coder's digital output and decoder's digital input were not initially taken into account. This omission caused a significant delay in achieving correct operation of the coder-decoder pair.

It is recommended that before starting any experimental work involving codecs, the specifications given by the manufacturer should be thoroughly understood. If the specific codec pair DF331/DF332 manufactured by Sliconix, Inc., is used then Ref. 25 is a very good complementary information source.

Second, the sync pulse duration (8 fast clock pulses) was set originally by a monostable integrated circuit using an external resistor and capacitor. This circuit caused the sync pulse duration to vary between 7 and 9 fast clock pulses according to the resistance and capacitance variations. Until the three-bit counter shown in Fig. 12 was used, the coder-decoder pair did not operate.

Third, the operational amplifiers used to implement the original transmit lowpass filter caused an offset voltage to appear at the coder input. This voltage saturated the coder, and until an offset control method was found as

discussed in the input section, the coder would not function.

Fourth, the wide use of TTL circuits in this system introduced interfacing and noise problems. These problems caused noisy operation and erratic coding and decoding. In addition to noise generated by TTL circuits, power supply and ground-line noise was also present. The total noise that was measured at the decoder output originally was 250 mV.

Some of the above problems were solved by additional circuitry including noninverting buffers and smoothing capacitors, while other less critcal problems remain. The noise that was finally measured at the decoder output was less than 50 mV. For these types of problems, Ref. 3 and 4 provide information and are both recommended for future work.

Fifth, the use of TTL circuits in this system rather than MOS, imposed by speed requirements, resulted in use of a large number (9) of power supplies. Fewer power supplies could be used if zener diodes and resistors are used to implement proper voltage dividing circuits.

Whatever the problem and in spite of the "stress" that the codec pair experienced during this work, the chips survived and functioned very well.

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