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Development of the phase synchronization circuit for wirelessly distributed digital phased array

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THESIS

DEVELOPMENT OF THE PHASE SYNCHRONIZATION CIRCUIT FOR WIRELESSLY DISTRIBUTED DIGITAL PHASED ARRAY

by

Tsai, Yen-Chang

September 2009

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The Wirelessly Distributed Digital Phased Array (WDDPA) is an ongoing research program at the Naval Postgraduate School (NPS) which has numerous possible applications in radar and communication systems. The WDDPA incorporates many array elements randomly or nonuniformly in the environment or on a platform. Array elements are synchronized and controlled over a wireless channel. Compared to conventional phased array systems, its advantages are adaptability, survivability and flexibility.

Phase synchronization is a critical component of the WDDPA development. The common phase reference is vital to steer the beam and control the radiation pattern for the phased array system. The objective of this paper is to improve the WDDPA synchronization operation. Previous hardware and software architectures were replaced or modified to improve the accuracy and speed of the phase synchronization.

A series of experiments, first for hardwired channels, then for wireless channels, were conducted successfully to verify the synchronization operation for two elements. Several problems with the circuit were diagnosed and then addressed. The overall performance of the improved synchronization circuit for the demonstration array was satisfactory, allowing phases to be synchronized within 20° wirelessly. The architecture for the potential successor of the synchronization circuit is introduced. It is more flexible and robust than the current circuit and thus more desirable for future applications of the WDDPA.

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Phase synchronization is a critical component of the WDDPA development. The common phase reference is vital to steer the beam and control the radiation pattern for the phased array system. The objective of this paper is to improve the WDDPA synchronization operation. Previous hardware and software architectures were replaced or modified to improve the accuracy and speed of the phase synchronization.

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LIST OF ACRONYMS AND ABBREVIATIONS

ADC	analog-to-digital convertor
BAMP	baseband differential instrumentation amplifier
BMD	ballistic missile defense
BFN	beamforming network
CG(X)	capital multi-mission surface cruiser
COTS	commercial-off-the-shelf
cRIO	compact reconfigurable input/output
DAC	digital-to-analog convertor
DBF	digital beamforming
EWR	early warning radar
FOV	field of view
FPGA	floating point gate array
ICBM	intercontinental ballistic missile
IF	intermediate frequency
LNA	low noise amplifier
LO	local oscillator
LOS	line-of-sight
LPA	low power amplifier
NCW	network-centric warfare
NI	National Instruments
NPS	Naval Postgraduate School
PA	power amplifier
PCI	peripheral component interconnect

RRE	radar range equation
RX	receive
SNR	signal-to-noise ratio
TTL	transistor-transistor logic
TX	transmit
UAV	unmanned aerial vehicle
UV	unmanned vehicle
WDDPA	wirelessly distributed digital phased array
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	wireless local area network

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I. INTRODUCTION

A. BACKGROUND

The initial application of phased array antennas in military sensor systems can be traced back to the late 1930s [1]. Since the 1960s, electronically steered phased arrays, such as the well-known U.S. Navy AN/SPY–1 phased array radar shown in Figure 1, have been employed in some of the more demanding military combat systems [2]. Up to now, the phased array has been considered the mainstream antenna architecture of high performance sensor or communication systems, especially for radar [3]. It is applied widely in systems at sea, on land, in the air and even in outer space.

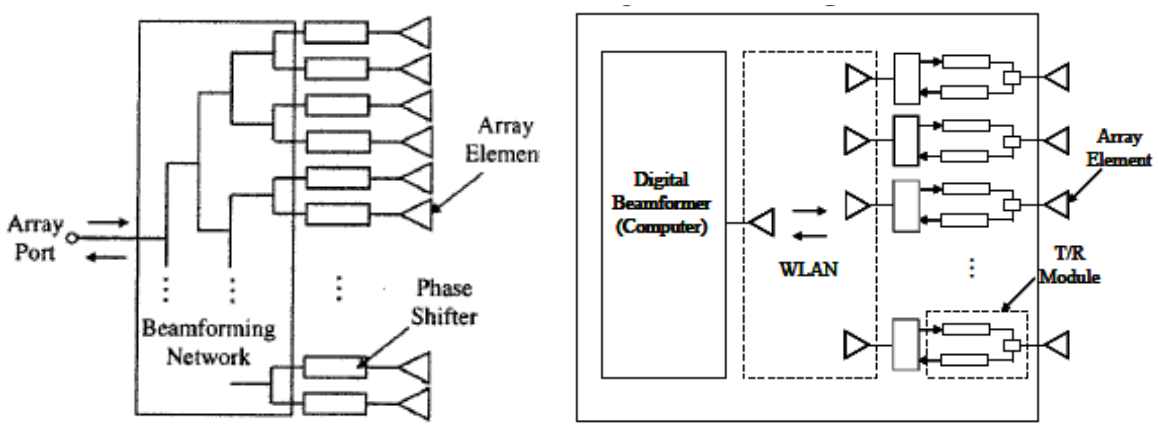
A phased array has numerous advantages over traditional antennas. The most prominent point in radar applications is that beam-steering is controlled electronically by applying phase shifters and switches instead of positioning the antenna mechanically. The prompt and precise beam switching for phased array radars yields versatile and superior capabilities, e.g., the ability to perform search and multiple target tracking simultaneously. This provides radar the flexibility and adaptability to conduct various functions for different missions and battle environments.

Figure 1. CG–54 with AN/SPY–1 radar highlighted (From [4])

Along with those advantages, the phased array has inherent disadvantages and limitations, such as cumbersome physical size, heavy weight and complicated beamforming network (BFN) architecture. A complicated hardwired beamforming system means high cost, high volume and weight, and low survivability. The large physical size usually results in low stealth, low flexibility and high maintenance requirements.

By riding on the superior advances of commercial wireless communication technology and computer processing capabilities of the past decade, it is now possible to minimize many of the disadvantages of phased array sensors. Additionally, the improvement becomes necessary and vital for success in the modern battlefield. The wirelessly distributed digital phased array (WDDPA) will be a potential system designed to integrate modern technologies to meet the needs of next-generation sensor or communication systems.

Figure 2 shows the simplified configurations of the BFN of a conventional phased array system and a WDDPA. Conventional phased array systems are composed of a great number of array elements, which might be dipoles or slots, and the individual element is usually controlled by its own phase shifter. The antenna port is connected to the individual array element by a network of transmission lines and power dividers, i.e., the BFN. On transmit (TX), the encoded baseband message or radar waveform is up-converted to the operating frequency then transmitted via the antenna after amplification. On receive (RX), the signal is received via the antenna, amplified, down-converted, and then the encoded message or radar waveform is recovered [5].



(a) Analog beamforming (b) WDDPA

Figure 2. (a) Analog BFN and (b) WDDPA(From [5])

For the WDDPA, each element has an individual T/R module that is a combined transmitter and receiver. Every T/R module is controlled by the digital beamformer via a wireless channel. As Figure 2 (b) shows, the need for the hardwired microwave circuitry of the analog BFN is eliminated in the WDDPA, improving the survivability of the overall system compared to a hardwired BFN. The other critical advantage that comes with the elimination of circuitry is that the system is capable of operating over a wider frequency band, increasing its versatility.

Another prominent feature of the WDDPA is that, because of the wireless architecture, the system array elements are able to be distributed randomly or nonuniformly in the environment or on platforms. This leads to a low-profile system with ultimate flexibility that can be integrated into the platform. WDDPA makes the whole system much less detectable to enemy sensors and its distributed nature makes it almost impossible to give WDDPA a single “deadly hit.”

The following two examples clearly illustrate WDDPA applications in the field. The first is the ship-based distributed array radar for ballistic missile defense and the second is distributed beam-forming by a swarm of unmanned vehicles.

1. Forward-deployed Ballistic Missile Defense and CG(X)

On April 5, 2009, North Korea launched a three-stage rocket carrying a claimed experimental communications satellite which flew over Japan and fell into the Pacific Ocean after traveling 3,230 kilometers [6]. The launch was believed to be a part of the testing of Taepodong–2 intercontinental ballistic missiles (ICBMs). It not only caused tension in Pacific Rim nations but also drew renewed worldwide attention to recent U.S. Ballistic Missile Defense System (BMDS) developments. The sea-based BMDS, also known as forward-deployed BMDS, is the key component of the U.S. integrated BMD, as shown in Figure 3. This is because it is extremely difficult to counter sea-based BMDS due to surface combatants' mobility at sea. The advance of sea-based BMDS can certainly add strength to the overall BMDS.

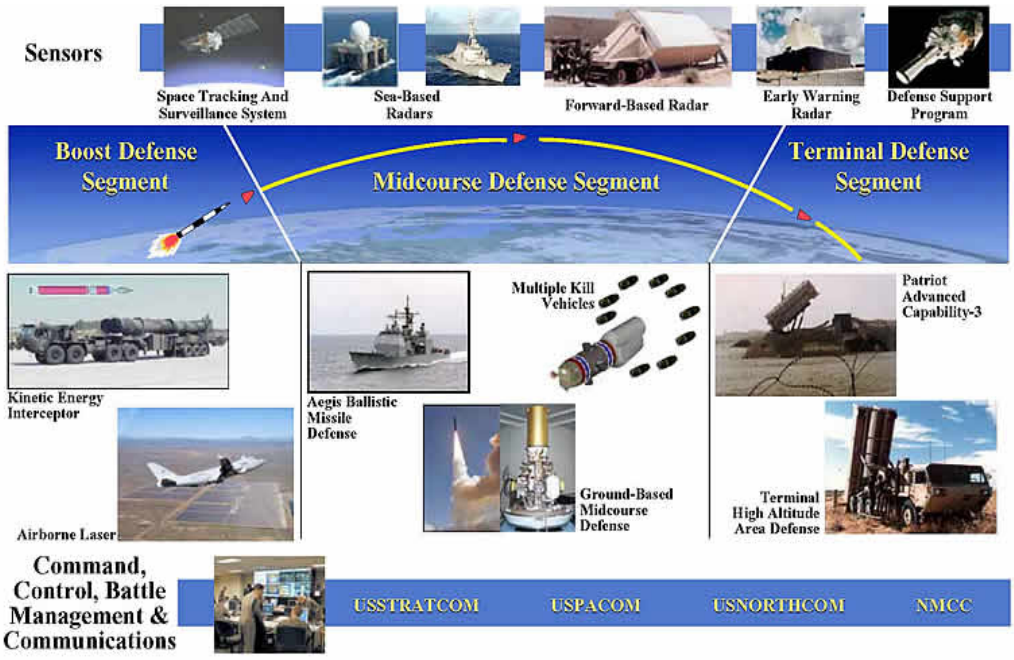


Figure 3. BMDS structure (From [7])

The sea-based BMDS now employs modified combat systems on several U.S. Navy Aegis cruisers and destroyers in order to provide needed but limited BMD capability in their remaining years of service. The proposed FY2010 defense budget requests a total of $1,859.5 million for the modification, which is approximately

$260 million for each implemented surface combatant [8]. Although generous budgets are spent, the modification *is not to* intercept ICBMs or ballistic missiles inside the atmosphere, during either their initial boost phase of flight or their final (terminal) phase of flight [9].

The U.S.'s future capital multi-mission surface cruiser, the CG(X), is designed to be provided with the initial operational capability to be a highly capable BMD platform. It is set for service in 2019 [10]. A descendant of the DDG–1000 originally expected to be commissioned in 2014 (Figure 4), CG(X) was supposed to adopt a similar hull design and newly developed concepts of combat systems. Recent discussions [10]–[12] showed that in order to carry out additional BMD missions other than DDG–1000, it will be necessary to accommodate the powerful advanced S-band radar in the CG(X). However, under the conventional phased array architecture and corresponding power requirements, this kind of BMD radar requires a much larger ship size: about 22,000 to 24,000 tons displacement compared to the 14,500 tons of a DDG–1000 [10]–[11].

Figure 4. Artist's concept of DDG– 1000 (From [13])

The price of the added BMD capability is an estimated $4 billion for each CG(X), much more than the $3 billion procurement cost of the controversial DDG–1000 [10]–

[11]. References [14] and [15] have investigated whether it is possible to equip the DDG–1000 with adequate early warning radar (EWR) operating at 300 MHz employing a WDDPA structure. EWR is a secondary radar operating in conjunction with the primary S-band radar.

The most prominent feature of this kind of EWR is a digital phased array radar with thousands of integrated ship-wide opportunistic array elements as shown in Figure 5. Elements are placed at available open areas over the entire ship's structure. Low-profile patch antennas can be integrated into the ship's structure, meeting the requirement of enhanced stealth. The cost associated with bulky ship size can also be reduced dramatically without sacrificing required BMD capability. The opportunistic array in the context of EWR can detect and track targets over 1000 km due to its high angular resolution capability, which is provided by a very narrow beamwidth (on the order of 0.005 radians) [14].

Implementing such array architecture on the CG(X) has the potential to fulfill the U.S. Navy's BMD mission at a relatively lower cost by performing exo-atmospheric surveillance, tracking and preliminary discrimination. This relieves the primary radar of the burden of BMD.

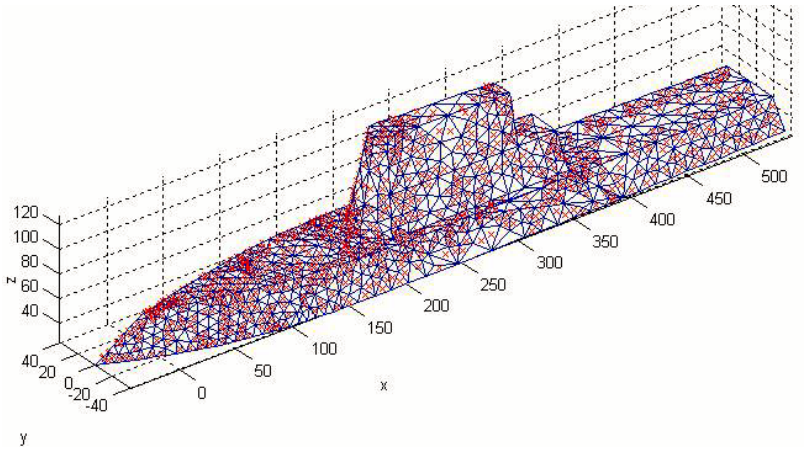


Figure 5. CAD model of DDG–1000 with 1200 distributed arrays (From [14])

2. Network-centric Warfare and Unmanned Vehicles

Network-centric warfare (NCW) is recognized as the cornerstone of military transformation occurring in the world today [16]. It has changed the military not only in operation's concepts, but also in weapon systems. Unmanned vehicles (UVs) implemented with WDDPA could be a great means to advance the spirit of NCW.

UVs, especially the unmanned aerial vehicles (UAVs), are widely used in the battlefield for surveillance and reconnaissance. During Operation Iraqi Freedom, 16 Predator and 1 Global Hawk (shown in Figure 6) were deployed in operation for thousands of hours [17]. They were all remotely controllable via satellite links from command centers in the continental United States, decreasing personnel casualties dramatically.

Figure 6. Predator and Global Hawk (From [18])

Most current UAVs, however, do not have high-resolution recognition or detection capabilities in the battlefield because they are large and must fly at relatively high altitudes, which degrades video resolution. The cost issue also prohibits widespread deployment [19].

With the combined concept of WDDPA and NCW, a distribution of numerous mini UAVs that are equipped with individual T/R elements could be an improvement over those limitations. Among the deployed mini UAVs, one is assigned to be the master UAV and the others are the slave UAVs. Via the wireless network, the master UAV is in charge of transmitting the acquired information to the control unit and synchronizing

slave UAVs in order to perform coherent operation. A robust and cost-effective sensor network like this is able to carry out the surveillance or intelligence mission in a hot zone (Figure 7).

One advantage is that the cost will be much lower than larger systems, such as the Global Hawk or Predator. For a MQ–1B Predator, the cost is approximately $10 million, whereas a mini UAV cost can be less than $1,000 [19]–[20]. Secondly, with WDDPA architecture, UAVs work with coherent operation and are able to fly at much lower altitudes, which can lead to higher resolution recognition capabilities. Lastly, countermeasures for this sensor network will be very difficult in practice, because of their small size. The WDDPA network is relatively insensitive to a small number of UAV losses, increasing its survivability.

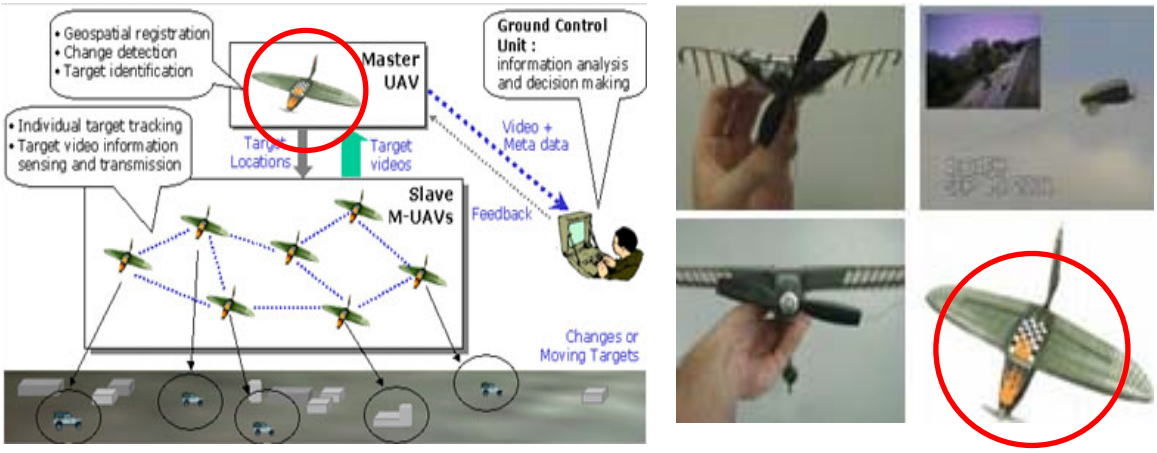


Figure 7. Configuration of wireless sensor network with mini UAVs highlighted (From [20])

B. WDDPA ARCHITECTURE AND SYNCHRONIZATION

The development and evolution of different aspects of WDDPA have been contributed by several Naval Postgraduate School (NPS) researchers. Several technological challenges still need to be solved in order to bring WDDPA into practice.

Phase and time synchronization are recognized as vital issues of WDDPA development. Efficient operation relies on the capability to synchronize numerous elements wirelessly in order to perform coherent processing.

Figure 8 shows that the architecture of a WDDPA system implemented on a ship's hull, illustrating the concept of phase synchronization. Thousands of T/R modules, considered a self-standing array element, are randomly distributed over the superstructure and hull. The system is composed of the central digital controller that communicates wirelessly with all the array elements. The central digital controller computes the beam-control data and radar waveform parameters and transmits them to the elements wirelessly. The local oscillator (LO) and synchronization signals are transmitted to the elements wirelessly [15].

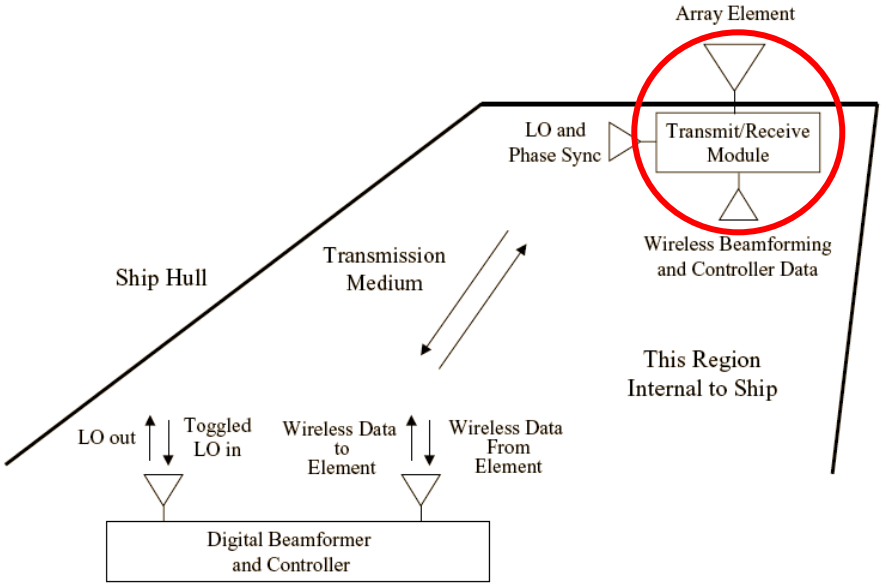


Figure 8. WDDPA system architecture implemented on a ship's hull with a single element highlighted (From [5])

One of the elements is assigned to be the master element, providing its phase information back to the central controller as the reference, while the others are slave elements. In normal conditions, the system is supposed to perform coherent processing of all elements. Periodically, in order to keep all the elements coherent, the central controller

needs to measure phase difference between the master and slave elements. It achieves this goal by executing a synchronization process. The controller sends out the synchronization signal (i.e., beacon) to each element in sequence to synchronize all the slave elements. An active phase synchronization technique is applied to compensate for element dynamic position and propagation channel changes.

Loke [15] first examined possible approaches to dynamically synchronize the elements to a common frequency and then proposed a “brute force” method that has a convenient and simple hardware setup. He also addressed the possible problem of synchronizing modules on a ship which has deforming surfaces and concluded that no correction is needed when operating in the VHF/UHF frequency bands, because the ship deformation is relatively smaller compared to the wavelength.

Grahn [21] applied Loke’s proposal of the “brute force” method to design and implement a synchronization circuit composed of commercial-off-the-shelf (COTS) microwave hardware into existing T/R modules. He then examined several configurations of synchronization circuits in wired and wireless structures, trying to validate the previous proposed concept of phase synchronization. Finally, he found a problem that caused unsatisfactory performance. He suggested that the power leakage caused by low isolation of the circulator or the power divider in the synchronization circuit was affecting the performance.

Djerf and Tornazakis [22] developed a LabVIEW control and processing program that handles all the functions within a floating point gate array (FPGA) structure. They also verified all the components in a two-element setup with integrated synchronization circuits. Furthermore, they designed several different synchronization circuits to investigate the problem reported by Grahn. In the end, they proposed that the simple synchronization circuit would not perform adequately with realistic devices because the peaks and nulls of the voltage waveform were always distorted and shifted, resulting in inaccurate phase compensation results. The inability to control signal levels to the LO ports of the modulators and demodulators was also a problem.

C. PROBLEM STATEMENT AND THESIS OBJECTIVE

Grahn, Djerf, and Tornazakis had met very similar problems in that the combined LO returned signal power level curves were distorted, which caused the *null* (minimum) of the waveform to be shifted and destroyed. Accordingly, the master was not able to provide an adequate reference to all the elements through the synchronization process. They have proposed some possible errors, such as LO leakage, leakage caused by low isolation of the circulator in the synchronization circuit, and poor performance of the low power amplifier (LPA).

The objective of this paper is to resolve the problem and verify the operation of the synchronization circuit. The same "brute force" synchronization algorithm is still applied for its unique advantage of convenience. Next, some parts of the hardware and software architectures are modified to improve the accuracy and speed of the phase synchronization. The FPGAs are no longer used in hardware and new components were investigated and applied to provide more processing capability and faster sampling speed. As for software, LabVIEW is still used but is modified substantially because of the change in hardware.

Furthermore, once the problem is resolved, the wireless synchronization process will be validated in order to carry on the development of WDDPA. Several different synchronization circuit configurations are implemented to examine the tradeoffs between proposed ideas. The power budget of the overall synchronization circuit is also discussed.

D. SCOPE AND ORGANIZATION

Chapter II discusses the architecture of the WDDPA system. The previous synchronization concept and wireless communication network requirements are summarized. Then, the present hardware components and software architectures are addressed. Finally, the revised two-element WDDPA configuration is introduced.

Chapter III examines and verifies the implementation of the new setup of synchronization circuits with the wired LO source. The comparisons between results of current and previous setups are discussed. A comprehensive analysis of the performance of the synchronization process is addressed.

Chapter IV investigates the synchronization process through the wireless network. The demonstration of transmission and reception between two T/R modules is completed and compared to Grahn's result. Several methods to improve the overall system performance are examined in a series of experiments. The analysis of wireless synchronization process is then presented.

Chapter V summarizes the work and offers suggestions for future research in WDDPA phase synchronization.

II. WDDPA ARCHITECTURE

A. DISTRIBUTED ARRAY CONCEPT AND OPERATION

The core concept of the WDDPA is to incorporate digital wireless beamforming architecture into the structure of a distributed phased array. Conventional phased array antennas are usually periodic arrays composed of multiple single-element antennas spatially distributed in two or three dimensions, based on a needed functionality. Compared to a conventional periodic array, a distributed array has several unique characteristics, and the conventional array formulas must be re-examined for the purpose of WDDPA development.

Basic array antenna and radar performance parameters have been presented in numerous textbooks (see, for example, [23]). The basic equations for array patterns, directivity and radar range equations are re-examined in order to clarify the overall WDDPA system performance.

1. Element Factor

The element factor is the normalized radiation pattern of individual elements in the array. Typically, the field of view (FOV) of a single element is wide and its directivity or gain should be relatively low. With the contribution of all array elements, the radiation pattern of a phased array can achieve very directive and high gain. However, when array elements are distributed in different environments from conventional setups, not every element can illuminate the target due to obstruction of platform superstructures or other environmental factors. Therefore, while the target is not in the FOV of an element, it does not contribute to the array pattern [3]. The element factor is expressed as:

$$EF_n = \begin{cases} \left|\hat{n}_n \bullet \hat{r}\right|, \ \hat{n}_n \bullet \hat{r} > 0 \\ 0, \text{ otherwise} \end{cases} \tag{1}$$

where

EF_n = element factor of the n^{th} element.

$\hat{n}_n$ = vector normal to the surface of the n^{th} element.

$\hat{r}$ = vector in observation direction

Equation (1) defines a general cosine type of pattern.

2. Array Factor

Array factor is the normalized radiation pattern of the array composed of multiple individual elements. The DDG–1000 model in Figure 9 is used to illustrate the spherical coordinate system reference. A general form for the three-dimensional array factor with elements located at (x_n, y_n, z_n), $n = 1, 2, 3, \ldots, N$ is [3], [14]

$$AF(\theta,\phi) = \sum_{n=1}^{N} A_n e^{+j\psi_n} e^{+j\psi_s} e^{+j\vec{k}\bullet\vec{r}_n} \tag{2}$$

where

$A_n e^{+j\psi_n}$ = complex coefficient of the n^{th} element that accounts for sidelobe control and corrections for all hardware nonidealities including synchronization

ψ_s = beam scanning phase weights

$= -k\left[\left(\sin\theta_s \cos\phi_s\right)x_n + \left(\sin\theta_s \sin\phi_s\right)y_n + \left(\cos\theta_s\right)z_n\right]$

(θ_s, ϕ_s) = scan angle as defined by the coordinate system in Figure 9

$\vec{k}$ $= k\left(\hat{x}\sin\theta\cos\phi + \hat{y}\sin\theta\sin\phi + \hat{z}\cos\theta\right)$

k $= \dfrac{2\pi}{\lambda}$

λ = the wavelength

(x_n, y_n, z_n) = location of element n

$\vec{r}_n$ = position vector from the array origin to element n

$= \hat{x}x_n + \hat{y}y_n + \hat{z}z_n$

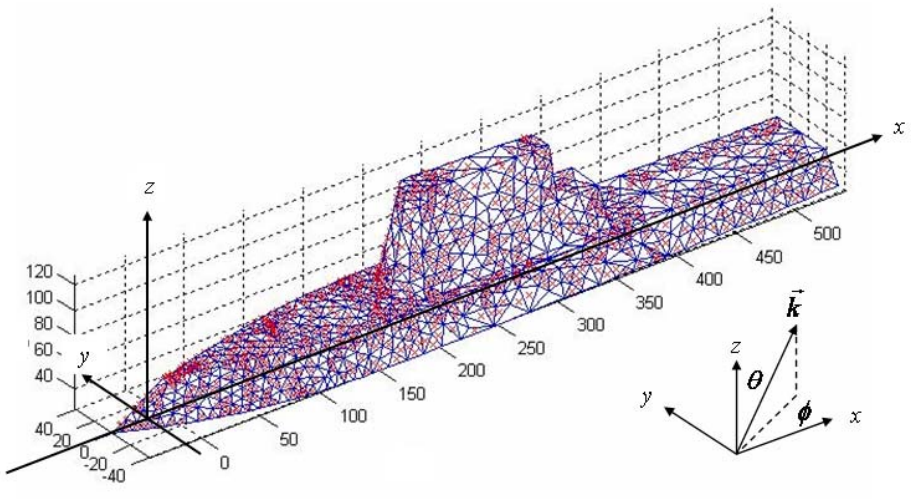


Figure 9. Spherical coordinate system referenced to DDG–1000 CAD model (From [3])

3. Total Array Pattern

The transmitting and receiving array pattern can be computed from the element locations and orientations. The pattern factor $F(\theta,\phi)$ is the product of element factor $EF_n(\theta,\phi)$ and array factor $AF(\theta,\phi)$, combining Equations (1) and (2) [3]:

$$F(\theta,\phi) = \sum_{n=1}^{N} A_n e^{+j\psi_n} e^{+j\psi_s} e^{+j\vec{k}\bullet\vec{r}_n} EF_n(\theta,\phi) \tag{3}$$

4. Directivity

Directivity is the maximum value of the directive gain. It is one important characteristic in the description of the antenna performance. The directive gain can be defined in terms of the normalized pattern factor $F_{\text{norm}}(\theta,\phi)$ [3]:

$$D(\theta,\phi)=\frac{4\pi}{\int_0^{2\pi}\int_0^{2\pi}\frac{\left|F(\theta,\phi)\right|^2}{\left|F_{\max}\right|^2}\sin\theta d\theta d\phi}=\frac{4\pi}{\int_0^{2\pi}\int_0^{2\pi}\left|F_{\text{norm}}(\theta,\phi)\right|^2\sin\theta d\theta d\phi} \tag{4}$$

Directivity is the maximum value of the directive gain without any loss occurring in the array. When loss occurs, the gain is equal to the directivity multiplied by the efficiency [3]:

$$G(\theta,\phi)=\eta D(\theta,\phi)=\frac{4\pi A_e}{\lambda^2}\left|F_{\text{norm}}(\theta,\phi)\right|^2 \tag{5}$$

where

η = the antenna efficiency, $0\le\eta\le1$

A_e = the array effective area

5. Radar Range Equation

Reference [3] customizes the radar range equation (RRE) for a distributed array to include the various phase shifts of the received power for wireless beamforming application. Figure 10 shows an arbitrary number of array elements distributed relatively close to each other compared to the range to the target.

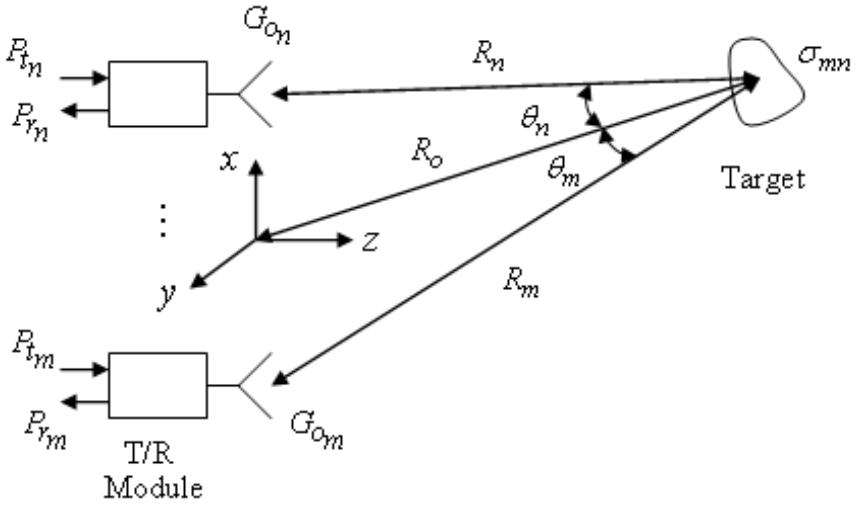


Figure 10. Distributed array operation configuration (From [3])

Therefore, the deviation of the aspect angles between individual elements is so small that it can be neglected, and the range from each element to the target is considered approximately the same. Additionally, in this model, all element characteristics are identical, which means equal transmit power, equal antenna effective area, and equal antenna gain. After substitution and reduction from the conventional RRE, and including phase shifts in the receive channels in the distributed array, the received power at element m yields:

$$\overline{P_{r_m}} = \frac{\overline{P_t} G_o^2 \sigma \lambda^2}{(4\pi)^3 R_o^4} \left| \sum_{n=1}^{N} (1) \right|^2 = \frac{\left(N \overline{P_t}\right)\left(N G_o\right) G_o \sigma \lambda^2}{(4\pi)^3 R_o^4} \tag{6}$$

where

$\overline{P_t}$ = the time-averaged power transmitted by each element = $\overline{P_{t_m}} = \overline{P_{t_n}}$

G_o = the antenna gain of each element = $G_{o_n} = G_{o_m}$

σ = radar cross section of the target

λ = wavelength

R_o = the path distance from the array origin (phase reference

= $R_n = R_m$

N = the total number of elements

In this simplified RRE, $\overline{P_{r_m}}$ is considered as the minimum detectable signal power at element *m*, hence R_o can be obtained if all the other variables are known. The derived formula clearly shows that for *N*-elements in a coherent distributed array system, the total transmit power is $N\overline{P_t}$ and the overall antenna gain is NG_o . The range R_o is in proportion to the square root of the number of element N , if other variables stay the same.

6. Signal-to-noise Ratio

Signal-to-noise ratio (SNR) is one of the vital measures for a radar system. It is obtained from the RRE, in which $\overline{P_{r_m}}$ is the power received by a single element *m*. The equation derived by the thermal noise power for an individual element in the array is $N_o = k_B T_S B$:

$$\left(\frac{S}{N_o}\right)_m = \frac{\overline{P_{r_m}}}{N_o} = \frac{G_{o_m}\lambda^2}{(4\pi)^3 k_B T_S B}\left|\sum_{n=1}^{N}\frac{\sqrt{\overline{P_{t_n}}G_{o_n}\sigma_{mn}}}{R_n R_m}\exp\{-j2kR_o\}\right|^2 \tag{7}$$

where

k_B = Boltzman's constant (operated with a matched input and load)

= 1.38×10^{-23} J/K

T_s = the system noise temperature (degrees Kelvin)

B = the system bandwidth (hertz)

If there are identical N elements in the distributed array system, using coherent integration yields signal amplitude multiplied by N. The associated power of coherent performance is proportional to N^2 [3]. The thermal noise in the system is considered as uncorrelated Gaussian white noise, which indicates that the total noise power in the array is additive. This also leads the total noise power to be N times the noise power in the single element. The array SNR is then improved by a factor of N:

$$\left(\frac{S}{N_O}\right)_{array} = N\left(\frac{S}{N_O}\right)_1 \tag{8}$$

B. WIRELESS BEAMFORMING CONCEPT

As previously stated, the core concept of WDDPA is to incorporate digital wireless beamforming into the architecture of a distributed phased array. The two major separate aspects here are the distributed array and wireless beamforming. Distributed

array related concepts and formulas were reviewed in the last section. This section reviews the concepts of wireless networking and digital beamforming (DBF).

1. Digital Beamforming

The general DBF architecture is shown in the Figure 11. In this architecture each element is composed of a transmitter and receiver. The transmitter consists of a baseband waveform generator, modulator and power amplifier (PA). The receiver is composed of a low noise amplifier (LNA), demodulator, and analog-to-digital convertor (ADC). On TX, the waveform is generated from the information provided by the central digital beamformer, and sent to the array element. The waveform is generated at each element and then transmitted simultaneously. On RX, the returned signal is received by the element, amplified, down-converted, sampled and passed to the computer.

Note that the phase reference is required to be distributed in the array system to ensure that all of the LO signals of the deployed elements perform coherent processing, i.e., phase synchronization.

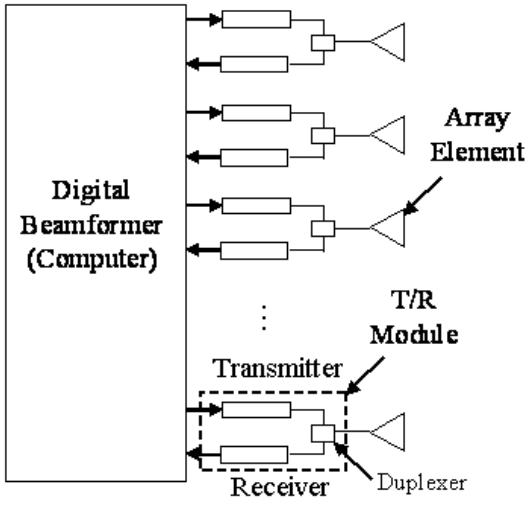


Figure 11. Generic DBF architecture (From [3])

Reference [3] implements the phase shift factor ψ_n into the element weight W_n for beamforming:

$$W_n = A_n \exp[-jk\left(x_n u_s + y_n v_s + z_n w_s\right) + j\psi_n] \tag{9}$$

and the corresponding array factor $F(\theta,\phi)$ becomes:

$$F(\theta,\phi) = \sum_{n=1}^{N} W_n \exp\left[\, jk\left(x_n u + y_n v + z_n w\right)\right] \tag{10}$$

where

W_n = $A_n e^{j\psi_n} e^{j\psi_s}$ = element weight for beamforming

(u,v,w) = direction cosines of the observation point

= $(\sin\theta\cos\phi,\ \sin\theta\sin\phi,\ \cos\theta)$

(u_s, v_s, w_s) = direction cosines for scan angle

= $(\sin\theta_s\cos\phi_s,\ \sin\theta_s\sin\phi_s,\ \cos\theta_s)$

In the beamforming process, the element weight W_n is sent to the modulator on TX. On RX the central controller applies the element weight to the received signal from the demodulator and then computes the array factor.

2. Wireless Network Requirement

Potentially thousands of elements can be implemented in the WDDPA system. The weight and complexity of routing data and transmission lines to all elements are difficult. Wireless communication is another critical technology for the BFN. Figure 2 (b) shows a WDDPA configuration where all the self-standing T/R modules are required to continuously communicate with the central controller wirelessly, including beamforming signals, synchronization signals, element phase weights, and digitized received signals. A distributed phased array employing wireless beamforming requires a very high data rate.

Reference [15] examined the wireless network requirements of the distributed array as shown in Table 1. On TX, a total of eight bits of data are required in the setup. They are composed of waveform control, synchronization, and phase weight data. The needed TX data rate is not challenging for modern commercial wireless hardware.

TX/RX	Wireless Data Description	Source	Data Rate	
TX	Waveform Control	Central Controller	2 b/s	8 b/s
	Synchronization	Central Controller	2 b/s	
	Phase Weights	Central Controller	4 b/s	
RX	Digitized Received Signal	Array Element	100 MS/s (sampling rate) 1.6 Gb/s	

Table 1. A summary of the wireless network requirement for WDDPA (After [15])

On RX, a high data rate is needed because the performance of the ADC affects the resolution of the received digitized signal [3]. The sampling rate of the ADC must meet the Nyquist condition, which is at least twice the intermediate frequency (IF) bandwidth (in a super heterodyne receiver) or twice the baseband frequency (in a homodyne system). The approximate data rate requirement is given by [24]:

$$R_b = N_c \times N_b \times R_s \tag{11}$$

where

R_b = data rate

N_c = data channels per array element

N_b = ADC bits of resolution

R_s = ADC sampling rate (samples per second)

Therefore, if a two-channel ADC is simultaneously sampled with 100 MS/s for each element and the resolution is eight bits, then for each element in the wireless

network, the required data rate is approximately $R_b = 2 \times 8 \times 100$ MS/s $= 1.6$ Gb/s. For an N-element full-scale array, the total required data rate is $1.6N$ Gb/s. Furthermore, if deformations of a platform or complex non line-of-sight (LOS) environments are taken into consideration, a much higher data rate is required.

Currently, the most commonly used wireless local area network (WLAN) is based on the IEEE 802.11 standard. Some of its variants, such as IEEE 802.11a (5 GHz) and IEEE 802.11g (2.4 GHz) standards, offer a peak data rate 54 Mb/s. Obviously, 54 Mb/s would not be sufficient for a full-scale developed WDDPA according to Equation (11).

With each generation of technology, wireless data rates have increased significantly [25]. For example, IEEE 802.16 is another series of wireless broadband standards that is hugely successful both in universal spread of users and commercial interests of IEEE 802.11 applied in WLANs. The IEEE 802.16e, adopted in the well-known broadband wireless access (WiMAX) technology, standardizes networking between various fixed access points and mobile devices. Originated in 2005, it provides data rates up to 70 Mb/s [26]. In late 2006, IEEE 802.16m was proposed by the IEEE 802.16 working group. In early 2009, it was reported that the new standard will push data rates up to 100 Mb/s for mobile application and 1 Gb/s for fixed application [25]–[27] in order to offer an advanced air interface to meet future cellular layer requirements. Stimulus from the commercial market during the fast advance of wireless communication technology will benefit WDDPA.

To handle the high data rate, hybrid optical and wireless configurations are also possible. Fiber optic links could be used for remote parts of the ship, with short-range wireless networks used for clusters of nearby elements. Currently, fiber optic links are capable of data rates greater than 40 Gb/s [28].

C. WDDPA DEMONSTRATION OVERVIEW

Up to now, the demonstration of the WDDPA has mainly been from the perspective of the ship-based distributed array radar. This is illustrated by the EWR implemented on the DDG–1000 (Figure 12). Several researchers [12]–[17] have

examined whether the EWR employing a WDDPA structure is capable of carrying out the mission of a secondary BMD radar. This section reviews the system as currently conceived.

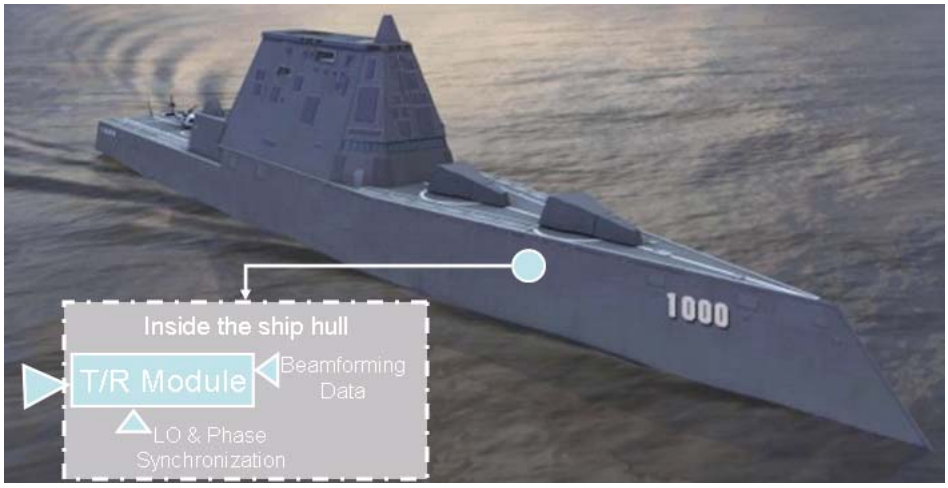


Figure 12. Configuration of WDDPA elements embedded in DDG–1000's hull (After [29])

The opportunistic array is assumed to operate at 300 MHz in the VHF/UHF band. In the context of EWR, it is expected to detect and track targets at ranges over 1000 km, which affects the number of elements implemented. The system's high angular resolution capability is provided by the narrow radar beamwidth. Tong [14] did extensive system simulations of radar performance. Validation of the critical concepts, such as synchronization, was required; therefore, a simplified system was built for the purpose of validation and verification. This was done at 2.4 GHz to take advantage of the COTS microwave hardware and other needed components. COTS hardware was also used for wireless communication devices and the central controller in the demonstration array.

Four major subsystems make up the WDDPA demonstration array as shown in Figure 13: (1) Central Controller, (2) T/R Module, (3) LO System, and (4) Wireless Communication Network. Each was developed and tested, and improvements were made based on the testing outcomes.

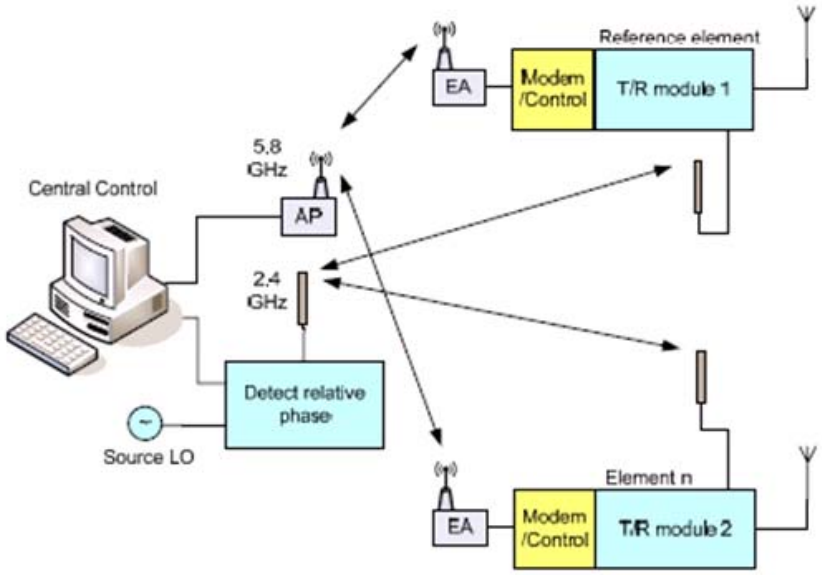


Figure 13. WDDPA demonstration array configuration (From [21])

1. Central Controller

The central controller acts as the “brain” of the overall WDDPA system, as shown in Figure 13. It is basically a computer installed with the required application software. LabVIEW 8.6, from National Instruments, was selected for the demonstration array. It controls data flow and synchronization, and also plays the role of a digital beamformer. For a full-scale WDDPA system, the central controller must be capable of generating the beamforming control data, as well as rapidly processing received digitized signal data for all the elements. Meanwhile, it must be able to monitor every element’s operation for the purpose of optimizing system performance.

For the small demonstration array, the basic needed function of the central controller is to offer the operator an interface to input control signals to the T/R modules and manage the data transfer between a small number of T/R modules (two elements in the present setup). One of the main tasks for the controller is performing the synchronization process. In order to maintain the coherence, the central controller has the

capability to detect the phase difference between two T/R modules. Then, the master element is assigned to provide its phase information as the reference for the slave elements.

2. T/R Module

In the WDDPA architecture, as shown in Figure 13, the system is composed of numerous self standing T/R modules, which are capable of transmitting the assigned signals, receiving returned signals, and communicating with the central controller wirelessly. Each T/R module integrates a local controller and a LO antenna, and is equipped with an antenna for TX and RX of the radar signal. A simplified T/R module is shown in Figure 14.

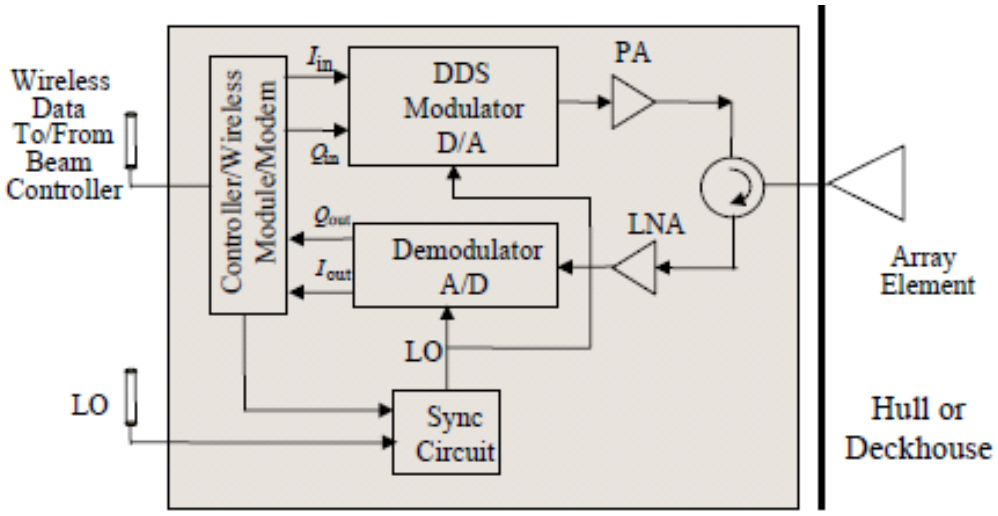


Figure 14. Simplified configuration of T/R module (From [23])

In the WDDPA development process, a functional demonstration T/R module using various COTS microwave components has been improved in several iterations. Improvements include the performance of the modulator and demodulator, the development of the synchronization circuit, and the control of power levels in the system. The present functionality and configuration of the T/R module is as follows:

The central controller sends the beamforming control information generated from the operator's inputs to each T/R module's local controller over a wireless network. The

Analog Devices AD 8346 modulator requires five inputs, which are the LO, and differential in-phase and quadrature-phase voltages (LO, IP, IN, QP and QN).

The quadrature-phase voltages from the baseband waveform are up-converted by the modulator board. After amplification, the needed waveform is transmitted. All the elements are required to perform in coherent operation, which means all the transmissions occur simultaneously.

On RX, the received echo signal is amplified by a LNA before the demodulator (Analog Devices AD 8347) mixes the LO and incoming signals. Then the demodulator produces four differential outputs i.e., IP, IN, QP and QN. A differential input instrumentation amplifier (more details in the Appendix) is applied in the most recent setup to convert four channels into two channels (I and Q). After sampling, the samples are sent back to the central controller via the wireless network. The signal processing and beamforming are executed by the central controller.

3. LO System

The LO concept shown in Figures 13 and 14 distributes a LO signal (2.4 GHz for the demonstration array) wirelessly to all elements in the system. Each implemented element is equipped with a dedicated LO antenna. The received LO from the master controller is used as the local oscillator signal, eliminating the requirement for a signal source at every element.

To optimize system performance, each element has to be synchronized to a common phase and time reference. The central controller executes the synchronization process. The phase of the distributed LO signal in the master element is assigned as a reference to all of the slave elements. The central controller calculates the phase differences between master and slave elements, and then compensates for the difference in the processing. Therefore, the system is synchronized and coherent operation is ensured.

Note that this approach also compensates for any phase difference in the LO transmission channel between the central controller and elements. The process must be

repeated often enough to maintain adequate synchronization, with the frequency determined by the stability of the equipment and propagation channels between the controller and elements.

4. Wireless Communication Network

The WDDPA concept is based on up to thousands of distributed elements implemented randomly or non-uniformly in the environment or on platforms. Therefore, a conventional wired data transfer system is not realistic. The wireless architecture makes the WDDPA feasible.

All the communications between the central controller and numerous elements are accomplished via a robust wireless network which functions as the “nerve” of the overall WDDPA system. In the wireless network, each element behaves as a node on the network. By taking advantage of modern commercial wireless communication technology, constructing an efficient and cost-effective demonstration array of the network is achievable.

In the present two-element configuration, the wireless network for communication between the central controller and elements is the IEEE 802.11a standard. The operation frequency is 5.8 GHz, as shown in Figure 13, in order to prevent possible interferences with the LO system (2.4 GHz). The wireless access point (WAP) is connected to the central controller. For each element in the WDDPA demonstration array structure, the local controller is connected to an antenna which acts as an access point to the central controller.

Noris [30] addresses the WDDPA wireless network challenges and possible solutions in more depth.

D. WDDPA SYNCHRONIZATION PROCESS

1. Synchronization Operation and Concept

The common phase reference is extremely crucial in order to steer the beam and control the radiation pattern simultaneously for any phased array system. A phased array system is composed of numerous elements, whereby the radiation pattern is determined by controlling the phase shifts of individual elements. The phase information is always relative to a common reference. The objective of this paper is to improve the WDDPA phase synchronization operation.

The "brute force" synchronization technique, a systematic phase adjustment of each element, was proposed and then applied in the WDDPA by Loke [15]. The major advantages of this technique are its simplicity and regularity.

Figure 15 demonstrates the simplified "brute force" phase synchronization process. The dashed block represents an element, and needed synchronization hardware components are incorporated in each element. The "brute force" synchronization is applied one element at a time. The first element to be synchronized (the slave) is chosen, and the central controller sends out the signal to execute the phase synchronization process. The selected slave element is then in the synchronization mode and the switch (circled) is positioned for the synchronization operation. The LO signal is passed through the synchronization circuit, which is composed of circulators, power dividers, a PA, and a phase shifter. Then the modified LO signal is sent back and compared to the signal of a specific master element reference at the central controller.

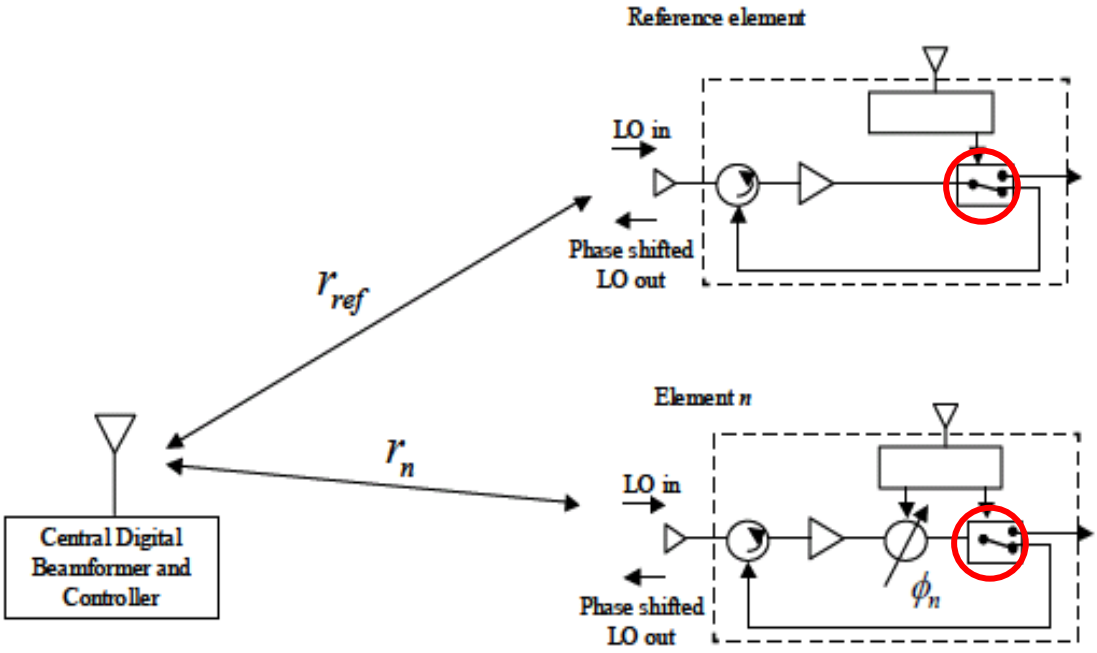


Figure 15. Simplified "brute force" schematic phase synchronization with the switch highlighted (From [23]).

The central controller runs a phase comparison algorithm, combining the master's reference signal and a returned LO signal from the slave. The process is repeated by stepping through 360 degrees of phase at the slave. The power sensor enables the central controller to display the graph of phase difference versus combined signal power level as shown in Figure 16. It is relatively easy to detect the minimum in comparison to the maximum.

Figure 16 clearly shows that the shape at higher power levels is quite flat, which makes it very difficult to define the maximum point. Therefore, using the minimum location of the resulting power level is preferable for synchronization purposes. Ideally, the minimum is supposed to be a very deep notch; however, because of the phase accuracy of the equipment and signal amplitude differences, the notch is shifted and filled. Figure 16 shows an acceptable approximate minimum location. Reference [23] states that if the phase difference of elements can be measured to an accuracy of 20 degrees in the synchronization process, it is sufficient for WDDPA operation.

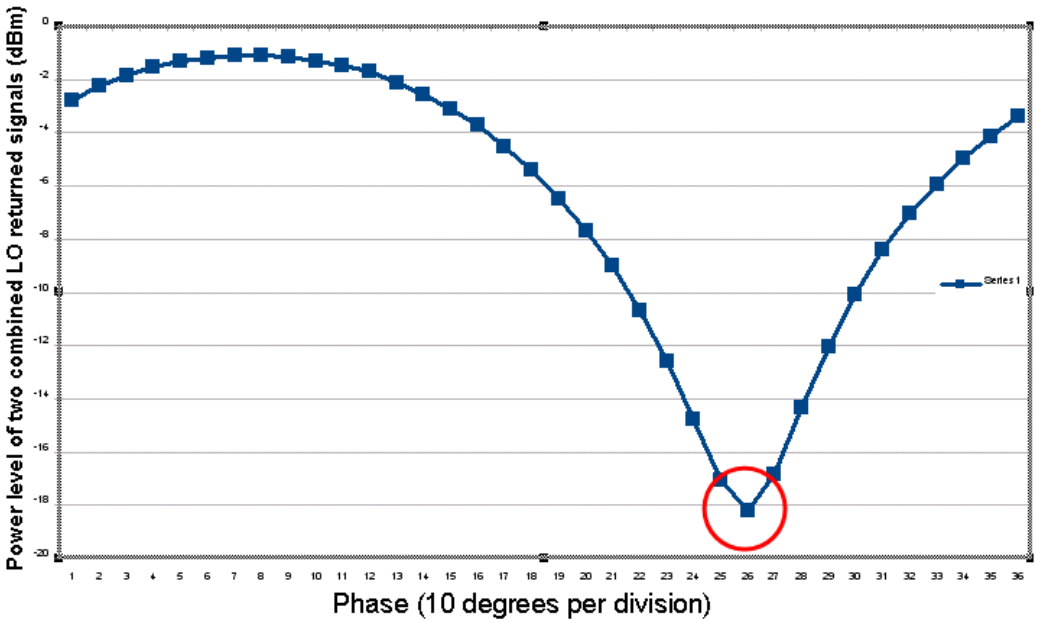


Figure 16. Illustration of the WDDPA phase comparison algorithm with the minimum highlighted

Every element's location has to be known by the central controller in order to compute the array factor. The phase difference caused by the elements' various location errors can be taken into consideration in the central controller for beamforming and control, i.e., Equation (10). For the demonstration WDDPA system, the LO signal needs to be distributed wirelessly as a beacon. The nature of the relative phases of the overall system inevitably will change due to the elements' dynamic positions and propagation channel changes. Hence, the phase synchronization process must be repeated periodically in order to maintain coherence.

2. Previous NI LabVIEW FPGA

Burgstaller [31] first adopted the National Instruments (NI) LabVIEW FPGA system as the host interface of the central controller in the WDDPA. The previous phase synchronization system is shown in Figure 17.

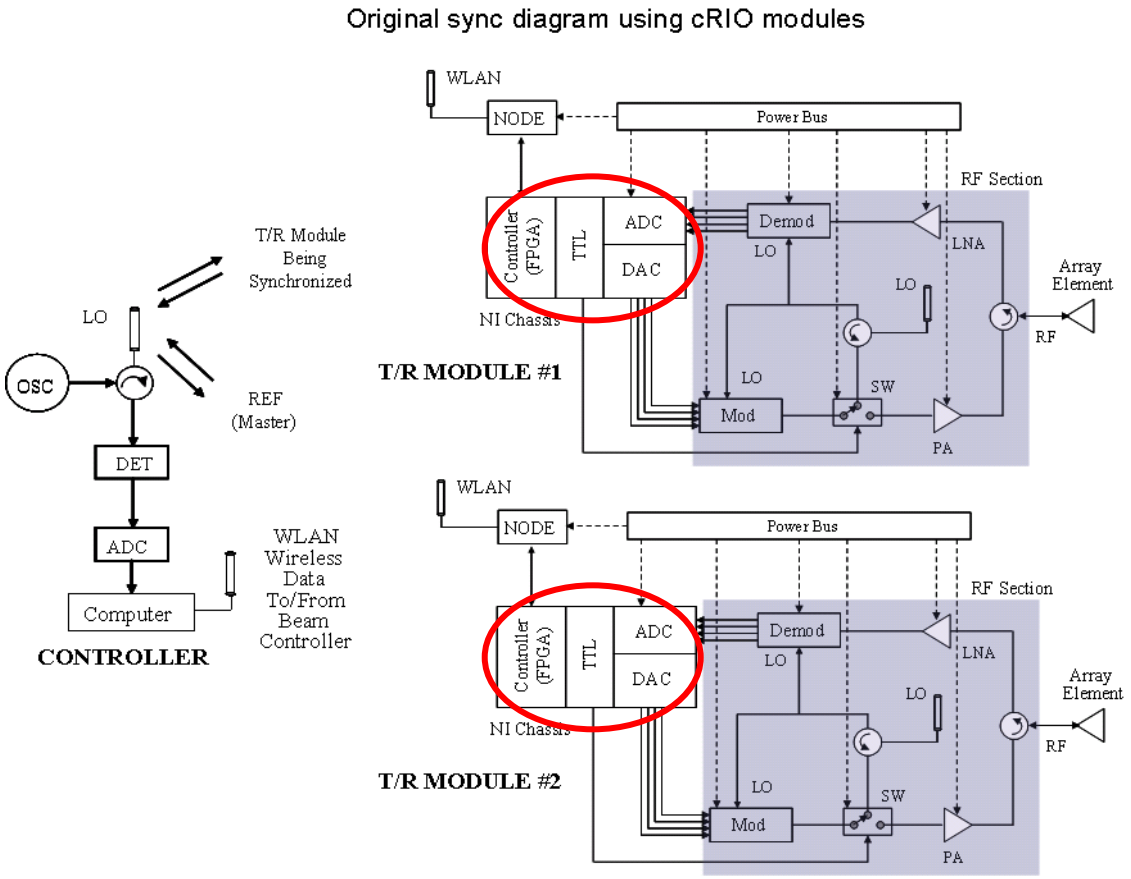


Figure 17. Original synchronization diagram for two modules with LabVIEW FPGA system highlighted (From [32])

Originally, the central controller was a Microsoft Windows personal computer (PC) with serial and parallel ports. These ports could not directly read RF or analog voltage levels [21]. An interface with the functionality of an ADC would be needed in the central controller. Also, for phase synchronization, each T/R module must incorporate hardware capable of switching between synchronization and normal modes; transistor-transistor logic (TTL) control switches needed to be connected to digital outputs for the T/R module. Hence, the LabVIEW FPGA system as shown in Figure 18 was designed for this purpose. The FPGA system contains two major parts: LabVIEW FPGA modules and the compact reconfigurable input/output (cRIO) hardware components. The LabVIEW FPGA modules extend the LabVIEW environment for virtual instruments (VIs) to be implemented as the software interface of the FPGAs on cRIO hardware. References [21]–[22], [31] have more detailed description of the previous LabVIEW FPGA system.

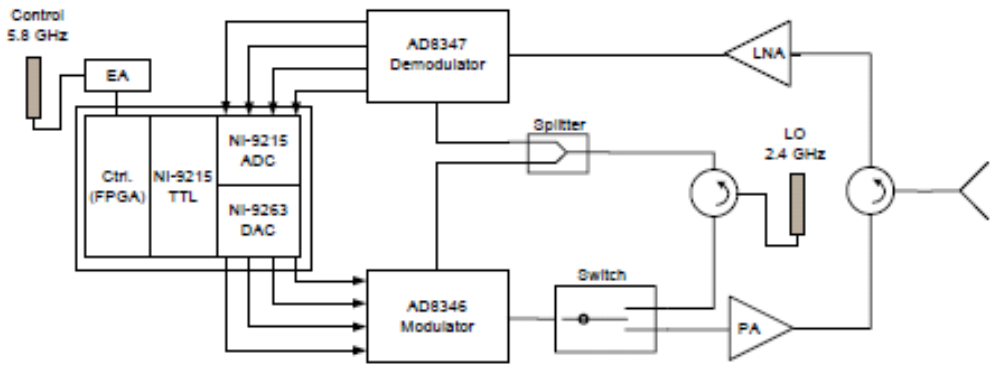


Figure 18. The detailed element module diagram of previously implemented LabVIEW FPGA system (From [21])

The implemented application software, NI LabVIEW, is used to control the incorporated LabVIEW FPGA system modules. It is a well-known, industry-leading software tool featuring graphical programming that is designed for test, measurement, and control applications [33]. The previous software interface of the demonstration array is illustrated in Figure 19, which shows NI LabVIEW installed on a PC-platform. It has specific VIs that are implemented to control all the FPGAs.

For the development of the related LabVIEW program, readers can find more in-depth details in [21]–[22], [31].

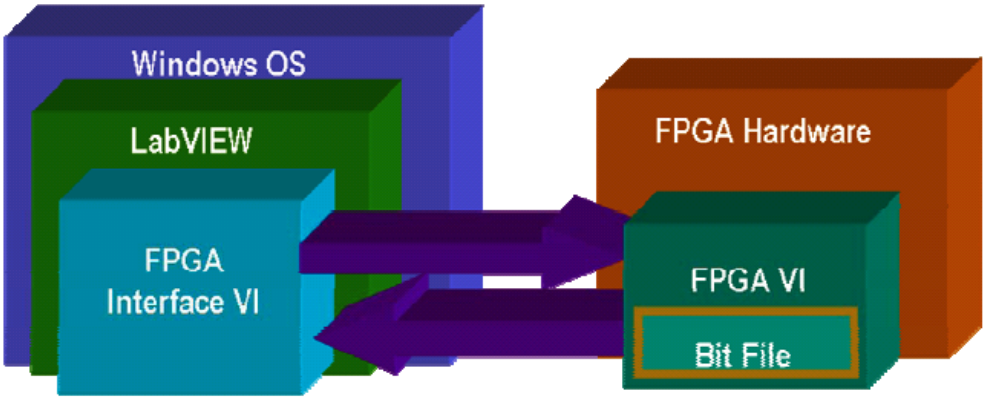


Figure 19. Schematic model of the LabVIEW software interface (From [31])

3. New Module Hardware

To resolve the hardware problems and verify the operation of the synchronization circuit, FPGAs and part of NI LabVIEW software architectures were replaced to improve the accuracy and speed of the phase synchronization. The demanding timing and synchronization requirements of instrumentation systems for the WDDPA demonstration array could not be met by the FPGA, cRIO analog output module, and cRIO Analog Input Module.

The NI peripheral component interconnect (PCI) extensions for instrumentation, called PXI for short, is the main apparatus adopted as the central controller for the demonstration array [32]. The software interface is modified as in Figure 20.

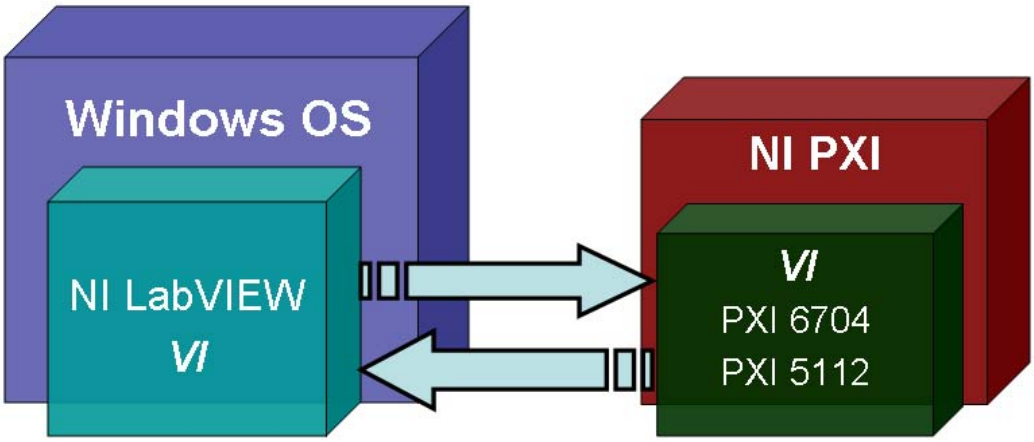


Figure 20. New schematic model of the LabVIEW software interface (After [31])

a. Implementation of Single PXI Controller

NI PXI is a PC-based platform that incorporates NI LabVIEW software and can accommodate both PXI and PXI Express modules. It is implemented as the successor of LabVIEW FPGAs and the original PC controller because of its high performance processing capabilities and hardware compatibilities. PXI is capable of operating mechanical, electrical, and software tests and measurements that define

complete systems [34]. The single PXI controller deployed in the new setup is composed of four parts as described in the following paragraphs.

- NI PXIe–1062Q 8–slot PXI Express Chassis

The PXIe–1062Q 8–slot chassis shown in Figure 21 is used to accommodate the PXI modules, which are deployed to control the T/R module and process the signals. Note that the PXIe–1062Q is the chassis, and it is required to house all other hardware. It includes the PXIe–8130 embedded controller, with the computer capability to act as the local controller. The other feature of PXIe–1062Q is the four PXI slots which allow PXI modules to be placed. It has a shared data rate of 132 MB/s. Each PXI slot provides connectivity to the 32–bit/33 MHz PCI bus on the backplane. For the two-element WDDPA demonstration array, the capability is sufficient to control two array modules at same time. [35].

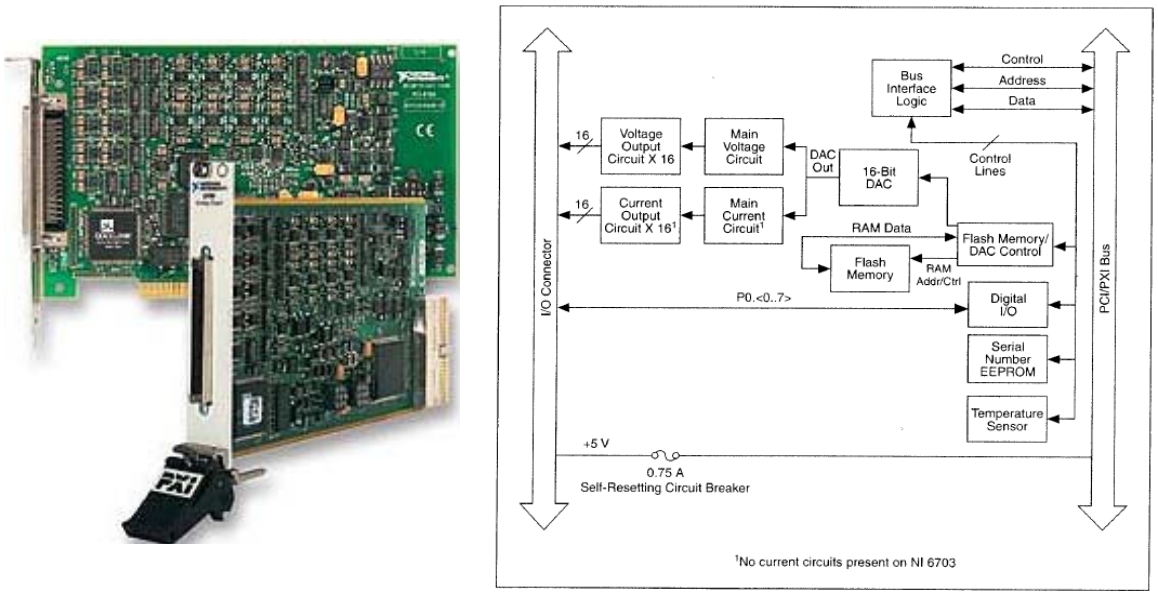
Figure 21. NI PXIe–1062Q 8–slot PXI Express Chassis (From [35])

- NI PXI–6704 Analog/Digital Output Module

The PXI–6704 shown in Figure 22 is a NI PXI module, acting as a digital-to-analog convertor (DAC) and digital output device for the PXI computer with 16–bit resolution. With PXI–6704, the central controller is able to control eight digital input/output (I/O) lines. For each T/R module, two digital I/O lines are needed to control

the switches with a TTL signal as shown in Figure 15. PXI–6704 also has 16 voltage output channels and 16 current channels for a total 32 analog output channels [36].

The modulator board, Analog Devices AD 8346, requires four inputs from a PXI–6704 (IP, IN, QP and QN) to generate and up-convert a baseband waveform. After receiving the inputs from the operator, the PXI–6704 sends the beamforming control information via four voltage output channels to the AD 8346 in each T/R module.



(a) PXI–6704 module (b) PXI–6704 function block diagram

Figure 22. NI PXI–6704 analog/digital output module (From [36])

- NI PXI–5112 100 MHz Digitized Oscilloscope

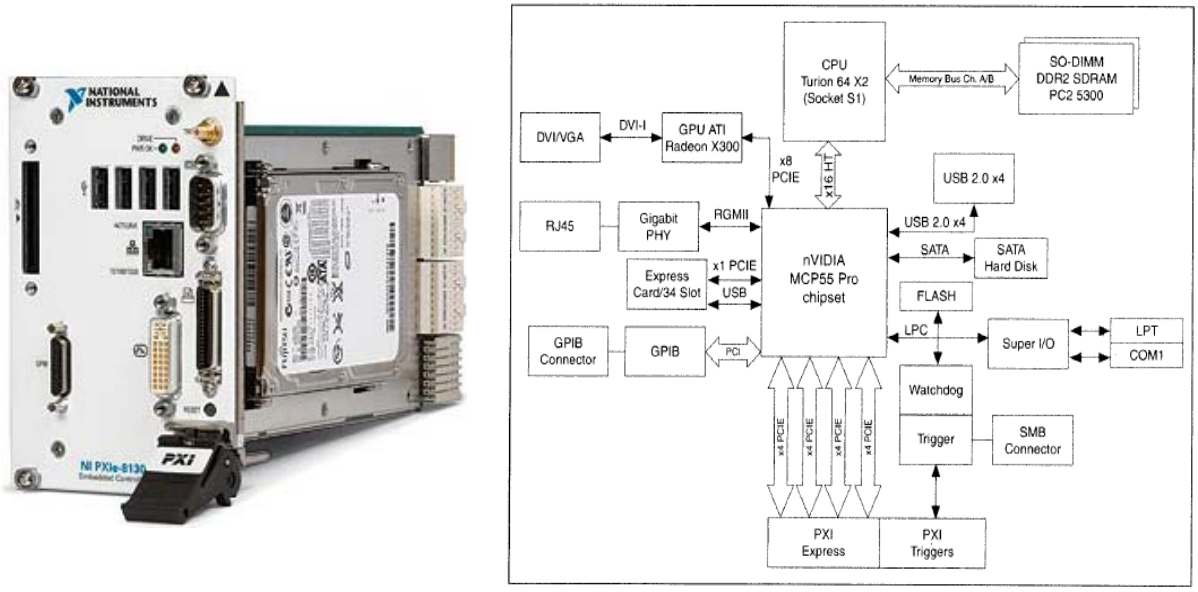
NI PXI–5112 digitized oscilloscope is based on the high-speed PCI bus. It is capable of storing a large amount of onboard acquisition memory, operating over a wide analog bandwidth, and handling a large analog input range. PXI–5112 processing capability is much faster than previous FPGAs instruments. It is selected to acquire and process large amounts of data from the T/R modules. The PXI–5112 specifications are summarized in Table 2 [37].

NI PXI–5112 Acquisition System Specifications	
Resolution	8 bits
3 dB Bandwidth	100 MHz max; 20 MHz typical with bandwidth limited enabled
Channels	2 simultaneously sampled, single ended
Maximum Sampling Rate	100 MS/s
Onboard Sample Memory	32 MB per channel
Calibrated Vertical Range	± 25 mV to ± 25 V in 10% steps
Operating Temperature	0° C to 40° C (Typical at 25° C)

Table 2. NI PXI–5112 Specifications (After [37])

- NI PXIe–8130 Embedded Controller

The PXIe–8130 shown in Figure 23 is an AMD Turion 64X2 processor-based embedded controller for use in the PXIe–1062Q 8–slot PXIe chassis. It is a high-performance and high-bandwidth controller device for modular instrumentation and data acquisition applications. It has an nVidia MCP55 Pro chipset that is connected to the AMD processor via an 800 MHz hyper transport link which provides each PXI slot in the chassis up to 1 GB/s of dedicated bandwidth with the overall system bandwidth of 4 GB/s [38].



(a) PXIe–8130 embedded controller (b) PXIe–8130 block diagram

Figure 23. NI PXIe–8130 embedded controller (From [38])

b. Agilent Power Sensor U2001A

The Agilent U2001A USB power sensor shown in Figure 24 is connected to the central controller to combine the synchronization signals from master and slave elements. It is deployed because of its fast measurement and convenient setup. Power measurement can display on the central controller monitor via a USB port. The operating radio frequency range is from 10 MHz to 6 GHz, and the power level dynamic range is from –60 dBm to +20 dBm. The corresponding VI is programmed for the purpose of centralized control within the LabVIEW environment.

Figure 24. U2001A USB power sensor (From [39])

c. Vaunix Technology LSG–402 Signal Generator

The Vaunix Technology Lab Brick LSG–402 signal generator shown in Figure 25 is used as the LO source in the system. The stability of the LO signal is sufficient and its small size is convenient for experimentation. The LO power level and operating frequency is controlled by the central controller via a USB port. It has a graphical user interface (GUI) for operator use [40].

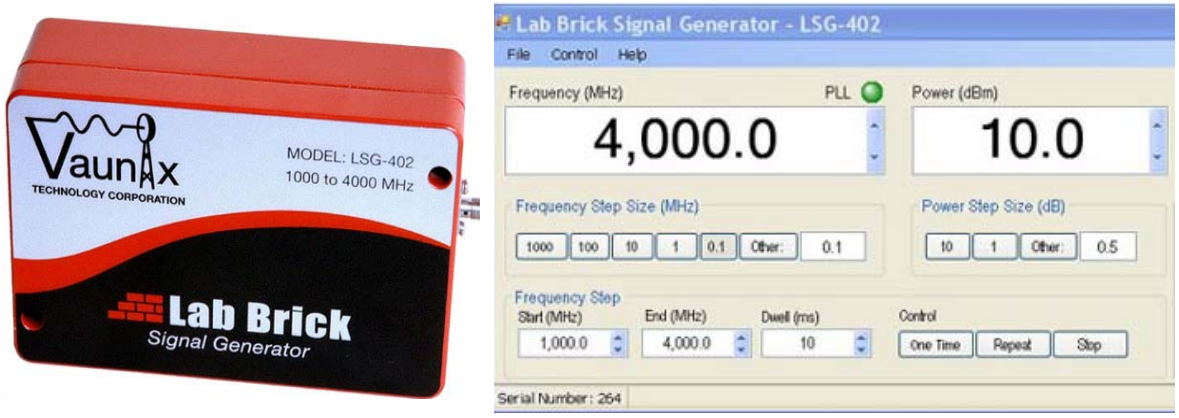


Figure 25. Lab Brick LSG–402 (From [40])

d. Baseband Differential Instrumentation Amplifier

The baseband differential instrumentation amplifier shown in Figure 26, BAMP for short, was made to convert four differential outputs (IP, IN, QP and QN) from the AD 8347 demodulator to two inputs (I, Q) for the NI PXI–5112 digitized oscilloscope. Robert Broadston, NPS Microwave Lab Director, designed and built this differential instrumentation amplifier to be incorporated with the AD 8347 demodulator. More BAMP details and circuits diagrams can found in the Appendix.

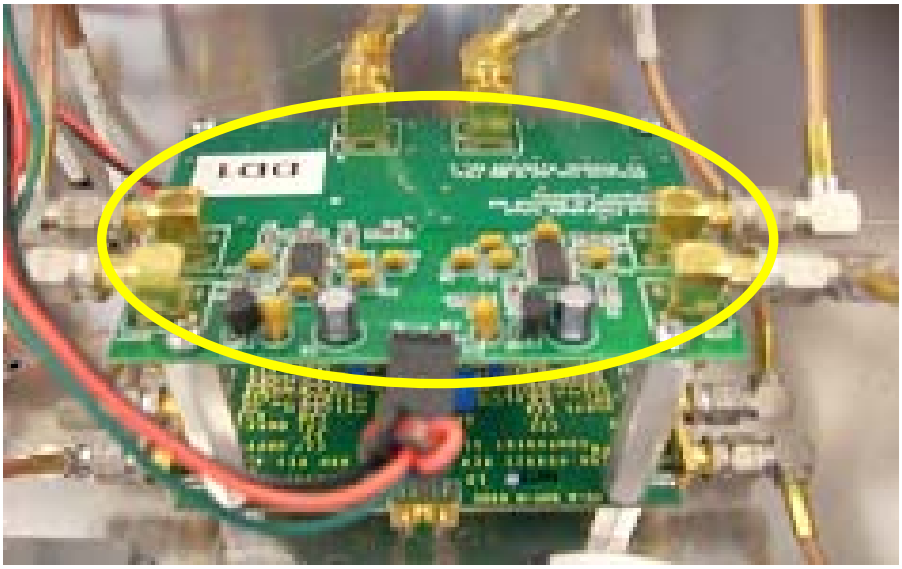


Figure 26. The differential amplifier board marked as DD1 placed above an AD 8347 demodulator

e. LabVIEW Software Program Modification

NI LabVIEW continues to be adopted as the main application software of the new setup. References [21]–[22] have developed a mature LabVIEW program and some functional VIs for previous FPGA implementation. Part of their work forms the basis of the present program. Hardware changes from the FPGA system to the PXI controller require a corresponding software modification.

Jiheon Ryu, an NPS Research Associate from the Engineer Scientist Exchange Program (ESEP), developed the control VIs for the AD 8346 modulator and AD 8347 demodulator. He also conducted a series of critical tests concerning the performance of the modulator, demodulator, and BAMP. These test results are recognized as vital accomplishments for the subsequent experimentation in this paper.

The other parts of the LabVIEW program, such as switch control, Agilent power sensor program, and other related VIs, are corporate with Ryu's work in order to validate the synchronization process from the complete program.

E. NEW DEMONSTRATION SETUP

The final revised two-element WDDPA configuration is shown in Figure 27. Ideally, each module should have its own local PXI controller. In order to reduce costs, the two modules share a single PXI box. The full capability of the T/R module is maintained so that testing of the module functionality can be performed.

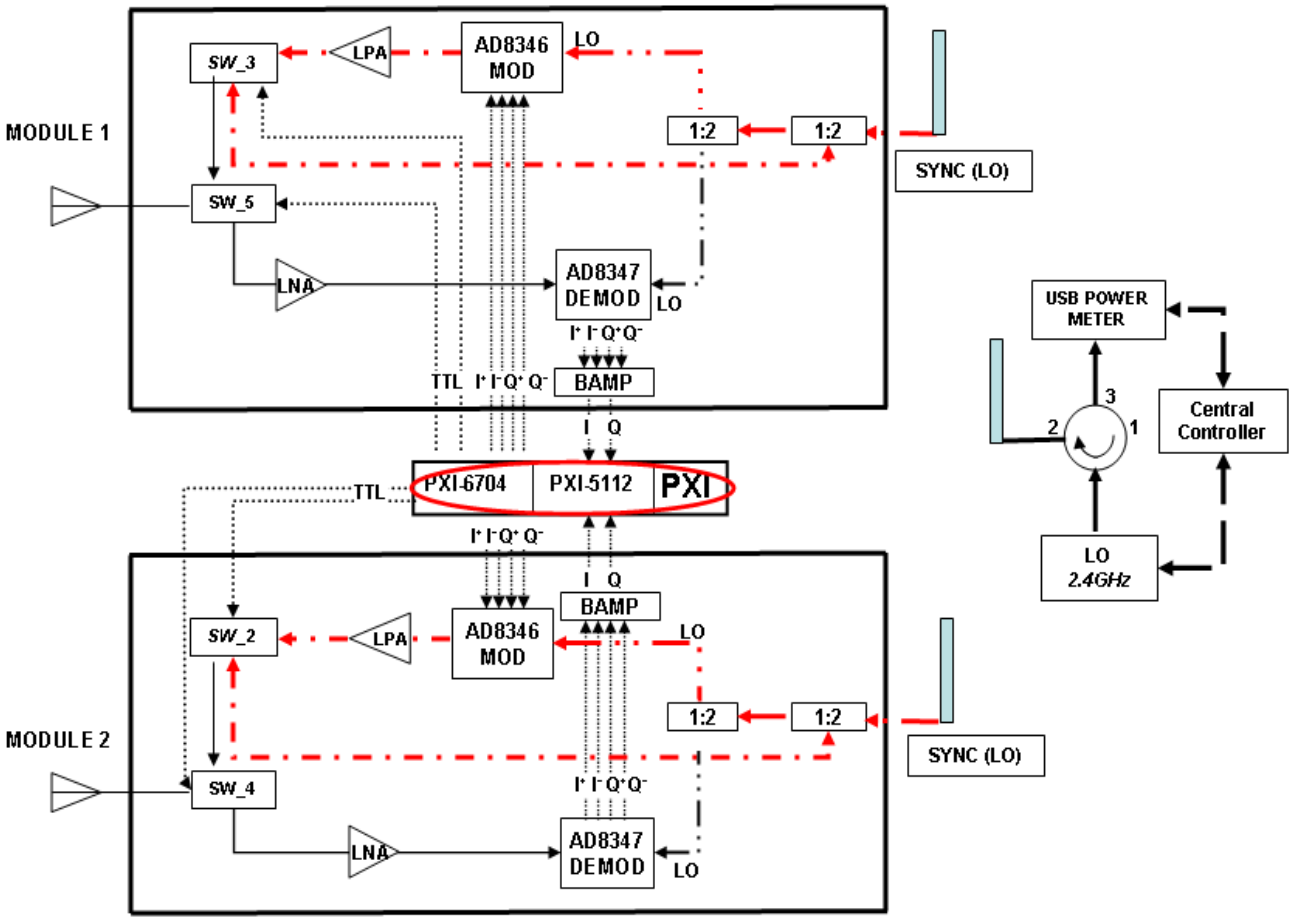


Figure 27. The final configuration of two T/R modules with the single PXI controller highlighted

The highlighted middle part of configuration is the combined local controller, a single NI PXI controller incorporated with PXI–6704, and PXI–5112 modules. During the synchronization process, two PXI–6704 modules (one for each element) are deployed to send out beamforming information and TTL signals to the modulators and individual switches.

This configuration is used to validate of the synchronization process. The individual modulator up-converts the waveform and beamforming control signal provided in terms of IP, IN, QP, and QN from the PXI–6704. The signal is then amplified approximately 18 dB by the PA, RF Bay LPA–4–14 RF Amplifier [21]–[22]. The PXI–6704 also sends out TTL signals to control the switches so that they operate in either the transmission or synchronization mode. For synchronization, the modulator boards act as phase shifters, and step through a range of phases at the command of the master controller. Then the transmitted signals from the master and slave are sent back to the central controller, where they are combined and the results for all phase steps are plotted in order to find the null. The theoretical synchronization process is done by localizing the null, representing where two signals are 180 degrees apart.

Note that the demodulators are vital components in the WDDPA receive function, but they are not necessary in the current synchronization process.

F. SUMMARY

In this chapter, the most critical concepts and operation of the distributed array and wireless BFN are summarized. The vital parameters of the WDDPA are then discussed with regard to distributed arrays and wireless BFNs. Furthermore, the basic architecture of the WDDPA demonstration array is broken into four parts and discussed briefly.

The new WDDPA demonstration architecture, using a single PXI controller, is presented. The new single controller architecture has cost advantages, as well as more processing capability and a faster sampling speed. Full functionality of the T/R module is maintained, allowing the validation of critical concepts.

The main objective of this paper is to validate and evaluate the operation of the synchronization circuit. Accordingly, the concept of the “brute force” synchronization algorithm is highlighted. The synchronization operation and the related circuits are also discussed.

In Chapter III, the comprehensive test of a single element wired to the central controller is first conducted. The signal power level through the synchronization circuit in each element is examined and investigated. To prevent similar problems met by [21]–[22], several alternatives of hardware combinations are discussed. Two-element experimentation is conducted after verification and validation of single-element synchronization is completed successfully.

III. WIRED SYNCHRONIZATION TESTING

A. BACKGROUND

Several different configurations of the synchronization circuit have been tested in references [21]–[22]. In those experiments the combined LO returned signal curves were distorted, causing the minimum of the waveform to be shifted and destroyed. It was suspected that the LPA and LO power leakage were the major factors causing serious distortion of the LO returned signal curves [21]–[22], [31].

The objective of this chapter is to first verify the hardwired synchronization operation of two elements. Wired transmission paths ensure that the two T/R modules receive a high quality LO signal without interference or multipath. After the wired case is successfully demonstrated, the wireless synchronization will be conducted in Chapter IV.

References [21]–[22], [31] have investigated each individual T/R module component's performance. To ensure the quality of the assembled module, it is still necessary to test all of the module components to verify that they function up to product specifications. Following that, each module is verified in the normal and synchronization modes of operation.

Several possible causes are identified to account for the deviation from ideal performance, and modifications are proposed to improve the performance of the synchronization circuit.

B. SINGLE-ELEMENT TESTING

Figure 28 shows the present architecture of the WDDPA T/R module. A metal box with a lid is used for each module to mount the hardware components, helping to protect against possible electromagnetic interference from the outside.

The boxed modules also offer a relatively convenient arrangement for breaking into the circuit for measurement and allow for simple modifications of the circuit.

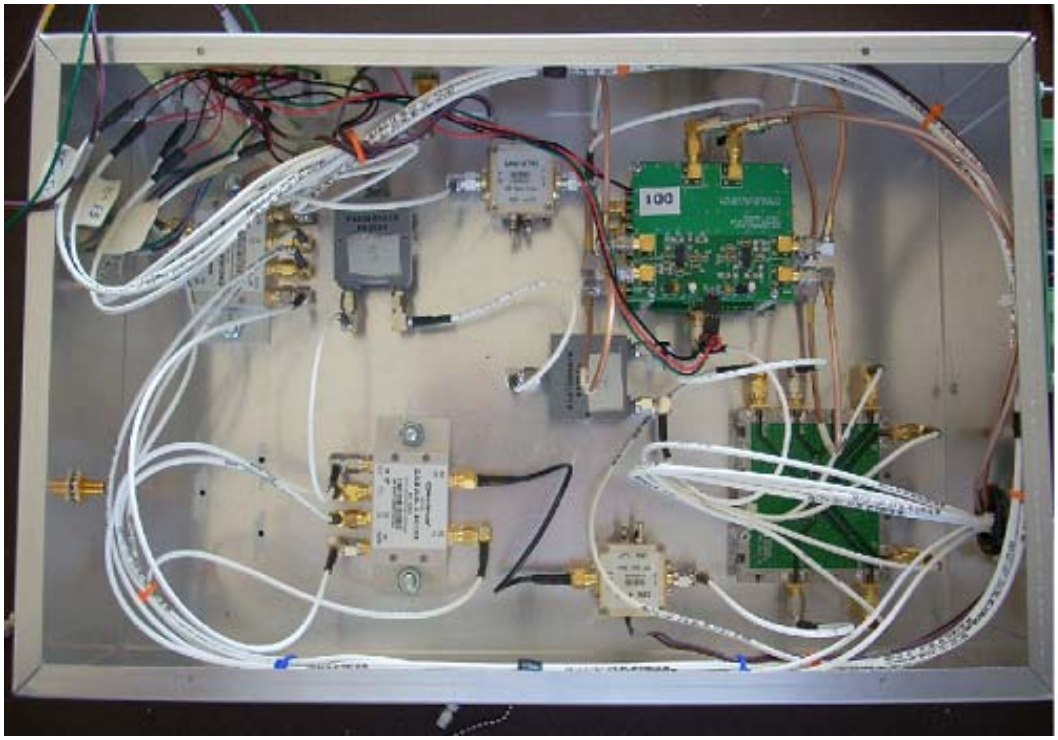


Figure 28. The metal box accommodating original hardware components

1. Module Components

All the hardware components implemented in the T/R module have been investigated thoroughly in [21]–[22], [31]. They perform up to the manufacturer's claim, and in many cases even outperform the specifications. Table 3 lists all the components implemented in the T/R module. Note that not every component is required for the synchronization operation.

WDDPA T/R Module Hardware Components			
Module Component	Make (Model)	Number	Required for Synchronization
Modulator Board	**Analog Devices (AD 8346)**	**1**	**Yes**
Demodulator Board	Analog Devices (AD 8347)	1	No
Low Power Amplifier	**RF Bay (LPA–4–14)**	**1**	**Yes**
Low Noise Amplifier	RF Bay (LNA–2700)	1	No
Switch	**Mini-Circuits (ZASWA–2–50DR)**	**2**	**Yes (1)**
Power Divider	**Pasternack (PE2014)**	**2**	**Yes**
Baseband Differential Power Amplifier	BAMP Built by Robert Broadston	1	No

Table 3. Components deployed in T/R module (After [22])

Evaluation of the two-element synchronization operation is the focus of this chapter. Understanding how the circuit performs the synchronization is important to the objective. Figure 29 shows the path that LO signals take in the synchronization circuit of a T/R module.

After entering from the top the LO signal from the controller passes through two power dividers, and then is sent into the AD 8346 Modulator LO port. The LO signal serves as the phase reference for the transmitted radio frequency (RF). Phase shifts are introduced according to the beamforming control signal. At the RF output of the AD

8346, the baseband signal (phase-shifted LO) is amplified by the LPA. The switch directs it to the first power divider. The phase shifted LO signal from the module is then transmitted back to USB power sensor.

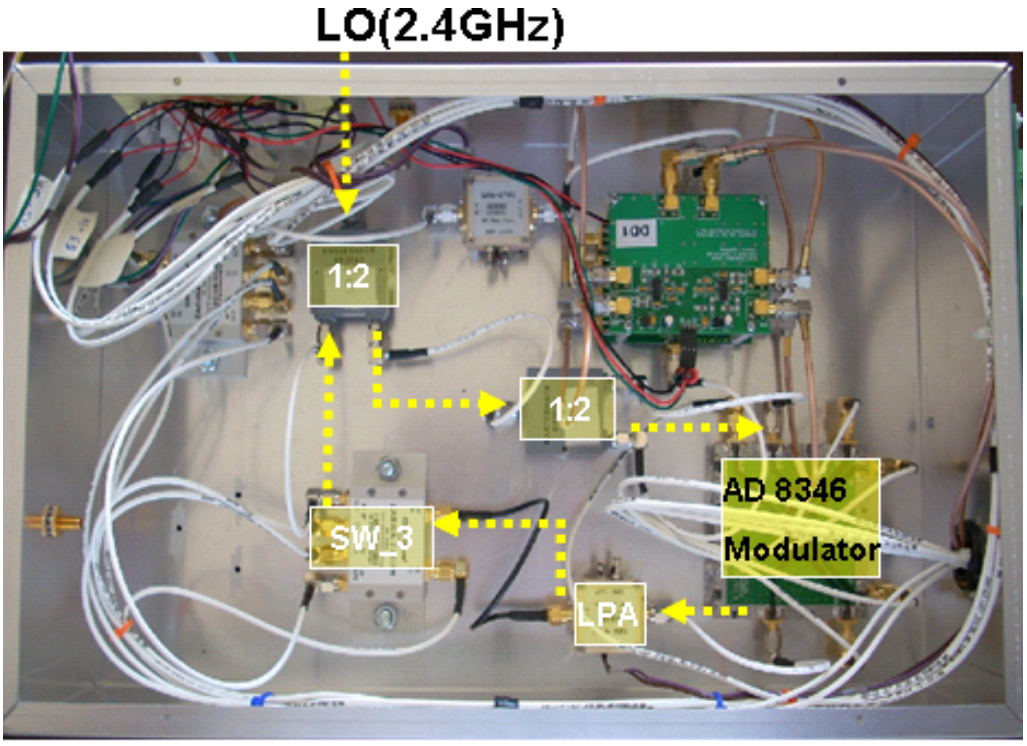


Figure 29. Highlighted LO signal passing through the synchronization circuit in a boxed T/R module

Figure 30 shows the simplified diagram, illustrating the LO signal passing through the synchronization circuit of a single module. The bold box represents for the T/R module and inside is the hardware components as noted. As stated in Table 3, the components required in the synchronization circuit are as follows: two power dividers, one modulator, one LPA, and one switch. The red dashed line represents for the LO signal.

The phase-shifted LO signals from the modules are sent to the USB power sensor, and the central controller displays the plot of the combined signal. Therefore, the stability of the signal power level in each element is very important to the synchronization process.

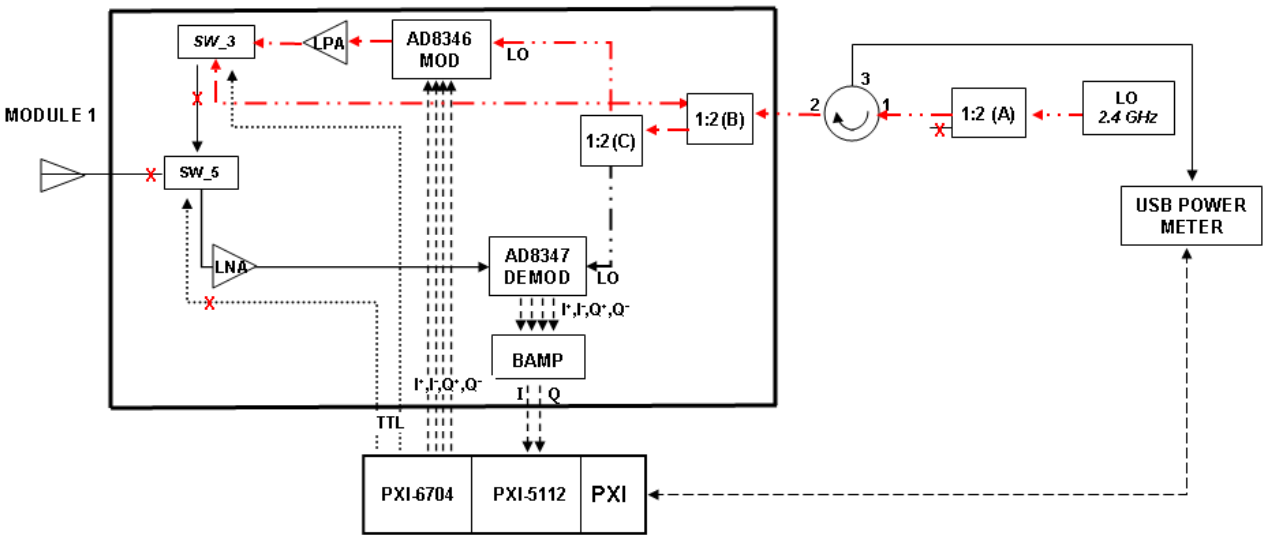


Figure 30. The illustration diagram of single T/R module with LO signal highlighted

2. LO Signal Power Measurements

To ensure the synchronization operation, the LO signal power levels at various points in T/R module 1 are examined in this section. In order to generate the RF signal properly, the LO input power in the AD 8346 modulator board must be maintained between −6 and −12 dBm, according to the specification shown in Table 4. In the current one-element setup, the LO output power is set to 10 dBm to provide the LOIN port at the AD 8346 −7 dBm input power, once the insertion loss from other components and cables is taken into consideration.

AD 8346 Modulator			
Parameters	Min	Max	Units
Operating Frequency	0.8	2.5	GHz
Output Power	−13	−6	dBm
LO Input	−12	−6	dBm

Table 4. AD 8346 specifications (From [41])

The central controller commands the AD 8346 modulator board to act as the phase shifter, stepping through 360 degrees. The beamforming amplitude is 2 V for the subsequent testing. The operator can examine the curves of the returned LO power level on the display of the central controller.

The red numbers in Figure 31 represent the LO power measurements. The output is 10 dBm in order to provide the AD 8346 modulator approximately –7 dBm, sufficient to phase shift the waveform based on the beamforming control signal.

Note that shifted LO signal (baseband) is measured –45 dBm at the VOUT port of AD 8346 board. According to the specifications in [41]–[42], the signal power is –10 dBm (within the range of –13 and –6 dBm) so there must be some unidentified errors occurring in the T/R module. A diagnostic test is required to find out what caused the degraded baseband signal power level.

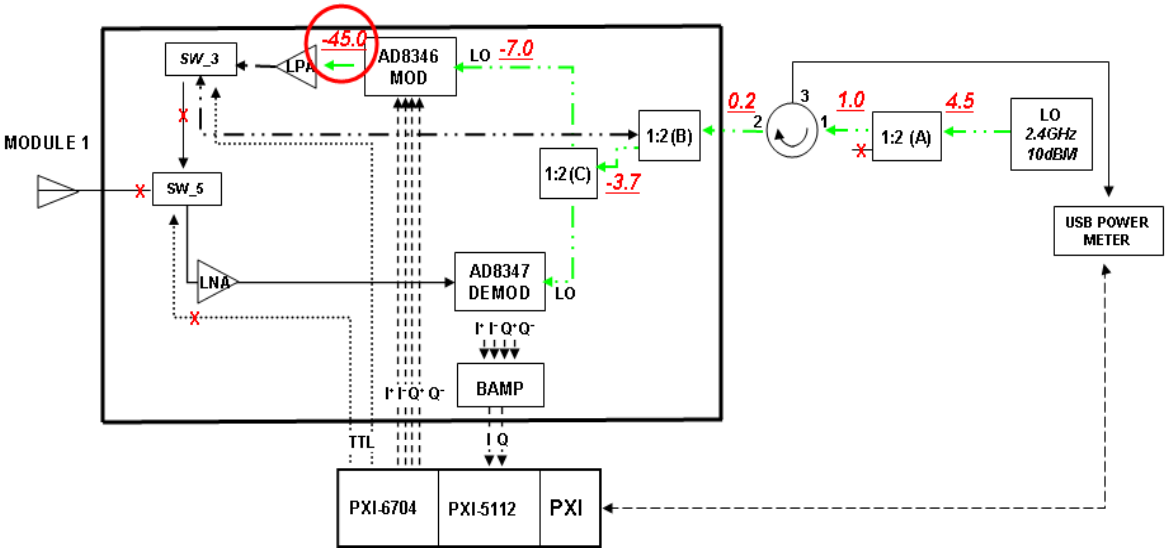


Figure 31. Measurements of LO signal power level in T/R module 1 with the LO output power highlighted (power is in dBm)

3. Diagnostic Test

The spectrum analyzer, an Anritsu MS2721A Spectrum Master shown in Figure 32, is used to observe the LO signal.

Numerous unwanted spurious signals or “spurs” (most likely inter-modulation products, IM) are observed in the circuit, as shown in Figure 32. The span of the spectrum analyzer is from 0.8 to 2.5 GHz, which covers the AD 8346 modulator’s operating frequency. The spurs exist with the LO signal, and many of them have approximately the same power level as the LO.

Based on this observation, power levels of these spurs vary dramatically. This caused the instability of the phase of the baseband signal, and affects the power levels of the returned LO signal.

Ong [43] earlier noted that some remnants of the LO were present in the output port of the AD 8346 modulator board. This is known as LO feedthrough. It occurs when the LO signal leaks directly to the RF output port due to parasitic capacitance, power supply coupling, etc. The described LO feedthrough phenomenon is also observed in this case. The LO feedthrough is considered one of the major factors leading to the distorted signal power level curves observed in [21]–[22]. To improve the performance of the synchronization circuit, several alternatives are tested in order to lower or eliminate the effect of unwanted spurs and leakage.

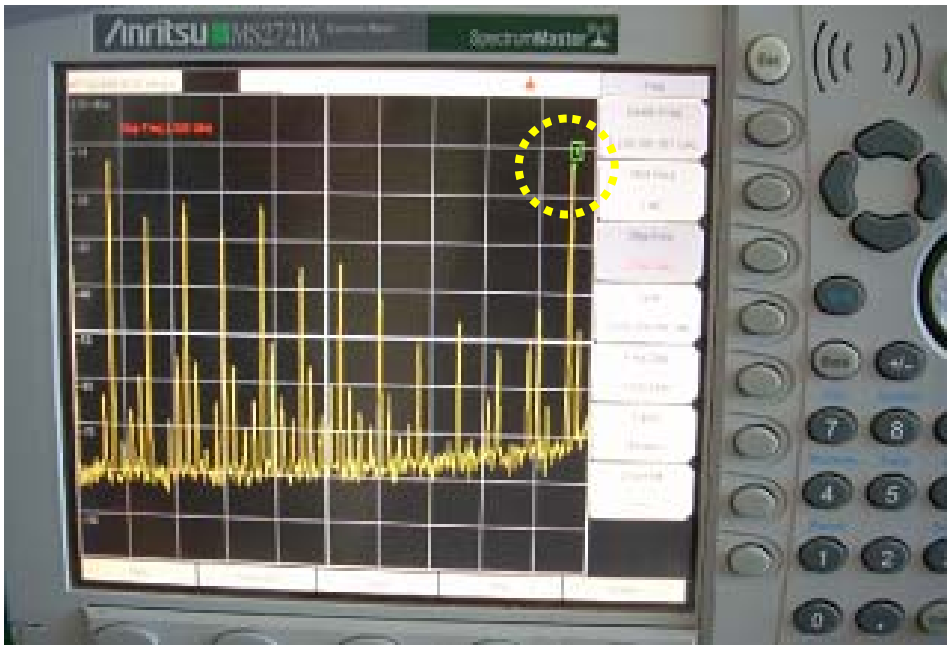


Figure 32. Numerous spurs occurring in the AD 8346 modulator board with 2.4 GHz LO signal highlighted

C. ALTERNATIVES INVESTIGATION

To evaluate possible measures to improve the performance of the synchronization circuit, a thorough investigation of individual hardware components in the synchronization circuit was performed, as presented in the subsequent sections.

1. Removal of LPA

References [21]–[22] both stated that the implementation of the LPA degraded the performance of the synchronization circuit. Accordingly, the first step in the diagnosis was testing of the synchronization circuit after removing the LPA.

Figure 33 shows the circuit arrangement for measurement of LO signal power level in module 1 without LPA. The baseband signal from the AD 8346 modulator is directed to the control switch. The LO signal power level is measured, showing that the power increased from the previously measured −45 dBm to −30 dBm. Although 15 dB is a very significant change, it is still far from the expected value of −10 dBm [42].

Note that LPA is supposed to amplify the modulator RF power level (which is just phase shifted LO in this case). Compared to the last setup, the signal power was reduced, not increased. Spurs, as shown in Figure 32, still exist. Also, LO feedthrough affects the synchronization circuit, leading to the distorting and degrading the performance of the AD 8346 modulator.

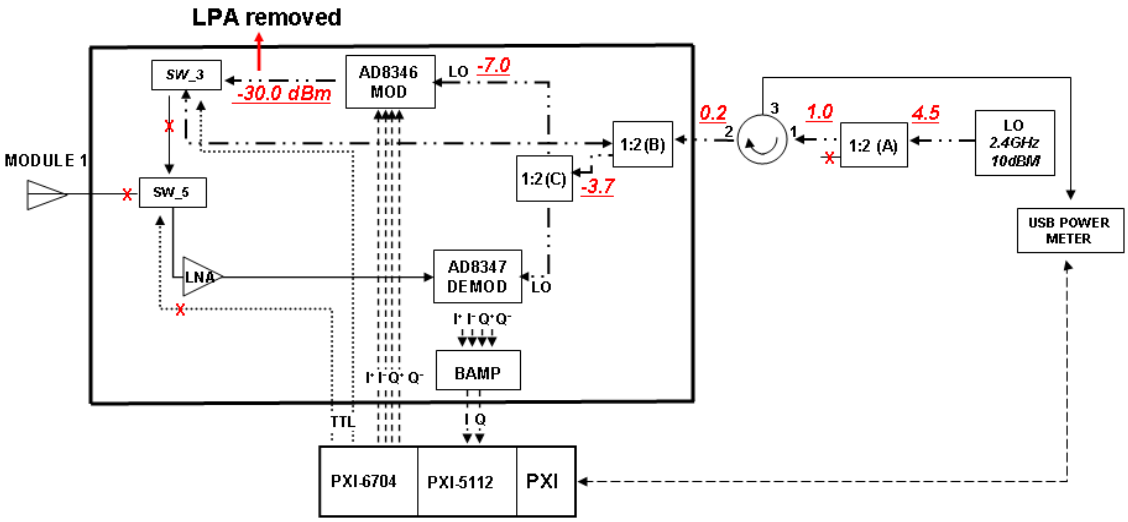


Figure 33. Measurement of LO signal power level in T/R module 1 without LPA (power in dBm)

2. Implementation of Isolator

Next, an isolator (circulator with one port terminated) as shown in Figure 34 is placed in the original position of the LPA.

Figure 34. An isolator is inserted at the location of the LPA

Figure 35 shows that signal power level at VOUT port is -26 dBm, 4 dB higher than the setup without the LPA. It still does not meet the expected signal level. The

behavior of spurs observed in the circuit, however, is slightly improved compared to the initial state, and were even eliminated for some phase values when the PXI–6704 stepped through some specific values.

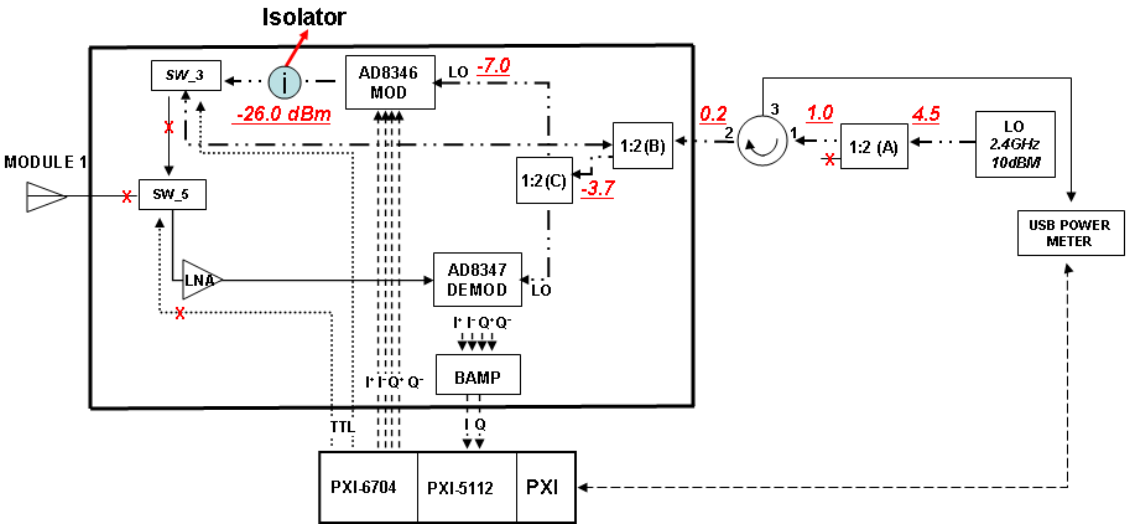


Figure 35. Measurement of LO signal power level in T/R module 1 with isolator implemented (power in dBm)

3. Removal of Switch

As Figure 36 shows, the isolator is kept in place of the LPA and the switch is removed.

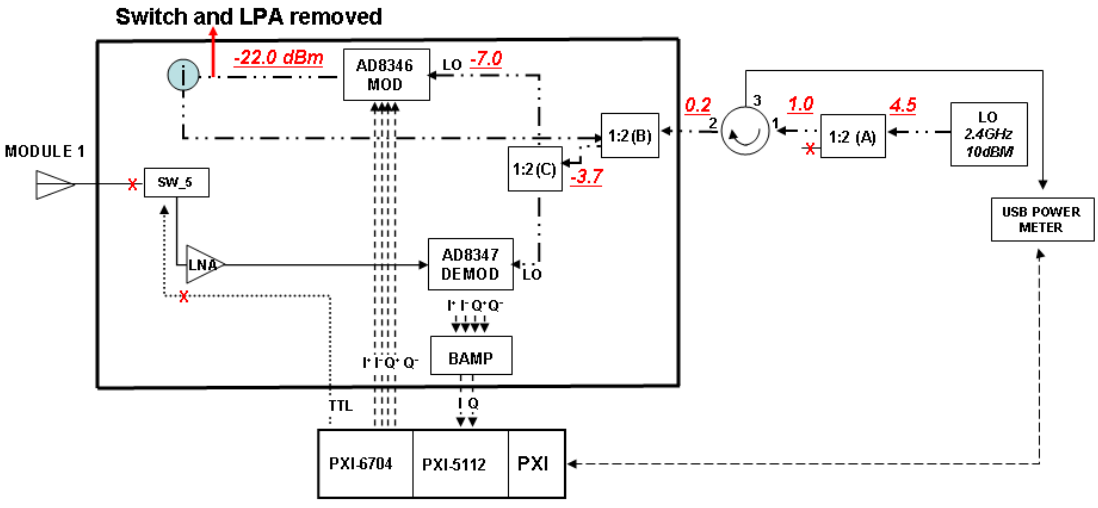


Figure 36. Measurement of LO signal power level in T/R module 1 with the switch and LPA removed (power in dBm)

The switch is required in the control of the synchronization and normal modes, the reason it is removed in this setup is to isolate the possible effects of the individual hardware components. The result showed another 4 dB improvement, but this does not solve the fundamental problem that the spurs cause the instability of the synchronization circuit.

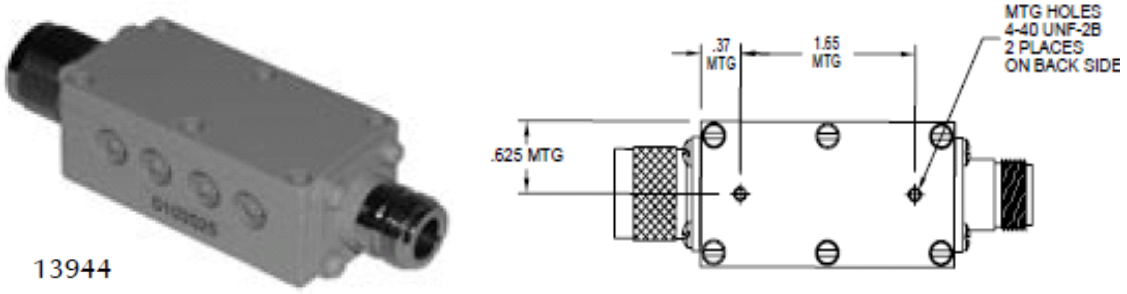
4. Implementation of Filter

The previous modifications were not successful in eliminating the spurs caused by the LO feedthrough. Ryu therefore proposed the implementation of an appropriate bandpass filter in the current synchronization circuit to eliminate the spurs.

Note that for the WDDPA's future applications, the implementation of the filter will limit its operating frequency range. Accordingly, the filter implementation is a way to verify the operational concepts of the WDDPA synchronization circuit for demonstration purposes only.

a. Investigation of MFC–13944 Filter

To meet the goal of an efficient and cost-effective WDDPA demonstration array, Microwave Filter Company's (MFC) 13944 economical 2.4 GHz full band bandpass filter (MFC–13944) was adopted. In accordance of the two-element setup, two filters are needed.



(a) MFC–13944 (b) Profile of MFC–3944 filter

Figure 37. Model 13944 full band bandpass filter (From [44])

The vital parameters of the MFC–13944 filter are summarized in Table 5. The LO feedthrough is 2.4 GHz which is passed through the filter. The spurs must be sufficiently suppressed; therefore, the rejection is important to the current setup.

MFC–13944 2.4 GHz Filter	
Parameter	Specification
Center Frequency	2442 MHz
Relative 3 dB Bandwidth	100 MHz (Min)
Insertion Loss (at center frequency)	1.5 dB (Max)
Rejection	40 dB at 2242 MHz 40 dB at 2642 MHz

Table 5. MFC–13944 filter specification (From [45])

Figures 38 and 39 show the scattering parameters of the two MFC–13944 filters using the Agilent Technologies 8510C Vector Network Analyzer [46]. The center frequency is 2.44 GHz as the specification claims. The observed 3 dB bandwidth is approximately 140 MHz for both of the filters, and the specification states that the minimum bandwidth is 100 MHz. As for insertion loss, both are around 0.7 dB, outperforming the specification. In summary, the test result shows that both of the filters performed within the range of the manufacturer's specification.

Filter 1

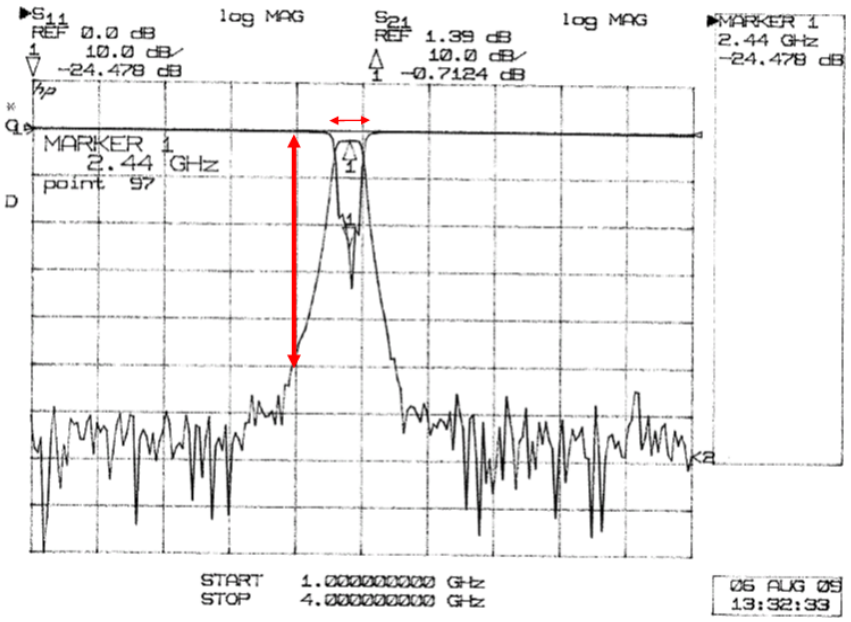


Figure 38. Filter 1 performance with the 3 dB bandwidth and rejection highlighted

Filter 2

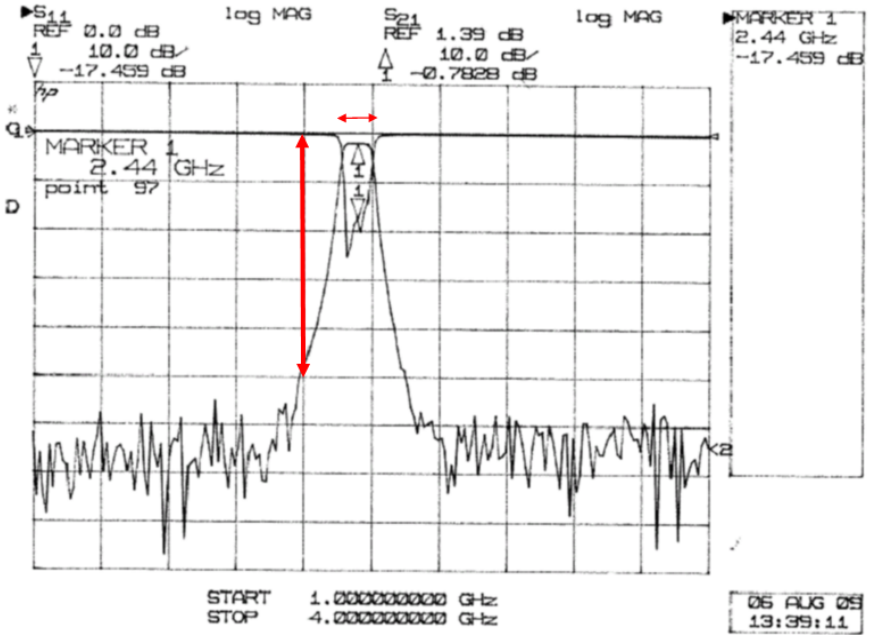


Figure 39. Filter 2 performance with the 3 dB bandwidth and rejection highlighted

b. Module Testing with MFC–13944 Filter

To compare the results with the previous setups, the MFC–13944 is placed in the synchronization circuit without the LPA, control switch, or isolator.

Figure 40 shows that the LO source output power is maintained at 10 dBm. The control VI of the PXI–6704 sets the amplitude at 2 V and also commands phase to step through 360 degrees, as in other setups. The LO power level at the VOUT port of the AD 8346 board is measured -8 dBm, which meets the expected power in [41]–[42] and no spurs are observed.

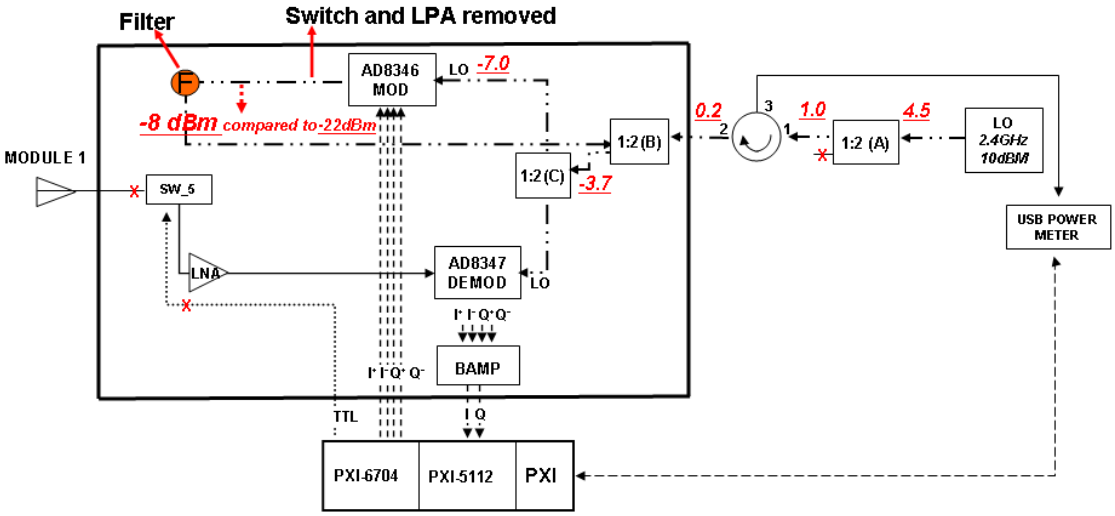


Figure 40. Measurement of LO signal power level in T/R module 1 with MFC–13944 implemented

To further clarify the effect of the MFC–13944 in the synchronization circuit, the LPA is placed back in the circuit and tested with results as shown in Figure 41.

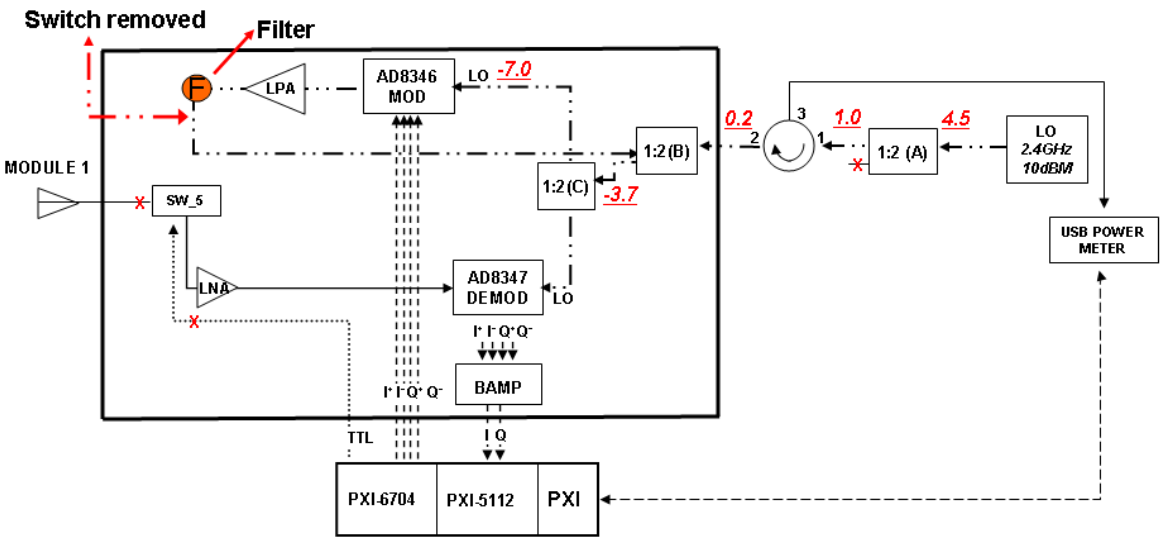


Figure 41. Measurement of LO signal power level in T/R module 1 with MFC–13944 and LPA implemented

The comparisons of these two setups are made and summarized in Table 6. Note that with the implemetaiton of the MFC–13944 filter, spurs are not observed in the synchronization circuit. Also, unlike measurements in the first two setups (Figures 31 and 33), the LPA does amplify the RF output.

LO Power Level	**With LPA**	Without LPA
Max	–8.3 dBm	–15.7 dBm
Min	–12.1 dBm	–24.4 dBm
Average	–10.4 dBm	–20.1 dBm
Difference	3.9 dB	8.7 dB
Spurs	**No**	No

Table 6. Modulator RF output power comparison of two setups (with and without LPA present)

5. Summary

The addition of the MFC–13944 filter ensures the LO power stability in the synchronization circuits. To make each T/R module perform the synchronization process properly, the potential interference spurs must be reduced to a negligible level. The previous setups illustrate the necessity of adequate filtering.

In the next step, a simple but useful experiment will be conducted. Initially, the LO source was only provided to the circulator from which it passed to the module. After passing through the synchronization circuit, phase shifted and retransmitted by the modulator, the signal was sent to the USB power sensor through the circulator. Now, by inserting a power divider, some of the 2.4 GHz signal is sent to the USB power sensor directly as shown in Figure 42.

Signal (A) is the phase shifted signal (to be stepped through 360 degrees). It is summed with signal B from the LO source and directed to the USB power sensor.

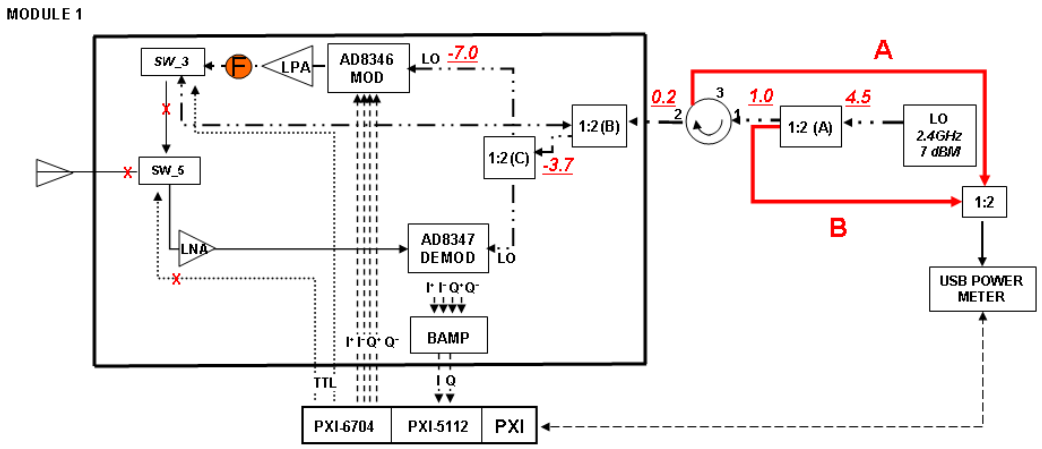


Figure 42. The returned LO signal A and the reference signal B highlighted (power in dBm)

With this easy setup, combining the phase shifted signal (A) and the reference signal (B), the power sensor enables the central controller to display the graph of combined signal power versus module phase shift, which is the fundamental measurement of the WDDPA synchronization operation.

The LO power level at various points in the circuit was subsequently measured, and noted in Figure 42. All the input information controlled by the PXI–6704 is the same as in the previous setups in this chapter. Figure 43 shows the shape of the combined signals from the reference and module.

If the LO power levels remain reasonably stable in the synchronization circuit, no spurs or other interference occur. The waveform should be symmetrical and the notch deep enough to determine the minimum location for synchronization purposes. The notch is approximately 18 dB deep in this case. The returned power level is measured every 10 degrees, which is adjustable in the control VI of the PXI–6704.

According to the result shown in Figure 43, the implementation of MFC–13944 is necessary for successful synchronization in the WDDPA demonstration array.

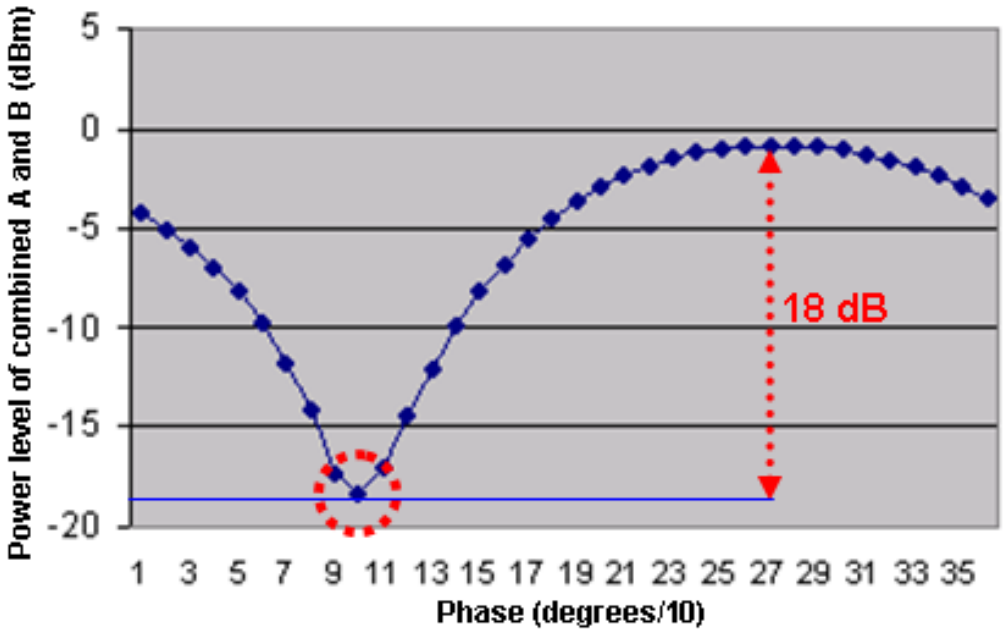


Figure 43. The result of the synchronization process of the filter-implemented T/R module 1 with the minimum power level highlighted

D. VALIDATION OF NEW SYNCHRONIZATION CIRCUIT

This section describes the series of experiments that were conducted to validate the synchronization circuit. Several different devices, such as a coaxial cable, the 3 dB quadrature coupler, and the phase shifter, were selected to be incorporated with the T/R module 1, to determine whether the new synchronization circuit with the MFC–13944 filter is able to detect the shifted phase. Also note that in the subsequent testing, the filter is placed between the AD 8346 modulator and LPA, to improve the stability of the modulator power.

Once these tests were completed successfully, showing that the filter-implemented circuit works as expected, a two-element synchronization experiment was conducted.

1. Testing with Coaxial Cable

A common coaxial cable with connectors is selected to introduce a phase shift for the synchronization operation as shown in Figure 44. Note that the coaxial cable is connected in the path of LO reference signal (B). The rest of the setup is identical to Figure 42.

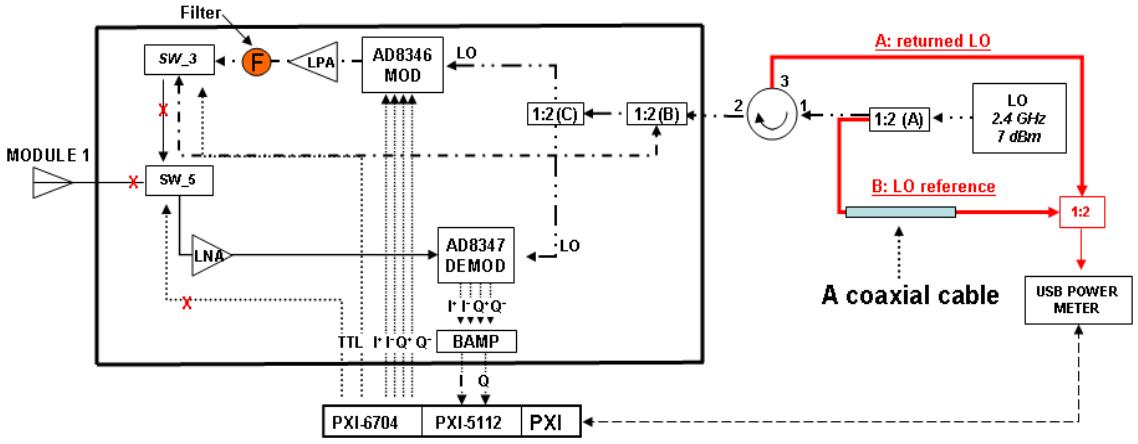


Figure 44. Application of a regular coaxial cable in the synchronization testing

To identify if the phase shifts by the proper amount, the phase of the coaxial cable was measured with the 8510C Vector Network Analyzer. Figure 45 shows that the phase

of the cable is approximately 66 degrees, and Figure 46 shows that the phase reference without the cable is about –42 degrees. Therefore, the difference of two values, 108 degrees, is supposed to be the shifted phase.

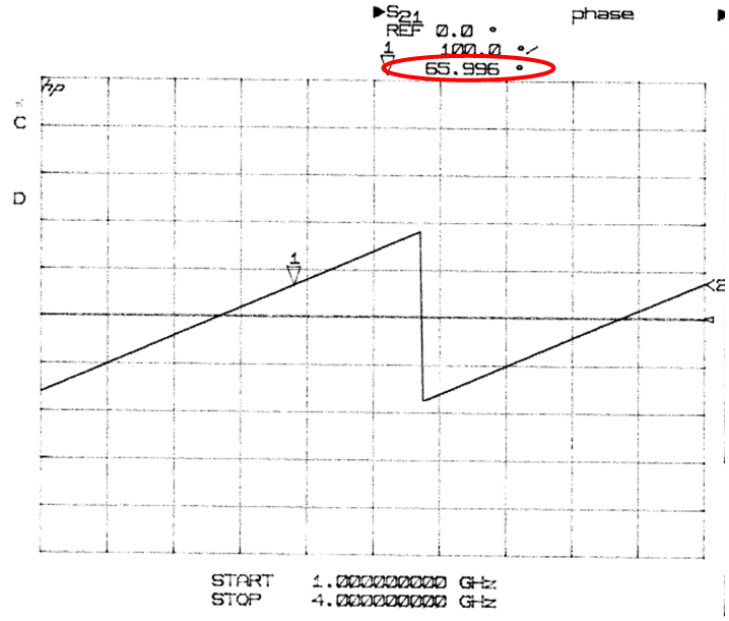


Figure 45. The phase of the coaxial cable

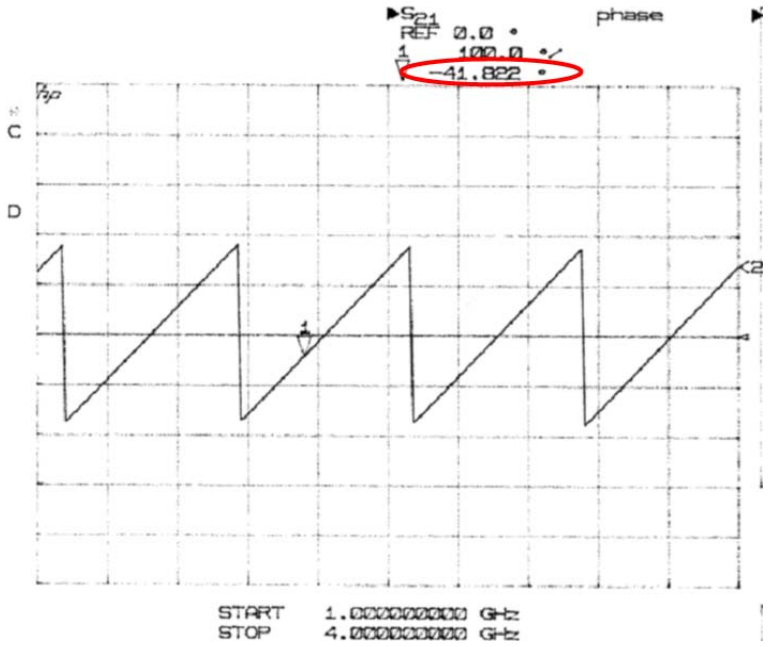


Figure 46. The phase reference without the coaxial cable

Figure 47 shows the measurement of the two combined signals of the setup with and without the coaxial cable.

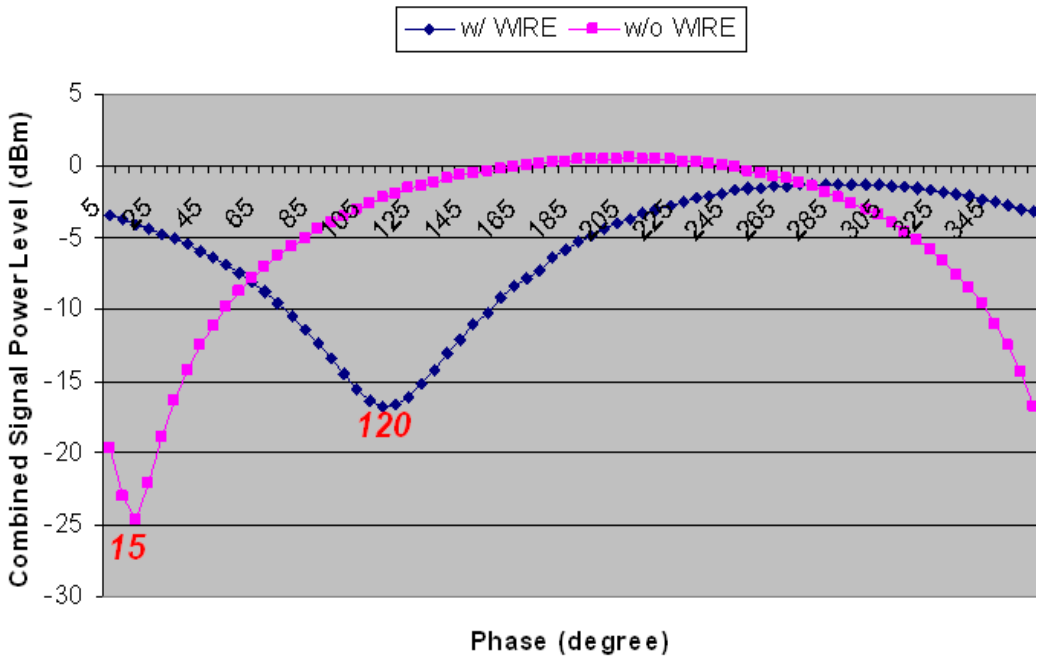


Figure 47. The shifted phase with the implementation of the coaxial cable

There are two curves shown in Figure 47: one is the combined signal without the coaxial cable, and the other is with the cable. The measurement was taken by the USB power sensor every five degrees and, as noted in Figure 47, the null of the initial setup is 15 degrees and the null of the coaxial cable-implemented circuit is 120 degrees. The difference is 105 degrees, compared to 108 degrees from the calibration by the network analyzer. Therefore, the error is only three degrees. This shows that the synchronization circuit is able to detect the shifted phase.

Also note that, aside from the location of the null, the two curves have different shapes. To be more specific, the depth of the individual notches is different. The initial setup has the notch depth at 26 dB, whereas the other is approximately 17 dB. The difference is 9 dB. This is because the signal power levels of A and B in Figure 44 are different in each case.

If the power levels of A and B are close, then the shape of the combined signal power levels will have a deep notch. If the power levels are not equal, but still relatively close, then the shape will be similar to the one with a cable, as shown in Figure 47. Unequal amplitudes make it difficult to detect the location of the null accurately. Once the difference of two signals becomes very large, the overall performance of the method will degrade dramatically.

2. Testing with 3 dB Quadrature Coupler

The 3 dB coupler applied in this test, shown in Figure 48, is a quadrature coupler where the phase difference between the two output ports is either 0 or 90 degrees.

Figure 48. Anaren 3 dB quadrature coupler with the phase of the two ports highlighted

Figure 49 shows the measured phase difference, 90 degrees on the plot, between the output ports measured by the network analyzer.

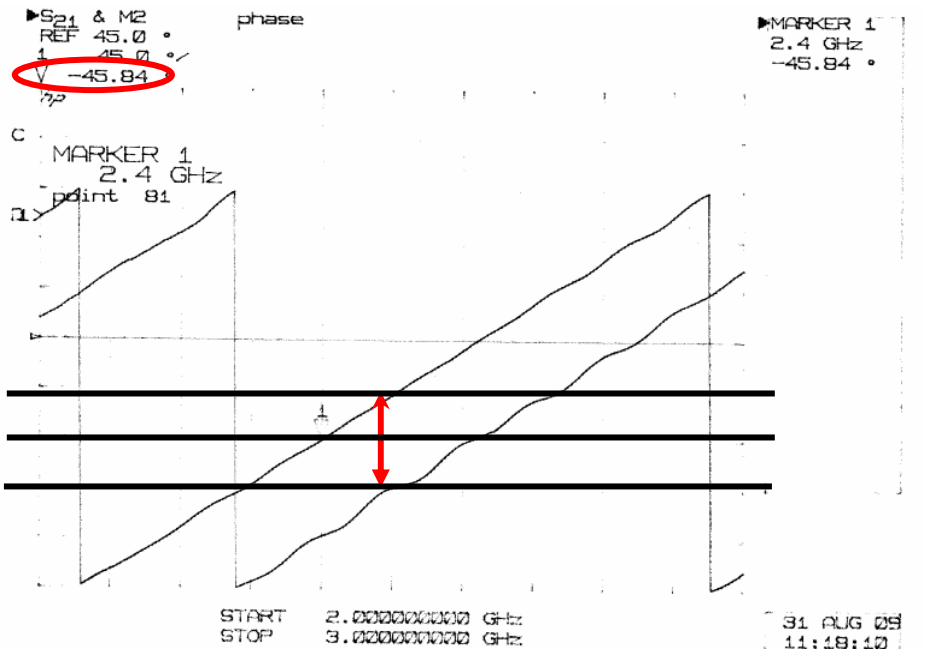


Figure 49. The phase difference between two ports of the 3 dB quadrature coupler

Figure 50 shows the setup with the 3 dB coupler implemented in the path of signal B to shift it either 0 or 90 degrees, depends on which port is connected.

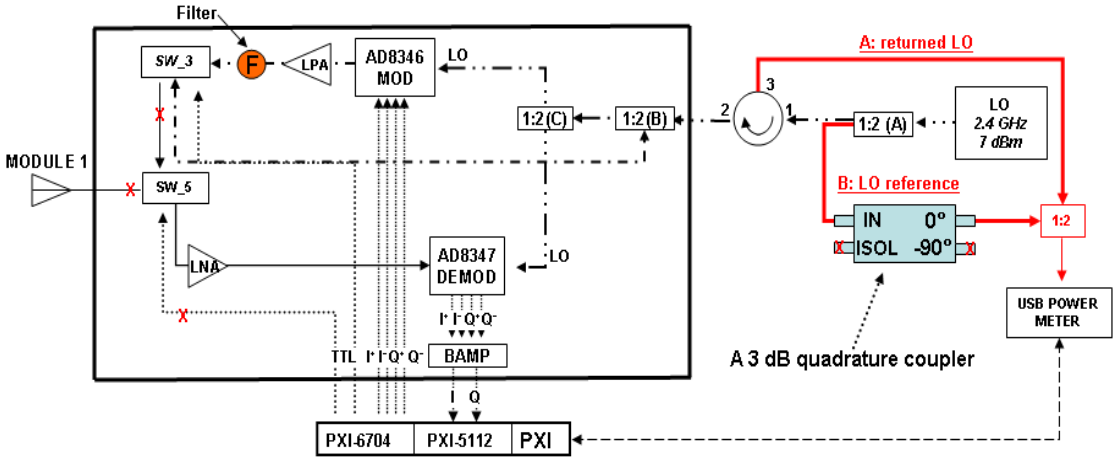


Figure 50. Application of a 3 dB quadrature coupler in the synchronization testing with 0° port connected

Figure 51 shows the result with the 3 dB quadrature coupler-implemented circuit. Using the synchronization process the null location when using the 0° port is 265

degrees, and the null location using the −90° port is 355 degrees. The difference is 90 degrees, in accordance with the expected shifted phase.

For the measurement, signal A and B are adjusted with attenuators to be the same level. Note the depth of the notch is approximately 34 dB, which is much deeper than the previous setups.

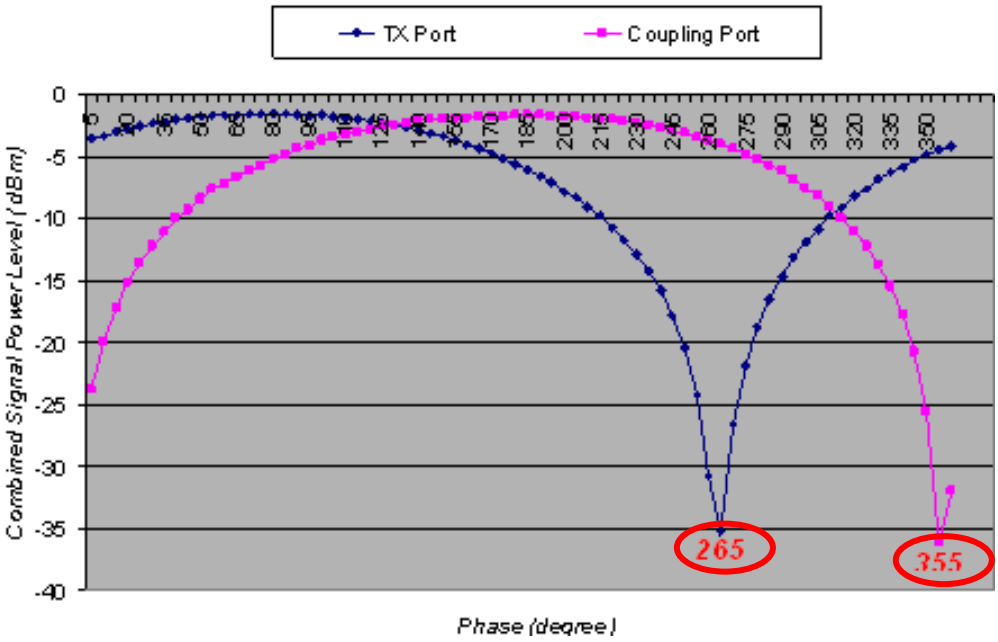


Figure 51. The shifted phase of the 3 dB coupler implemented circuit with the nulls highlighted

3. Testing with Phase Shifter

The previous two tests verified that high quality nulls can be formed using a length of cable and a quadrature coupler as phase shifting devices. To ensure the synchronization circuit not only works in some limited cases but also for an arbitrary shifted phase, two 180-degree mechanical phase shifters were cascaded as shown in Figure 50. For each phase shifter, a turn of the knob is approximately 5.5 degrees. Together they are able to change a total of 320 degrees at 2.4 GHz.

Figure 52. Two mechanical phase shifters in pairs (From [22])

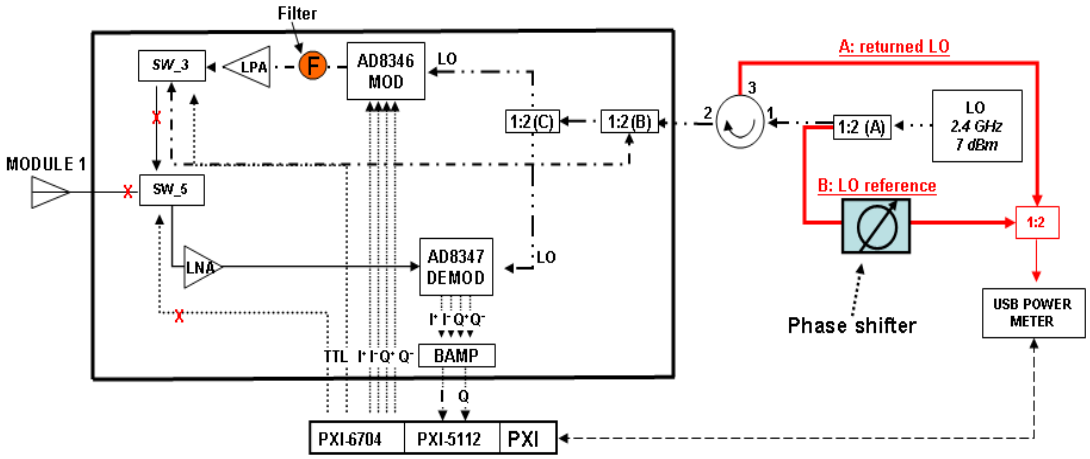


Figure 53. Application of the phase shifter in the synchronization testing

In this test, the phase is shifted by 6 turns (33 degrees) each time. At first, both knobs of the phase shifter are turned counterclockwise to the stops and turned clockwise back another turn (to avoid distortion near the stops). Then the PXI–6704 steps through 360 degrees and the USB power sensor takes the measurement every degree. The phase shifter is repeatedly turned clockwise by six complete rounds, and the whole process is run again. A total of 11 repetitions (320 degrees) are completed. Table 7 shows the summarized results.

Number of Turns (Expected Phase Shifted)	Null	Observed Shifted Phase	Error
0 (reference)	**316**	**0**	**0**
6 (33)	350	34	1
12 (66)	**23**	**67**	**1**
18 (99)	57	101	2
24 (122)	**83**	**127**	**5**
30 (155)	114	158	3
36 (188)	**146**	**190**	**2**
42 (221)	178	222	1
48 (254)	**213**	**257**	**3**
54 (287)	244	288	1
60 (320)	**276**	**320**	**0**

Table 7. The summarized phase shifting error by applying the phase shifter (in degrees)

Figure 54 shows the shifted phase of 0 (reference), 12, 24, 36, 48 and 60 turns. The measurements are taken every degree when the PXI–6704 steps through 360 degrees. All of the shapes are symmetrical and the depths of the notch are between 17 to 20 dB, sufficient for localizing the null. For all the cases, the nulls are located within five degrees of the expected phase shift.

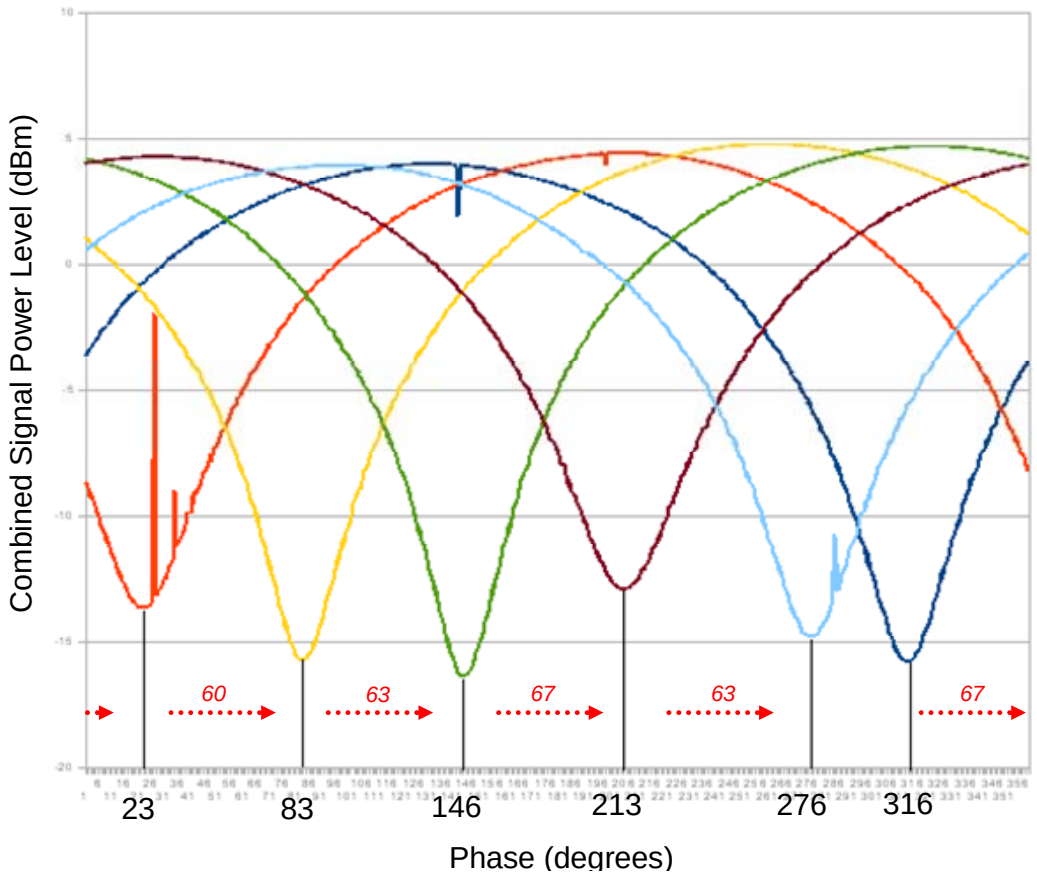


Figure 54. Phase shifted by implementing the mechanical phase shifter

4. Summary

These three experiments demonstrated that the shifted phase difference is detected by the synchronization algorithm with acceptable accuracy. The central controller runs a phase comparison algorithm, combining the LO reference signal and a returned RF signal from T/R module 1, which is essentially the phase shifted LO. The process represents a relatively easy simulation of one master and one slave element. Note that the transmission path between the master and slave is simulated with a coaxial cable.

E. TWO-ELEMENT SYNCHRONIZATION TESTING

The previous section shows that the elimination of the spurs by implementing the MFC–13944 filter improves the performance of the synchronization circuit. A series of T/R module experiments were conducted to measure phase shifts and the results were as expected.

The previous setup is basically composed of a single element, T/R module 1. With this relatively simple configuration, the synchronization concept and operation were demonstrated. In this section, the demonstration is extended to a two-element array. However, before T/R module 2 is implemented in the experimentation, the performance of T/R module 2 has to be verified with the same procedure as for T/R module 1.

During the process, an unexpected distortion of the shape of the combined LO power level of module 2 was found. Once the graph is distorted, it is very difficult to locate the null, and the value of the shifted phase is not reliable. The potential causes and solutions of the distortion are presented in the subsequent sections.

1. LO Power Leakage

For non-ideal devices there is power leakage occurring in the synchronization circuit. This is one of the major factors affecting the performance of the synchronization circuit, as discussed in [21]–[22], [31]. (Note that this is different than the LO feedthrough that occurs in the modulator). Figure 55 shows that the LO power leakage occurs due to insufficient isolation at coupler ports in the T/R module. It also occurs at the circulator applied in the connection of the USB power sensor.

Power leakage (D), shown in Figure 55, is discussed in [22] and [31]. Originally, the returned LO power was supposed to pass through the power divider highlighted in Figure 55. (This was originally a circulator but [22] suggested it be replaced by a power divider for improved isolation.) After the LO signal passes through the slave element and returns to the central controller, the reference and the phase-shifted LO are compared.

If the LO signal provided to the T/R module is not a stable source, then the comparison is in error. Leakage causes variation in the LO amplitude and phase,

resulting in distortion because it adds and cancels with the signal received from the controller. The shape of the combined signal power curve is distorted.

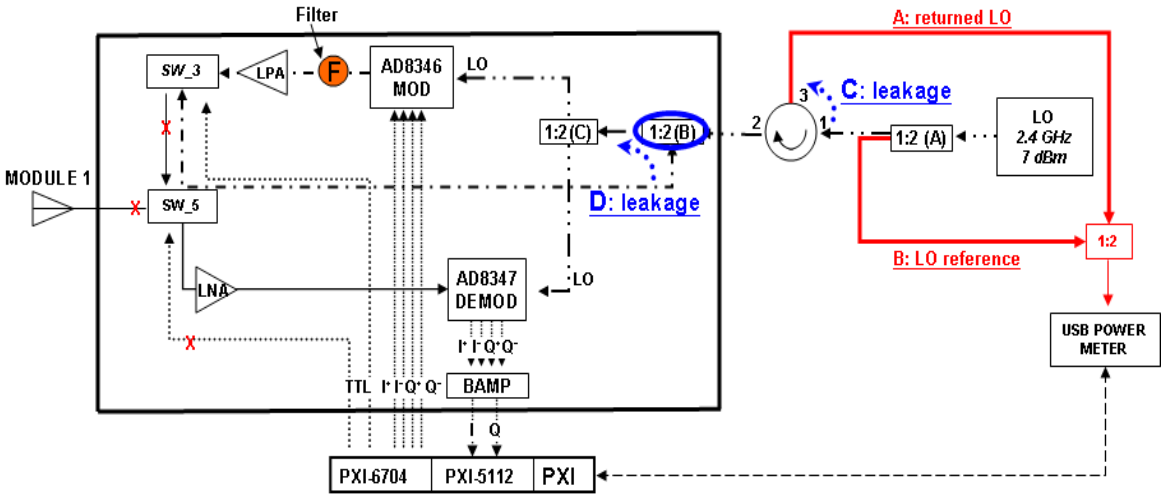


Figure 55. Illustration of possible LO power leakage occurred in the setup of the T/R module

Therefore, in order to eliminate the effect of the unstable power measurement caused by leakage (D), increasing the LO source power is a possible solution. However, the power leakage (C), occurring in the areas of port 1 to port 3 of the circulator, becomes larger.

On the other hand, to lower the LO source power to decrease the leakage (C) will cause the leakage (D) to be relatively higher with respect to the input LO power. Note that the leakage (D) will mix with the original LO input passing through the AD 8346 modulator and the LPA causing the synchronization circuit to behave as a feedback system. Since it forms a closed loop, this causes instability of the LO power level.

Ryu described the phenomenon as the “dilemma” of the synchronization process. Figure 56 shows the typical distortion due to the LO power leakage. The most obvious characteristic is the asymmetrical shape. The approximate maximum located is 225 degrees and the minimum is approximately 20 degrees, not 180 degrees apart. However, the shape can possibly be in error yet still be symmetric, and this is why a thorough examination of the synchronization circuit is needed.

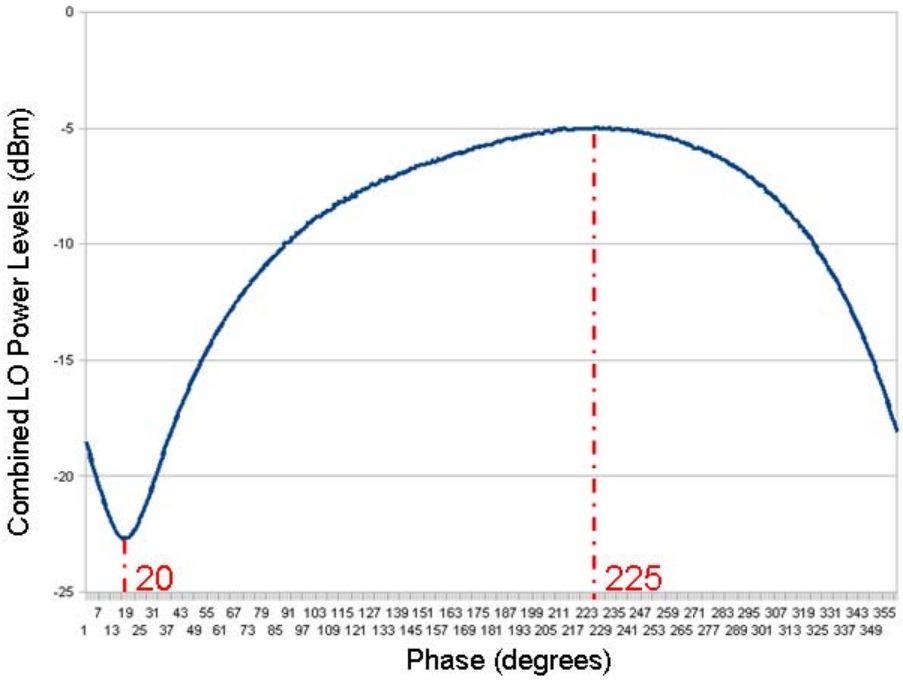


Figure 56. A typical distortion of the shape of the combined LO power level

2. Analysis of LO Power Balance

Due to the sensitive nature of the LO power in the synchronization circuit, an adequate power balance arrangement can effectively improve the performance of the synchronization circuit. This can done by implementing proper attenuation after LPA and adjusting LO source power to balance the LO power leakage in the circuit.

Figure 57 shows the comparison of the circuit before and after implementing 8 dB attenuation. Compared to the shape before the power balance, it is obviously much more symmetrical. The asymmetry has been eliminated to a negligible level; the depth of the notch, however, is also decreased from 23 dB to 13 dB.

The LO power balance is one approach to decrease the effect of LO power leakage. However, balancing the LO power level in the circuit might not be practical in the future synchronization operation due to the wide range of power levels that will be encountered. The cancellation of LO power leakage will be more effective, and this will be addressed in Chapter IV.

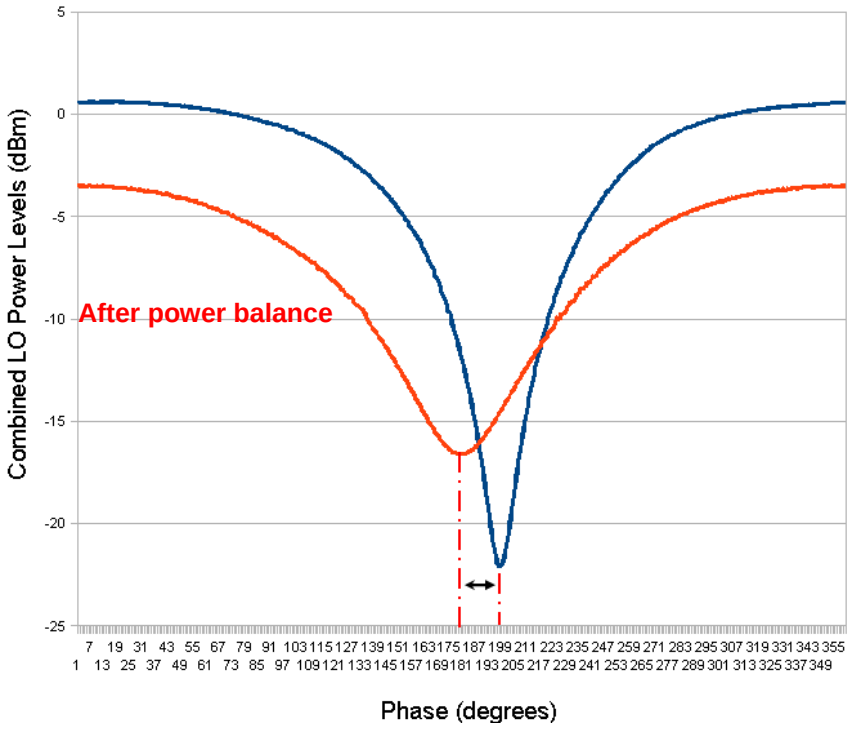


Figure 57. The comparison of the circuit before and after implementing 8 dB attenuation

3. Validation of LO Power Balance

The addition of a 3 dB quadrature coupler is used to examine signals in T/R module 2 after balancing the LO power level. Figure 58 shows that the null at 55 degrees is shifted by approximately 85 degrees to 140 degrees.

As a more general test, the phase shifter is applied to be sure the phase can be shifted to the right location. Figure 59 shows the phase shift after six complete turns of the phase shifter. As stated in last section, for the applied phase shifter, every six complete turns gives the phase approximately 33 degrees of phase shift. In this case, the phase is shifted from 217 degrees to 283 degrees, which is in accordance with the expected.

Due to the nature of instability of LO power found in T/R module 2, any change of the implemented hardware components requires rebalancing of the LO power as demonstrated in the change of notch depths in Figures 58 and 59.

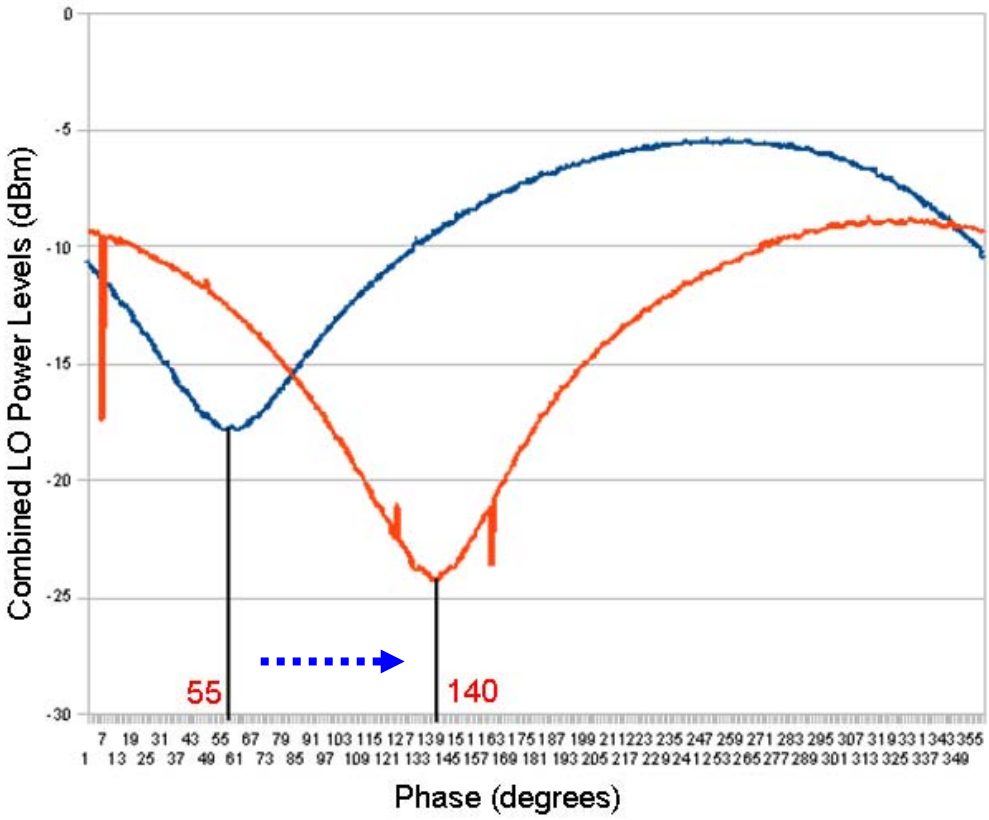


Figure 58. Phase shift after implementing 3 dB quadrature coupler

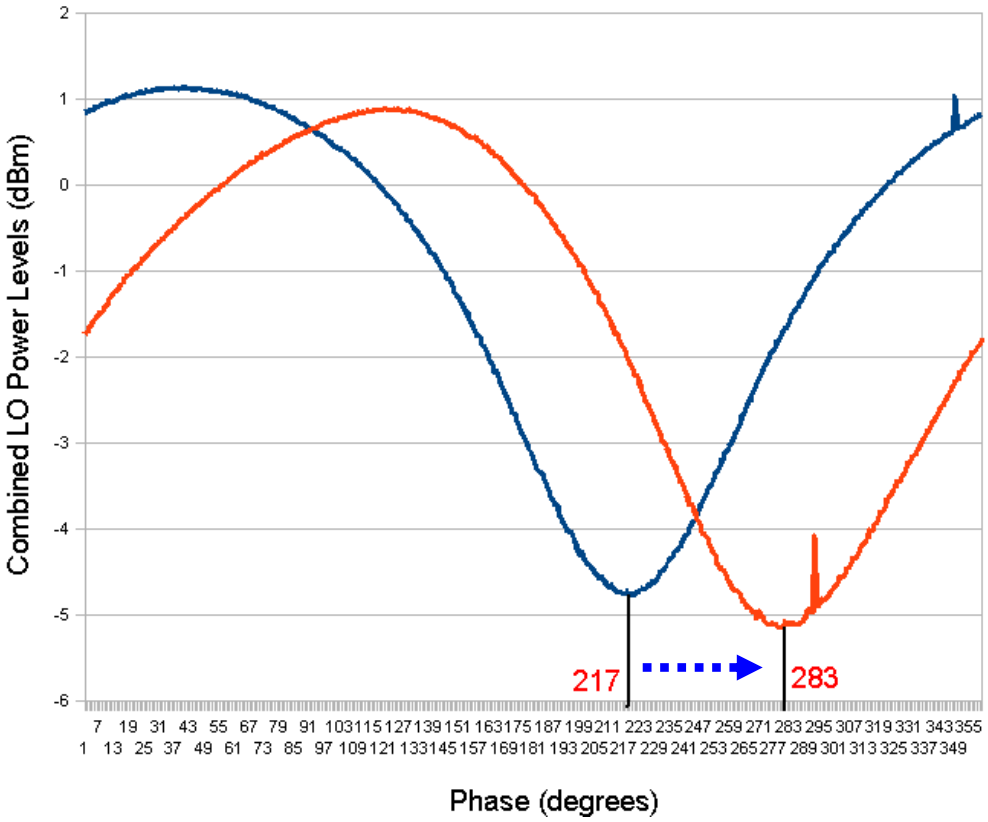


Figure 59. Phase shift after six complete turns of the phase shifter

4. Two-element Testing

Figure 60 shows the two T/R modules. To optimize the synchronization circuit, the LO power in the modules must be balanced. Therefore, a 1 dB/step variable attenuator, as shown in Figure 61, is implemented in T/R module 2.

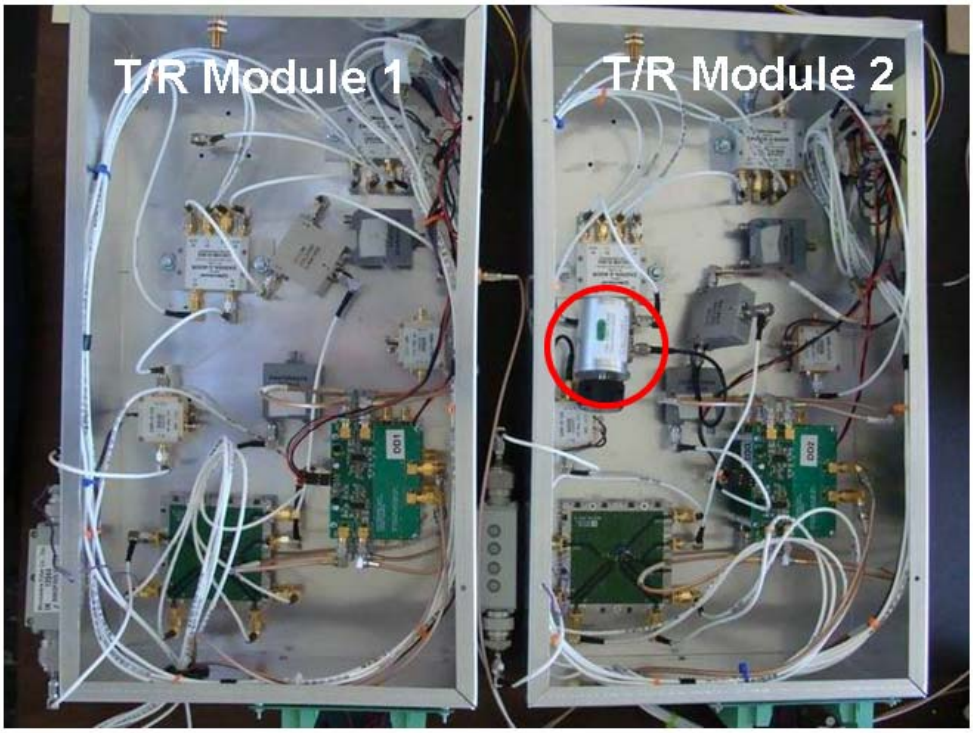


Figure 60. Configuration of T/R module with the 1 dB/step variable attenuator highlighted

Figure 61. The 1 dB/step variable attenuator implemented in T/R module 2

Figure 62 shows the block diagram of the two-element setup. Note that two attenuators are placed in the circuit to optimize the shape of the combined LO power. They can also be used to simulate variations in the free space path loss for the wireless synchronization.

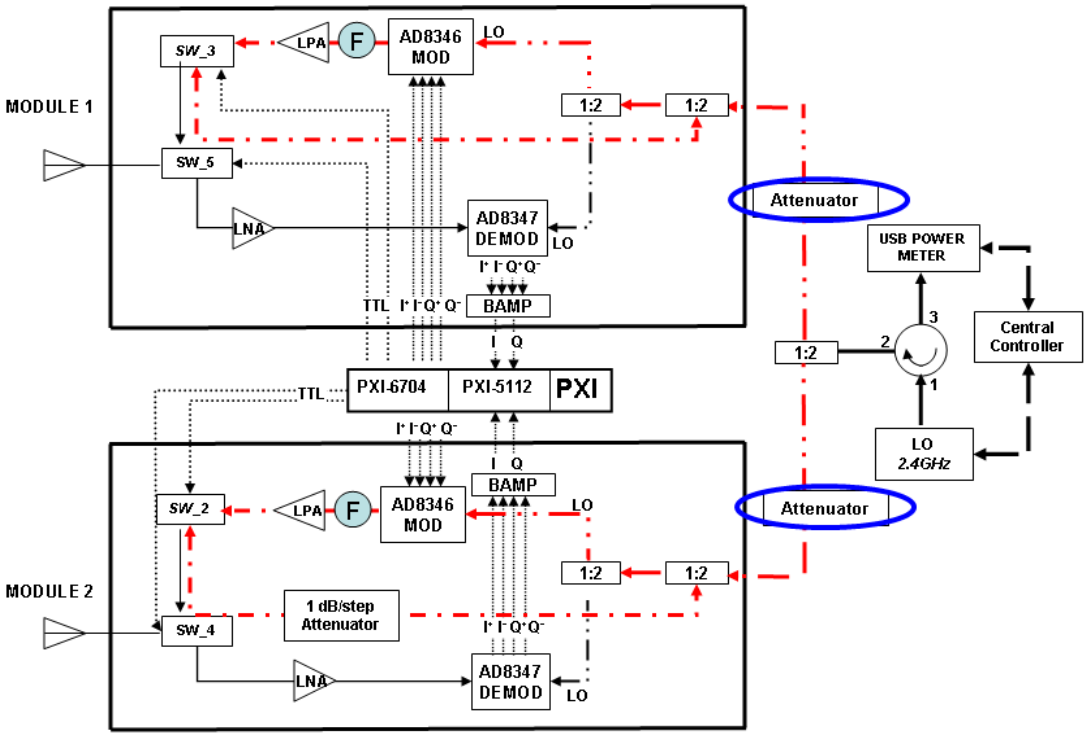


Figure 62. Configuration of two-element testing setup

T/R module 1 is selected to be the master element and T/R module 2 is the slave. The master element maintains the same phase, while the slave element steps through 360 degrees. Figure 63 shows the results with the phase of the master element set at 0, 90, and 180 degrees. Note that the waveform moves the proper direction with approximately 90 degrees per step. This means the synchronization process for this two-element setup is capable of detecting the shifted phase.

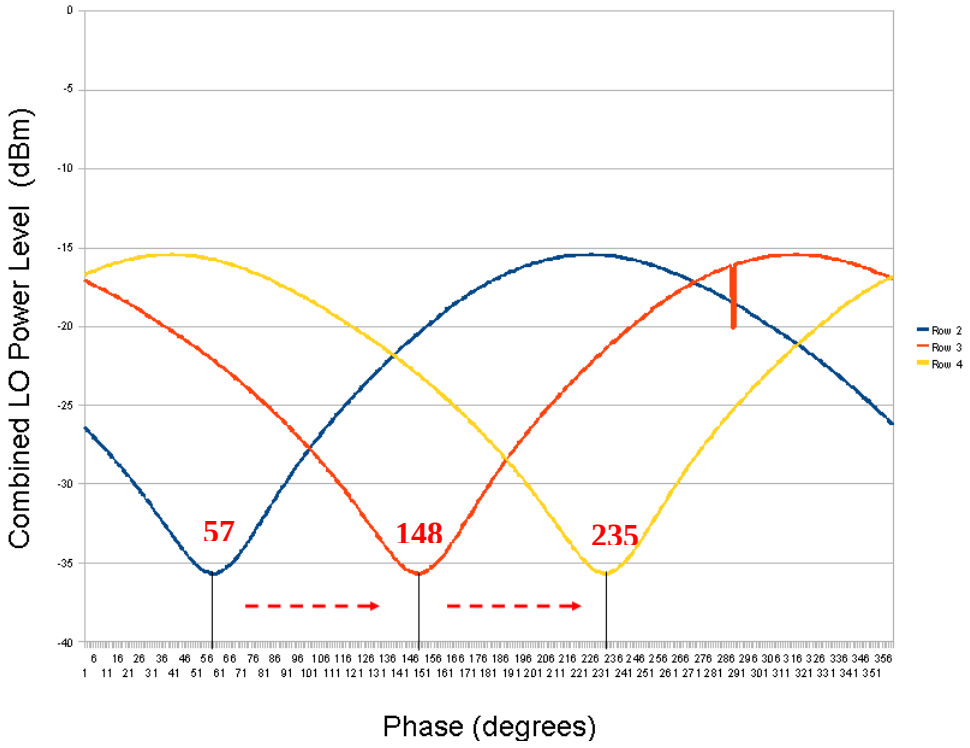


Figure 63. Phase shifted by operating beamforming control of the master element

F. SUMMARY

In this chapter, a series of wired synchronization experiments were discussed. The synchronization operation was verified and validated through a series of tests with one and two modules. The spurs were observed to affect the performance of the synchronization circuit. An MFC-13944 filter was implemented to eliminate spurs and was proven effective.

The insufficient isolation of the circulators and power dividers caused inaccuracy of the shifted phase measurements. Balancing the LO power in the circuit by implementing a variable attenuator proved to be effective in improving the performance. However the solution does not fundamentally resolve the distortion.

Wired two-element testing was successfully completed. To optimize the shape of the signal power curve, two attenuators were implemented in the paths to the USB power sensor. The phase was shifted to the expected locations.

In this chapter problems with the synchronization circuit were diagnosed, corrected and then validated. The performance of the demonstration array is considered satisfactory. Next, to carry on the development of WDDPA, the wireless synchronization operation will be validated in Chapter IV.

IV. DEVELOPMENT OF WIRELESS SYNCHRONIZATION

A. BACKGROUND

Measurements and results from the experiments in Chapter III verified that the phase synchronization process of the hardwired LO distribution is viable. The signal paths between the modulator and controller were represented by coaxial cables. Several measures have been discussed to improve the shape of the returned signal power curves, and they will be applied in the subsequent tests. The focus of this chapter is to validate wireless synchronization operation.

Compared to the hardwired LO distribution, wireless phase synchronization has to take free space propagation loss into consideration. The wireless configuration shown in Figure 27 in Chapter II was tested to evaluate the performance of the current synchronization circuit.

B. WIRELESS SYNCHRONIZATION DEMONSTRATION

1. Investigation of Free Space Propagation Loss

Stubby antennas in [21]-[22], [31], as shown in Figure 64, continue to be used as the LO antennas for the two modules.

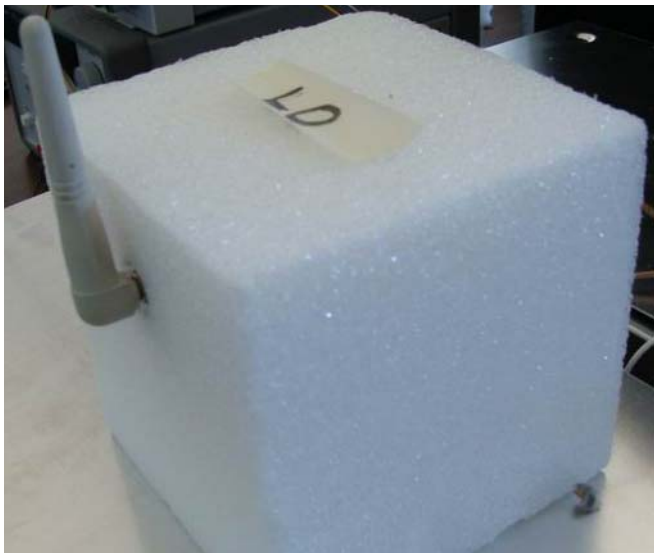


Figure 64. The stubby antenna implemented in the wireless synchronization testing

Figure 65 shows the insertion loss between two stubby antennas (each with the coaxial cable) separated 50 cm as measured by the Network Analyzer. The loss is approximately –31 dB. For 13 cm, which will be the configuration applied later in this chapter, the loss is approximately 18 dB.

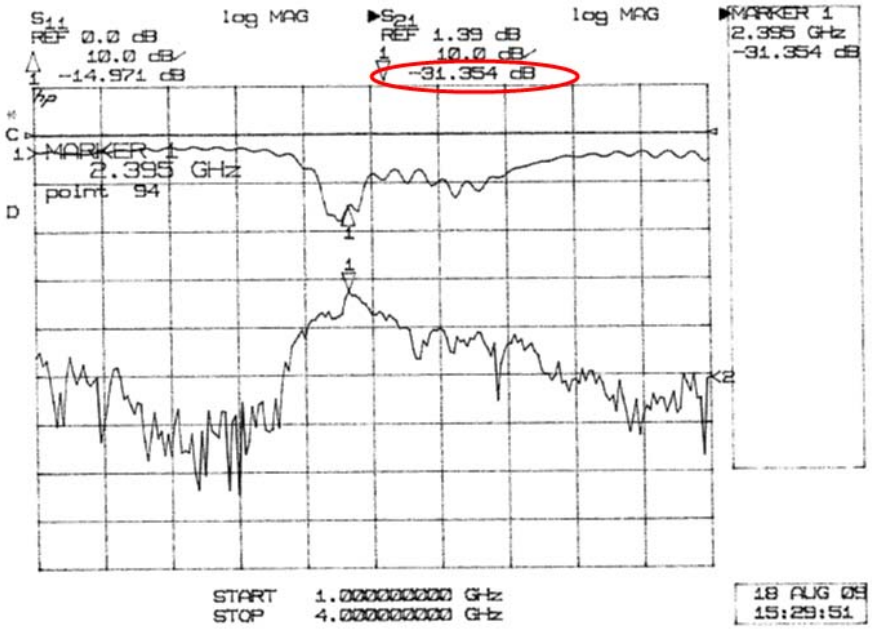


Figure 65. The system loss of two stubby antennas placed 50 cm apart

In order to scale the power for free space, a set of attenuators were added to the hardwired two-element configuration as shown in Figure 66. Two attenuators were individually inserted in the paths of the wired LO distribution. Based on the propagation loss of the antennas, 30 dB and 40 dB were implemented in the paths of the wired LO distribution. In order to prevent distorted signal power curves, LO power balance as discussed in Chapter III was applied in both modules.

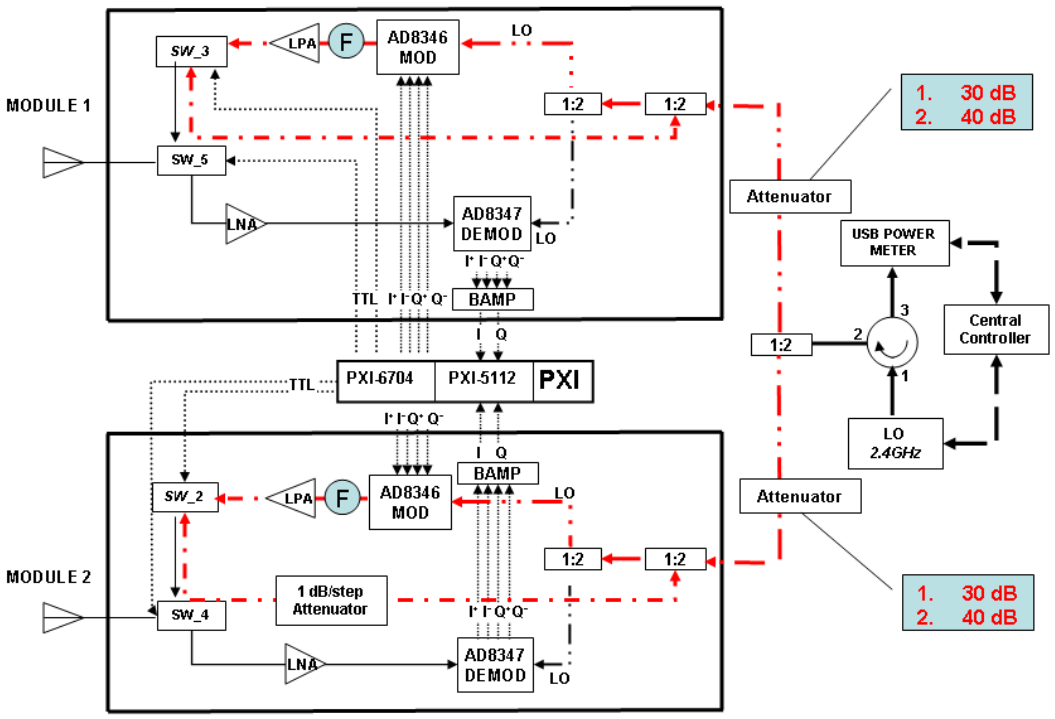


Figure 66. Configuration of attenuation implemented in the route of the wired LO distribution

Figure 67 shows the result for the 30 dB attenuation. The returned power level can be as low as –47 dBm. The depth of the notch is approximately 22 dB down. The null is not as clear as the previous setups because the LO signal is so low that the noise power can interfere with the shape of the curve.

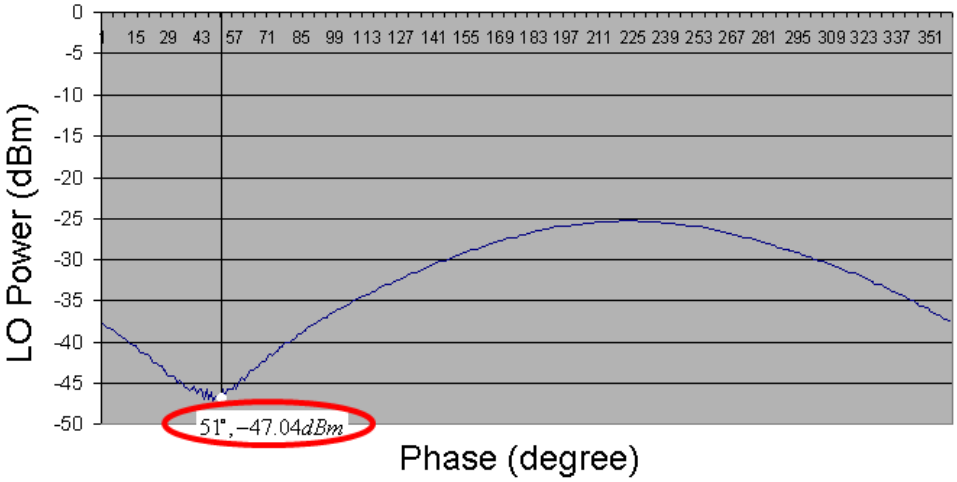


Figure 67. The curve of the 30 dB attenuator implemented in the circuit with the null highlighted

Figure 68 shows the null region from 43 to 58 degrees. The null is filled with noise and is flat over approximately 15 degrees. If the center is taken as the null location, it is within the range of 20 degrees, which is sufficient for the WDDPA synchronization operation.

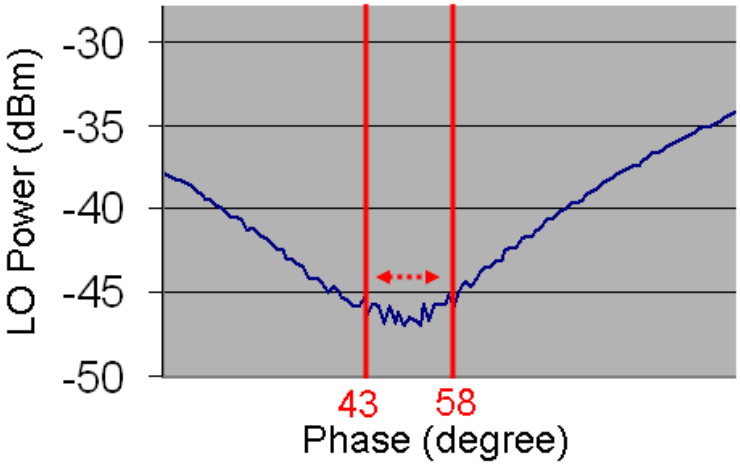


Figure 68. The null region of the 30 dB attenuator implemented

Figure 69 shows the curve after inserting 40 dB of attenuation in the path. Because the returned signal power level is very low, the notch is filled by the noise. The null is extremely difficult to locate, so the shifted phase cannot be detected accurately. This will be a potential problem in the wireless synchronization operation.

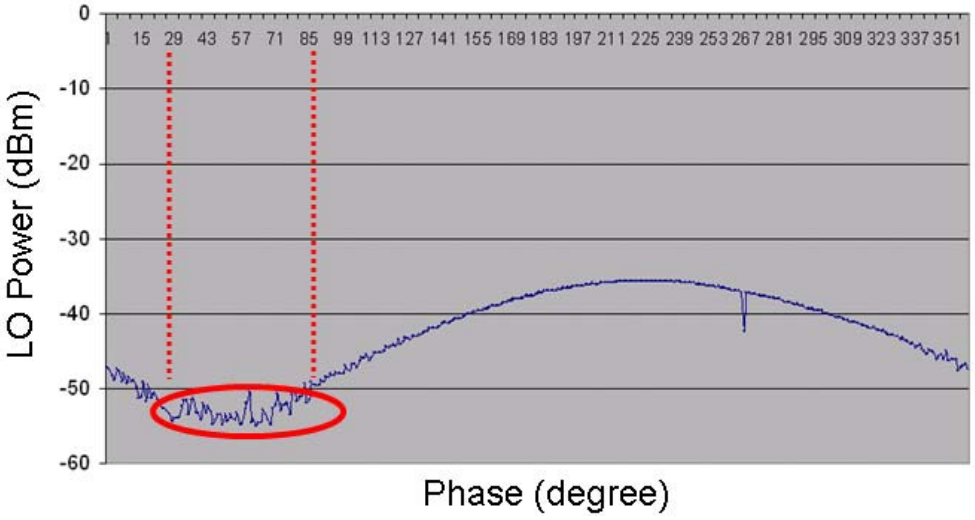


Figure 69. The curve of the 40 dB attenuator implemented with the obscure region highlighted

Processing can reduce the problem. Figure 70 shows a plot of the moving average line in Microsoft Excel or other similar software. It can improve the distorted curve and provide an approximate location of the null.

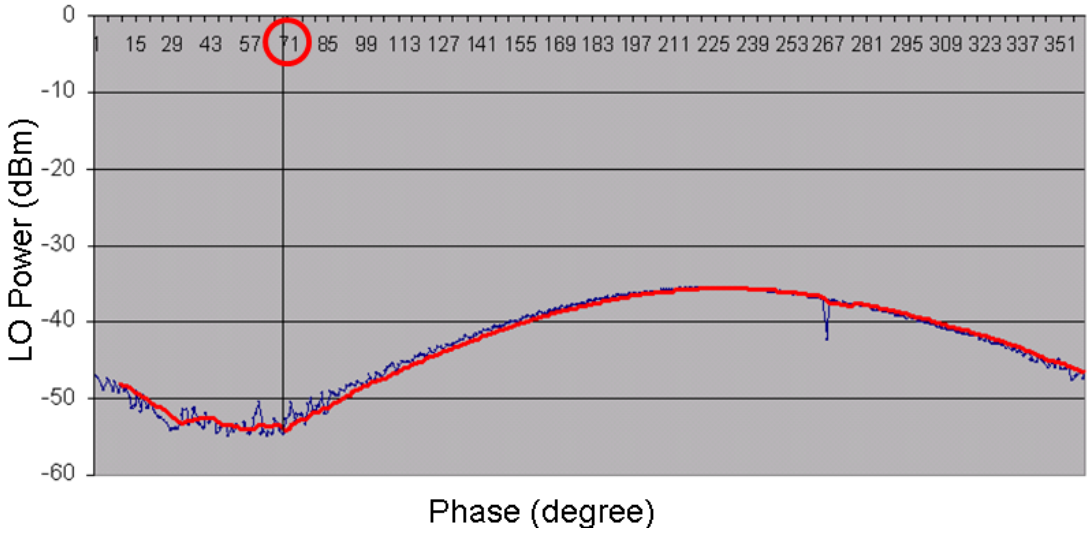


Figure 70. The estimation of the null with 10 points moving average line highlighted

This simple setup reveals a potential problem: free space propagation can dramatically decrease the SNR, leading to the difficulty of locating the shifted phase. Because of the low signal power level, any interference can easily distort the curve of the

returned signal power. Therefore, the controller must increase the TX power level for elements that are distant relative to those that are nearby.

2. Demonstration of Wireless Synchronization Operation

The setup for the wireless synchronization is shown in Figure 71. Considering the free space channel and the signal power budget, the stubby antennas are placed 13 cm apart. The propagation loss is approximately 18 dB. The LO output is 10 dBm, which is the maximum output power that Lab Brick can transmit. The circulators are used in place of the power dividers for the lower insertion loss. With the modified setup, the signal input power at the LOIN port of the AD 8436 board is measured as −12 dBm, which is in the operating range of the modulator board.

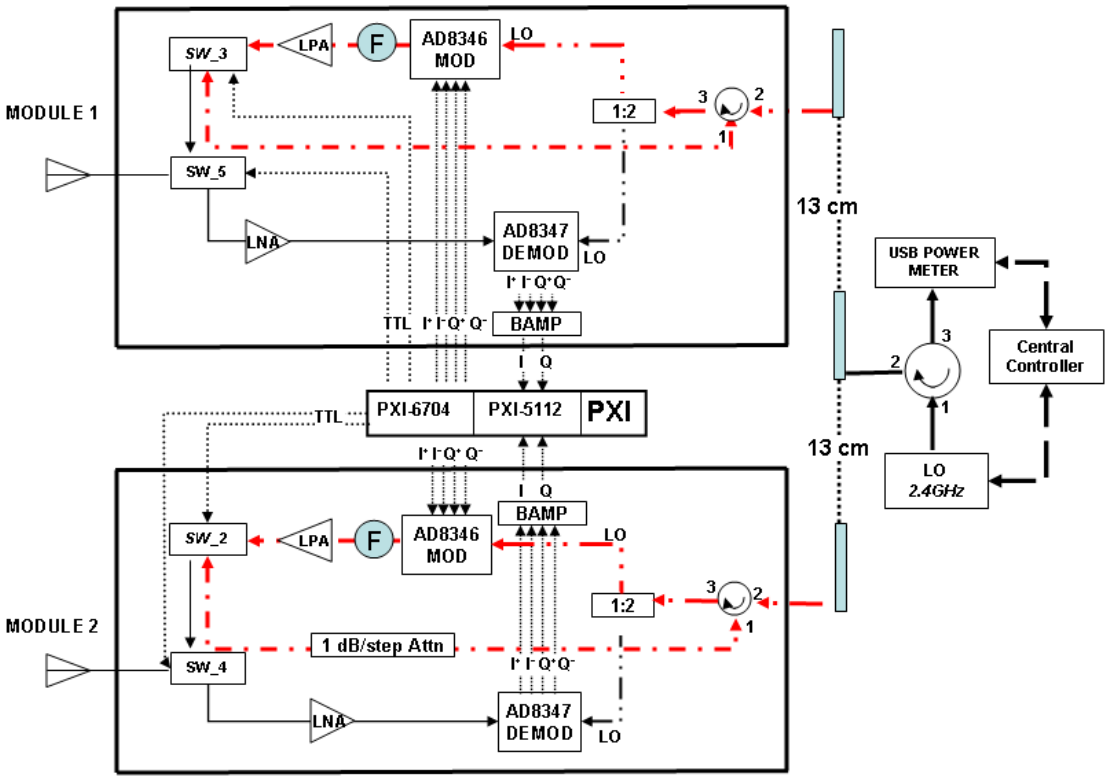


Figure 71. The simplified WDDPA diagram of the wireless synchronization operation

Module 1 is selected to be the slave element. The phase is stepped through 360 degrees at the slave while the master element (module 2) has a fixed phase set at 0, 90,

180 or 270 degrees. The power sensor enables the central controller to display the graph of the phase shift versus the returned signal power level. Therefore, there should be four curves displayed in the graph. If the null of the each curve can be shifted by 90 degrees (or within 20 degrees tolerance range), the synchronization circuit is considered operating successfully.

Figure 72 shows the result of the experiment. The shapes of all power curves are distorted similarly. There is almost no phase shift that can be observed in the graph. The null cannot be located from the curve. The result shows that the design of the current circuit is not capable of executing the synchronization process. Therefore, a more detailed analysis of the associated problems is necessary, and it is presented in the next section.

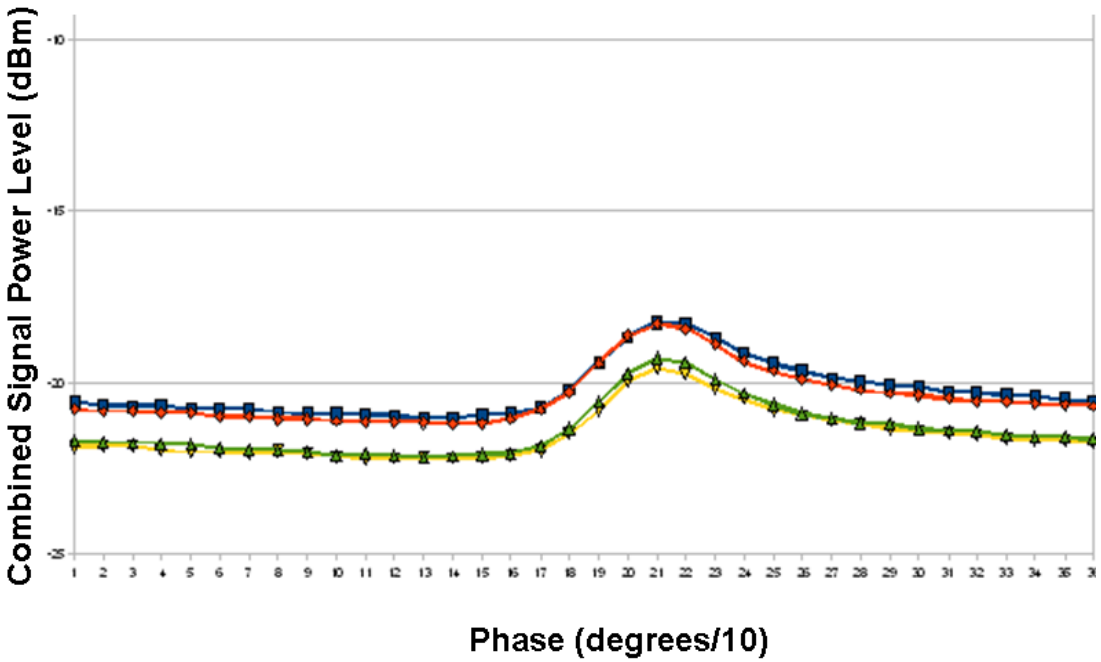


Figure 72. The power curves of the phase of the master element set at 0, 90, 180 and 270 degrees

C. ANALYSIS

From the experiments, two factors are recognized that cause the distorted power curves: (1) LO power leakage and (2) spurious signals.

1. LO Power Leakage

In Chapter III, the LO power leakage occurring in the synchronization circuit of the individual T/R module was discussed. In the single-element testing, the power leakage occurs not only in the T/R module but also in the circulator at the controller in connection with the USB power sensor.

The same situation occurs in the wireless synchronization testing. Furthermore, it dominates the distorted shape of the curves as shown in Figure 72.

Figure 73 shows two types of leakage in the wireless synchronization setup. The effect of the leakage (D) still exists in both of the T/R modules. The leakage (E) is similar to the leakage (C) in Figure 55.

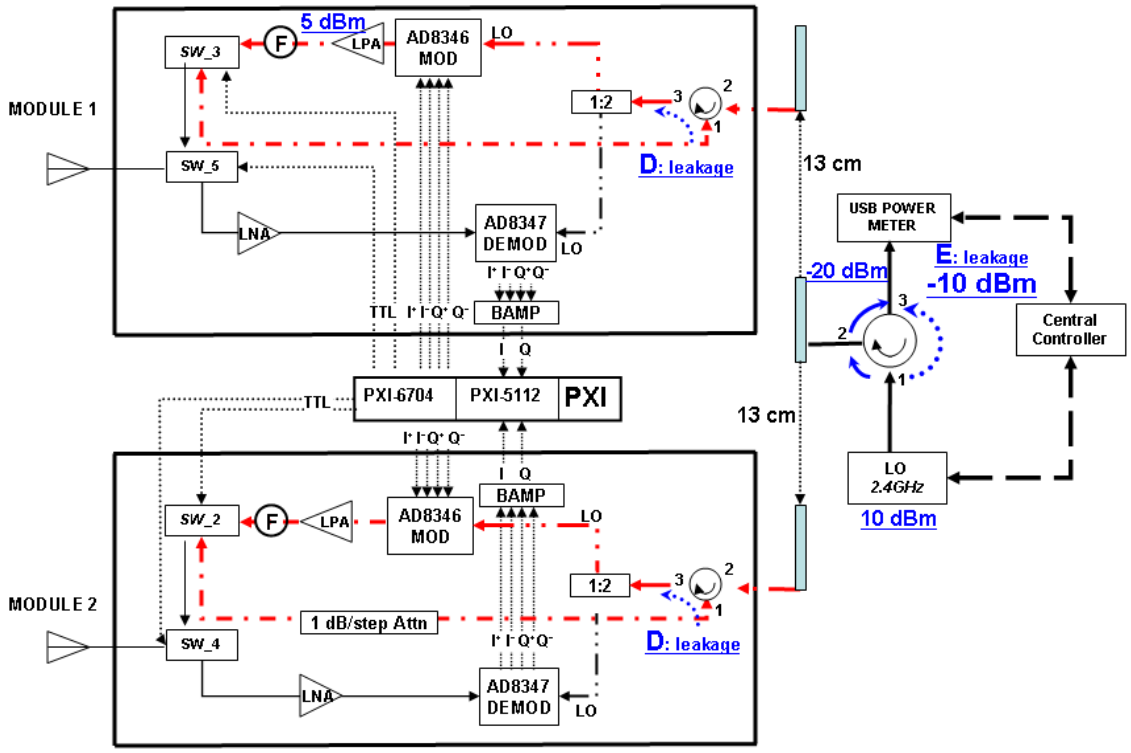


Figure 73. Illustration of LO power leakage occurring in the wireless synchronization setup

Previously, the power leakage was decreased to a negligible level by balancing the distributed LO power in the wired synchronization testing. In the wireless testing, the received LO power level, lower than –20 dBm, is relatively small in comparison to the 10 dBm output power of the LO source.

The power leakage (E) is approximately −10 dBm through the circulator because the isolation of the circulator is –20 dB. Accordingly, the leakage (E), −10 dBm, is much larger than the received signal power. The phase shift of the slave element cannot be detected by the comparison algorithm of the central controller.

2. Spurious Signals

On a spectrum analyzer, the spurs shown in Figures 74 and 75 are observed while the amplitude of the beamforming control signal is maintained at 2 V (the same as in the wired synchronization testing).

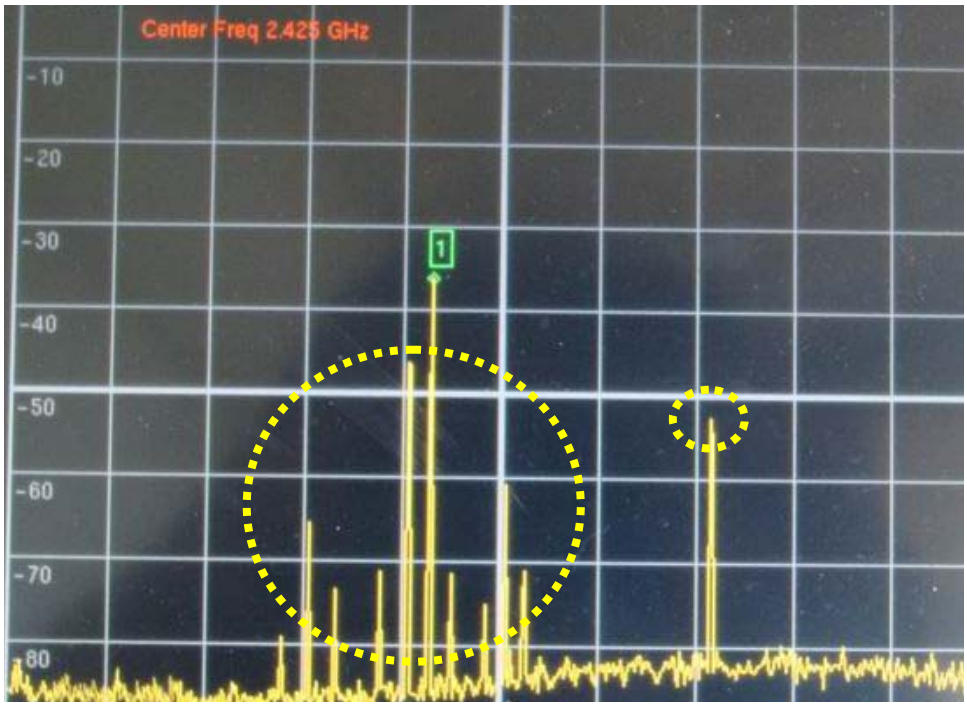


Figure 74. The highlighted spurs

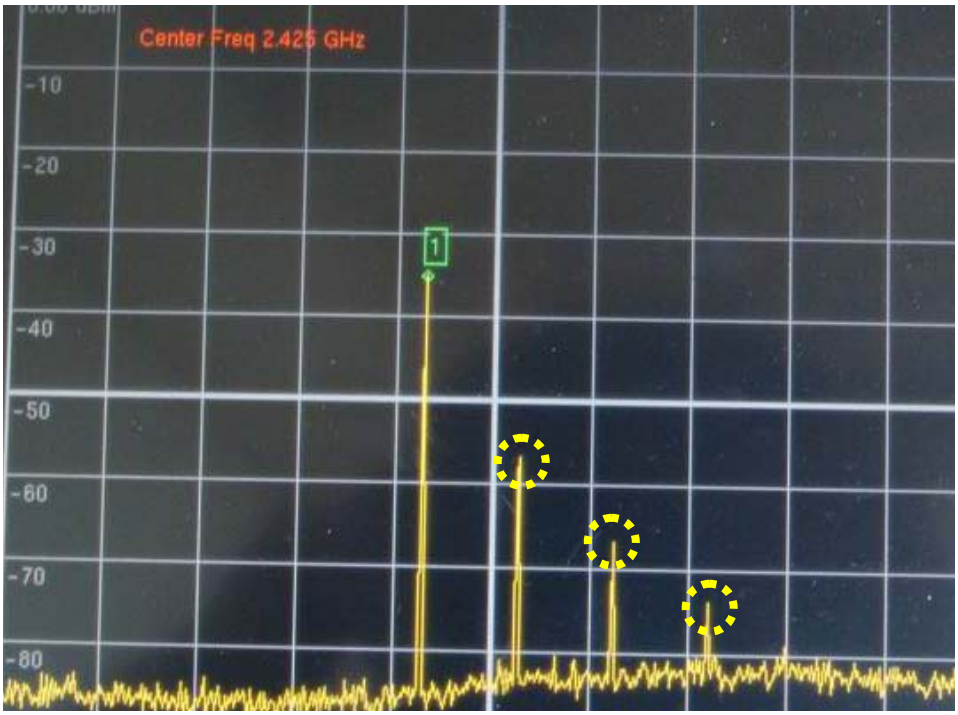


Figure 75. The different type of spurs

Variations in the spurs were observed when the amplitude was set to more than 1.2 V. When the amplitude is set higher, more spurs are generated in relation to the amplitude. After several trials, it was found that when the amplitude is lower than 1.2 V, no spurs are observed.

Spurs occurring in the wireless testing behave differently than the ones in the wired synchronization testing in Chapter III. The spurs occur within the bandwidth of the MFC–13944 filter, so they are not suppressed by the filter. Therefore, they affect the modified LO signal power level.

To eliminate the spurs and improve the shape of the power curves, the amplitude was set at 1.2 V in the subsequent wireless synchronization tests.

D. IMPROVEMENT IN SYNCHRONIZATION OPERATION

With the analysis of the probable causes of the curve distortion, some measures are proposed to improve the performance of the synchronization circuit.

1. Leakage Power Cancellation Circuit

As discussed in the last section, the LO power leakage occurring in the circulator connected to the USB power sensor affects the accuracy of the received signal power level dramatically. The LO power balancing in the synchronization circuit is not sufficient to eliminate the effect. Therefore, the leakage power cancellation circuit shown in Figure 76 was proposed by Ryu to improve the performance of the synchronization operation.

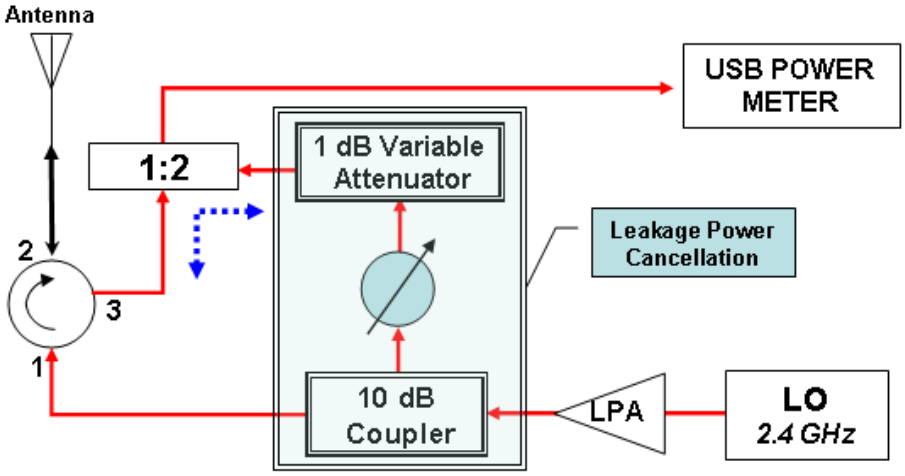


Figure 76. Diagram of the leakage power cancellation circuit

Figure 77 shows the hardware components implemented in the wireless synchronization testing.

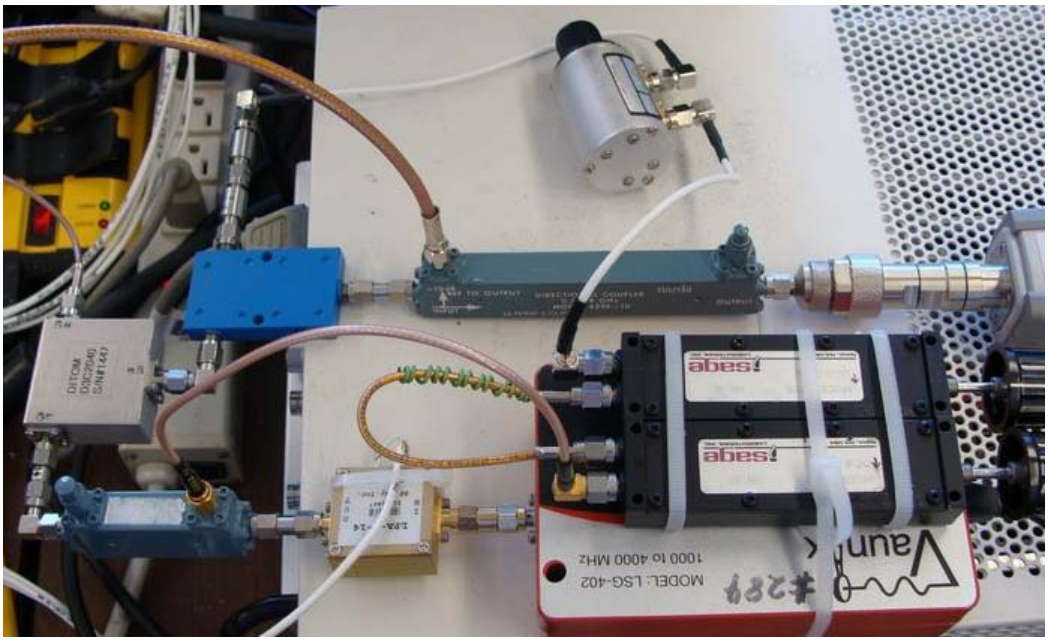


Figure 77. The appearance of the implemented leakage power cancellation circuit

The purpose of the 10 dB coupler is to redirect some of the output power of the LO source. The phase shifter adjusts the cancellation power to be the opposite phase of the leakage signal. The variable attenuator adjusts the signal amplitude. With the adjusted amplitude and phase, the cancellation signal is generated to eliminate the leakage signal. Ideally, with the cancellation signal, there will be no effect from the LO leakage.

In reality, it is not possible to eliminate all the leakage, because other signals are combined with the leakage signal. Figure 77 shows two other main factors affecting the leakage signal: (a) antenna mismatch and (b) reflection from the outside environment.

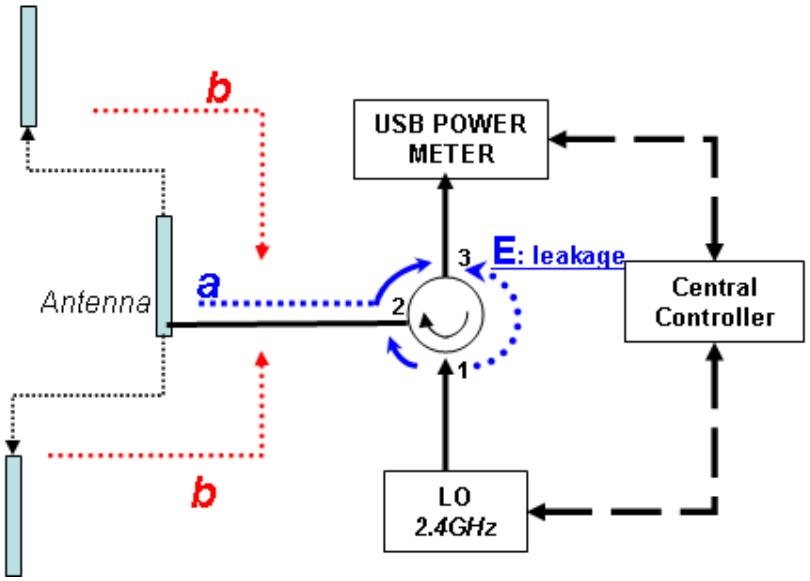


Figure 78. Two main factors affecting the leakage signal: (a) antenna mismatch and (b) reflection from outside environment

These two factors play important roles in the cancellation of the leakage. For discussion, these signals will also be called “leakage signals.” The cancellation signal is supposed to have the same amplitude and phase as the leakage signal. Because of the other two contributors, generation of an ideal cancellation signal is not possible.

However, meeting the goal of the reducing the effect on the received signal power does not require an ideal cancellation circuit. According to the experiment, if the leakage signals can be reduced to approximately –50 dBm, the desired signal components primarily determine the power curves. With the implementation of the power cancellation circuit, Figure 79 shows the leakage power levels are reduced to –65 dBm, which is sufficient for the current wireless implementation.

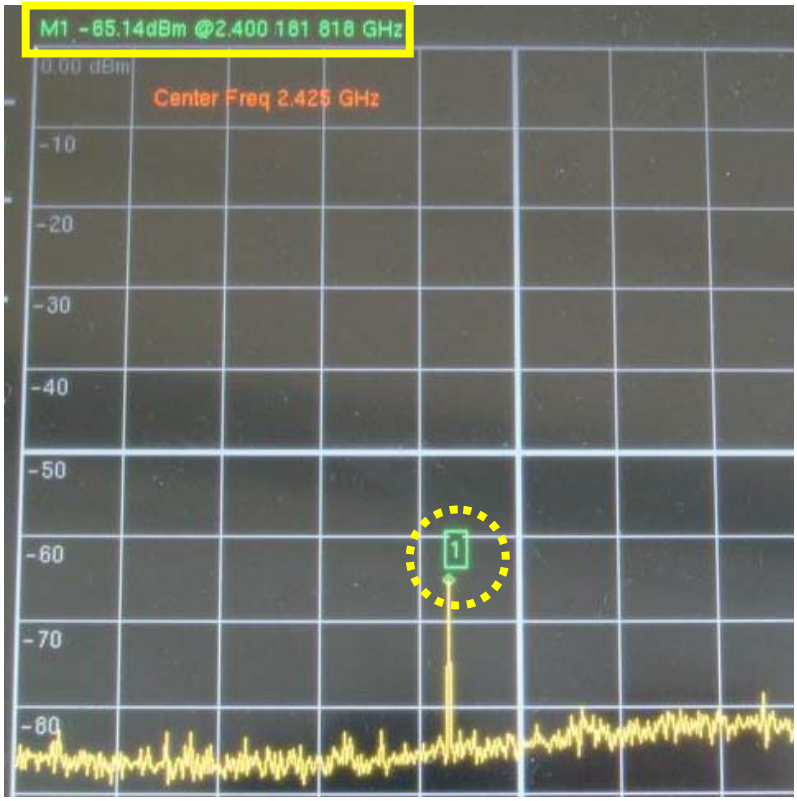


Figure 79. The reduced leakage signals with power level of −65 dBm highlighted

2. Implementation of the LPA

The cancellation circuit has some insertion loss, which could cause insufficient signal power level at LOIN of the AD 8346 modulator board. Therefore, an extra LPA is required to improve the power budget.

Figure 80 shows the improved two-element WDDPA demonstration array. Note that the output power of the LO source is 0 dBm, which enables the LO input power at the AD 8347 board to be −12 dBm (within the operation range). The distributed LO power is balanced in the demonstration array.

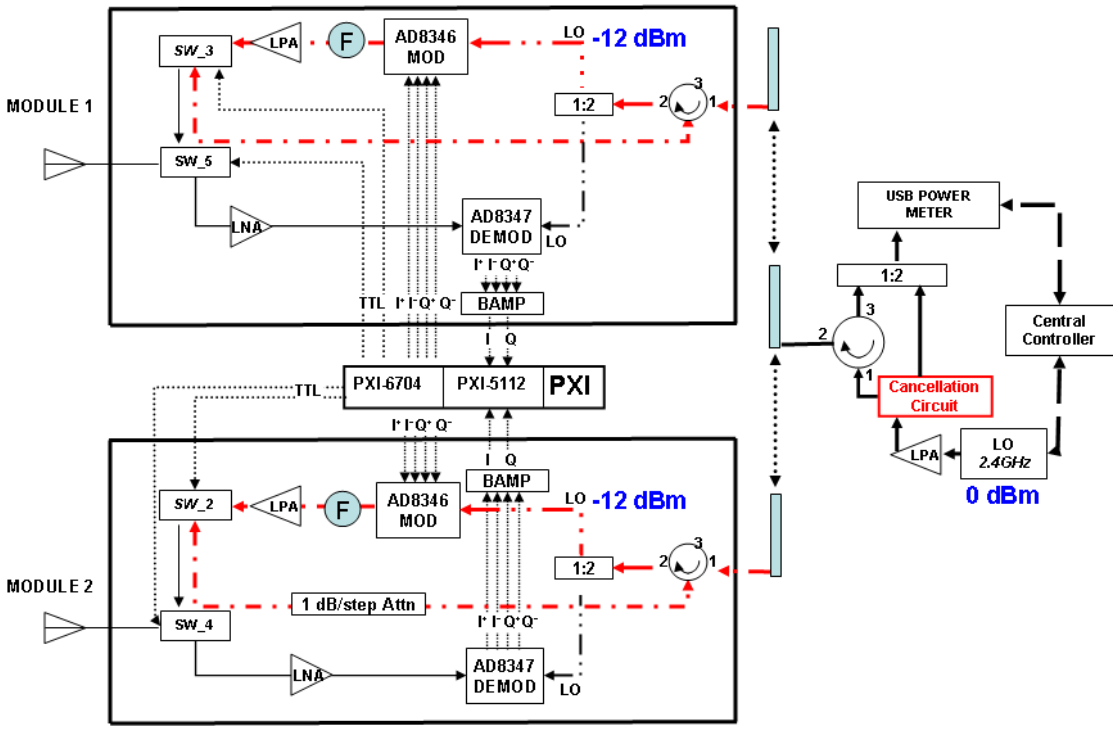


Figure 80. The improved two-element WDDPA demonstration array

E. THE MODIFIED TWO-ELEMENT WIRELESS TESTING

With the improved two-element setup, the test is conducted by stepping through 360 degrees of phase at the T/R module 1 when T/R module 2 has three fixed phases set at 0, 90 and 270 degrees. If the nulls of the curves can be shifted by 90 and 180 degrees (or within 20 degrees), the circuit is proven to be capable of operating successfully. Figure 81 shows the results of the experiment.

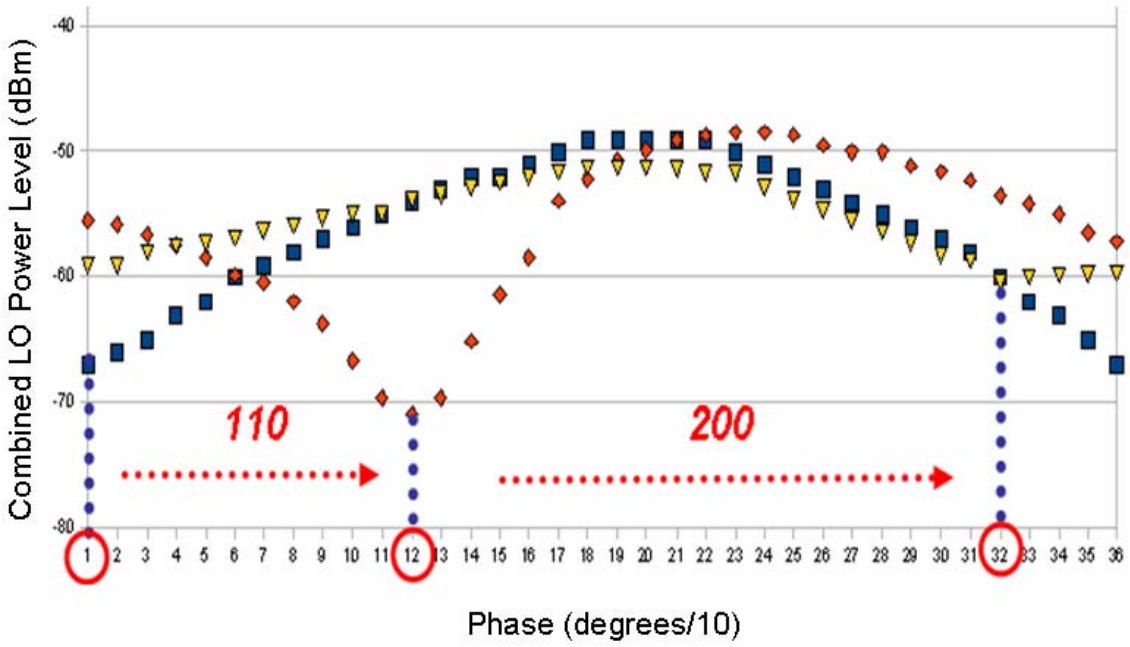


Figure 81. The curves of the phase of the T/R module 2 fixed at 0, 90 and 270 degrees

The null of the first curve is at 10 degrees, which is the curve of T/R module 2 set at 0 degrees. The next curve shows the phase of T/R module 2 fixed at 90 degrees. The phase difference between these two curves is approximately 110 degrees, which is within tolerance for synchronization. The null of the last curve is at 320 degrees, which is 200 degrees shifted from the last curve. The phase shift is maintained within tolerance of the required WDDPA synchronization operation.

Note that the depths of the notches vary. Some of the curve notches can be as deep as 22 dB while some are less than 10 dB because once the phase of the master was changed, the amplitude of the individual signal components changed. As the amplitude imbalance increases, the depth will decrease, as discussed on pages 62 and 63 in Chapter III.

Several similar experiments with the different phase shifts were conducted to ensure that the synchronization circuit would work for all phase shifts. Figure 82 shows

data for T/R module 2 set at three fixed phases of 0, 90, 135 and 330 degrees after balancing the distributed LO power in the T/R modules. Table 8 summarizes the test results.

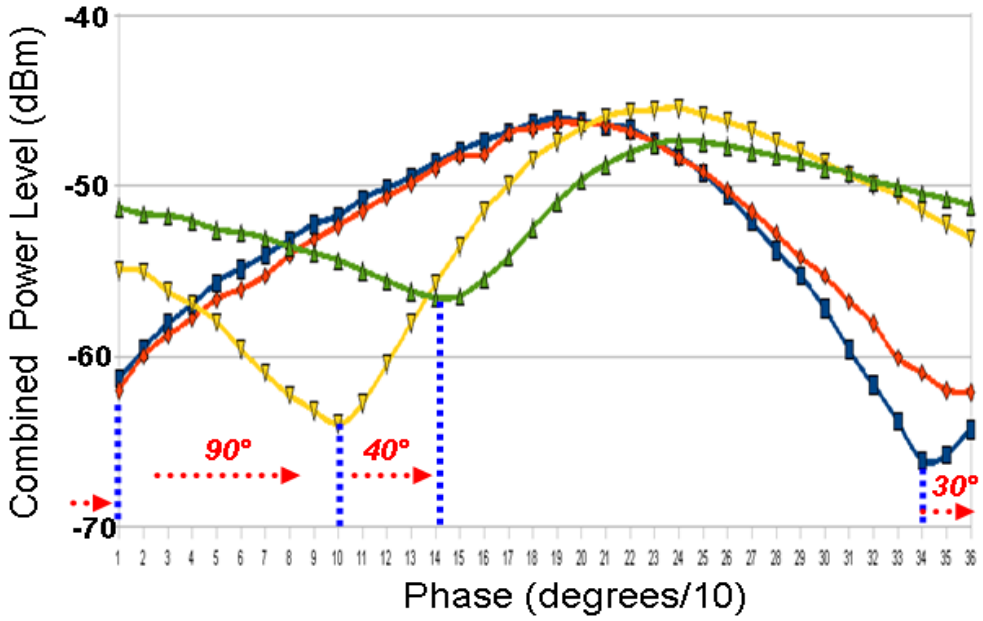


Figure 82. The curves of the phase of the T/R module 2 fixed at 0, 90, 135 and 330 degrees

Phase of the master	Null of the Curve	Phase Shift	Error
330	340	-30	0
0 (reference)	**10**	**0**	**0**
90	100	90	0
135	**140**	**40**	**5**

Table 8. The summarized test results (in degrees)

The measurement was taken every 10 degrees by observing the received signal power level from the spectrum analyzer. The error was within five degrees of the expected values as shown in Table 8.

Although the shapes of the power curves were slightly distorted in some cases, the nulls were still able to be located. Note that the depth of the each notch varies. In this case, when the phase of the master element is set between 180 and 270 degrees, the depth can be less than 5 dB unless the amplitude of the beamforming control signal is modified in order to balance the signal powers.

Overall, the results show that with the hardware modifications in the WDDPA demonstration array, the wireless synchronization operation is successfully validated and verified.

F. SUMMARY

This chapter focused on the validation of the WDDPA wireless synchronization operation. The wireless synchronization was continued from the wired case. It was found that leakage signals from non-ideal devices and spurious signals affected the performance of the synchronization circuit.

The implementation of the cancellation circuit eliminated the effect of the leakage signals at the controller. The reduction of the modulator amplitude of the beamforming control signal prevents the spurious signals. With the additional LPA, the distributed LO power can overcome the free space path loss and is still sufficient to drive the AD 8346 modulator board.

The new configuration is then applied to examine the performance of the modified synchronization circuit. The result shows that the two-element wireless synchronization operation is effective. The distorted curves as shown in Figures 83 and 84, taken from [21]-[22], were improved to a satisfactory level, as shown in Figure 82. The circuit configuration for these plots is similar to Figure 71. The performance of the new circuit meets the goal of validating the synchronization operation for the WDDPA.

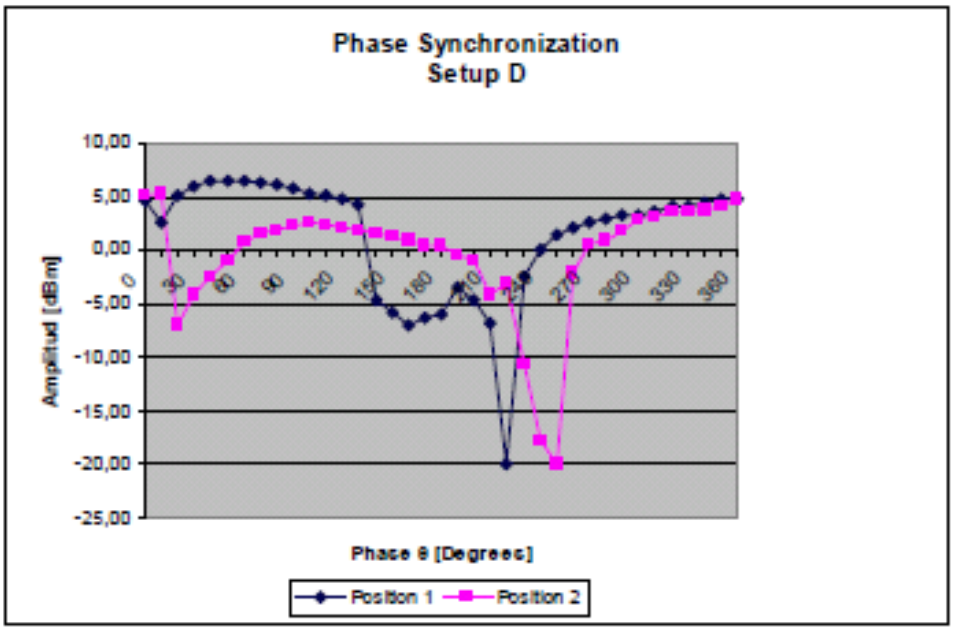


Figure 83. The distorted power curves of the setup D in [21] (From [21])

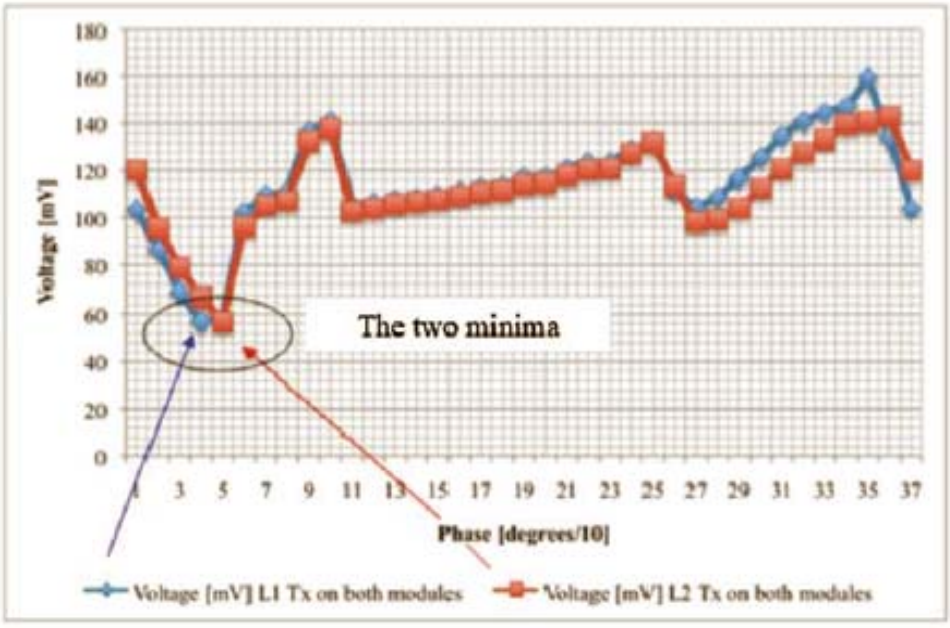


Figure 84. The distorted curves of the phase synchronization testing in [22] (From [22])

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V. CONCLUSION AND RECOMMENDATIONS

A. CONCLUSIONS

The focus of this paper was to improve the performance of the synchronization circuit based on the same "brute force" concept of searching for a null in the summed fields of a master and slave. Hardware changes from the previous FPGA system to the single PXI controller, and the corresponding software modifications, were completed to enhance the accuracy and speed of the phase synchronization. Two stages of the validations were the hardwired configuration and the wireless configuration.

The fundamental measurement of the WDDPA synchronization operation is to display the graph of combined signal power versus module phase shift. In the initial hardwired single-element synchronization testing, numerous spurious signals were observed in the circuit, affecting the distributed LO power stability. Therefore, the distorted power curves due to the unstable LO power make it difficult to locate the null. The implementation of the MFC-13944 filter successfully eliminated the spurs.

Next, experimentation moved to two-module testing. In two-module testing, the central controller runs a phase comparison algorithm, combining the master's reference signal and a returned LO signal from the slave. The process is repeated by stepping through 360 degrees of phase at the slave. The two-module wired synchronization operation was proven effective in Chapter III.

Finally, two-module wireless testing was conducted after the examination of the free space propagation loss and the other associated factors. Insufficient isolation of the circulators or power dividers caused inaccuracy in the measurements. To improve the performance of the synchronization circuit, leakage cancellation was introduced in Chapter IV. The final testing result for the wireless synchronization was satisfactory comparable to the wired testing. The curves might sometimes be distorted; however, the phase shift can be detected to within the 20 degree tolerance range.

In summary, the wired and wireless synchronization operation were verified and validated through a series of experiments. The performance of the synchronization circuit was improved over the foundation that previous researchers have laid.

B. RECOMMENDATIONS FOR FUTURE WORK

1. New Architecture of Phase Synchronization

Although the performance of the synchronization circuit has proven satisfactory, the modified circuit resulted in an overall array architecture that is more complicated than originally planned. To be more flexible and robust for future applications of the WDDPA, a new architecture for synchronization is necessary.

To control the LO power levels more precisely, as shown in Figure 85, an independent LO source at each T/R module is a potential solution [32].

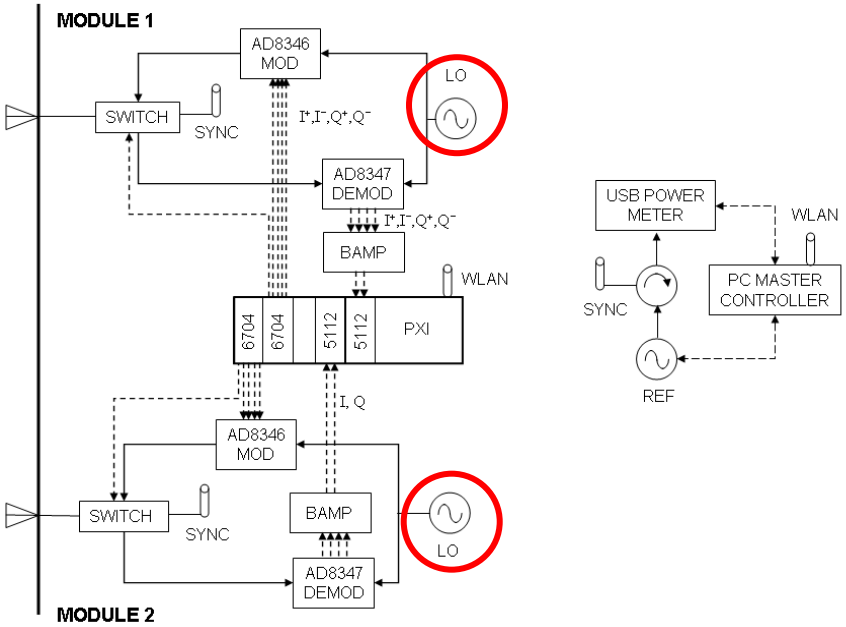

Figure 85. The new architecture of the WDDPA phase synchronization with the individual LO source highlighted (From [32])

The synchronization process would determine the phase of each LO source relative to the reference, as follows. The module receives the LO “beacon” from the controller and determines the phase using the demodulator. Then the measured phase can be reported to the controller via the wireless network. Alternately, a signal with the measured phase can be transmitted back to the controller by the modulator, and a power plot generated similar to the current process. The second method is more desirable because the measured phase difference would include differences in both the TX and RX paths of the modules.

2. Developing LabVIEW Program

The LabVIEW program introduced in this paper conducts the fundamental functions of the WDDPA synchronization operation for the purpose of evaluating the new hardware architecture. For the future application, a more extensive and versatile program should be developed that integrates all of the synchronization and beamforming processes.

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APPENDIX. BAMP DESCRIPTION

The Analog Devices AD8347 Direct Conversion Quadrature Demodulator produces four differential outputs (IOPP, IOPN, QOPP, QOPN) allowing the device to be used in battery-operated equipment with a single-sided DC power supply. This requires four analog-to-digital converters in the digital processor section of the various aperstructure array antennas.

To reduce cost and equipment complexity, a differential input instrumentation amplifier (BAMP) was designed to convert the four channels of differential data into two channels (I & Q). The second stage of the instrumentation amplifier sets the voltage gain A_v at 10. The final stage of the amplifier is a low pass filter with a 3 dB cutoff frequency of 10 MHz. This is an anti-aliasing filter for the AD converters. The AD8347 has a baseband bandwidth of 65 MHz, but AD converters have a maximum sampling rate of 100 MHz. The target signal for the receive-only arrays is an NTSC video signal with a bandwidth of approximately 6 MHz. The 10 MHz bandwidth of the filter is sufficient and also helps to reduce the computational load on the system controller.

The basic designs for each of the circuits are from National Semiconductor Application Note AN-31. Cutoff frequency for the filter is given by:

$$f_c = \frac{1}{2\pi\sqrt{R_{10}R_{11}C_{11}C_{12}}}$$

The op-amp chip is a National Semiconductor LM6722 Quad Wideband Video Op Amp. The functional schematic is shown as Figure 86.

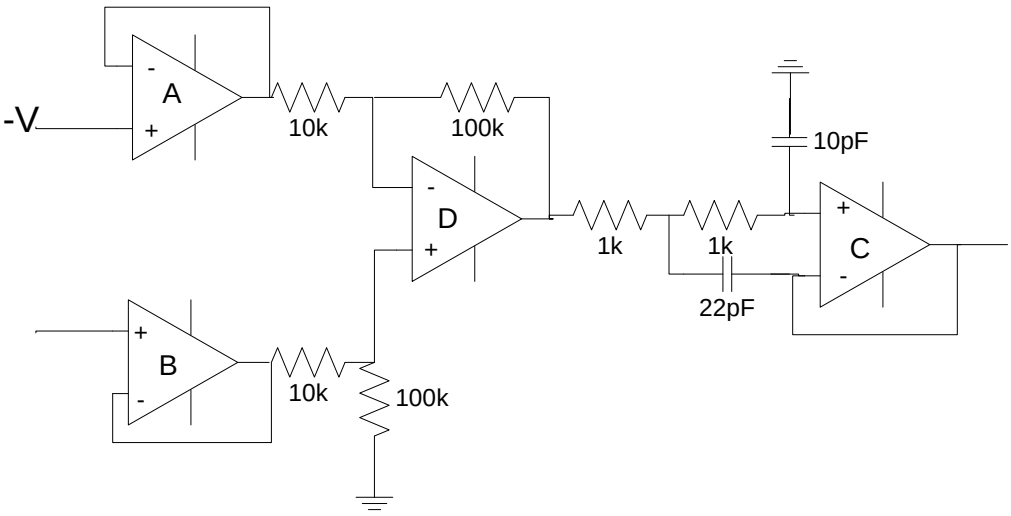

Figure 86. The functional schematic of the BAMP

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