Considering Microelectronic Trends in Advanced Wireless System Design

Dominique Noguet, Guido Masera, Venkatesh Ramakrishnan, Marc Belleville, Dominique Morche, and Gerd Asheid

***Abstract*—Wireless communication system design has been a booming topic since the shift into the digital era in the 1990s. In the same period of time, microelectronic technologies have reached new paradigm points as they were going deeper into the sub-micron area. This paper gives an overview of these emerging constraints and enablers, looking through the specific angle of how much this may impact future wireless system design. To this end, the paper analyzes the major requirements from modern digital communication systems, the way it is foreseen to evolve, and how it can be mapped onto the microelectronic roadmap.**

I. Introduction

RECENT advances in digital wireless communications introduced the use of complex and computational intensive algorithms. This is particularly true as far as the PHYsical and Medium Access Control (MAC) layers are concerned. Indeed, a general trend of these digital communication systems is to improve as much as possible the use of the spectrum resource, which is a scarce and expensive commonality. Efficiency means in this case spectrum efficiency (bit/Hz/s) but also coverage, coexistence, and quality of service provision. To that end, many techniques have been proposed over the last decade mainly, such as new modulation schemes (e.g. WCDMA and OFDM), space-time coding (or in a broader sense Multiple-Input Multiple-Output (MIMO)) techniques, channel coding, etc, that have pushed performance close to theoretical capacity limit [1]. This trend has put hardware designers under pressure; as they have to tackle these highly demanding schemes, while coping with power consumption issues and limited evolution of the silicon technology. Considering both the International Technology Roadmap for Semiconductors (ITRS) [2] and the evolution of wireless communication standards, is indeed a good way to understand that the evolution of the wireless world cannot be caught up by the Moores law alone and that new architectural concepts have to be found to fill the gap. This has moved the centre of attention to the exploitation of parallelism and, unavoidably, opened new questions about how to exploit the different levels of parallelism and how to develop consistent interconnection systems between the processing elements. These open questions are at the core of Multi-Processor System-on-Chip (MP-SoC) research. These systems try to exploit independent-tasks (or functional parallelism) by mapping them to a large number of processors, interconnected via a proper communication structure (e.g., Networks-on-Chip, (NoC)). Considering power consumption leads to even more stringent requirements since battery technology moves yet at a slower pace. As it was stressed above, wireless technology moves fast and more and more standards are to be considered at design time and used/maintained over their lifetime. This makes flexibility a must for current transceiver design. Over the past few years, chipset and equipment manufacturers have adopted a platform approach for the design of a new release to enable to consider the evolution between standards in an incremental efficient fashion in which a new chipset is considered as an evolution of its predecessor rather than a brand new design. However, such a methodology, though using a flexible approach at the design stage, does not necessarily lead to a flexible instantiation eventually. Yet, another approach consists in considering that a transceiver needs to handle flexibility in operation. This interest has been increasing over the past years and is referred to as Software Defined Radio (SDR) [3]. In fact, two levels of flexibility can be considered. The first one captures the ability of a transceiver to support a variety of different modes within a given standard. This is used for instance in adaptive modulation and coding schemes. The second one relates to the fact that a modern transceiver has to handle different standards that are switched from one another depending on availability and user needs. However, current solutions still exhibit low performance either in terms of flexibility or in terms of power consumption. This paper is an attempt to analyse trends in microelectronics in order to better understand the emerging constraints and enablers future wireless system designers need to consider. In Section II, the evolution of microelectronics is depicted, showing the constraints appearing in deep sub-micron CMOS technology as well as potential enablers from technologies that are aside the traditional Moores law track. Then, the specific requirements coming from the communication system design is highlighted in Section III, with a focus on key parameters that are directly impacted by the underlying microelectronic technology. A specific requirement that comes from the profusion of different standards is the thirst for more flexibility. This has to be addressed both at the digital and the RF level, though with specific solution in each case. This is the specific scope of Sections IV and V respectively, again considering how this can be helped by emerging technological solutions.

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II. Trends in Silicon Technologies

Wireless technology has benefited from the advances the silicon technology has offered in the 1990s and 2000s. The whole telecommunication mutation from the analog domain to the digital realm has in fact been made possible by the miniaturisation of transistors, leading to higher density though with low power efficient ICs. In turn, this move to digital communication has created the boom of the digital ICT at all layers, from broadband communications to multimedia services. With this in mind, it would not make sense to foresee what telecommunication will offer in the future without considering the trends in silicon technology research and industry. The key factor behind the digital revolution has been the CMOS technology down-scaling following the so-called Moores Law which coined in the early 70s that the number of transistors would double every year. Although this rule has been validated over the 40 last years by the silicon industry and by the ITRS [2], it is agreed that we are coming to a new era where this rule is no longer valid. Several reasons can be identified:

- The physics of silicon introduces side effects in deep sub-micron technology,
- Predictability of transistors behaviour is getting less accurate, leading to lower yield or less optimal usage of silicon,
- Power density is going to levels beyond what cooling can offer,
- Static power increases which makes no longer valid the assumption that the overall power consumption decreases as transistors shrink,
- Investments needed for new deep sub-micron CMOS are being so huge that only less than a handful of application justifies it.

For all these reasons, it is likely that we are on the verge of significant changes in the silicon capability roadmap, which make the analysis of future trends useful. Indeed, it is foreseen that the roadmap has to move from a pure down-scaling to new functionalities and combined technology vs. system innovation in order to manage future power, variability and complexity issues. However, there is no accepted candidate today to replace CMOS devices considering the four essential metrics needed for successful applications: dimension (scalability), switching speed, energy consumption and throughput [4], [5]. Moreover, when other metrics such as reliability, designability, and mixed-signal capability are added, the dominance of CMOS is even more obvious. It is then realistic to think that other micro or nano-technologies should be seen as future add-ons to CMOS and not as a substitute for it [6]. This transition between the "business as usual" era and the entry to the post 2015[1] period where new alternative or complementary solutions need to be found is depicted in Fig. 1.

Bearing in mind this disruptive future and rather than extending the technology evaluation proposed by the ITRS,

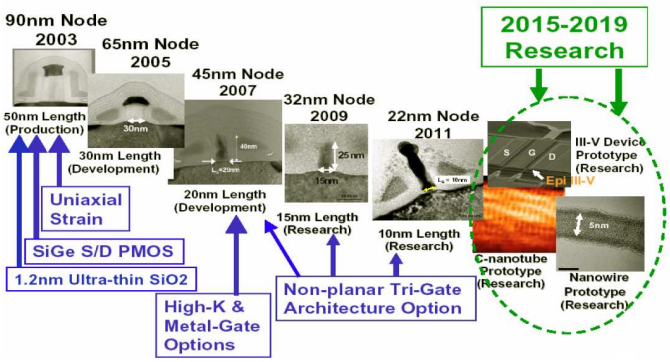

Fig. 1. Technology nodes and predicted end of CMOS down-scaling with possible alternatives (nanotubes and nanowires) for post-2015 nanotechnology[2]

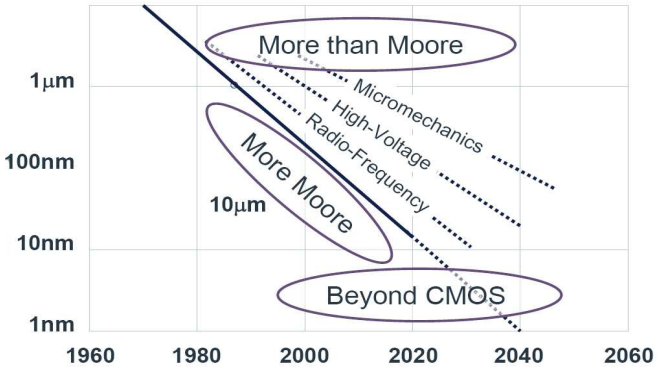

Fig. 2. Technology roadmap mirroring the European vision[3]

technology analysis carried out in Europe by EUREKA Medea experts [6] suggests considering 3 major paradigms:

- **More Moore**: corresponding to ultimate CMOS scaling
- **More than Moore**: corresponding to the use of heterogeneous technologies such as Micro Electro Mechanical Systems (MEMS) or Micro-Opto-Electro Mechanical Systems (MOEMS)
- **Beyond CMOS**: corresponding to nanotechnology alternatives to CMOS.

A. More Moore

This ultimate scaling of CMOS will be essential to supply the massive computing power and communication capability needed for the realisation of European Ambient Intelligence (AmI) applications at an affordable cost and a power efficiency exceeding 200 GOPS/Watt for programmable and/or reconfigurable architectures [7]. However, reaching this ultimate CMOS node at the deca-nanometre level around the year 2015 will require addressing cumulative interrelated challenges surveyed in [8], [9].

In the process technology domain, major challenges are: the massive introduction of new materials, the introduction of new device architectures, the move to Extreme Ultra-Violet (EUV) litho or nano-imprint lithography, the increase of random device and interconnect variability especially in memories, the reach of limit of Cu interconnects (e-migration, cross-talk, etc.), the conflict between dynamic and static power density.

[1]2015 is generically considered as the end of CMOS scaling because it has been shown that channel length will reach dimensions where the MOS device principle no longer operates.

[2]Source: Robert Chau, Intel, presentation at ICSICT, 2004.

[3]Source: IMEC, 2006.

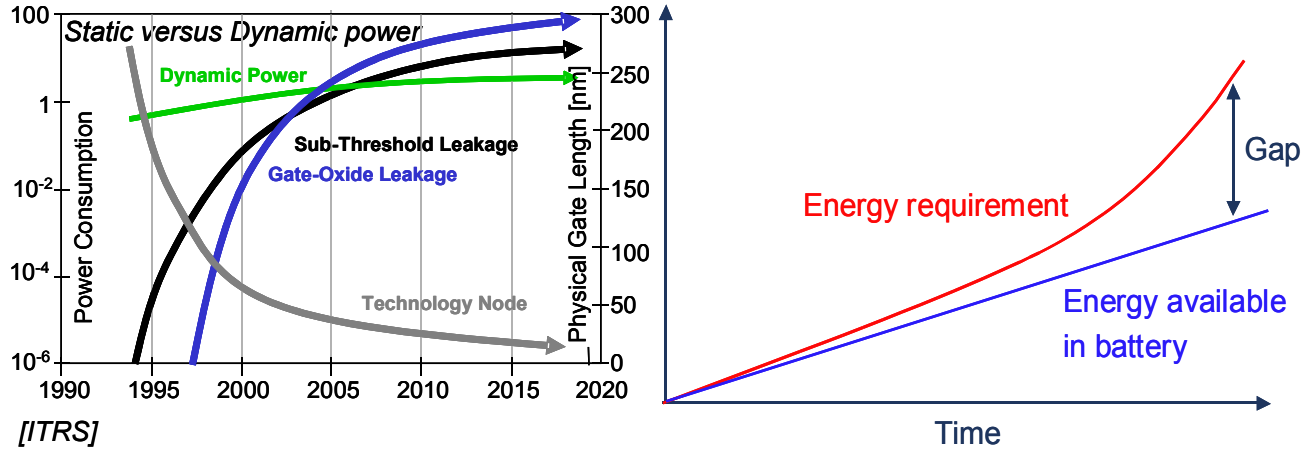

Fig. 3. Power consumption evolution with technology node vs. battery evolution

In the design domain, the key challenges are: the fact that ultimately non recurring engineering (NRE) cost may reach 1B€/platform if no drastic changes in design technology occur, due to increased hardware-software interaction on multi-core platforms.

Perhaps even more relevant is the fact that process technology challenges directly impact design challenges. One example that is relevant for handheld terminals is that static power will become prominent in the energy consumption bill. Unfortunately, it is not expected that battery power density will evolve at the same pace (see Fig. 3).

Random variability will impact parametric yield and will require novel ways to avoid corner-based design to cope with device uncertainty, and amenable to design automation. This will require the development of self-healing, defect- and error-tolerant, yet testable design based on low-cost on-chip adaptive control systems.

Reliable local and global on-chip communication in 22nm or smaller technology will be a much more limiting factor than transistor scaling and will require, besides the investigation of optical, wireless or CNT-based technologies, investigation of architectural solutions such as tile-base Globally Asynchronous Locally Synchronous (GALS) architectures exploiting Networks-on-Chip and MP-SOC. 3-D integration and System in Package (SiP) must also be studied as strong contenders to ultimate scaling for true system design, which is finally the ultimate goal of electronics.

Analog and RF design will have to cope with ultimate digital scaling and further sub-1 Volt scaling. This will require extreme creativity in analog and RF system design by compensating analog deficiencies by digital techniques.

Alternatives to bulk CMOS shall also be considered to overcome the shortcomings when scaling down to deep submicron. Silicon On Insulator (SOI) technologies are foreseen as relevant with this regard, as it could lead to a better tradeoff between active and static power leakage. A significant active power reduction can be achieved by using SOI devices. Indeed, SOI devices are well known to be able to achieve the same performances as Bulk device, but with a lower power supply. This is achieved thanks to lower parasitic capacitances (thick buried oxide for electrical isolation instead of junctions) and thanks to lower threshold voltage in dynamic mode[4]. Active power reduction up to 50% can then be achieved with SOI. DC leakage can also be controlled [10].

B. More than Moore

The "More than Moore" approach intends to address parallel routes to classical CMOS by tackling applications for which CMOS is not optimal. These applications can be classified in three major categories: interfacing to the real world, enhancing electronics with non-pure electrical devices, embedding power sources into electronics [6].

In the field of IC design for advanced 3G standards, the More than Moore class is expected to bring significant breakthroughs in RF front end design. Indeed, new complex signal modulations (e.g. OFDM) require very linear RF components in order to limit distortion and to ensure high signal throughput. Cellular phones can utilise up to seven different wireless standards or bands, including DCS, PCS, GSM, EDGE, CDMA, WCDMA, GPS and Wi-Fi, and each standard has its own unique characteristics and constraints. Additionally, next generation phones cannot be significantly larger than todays phones and they will need to have similar talk and standby battery lifetimes. Today, a large proportion of the components in a mobile phone are space consuming "passive" elements such as inductors, variable capacitors and filter devices. Integrated passive elements and RF MEMS/NEMS have been proposed to help solve these problems. High-quality passive elements are available through SiP technologies. Besides, nano-materials are expected to strongly improve the achievable capacitance per unit area value for capacitors. One key remaining issue though, is whether the extra cost of these non-standard technologies can be justified by the benefits they bring. Thus, whenever heterogeneous technology is considered, the trade-off between performance and cost must be analysed.

[4]In case of Partially Depleted SOI devices.

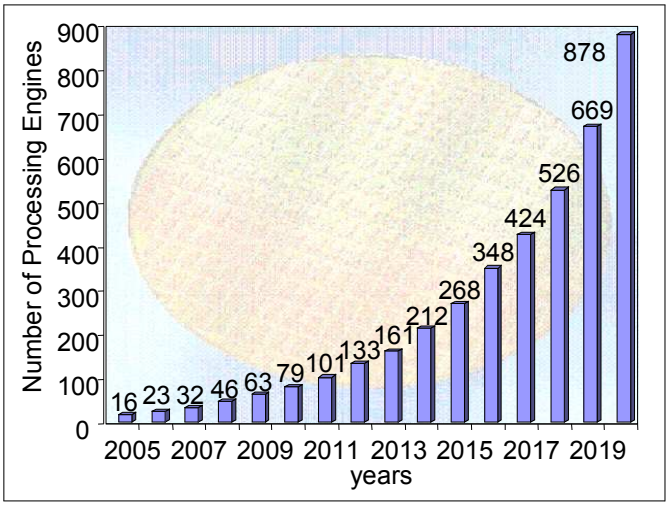

Fig. 4. Evolution of processor number in MP-SOCs[5]

C. Beyond CMOS

The "Beyond CMOS" paradigm intends to identify technologies that could replace CMOS, either in a disruptive or evolutionary way after CMOS will reach its ultimate limits. The ITRS Emerging Research Devices (ITRS-ERD) proposes criteria to evaluate the potential of emerging research devices and circuits with respect to future applications. The analysis presented in the ITRS-ERD document [2] is based on defining a set of criteria for logic and another set of criteria for memories, and applying them to potential technologies. These criteria are as follows:

- **For Logic**: scalability, performance, energy dissipation, gain, operational reliability, operating temperature, CMOS technological and architectural compatibility ,
- **For Memories**: scalability, performance, energy dissipation, OFF/ON ratio, operational reliability, operating temperature, CMOS technological and architectural compatibility .

Nano-technologies falling into this category correspond to building blocks such as: Atom scale technologies, Spin electronics, Molecular electronics, Ferromagnetic devices, Nanoelectromechanical systems, Organic/plastic electronics, Bio-sensors. Because these new devices have behaviours that sometimes differ significantly to classical transistors, "electronics" using these functions needs to be invented as well. From an architectural viewpoint, these technologies derive into: bio-inspired electronics, nanomechanical computing, quantum computing. Stating this, it is obvious that a description of the research challenges related to Beyond CMOS is far too broad to be surveyed in this paper. What can be kept in mind is that Beyond CMOS is extremely multi-disciplinary with extensions at all levels from building blocks to system usages.

III. Processing needs in wireless communication

Bearing in mind the evolution of silicon technology, designers also have to consider the evolution of the requirements from advanced wireless systems. Along their path towards next generation broadband wireless access, different standardization bodies (e.g. 3GPP, 3GPP2, IEEE, ETSI-DVB, etc.) have been introducing new standards that enhance their legacy radio access technologies. Examples of recent releases are: 3GPP Release 7 (HSPA+), Release 8 (LTE), Release 9 (LTE-Advanced), 3GPP2 (UMB), IEEE WLAN 802.11 (n, vht), IEEE WMAN 802.16 (d, e, m), ETSI DVB (T2, H, SH, NGH). Emerging and future wireless communication systems are characterized by a clear and steady convergence on both services and technologies. From the service perspective, operators are striving to offer to the users a wide spectrum of rich multimedia services including both interactive and broadcasting, which raise the need to embed complementary technologies (e.g. for uni-cast, multi-cast, and broadcast transmissions) into the future generations of radio access systems.

This context of coexistence and convergence is driving demand for flexible and future-proof hardware architectures offering substantial cost and power savings. Manufacturers have already started activities towards the provision of multi-mode handsets featuring the advancements of the recent radio access technologies (e.g. 3GPP LTE, WiMAX IEEE 802.16m, DVB-T2/H). However a large gap is growing in the field of flexible radio between advances in communication algorithms, methods, system architectures on one side, and efficient implementation platforms on the other. Despite the large amount of available results in the system level technologies related to multi-mode, multi-standard interoperability and smart use of available radio resources (adaptive coding and modulation, cross layer optimization, ...), a very limited number of hardware solutions have been proposed to really support this flexibility and convergence by means of power efficient, low cost reconfigurable platforms. In most cases, chipset vendors offer different solutions for each combination of standards and applications to be supported.

To enable a single modem to service multiple different wireless systems, highly flexible solutions are needed. In practice, currently implemented flexible hardware modems are focused on the receiver segment placed between the RF front end and the channel decoder. In this part of the modem, several digital signal processing algorithms, such as equalization, interference cancellation multipath correlation (rake receiver), synchronization, quadrature amplitude mapping/demapping and Fast Fourier Transform (FFT) can be run on vector processors, which allow for Giga-Operations Per Second (GOPS) rates resorting to very high level of parallelism. However, other functional components of a modern modem (such as channel decoding) are not efficiently supported by vector processors and alternatives to software programmable architectures are not considered solid solutions: cost of hardwired dedicated building blocks becomes rapidly unacceptable with the number of standards to be supported, while reconfigurable hardware, such as Field Programmable Gate Arrays (FPGAs), are too expensive in terms of silicon area and standby energy consumption (which is due to leakage current, proportional to area).

The design of high throughput software programmable architectures is currently the largely prevailing development

[5]Source: ITRS.

Standard	FEC	rates	block size	Throughput	Complexity (GOPS)
GSM	CC	3/4 - 1/4	33 - 876	up to 12 kbps	0,001
EDGE	CC	6/7, 1/3	39 - 870	5 - 62 kbps	0,005
UMTS	bTC	01-mar	40 - 5114	up to 2 Mbps	3
HSDPA	bTC	1/2 - 3/4	40 - 5114	up to 14.4 Mbps	30
CDMA-2k	bTC	1/2 - 1/5	378 - 20736	up to 2 Mbps	0,2
(WiMax)	dbTC	1/2 - 3/4	up to 648	up to 54 Mbps	72
IEEE802.16 (WiMAX)	LDPC	1/2 - 3/4	up to ~2500	>100Mbps	7
DVB-T/H	CC	1/4 - 7/8	(broadcast)	up to 32 Mbps	10

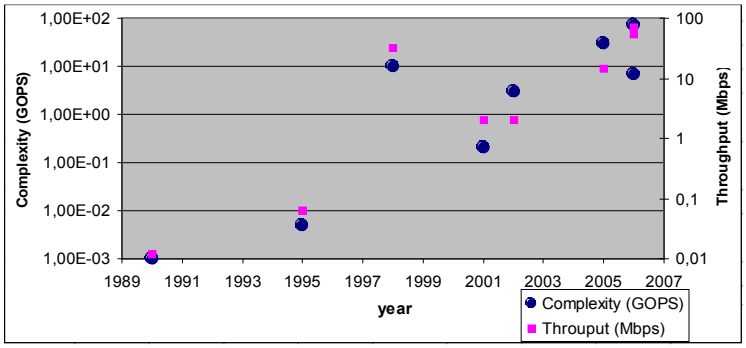

Fig. 5. Throughput and complexity trends for wireless standards

area for companies in the field of next generation base-band platforms. This dominating approach is the optimal solution for the current relatively limited needs for flexibility, but it is likely to be inadequate for future wireless systems that will be characterized by:

- Significantly larger amounts of standards and communication modes to be supported,
- Higher number of complex and heterogeneous processing algorithms,
- Higher level of dynamic flexibility to support cognitive and opportunistic radio concepts,
- Lower energy dissipation in both static and dynamic conditions.

Future of wireless communications cannot be guaranteed by current approaches towards flexible base-band platforms. Beside this research effort gap, known platforms for digital base-band processing show serious lacks of capabilities with respect to the radio flexibility that is currently studied at the system level and expected by the market. In particular presently available platforms suffer from two main limitations:

- Partial flexibility: since large difference is recognizable between the processing functionalities that are expected to be supported in a flexible receiver, and the actual level of flexibility that is achieved in hardware. As an example, advanced channel decoders are usually not included in the whole receiver as reconfigurable elements, but they are supported by means of separate components, designed and optimized to execute one specific decoding algorithm.
- Expensive flexibility: since flexibility comes at a very high cost in terms of occupied area and dissipated energy and required reconfiguration time; on the other hand, flexible platforms are requested to provide better overall die area and power figures than receivers designed by simply allocating multiple function-specific components. Moreover, simple, fast and energy efficient reconfiguration procedures are of primal importance to enable true flexibility, as awaited in cognitive and opportunistic radio systems.

A. The need for highly demanding building blocks

A rather reduced number of computationally intensive functionalities is associated with the key enablers commonly adopted by next generation radio access standards. A list of these technologies is presented in Fig. 5. The table on the left shows key characteristics of Forward Error Correction (FEC) technologies adopted in several standards that have been introduced during the last 15 years in the domain of wireless communications and digital broadcasting. Particularly Fig. 5 contains for each specified FEC the maximum data throughput and the processing complexity, expressed in GOPS. The plot on the right side clearly indicates that both throughput and complexity tend to increase exponentially with time. In more details, data throughput doubles within 15 months and this trend is almost in agreement with the evolution trend of performance in semiconductor industry, at least until Moores law remains valid (see section 2). However, Fig. 5 shows that the FEC complexity trend is faster, as the required GOPS doubles every 12 months.

The growing gap between silicon performance and FEC complexity trend implies that the efficient implementation of emerging and future error correcting techniques will not be guaranteed by the progress in the semiconductor industry, but will continue to impose application specific optimizations at the confluence of algorithm and architecture. Particularly in the implementation of computationally intensive base-band processing tasks, this joint effort at the algorithm and architecture levels can be targeted towards different optimization objectives, such as area occupation, throughput, power dissipation, and flexibility.

As for the area and throughput objectives, several cases can be cited to show how efficient implementations often come from joint design efforts spent at the algorithm and architecture levels. For example, although the original Low Density Parity Check codes (LDPC) decoding algorithm requires rather complex processing at the check nodes, all decoders implemented in the last few years resort to the min-sum approximation, which saves a significant portion of complexity with a marginal performance loss. Another relevant example is found in the MIMO detection domain, where several sub-optimal implementations have been proposed in the last few years as alternatives to sphere decoding. These solutions (e.g. k-best and LORD) exhibit close to Maximum Likelihood performance, simpler architecture, and deterministic detection delay at the same time. Additionally, the algorithm-

architecture interdependency in a specific application domain can be leveraged to improve energy efficiency.

Joint algorithm and architecture optimization can be also seen as a method to achieve flexibility through the development of unified processing algorithms that enable increased sharing of hardware resources. This unifying approach combines both algorithm and architecture alternatives into a joined optimization effort towards efficient flexibility in radio communications. The idea is to develop innovative processing algorithms, where limited and controlled performance degradation is accepted and exchanged for flexibility in the hardware implementation.

B. The need for power efficient design

Several IC implementations of turbo and LDPC decoders have been published in IEEE ISSCC International Solid State Circuits Conference (ISSCC) and in the Journal on Solid State Circuits (JSSC) series in the past few years. Looking at the characteristics that have been measured for those components, one can easily see that the power dissipation trend-line remains fairly constant across the last ten years and typically included in the range between a few tens and a few hundreds of mW. This general tendency is somehow surprising, as throughput and processing complexity have been increasing along the same period of time. The explanation of the observed trend on power dissipation comes from CMOS process down-scaling (particularly scaling of gate area and parasitic capacitance) that has substantially balanced the increase in computational effort. This appears as a very bright and encouraging conclusion. However power dissipation is expected to become a very critical issue in future developments for several reasons.

Fist of all, the static power dissipation has been usually neglected so far; however it will soon become comparable to the dynamic one in next generations of CMOS process technology (see section 2). Therefore, with a fixed power budget assigned to base-band components, the dynamic power consumption will need to be limited to a lower bound than in today implementations.

Secondly, some base-band functions will increase dramatically the need of processing energy. The most relevant example is probably given by joint MIMO detection and channel decoding. The concatenation of soft output MIMO detection and iterative error correction algorithms will create high complexity receivers where the FEC processing is organized around two nested feedback loops: an inner loop, associated with turbo or LDPC decoding iterations, and an outer loop, with exchanged soft information between MIMO detector and inner channel decoder. This arrangement will significantly increase the global complexity and affect both the required processing speed and dissipated power. For example, if a 300 mW turbo decoder is used as the inner unit in a concatenated system with 3 iterations of the outer loop, the power consumption of the turbo decoder will increase by a factor of 3.

A third reason comes from the increasing levels of flexibility that will be incorporated in next generations of channel decoders. Flexibility is ineluctably associated to a cost in terms of consumed energy, which tends to reduce the power efficiency.

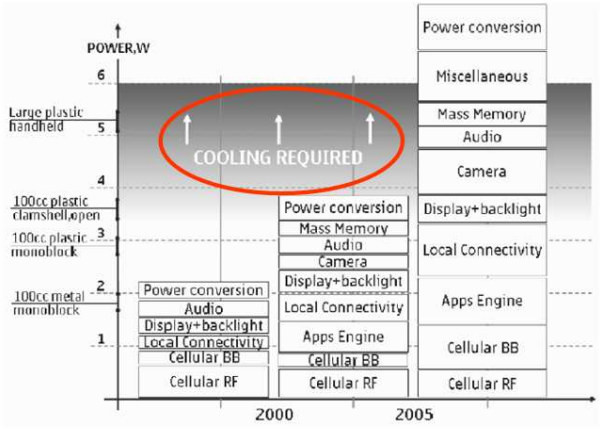

Fig. 6. Power consumption increase in wireless terminals[6]

The rise of power consumption combined with the wished reduction in size of handset devices causes temperatures to increase because the transfer of heat is proportional to the surface area. Increased temperatures have two effects. The first is that the temperature of the casing of the device can go up such that it becomes too hot to handle. The second effect is that higher temperatures make the electronic components unreliable and more likely to fail. In [11] it is envisaged that a dramatic increase of energy consumption of 4G mobile device will make active cooling a necessity, which is not attractive for users and manufactures. The performance of active cooling in a mobile devices is investigated in [12]. From the mobile manufacturers' perspective the energy consumption problem is critical, not only technically but also taking into account the market expectations from a newly introduced technology. This is in fact becoming a key concern: there exists a continuously growing gap between the energy of emerging radio systems and what can be achieved by:

- Battery technology evolution,
- Scaling and circuit design progress,
- System level architecture progress,
- Thermal and cooling techniques.

Considering this power consumption (and dissipation issue), designers are more and more considering power consumption as a key figure of merit. A simple model can help clarify this issue and at the same time suggests the main research direction to combat loss of efficiency in flexible architectures. In channel decoders, power efficiency is defined as the ratio between the number of decoded bits per second and the corresponding dissipated power. It is usually measured in Mbps/mW. The numerator of the ratio can be written as $N_b * f_{ck}$, where Nb is the number of bits decoded per clock cycle and fck is the clock frequency; neglecting the static contribution, the denominator can be expressed as $A * C_{sw} * V_{dd}^2 * f_{ck}$, where A is the total occupied area, C_{sw} is the average switched capacitance per unit area and V_{dd} is the supply voltage. Defining $A_b = A/N_b$ as the average area required to process one bit, the power efficiency can then be formulated as $\eta = 1/(A_b * C_{sw} * V_{dd}^2)$.

[6]Source: Frank Fitzek Marcos Katz, Cooperation techniques in wireless networks, Springer, 2007.

This simple model clearly shows that the power efficiency only depends on three parameters: two of them, C_{sw} and V_{dd} are tight to the evolution of silicon technology, while A_b is largely dependent on how the required processing functions are implemented. When two or more functions are mapped to a unique architecture capable of flexibly support all of them, this necessarily leads to the allocation of additional components that are used to handle the switching between two functions and not for the execution of the function itself. This results into an increased average area per decoded bit and impairs the efficiency. Therefore the search for efficient flexibility is the search for architecture solutions that minimize A_b.

C. The need for flexibility

Although throughput and area have been the dominant metrics driving the optimization of digital building blocks, recently, the need for flexible systems able to support different operative modes, or even different standards, has changed the perspective. In particular, the SDR paradigm made flexibility a fundamental property of future receivers, which will be requested to support a wide range of heterogeneous standards.

Run-time flexibility in a receiver is a very ambitious and innovative task that shall provide support to multiple versions of a specific functionality, each one characterized by a different trade-off between communication performance and energy (or throughput) efficiency. The fundamental purpose here is dynamically enabling the change between one version and another of the considered functionality, in response to energy constraints and user needs. This type of versatile platform will therefore give support to complex power management algorithms and optimal allocation of the spectrum resources. Although the concepts of adaptive and cross-layer optimization in mobile terminals are not new, the design of an implementation platform supporting those concepts is still an open problem and a very challenging research topic. Two key problems can be seen: the required level of flexibility is higher than in classical multi-standard architectures, and constraints on the reconfiguration latency are expected to be stricter.

Flexible algorithms and architectures must be developed to enable the support of energy management techniques involving all functionalities of the digital base-band processing chain. Specific optimization metrics and methods need to be introduced to drive algorithm and architecture design. Proper methods must also be developed for estimating the operative conditions and algorithms for realizing the energy management.

A relevant application example for the mentioned flexibility target is given by next generation wireless systems that use multiple antennas to deliver very high data rate services. In such systems, a feedback loop between MIMO detector and outer channel decoder enables iterative "Turbo-MIMO" processing: performance very close to *a posteriori* probability detection has been achieved with different detection techniques. While optimum error rate performance is obtained with soft-output maximum likelihood detection, linear and successive interference cancellation (SIC) algorithms are interesting alternative solutions, with an implementation complexity lower than the sphere decoding. Moreover, for low code rates or low modulation order, plain linear detection performs within 2dB of the performance bound; on the other hand advanced detection strategies (sphere decoding) is convenient for high code rate and higher order modulation [13]. Thus different performance-complexity-energy trade-offs are covered by a set of heterogeneous algorithms and a proper flexible platform is required to dynamically exploit the energy minimization opportunities offered by these trade-offs.

Current approaches to multi-standard functionality pragmatically aim at implementing a "just enough flexibility", by supporting codes and throughput requirements specified in some of the current standards. A rather small number of multi-standard decoders have been implemented so far. They can be classified in three categories.

1) *PIntra-family flexibility*, which support multiple modes belonging to the same functionality. As an example, one could design a turbo code decoder able to operate over several turbo codes, specified in different standards, such as UMTS, WiMAX and WiFi. The most common implementation approach for this category is hardware parameterized functions: the processing architecture is organized around a number of storage and computation units that are structured based on a number of parameters, such as block size and code rate.
2) *Inter-family flexibility*, which is capable of a wider flexibility, as they must process functions belonging to different and in some cases heterogeneous families (e.g. to stay with the FEC example, turbo and LDPC codes could be an example) specified in two or multiple standards. In this case, reusable hardware resources can be identified and shared among supported decoding algorithms, with the final objective to save area with respect to the straightforward allocation of several independently designed decoders ("Velcro approach").
3) *Full flexibility*, which supports high throughput implementation of a wide range of heterogeneous functions, not necessarily limited to the ones that are today specified in a standard. As an example, a fully flexible turbo code decoder should be able to support any interleaving law. The additional difficulty of this approach derives from the fact that parallel collision-free decoding architectures are heavily based on the specific features of the code family to be decoded; as a consequence, these architectures can hardly be exploited when multiple different codes must be supported. Common operator technique is another approach belonging to this class [14].

IV. Software Defined Radio Approach: Challenges and Opportunities

Flexibility requirements, when coupled with low-cost and less time-to-market constraints, make the development of a mobile device highly complicated and challenging. SDRs, with cognitive capabilities, are getting prominence as potential candidates to meet the future requirements of mobile wireless devices. Compared to the pragmatic design approach for flexibility mentioned above, the SDR approach aims at providing

a comprehensive design framework encompassing platforms, architectures, software, methodology and design tools.

A. Current Solutions

Current solutions for SDRs are component based and model driven, where a Platform Independent Model (PIM) of a waveform[7] is constructed as an assembly of components, e.g. [15], from the specification document, e.g. [16]. Each component represents a part of functionality in a whole waveform. From a PIM model, a Platform Specific Model (PSM), which denotes the implementation of a waveform, is obtained with or without using a library. Libraries internally developed or from third party vendors providing efficient implementations of few, sometimes even all, components of a waveform can improve overall system efficiency and drastically decrease development time. For example, Texas Instruments (TI) provides efficient implementations for implementing the WiMax waveform [17].

Some other approaches for developing SDRs are based on Software Communications Architecture (SCA) adopted by JTRS [18]. SCA is predominantly General Purpose Processor (GPP) based and uses CORBA as middleware abstracting the underlying hardware. This creates an operating environment that enables to develop applications independent of hardware, and methods for loading new applications, configuration and control.

B. Key Problems

Though each of the above solutions improves the development of SDR in one way or the other, there are associated issues often leading to situations where one solution does not fulfil all requirements. A serious drawback in the libraries that are available today on the market is that they are specific to one waveform or to one hardware platform. For example, the library in [17] is specific to the WiMax waveform targeting a specific Processing Element (PE), namely the TMS320TCI6482 DSP. Moreover, some of the libraries are proprietary in nature; the details on the components and their interfaces are not known. Even though library based approaches have the potential to increase efficiency and portability, the lack of standardization decreases reuse of implementations drastically.

Similarly, overhead caused for supporting SCA is a key deterrent for its usage, particularly in physical layer processing, due to the existence of hard constraints, e.g. latency [19]. Though abstraction of the underlying hardware platform makes mapping of a waveform description onto a hardware platform easy, it completely blocks the opportunity to exploit the architectural capabilities of a hardware platform. Hence, an optimum mapping is not possible. Mapping should consider the requirements of a waveform, e.g. processing complexity, available resources in a hardware platform, e.g. memory, and constraints of a waveform, e.g. throughput, when optimizing with respect to design requirements like energy efficiency. Therefore, constraint aware mapping is a key for improving the overall efficiency of the complete system.

[7]In this context, the term waveform represents a complete wireless standard with several modes.

The efficiency of a waveform implementation is a pivotal factor for overall footprint and energy efficiency. Investigations done on implementation efficiency indicate optimization limits depending on the implementation type [20]. For example, implementing in assembly is more efficient than C-code because assembly code can better exploit the architecture of a PE. A GPP offers high flexibility, but requires more energy per decoded bit than, e.g. a Digital Signal Processor (DSP). Therefore, entirely GPP and C-based SDR solutions are not suitable for battery operated devices due to low implementation efficiency.

Merely increasing parallelism in order to increase computation power, without considering efficiency will lead to high area and energy consumption. Therefore, in SDR systems where future requirements of computational performance will be in the order of tens to thousands of GOPS, techniques like massive pipelining, increasing the number of GPP cores or speeding up the clock are not satisfactory due to energy efficiency reasons. HW platforms for SDRs will, most likely, be heterogeneous in nature with programmable PEs like Application Specific Instruction-set Processors (ASIPs), DSPs, GPPs and Application Specific Integrated Circuits (ASICs) or even physically optimized ICs. Design requirements of a SDR system, including flexibility and efficiency, will determine the type and number of PEs. For example, physically optimized ICs provide very high performance and power/energy efficiency; however they offer least flexibility whereas GPPs provides full flexibility at the cost of very low energy efficiency.

Numerous issues in waveform development for SDRs are due to the "specification-to-implementation" problem. In general, waveform specification is in the form of a textual document with details on different modes, constraints and critical loops that have to be met by a waveform implementation. Textual documents provide redundant information, which is sometimes verbose and sometimes terse. Therefore, creating a PIM of a waveform incorporating all the features like latency and deriving a PSM model, meeting key requirements like throughput from it, is a cumbersome task, often error prone. Therefore, design, development, integration and testing of waveforms have become highly complex and time consuming.

C. Challenges

The paradigm of SDR poses new challenges or makes current design challenges more stringent. The most relevant ones are:

- *Portability*, which can be defined as the inverse of porting effort, represents the ease with which one waveform can be moved to another hardware platform [20]. Portability requires a platform independent waveform description.
- *Efficiency* with respect to area and energy is essential in order to decrease the power/energy consumption and extend the battery life. However, this requires high efficiency in waveform implementation.
- *Interoperability* denotes the ability that a waveform implemented on two different hardware platforms interoperates with each other.
- *Loadability* illustrates the ease with which a waveform can be loaded, over-the-air, into a hardware platform,

programmed, configured and run. Loadability can be increased by well defined and known interfaces in waveform implementation.
- *Trade-offs* between flexibility and efficiency becomes challenging in the wake of their contradictory nature. This makes heterogeneous multi-processor system-on-chips (MPSoCs), an inevitable candidate as the hardware platform for implementing a waveform.
- *Cross layer design* and optimization techniques are getting popular, if not mandatory, in order to cope with the increasing need for spectrum and energy efficiency. This leads to very tight dependencies, interactions between physical and MAC, higher layers that have cognition, requiring flexibility in implementation and algorithms.

Most of the challenges in SDR arise due to the contradictory requirements of flexibility, performance and efficiency. Heterogeneous MPSoCs with specialized PEs can pave the way to solve the dilemma of contradicting demands of high computational performance at the one hand and energy efficiency on the other. However, designing such a system is a challenging task. Tools are required for the development of the dedicated PEs as well as of the whole SoC. High speed simulation is necessary in order to support design space exploration and verification at an early phase.

Still, the complexity of modern flexible implementation structures would hardly be manageable and their development is a tedious and error-prone task. What is needed is a description method that can lead to a (semi-) automatic generation of a waveform implementation directly from the specification. Therefore, a methodology is required, that raises the abstraction level of receiver design to make it manageable.

D. Opportunities

As mentioned earlier, direct implementation on a low abstraction level is not well suited for an efficient portable waveform implementation. Raising the abstraction level leads to library based approaches, where efficient implementations of basic components are available and can be assembled to implement the complete transceiver. Also, a library based approach enables efficient utilization of heterogeneous MPSoCs.

1) Design Principles: There are several key design principles that must be considered while building a library that can pave way for Waveform Description Language (WDL) based SDR development. They are:

- Hardware architectures that offer full flexibility, e.g. GPPs, are not efficient and are costly in terms of area and energy consumption. Therefore, application specific optimization is needed in order to increase both energy efficiency and computation performance. If limited flexibility can be offered, such architectures can still be tuned for different requirements.
- Algorithms that might work efficiently for one scenario might not be efficient for another, e.g. sophisticated and complex algorithms might be needed in a bad channel while simple algorithms might be sufficient in a good channel. This creates the need for analyzing algorithms that are scenario-specific and to identify the common kernels in these algorithms ("Nuclei") to maximize reuse.
- Building a library that is based only on functionalities in waveforms limits reuse of the library. For example, if one of the components in a library is a modulator of a particular scheme, a different scheme in another waveform renders it useless. Therefore, emphasis should not be on the functionalities but on the algorithms that are used for implementing such functionalities. This not only increases reusability, but also provides algorithmic flexibility.
- Flexibility in implementing a waveform can be provided, even in a fixed hardware platform, through different implementation algorithms and configuration parameters like implementation-method, input data-width, scaling, etc. However, a PE in a hardware platform should have architectural capabilities to support different implementation algorithms efficiently.
- Providing easy programmability for complex systems like SDR is essential to exploit efficiently the hardware resources. A programming model that can bridge the gaps between waveform, hardware platform and mapping is needed. This model should allow a designer to utilize the flexibility present in a hardware platform in order to increase the implementation flexibility.
- Due to the presence of a number of layers with very high interaction between them in typical waveforms, it is essential to treat SDR development as a joint optimization problem.
- In spite of advances in standardization due to bodies like SDR Forum [21], NGMN alliance [22], JTRS program [18], etc., lack of complete and unified standardization is preventing huge advances in SDR technology. Due to this, reusability of other solutions, participation of different vendors is limited, indirectly leading to increase in development costs. This also prevents co-operations and sharing knowledge between academia and industry on the one hand and between military and civil domains on the other hand.

Due to the strong dependencies between algorithms, hardware architecture and tools, it is necessary to investigate these aspects jointly in order to identify an efficient SDR development methodology. For example, a detailed algorithm analysis can drive the component identification and implementation, which then feeds back the analysis results which may cause revision of the algorithm itself, making it algorithm architecture co-design. Furthermore, the real implementation of Nuclei has the potential to deliver important information on the interfaces and parameters which are required for tools exploiting the spatial and temporal mapping of a waveform description. Therefore, joint results achieved by working together in the three domains listed before are needed, making SDR development algorithm, architecture and tools co-design.

2) Algorithms: Since SDRs have to offer flexibility, it is efficient, if not necessary, to exploit the tradeoffs between complexity and error rate performance in different algorithms. For example, in a spatially multiplexed MIMO signal, though exhaustive search delivers the minimum error rate, the enor-

mous computational complexity is a heavy burden for the base band receiver. On the other hand, low-complexity algorithms such as zero-forcing detection can operate in a limited SNR range only. Therefore, it is essential to analyze such algorithms jointly along with their tradeoffs.

Algorithms that are used for implementing different functionalities can have common computation and communication patterns. This commonality can be exploited by identifying such common kernels that are also computation intensive. Such algorithms might be used in different applications. If the granularity of such kernels is optimum, i.e. not coarse grained as a complete channel decoder nor as fine-grained as an adder, it can enhance reusability and can enable the availability of optimized implementations for such kernels. However, emphasis should be on the implementation-friendly algorithms in order to enable various implementation alternatives, based on different algorithms, without sacrificing efficiency.

3) Tools: Tools must offer a seamless environment for developing SDRs by providing the infrastructure to capture the waveform specification, to do mapping, implementation, integration and verification. Due to a huge number of critical paths involving several components of a waveform, a constraint aware mapping approach is needed. It increases the chances of successful mapping and decreases the number of iterations. However, it complicates not only the tool development but also the identification of the appropriate ways for describing the impacts with respect to constraints.

In order to validate and evaluate the spatial and temporal mapping decisions as well as the performance of the overall system, a system simulation environment in software is needed, which simulates the system behaviour in terms of functionality and timing. The software based system simulation plays a key role in exploration and verification of the spatial and temporal mappings. The information obtained by the simulation can be fed back to the higher layers in order to improve the mapping quality. This can be considered as an iterative approach, which is repeated until a satisfying result is obtained.

4) Architectures: In general, heterogeneous MPSoCs can provide high performance due to parallel processing of tasks and at the same time provide flexibility and efficiency due to the heterogeneous, function-optimized nature of PEs. Among the PEs, ASIPs are very attractive candidates for implementing SDR systems, where a fine balance between flexibility through programmability and efficiency through application specific architecture optimization is essential. For example, conventional load store memory architectures may not be able to meet the throughput-latency demands of SDR applications and may become a bottleneck. Therefore, special application specific memory architectures, in addition to other architectural options, are needed to meet these demands. Similarly, due to extremely high throughput and short latency demands in the communication between PEs in an MPSoC, conventional communication schemes like buses are most likely to fail. Instead, the idea of specialized communication architectures, including dedicated links between PEs, even special links that are optimized separately for throughput and latency is gaining more interest.

To summarize, requirements and therefore complexity of SDRs are increasing day-by-day, mainly driven by new applications and services in wireless communication systems. Design and development of a SDR has inherently numerous challenges due to the contradicting nature of flexibility and efficiency requirements. However, this provides tremendous opportunities and calls for a radical change in the way such complicated systems are built. One promising approach, like [23], that has the potential to provide implementation flexibility even in a fixed hardware platform, is the WDL based waveform development using a library of algorithmic kernels. This approach promises not only the participation of vendors by standardization and open interfaces, but also provides algorithmic and implementation flexibility even in a fixed hardware platform.

V. RF TRENDS IN FLEXIBLE RADIO

The digital communication research on multi-standard radio has started based on the assumption of the Software Radio, which extrapolated that RF stages of a radio would be transparent for the baseband processing either thanks to highly flexible RF components or to very high speed converters. Both have shown limitations and further research is needed to achieve highly flexible SDR. In fact, too major approaches emerge for designing a flexible RF. The first one considers very large band RF that can therefore accommodate several systems. This approach suffers from bad sensitivity level though. The second one relies on tuneable components with which parameters can be adapted to match the system requirements. These rules often contradict the guidelines that RF designer are used to consider when defining an RF architecture, which is usually optimised for sensitivity, power consumption, and IC integration.

At the transmitter side, classical approaches usually result in low flexibility architectures sketched in Fig. 7.

In such designs, lump elements freeze the circuit performance to given specifications. Thus, this classical circuitry will hardly be adaptable. Multi-standard terminals based on this concept end up with a RF front-end comprising several RF ICs in parallel, also referred to as the Velcro approach. In order to come up with a less costly and bulky approach, new architectures in which the boundary between the analog and digital world has been modified to enable the use of waveform shaping in the digital domain has been proposed.

For instance [24] suggests using a LInear amplifier with Non linear Components (LINC) architecture to efficiently address large Peak to Average Power Ratio (PAPR) OFDM signals. The advantage of this approach is that amplifiers have to handle constant envelop signals despite the non constant envelop nature of the OFDM signal. This leads to better power efficiency and better flexibility, especially when the signals are shaped in the digital domain [25]. Despite its higher flexibility, this architecture still hardly copes with wide band signals and cannot be tuned over a large central frequency range. This is mainly due to the limited flexibility offered by nowadays analog stages.

Similarly, the trend at the receiver side is to limit the number of analog components. The hype for zero-IF or low

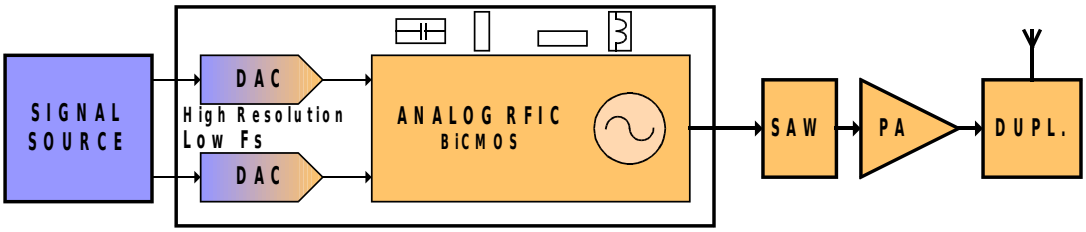

Fig. 7. Classical TX architecture

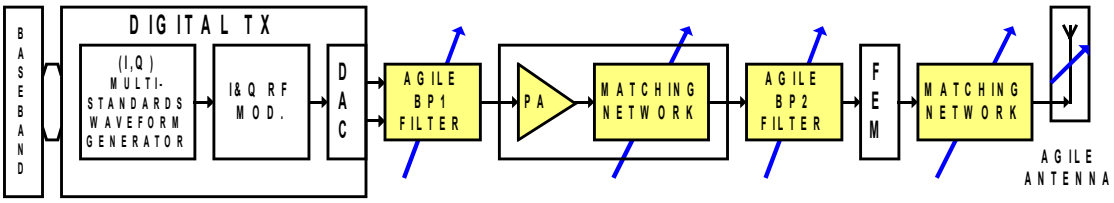

Fig. 8. Flexible TX architecture

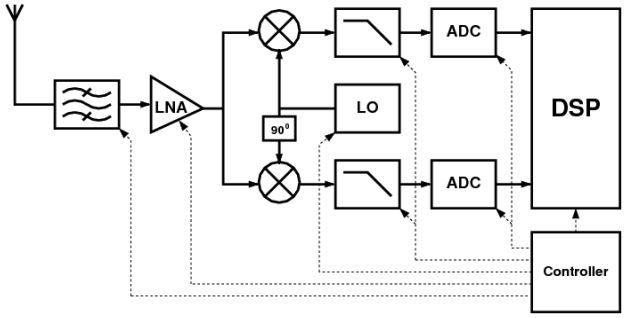

Fig. 9. Flexible zero-IF RX architecture

IF architectures in the past few years partly came from this trend.

The zero-IF architecture (Fig. 9) has indeed several fundamental advantages over its heterodyne counterpart. The intermediary IF stages are removed and the functions of channel selection and subsequent amplification at a nonzero IF are replaced by low-pass filtering and baseband amplification, for which a monolithic integration is feasible. Although zero-IF exhibit relevant specifications, it suffers from well identified problems such as DC offset, LO leakage and I/Q mismatch (the first being the most prominent one). The low-IF receiver concept has been developed to avoid these drawbacks. Fundamentally the low-IF receiver originates from the conventional heterodyne receiver system. The main difference is that the digitization process is shifted from the baseband part to the IF part. By implementing A/D conversion at this earlier stage, more flexibility at the receiver can be achieved. The concept of low-IF has become even more attractive recently, especially for emerging systems which require higher transceiver flexibility while keeping the terminals' compact size and energy efficient. There are several benefits that can be obtained by implementing early conversion, namely: the high degree of programmability at the receiver, and the avoidance of issues associated with analog baseband demodulation, such as I/Q imbalance, DC offset, etc. Despite all these supporting facts, there is still one main obstacle for implementing such architecture: it requires a fast high-bandwidth high-dynamic-range conventional ADC for converting radio signal with sufficient fidelity. Therefore, improving the performance of ADC is crucial to enhance the flexibility of RF receivers. Besides the performance, power consumption of the conversion stages is a matter of concern to integrate such solutions in low power battery operated devices.

Even when limiting the analog part of the transceiver, the use of tuneable filtering is needed, each filter being dedicated to the given bandwidth of the targeted system. RF filtering has always been considered as the bottleneck of the front-end implementation and making it tuneable represents a huge challenge [26]. For instance, Bulk Acoustic Wave (BAW) filters are highly selective band-pass filters that are convenient for a particular application. However, even if BAW filters are tuneable in frequency, this is only limited to a few percents, and tuning control is quite complex to implement in practice. Besides, practical implementations based on Yttrium Iron Garnet (YIG) resonators provide multioctave bandwidths and high quality-factor resonators. However, they consume a significant amount of dc power (1 to 3 W), and their linearity is poor. Moreover they are bulky, expensive and cannot be easily miniaturized for wireless communications. Alternatively, diode varactor-tuned circuits are simple and require little bias current and size, but they have not met the expectations in terms of loss. Solid-state varactors can provide a wide tuning range, but they have loss and linearity problems at microwave frequencies. Therefore, low cost and high performance tuneable solid state resonators is still a myth. Besides solid state solutions, RF MEMS can provide a relevant alternative. Being constructed entirely of low loss metals and dielectrics, these mechanical structures feature inherently low loss properties.

VI. Conclusion

Recent trends in silicon technology and communication system demands exhibit a growing gap between application

needs and what the technology can deliver. A key driver for the telecom industry is the wireless mobile business. Mobility, which relies on battery operated handheld devices, provide stringent requirements on equipments in terms of processing power, power consumption and flexibility. At the same time the battery and silicon technology does not progress at the same pace. The emergence of new standards implementing ever more efficient air interfaces also put stringent constraints on the design time. Thus, the reuse of hardware building blocks and a proper methodology and tools are needed to evaluate hardware performance tradeoffs at the earliest stage. Flexible radio is a promising approach in this regard. However, a unified framework is still to be found to enable the co-design of communication functions and hardware platforms.

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