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Compact Modeling of Multi-layered MoS_2 FETs including Negative Capacitance Effect

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***Abstract*—In this paper, we present a channel thickness dependent analytical model for MoS_2 symmetric double-gate FETs including negative capacitance (NC) effect. In the model development, first thickness dependent model of the baseline 2D FET is developed, and later NC effect is included in the model using the Landau-Khalatnikov (L-K) relation. To validate baseline model behavior, density functional theory (DFT) calculations are taken into account to obtain numerical data for the K and Λ valley dependent effective masses and differences in the energy levels of N-layer (N = 1, 2, 3, 4, and 5) MoS_2. The calculated layer dependent parameters using DFT theory are further used in a drift-diffusion simulator to obtain electric characteristics of the baseline 2D FET for model validation. The model shows excellent match for drain current and total gate capacitance of baseline FET and NCFET against the numerical simulation.**

***Index Terms*—Metal-oxide-semiconductor field-effect transistor (MOSFET), Compact modeling, molybdenum disulfide (MoS_2), transition metal dichalcogenide (TMD), Double Gate (DG), Negative Capacitance FET (NCFET).**

I. Introduction

To obtain performance improvement in a field-effect-transistor (FET) characteristics with scaling, many techniques are being explored and replacing silicon in the channel region with an alternative material is one of the attractive and viable option. The potential alternative materials being explored are germanium, silicon-germanium, III-V group materials, 2D materials etc. In the 2D materials, layered semiconductors like TMDs [1]–[4] (such as MoS_2, $MoTe_2$, WSe_2) along with phosphorene [5], monochalcogenides [6], [7] etc. have drawn attention owing to their atomic-scale thickness, superior transport properties over silicon, and dangling-bond free interfaces for the post-silicon era [8]–[10]. In addition to geometrical scaling, application of negative capacitance has been demonstrated in conventional silicon and TMD channel based devices to achieve power supply scaling [11]–[14].

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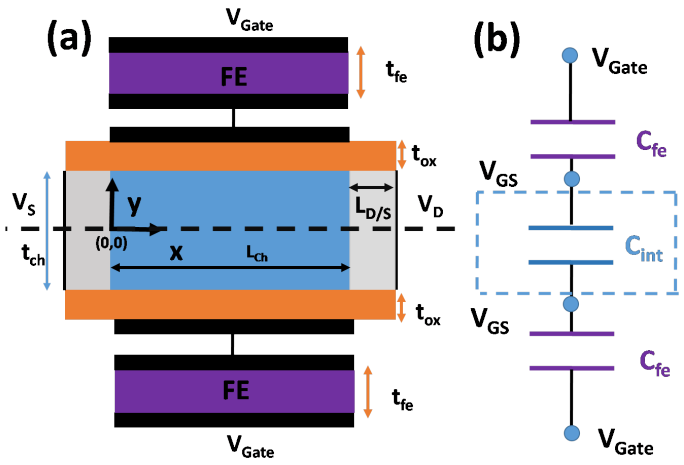

Fig. 1: (a) Schematic of the MoS_2 symmetric Double Gate (DG) Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) Negative Capacitance (NC) transistor with SiO_2 as insulator (dielectric). In the schematic t_{fe} represents thickness of ferroelectric, t_{ox} represents the oxide thickness and $t_{ch} = N_{layer}t_{layer}$ represents the thickness of the channel where t_{layer} is the thickness of mono-layer MoS_2 and N_{layer} is the number of MoS_2 layers. V_{Gate}, V_S and V_D represents applied voltages at gate, source and drain terminal with respect to the source terminal, respectively. The length of channel and drain/source region are represented by L_{ch} and $L_{D/S}$, respectively. (b) Simplified capacitance network for the same. In which V_{GS} is the gate to source voltage of baseline FET, C_{int} is the capacitance of baseline FET, and C_{fe} is capacitance of ferroelectric capacitor.

The emergence of a large number of 2D layered materials led to remarkable progress in the growth of large-scale mono-layer to few layers MoS_2 using different methods [15]–[17]. Application of the TMD based FETs has already been demonstrated in an inverter, a NAND gate, a static random access memory (SRAM), and a five-stage ring oscillator based on a direct-coupled transistor logic technology [18]. Among TMDs, MoS_2 has been projected as one of the most promising candidate for low power electronics because of its electronic properties [19]–[22].

SPICE models are an integral part of EDA tools to estimate the performance of a circuit before its large-scale production. Recently, significant efforts have been made in developing a compact model for TMD material based FETs to estimate the circuit performance based on these devices [23]–[28]. The model presented in [23] has formulated the electrostatics from an equivalent lumped capacitive network and only includes drift component of drain current. The models presented in [24]–[28] are developed assuming mono-layer TMD in the

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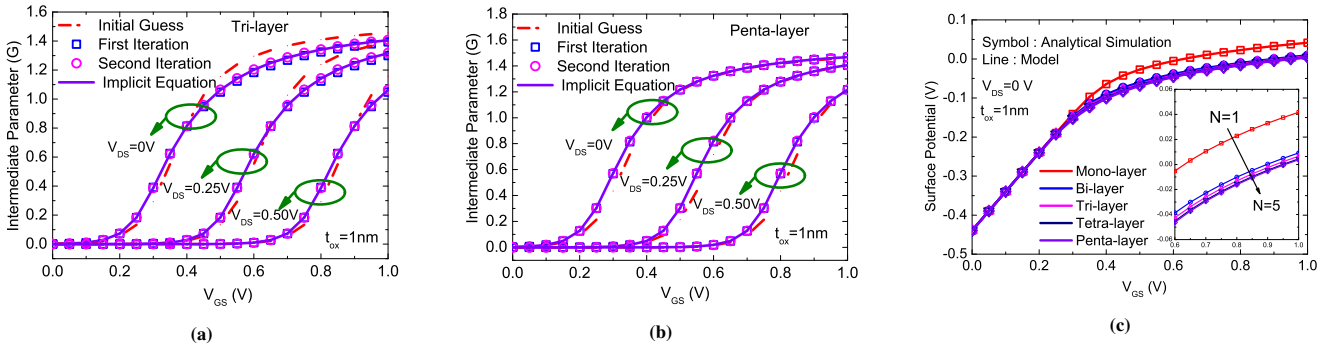

Fig. 2: Validation of explicit solution of intermediate term G against its numerical simulation obtained from (15) for (a) tri-layer and (b) penta-layer. In this validation, 1 nm thick SiO_2 is used as a gate oxide thickness. The solution of G after the second iteration shown by the circle is excellently capturing the numerical simulation data of implicit equation. (c) Validation of compact explicit solution of surface potential against the numerical simulation data obtained from (10) and (15) for mono-layer to penta-layer double-gate FETs at V_{DS} = 0 V.

channel with negligible variation in the potential along the channel thickness. Since multilayer TMDs show encouraging results [29]–[32], therefore a dedicated model is required to cover the device behaviour from mono-layer to multilayer. The assumption of constant potential along channel thickness will not be valid as the channel thickness increases from mono-layer to multilayer.

In this work, we present a surface potential based compact model for drain current of multilayer MoS_2 symmetric double-gate structure including NC effect extending our previous IEEE EDTM-2019 work [33]. In this model, by including the effect of the channel thickness, the current is calculated using Drift-Diffusion transport. The work is presented as follows: section II describes model formulation, result and discussion is presented in section III and finally conclusion in section IV.

II. Model Formulation

A. Mobile Carrier Density

The band-structure of N-layer MoS_2 along high symmetry direction $\Gamma - K - \Lambda - \Gamma$ is adopted from Fig. 1 (a) of the previous work [34]. In conduction band, several energy bands exist at Λ-valley and one degenerate energy band at the K-valley that are very close in energy. In particular, the valley degeneracy at the K-valley is 2N, while at the Λ-valley there are N energy levels, with 6-fold valley degeneracy, where N is the number of layers. For modeling purpose, we have considered only the minimum of the conduction band at the K-valley and the minima of the first two energy levels at the Λ-valley.

The model of MoS_2 based DG-FET is developed by considering the effect of two most relevant valleys i.e. the minima of conduction band at K-valley (E_K) and the minima of first two energy levels at Λ-valley (E_{Λ_1} and E_{Λ_2}), as discussed earlier. The density of state (DOS) corresponding to K-valley and Λ-valley are calculated as follows:

$$D_K = \frac{g_s g_{V_K} m_K}{2\pi\hbar^2}\, U(E - E_K)$$
$$D_\Lambda = \frac{g_s g_{V_\Lambda} m_\Lambda}{2\pi\hbar^2} \sum_i U(E - E_{\Lambda_i}) \quad (1)$$

where D_K and D_Λ are the DOS corresponding to K-valley and Λ-valley, $\hbar$ is the reduced Planck's constant, g_s is the spin degeneracy, $g_{V_{K/\Lambda}}$ and $m_{K/\Lambda}$ are the valley degeneracy and effective mass corresponding to K/Λ-valley, respectively, and U is the step function. Note that E_{Λ_1} and E_{Λ_2} have the same valley degeneracy and effective mass for N-layer MoS_2.

To develop a more accurate model, differences in energy levels ΔE_1 and ΔE_2 are taken into account, where $\Delta E_1 = E_{\Lambda_1} - E_K$ and $\Delta E_2 = E_{\Lambda_2} - E_K$. Now using Fermi-Dirac distribution, mobile charge carrier density (n) can be written as follows:

$$n = \int_{E_K}^{\infty} D_K f(E - E_F) dE + \int_{E_K + \Delta E_1}^{\infty} D_\Lambda f(E - E_F) dE + \int_{E_K + \Delta E_2}^{\infty} D_\Lambda f(E - E_F) dE \quad (2)$$

where $f(E - E_{E_F})$ represents the Fermi-Dirac (FD) distribution function. Note that in the calculation of charge density in (2), contribution of both valleys (K and Λ) are included.

Using D_K and D_Λ from (1) into (2), n can be written as follows:

$$n = n_K + n_{\Lambda_1} + n_{\Lambda_2} \quad (3)$$

where

$$n_k = D_K kT \ln\left[1 + e^{\left(\frac{E_F - E_K}{kT}\right)}\right]$$

$$n_{\Lambda_1/\Lambda_2} = D_\Lambda kT \ln\left[1 + e^{\left(\frac{E_F - E_K - \Delta E_{1/2}}{kT}\right)}\right]. \quad (4)$$

where k is the Boltzmann constant and T is the temperature in Kelvin.

It is noticeable that (4) has terms in form of $\ln(1+\exp(x))$ and using these equations in (3) to obtain charge density requires the integration of $\ln(1 + \exp(x))$. This integration is complex and involves polylogarithmic function ($Li_2(x)$),

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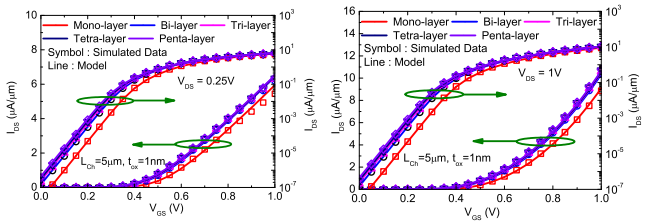

Fig. 3: Comparision of transfer characteristic of model against simulation data of baseline DG-FET. The channel length of the DG-FET is $5\ \mu m$ and oxide thickness t_{ox} is 1 nm while channel thickness varies from mono-layer to penta-layer. Transfer characteristics in panel (a) and (b) are shown at $V_{DS} = 0.25\ V$ and $V_{DS} = 1.0\ V$, respectively.

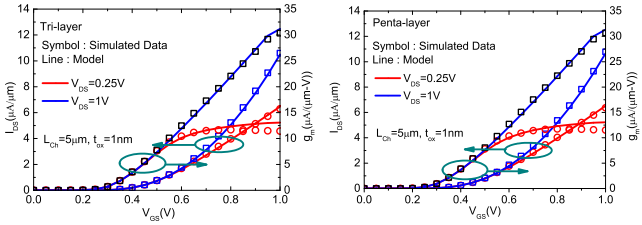

Fig. 4: Validation of transconductnace (g_m) of model against simulation data of baseline DG-FET. The channel length of the DG-FET is $5\ \mu m$ and oxide thickness t_{ox} is 1 nm. The transconductnace is shown for tri-layer and penta-layer in (a) and (b), respectively.

which introduces complexity in the compact model development. Thus, the Maxwell-Boltzmann (MB) distribution is used further in the model development.

In (4), substituting E_K by $-q\phi_s$, E_F by $-qV$ (where q is the electronic charge) and using MB approximation, charge density in (3) can be expressed as follows:

$$n = De^{\left(\frac{\phi_s - V}{V_t}\right)}\ , \tag{5}$$

where

$$D = \left[D_K kT + D_\Lambda kT e^{\left(\frac{-(\Delta E_1 + \Delta E_2)}{kT}\right)}\right]\ . \tag{6}$$

In (5), $V_t = kT/q$ is thermal voltage and V is the electron quasi-Fermi potential.

In the next section, (5) is used to calculate the surface potential in terms of external applied terminal voltages which is further used to develop drain current model.

B. Modeling of Surface potential

For the undoped or lightly doped channel, using the gradual-channel approximation (GCA) [35], the Poisson's equation along the thickness of the channel can be written as follows [36], [37]:

$$\frac{d^2\phi(y)}{dy^2} = \frac{qD}{\epsilon_{ch} N_{layer} t_{layer}} e^{\left(\frac{(\phi_s - V)}{V_t}\right)}\ . \tag{7}$$

Applying the symmetric boundary condition ($d\phi(y)/dy = 0$ at $y = 0$) and integrating (7), we obtain:

$$\frac{d\phi(y)}{dy} = \sqrt{\frac{2qDV_t}{N_{layer} t_{layer}}\left(e^{\left(\frac{\phi(y) - V}{V_t}\right)} - e^{\left(\frac{\phi_o - V}{V_t}\right)}\right)} \tag{8}$$

where ϕ_o is the potential at center of the channel thickness (at y=0 in Fig. 1 (a)). The surface potential ϕ_s can be obtained by integrating (8) from $y = 0$ to $y = t_{ch}/2$ in y-direction corresponding to $\phi = \phi_o$ to $\phi = \phi_s$. After integration of (8), obtained potential at any point along thickness ($\phi(y)$) and at surface (ϕ_s) can be written as follows.

$$\phi(y) = \phi_o - 2V_t \ln\left[\cos\left(\frac{2Gy}{t_{ch}}\right)\right] \tag{9}$$

and

$$\phi_s = V - 2V_t \ln\left[\frac{t_{ch}}{2G}\sqrt{\frac{qD}{2V_t t_{ch}\epsilon_{ch}}}\cos G\right] \tag{10}$$

where

$$G = \frac{t_{ch}}{2}\sqrt{\frac{t_{ch}\epsilon_{ch}}{2qDV_t}} e^{\left(\frac{\phi_o - V}{2V_t}\right)}\ . \tag{11}$$

In (11), the range of G is 0 to $\pi/2$ (at $y = t_{ch}/2$, in (9) the argument of cosine cannot exceed $\pi/2$).

Further, boundary condition at the interface of MoS_2 and SiO_2 form a relation between the G, t_{ox}, ϕ_s and V_{GS} and is expressed as follows:

$$C_{ox}(V_{GS} - V_{FB} - \phi_s) = \epsilon_{ch}\left.\frac{d\phi}{dy}\right|_{y=\frac{t_{ch}}{2}} \tag{12}$$

where

$$\left.\frac{d\phi}{dy}\right|_{y=\frac{t_{ch}}{2}} = \frac{4V_t G \tan G}{t_{ch}}\ . \tag{13}$$

Using (12) into (10), an implicit expression in terms of G can be obtained as follows:

$$\left[\frac{V_{GS} - V_{FB} - V}{2V_t}\right] + \ln\left[\frac{t_{ch}}{2G}\sqrt{\frac{q}{2V_t t_{ch}\epsilon_{ch}}}\cos G\right] = \frac{2\epsilon_{ch} t_{ox}}{\epsilon_{ox} t_{ch}} G\tan G \tag{14}$$

Simplifying (14), we have -

$$\ln G - \ln\cos G + sG\tan G = H \tag{15}$$

where

$$s = \frac{2\epsilon_{ch} t_{ox}}{\epsilon_{ox} t_{ch}} \tag{16}$$

and

$$H = \ln\left[\frac{t_{ch}}{2}\sqrt{\frac{qD}{2V_t t_{ch}\epsilon_{ch}}}\right] + \left[\frac{V_{GS} - V_{FB} - V}{2V_t}\right]\ . \tag{17}$$

Since ϕ_s is a function of G and the calculation of G requires a numerical solution, which reflects that ϕ_s also needs

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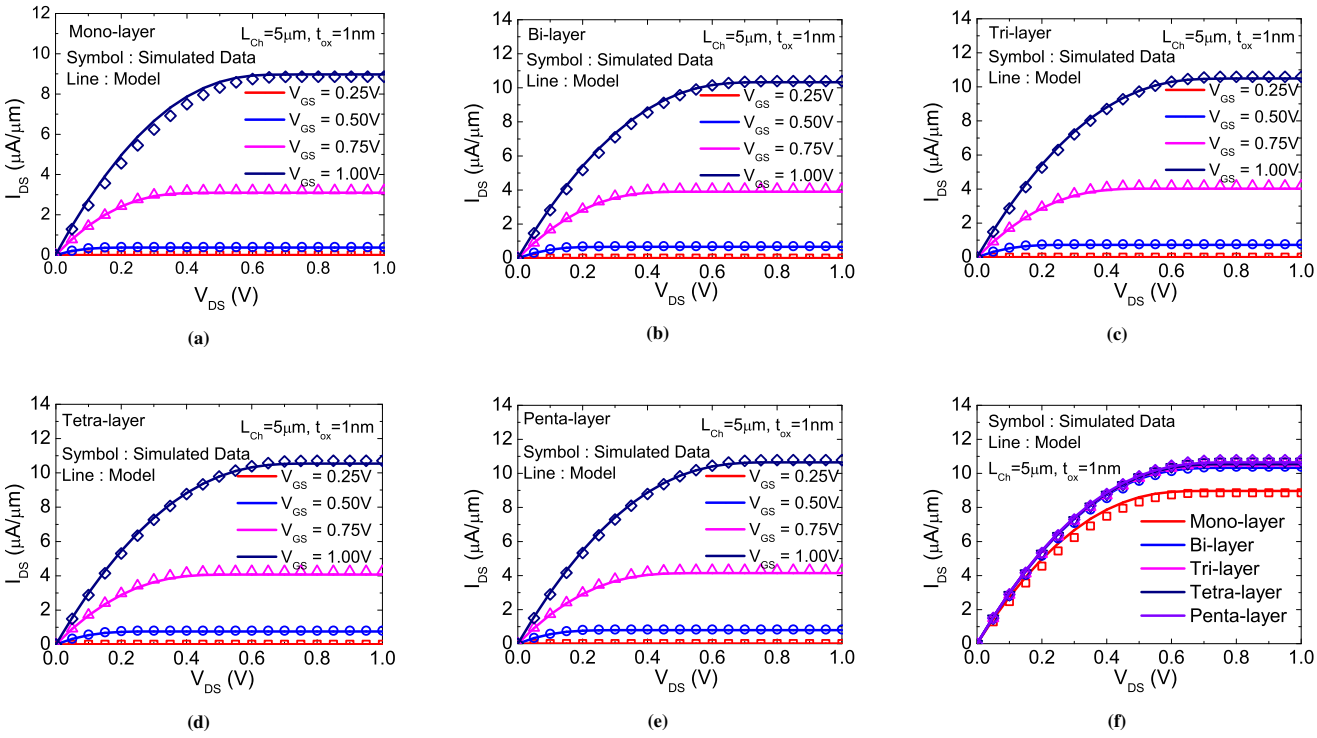

Fig. 5: Validation of output characteristic of baseline DG-FET of channel length (L_{Ch}) = 5 μm, and t_{ox} = 1 nm for (a) mono-layer, (b) bi-layer, (c) tri-layer, (d) tetra-layer, and (e) penta-layer with model at different values of V_{GS} = 0.25 V, 0.50 V, 0.75 V, and 1 V. (f) shows the validation of layer-dependent output characteristics at $V_{GS} = 1V$.

a numerical solution. To perform fast circuit simulation, an explicit solution of (15) is desirable to improve computational efficiency of the model. The explicit solution of G using (15) can be obtained by following these two steps:

1 Use range of G to obtain initial guess of the ϕ_o. In this process, using the maximum value of G (i.e. $\pi/2$), the maximum value of ϕ_o is obtained while the minimum value of ϕ_o is $V_{GS}-V_{FB}$. Further a unified ϕ_o is obtained using ϕ_{omax} and ϕ_{omin} as follows:

$$\phi_o = MIN[\phi_{omin}, \phi_{omax}, \Delta] \tag{18}$$

In (18), the expression of MIN function is given as :

$$MIN[a, b, \Delta] = \frac{1}{2}\Big[(a+b) - \sqrt{(a-b)^2 + \Delta}\Big] \ . \tag{19}$$

where Δ is the smoothing parameter.

2 Now, the initial guess for G is obtained by using the calculated value of ϕ_o (from (18)) in (11). The accuracy of obtained initial guess of G is further improved by subtracting a correction (θ) term determined by using Halley's method [38]. The accuracy of G is improved by using only two iterations, as follows:

$$\begin{aligned} G_1 &= G_0 - \theta\big|_{G=G_0} \\ G_2 &= G_1 - \theta\big|_{G=G_1} \end{aligned} \tag{20}$$

where

$$\theta = \frac{g}{g'}\left[1 + \frac{gg''}{2g'^2}\right] \ . \tag{21}$$

In (21), g' and g'' are first and second derivative of g with respect to G, respectively, and g is defined as follows:

$$g = \ln G - \ln\cos G + sG\tan G - H \ . \tag{22}$$

1.

C. Drain Current Model

Drain current (I_{DS}) model is obtained using drift-diffusion transport [39], which can be written as [40]:

$$I_{DS} = W\mu Q\frac{dV}{dx} = W\mu Q\frac{dV}{dG}\frac{dG}{dx} \tag{23}$$

From Gauss's law, total mobile charge density (Q) can be estimated as :

$$Q = 2\epsilon_{ch}\frac{d\phi}{dy}\bigg|_{y=\frac{t_{ch}}{2}} = \frac{8\epsilon_{ch}V_t G\tan G}{t_{ch}} \tag{24}$$

In (23), W represents channel width, μ represents charge mobility, and Q represents total mobile charge per unit area. Differentiating (15) with respect to G to obtain dV/dG and then integrating (23) from source (i.e. $x = 0$, $V = 0$, and

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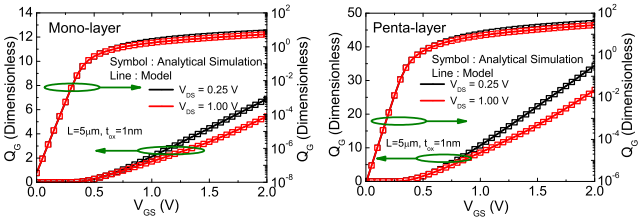
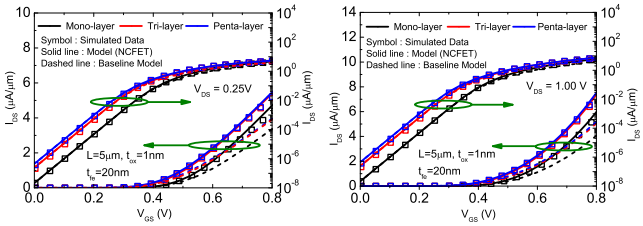


(a) (b)

Fig. 6: Validation of Q_G against its numerical simulation obtained using (30) for (a) mono-layer and (b) penta-layer at 0.25 V and 1V value of V_{DS}. In this validation, 1 nm thick SiO_2 is used as a gate oxide thickness.



(a) (b)

Fig. 7: Comparision of transfer characteristic of model against simulation data for symmetric MoS_2 DG-NCFET. The channel length of both DG-NCFET and baseline is 5 μm, ferroelectric thickness t_{fe} is 20 nm, and oxide thickness t_{ox} is 1 nm. For mono-layer, tri-layer and penta-layer at $V_{DS} = 0.25\ V$ in panel (a) and at $V_{DS} = 1.0\ V$ in panel (b).

$G = G_S$) to drain (i.e. $x = L$, $V = V_{DS}$, and $G = G_D$), I_{DS} can be written as follows:

$$I_{DS} = \frac{\mu W}{L}\frac{16\epsilon_{ch}}{t_{ch}}V_t{}^2[f(G_S) - f(G_D)] \tag{25}$$

where

$$f(G_S) = G_S \tan G_S - \frac{1}{2}G_S{}^2 + \frac{1}{2}s(G_S \tan G_S)^2$$
$$f(G_D) = G_D \tan G_D - \frac{1}{2}G_D{}^2 + \frac{1}{2}s(G_D \tan G_D)^2 \ . \tag{26}$$

Explicit solution of the G_S and G_D can be obtained from discussion presented in previous subsection, therefore, using the explicit solution of G_S and G_D, an explicit solution of I_{DS} is achieved.

D. Negative Capacitance (NC) Effect

The NCFET can be considered as baseline FET in series with ferroelectric capacitor, as shown in Fig. 1 (b). Therefore, the applied gate voltage (V_{Gate}) to the NCFET can be written as :

$$V_{Gate} = V_{fe} + V_{GS} \tag{27}$$

where, V_{GS} is the voltage at the gate of baseline FET and V_{FE} is the voltage across the ferroelectric. The voltage across ferroelectric (V_{fe}) can be related to charge per unit area of ferroelectric (Q_{fe}) using the Landau-Khalatnikov (L-K) theory of ferroelectric [41] and written as :

$$V_{fe} = 2\alpha t_{fe}Q_{fe} + 4\beta t_{fe}Q_{fe}^3 + 6\gamma t_{fe}Q_{fe}^5 \tag{28}$$

where α, β and γ are material dependent parameters, also called Landau parameters, and t_{fe} is the thickness of ferroelectric film.

Q_{fe} is gate charge (Q_G) per unit area for baseline FET. Therefore, once Q_G is known, we can calculate V_{fe} using (28) and V_{GS} from (27). Finally, drain current can be calculated using (25).

1) Calculation of Gate Charge (Q_G): The gate charge can be obtained by integrating mobile charge density (Q) along the channel. The mathematical expression can be written as :

$$Q_G = -W\int_0^L Q dx = -\frac{W^2\mu}{I_{DS}}\int_{G_S}^{G_D} Q^2\frac{dV}{dG}dG \tag{29}$$

Using Q from (24) into (29) and integrating (29) along channel, the simplified form of Q_G can be written as-

$$\frac{Q_G}{WL} = \frac{8V_t\epsilon_{ch}}{t_{ch}}\left[\frac{g(G_D) - g(G_S) - \int_{G_S}^{G_D} G^2\tan G dG}{f(G_S) - f(G_D)}\right] \tag{30}$$

where

$$g(G) = \frac{(G\tan G)^2}{2} + s\frac{(G\tan G)^3}{3} \tag{31}$$

To calculate Q_G, we need to integrate $G^2\tan G$. This integration is complex and involves polylogritmic function of order two and three, which complicates the compact model development.

Here, we have used Taylor's series expansion of $\tan G$ to evaluate the integral $G^2\tan G$ and hence Q_G. The Taylor's series expansion of $\tan G$ can be written as [42] :

$$\tan G = G + \frac{1}{3}G^3 + \frac{2}{15}G^5 + \frac{17}{315}G^7 + \frac{62}{2835}G^9 + o(x^{11}) \tag{32}$$

The gate capacitance of baseline and NCFET can now be calculated using (30) and (28).

III. Results and Discussion

In the baseline FET model development, expressions of the surface potential, drain current and mobile charge density are expressed in from of intermediate parameter "G". Since "G" is in implicit form and to make the proposed model explicit, "G" is expressed in the explicit form. Therefore, first validation of the explicit form of "G" against numerical simulation of its implicit form expressed in (15) is presented in Fig. 2 (b-c) for tri-layer and penta-layer. A close agreement between the explicit and numerical solution of G is obtained after two iterations using the Halley's method. Further, compact model of the surface potential of the baseline FET is verified with numerical simulation of (15) and (10) at V_{DS} = 0 V (see Fig. 2 (c) for all five layers). The inset of Fig. 2 (c) shows the magnified view of surface potential which is in good agreement with the numerical simulation results for mono-layer to penta-layer devices.

The proposed drain-current model of basline FET is validated against the numerical simulation data, with SiO_2 as

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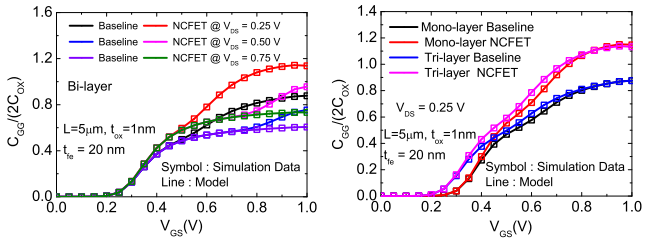

Fig. 8: Comparision of normalized gate capacitance for (a) baseline DG-FET and (b) DG-NCFET with baseline DG-FET. The channel length of the both DG-NCFET and baseline is 5 μm, ferroelectric thickness t_{fe} is 20 nm, and oxide thickness t_{ox} is 1 nm.

gate dielectric and MoS_2 as channel material. A detailed information about device parameters used in the numerical simulation is listed in table-I. The Validation of transfer characteristics and transconductance (g_m) of baseline DG-FET are shown in Fig. 3 (a-b) and Fig. 4 (a-b) respectively. The model prediction shows good agreement with simulated data. The ouput characteristics of baseline DG-FET for all five layers at different value V_{GS} (ranging between 0 to 1 V with interval of 0.25V) are validated and shown in Fig. 5 (a-e). Fig. 5 (f) shows a comparative prediction of output characteristics of model and simulation data for all five layers at $V_{GS} = 1V$, where the model shows a consistent behavior with the change in the layer thickness against simulation data. Note that the current is almost the same beyond mono-layer which can be understood with the help of valley switching in the band structure as we move from mono-layer to multi-layer. For mono-layer, majority of the mobile charge carrier density is contributed by K-valley because the minima of the conduction band is located at K-valley, and other lowest energy levels at Λ (E_{Λ_1} and E_{Λ_2}) valley are at higher in energy. As the number of layers increases, K-valley moves upwards and therefore Λ-valley becomes the conduction band minima with energy level E_{Λ_1}. Beyond mono-layer, K-valley lies in between E_{Λ_2} and E_{Λ_1}, where E_{Λ_1} is lowest in energy. With an increase in the number of layers, these energy levels (E_K, E_{Λ_1}, and E_{Λ_2}) come closer and in turn results in an increase in carrier density.

In modeling of NC effect using the L-K relation, modeling of the total gate charge (Q_G) is an essential requirement. In this process, the total gate charge is formulated in subsection D of section II. The obtained expression of the Q_G has a term of integral (integral of $G^2 \tan G$) which leads to involvement of polylogarithm terms. Since polylogarithm is not desirable for the fast simulation in a compact model development. Therefore, to obtain an explicit expression for the Q_G, Taylor series expansion of the $\tan G$ upto 9^{th} power of G is used in the integration. The obtained explicit form of Q_G is shown against numerical solution of (30) in Fig. 6 (a-b). Further, the transfer characteristic of NCFET is validated against simulated data and shown in Fig. 7 (a-b). In Fig. 8 (a), the validation of normalized gate capacitance for baseline FET with bi-layer MoS_2 channel at different value of V_{DS} is shown. The validation of normalized gate capacitance of NCFET and baseline at V_{DS}= 0.25V for mono-layer and tri-layer is shown in Fig. 8 (b). The model shows excellent match with simulated data. In the simulation and model, $Hf_{0.5}Zr_{0.5}O_2$ is used as ferroelectric material for gate-stack with thickness of 20 nm. The Landau parameters are adopted from [13] and used in simulation and modeling. Note that in model validation, V_{FB}, μ, ΔE_1 and ΔE_2 are used as a parameter.

TABLE I: Device Parameters Used in Simulation

Device Parameter	Value
Channel Length (L_{Ch})	$5\mu m$
Channel Permittivity (ϵ_{ch})	$4.8\epsilon_o$
Channel mobility (μ)	50 $cm^2/(V-s)$
Channel electron affinity	4.3 eV
S/D region length $L_{S/D}$	200 nm
Oxide thickness (t_{ox})	1 nm
Oxide Permittivity (ϵ_{ox})	3.9 ϵ_o
Oxide electron affinity	1.15 eV
Drain/Source contact work function	4.3 eV
Gate contact work function	4.75 eV

IV. CONCLUSION

In this paper, an explicit thickness dependent surface potential based compact model of baseline MoS_2 channel DG-FET is presented. In addition to the baseline model, thickness dependent model considering the negative capacitance effect is also presented using the L-K relation. Both the baseline and negative capacitance models are verified against the numerical simulation data. The model behavior shows excellent agreement with numerical simulation data for mono-layer to penta-layer of MoS_2 in the channel region. The explicit nature and excellent agreement of model against simulation data reflects model suitability for complex circuit simulation designed using DG-FETs of mono-layer to penta-layer MoS_2.

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