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Hybrid Transformerless PV Converters with Low Leakage Currents: Analysis and Configuration

Zhongting Tang¹, Yongheng Yang¹, Jianghu Wan^{2*}, Frede Blaabjerg¹

¹ Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark

² School of Automation, Central South University, Changsha 410083, China

* E-mail: wanjianghu@csu.edu.cn

Abstract: This paper proposes a type of hybrid transformerless PV converters with simultaneous AC and DC outputs. It is specifically suitable for residential PV systems due to its high efficiency, versatility and flexibility, while maintaining lower leakage currents. The proposed converter is configured by replacing the control switch of the boost converter with a transformerless voltage source inverter (VSI), enabling multiple outputs. In addition, a symmetrical boost-inductor is adopted to clamp the common-mode voltage (CMV) as a constant, resulting in low leakage currents. To illustrate the configuration principle, a hybrid converter with a highly efficient and reliable inverter concept (HERIC) as the VSI is exemplified. Besides, the dedicated modulation scheme for the proposed converter is detailed to achieve low leakage currents, reactive power injection and high efficiency. Furthermore, as the shoot-through state of inverter legs is allowable for the proposed converter, i.e., no need to add deadtime, the reliability and power quality of the proposed converter can be improved. Simulations and experimental tests are performed on an example hybrid converter (with an HERIC as the VSI) to validate the analysis.

1 Introduction

The photovoltaic (PV) energy is becoming competitive among various renewable energy sources (i.e., wind, solar thermal, hydro and wave energy) [1]. Attractive policy incentives and the continuous declining price of PV modules enable the fast development of low- and medium-power PV systems for modern commercial and residential applications [2]. As the key to the interface of the PV energy and grid, a smart inverter with high versatility (i.e., multiple sources and loads), high power density, high reliability, high efficiency and high flexibility in grid-supporting is of interest in such applications [3], [4].

In terms of PV system configurations, the prior-art hybrid converters typically have two structures, as shown in Fig. 1, where one PV source is simultaneously converted to DC and AC power at multiple buses. The hybrid converters can be used to convert the PV energy directly (i.e., the input voltage is sufficient) or indirectly (i.e., adding a DC-DC converter after the PV input to achieve a wider range of input voltages, as the optional DC-DC converter shown in Fig. 1). As it is observed in Fig. 1(a), the separated power conversions (i.e., a DC-DC converter and an inverter) are connected to the PV source [5], [6]. In this case, although the DC output is generated by a DC-DC converter and the AC output is obtained through the inversion stage, high costs associated with large system volume are generally incurred. Besides, the disadvantages of the separated cells also exist in the traditional hybrid converter (e.g., high voltage and current stress, and large power losses of the control switch in boost converter [7], and severe distortions due to the deadtime and minimum pulse width limitation of the inverter [8], [9]). Thus, to reduce the system cost, while achieving high power density and increasing reliability, the stand-alone hybrid converter was introduced [10]-[12], as shown in Fig. 1(b). Its main advantages include: (1) inherent shoot-through capability eliminates the damage risk caused by external interferences (i.e., alleviating the electromagnetic interference-EMI) and decrease the distortion induced by the deadtime effects [8], [9]; (2) fewer power devices are used to perform both DC-DC and DC-AC conversions, compared to the configuration in Fig. 1(a) (i.e., high power density but low system costs are possible). For example, [10] proposed a family of hybrid converter topologies with

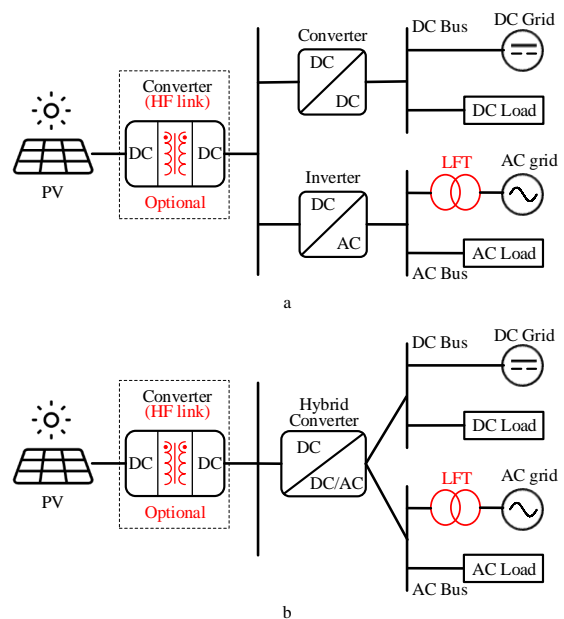


Fig. 1: Hybrid power converter Structures for PV applications

a Separated converters

b Stand-alone hybrid converters

one AC and one DC output, where the switch of the boost converter is replaced by a voltage-source-inverter (VSI). In addition, [11] and [12] introduced two split-source inverters to enhance the compactness, efficiency, flexible power flow and voltage-boosting.

However, when applied to PV systems, the above hybrid converters, which includes the traditional hybrid converters and the stand-alone hybrid converters in [10]-[12], have to address the leakage current issue, as required in the strict grid standards [13], [14]. Thus, either high-frequency transformers (HFTs) or low-frequency transformers (LFTs) are installed between the PV panels and the

AC power grid, as shown in Fig. 1, where the HF-link DC/DC converter contains a DC/AC conversion, an HFT and an AC/DC conversion. Although the effective galvanic isolation can be attained, the converter with transformers has low power density and high system cost. To achieve multiple outputs and simultaneously low leakage currents, a transformerless hybrid converter was proposed in [15], where the VSI is replaced by a dual-buck inverter to clamp the common-mode voltage (CMV) to zero in each operation mode. Although achieving low leakage current, the dual-buck inverter has compromised on power density and system cost due to the inefficient utilization of the AC filter inductors [16].

Notably, many topologies [17] and modulation methods have been reported to suppress the leakage currents for single-phase transformerless inverters in the literatures, including the full-bridge inverter with a hybrid modulation scheme [18], DC-decoupling inverters [18], [20], AC-decoupling inverters [21]-[24], etc. Among the above inverters, the highly efficient and reliable inverter concept (HERIC) with improved modulation strategies has better performances in leakage current suppression, high efficiency and reactive power injection due to its symmetrical structure [23], [25]. It is worth noting that the reactive power injection, required by standards, e.g., the IEEE Std 1547-2018, is critical in grid-friendly and flexible PV systems [14]. When compared to the hybrid converter with stand-alone type [10]-[12], [15], the above transformerless inverters do not have shoot-through protection capability. That is, deadtime is required in practice, decreasing the power quality of the grid current.

With the above concerns, to achieve simultaneous AC and DC outputs and to ensure low leakage currents, this paper proposes a type of hybrid transformerless converters, where the inductor of the conventional boost converter is split into two symmetrical ones (placed at the positive and negative DC rails), as shown in Fig. 2(a) [26]. In addition, the switch of the conventional boost converter is replaced with a transformerless VSI, which maintains a constant CMV, and thus, low leakage currents. The configuration principle is demonstrated on the converter taking the HERIC (i.e., owning reactive power injection with the improved modulation method mentioned above) as the VSI in Section II. Moreover, the modulation and operation modes (i.e., including the operation principle and CMV analysis) of the proposed converter is presented in detail. In Section III, the steady-state analysis, component design and control strategy are given. Then, Section VI presents the losses analysis and comparisons with prior-art hybrid converters. Due to the shoot-through capability and symmetrical structure, the proposed converter with the dedicated modulation method can achieve good performances in terms of low leakage currents, high power quality, reactive power injection, high efficiency, and high reliability, while maintaining low system costs. Simulation and experimental results are provided in Section V, which validates the effectiveness of the proposed hybrid transformerless power converter. Finally, Section VI gives concluding remarks.

2 Configuration Principle of the proposed hybrid transformerless converter

2.1 Configuration of the proposed converter

The general configuration of the proposed transformerless hybrid converter is illustrated in Fig. 2(a). As shown in Fig. 2(a), the following principles are considered when deriving the hybrid converters: (1) two symmetrical boost inductors (i.e., L_{b1} and L_{b2} with $L_{b1}=L_{b2}$) are placed at the positive and negative DC rails; (2) a transformerless VSI, which can clamp the CMV to be half of the DC input voltage, is adopted to replace the control switch of the boost converter; (3) a power diode D and an output capacitor C_{DC} are used for the DC-DC conversion to supply DC loads as well as absorbing the pulsating power generated by the VSI; (4) symmetrical output L -type filters are used for good current quality and also to reduce the impact from the differential-mode voltage (DMV), where $L_{ac1}=L_{ac2}=L_{ac}/2$. Furthermore, the leakage current path is also exemplified in Fig. 2(a), where Z_{GcGd} is the impedance between the PV parasitic capacitor C_{PVg} and the ground, and i_{leak} is the leakage

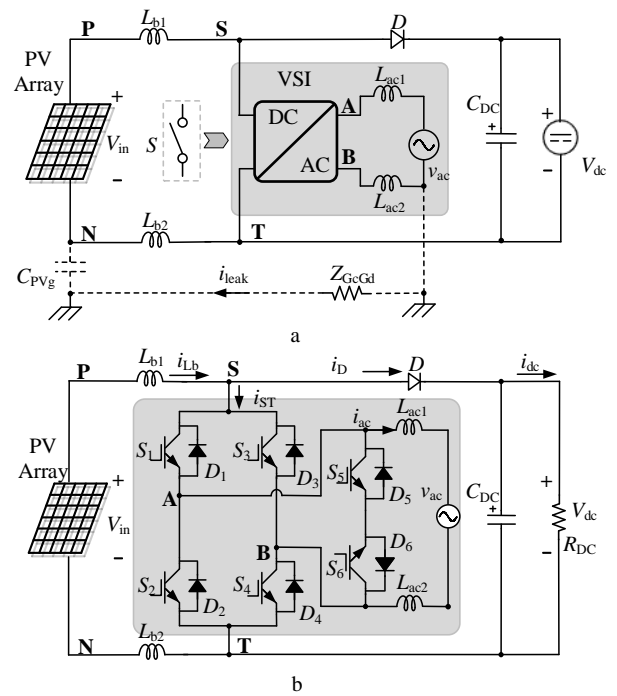


Fig. 2: Hybrid power converter Structures for PV applications
a General configuration
b Hybrid converter with the HERIC as the VSI

current. In Fig. 2, **P** and **N** are the positive and negative terminals of the DC input, **S** and **T** are the positive and negative input terminals of the VSI with **A** and **B** being its output terminals.

In this paper, the above configuration principle is further elaborated on an HERIC-based hybrid converter. According to Fig. 2(a), the VSI of the hybrid transformerless converter can be replaced by an HERIC topology (i.e., including the power devices S_{1-6} with the anti-parallel diodes D_{1-6}) [23], as shown in Fig. 2(b). Moreover, V_{in} , V_{dc} and v_{ac} are the DC input voltage, the DC output voltage and the AC output voltage, respectively. i_{Lb} is the current of the symmetrical boost inductors, i_{ST} is the VSI input current, i_D is the power diode current, and i_{dc} is the DC load current. Furthermore, i_{ac} is the grid current and its positive direction is defined as the direction from the VSI to the AC grid. Operation modes and the CMV analysis of the proposed converter are then detailed considering a DC load R_{DC} and an AC grid.

2.2 Modulation

For simplicity, only the continuous conduction mode is considered when the hybrid converter is operating as a boost converter. Fig. 3(a) shows the modulation method of the proposed converter, where a triangular carrier is adopted, d represents the duty cycle of the shoot-through interval (i.e., representing the ratio of the on-time to the switching period time in a boost converter) and m_U is the duty cycle of the modulation signal with the improved modulation method for the HERIC (i.e., being the same as the unipolar pulse width modulation (PWM)) [25]. Accordingly, there are four operation modes of the proposed converter, i.e., **ST**, **Pv**, **Nv**, and **Zv-ST** is the shoot-through mode, **Pv** represents the mode of the differential-mode voltage v_{dm} being positive ($v_{dm} = +V_{dc}$), **Nv** denotes the mode of v_{dm} being negative ($v_{dm} = -V_{dc}$), and **Zv** indicates the mode of v_{dm} being zero ($v_{dm} = 0$).

According to the zoomed-in view of Fig. 3(a) in one switching cycle T_{sw} , as shown in Fig. 3(b), the operation modes can be expressed as

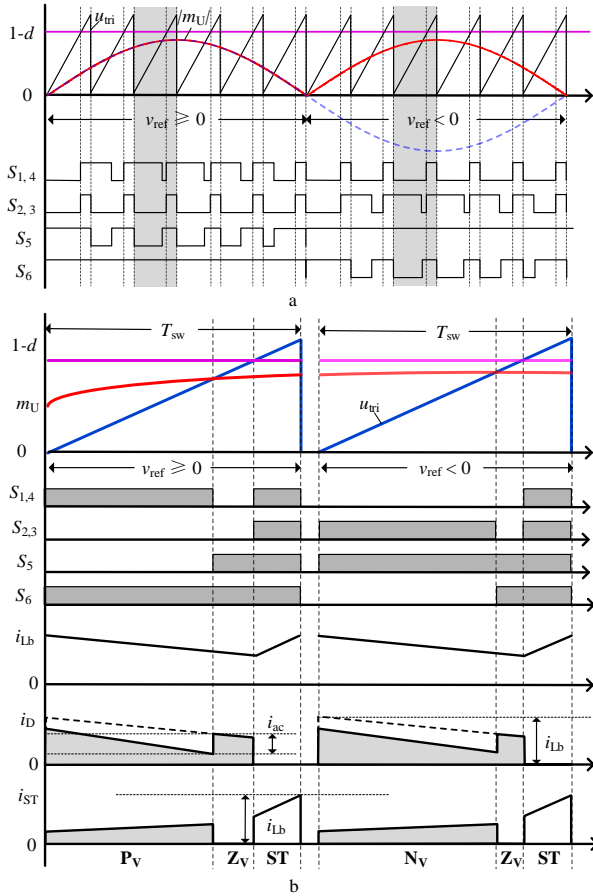


Fig. 3: Modulation scheme of the proposed converter, where d represents the **ST** interval and m_U is the modulation signal
a Modulation scheme
b key current waveforms

$$Mode \Leftrightarrow \begin{cases} \mathbf{Pv}, & 0 \leq u_{tri} < |m_U|, v_{ref} > 0 \\ \mathbf{Nv}, & 0 \leq u_{tri} < |m_U|, v_{ref} < 0 \\ \mathbf{Zv}, & |m_U| \leq u_{tri} < 1 - d \\ \mathbf{ST}, & 1 - d \leq u_{tri} \leq 1 \end{cases}$$

where u_{tri} is the carrier amplitude.

Key waveforms (i_{Lb} , i_D and i_{ST}) are also given in Fig. 3(b). Clearly, i_{Lb} increases in the **ST** mode to boost the voltage and it decreases in other modes (**Pv**, **Nv** and **Zv**). Based on the Kirchhoff's current law, at the node **S**, the current can be expressed as

$$i_{Lb} = i_{ST} + i_D \quad (1)$$

which is consistent with that in Fig. 3(b). Notably, although the HERIC can also generate three voltage levels, i.e., zero voltage during the **ST** and **Zv** mode, $+V_{dc}$ during the **Pv** interval and $-V_{dc}$ for the **Nv** interval, there are only two voltage levels changing (i.e., between $+V_{dc}$ and 0 or $-V_{dc}$ and 0) in half a cycle.

2.3 Analysis of Common Mode Voltage

When the voltage of parasitic capacitance C_{pv_g} (see Fig. 2) changes at a high frequency, large leakage currents will be generated. Then, it increases system power losses, induces EMI issues, and poses serious safety problems to personnel and other equipment [27]. According to the VDE 0126 [13], the distributed generation system must be triggered within a certain time to ensure safety, when the leakage current exceeds 300 mA (RMS– root-mean-square value). To

achieve a low leakage current, the CMV must be a constant or vary at a very low frequency. Assuming $L_{ac1} = L_{ac2}$, the DMV impact on the leakage current can be neglected. According to Fig. 2(a), the CMV v_{cm} and the DMV (v_{dm}) of the proposed converter can be given as

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} \quad (2)$$

$$v_{dm} = v_{AT} - v_{BT} \quad (3)$$

where v_{AN} and v_{BN} are the voltages of terminals **A** and **B** to **N**, v_{AT} and v_{BT} are the voltages of terminals **A** and **B** to **T**, and v_{ST} represents the voltage of the terminal **S** to **T**, respectively.

Fig. 4 shows the four operation modes (i.e., **ST** mode, **Pv** mode, **Nv** mode and **Zv** mode) and their equivalent circuits, where C_{g1-4} is the corresponding junction capacitance of the switches S_{1-4} . Then, the CMV and DMV can be analyzed in different modes as follows.

a) **ST** mode: Fig. 4(a)-(c) illustrates the **ST** mode, during which the HERIC is taken as a boost switch (i.e., S_{1-6} are ON). Then, L_{b1} and L_{b2} are charged by the DC input source. As shown in Fig. 3(b), the boost inductor current i_{Lb} increases, and $V_{Lb1} = V_{Lb2} = V_{in}/2$. The power diode D is reverse-biased, and $i_D = 0$. The capacitor C_{DC} is discharged to supply the load R_{DC} . Fig. 4(c) presents the equivalent circuit of the **ST** mode, where the CMV is clamped by L_{b1} and L_{b2} , and the terminal voltages $v_{AN} = v_{BN} = V_{Lb2}$, and $v_{AT} = v_{BT} = 0$. Then, the voltages v_{cm} and v_{dm} can be expressed as

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} = \frac{V_{Lb2} + V_{Lb2}}{2} = \frac{V_{in}}{2} \quad (4)$$

$$v_{dm} = v_{AT} - v_{BT} = 0 - 0 = 0 \quad (5)$$

The HERIC operates in a freewheeling interval at this time. As shown in Fig. 4(a) and (b), there are three bidirectional current paths for the grid current i_{ac} . When $i_{ac} \geq 0$, i_{ac} can flow through S_6 and D_5 , S_4 and D_2 , and S_1 and D_3 (i.e., the pink components in Fig. 4(a)). While $i_{ac} < 0$, as seen as the pink components in Fig. 4(b), the three current paths are flowing through S_5 and D_6 , S_2 and D_4 , and S_3 and D_1 .

b) **Pv** mode: As it is shown in Fig. 4(d)-(f), the HERIC operates as a VSI in the positive half-cycle (i.e., $v_{ref} \geq 0$). S_1 , S_4 and S_6 are ON, while S_2 , S_3 and S_5 are OFF to achieve $v_{dm} = +V_{dc}$. As demonstrated in Fig. 3(b), the boost current i_{Lb} decreases and it simultaneously flows through the diode D and the HERIC. The capacitor C_{DC} is then charged, and the charging voltage is $v_{ST} = V_{dc} = V_{in} + V_{Lb1} + V_{Lb2}$. Additionally, v_{ST} provides the DC load voltage. As shown in Fig. 4(f) (i.e., the equivalent circuit of the **Pv** mode), the terminal voltages are $v_{AN} = V_{in} + V_{Lb1}$, $v_{BN} = -V_{Lb2}$, $v_{AT} = V_{in} + V_{Lb1} + V_{Lb2}$, and $v_{BT} = 0$. the voltages v_{cm} and v_{dm} in this operation mode are calculated as

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} = \frac{V_{in} + V_{Lb1} - V_{Lb2}}{2} = \frac{V_{in}}{2} \quad (6)$$

$$v_{dm} = v_{AT} - v_{BT} = V_{in} + V_{Lb1} + V_{Lb2} - 0 = V_{dc} \quad (7)$$

where the symmetrical filter voltages are equal, i.e., $V_{Lb1} = V_{Lb2}$. Regarding the HERIC, there is a bidirectional current path for the grid current i_{ac} in the **Pv** mode, as presented in Fig. 4(d) and (e). $i_{ac} \geq 0$, i_{ac} flows through S_1 and S_4 to achieve $v_{dm} = V_{dc}$ (i.e., the pink components in Fig. 4(d)); $i_{ac} < 0$, i_{ac} flows through D_1 and D_4 to achieve $v_{dm} = V_{dc}$ (i.e., the pink components in Fig. 4(e)).

c) **Nv** mode: As presented in Fig. 4(g)-(i), the HERIC works in the negative half-cycle (i.e., $v_{ref} < 0$) as a VSI. In this case, S_2 , S_3 and S_5 are ON, while S_1 , S_4 and S_6 are OFF to achieve $v_{dm} = -V_{dc}$. In the **Nv** mode, the key current waveforms are shown in Fig. 3(b), where the boost filters are in discharging mode to support the operation of the HERIC, to charge the capacitor C_{DC} and to supply the DC load. Moreover, as it is observed in Fig. 4(i) (i.e., the equivalent circuit of the **Nv** mode), the terminal voltages are $v_{ST} = V_{dc} = V_{in} + V_{Lb1} + V_{Lb2}$, $v_{AN} = -V_{Lb2}$, $v_{BN} = V_{in} + V_{Lb1}$, $v_{AT} = 0$ and $v_{BT} = V_{in} + V_{Lb1} + V_{Lb2}$. Hence, v_{cm} and v_{dm} can be given by

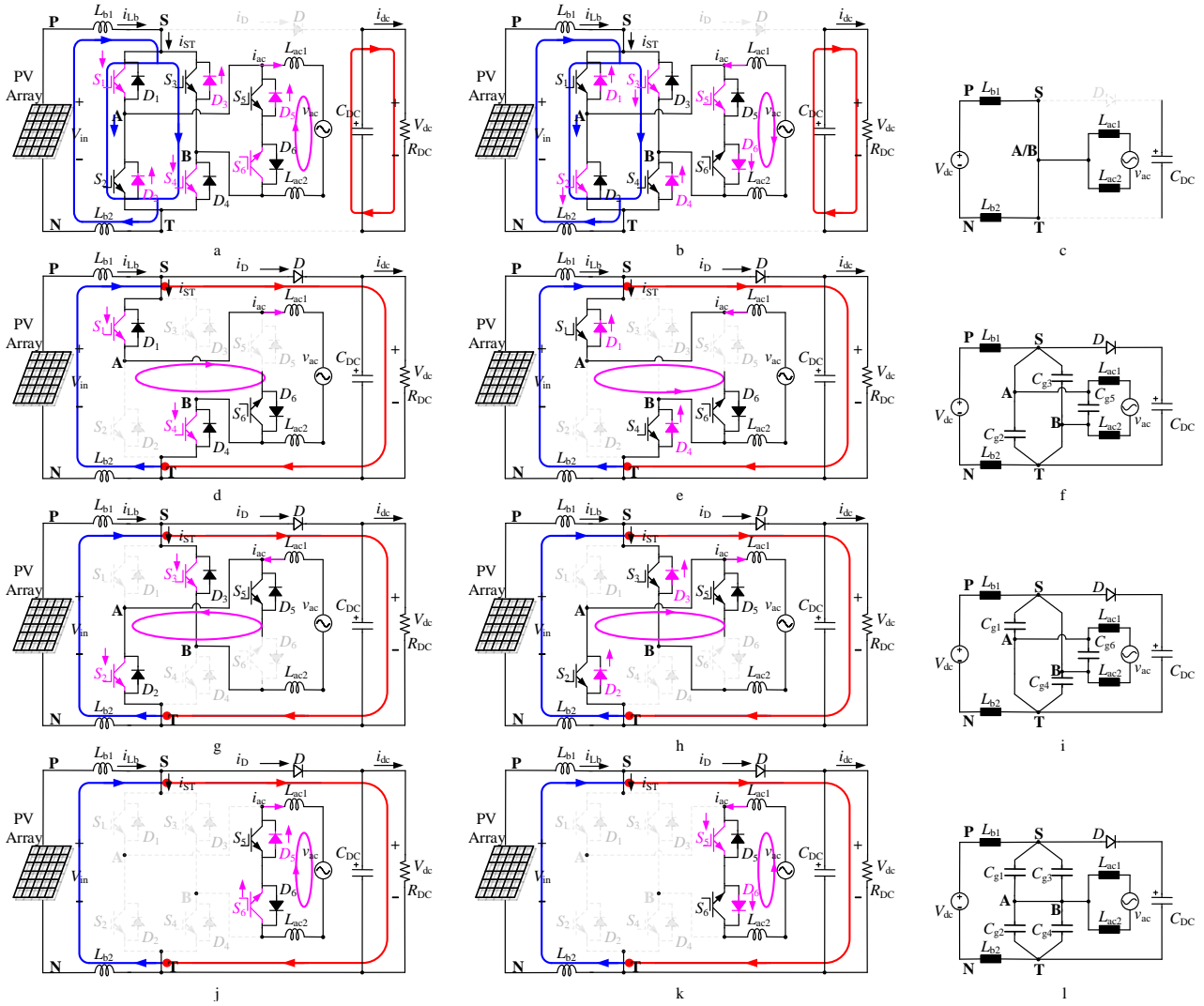


Fig. 4: Operation modes and their equivalent circuits of the proposed symmetrical transformerless hybrid converter

a ST mode, $i_{ac} \geq 0$; b ST mode, $i_{ac} < 0$; c ST mode, equivalent circuit;
d Pv mode, $i_{ac} \geq 0$; e Pv mode, $i_{ac} < 0$; f Pv mode, equivalent circuit;
g Nv mode, $i_{ac} \geq 0$; h Nv mode, $i_{ac} < 0$; i Nv mode, equivalent circuit;
j Zv mode, $i_{ac} \geq 0$; k Zv mode, $i_{ac} < 0$; l Zv mode, equivalent circuit

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} = \frac{-V_{Lb2} + V_{in} + V_{Lb1}}{2} = \frac{V_{in}}{2} \quad (8)$$

$$v_{dm} = v_{AT} - v_{BT} = 0 - (V_{in} + V_{Lb1} + V_{Lb2}) = -V_{dc} \quad (9)$$

in which $V_{Lb1} = V_{Lb2}$. As depicted as Fig. 4(g) and (h), the HERIC can also provide a bidirectional current path. When $i_{ac} \geq 0$, i_{ac} flows through S_2 and S_3 to obtain $v_{dm} = -V_{dc}$, as shown as the pink components in Fig. 4(g). When $i_{ac} < 0$, i_{ac} flows through D_2 and D_3 to achieve $v_{dm} = -V_{dc}$, as presented as the pink components in Fig. 4(h).

d) **Zv mode:** In this case, as shown in Fig. 4(j)-(l), S_5 and S_6 are ON and S_{1-4} are OFF. According to the key current waveforms in Fig. 3(b), i_{Lb} decreased and the boost inductors provide power to the output capacitor and DC load simultaneously. Then, the CMV is clamped by the switch junction capacitors C_{g1-4} (i.e., assuming $C_{g1} = C_{g2} = C_{g3} = C_{g4}$), as depicted as Fig. 4(l). Consequently, the voltage of those junction capacitances V_{Cg1-4} can be expressed as

$$V_{Cg1-4} = \frac{V_{in} + V_{Lb1} + V_{Lb2}}{2} \quad (10)$$

Notice that the terminal voltages are $v_{AN} = V_{Cg2} - V_{Lb2}$, $v_{BN} = V_{Cg4} - V_{Lb2}$, $v_{AT} = V_{Cg2}$ and $v_{BT} = V_{Cg4}$, and $V_{Lb1} = V_{Lb2}$, v_{cm}

and v_{dm} in Fig. 4(l) can be obtained as

$$v_{cm} = \frac{v_{AN} + v_{BN}}{2} = \frac{(V_{Cg2} - V_{Lb2}) + (V_{Cg4} - V_{Lb2})}{2} = \frac{V_{in}}{2} \quad (11)$$

$$v_{dm} = v_{AT} - v_{BT} = V_{Cg2} - V_{Cg4} = 0 \quad (12)$$

Similarly, the grid current i_{ac} has a bidirectional path (i.e., shown in Fig. 4(j) and (k)). i_{ac} flows through S_6 and D_5 when $i_{ac} \geq 0$, as shown as the pink components in Fig. 4(j). i_{ac} flows through S_5 and D_6 when $i_{ac} < 0$, as demonstrated as the pink components in Fig. 4(k).

According to the above analysis, the proposed converter can clamp the CMV to be half of the input voltage V_{in} in all operation modes, i.e., Eqs. (4), (6), (8), and (11). In addition, it can achieve the bidirectional current path in any operation mode. Therefore, it has a good performance in terms of low leakage currents and flexible reactive power injection (due to the possibility of bidirectional current flow).

3 System Design

3.1 Steady-state Analysis

Considering a single-switch boost converter [28], the relationship between the DC input voltage V_{in} and the DC output voltage V_{dc} can be expressed as

$$\frac{V_{dc}}{V_{in}} = \frac{1}{1-d} \quad (13)$$

which illustrates that the DC gain of the hybrid converter is also $1/(1-d)$. The HERIC output will be zero at this moment. Furthermore, the duty cycle of the modulation signal for the DC-AC conversion i.e., m_U can be calculated as

$$m_U = \frac{v_{ac}}{V_{dc}} = \frac{v_{ac}(1-d)}{V_{in}} \quad (14)$$

Since the DC-DC and DC-AC conversions should be finished in one switching cycle, d and m_U should be bounded as:

$$d + m_U \leq 1 \quad (15)$$

Accordingly, the maximum value of the modulation signal must be $m_{Umax} \leq 1-d$, resulting in that the peak of the AC output voltage V_{acpeak} should be constrained as:

$$V_{acpeak} = m_{Umax} V_{dc} \leq \frac{V_{in}(1-d)}{1-d} = V_{in} \quad (16)$$

implying that the input voltage V_{dc} must be larger than the peak grid voltage V_{acpeak} to ensure simultaneous DC and AC outputs. This is also the case for conventional VSIs. Notably, the DC-DC gain is adjustable from 1 to infinity in theory.

Moreover, the AC output can be connected to a grid or loads, while the DC output can also be connected to a DC grid or DC loads. This paper focuses on the low leakage currents and the reactive power injection in the AC side of the proposed converter. Thus, a passive DC load and a grid are considered. As mentioned previously, when applied to PV systems, the hybrid converter can be used to convert the PV energy directly or indirectly. Therefore, if the proposed converter is employed in a single-stage grid-connected PV system, the control strategies should adopt an effective operation [29]. Thus, when designing the control scheme for the proposed converter, the following should be considered:

1) $V_{acpeak} \leq V_{in} \leq V_{dc}$. The hybrid converter simultaneous output DC and AC power. Generally, the PV input voltage is fluctuating in a small range under various irradiance conditions [29]. Thus, the operation of the hybrid converter will not be affected when the fluctuating voltage is within this range of $[V_{acpeak}, V_{dc}]$.

2) $V_{acpeak} > V_{in}$. The hybrid converter acts as the conventional boost converter, and the AC grid can be disconnected to ensure the modulation of the VSI according to Eq. (16), or the PV energy can be transmitted to DC output. As an alternative, the boost inductor can be replaced by a symmetrical impedance network [30] in a way to improve the boosting.

Notably, there are limitations for the AC and DC output power due to the unidirectional conduction of the power diode D [10]. Hence, the pulsating power of the VSI only can be absorbed by the DC output capacitor C_{DC} , and then consumed at the DC output. That is, the power limitation of the proposed converter can be expressed as

$$P_{dc} \geq P_r \quad (17)$$

where P_{dc} represents the DC output power, and $P_r = 0.5V_m I_m \cos(2\omega + \varphi)$ is the instantaneous pulsating power with V_m and I_m being the amplitudes of the grid voltage and current, and φ being the displacement angle. Therefore, the proposed converter can only be operated as a boost converter instead of a VSI, if one output is needed.

3.2 Component Design

The passive components of the hybrid converter include the symmetrical boost inductors L_{b1} and L_{b2} (i.e., $L_{b1} = L_{b2}$), the DC output capacitor C_{DC} and the symmetrical L -type filter L_{ac1} and L_{ac2} (i.e., $L_{ac1} = L_{ac2}$). Since the AC output filters can be designed following the rules of the prior-art grid-connected VSIs [17]-[24], the design of L_{ac1} and L_{ac2} of the proposed converter is not discussed in this paper. To ensure the operation, L_{b1} , L_{b2} and C_{DC} should be properly designed in the following.

1) *Boost inductors* L_{b1} and L_{b2} : The design of the boost inductors is related to the current ripple ratio γ , and the optimal value of γ is 0.4 when considering the overall stresses and power density in a converter [31]. Therefore, the boost inductors of the proposed converter can be designed as

$$L_{b1} = L_{b2} = \frac{L_b}{2} \geq \frac{V_{in}d}{\gamma I_{Lb} f_{sw}} \quad (18)$$

where L_b represents the total inductance of the boost inductors, I_{Lb} is the average value of the boost inductor current i_{Lb} , and f_{sw} is the switching frequency.

2) *DC output capacitor* C_{DC} : The DC output capacitor for the proposed converter is designed to maintain and filter the DC output voltage. At the same time, it balances the pulsating power of the VSI. When considering the DC output ripple voltage of the boost converter, i.e., ΔV_{dc} , C_{DC} should be designed as

$$C_{DC} \geq \frac{I_{dc}d}{\Delta V_{dc} f_{sw}} \quad (19)$$

where I_{dc} is the average value of the DC output current i_{dc} . Seen from the energy storage perspective, large inductance is generally required to store the same amount of energy, when compared to capacitors. That is, inductors have low cost-effectiveness to balance the inherent pulsating power. Hence, only the DC-link capacitor is considered for the conventional single-phase VSI to maintain power density [32]. Considering the power balance, C_{DC} should be

$$C_{DC} \geq \frac{P_r}{\omega V_{dc} \Delta V_r} \quad (20)$$

in which ΔV_r is the required pulsating voltage, ω is the grid frequency, and P_r is the instantaneous pulsating power, respectively. According to Eqs. (18) and (19), the output capacitor C_{DC} can be selected as

$$C_{DC} = \max\left(\frac{I_{dc}d}{\Delta V_{dc} f_{sw}}, \frac{P_r}{\omega V_{dc} \Delta V_r}\right) \quad (21)$$

3.3 Basic Control

To simplify the control, the PV input voltage V_{in} is assumed as a constant. The control for the proposed converter includes two parts, as shown in Fig. 5. One is the voltage loop with a proportional-integral (PI) controller for the DC output, where V_{dc}^* is the voltage reference. The other is a proportional-resonant (PR) controller $G_{pr}(s)$ with multi-resonant controllers $G_{nr}(s)$ for the AC regulation, which can achieve zero-error tracking and improve the power quality [8]. Moreover, I_{ref} is the amplitude of the reference current i_{ac}^* , and the phase angle θ is achieved through the PLL of v_{ac} (i.e., performing grid synchronization). In addition, only one resonant controller $G_{3r}(s)$ is adopted for simplicity. In all, good performances in terms of fast dynamics and good power quality can be achieved in this way.

4 Comparison Analysis

4.1 Losses Analysis and Comparison

The losses analysis and comparison are carried out when the proposed converter adopts IGBT power devices. According to [33], the

Table 1 Loss Analysis and Comparison of the Systems in Figs. 2(b) and 6, Supplying the Same Loads.

Converter	Conduction losses due to i_{Lb}	Conduction losses due to i_{ac} (ST mode)	Conduction losses of D	Switching losses
Proposed converter	$2V_{ce0}I_{Lb} + r_c I_{Lb}^2$	$(V_{ce0} + V_{d0})\frac{2I_m}{\pi} + (r_c + r_d)\frac{I_m^2}{6}$	$V_{d0}I_{dc} + r_d I_{dc}^2$	$(E_{onT} + E_{offT})\frac{f_{sw}V_{dc}I_{Lb}}{V_{CC}I_{CC}} + (E_{offT} + E_{onD})\frac{2f_{sw}V_{dc}I_m}{\pi V_{CC}I_{CC}}$
Two-stage inverter	$V_{ce0}I_{Lb} + r_c I_{Lb}^2$	$(V_{ce0} + V_{d0})\frac{2I_m}{\pi} + (r_c + r_d)\frac{I_m^2}{2}$	$V_{d0}(\frac{2I_m}{\pi} + I_{dc}) + r_d(\frac{I_m^2}{2} + \frac{4I_m I_{dc}}{\pi} + I_{dc}^2)$	$(E_{onT} + E_{offT})\frac{f_{sw}V_{dc}I_{Lb}}{V_{CC}I_{CC}} + (E_{onT} + E_{offT} + E_{onD})\frac{2f_{sw}V_{dc}I_m}{\pi V_{CC}I_{CC}}$

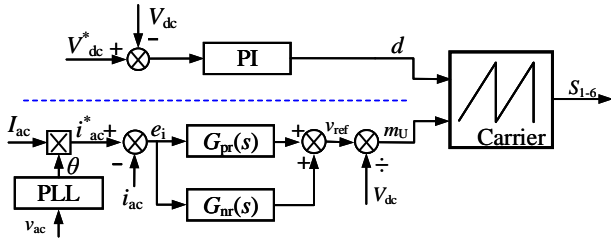


Fig. 5: General control block diagram for the proposed converter

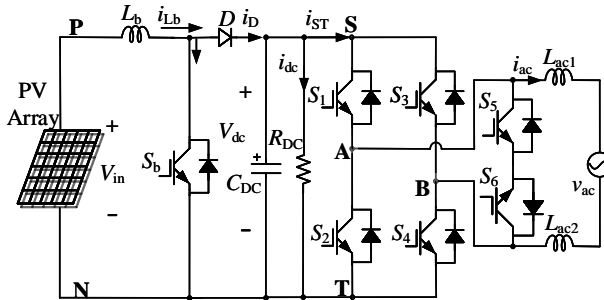


Fig. 6: Traditional two-stage inverter with the HERIC as the VSI, where S_b is the boost control switch, the boost converter operates as the ST mode, and the HERIC inverter is in the freewheeling interval

IGBT losses consist of the conduction losses, switching losses and negligible blocking losses. the proposed converter is then compared with the traditional two-stage inverter with an HERIC, as shown in Fig. 6, in terms of power losses. For a fair comparison, the two-stage inverter supplies a DC load R_{CD} at the DC link, as demonstrated in Fig. 6.

Conduction Losses: The IGBT conduction losses can be calculated as

$$P_{CT} = \frac{1}{T_{sw}} \int_0^{T_{sw}} (V_{ce0}i_c + r_c i_c^2) dt = V_{ce0}I_{cav} + r_c I_{crms}^2 \quad (22)$$

in which V_{ce0} is the IGBT on-state zero-current collector-emitter voltage, and r_c represents the collector-emitter on-state resistance [33]. In addition, I_{cav} and I_{crms} are the average and RMS IGBT currents. Similarly, the anti-parallel diode conduction losses can be expressed as

$$P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} (V_{d0}i_d + r_d i_d^2) dt = V_{d0}I_{dav} + r_d I_{drms}^2 \quad (23)$$

where V_{d0} is the diode on-state zero-current voltage, r_d represents the diode on-state resistance [33], and I_{dav} and I_{drms} are the average and RMS diode currents, respectively.

When operating in the inversion, the conduction losses are identical in both the proposed converter and the traditional two-stage

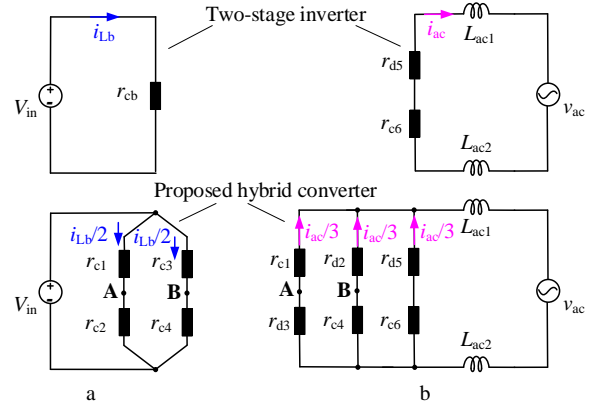


Fig. 7: Equivalent circuits of the systems when S_b is ON or in the ST mode, where the upper diagrams are the equivalent circuits of two-stage inverter in Fig. 6, and the lower ones are those of the proposed converter, the IGBT on-state resistance is $r_{cb} = r_{c1-6} = r_c$, and the diode on-state resistance are $r_{d1-6} = r_d$.

a Boost operation
b Freewheeling operation

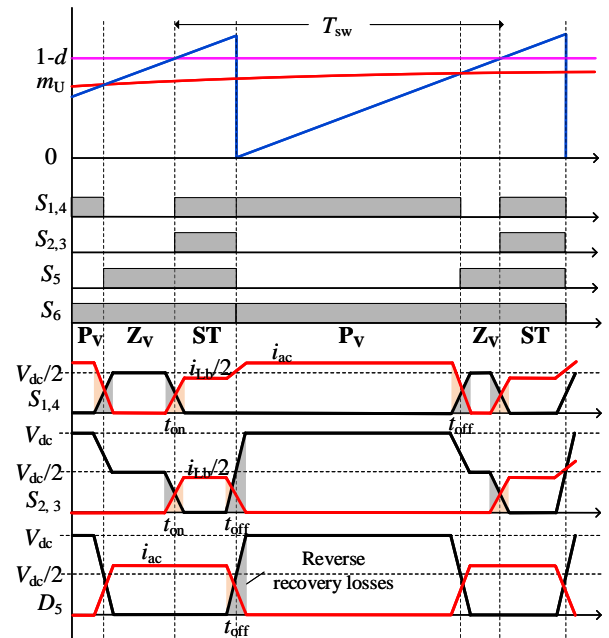


Fig. 8: Distribution diagram of the switching losses in positive cycle, where t_{on} and t_{off} are the turn-ON time and the turn-OFF time of power switches

inverter (see Fig. 6). Fig. 7 shows the equivalent circuit of both converters when S_b of the two-stage inverter is ON or the proposed converter is in the ST mode. Assuming that the grid current i_{ac} is

Table 2 Comparison of the Proposed Converter and Prior-art Converters

Category	Traditional two-stage inverter (Fig. 6)	BDHC in [10]	Transformerless hybrid converter in [15]	Proposed converter
Device-count	7 IGBT, 1 Diode	4 IGBT, 1 Diode	6 IGBT, 1 Diode	6 IGBT, 1 Diode
Device stress	IGBT: V_{dc} , $\max(i_{dc}, i_{ac})$ Diode: V_{dc} , $i_{dc} + i_{ac}$	IGBT: V_{dc} , $\max(i_{dc}, i_{ac})$ Diode: V_{dc} , i_{dc}	IGBT: V_{dc} , $\max(i_{dc}, i_{ac})$ Diode: V_{dc} , i_{dc}	IGBT: V_{dc} , $\max(\frac{i_{dc}}{2}, i_{ac})$ Diode: $V_{dc} - \frac{V_{in}}{2}$, i_{dc}
DC gain	$\frac{1}{1-d}$	$\frac{1}{1-d}$	$\frac{1}{1-d}$	$\frac{1}{1-d}$
AC gain (V_{acpeak}/V_{in})	$\frac{1}{1-d}$	1	1	1
Dead-time effect	Yes	No	No	No
Leakage currents	Low	High	Low	Low
Power density	Low	High	Low	High
Conversion efficiency	Low	Low	Low	High

positive, i_{ac} flows through S_6 and S_5 of the traditional two-stage inverter at this period. The losses comparison results are presented in Table 1, and the corresponding analysis is in the following:

1) As presented in Fig. 7 (a), the boost inductor current i_{Lb} flows through S_b of the traditional two-stage inverter while flows through S_{1-4} in the proposed converter. Thus, the conduction losses induced by i_{Lb} are almost the same with a difference of $V_{ce0}I_{Lb}$.

2) In the **ST** mode, the grid current i_{ac} of the proposed converter has three paths, while i_{ac} of the traditional two-stage inverter only has one path, resulting in lower conduction losses.

3) For the diode D , the diode average current I_{dav} of the proposed converter is equal to I_{dc} (i.e., the average of the DC output current i_{dc}), while $I_{dav} = I_{dc} + 2I_m/\pi$ in the traditional two-stage inverter (i.e., $2I_m/\pi$ is the average of the grid current i_{ac}). That is, the conduction losses of the two-stage inverter are larger than those of the proposed converter, especially when the AC output power is large.

Switching Losses: According to [33], the switching losses of the IGBT contains turn-ON losses, turn-OFF losses and reverse recovery losses, which can be calculated as

$$P_S = P_{swT} + P_{swD} = (E_{onT} + E_{offT} + E_{onD})f_{sw} \frac{V_{ceav}I_{cav}}{V_{CC}I_{CC}} \quad (24)$$

where P_{swT} and P_{swD} are the switching losses of the IGBT and the anti-parallel diode, and E_{onT} , E_{offT} , and E_{onD} are the turn-ON, turn-OFF, and diode reverse-recovery energy, correspondingly, which are provided in the datasheet under certain test conditions (i.e., the test voltage V_{CC} and current I_{CC}). Moreover, V_{ceav} and I_{cav} are the average voltage and current of the IGBT, respectively.

With the above, the switching losses can be calculated, and Fig. 8 illustrates the switching losses of the proposed converter. As shown in Fig. 8, there are turn-ON losses on S_{1-4} when the mode changes from **Zv** to **ST**. Then, from **ST** to **Pv**, there are turn-OFF losses on $S_{2,3}$, and the diode reverse recovery losses are generated on D_5 . Finally, for **Pv** to **Zv**, the turn-OFF losses will be generated on $S_{1,4}$. Compared to the switching losses of the traditional two-stage inverter, the switching losses of the proposed converter are reduced by $\frac{2E_{onT}f_s V_{dc} I_m}{\pi V_{CC} I_{CC}}$, as summarized in Table 1.

4.2 Comparison with Prior-art Converters

the proposed converter can achieve AC and DC outputs simultaneously. A comparison with the prior-art hybrid converters is shown in Table 2. It can be summarized as:

(1) *Low component-count with shoot-through capability:* When compared to the traditional two-stage inverter with the HERIC as the VSI (i.e., an example of the separated converters, as shown in Fig. 6, the proposed converter has fewer power devices with less current stress and voltage stress to achieve multiple outputs, while

Table 3 System Parameters

Parameters	Symbol	Values
DC input voltage	V_{in}	0–200V
DC output voltage	V_{dc}	0–360V
AC grid voltage (RMS)	v_{ac}	0–110V
Grid frequency	f_g	50 Hz
Boost inductors	L_{b1}, L_{b2}	0.4 mH
output capacitor	C_{DC}	2800 μ F
L -type inductors	L_{ac1}, L_{ac2}	0.75 mH
Switching frequency	f_s	20 kHz
PV parasitic capacitor	C_{PVg}	200 nF

maintaining the same DC gain. Additionally, the proposed converter has the shoot-through protection, leading to lower EMI and higher reliability, and the power quality can then be improved to a certain extent (i.e., due to the elimination of the deadtime). Notably, as presented in Table 2, the AC gain of the proposed converter is lower than that of the traditional two-stage inverter.

(2) *Low leakage currents:* Comparing the proposed converter with the BDHC in [10], the leakage currents can be suppressed to a low level (i.e., satisfying the grid standard [13]) with the symmetrical structure. It makes the proposed converter specifically suitable in PV applications.

(3) *High power density:* the proposed converter has a higher power density than the transformerless hybrid converter in [15]. Both hybrid converters employ an L -type filter in the AC side. However, since a dual-buck inverter was adopted as the VSI [16], only one inductor is utilized, while the other is idle. That means the L -type filter of the hybrid converter in [15] should be two times in terms of value and volume as that for the proposed converter, resulting in low power density.

(4) *Reactive power injection and independent control:* With the modulation scheme in Fig. 3(a), the reactive power injection can be flexible injected. Furthermore, the DC gain and AC modulation signal can be controlled independently within the voltage and power limitations according to Eqs. (15) and (17). In all, the proposed converter can achieve flexible reactive power injection.

5 Simulation and Experimental Results

The proposed hybrid transformerless converter is validated through simulations and experimental tests. The power switches S_{1-6} are from Infineon (part no. IKW30N65NL), and the diode D is from ROHM (part no. RFUH20TF6SFHC9). All the system parameters are detailed in Table 3, where the passive components are designed for a rating of 5 kW, and the PV parasitic capacitance C_{PVg} is chosen

based on [34]. As mentioned, the DC input V_{in} adopts a DC power supply to demonstrate the proposed converter.

5.1 Simulations Results

To verify the losses analysis and comparison between the traditional two-stage inverter with the HERIC as the VSI (i.e., as shown in Fig. 6) and the proposed converter, simulations are carried out in Piecewise Linear Electrical Circuit Simulation (PLECS) software. The correspondingly thermal-loss models of the power devices are established based on the device datasheets (i.e., Infineon IGBT-IKW3N65EL5 and ROHM diode-RFUH20TF6SFHC9). The system parameters of the traditional two-stage inverter are the same as that in Table 3. Besides, the input and output voltages are $V_{in} = 140$ V, $V_{dc} = 160$ V and $v_{ac} = 78$ V/ 50 Hz (RMS), and the DC load R_{DC} is 25.6Ω in the simulation tests.

Fig. 9 shows simulation results, where P_S and P_C represent the switching losses and the conduction losses of the power devices. The efficiency of two configurations under $P_{ac} : P_{dc} = 0.4$ is compared in Fig. 9(a), where only the losses of the power devices are considered. In addition, Fig. 9(b) shows the switching losses and conduction losses of the IGBT (with an anti-parallel diode) for the two converters with $P_{dc} = 1.4$ kW and 1 kW, respectively, and the total power being 1.4 kW. Furthermore, when the AC and DC power ratio is varying, the efficiency is also compared, as demonstrated in Fig. 9(c), where the total power is 1.4 kW and the limitation in Eq. (17) is also considered. The results indicate that only the conduction losses of the traditional two-stage inverter are slightly less than that of the proposed converter under $P_{ac} : P_{dc} = 0$. With $P_{ac} : P_{dc}$ increasing, both the switching losses and the conduction losses of the traditional two-stage inverter become larger than those of the proposed converter. Therefore, the proposed converter can achieve a higher efficiency than the traditional two-stage inverter, which validates the discusses in Section IV.A, and it has fewer components with less current stress and voltage stress.

5.2 Experiments Results

Fig. 10 shows the experimental setup of the proposed converter system, where control and modulation algorithms are implemented in a fixed-point digital signal processor (DSP) from TI (TMS320F2812). The DC output is an ET5420 electronic load, and the AC output is connected to the AC grid, referring to Fig. 2(b). The system parameters are the same as in Table 3.

Figs. 11 and 12 show the steady-state performances of the proposed symmetrical transformerless hybrid converter with different DC and AC gains. The DC input voltage V_{in} , the DC output voltage V_{dc} , the grid voltage v_{ac} and the grid current i_{ac} are shown in Figs. 11(a) and 12(a). The input and output voltages of Fig. 11(a) are $V_{in} = 140$ V, $V_{dc} = 160$ V and $v_{ac} = 78$ V/ 50 Hz (RMS), and the DC load R_{DC} is 25.6Ω . While those parameters in Fig. 12(a) are $V_{in} = 180$ V, $V_{dc} = 260$ V, $v_{ac} = 110$ V/ 50 Hz (RMS), and $R_{DC} = 140 \Omega$. Due to the inherent pulsation power of the HERIC, there are certain ripples in the output voltage V_{dc} . Nevertheless, the results in Figs. 11(a) and 12(a) demonstrate the multi-output feature of the proposed converter. Additionally, Figs. 11(b) and 12(b) show the CMV, the inverter output terminal voltages, and the leakage currents. Observations in Figs. 11(b) and 12(b) indicate that the leakage current i_{leak} is well suppressed below the limit (300 mA). Moreover, both experimental results illustrate that v_{dm} of the proposed converter at the AC output has the same performance as the single HERIC with the unipolar PWM (i.e., changing between $+V_{dc}/-V_{dc}$ and 0) at the switching frequency). Therefore, with the proposed modulation method in Fig. 3, the proposed converter can achieve good power quality, low losses, and low leakage currents and multiple outputs.

Moreover, the key current waveforms (i.e., i_{Lb} , i_D and i_{ST}) during switching are shown in Fig. 13. It should be noted that the experimental data of these variables are obtained through the oscilloscope and then replotted in MATLAB due to the lack of current probe. It can be observed in Fig. 13 that the key waveforms agree well the

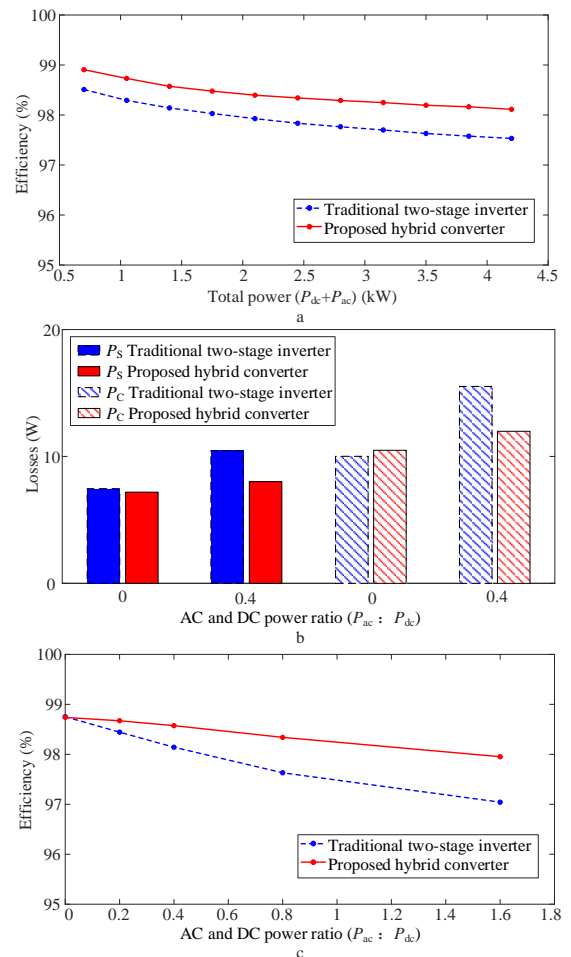


Fig. 9: Power losses and efficiency comparison between the traditional two-stage inverter and the proposed converter
a Efficiency comparison at different power levels (i.e., $P_{ac} : P_{dc} = 0.4$)
b Power losses comparison of conduction losses and switching losses
c Efficiency comparison at different $P_{ac} : P_{dc}$ and $P_T = 1.4$ kW

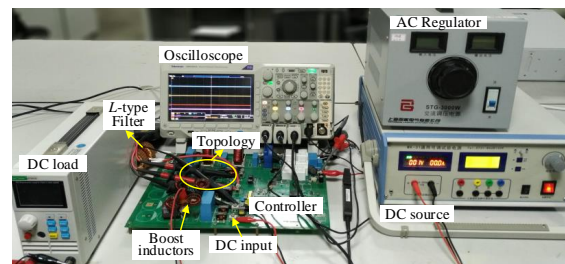


Fig. 10: Prototype of the proposed hybrid transformerless converter system

analysis in Fig. 4(c). Notably, the spikes of the HERIC input current i_{ST} are normal, which are due to the nonidealities of power devices. It thus confirms the effectiveness of the modulation method for the proposed converter.

To further verify the reactive power injection capability, the experimental tests of the proposed converter have been performed under non-unity power factors (i.e., the power factor $\cos\varphi = +0.866$ and -0.866). The experimental results are shown in Fig. 14, in which Fig. 14(a) corresponds to the case of i_{ac} lagging v_{ac} , $\cos\varphi = +0.866$, and Fig. 14(b) presents the case of i_{ac} leading v_{ac} , $\cos\varphi = -0.866$. As can be seen in Fig. 14, the proposed converter can provide and absorb reactive power upon demands.

the proposed converter is then tested under load changes, and the experimental results are presented in Fig. 15. Here, the grid current

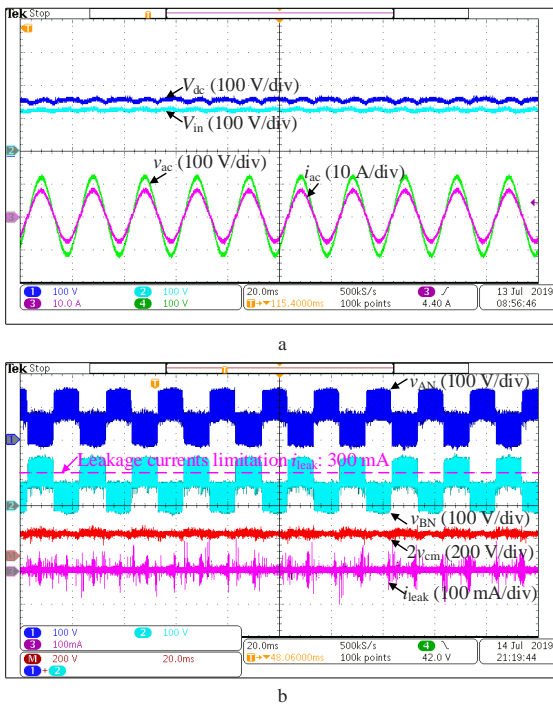


Fig. 11: Experimental results of the proposed hybrid transformerless converter under DC gain being 1.143 and maximum modulation signal being 0.7857 (time: 20 ms/div)
 a Input and output waveforms (i.e., V_{in} , V_{dc} , v_{ac} and i_{ac})
 b the CMV, inverter output terminal voltages v_{AN} and v_{BN} , and the leakage current i_{leak}

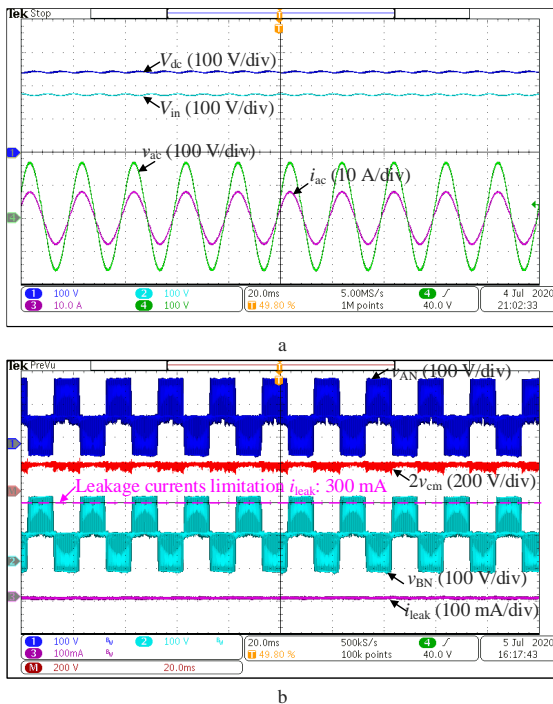


Fig. 12: Experimental results of the proposed hybrid transformerless converter under DC gain being 1.444 and maximum modulation signal being 0.867 (time: 20 ms/div)
 a Input and output waveforms (i.e., V_{in} , V_{dc} , v_{ac} and i_{ac})
 b the CMV, inverter output terminal voltages v_{AN} and v_{BN} , and the leakage current i_{leak}

amplitude (RMS) was changed to 2.5 A and then back to 5 A, as the AC load changes. For the DC load changes, the current was changed to 2.4 A and then restored to 4.8 A. Observations in Fig. 15 indicate that the proposed converter can operate stably under dynamic

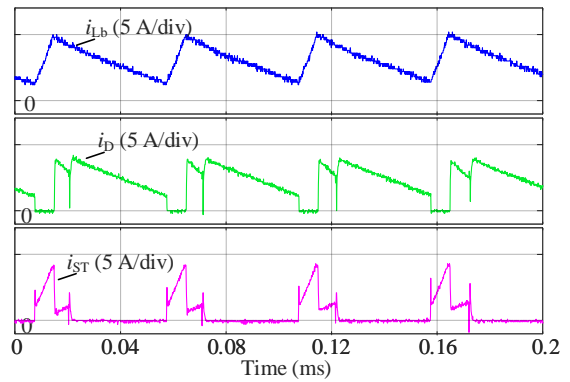


Fig. 13: Experimental results of key current waveforms during switching, i.e., the boost current i_{Lb} , the diode current i_D and the input current of the VSI i_{ST} (time: 40 ms/div)

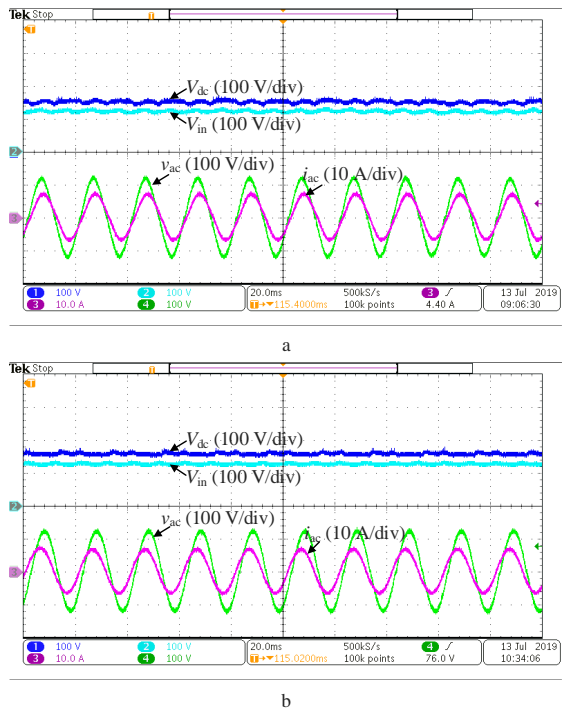


Fig. 14: Experimental results of the proposed converter at non-unity power factors (time: 20 ms/div)
 a i_{ac} lagging v_{ac} , $\cos \phi = +0.866$
 b i_{ac} leading v_{ac} , $\cos \phi = -0.866$

loading changes. That is as long as the proposed converter satisfied the limitation in Eq. (15) and Eq. (17), the current quality of the inverter will not be affected by the loading changes due to the separated control in Fig. 5.

Additionally, Fig. 16 shows the experimental efficiency comparison between the traditional two-stage inverter (i.e., a boost converter and an HERIC) and the proposed converter, where different AC and DC power ratios $P_{ac} : P_{dc}$ are considered with the total power being 1.4 kW. The conversion efficiencies are calculated by measuring the three input and output voltages and currents. In that case, the measured efficiencies in Fig. 16 consider the losses of the power devices as well as the boost and AC filters. The result shown in Fig. 16 agrees well with that in Fig. 9(c), which indicates that the proposed converter can obtain a higher efficiency than the traditional two-stage inverter. It is valuable to mention that when the AC output power accounts for more, the efficiency benefit of the HERIC will become significant.

As a summary, the above simulation and experimental tests have validated the effectiveness of the proposed hybrid transformerless

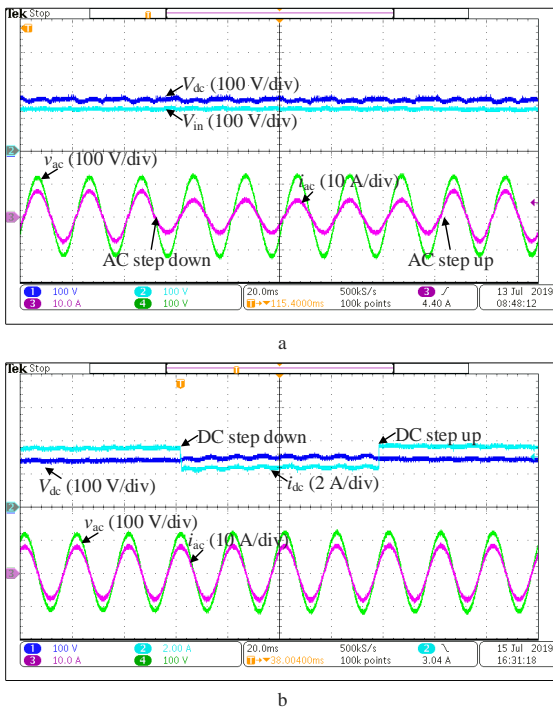


Fig. 15: Experimental results of the proposed converter under load changes (time: 20 ms/div)
a AC load change
b DC load change

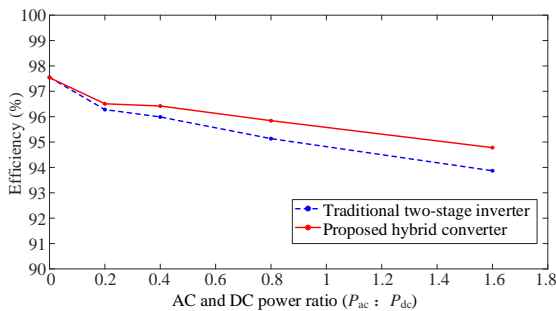


Fig. 16: Measured efficiency of the traditional two-stage inverter and the proposed converter under different $P_{ac} : P_{dc}$ and $P_T = 1.4$ kW

converter in terms of low leakage currents, simultaneous DC and AC outputs, and flexible reactive power capability for grid-friendly hybrid PV systems. In addition, with the corresponding modulation scheme, the proposed converter can maintain good power quality and high efficiency. Therefore, the proposed converter can be a promising and cost-effective solution for future smart PV systems.

6 Conclusion

In this paper, a type of hybrid transformerless converters have been proposed, which can achieve simultaneous DC and AC outputs, low leakage currents, and inherent shoot-through capability. The configuration principle for this type of converter has been presented, i.e., 1) a symmetrical boost inductor should be employed to ensure a constant CMV when operating as a boost converter; 2) a transformerless inverter should be adopted as the switch to maintain a constant CMV when acting as a VSI. This has been demonstrated on a converter with the HERIC as the VSI, and the corresponding modulation method, CMV analysis and losses comparison are detailed to illustrate the performance in reactive power injection,

low leakage currents and high efficiency. Simulations and experimental results have then verified the effectiveness of the proposed converter in terms of multiple outputs, low leakage currents, flexible reactive power capability, high efficiency and high reliability. Notably, other transformerless topologies can be constructed based on the configuration methodology.

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8 References

- [1] Blaabjerg, F., Yang, Y., Yang, D. and Wang, X.: 'Distributed power generation systems and protection', Proc. IEEE, 2017, 7, (105), pp. 1311–1331
- [2] Boroyevich, D., Cvetkovi'c, I. Gong, D., Burgos, R., Wang, F. and Lee, F.: 'Future electronic power distribution systems a contemplative view'. Proc. 12th Int. Conf. OPTIM Elect. Electron. Equip., May 2010, pp. 1369–1380
- [3] Braun, M., Stetz, T., Bründlinger, R., Mayr, C., Ogimoto, K., Hatta, H., Kobayashi, H., Kroposki, B., Mather, B., Coddington, M., Lynn, K., Graditi, G., Woyte, A. and MacGill, I.: 'Is the distribution grid ready to accept large-scale photovoltaic deployment? State of the art, progress, and future prospects: Distribution grid and large-scale PV deployment', Prog. Photovolt: Res. Appl., 2012, 6, 20, pp. 681–697
- [4] Lv, Z., Zhang, Y., Xia, Y. and Wei, W.: 'Adjustable inertia implemented by bidirectional power converter in hybrid AC/DC microgrid', IET Gener. Transm. Distrib., 2020, 17(14), pp. 3594–3603
- [5] Adda, R., Ray, O., Mishra, S. K. and Joshi, A.: 'Synchronous-reference-frame-based control of switched boost inverter for standalone DC nanogrid applications', IEEE Trans. Power Electron., 2013, 3, (28), pp. 1219–1233
- [6] Tseng, K.-C. and Huang, C.-C.: 'High step-up high-efficiency interleaved converter With voltage multiplier module for renewable energy system', IEEE Trans. Ind. Electron., 2014, 3, (61), pp. 1311–1319
- [7] Blaabjerg, F. and Ionel, D. M.: 'Renewable Energy Devices and Systems with Simulations in MATLAB® and ANSYS®' (CRC Press, 2017, 1st edn.)
- [8] Schirone, L., Macellari, M. and Pellitteri, F.: 'Predictive dead time controller for GaN-based boost converters', IET Power Electron., 2017, 4, (10), pp. 421–428
- [9] Tang, T., Yang, Y., Zhou, Su, M., Jiang, T., Blaabjerg, F., Dan, H. and Liang, X.: 'Modulation for the AVC-HERIC inverter to compensate for deadtime and minimum pulsewidth limitation distortions', IEEE Trans. Power Electron., 2020, 3, (35), pp. 2571–2584
- [10] Ray, O. and Mishra, S.: 'Boost-derived hybrid converter with simultaneous DC and AC outputs', IEEE Trans. Ind. Appl., 2014, 2, (50), pp. 1082–1093
- [11] Lee, S. S. and Heng, Y. E.: 'Improved single-phase split-source inverter with hybrid quasi-sinusoidal and constant PWM', IEEE Trans. Ind. Electron., 2017, 3, (64), pp. 2024–2031
- [12] Lee, S. S., Tan, A. S. T., Ishak, D. and Mohd-Mokhtar, R.: 'Single-phase simplified split-source inverter (S3I) for boost DC-AC power conversion', IEEE Trans. on Ind. Applicat., 2019, 10, (66), pp. 7643–7652

- [13] DIN VDE 0126: 'Automatic Disconnection Device Between A Generator and the Public Low-Voltage Grid', German Standard, 2010
- [14] IEEE Standard 1547.2: 'IEEE Standard for Interconnecting and Interoperability of Distributed Resources With Associated Electric Power Systems Interfaces', 2018
- [15] Dey, S., Bussa, V. K. and Singh R. K.: 'Transformerless hybrid converter with AC and DC outputs and reduced leakage current', *IEEE J. Emerg. Sel. Top. Power Electron.*, 2019, 2, (7), pp. 1329–1341
- [16] Yang, F., Ge, H., Yang, J., Dang, R. and Wu H.: 'A family of dual-buck inverters with an extended low-voltage DC-input port for efficiency improvement based on dual-input pulsating voltage-source cells', *IEEE Trans. Power Electron.*, 2018, 4, (33), pp. 3115–3128
- [17] Li, W., Gu, Y., Luo, H., Cui, W., He, X. and Xia, C.: 'Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression', *IEEE Trans. Power Electron.*, 2015, 7, (62), pp. 4537–4551
- [18] Wu, T., Kuo, C., Sun, K. and Hsieh, H.: 'Combined unipolar and bipolar PWM for current distortion improvement during power compensation', *IEEE Trans. Power Electron.*, 2014, 4, (29), pp. 1702–1709
- [19] Victor, S. B. M., Greizer, F. and Hubler, U.: 'Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage', U.S. Patent 7 411 802 B2, 2008
- [20] Xiao, H., Liu, X. and Lan, K.: 'Optimised full-bridge transformerless photovoltaic grid-connected inverter with low conduction loss and low leakage current', *IET Power Electron.*, 2014, 4, (7), pp. 1008–1015
- [21] Yu, W., Lai, J. J., Qian, H. and Hutchens, C.: 'High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non-isolated AC module applications', *IEEE Trans. Power Electron.*, 2011, 4, (26), pp. 1253–1260
- [22] Islam, M. and S. Mekhilef: 'H6-type transformerless single-phase inverter for grid-tied photovoltaic system', *IET Power Electron.*, 2015, 4, (8), pp. 636–644
- [23] Heribert, S., Christoph, S. and Jurgen, K.: 'Inverter for transforming a DC voltage into an AC current or an AC voltage', Europe Patent 1 369 985 (A2), 2003
- [24] Zhou, L., Gao, F. and Xu, T.: 'A family of neutral-point-clamped circuits of single-phase PV inverters: Generalized principle and implementation', *IEEE Trans. Power Electron.*, 2017, 6, (32), pp. 4307–4319
- [25] Freddy, T. K. S., Lee, J.-H., Moon, H.-C., Lee, K.-B. and Rahim, N. A.: 'Modulation technique for single-phase transformerless photovoltaic inverters with reactive power capability', *IEEE Trans. Ind. Electron.*, 2017, 9, (64), pp. 6989–6999
- [26] Tang, Z., Yang, Y., Su, M., Han, H. and Blaabjerg, F.: 'A symmetrical transformerless hybrid converter with leakage current suppression'. Proc. of the IEEE ECCE, Sep. 2019, pp. 6680–6685
- [27] Gub'ia, E., Sanchis, P., Urs'ua, A., L'opez, J. and Marroyo, L.: 'Ground currents in single-phase transformerless photovoltaic systems', *Prog. Photovolt. Res. Appl.*, 2007, 7, (15), pp. 629–650
- [28] Erickson, R. W. and Maksimovic, D.: 'Fundamentals of Power Electronics' (Norwell: MA: Kluwer, 2001, 2nd ed. pp. 22–27)
- [29] Ciobotaru, M., Teodorescu, R. and Blaabjerg, F.: 'Control of single stage single-phase PV inverter'. Proc. of 2005 European Conference on Power Electronics and Applications, Sep. 2005, pp. P.1–P.10
- [30] Li, K., Shen, Y., Yang, Y., Qin, Z. and Blaabjerg, F.: 'A transformerless single-phase symmetrical Z-source HERIC inverter with reduced leakage currents for PV systems'. Proc. of the IEEE APEC, Mar. 2018, pp. 356–361
- [31] Maniktala, S.: 'Switching Power Supplies A–Z' (Amsterdam: The Netherlands: Elsevier, 2012, 2nd ed. pp. 72–74)
- [32] Shadmand, M. B., Li, X., Balog, R. S. and Abu Rub, H.: 'Constrained decoupled power predictive controller for a single-phase grid-tied inverter', *IET Renew. Power. Gener.*, 2017, 5, (11), pp. 659–668
- [33] Graovac, D. D. and P'urschel, M.: 'IGBT power losses calculation using the data-sheet parameters' (Infineon, 2009, pp. 1–17)
- [34] Araneo, R., Lammens, S., Grossi, M. and Bertone, S.: 'EMC issues in high-power grid-connected photovoltaic plants', *IEEE Trans. Electromagn. Compat.*, 2009, 3, (51), pp. 639–648