ADVANCED InP/InGaAs ELECTRONIC/OPTOELECTRONIC INTEGRATED CIRCUITS FOR HIGH SPEED MMIC APPLICATIONS

A thesis submitted to The University of Manchester for the degree of

Doctor of Philosophy

In the Faculty of Science and Engineering

2020

SAAD GAZAI MUTTLAK

School of Electrical and Electronic Engineering

TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

2D	Two Dimensional
3D	Three Dimensional
A/Amp	Ampere (Current Unit)
AC	Alternating Current
ADS	Advanced Design System
AlAs	Aluminium Arsenide
AlGaAs	Aluminium Gallium Arsenide
AlSb	Aluminium Antimonide
APD	Avalanche Photodiode
AR	Anti-Reflection
ASPAT	Asymmetric Spacer Tunnel Layer Diode
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
CE	Common Emitter
CMOS	Complementary Metal-Oxide Semiconductor
CPW	Coplanar Waveguide
C-V	Capacitance-Voltage
CW	Continuous Wave
DBQW	Double-Barrier Quantum Well
DC	Direct Current
DUT	Device under Test
EBL	Electron Beam Lithography
E_C	Conduction Band
EDFA	Erbium-Doped Fibre Amplifier
EM	Electromagnetic
EPON	Ethernet Passive Optical Network
E_V	Valence Band
eV	Electron Volt

FFT	Fast Fourier Transform
FTTH	Fibre-to-the-Home
GaAs	Gallium Arsenide
Ge	Germanium
GHz	Gigahertz
GPON	Gigabit Passive Optical Network
GSG	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HZ	High Impedance
IC	Integrated Circuit
IC-CAP	Integrated Circuit Characterization and Analysis Program
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
InP	Indium Phosphide
IoT	Internet of Things
ISI	Inter-Symbol Interference
ITU	International Telecommunications Union
I-V	Current Voltage
K	Kelvin
LCA	Lightwave Component Analyser
LNA	Low Noise Amplifier
MBE	Molecular Beam Epitaxy
MFB	Multiple Feedback
MIC	Microwave Integrated Circuit
MIM	Metal Insulator Metal
mm	Millimeter
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal Organic Chemical Vapour Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

MOVPE	Molecular Organic Vapour Phase Epitaxy
mS	Milli-Siemens
NDR	Negative Differential Resistance
NiCr	Nickel Chromium
nm	Nanometre
NRZ	Non-Return-Zero
OEIC	Optoelectronic Integrated Circuit
ONU	Optical Network Unit
OOK	On-Off Keying
P2MP	Point-to-Multipoint
PCM	Process Control Monitoring
pF	Pico Farad
PON	Passive Optical Network
PRBS	Pseudo-Random Bit Stream
PVCR	Peak to Valley Current Ratio
QCL	Quantum Cascade Lasers
RC	Resistance and Capacitance
RF	Radio Frequency
RTD	Resonant Tunnelling Diode
RZ	Return-Zero
SDD2P	Symbolically Defined Devices Two Ports
SFB	Single Feedback
SGP	SPICE Gummel-Poon
Si	Silicon
SMF	Single Mode Fibre
SRF	Self-Resonant Frequency
TaN	Tantalum Nitride
TBRTD	Triple Barrier Resonant Tunneling Diode
TCR	Temperature Coefficient of Resistance
TDMA	Time Division Multiplexing

TED	Transferred Electron Device
THz	Terahertz
TIA	Transimpedance Amplifier
TL	Transmission Line
TLM	Transmission Line Model
TWDM	Time and Wavelength Division Multiplexed
UCSD	University of California-San Diego
UTC-PD	Uni-Travelling Carrier Photodiode
V	Volt (Voltage Unit)
VNA	Vector Network Analyser
WGPD	Waveguide Photodiode
WLAN	Wireless Local Area Network

ABSTRACT

The foundation of this research relied on the development and improvement of two key InP-based technologies, namely the Resonant Tunnelling Diode (RTD) and the Heterojunction Bipolar Transistor (HBT). This was firstly consolidated by a detailed experimental investigation of Double Barrier Quantum Well (DBQW) InGaAs/AlAs RTDs designed to improve the diode's DC and RF characteristics through a design of experiments utilizing five different device structures targeting high current densities and large Peak to Valley Current Ratios (PVCR) for use in oscillator and amplifier ICs respectively. The measured results of the RTDs showed a significant increase in the current density with thinner barriers and quantum well widths. An estimated high frequency operation limit of 2.7THz was deduced for a 2×2 μm^2 mesa RTD (sample #327). This device had a high current density J_P of 10.8mA/μm^2 while still maintaining an excellent PVCR ~5, one of the highest ever reported for such a high current density making the diode suitable for low-cost *mm*-wave/THz regime applications. In addition, a much more prominent finding is that of a very high negative differential conductance, G_{RTD} of 95mS/μm^2, the highest ever reported and largely responsible for the 2.7THz cut off frequency. An electromagnetic modelling of a 9μm^2 InGaAs/AlAs RTD (sample #230) integrated with a CPW resonator predicts a 100 GHz fundamental frequency oscillator with an output power of 100µW. Furthermore, a novel K-band reflection based amplifier module was designed exploiting the NDR feature of RTD sample #277 incorporated with a lumped element branch coupler provided a high gain of 32 dB at 25.3 GHz while maintaining a µW level DC power consumption of 256µW. This corresponds to a record figure of merit of 125dB/mW, validating the excellent performance of the amplifier.

An extensive study of an InP/InGaAs PIN-PD and SHBT modules employing large-signal built-in AGILENTHBT model from Keysight-ADS and opto-electrical equivalent circuit models extractions were undertaken. Those devices were fabricated and tested at the University of Manchester facility. Due to the specific design of the InP/InGaAs epilayer structures and considering the trade-off between high performance PIN and HBT to fulfil optimum 10 to 20Gb/s OEICs, a 10×10μm^2 emitter mesa size transistor demonstrated an f_T and f_{max} of 54 and 57GHz respectively. The room temperature measurement for the PIN photodiode I-V characteristics with an optical window size of

20µm showed a low dark current of ~1.5nA under fully-depleted conditions. The measured photo-current was 41.5µA at -11dBm input optical power with a laser wavelength of λ=1.55µm, corresponding to a 0.5 A/W and 0.45 DC responsivity and quantum efficiency respectively without the use of antireflection coatings. The experimental data also revealed that the extracted high-frequency limit of RC time constant and carrier transit time were ~17.7 and 36GHz respectively. This is theoretically adequate for up to 25Gb/s operation and offering an outstanding feasibility for low cost OEICs for forthcoming generations 10Gb/s EPON (Ethernet Passive Optical Network) optical communication systems.

An OEIC with single and multiple feedback loop toplogies was modeled. The single feedback transimpedance amplifier, SFB-TIA exhibited a 32dBΩ transimpedance gain with a bandwidth of 14GHz and a series peaking inductor technique was used to further extend the -3dB bandwidth, contributing to widening the bandwidth to 18GHz. Since the conventional SFB-TIA has low optical overload response, a multiple feedback transimpedance amplifier, MFB-TIA circuit was therefore used which provided a gain of 45dBΩ with an electrical bandwidth exceeding 18GHz. This was achieved without the need for integrating a passive peaking element alongside producing deviation in the group delay of 11.7psec up to 20GHz. On-Off keying (OOK) NRZ 2^{15}-1 pseudo-random bit stream patterns were applied to the SFB and MFB photoreceivers and it was found that the eye diagrams were clearly open with no observation of inter-symbol interference for 10 and 20 Gb/s operation responses.

DECLARATION

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

COPYRIGHT STATEMENT

ACKNOWLEDGEMENT

I would like to express my great appreciation to my supervisor, Professor Mohamed Missous, who offered me this valuable opportunity to do research at the University of Manchester and for his highly professional character in the process of consultation and guidance that continuously improved my knowledge during the PhD study.

A special thanks to Higher Committee for Educational Development in Iraq (HCED) for their financial support and grateful help during my PhD research. Also, warm thankful to fellow colleagues for their cooperation towards understanding the ideas in this study.

In the same time, I would like to show my gratefulness to my parents and my wife Sahar who have encouraged me along my life; I dedicated a special and heartiest tribute to them for their help and support…

DEDICATION

This thesis is dedicated to my father who passed away on the day I started my PhD research, I wish I could tell him that I miss him so much.

Saad

PUBLICATIONS

JOUNAL PUBLICATIONS

1. **Saad G. Muttlak**, O. S. Abdulwahid, J. Sexton, M.J. Kelly and M. Missous, "*InGaAs/AlAs Resonant Tunneling Diodes for THz Applications: An Experimental Investigation*", IEEE Journal of the Electron Devices Society, DOI: 10.1109/JEDS.2018.2797951.
2. **Saad. G. Muttlak**, Ioannis Kostakis, Omar S. Abdulwahid, J. Sexton, and M. Missous, "*Low-Cost InP-InGaAs PIN-HBT Based OEIC for up to 20Gb/s Optical Communication Systems",* IET Optoelectronics, DOI: 10.1049/iet-opt.2018.5032.
3. K. N. Zainul Ariffin, Y. Wang, M. R. R. Abdullah, **S. G. Muttlak**, Omar S. Abdulwahid, J. Sexton, Ka Wa Ian, Michael J. Kelly and M. Missous, "*Investigations of Asymmetric Spacer Tunnel Layer (ASPAT) Diode for High-Frequency Application"* IEEE Transaction on Electron Devices, DOI:10.1109/TED.2017.2777803.
4. O. S. Abdulwahid, I. Kostakis, **S. G. Muttlak**, J. Sexton, K.W. Ian and M. Missous, "*Physical Modelling of InGaAs-InAlAs APD and PIN Photodetectors for >25Gb/s Data Rate Applications",* IET Optoelectronics, DOI: 10.1049/iet-opt.2018.5030.

CONFERENCE PUBLICATIONS

1. **Saad G. Muttlak**, Omar Abdulwahid, J. Sexton and M. Missous, "*InGaAs/AlAs Resonant Tunneling Diodes with Very High Negative Differential Conductance for Efficient and Cost-Effective mm-wave/THz Sources*", UCMMT 2019, IEEE proceedings, August 2019, DOI: 10.1109/UCMMT47867.2019.9008338.
2. Omar Abdulwahid, **Saad G. Muttlak**, J. Sexton, M. Missous and M. J. Kelly, "*24GHz Zero-Bias Asymmetrical Spacer Layer Tunnel Diode Detectors*", UCMMT 2019, IEEE proceedings, August 2019, DOI: 10.1109/UCMMT47867.2019.9008351.

3. Abdelmajid Salhi, James Sexton, **Saad G. Muttlak**, Omar Abdulwahid and M. Missous, "*InGaAs/AlAs Metamorphic Asymmetric Spacer Tunnel (mASPAT) Diodes on GaAs Substrate for Microwave/millimetre-wave Applications*", UCMMT 2019, IEEE proceedings, August 2019, DOI: 10.1109/UCMMT47867.2019.9008328.

4. **Saad G. Muttlak**, J. Sexton and M. Missous, "*Modelling of millimeter wave resonant tunnelling diode-based oscillators*", UCMMT 2017, IEEE proceedings, September 2017, DOI: 10.1109/UCMMT.2017.8068350.

5. **Saad G. Muttlak**, O. S. Abdulwahid, J. Sexton and M. Missous, "*Modeling of high gain and μW level power consumption resonant tunneling diode-based amplifiers*", UCMMT 2017, IEEE proceedings, September 2017, DOI: 10.1109/UCMMT.2017.8068351.

6. O. S. Abdulwahid, **Saad G. Muttlak**, J. Sexton, M. Missous, K. W. Ian, M. J. Kelly, "*2nd Subharmonic mixer based asymmetric spacer tunnel diode (ASPAT)*", UCMMT 2017, IEEE proceedings, September 2017, DOI: 10.1109/UCMMT.2017.8068352.

7. K. N. Zainul Ariffin, M. R. R. AbduUah, Y. K. Wang, **Saad G. Muttlak**, O. S. Abdulwahid, J. Sexton; M. Missous and M. J. Kelly, "*Asymmetric spacer layer tunnel diode (ASPAT), quantum structure design linked to current-voltage characteristics: A physical simulation study*", UCMMT 2017, IEEE proceedings, DOI: 10.1109/UCMMT.2017.8068358.

8. Doychinov, D.P. Steenson, **Saad G. Muttlak**, J. Sexton and M. Missous, "*Investigation of mm-wave RTD Based Amplifiers*", IRMMW 2016, IEEE proceedings, DOI: 10.1109/IRMMW-THz.2016.7758969.

9. K. N. Zainul Ariffin, **Saad G. Muttlak**, M. Abdullah, M. R. R. Abdullah, Y. Wang, and M. Missous, "*Asymmetric Spacer Layer Tunnel $In_{0.18}Ga_{0.82}As/AlAs$ (ASPAT) Diode using Double Quantum Wells for Dual Functions: Detection and Oscillation"*, UCMMT 2015, IEEE proceedings, DOI: 10.1109/UCMMT.2015.7460599.

POSTERS AND PRESENTATIONS

1. **Saad G. Muttlak**, J. Sexton and Mohamed Missous**, "***A low cost InGaAs-InP HBT-PIN Based Optoelectronic Integrated Circuit for up to 20Gb/s Optical Communication Systems"*, UK Semiconductor Conference 2018, Sheffield, Oral Presentation.

2. **Saad G. Muttlak**, O. S. Abdulwahid, J. Sexton, Michael J. Kelly and Mohamed Missous**, "***High Current Density Resonant Tunneling Diodes for mm-wave/THz Applications"*, THz Electronics Workshop 2018, Glasgow, Poster Presentation.

3. **Saad G. Muttlak**, O. S. Abdulwahid, J. Sexton and Mohamed Missous**, "***Modeling of a K Band Submilliwatt Power Consumption Resonant Tunneling Diode based Amplifiers"*, UK Semiconductor Conference 2017. Sheffield, Oral Presentation.

4. **Saad G. Muttlak**, J. Sexton and Mohamed Missous**, "***Millimeter Wave Integrated Resonant Tunnelling Diode oscillators"*, UK Semiconductor Conference 2016, Sheffield, Oral Presentation.

5. **Saad G. Muttlak**, J. Sexton and Mohamed Missous, **"***Room Temperature operation, Millimeter Wave Integrated Resonant Tunnelling Diode oscillators*", IOP Student Competition. UK Semiconductor Conference 2016, Sheffield, Oral Presentation.

6. **S. G. Muttlak**, M. A. Md Zawawi and M. Missous, Mohamed Missous, "*Experimental and Physical Modelling of Resonant Tunneling diode with Offset Slot Antenna for Sub-Millimeter Wave Applications*", SIOE Conference 2016. Cardiff, Poster Presentation.

7. **S. G. Muttlak**, Omar S. Abdulwahid, K. N. Zainul Ariffin, J. Sexton and M. Missous, "*A High Gain, μW Power Consumption Quantum Tunneling Diode Amplifier for Next Generation THz electronics*", EEE Poster Conference 2016, Manchester, Poster Presentation.

CHAPTER 1: INTRODUCTION

1.1 Overview of High Frequency Electronic Devices

Over the last forty years, increasing demand for the design and fabrication of ultra-low power, high speed electronic circuits including MMICs (Monolithic Microwave Integrated Circuits) has made semiconductor technology the natural choice for a range of applications. The advances and development in Molecular Beam Epitaxy (MBE) technique which has allowed researchers to achieve new concepts and developments in electronic devices, such as heterojunction bipolar transistors (HBTs), high electron mobility transistors (HEMTs) and resonant tunneling diodes (RTDs).

So far, integrated electronic systems, in particular smart phones and tablets are becoming more attractive for consumer and demands for these portable systems is increasing exponentially as a result of competition in the electronics market. These systems, however, still have some drawbacks, for example power consumption issues due to operation at high frequencies. This leads to increase in the temperature of the system and thus efforts have been devoted to develop new electronic device structures that can overcome these challenges.

One of the possible solutions to address the aforementioned issues is to reduce the supply voltage and the power being dissipated by the circuits. Tunneling-based devices have a great deal to offer as potentially the best candidate in realizing compact, room temperature operation heterostructure devices. These diodes have the ability to effectively support very high switching speed, well into the THz regime. The attractiveness of RTDs is indeed following the pioneering work reported by Esaki and Tsu in the 70's[1]. Millimeter wave and THz frequencies operating devices are currently becoming promising and feasible for a wide range of applications including wireless Gb/s data transmissions, high resolution imaging and non-destructive testing to name a few[2].

Conventional transistor technology is not capable of efficiently accommodating applications beyond 300GHz operation frequency. Nevertheless, HEMTs and HBTs devices have been recently reported with a current gain cut off frequency (f_T) approaching 1 THz[3]. This is limited by the carrier drift velocity and the capacitance of the device, which is inversely proportional to the gate length as well as base and collector

contacts for HEMTs and HBTs respectively. Therefore to reach near THz frequency operation, the gate length of the HEMTs must be extremely small (i.e. <20 nm) and so a 610GHz f_T was demonstrated for HEMT [4] with a gate length of 15nm. Similarly, for HBTs an f_T of 670 GHz was achieved with a very thin base and collector layers of 20 and 60nm respectively[5]. Due to these nanoscale dimensions required for transistor technologies, stringent lithography is necessary, which uses very costly phase shift masks and complex process flows.

From a practical point of view, the operating frequency of circuits utilizing heterojunction or HEMT transistors is typically implemented at a third or less of their cut off frequencies, therefore the most useful fastest transistor circuits can only be realised up to 250 or 300 GHz [6]. By contrast, as the RTD is based on quantum mechanical phenomena, its transit time is in the range of several tens of femtoseconds, providing among the fastest switching speed well into the sub-millimeter and millimeter wave regions using relatively large feature sizes. For example, exploiting a 2μm^2 mesa area RTD device, ~1THz operating frequency can be easily attainable [7] and this is carried out with less expensive masks than other technologies.

Due to the promising characteristics of RTDs, many heterostructure devices have been studied in an attempt to improve their performances in circuit implementations. Recently, a high RTD oscillation frequency of 1.86 THz[8] exploiting Metal Organic Chemical Vapour Deposition (MOCVD) growth technique, was reported by Asada *et.al* with an indium rich quantum well. This was followed by 1.98THz, which is the highest reported to date by the same group [9], though at the expense of a very small output power (nW scale). However, there is a drawback with the monolithic integration of RTDs in that it is difficult to integrate useful numbers and density of RTD devices with transistors (HEMTs or HBTs) into integrated circuits [6].Other multifaceted issues are changes (or non-uniformities) in the RTDs I-V characteristics across a wafer for linear and nonlinear parameter extraction in wafer mapping. This includes variations in the diode's characteristics from wafer to wafer and the fabrication-dependent parasitic impedances which are challenging issue[10]. In fact, these problems can be effectively addressed when particular attention is given to the fabrication process and to the high frequency test equipment during measurements.

The dramatic increase in data traffic due to the rapidly growing demands for ultra-high data rates for both telecom and datacom is driving sustained developments in cost effective, mass produced, optoelectronic integrated photoreceiver (OEIC) operating at 10Gb/s and beyond[11-13]. HEMTs and HBTs technologies with a cutoff frequency reaching 100GHz and beyond are highly useful for such fields, so they have been extensively investigated by integrating PIN/avalanche photodiodes with front-end transimpedance amplifiers, TIAs[12, 14-16]. Full-scale characterizations of the receivers using CAD (Computer-Aided-Design) tools prior to the fabricated circuits are invaluable in the prediction of prospective performances and to aid in further optimizations. This project; therefore, includes the design, characterizations and modelling of high speed InP/InGaAs PIN-SHBT based monolithically integrated photoreceivers for >10Gbs data rate operation. As the PIN depletion region is made of an intrinsic InGaAs layer, the circuit operates at the standard optical wavelength of 1.55μm.

1.2 Solid State Terahertz Sources and Applications

The terahertz band is defined as the region of the electromagnetic (EM) spectrum located between the microwave and infrared light. Since it is challenging to have efficient emitters operating in these frequencies, such a band is known as the terahertz gap[17]. In general, the EM spectrum is traditionally divided into different frequency bands. One of the widespread frequency designations as reported by IEEE is summarized in Table (1.1) [18].

TABLE 1.1: A SUMMARY OF FREQUENCY BANDS CATEGORIZED BY IEEE ORGANIZATION IN 2009[3].

IEEE STANDARD FREQUENCY BANDS	Ku	K	Ka	V	W	*mm*-wave
RANGE (GHZ)	12-18	18-27	27-40	40-75	75-110	110-300

The sub-millimeter or Terahertz band is defined by ITU (International Telecommunications Union) as the band of frequencies from 300GHz to 3THz[19]. A great deal of effort has been dedicated to developing efficient emitters operating in the THz regime (i.e. providing high RF power). These frequencies are currently covered by optical and solid state electronic devices as shown in figure (1.1)[20]. It can be observed that the available output power generated by solid state electronics sharply decreases

with frequency, particularly above 100GHz. The RF power provided by vacuum-based devices is as high as 1 Watt, however these are bulky, costly, not efficient and are short-lived[21]. Alternatively, quantum cascade lasers (QCL) can operate at very high frequencies as emitters. This device is a composite of multiple quantum well heterostructures. To date, the lowest operating frequency reported is 2.1THz with an output power of 1.2mW in continuous wave (CW) mode at cryogenic temperature. Unfortunately, the performance of such semiconductor laser degrades with temperature (i.e. at 40K or even lower in CW mode)[22]. This technology is thus constrained by the requirement of cryogenic cooling, imposing prohibitive costs and bulky systems.

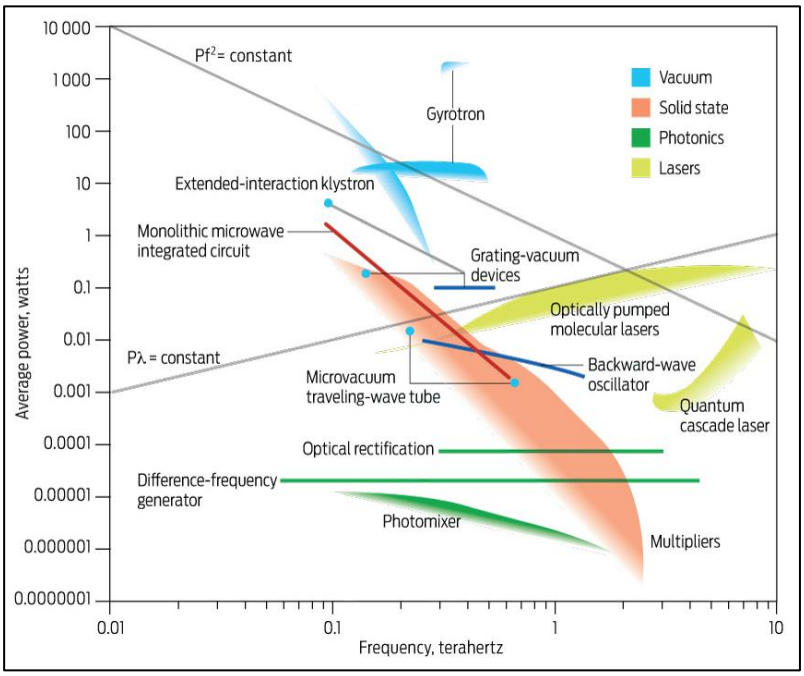


Figure 1.1: Terahertz output power versus frequency generated by different technologies[20].

Unlike QCLs, RTDs are capable of operating at room-temperature and consequently, they are promising and attractive for realizing compact, coherent and low-cost terahertz sources. This section is solely concerned with solid state THz sources and especially those that have a negative resistance region in their IV characteristics, for instance impact ionization avalanche transit time (IMPATT) diodes, Gunn diodes and RTDs.

The Gunn diode consists of n-doped semiconductor materials (i.e. GaAs, InP). In the GaAs or InP , the carrier drift velocity reaches its maximum as an applied voltage bias is increased and then it begins to actually decrease as the electric field is further increased, pushing up electrons which have enough energy to a different conduction band, where

the electron drift velocity is lower and eventually a lower saturation velocity. This is because of dissimilar electron effective mass and mobility along different conduction band valley (Γ valley and L valley) contributing to an overall reduction in current at higher applied voltages until all electrons are in the "slow" band. This is the principle behind the I-V characteristic of Gunn diodes exhibiting a negative differential resistance (NDR). Due to the transfer of electrons to a different conduction band, the latter devices are also known as transferred electron devices (TEDs)[6]. An oscillation frequency of 162 GHz with 25mW for InP Gunn diode oscillator was reported in 2000[23].

The IMPATT diode is a two-terminal p-n junction diode, in which when a high field is applied in reverse bias on the diode and it reaches a certain threshold voltage, avalanche breakdown occurs. Depending on impact ionization and transit time properties, a dynamic negative resistance is produced. It is worthwhile mentioning that the IMPATT negative resistance is different from that of an RTD whose IV characteristic has an NDR. This means that the IMPATT negative resistance comes from the phase difference between ac current and voltage in the time domain[6]. One of the main advantageous of the IMPATT diode is its high power capability at microwave frequencies, an output power of 25mW at 217 GHz for silicon-based IMPATT diode was previously demonstrated[24]. TeraSense Ltd. has introduced a THz source based IMPATT diode incorporating a conical horn antenna operating at 100GHz with an output power of 330mW and then extended to 300GHz using a nonlinear diode frequency multiplier[25]. The downside is that IMPATT diodes, suffer from high phase noise and particular attention is required to avoid detuning and burnout of the device. Nevertheless the oscillation frequency of IMPATT diode can reach as high as 300 GHz[26]. The main criticism of both Gunn and IMPATT devices based oscillators is practically attributed to their requirements for a rectangular waveguide (WR6-WR10) cavity technique, which is not suitable with MMICs and their DC-RF conversion efficiency is often around 3%[23, 24].

On the other hand, the quantum mechanical based RTDs are compact devices with very small active sizes (i.e. $< 4\ \mu m^2$), which can be easily integrated into MMICs for realizing small THz transceiver chips. The usefulness of *mm*-wave/THz waves has been intensively demonstrated for use in a number of applications and the interest is currently growing very rapidly. Amongst the key applications:

1.2.1 Security

mm-wave/THz frequencies can be utilized in the field of security imaging, considered potentially useful for airport safety[27]. It was previously reported that the wave radiation of frequencies beyond 300GHz can pass through clothes and is then absorbed in the human bodies. For plastic, paper, liquid, metal and non-metal items detection, this technology is highly beneficial[28]. The reason is mainly due to the non-ionized radiation nature of the terahertz electromagnetic waves, deemed safe when someone is exposed to them in comparison with very short wavelength radiations such as X-rays [29].

1.2.2 Biomedical

In the biomedical area, terahertz frequencies are particularly attractive for cancer detection purposes. Since EM waves have less photon energy, thus biological soft tissues are not damaged by millimeter or sub-*mm* wave frequencies. To this end, identification and differentiation of tumour tissues could help in the early detection of such stubborn diseases[30, 31].

1.2.3 Monitoring and Astronomy Research

Climate changes can be also monitored using THz waves, for example many gas absorption lines are located in the range of frequencies between 30GHz to 3THz. Thus, the importance of accurately identifying and qualifying these gases comes from the idea of ice crystal and water vapour detection[32]. A similarly important field for THz is astronomy in that receiving ultra-high frequency signals can provide insight into stars and universe formation[33]. Furthermore, *mm*-waves are used in the area of identifying the composition of celestial bodies' atmosphere, which can help to understand the main constituents of such objects[34].

1.2.4 Communications

One of the most important applications regarding this work is the use of EM waves in high Gb/s communications and the possibility of exploiting such bands is in the spectrum above 30GHz (in the range 75 to 110GHz, W-band). In fact, high definition-TV (HDTV) and gigabit WLAN (Wireless Local Area Network) are the main applications where terahertz frequencies can be utilized[35]. These frequencies are being explored for 5th

generation mobile systems[36]. Furthermore, a 30Gb/s modulated terahertz source using resonant tunneling diode was recently reported by Asada *et al*[37].

1.3 Emergence and Development of RTD Transceivers

In 1991, an oscillation frequency of up to 712GHz with an output power of 0.3μW was reported using an InAs/AlSb RTD integrated with a rectangular waveguide resonator. Soon after, RTD oscillators were demonstrated using quasi-optical structure (i.e. single RTD mounted in a rectangular waveguide) at fundamental frequencies of 103GHz and 210GHz with output power of 50 and 20μW respectively[38, 39]. In 1996, A. C. Molnar *et al* reported an RTD oscillator with 16 RTDs integrated with slot antenna at 310 GHz with a 28μW output power[40]. Later in 2005, Orihashi *et al* from Tokyo Institute of Technology led by Professor Asada used a similar antenna radiator and accomplished a one THz harmonic oscillation using InGaAs/AlAs resonant tunneling diode[41]. Such a massive stride has been obtained as a consequence of using an indium rich quantum well, providing very high current densities exceeding 20mA/μm^2. A typical RTD THz emitter with a slot antenna is shown in figure (1.2). Further discussion regarding the RTD characteristics and performance are presented in chapter two.

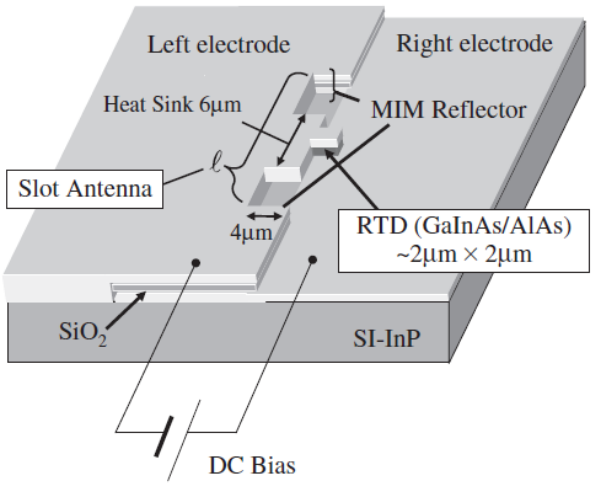


Figure 1.2: Typical structure of an RTD THz oscillator integrated with a slot antenna realized using two MIM reflectors. Adapted from[42].

Due to the very high impedance of slot antennas, which produces a mismatching between the diode and antenna and thereby degrade the RF output power, the offset slot antenna was thus proposed by the Asada's group in 2007[42]. Since the peak of the radiation

conductance (i.e. the real part of the admittance) of the offset slot antenna decreases with offset and is shifted to a low frequency, a low antenna's impedance can be obtained at high frequency[42]. This provides a good match with the integrated diode. Accordingly, an impressive output power of 610 µW at 620GHz oscillation frequency for RTD emitters with two integrated elements was demonstrated in 2012 taking advantage of offset slot antenna technique[43]. However, integrating several devices increases the capacitance of the circuit, which in turn reduces the operation frequency.

With a single RTD emitter, a very high oscillation frequency of 1.86THz was recently achieved but with extremely low output power of 0.03µW[8]. The highest oscillation frequency reported to date is 1.98THz and was obtained by reducing the conduction loss of the highly doped InGaAs cap layer underneath the air-bridge[9]. Power combining techniques with array configuration using two RTDs in parallel has also been realized exploiting coplanar waveguide (CPW) as a resonator[44]. Generally speaking, the combined output power is element number dependent and it is theoretically proportional to the square of the oscillator number[45, 46]. However, for an efficient multi-element topology, the small difference between the individual device frequencies is a challenge for combining. This is because it requires a stringent uniformity for the mesa area of the individual diodes, ensuring near identical device performance which would then provide a reasonable chance of injection locking. Furthermore, the coherency of the combined power is difficult to obtain and the predicted power is often degraded due to the leakage effect of the coupling stub[47]. Another potential structure for power combining technique stated in [48] is the mutual injection locking between subterahertz oscillating RTDs, in which there is no need for a coupling stub; nevertheless, it is highly sensitive to the position of the RTD oscillators[47].

As an alternative array configuration, a dipole antenna was reported by the Tokyo Institute of Tech. group for several peak frequencies, and which was highly efficient for use in imaging applications. This technique achieved an output power of about 135µm at 0.92THz with ten-integrated oscillators[49]. For a low frequency on-off keying (OOK) transceiver, a resonant tunneling diode integrated with an InP-based HBTs showed µW level DC power consumption at an oscillation frequency of 5.7GHz[50]. The increase in RTD oscillator's performance over the last two decades is plotted versus oscillation frequency as shown in figure (1.3)[8, 38-44, 47, 51-59].

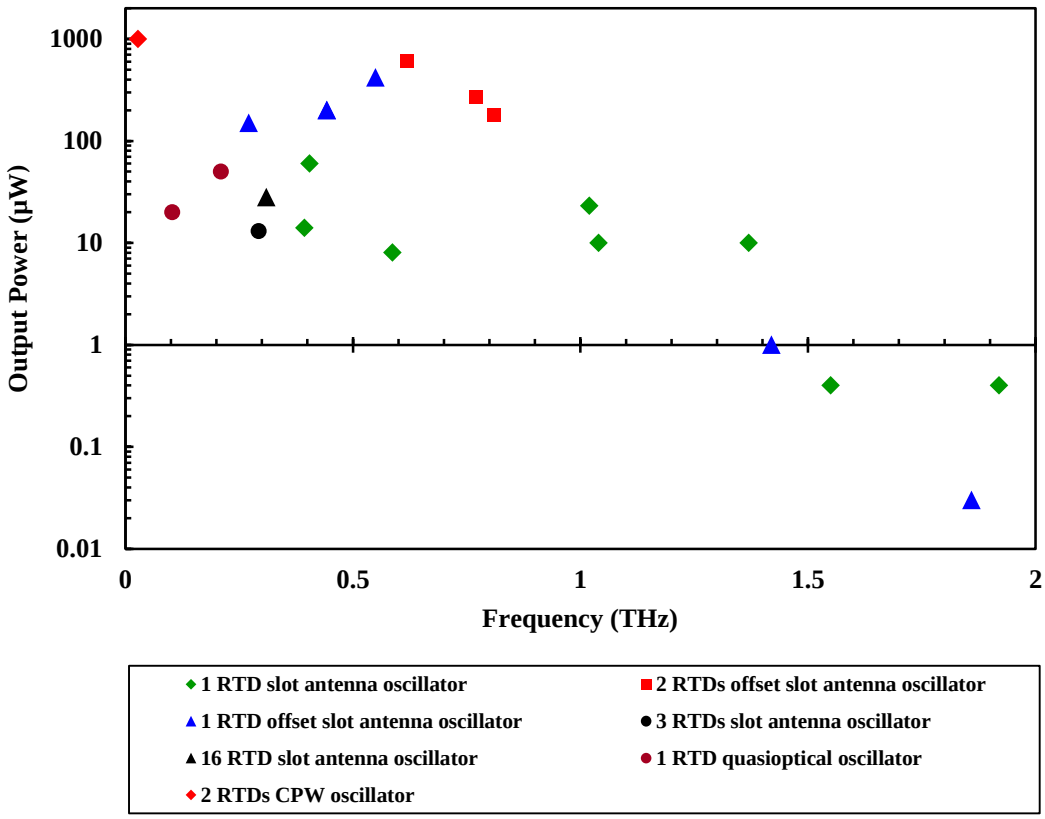


Figure 1.3: Development in the performance of RTD emitters in terms of RF power versus frequency.

As shown in figure (1.3), the output power exponentially deceases with the oscillation frequency. This result can be attributed to the decrease in the negative differential resistance of the RTDs with frequency due to transit delay time in the double barrier quantum well and the collector depletion region. Despite the increase in the output power of RTD emitters realized by offsetting the diode from the centre of the antenna, they still require a Si lens to couple the radiation out of the substrate. Thus, a different technique based on a square patch antenna was proposed through fabricating the antenna on a 7 µm thick BCB layer, which is stacked on the RTD with a slot resonator to eliminate the bulky Si lens. However, the achieved output power was low (i.e. 40µW at a fundamental frequency of 500GHz)[49]. Furthermore, horizontal radiation using horn antenna has been also employed for the same reason but the extremely low output power of 0.6µW at a 455GHz oscillation frequency makes this technique not useful to date[50].

Unlike integration with slot antenna, a triple-push topology using a CPW resonator has achieved a 3rd harmonic oscillation of 1.27THz[60] and then extended up to 1.52THz[61]. This technology; however, still suffers from µW output power levels due

to the requirement of strictly identical RTD sub-oscillators with a very small performance deviation among the devices[61].

Additionally, an RTD based differential topology oscillator for power coupling enhancement was proposed and showed a radiated output power of 47µW at 675GHz[62]. This circuit configuration can be basically fabricated with a differential-fed dipole antenna including a pair of RTDs and transmission line inductors. Due to the differential mode operation, the oscillator circuit becomes insensitive to the common mode noise caused by the bias circuitry and semi-insulating substrate[62]. For high data wireless communications, RTDs based transmitters and detectors were demonstrated in 2011 for operation in the sub-terahertz region. A data rate of 1.5Gb/s at 300GHz was obtained with error free transmission (10^{-12})[63]. Subsequently, the same author reported an error free wireless system at 300GHz with a bit rate of 2Gb/s using RTDs[64]. During the same period, Asada demonstrated a wireless data transmission with direct amplitude shift key (ASK) employing RTDs as THz sources at 542GHz with a measured bit error rates (BER) of $2x10^{-8}$ and $3x10^{-5}$ at 2 and 3Gb/s data rates respectively[58], followed by as high as 10Gb/s data rate with 20GHz bandwidth[65].

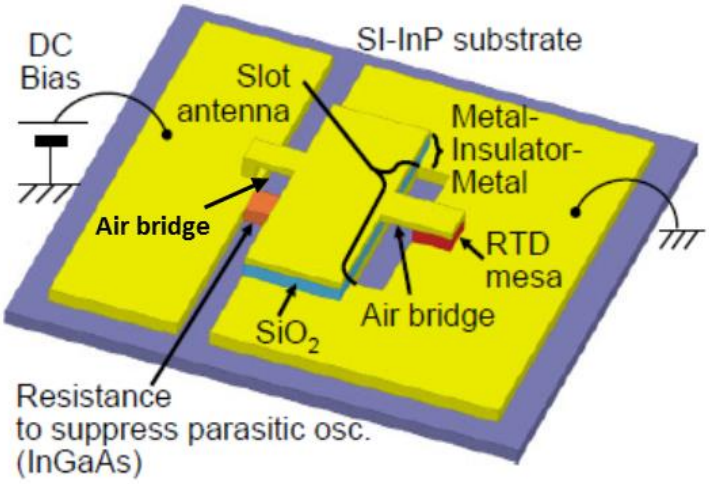


Figure 1.4: Typical structure of an RTD oscillator with a modified MIM capacitor for high data rate wireless communications. Adapted from[66].

For wide band direct modulation RTD transmitters, a few hundred femtofarad of metal-insulator-metal (MIM) capacitor is necessary as this capacitor normally connected with bonding wires and other parasitic components surrounding the diode and all of these act

as a low pass filter. From which, the cut-off frequency of the direct modulation is constrained to ~15GHz (theoretically adequate for up to 20 Gb/s data rate operation). Therefore, a modified structure of an RTD transmitter with only one MIM capacitor has been proposed as depicted in figure (1.4)[66]. The trend in data rates is increasingly growing as shown in figure (1.5)[37, 58, 63-65, 67]. This has led to demonstrating a high bit rate of 30Gb/s using a modulated terahertz RTD source operating at a centre frequency of 500GHz[30], followed by the highest data rate of 34Gb/s reported to date[60].

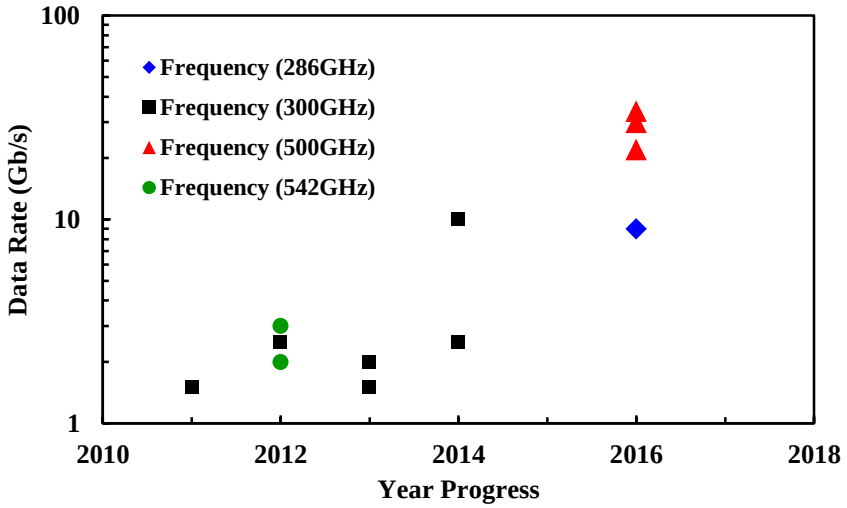


Figure 1.5: Trend in data rate of mm-wave/THz regime wireless communication using resonant tunnelling diodes as a transmitter.

Figure (1.5) shows an exponential increase in the wireless data rate trend using resonant tunneling diodes transmitters, reflecting the importance of improving the characteristics and performance of the RTDs for mm-wave/THz applications. From a high frequency detector viewpoint, RTDs have been also used in direct and heterodyne receivers as the double barrier tunnelling devices have a nonlinear region near their peak voltage[68, 69]. Conversely, the nonlinearity of the triple barrier resonant tunneling diodes (TBRTDs) does pinpoint to a zero bias voltage detector, due to the existence of three barriers and double quantum wells. A voltage sensitivity of a TBRTD based detector of ~3000 V/W at 30GHz was recently achieved[70]. As a different approach, a novel Asymmetric Spacer Layer Tunnel (ASPAT) diode structure formed with an AlAs barrier sandwiched between double quantum wells of $In_{0.18}Ga_{0.82}As$, offering dual functions including detection and oscillation capability was recently reported. This was obtained by the

device exhibiting a negative deferential resistance region and zero bias turn-on features in its I-V characteristic[71]. With this in mind, a wide range of applications makes such devices attractive for research and applications particularly at terahertz gap.

1.4 Resonant Tunneling Diodes Based THz Amplification

Considering the unique negative differential resistance feature of the RTD, the transmission line losses can be compensated and exploited to provide gain. There are basically two ways to realize an RTD amplifier; the active transmission line and RF signal reflection amplifiers. The first attempt of using an interband tunnel devices integrated with a FET transistor for low frequency amplification was reported in 2003[72]. A double barrier RTD based amplifier circuit implementation operating at 5GHz was recently demonstrated[73-75]. Later on, Missous and his group presented a modeling and theoretically analyse of a novel K-band reflection based amplifier utilizing InGaAs/AlAs RTDs and achieved a high gain of 32dB while maintaining a very low DC power consumption of 100µW[76].

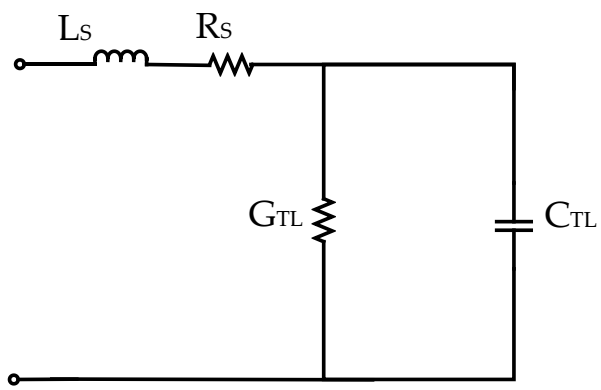


Figure 1.6: Lumped element representation of a single section of a transmission line.

To fully understand how such an amplifier works, further analysis regarding the operating principle of the tunneling devices amplifier including transmission line equivalent circuit and related equations were largely discussed in this section. Since the transmission lines (TLs) are lossy, RF signals that propagate through them undergo a phase shift. It means that the equivalent circuit of the TL has reactive and lossy elements as well as conductance component representing the leakage between signal and ground as depicted in figure (1.6)[77]. It is noteworthy to mention that all the lumped elements of the equivalent circuit are considered per unit length of the transmission line.

Depending on the standard analysis for lossy transmission line, the voltage signal along it is given by[77]:

$$V = Ae^{\gamma x} + Be^{-\gamma x} \tag{1.1}$$

Where:

$$\gamma = \alpha + j\beta = \sqrt{(R + jwL)(G + jwC)} \tag{1.2}$$

α and β are the attenuation and phase constants of the transmission line respectively. The characteristic impedance of the TL, Z_o can be expressed as:

$$Z_0 = \sqrt{\frac{R + jwL}{G + jwC}} \tag{1.3}$$

The most important term of equation (1.2) is the attenuation constant, which is approximately expressed as:

$$\alpha = \frac{R}{2}\sqrt{\frac{C}{L}} + \frac{G}{2}\sqrt{\frac{L}{C}} \tag{1.4}$$

The characteristic impedance equation can be also re-written as:

$$Z_o = \sqrt{\frac{L}{C}} - j\sqrt{\frac{L}{C}}\left(\frac{R}{2wL} - \frac{G}{2wC}\right) \tag{1.5}$$

For the sake of simplicity, the series resistance due to the transmission line length, is trivially small and neglected; hence equation (1.4) and (1.5) become [73]:

$$\alpha = \frac{G}{2}\sqrt{\frac{L}{C}} \tag{1.6}$$

$$Z_o = \sqrt{\frac{L}{C}}\left(1 + j\frac{G}{2wC}\right) \tag{1.7}$$

Owing to equations (1.1) and (1.6), a signal received at the end of a TL is exponentially dependent on its conductance. Hence, the attenuation of the transmission line could be negative, if RTDs with their inherently negative resistance feature are used as active load.

This contributes to providing gain at the output node of the circuit without a need of using three terminal devices.

1.5 Optoelectronics for Fibre-to-the-Home applications

As the work presented here is also involved with optoelectronic integrated circuits design and testing, an overview of optical communications field is necessary. Further discussions including characterizations and simulation methods of optoelectronic receivers are presented in detail in chapters six. The increased growth in data traffic makes the demand for high capacity data transferring ever more pressing[78]. Free space RF transmission system is unfortunately unable to support large bandwidth (10Gb/s) and to ensure a long-distance transmission, relatively large power is required. For cable data transmission architectures, radio frequency signal propagation over coaxial cables is easy to implement with IC transceivers; however, this is only used for short distance and low data rate applications due to the cables losses and bandwidth limitation[78]. Accordingly, these transmission system technologies are currently becoming inefficient in accommodating the mainstream of high data rate market requirements.

By contrast, fibre optic links are being used increasingly as a replacement over the conventional coaxial cable and waveguide signal distribution. Fibre-optic communication is defined as sending information over a distance by transferring pulses of light through a fibre and at the receiver side the data is then converted into electrical signals, which can be easily processed by electronic circuits. Generally, the advantages of fibre-optic communication have led to considering this system architecture as the most favourable transmission solution in many applications. Advantages include the tremendously large bandwidth obtained (exceeding 50THz), corresponding loss of as low as 0.2-0.5dB/km and allowing long distance (>100km) at high data rate of >10Gb/s and insensitive to electrical disturbance with almost no crosstalk effect among fibre channels in the same cable[78-80]. For example, twisted copper cables have a bandwidth length product of 10 Mbkm/s, whereas a single mode fibre (SMF) optics can indeed provide 10^6 Mbkm/s[81]. In addition to the aforementioned applications, many supercomputing and server systems in data centres are currently utilizing optical rack to rack interconnections, providing an effective solution for space reduction. This technology is used for short communication distances starting from a few mm for on-chip to several cm for off-chip applications[82].

20km is a standard distance between central office and subscriber for well-established international optical systems, large bandwidth requirement can only be supported exploiting optical fibre transmission such as fibre-to-the-home (FTTH) networks[81]. Passive optical networks (PON) are recently becoming widespread system for FTTH and these networks form point-to-multipoint (P2MP) architecture with no need for an active star configuration, allowing reduction in the installation cost and avoiding extra maintenance cost as well. The only downside of using the PON configurations is that loss in the power splitter/combiner associated with such architecture causes marginally shorter optical link lengths in comparison with active star configuration[80].

As an optical architecture standard, 2.5Gb/s gigabit PON (GPON) is being deployed and the next generation 10Gb/s EPON (IEEE 802.2av, ratified September 2009) started to be deployed in late 2013[80, 83]. Due to the passive splitter/combiner used in PON systems which is shared by every optical network unit, ONU (i.e. customers), employing a multiple access technique is indispensable to avoid data transmitted collisions. Hence, several multiple access techniques have been proposed to address this issue. Furthermore, time division multiplexing (TDMA) is considered one of the most appealing methods that have the capability to provide high data rate communications with modest complexity[84].

In 2012, time and wavelength division multiplexed (TWDM) was chosen to be the favoured solution dedicated for the next PON generation stage 2 (NG-PON2)[85]. The main principle is to realize 40Gb/s data rate systems using four different wavelengths, in which each single wavelength provides 10Gb/s (i.e. 4×10Gb/s)[86]. The importance of this system is that it can be extended to 100Gb/s employing 10 different wavelengths. However, the transceiver design would be complex, making the cost of this technique unaffordable for end customers. To overcome this drawback, efforts were devoted to demonstrate a single wavelength photoreceiver, that is able to support high data rate of 40Gb/s and beyond[83, 87]. The outstanding progress carried out in optical systems is strongly based on the massive improvement in III-V semiconductor device technology over the last three decades.

1.6 Major Contributions and Thesis Overview

The aim of this thesis is thus to study the double barrier resonant tunneling diode characteristics and pave the way towards commercial, high performance and reliable

RTD-based circuits. This includes realizing high-frequency oscillators and microwave amplifiers. The work started with further investigation of the ultra-high frequency characteristic of RTDs obtained from their I-Vs and equivalent circuit parameters and developing accurate physical models and equivalent circuits. This has involved the use of various indium-rich quantum well epilayer structures in the attempt of maximizing the performance of the double barrier tunneling devices to be then tailored to *mm*-wave/THz applications. The key-driving force is to bias the RTD in the unique NDR feature and developing fully integrated circuits. This required the use of passive elements, namely resistors, MIM capacitors and spiral inductors which have been thoroughly modelled and characterized in this research. Furthermore, optimization of the coplanar waveguide configurations was carried out including their dimensional and effective relative dielectric constant impacts. The aim was to choose the most suitable values and dimensions of the passive components for actual circuit operation in RF and *mm*-wave/THz regime frequencies.

A complementary objective of this work was to characterize and model a transimpedance front-end amplifier (TIA) integrated with a PIN diode for high data rate exceeding 10Gb/s optical receivers utilizing an InP/InGaAs HBT. Different amplifier topologies were realized with the main purpose of optimizing their high-speed capabilities. The heterojunction transistor and PIN photodiode were individually fabricated and tested, followed by experimentally validating their equivalent circuits up to 40GHz. Various window sizes of the PIN-PD were fabricated using a top-illuminated configuration at a standard optical wavelength of 1.55µm. The transimpedance amplifier was designed and realized in Keysight-ADS software, exploiting a series peaking inductor to alleviate the loading effect of the photodiode's capacitance on the TIA and hence enhancing the bandwidth of the integrated circuit. In-depth discussion and analysis related to monolithically integrated photoreceiver module will be highlighted in later chapters.

The organization of this thesis is presented into seven main chapters. The first chapter contains the background information concerned with emerging RTDs devices, covering introduction, terahertz frequencies and applications as well as the aims and objectives of the work. This chapter also focuses on the conceptual principle of the optical architecture standard and relevant topics, such as FTTH and gigabit PON systems. Chapter 2 summarises the literature reviews of resonant tunnelling diodes over the last three

decades providing a solid underpinning of material systems used and developments in the structures and characteristics of the tunnelling devices. Later in this chapter, discussion of the DC and high frequency characteristic of five different double barriers InGaAs/AlAs RTD samples is described and a comparison of their performance with state of art devices is undertaken. Chapter 3 is devoted to a description of the design procedures and equivalent circuit model of the relevant passive components for the IC realisation comprising: resistors, capacitors, spiral inductors and coplanar waveguides. The module presented in chapter three was predominantly built using 2.5D electromagnetic momentum simulator. Chapter 4 covers the modeling of an RTD integrated circuit, the involving design of a high performance, room temperature oscillator operating at 100GHz and a very low DC power consumption K-band reflection-based amplifier. This correspondingly describes how to satisfy conditions that needs to be fulfilled for proper circuit operation.

Chapter 5 presents the background and state of the art of an InP based HBT transistor and PIN-photodiode starting from their working principle and their most common used figure of merits, followed by comparing those characteristics and performance with other conventional technologies. Chapter 6 concentrates on characterizing the realized Agilent-HBT model and opto-electrical equivalent circuit of the PIN-PDs. It also highlights the mask design procedure and briefly describing the fabrication process of both devices. The achieved results are then compared with recent reported work in an attempt at giving an insight into critique of well-designed epilayer structure of the transistor and microfabrication process used throughout the research. Later in this chapter, the high speed OEIC design for >10Gbs optical communication systems is presented. An overview of such integrated circuit technologies and ways to improve their figure of merits, such as -3dB optical bandwidth and overall gain utilizing a specific technique is discussed. This includes employing both single and multiple feedback topologies in designing transimpedance amplifiers. Finally, Chapter 7 details the conclusions and possible research ideas that could be followed in future. This comprises some important aspects linked to the most appealing milestones achieved through the PhD programme and also potential improvements to further extend this project.

CHAPTER 2: CHARACTERIZATION OF DOUBLE BARRIER RESONANT TUNNELING DIODES

2.1 Introduction

This chapter focuses on three important aspects of this thesis. The basic operating principle and heterostructure design of the double barrier resonant tunneling diodes are of paramount importance prior to venturing into investigation of such a device's characterization. These include an in-depth description of the development in the material systems used for high diode's performance. The RTD DC characteristics, namely peak voltage, maximum negative differential conductance, peak current density and peak to valley current ratio (PVCR) are presented in this chapter. These characteristics are broadly studied for five different RTD structures, from which an optimum device structure is discussed, followed by a study of the influence of self-heating effects on the I-V characteristics of the devices.

Later in this chapter, RF equivalent circuits and parameter extraction of the RTDs are covered including radio frequency output power capability and estimations of the transit delay time in the double barrier quantum well and collector depletion regions. The experimental findings and the extracted parameters are then compared with recently reported state of art tunneling devices.

2.2 Quantum Tunnelling Phenomena

Tunneling is a quantum-mechanical phenomenon which was first discovery in the 20th century as a result of an extension study of radioactivity. In classical mechanics, particles (i.e. electrons) are confined by potential barriers and only particles whose energy are equal or exceed the potential barrier height can get across. This approach has been used for thermal emission of carriers to describe the operational principle of diodes. By contrast, in quantum mechanics description, a particle has both wave and particle properties[26]. A consequence of the wave nature is that this wavefunction is not instantaneously terminated at the boundary of the barrier. Thus, an electron has a finite transmission probability of tunneling through a barrier if the barrier thickness is thin enough. In semiconductor technology, homojuction semiconductor materials with abrupt

doping or heterojunction structures with multilayers can be exploited to create such a potential barrier. These structures involve growing compound, ternary and quaternary materials, as well as requiring insulators and metals in the fabrication process.

To this effect, the probability of electrons tunneling through a barrier is not equal to zero. This leads to the concept of tunneling probability and tunneling current, the first one can be found through solving Schrödinger equation in the different regions. Electrons travelling in a semiconductor crystal can be described using wave functions (ψ) that are solutions of the Schrödinger equation:

$$\frac{d^2\psi}{dx^2} + \frac{2m^*}{\hbar^2}[E - V(x)]\psi = 0 \tag{2.1}$$

Where x is the position vector, m^* is the effective mass of electron, $V(x)$ is the potential energy at position x, E is the total energy of the electron and ħ is the reduced Planck constant. Figure 2.1 depicts a structure, which is divided into two regions by a barrier, and how an electron tunnels through the barrier due to its wave property.

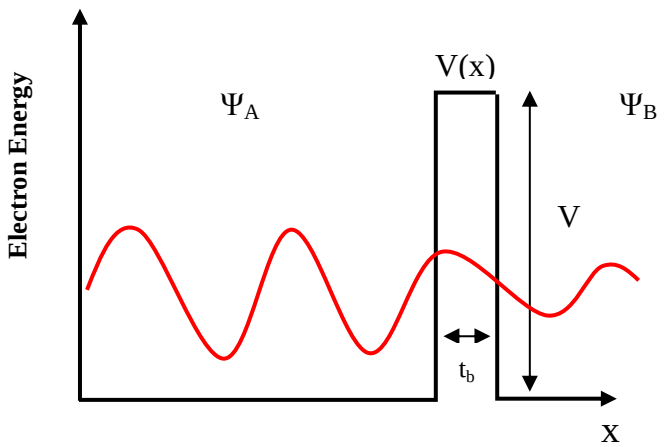


Figure 2.1: Wavefunctions showing electron tunneling through a potential barrier.

In the case of a single potential barrier of height V and width t_b, ψ has a general form $exp\ (\pm ikx)$, where $k = \sqrt{2m^*(E - V)}/\hbar$. Note that for tunneling mechanism, the energy E is below the barrier V, so that the term within the square root is negative and k is imaginary. The solution of the wave functions gives the transmission probability for a single barrier:

$$T_t = \left|\frac{\psi_A}{\psi_B}\right|^2 \approx \frac{16E(V-E)}{V^2} exp\left(-2t_b * \sqrt{\frac{2m^*(V-E)}{\hbar^2}}\right) \quad (2.2)$$

For a given energy value, a finite transmission coefficient can be obtained using a low barrier height and small effective mass as well as the approach of thinning the barrier itself. The overwhelming contributing feature of quantum based devices is the carriers' tunneling time across a potential barrier, which is dominated by the quantum transition probability per unit time instead of the conventional transit time concept[88]. This is highly useful in many applications due to the extremely short transit time, providing ultra-fast switching speed well into the *mm* and sub-*mm* wave regions.

2.2.1 Double Barriers Resonant Tunnelling Diode Structures

As a result of the great accuracy of Molecular Beam Epitaxy, atomic layer deposition of thin and uniform layers is readily achievable. The total thickness of RTD layers can be made thin enough (i.e. 200Å to 400Å) compared with the electron mean free path, or the de Broglie wavelength ($\lambda = h/P$), h is the Planck constant and P is the electron momentum. A simple DBQW RTD is composed of a small band gap material (GaAs) sandwiched between two large band gap materials (AlAs) as shown in figure (2.2). The difference in band gaps of these semiconductor compounds results in conduction and valence band discontinuities, denoted as ΔE_C and ΔE_V respectively.

In general, electrons in DBQW heterostructure can move freely in the x-y plane, where there is a continuous energy state distribution. In contrast, the separation between the energy levels in the quantum well, for example E_{n1} and E_{n2}, is larger than the electron's thermal energy (kT). This would lead to the particles appearing to be frozen into the ground state ($n = 1$) (discrete energy level) as illustrated in figure (2.2)[89]. It also means that carriers can only move in the plane perpendicular to the growth direction, while incapable of moving in the crystal growth direction (confinement direction). In such a case, the energy states inside the quantum well are indeed quantised due to quantisation of the electron wave function. The electron energy in the quantum well can be expressed as:

$$E = E_n + \left(\frac{\hbar^2}{2m^*}\right)\left(k_x^2 + k_y^2\right) \quad (2.3)$$

Where

$$E_n = \left(\frac{\hbar^2\pi^2}{2m_w^*}\right)\left(\frac{n^2}{{t_w}^2}\right) \tag{2.4}$$

Where n = 1, 2, 3… is an integer denoting the energy level index, E_n is the quantisation energy in the quantum well and m_w^* and t_w are the electron effective mass inside the quantum well and the thickness of the quantum well respectively.

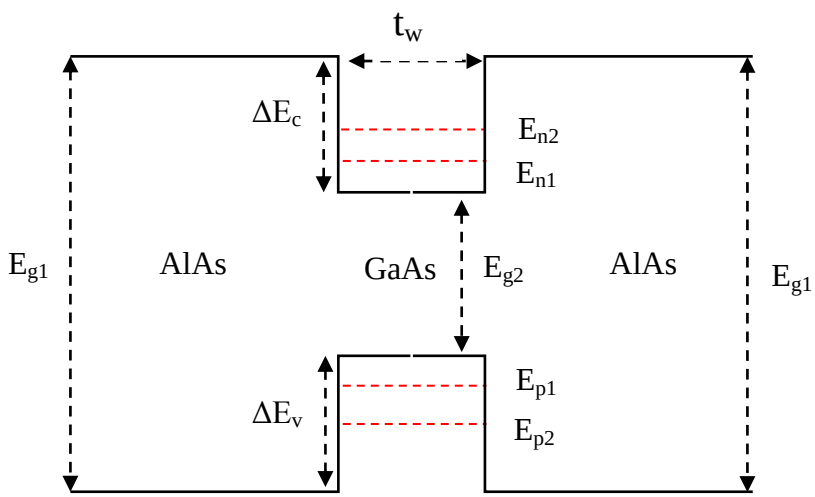


Figure 2.2: Band diagram of DBQW, the quantum well (GaAs) sandwich between two wide band gap materials of AlAs (barriers).

The broadening of the nth resonant level (ΔE) in the quantum well is given by the Wentzel-Kramers-Brillouin (WKB) approximation:

$$\Delta E_n = E_n\, exp\left(-2t_b\sqrt{\frac{2m_{e,t}^*(V - E_n)}{\hbar^2}}\right) \tag{2.5}$$

Where t_b is the barrier thickness, V is the barrier height and $m_{e,t}^*$ is the tunneling effective mass at energies close to the emitter conduction band[90]. The transmission coefficient (T_E) the full-width at half-maximum of the resonant level (i.e. T=0.5) can be approximated by:

$$T(E) = \frac{4T_{Lb}T_{Rb}}{(T_{Lb} + T_{Rb})^2}\left[1 + \left(\frac{E - E_n}{\frac{1}{2}\Delta E_n}\right)\right]^{-1} \tag{2.6}$$

Where T_{Lb} and T_{Rb} are the transmission coefficient through the left and right barrier respectively and E is the incident electron energy that is lower than the potential barrier height, V. As stated in equation (2.4), the resonant level in the quantum well can be pushed up through reducing the well width or/and growing a material with a low electron effective mass in the quantum well resulting into a higher value of the peak current density and peak voltage in the RTD. However, this leads to a lower potential barrier height by $(V - E_1)$ for the incident electrons with energy around E_1, broadening the width of the resonant level (ΔE_n) and so an evident improvement in the transmission coefficient (i.e. tunneling current) can be realized[91]. Furthermore, the energy difference between the adjacent resonant energy levels increases for narrower quantum well RTD structure. This contributes to a reduction in leakage current through the second resonant energy level, raising the peak-to-valley current ratio (PVCR)[92].

The lifetime of the electron in the resonant state, which represents the transit time of the carriers through the double barriers quantum well (τ_{dwell}) is given by:

$$\tau_{dwell} = \frac{\hbar}{\Delta E_n} \tag{2.7}$$

The positive outcome from widening (ΔE_n) is shortening τ_{dwell}, thereby a significant increase in the maximum operating frequency of the device is expected. Since the transmission coefficient is exponentially dependent on the barrier thickness as given by (2.8), further increase in the current density alongside high frequency device performance can be achieved as the barrier gets thinner.

$$T \propto exp(-2kt_b) \tag{2.8}$$

Where $k = \sqrt{2m_{e,t}^*(V - E_n)/\hbar^2}$ being k is the wave vector in the barrier[93]. One of the major characteristics of quantum tunnelling phenomena is that the tunnelling time is dominated by the quantum transition probability per unit of time instead of the conventional transit time. It means that the tunnelling time is ultrashort reaching several tens of femtoseconds compared with conventional transit time-based devices whose delay times are in the order of a picosecond. This offers an outstanding potential

switching speed for the resonant tunneling diodes, making them among the fastest of all solid state electronic devices. The first experimental demonstration of the DBQW RTD was reported by Chang *et al*[94]. This unique heterostructure has become one of the most common type RTD structure. In addition to the main DBQW layers, facilitating the function of a typical RTD device implies other associated layers as depicted in figure (2.3).

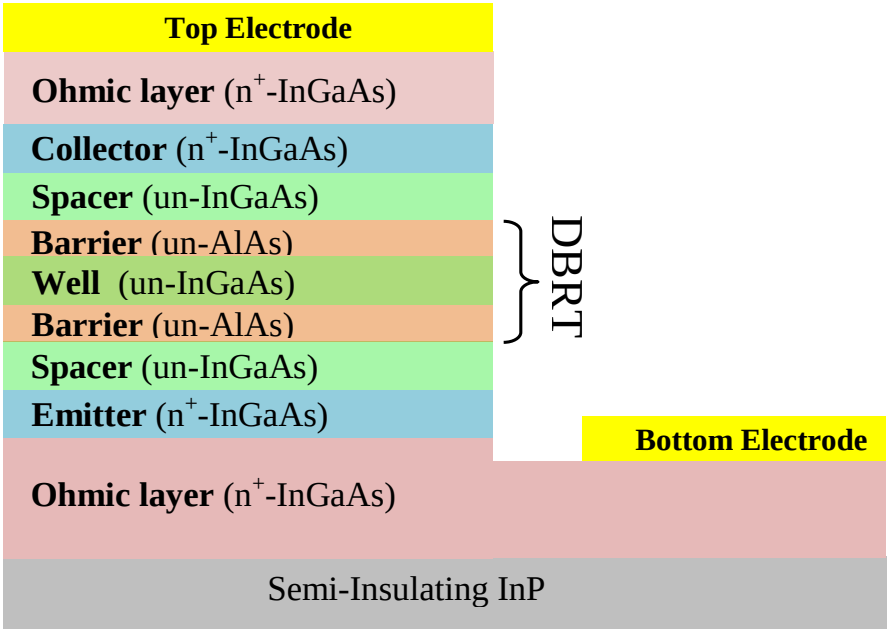


Figure 2.3: A typical epilayer structure of double barrier RTD using InGaAs/AlAs material system.

The structure is grown on a lattice matched InP semi-insulating substrate as this avoids generating additional defects, which would otherwise degrade the performance of the device. To enable low ohmic contact resistance, very heavily doped $In_{0.53}Ga_{0.47}As$ ($\geq 10^{19}$ /cm^3) is used for the contact layers; however, lightly less doped (3×10^{18} /cm^3) layers are exploited for the emitter and collector layers. This speed up the charge carriers due to the electrostatic forces created by the gradient of the emitter conduction band under bias and so a sufficient current density can be obtained.

The reason behind using undoped spacer layer is to minimize diffusion of donors from the doped emitter and collector to subsequent layers during growth, for instance from the n^+-InGaAs into the AlAs. This is due to the diffusion of impurities to such key regions will increase carriers scattering events; hence the current density of the device degrades. Furthermore, transport time of the carriers through the double barriers and quantum well (τ_{dwell}) will increase because of impact of incoherent tunneling effect[95]. It is

important to point out that the width of the barriers and spacers are not necessarily symmetry on both sides of the well as asymmetrical RTD structures are occasionally used in some particular applications such as high output power RTD based oscillators [96].

2.2.2 Operating Principle of DBQW Resonant Tunnelling Diode

There are many types of tunnel diode structures which are either double well, triple well or super-lattice structure. As stated in section (2.2), the wave function across the barrier indicates that an incident particle from the emitter side can appear in the collector side of the barrier if certain conditions are fulfilled. These can be satisfied by ensuring a sufficiently thin barrier with low height or/and small effective mass of an electron, since all these factors increase the finite transmission coefficient. The term "resonant" refers to electrons behaviour whose kinetic energies are lower than the barrier height; nevertheless, they are still able to pass though the potential barriers. The tunnelling probability of carriers is defined by the transmission coefficient, which is theoretically unity at the resonant state[97]. The operating principle of the DBRTD can be deduced using the conduction band diagram shown in figure (2.4). There is an interaction between charge carriers released from the emitter layer and the discrete energy states in the well, depending on the external applied voltage. The following series of graphs depicted in figure (2.5) show how the different applied voltages relate to the three main regions of the device's I-V characteristics. It is known that when the forward bias voltage applied (V_b) is zero, no current is observed as the first resonant quantised state is above the Fermi-level.

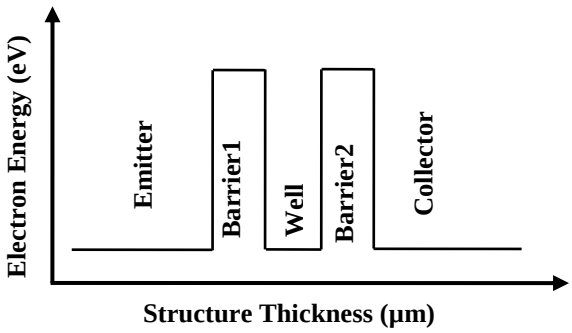
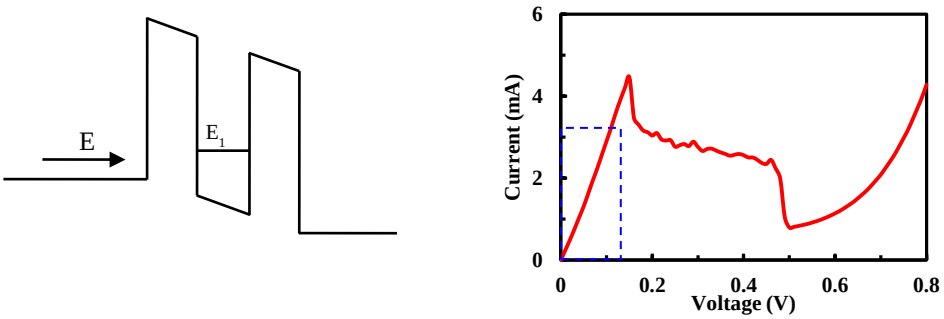
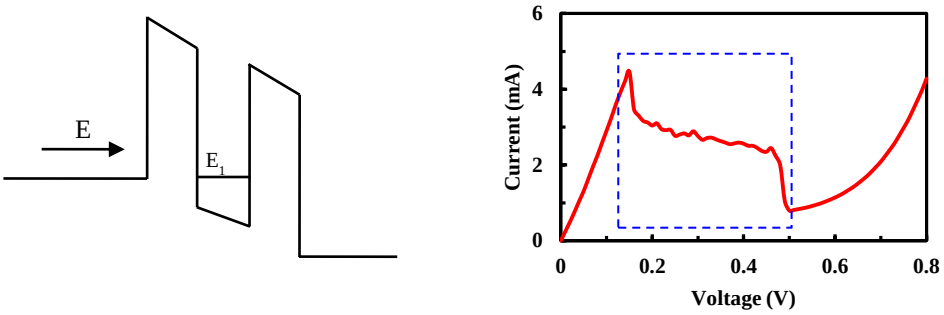


Figure 2.4: A conduction band of the energy band diagram profile of a double barrier RTD showing the barriers and quantum well as well as emitter and collector regions.

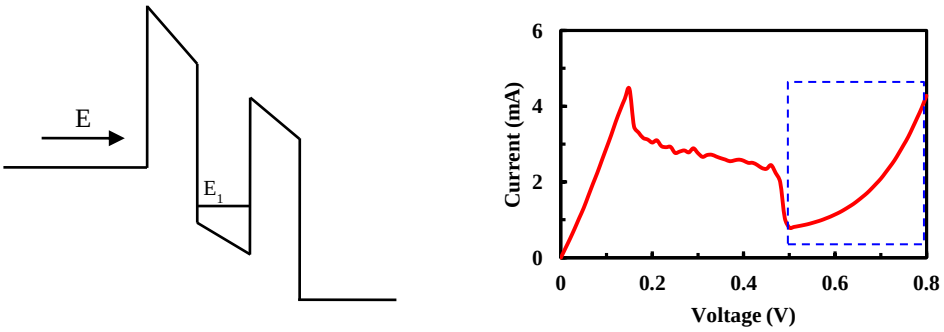
However, with a low external bias voltage, there is a small amount of current passing through the diode due to the existence of a number of electrons which have sufficient energy to surmount the barrier (figure (2.5, a)). The tunnelling probability also increases in accordance with the voltage bias. With further increase in the bias voltage, the electron energy in the collector side relative to that on the emitter side is lowered by $-eV_b$, pulling down the first confined state towards resonance.



(a) Low bias voltage, exhibiting the positive differential resistance (PDR) region.



(b) Resonant tunneling through E_1 followed by misalignment between the conduction band edge of the emitter and E_1, producing the negative differential resistance (NDR) region.



(c) High bias voltage, no tunnelling current through the first resonant level

Figure 2.5: Energy band diagram and corresponding regions in the IV characteristic of double barrier RTD under various bias voltages.

At this stage (figure (2.5, b)), the conduction band edge aligns with the first quantised state energy (E_1), which allows resonant tunneling through the double barrier to occur. This corresponds to a maximum current flow (I_P) in the device and at this point the applied DC bias is called the peak voltage (V_P)[98]. When a larger bias voltage is applied, the first resonant energy moves down the conduction band offset, the current subsequently drops due to off resonance condition as shown in figure (2.5, b and c). The voltage, at which current flow is minimum, is called the valley voltage (V_V) and the DC current is thus the valley current (I_V). The unique region between the peak and valley voltages is referred to as the negative differential resistance (NDR)[99]. From this, the crucial parameter of peak-to-valley-current ratio (PVCR) can be calculated using $PVCR = I_P/I_V$ [100].

The transmission coefficient decreases with further increase in the voltage bias until thermal emission mechanism takes place as shown in figure (2.5, c). This makes the number of electrons with high enough kinetic energy to overcome the barrier increases proportionally, hence the current starts to rise again. The high current of the second positive differential resistance (PDR) region is probably due to the thermionic emission phenomena and a small participation from an alignment with another allowed resonant level in the well. However, the first mechanism is evidently dominant; otherwise, an additional NDR region would be clearly exhibited.

2.2.3 State of Art RTD Material Systems

The capability of engineering the band-gaps of group III-V compound semiconductors is the most appealing feature that stimulates researchers to extensively use them in a range of applications. There is also the attraction of high electron mobility properties and hence, higher current density characteristics[101]. In general, high quality atomically thin layers have benefited from sustained developments in the MBE technique. This has been reflected by the growth of a wide range of semiconductor compound materials with accurate control of thickness to within a fraction of a monolayer as is indeed needed for tunneling devices. One such example is the QCL which requires many 100s of layers. Heterostructure devices give the designer lots of degrees of freedom in terms of offering different characteristics and features. However, there is a limitation to selecting pairs of

semiconductor materials as the possibility of creating lattice misfit dislocations at their interface is readily possible if their lattice constants are different. This implies particular attention when choosing two different materials by making sure that they have very close lattice constants, to avoid interface disturbance caused by breaking bonds. For two dissimilar materials forming a heterojunction, an abrupt difference in their lattice constants can generate crystalline defects. The localized states in the device structures act as trapping centres for carriers, contributing to undesirable impact on the device characteristics and performance.

The relationships between energy band gap for III-V and II-VI compounds plotted versus their lattice constants is depicted in figure (2.6)[102]. For instance, the conventional resonant tunneling diodes are grown based on GaAs technology, where GaAs and AlAs materials represent the well and barriers respectively. Both have almost identical lattice constants with a very small mismatch of $1x10^{-3}$ as shown in figure (2.6).

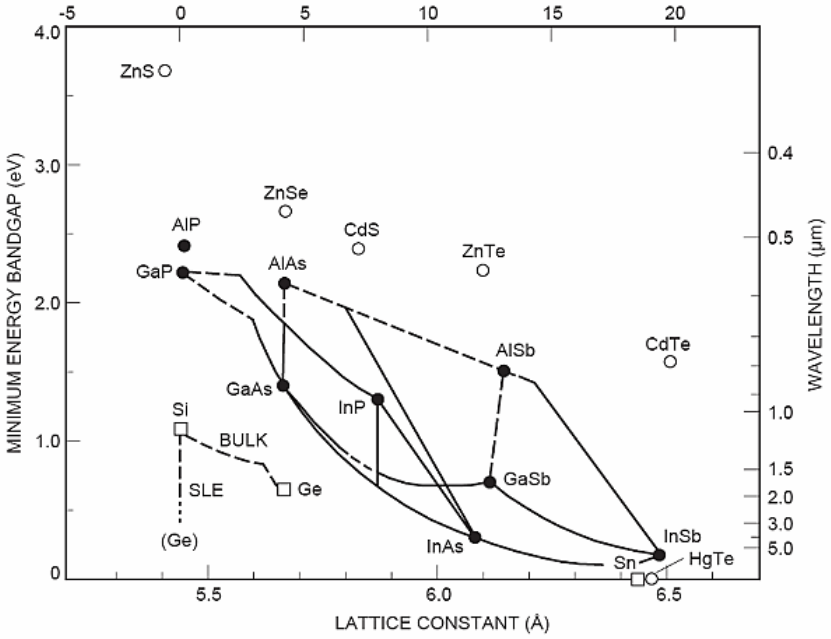


Figure 2.6: Energy band gap of III-V and II-VI compounds plotted versus their lattice constants for both direct (solid line) and indirect (dashed line) at room temperature[102].

The large difference in the band gap of these materials is preferred to produce large band discontinuity, GaAs and AlAs have band gap of 1.42eV and 2.83eV respectively (Both compounds are direct band gap material with a Γ-Γ tunneling mechanism). Slightly dissimilar lattice constant material systems can be grown with built-in strain. However, this is constrained to a certain critical thickness of epitaxial layer growth, which is

theoretically calculated based on the difference between the lattice constant of the materials[98]. From the electronics industry point of view, the preferred semiconductor material is silicon as it is compatible with ICs technology. This is the reason why a large number of attempts in accomplishing an interband RTD device harnessing Si/SiGe have been carried out. Due to the small conduction band discontinuity provided by Si/SiGe technology, there is not sufficient effective quantum confinement in SiGe DBQW structures[103]. An interband tunneling Si/SiGe device incorporating a δ-doped layer was recently demonstrated with PVCR of ~1.8, but with an extremely low current density of 0.01mA/μm^2[104]. To the best of our knowledge, the highest current density of SiGe RTD achieved to date is 2.18mA/μm^2[105]. On the basis of this consideration, resonant tunneling devices made of SiGe material systems still suffer from particularly severe drawbacks, degrading PVCR or/and peak current density with later being a significant issue.

On the other hand, the key advantages of III-V RTDs over conventional Si technology make the diodes capable of achieving high current density together with low peak voltage and large PVCR[93]. After resonant tunnelling was first proposed in 1973[1], many researchers succeeded in demonstrating the double barrier heterostructure using GaAs/$Al_{0.7}Ga_{0.3}As$ shortly afterwards in 1974[94, 106]. There has been an issue related to this particular RTD, which only exhibits a negative differential resistance at low temperatures (77K). This took a long time until it was resolved in 1985 by Shewchuck *et al*, who successfully reported a double barrier GaAs/$Al_{0.25}Ga_{0.75}As$ RTD showing an NDR at room temperature with a PVCR of 1.5. Variation in the mole fraction of AlGaAs ternary material was the key-factor behind this highly useful characteristics in RTD progress[106].

However, the conduction band offset obtained from GaAs/$Al_xGa_{1-x}As$ heterostructure is small, resulting in increased leakage current through to the upper resonant level and so providing inherently low PVCR values. In addition to this, the GaAs/$Al_xGa_{1-x}As$ has low electron mobility due to relatively high effective mass as shown in Table (2.1). These parameters are of importance in assessing the high current density capability of the devices. As an alternative approach, GaAs/AlAs RTD has supplanted the conventional GaAs/$Al_xGa_{1-x}As$ structure in an attempt to increase the potential barrier height, which is translated into improvement in the current density of the devices. The first demonstration

of GaAs/AlAs resonant tunnelling diode was reported in 1985 by Tsuchiya *et al*[107]. Later on, an impressive peak current density (J_P) of 2.5mA/μm^2 using GaAs/AlAs RTD grown using MBE technique was obtained[108] for a device size of 5μm^2.

TABLE 2.1: LATTICE CONSTANT, BAND GAP AND ELECTRON EFFECTIVE MASS OF COMMON BINARY AND TERNARY COMPOUND SEMICONDUCTOR MATERIALS USED TO REALIZE RTD AT 300K.

Alloy	Lattice Constant, (Å)	Energy gap, Eg (eV)	Effective mass, m*
$Si_{1-x}Ge_x$	$5.431+0.20x+0.027x^2$	$1.12-0.41x+0.008x^2$ (x<0.85) $1.86 - 1.2x$ (x>0.85)	$0.19m_0$ (x<0.85) $0.159m_0$ (x>0.85)
Si	5.431	1.12	$0.98m_0$
$Al_xGa_{1-x}As$	$5.6533+0.0078x$	$1.9+0.125x+0.143x^2$	$(0.067+0.083x)m_0$
GaAs	5.653	1.42	$0.067m_0$
AlAs	5.661	2.16 (indirect) and 2.83 (direct)	$0.1m_0$
$In_{0.52}Al_{0.48}As$	5.852	1.44	$0.075m_0$
$In_{0.53}Ga_{0.47}As$	5.868	0.76	$0.044m_0$
InAs	6.058	0.36	$0.023m_0$
AlSb	6.135	1.58	$0.12m_0$
$In_{0.8}Ga_{0.2}As$	5.978	0.49	$0.032m_0$
InP	5.869	1.35	$0.077m_0$

The impact of growth temperature on GaAs/AlAs RTDs I-V characteristic was also investigated and accomplished the highest PVCR of 5.35 reported to date[109]. The group led by Professor Missous at the University of Manchester has recently presented a GaAs/AlAs resonant tunneling diode with a very low peak voltage of 0.28V, attributed to the material condition used and an excellent growth control in the barrier down to fractions of a monolayer[110]. Further steps towards improving the performance of the tunneling devices were accomplished using the lattice matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ on a InP substrate in 1986[101]. This structure has a higher conduction band offset and a lower electron effective mass than the conventional

GaAs/AlAs material systems as depicted in Table (2.1); nevertheless, not much difference in outcomes were obtained in terms of J_P and PVCR.

Additional efforts by researchers led to pseudomorphic $In_{0.53}Ga_{0.47}As$/AlAs heterostructure operating at room temperature as proposed by Inata *et al* in 1987[111]. The benefit of utilizing an AlAs barrier instead of InAlAs is attributed to its low alloy-related scattering. This is limited by a requirement of sufficiently thin AlAs barrier (<3nm) for pseudomorphic growth onto the $In_{0.53}Ga_{0.47}As$ subsequent layers and hence causing a negligibly small concentration of misfit dislocations[112].

The highest peak to valley current ratio obtained using $In_{0.53}Ga_{0.47}As$/AlAs RTD is 23[111] and as high J_P as 6.8mA/µm^2 was later demonstrated by Shimizu *et al*[113]. Meanwhile, as these materials are highly attractive and promising for more improvement in RTD structures, incorporation of a low band gap InAs in the well has also been reported[114]. The key was to introduce a deep quantum well besides providing a large interval between the resonant levels, leading to achieving a very high PVCR of 30 at room temperature[114]. The highest J_P reported to date for RTDs with an InAs sub-well technique is 4.5mA/µm^2[115]. However, this is at the expense of an increase in the peak voltage to 0.7V, leading to a device with relatively high DC power consumption.

Benchmarking of the pioneering Esaki tunnel diode performance was performed using InGaAs technology grown on InP substrate and achieved a recorded J_P of 22 mA/µm^2[116]. Since then, several attempts were made to evaluate such a diode performance utilizing Si platform[117, 118]. In 2015, Paul Thomas *et al* experimentally investigated $In_{0.53}Ga_{0.47}As$ Esaki tunnel diode grown on Si substrate via graded buffer and obtained a PVCR and J_P of 12.9 and 0.3mA/µm^2 respectively[119]. Unlike InP-based RTDs, III-V Esaki tunnel diodes undergo an extensive variation in the valley current of the I-V characteristic among devices due to defect-assisted current mechanism[120]. Furthermore, these devices have rather thin depletion regions necessary for tunneling to occur, resulting in increased intrinsic capacitance in the range of a few tens of picofarad. This does show that Esaki-based tunnel diodes are not suitable for *mm*-wave/THz region applications.

Generally speaking, the aforementioned GaAs and InGaAs based RTDs have type-I band offset compared with technologies using Sb-containing semiconductor materials. In 1991 Brown *et al* achieved an oscillation frequency up to 712GHz for an RTD oscillator taking the advantage of InAs/AlSb material system[121]. Such a structure has several advantages in comparison with GaAs/AlAs devices; firstly InAs/AlSb has a staggered type-II band offset, making the attenuation coefficient of the carriers which tunnel through AlSb barrier smaller than that in the AlAs barrier. This simply reflects into high current density capability for a given barrier thickness[122, 123]. An InAs cap layer offers nearly ideal ohmic contacts, which in turn improve the maximum operation frequency of the device. Moreover, a very low effective mass of the InAs well does not merely contribute to an increase in the confinement energy, but also result in further minimizing the transit time across the collector depletion region[124].

2.2.4 Overview of Indium rich Double Barrier RTDs

Since indium-containing semiconductor materials can be heavily doped to 3×10^{19} cm^{-3}, these devices are now very popular among the RTD community as their associated parasitics are further minimized. More importantly, variation in the indium composition of the InGaAs material can easily offer promising properties particularly advantageous for high electron mobility, high band-offsets, and provide low ohmic contact resistance characteristics[125]. Accordingly, an indium rich InGaAs in the quantum well (i.e. $In_{0.8}Ga_{0.2}As$) was proposed by Matsuzaki in 2002[126].

A highly-strained compressive quantum well $In_{0.8}Ga_{0.2}As$ with AlAs barriers RTD was grown using Metal-Organic Vapor-Phase Epitaxy (MOVPE) technique[127]. Characterizations of the double barrier RTD with In-rich wells was reflected by exponentially dependent J_P on the AlAs barrier thickness[127]. Since then, this ternary material has been extensively studied by both NTT Photonics Laboratories and the Tokyo Institute of Technology research groups. The most important feature of utilizing In-rich InGaAs wells is to effectively produce a high peak current density at low voltage bias. The key driving is mainly due to the facility of pulling down the first resonant level in the quantum well[128], which is basically considered an alternative approach to the aforementioned InAs sub-well structure.

In 2003, NTT Photonics Laboratories reported a strained $In_{0.8}Ga_{0.2}As$/AlAs RTD grown on InP substrate and obtained J_P of 1.46mA/μm^2 at peak voltage of 0.43V and with a PVCR of 7.7[129]. A high peak current density of 4.09mA/μm^2 with a PVCR of 3.8 was simultaneously achieved by decreasing the barrier to 4 monolayer thickness[129]. Further increase in J_P to 13mA/μm^2 with a PVCR of 1.5 was demonstrated in a collaboration between NTT Photonics Laboratories and the Tokyo Institute of Technology research groups in 2008[130]. This result was attained by growing a thin AlAs barrier of 1.4 nm with 6 x 10^{18} cm^{-3} doping profile in the cap layer.

Later, Suzuki *et al* demonstrated a very high J_P of 24mA/μm^2 but at a high peak voltage of approximately 0.8V utilizing an AlAs barrier thickness of 1.2 nm and a graded spacer from the emitter side for use at ~ 1THz oscillation frequency[131]. This was then followed by reporting a higher current density of 28mA/μm^2 at a V_P of ~ 0.9 V, also exploiting a graded indium composition spacer layer for an RTD oscillator with a fundamental frequency of 1.08 THz[132].

In 2012, a room temperature fundamental oscillation of 1.31THz with 23mA/μm^2 high peak current density was achieved by Asada *et al* employing $In_{0.8}Ga_{0.2}As$ material [133]. In late 2014, an RTD oscillation frequency of 1.42 THz was demonstrated by the same author using In-rich well and emitter graded InGaAs/AlAs RTD[134]. Further increase in the indium mole fraction of the well alongside with a graded In-rich cap layer led to a J_P of 34mA/μm^2 and an oscillation frequency of 1.86THz[8]. It was followed by the highest peak current density of the double barrier RTDs reported to date of 50mA/μm^2 with an impressive oscillation frequency of 1.92 THz using offset slot antenna and about 0.1μm^2 mesa size device[135]. This remarkable finding was accomplished by the Tokyo Institute of Technology research groups as a consequence of extensive work in this particular field for many years, contributing to massive improvements in the structures of the resonant tunneling diodes and of course utilizing In-rich wells.

An attempt was made for realizing even higher J_P RTDs using wide band gap energy III-nitride was demonstrated [136, 137]; however, GaN-based devices still suffer from lack of reproducibility, mostly attributed to deep energy level trapping centers, which in turn degrade the peak to valley current ratio[138, 139]. The quality of these materials is not suitable yet for an effective RTD characteristic especially under the condition of the

available epitaxial growth technology. This is because the misfit dislocations exacerbate the degradation in the NDR characteristics of the GaN-based tunneling devices[140]. Instead, III-nitride material system is currently paramount in highly linear low distortion power amplifier implementations[141, 142].

Recently, highly compressively strained In-rich quantum well RTDs were successfully grown on semi-insulating InP substrates using the MBE technique at the University of Manchester facility. The objective was to achieve a high current density feature employing reasonably simple tunneling device structure. Additional aims were the use of these devices in sub-millimeter wave RTD oscillators. In-depth discussion and analysis related to the RTD sources including device characterizations, MMIC technology and oscillator components are elaborated in this and following chapters.

2.3 Photolithography and RTD Mask Design

Design of the device layout for desirable RTD performance requires extra care in terms of avoiding needless distances that might introduce additional parasitics. Feature sizes in this work were restricted to ~1μm resolution using conventional i-line photolithography technology. Despite this limitation, this technology is fairly easy to use and much more affordable than electron beam lithography (EBL) technology. Since EBL technique is superior in high resolution processing, this system is preferable in submicron scale device fabrication though the throughputs are very low[143]. Mask designs and layouts for individual RTD devices and MMIC RTD oscillators were extensively developed over the period of the PhD research.

After the growth process was accomplished, wafers were diced into 15mm×15mm size tiles. The fabrication procedure requires defining the device sizes including the top and bottom contacts alongside with bond pads for on-wafer probing measurements. With this in mind, the mask was designed with different mesa sizes of the RTD, such as square and finger devices (i.e. 6×6, 5×5, 4×4, 3×3, 2×2, 1×5, 1×4, 1×3, 1×2μm^2). The photo-mask used in this thesis is built employing Agilent Advanced Design System (ADS) software. It is generally composited of four steps and an example of a 2×2μm^2 emitter size is depicted in figure (2.7).

As mentioned above, the RTD devices were fabricated using standard i-line photolithography and utilized both dry and wet etching techniques. Furthermore, the fabrication of all devices in this project was performed in a clean room environment of class 1000. Even though laminar air flow and filter system controls the source of the contaminants all the time, there are still a few ways that cause samples contamination. These include handling the samples by human operators and other contamination is related to processing equipment[92]. On the basis of this consideration, during the preparation of the samples and before each step, the tile is cleaned with various solutions or/and techniques. The preparation steps are briefly discussed as follows: N-Methyl Pyrrolidone (NMP) solution is used to remove pollutants adhered on the surface of the sample. As some residues remain after performing the NMP process, the tile is then washed with high purity de-ionised (DI) water. To entirely eliminate the remnants of NMP, the sample is dunked into Acetone for 5 minutes in an ultrasonic bath. The next step was to dip the sample into an Iso-Propan-ol (IPA) solution for 5 minutes, providing a clean suface from Acetone remnants. This is eventually followed by using nitrogen (N_2) gun to blow-dry the sample.

The basic processing of the RTDs can be summarized into four steps, starting by the self-aligned technique in which the deposited top contact was employed as a hard mask (step#1). After lifting-off the metallization, the self-aligned mesa diodes were formed using reactive ion etching (RIE) of the top contact with methane and hydrogen in the ratio of 1:8. This dry etching was used to provide an almost isotropic side-wall, alleviating the effect of the leakage current that causes degradation in the PVCR of the devices. From this, the effective area of the device was defined with a mesa size of $2\times2\mu m^2$ as shown in figure (2.7). As the highly doped InGaAs cap layer does not act as an etch-stop layer, the mesa etching time is adjusted in order not to remove the ohmic layer where the bottom electrode is sitting. This step was then followed by the bottom contacts (step#2) deposited, allowing wet etching of the self-aligned air-bridges and device isolation to be carried out using H_3PO_4:H_2O_2:H_2O in a ratio of 3:1:50 (step#3).

All these steps are depicted in figure (2.7) showing the pattern dimensions designed in the mask. The distance between the layer structure and bottom electrode in step#2 was optimized to be 2μm due to the restrictions of the photolithography resolution. This crucial parameter determines the spreading resistance of the device and is considered one

of the major influences on the RTD radio frequency performance. In-depth investigation regarding the series resistance and RF characteristics of the RTDs will be elucidated later in this chapter.

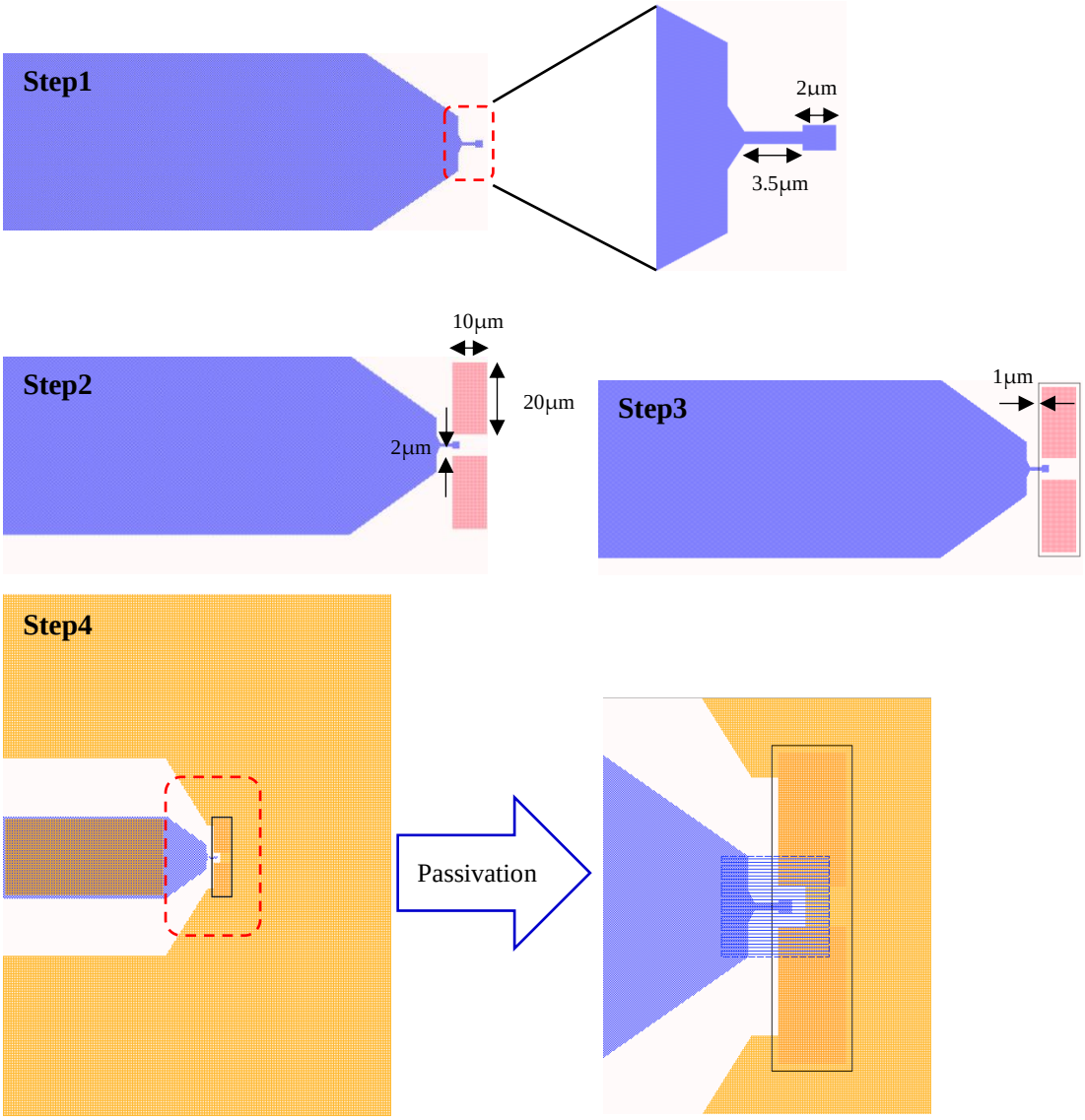


Figure 2.7: Top view of the RTD photo-mask designed using Agilent ADS software showing the process step by step for a 2×2 μm^2 device size as defined by the mask patterns.

Since the conventional wet etching does not only etch vertically, but it also etches the defined pattern laterally in the range of 0.25 to 0.5μm^2, depending on several parameters, for instance the concentration of the chemical solution used and the epilayer structure in terms of the material systems and their thicknesses. In fact, there are two major benefits which can be gained from the lateral etching profile; firstly the fabrication process would end up with smaller RTD sizes than the designated patterns, thereby improve the

performance of the diode at high frequencies. Secondly, this allows to completely open the area beneath the air-bridge strip; otherwise either the device size would be so large and dominated by the bottom contact area or it might result in a substantial deterioration of the NDR feature. Therefore, the wet-etching process had to be performed through carefully extending the isolation etching time and choosing a sufficient bridge length of 3.5µm to make sure the undercut process is complete. Figure (2.8) shows a cross section view of an InGaAs/AlAs RTD, including the electrodes and air-bridge formation.

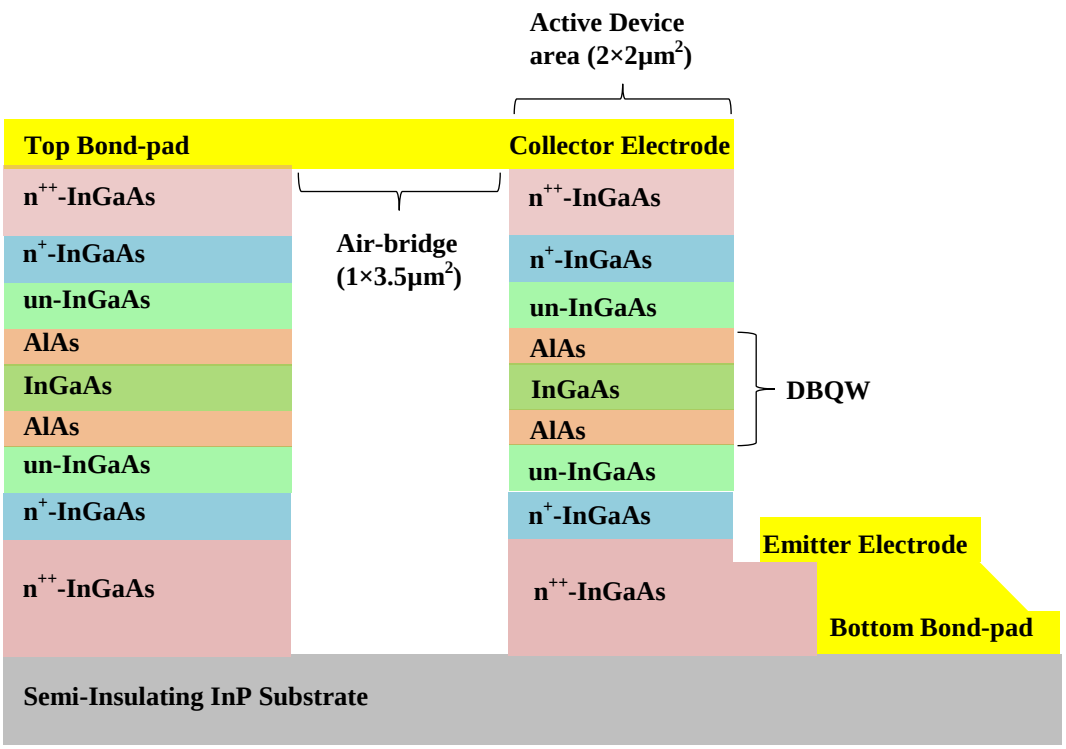


Figure 2.8: Cross section view of a 2×2 µm^2 InGaAs/AlAs RTD device size, clearly indicating the air-bridge formation. Note that the drawing is not to scale.

The downside is that the undercut profile attacks the area beneath the bottom contacts, contributing to potentially breaking the connection with the following step. To prevent this from happening, 1µm tolerance was pre-defined by covering the area all around the edges of the bottom contacts as shown in figure (2.7) step#3. Due to the large dimensions of the bottom electrode (10×20µm^2) with heavy doping profile ohmic layer, negligibly small contact resistance is obtained. It is worthwhile highlighting that the isolation of the device down to the semi-insulating substrate surface makes the surrounding devices electrically isolated. The non-alloyed ohmic contact scheme used was a thermally evaporated Pd/Ti/Pd/Au for both upper anode and lower cathode electrodes with a

thickness of 10/20/20/700 nm. Step#4 was dedicated for the coplanar waveguide (CPW) formation with standard dimensions, enabling the realization of 50Ω characteristic impedance necessary to match with S-parameter probe measurements.

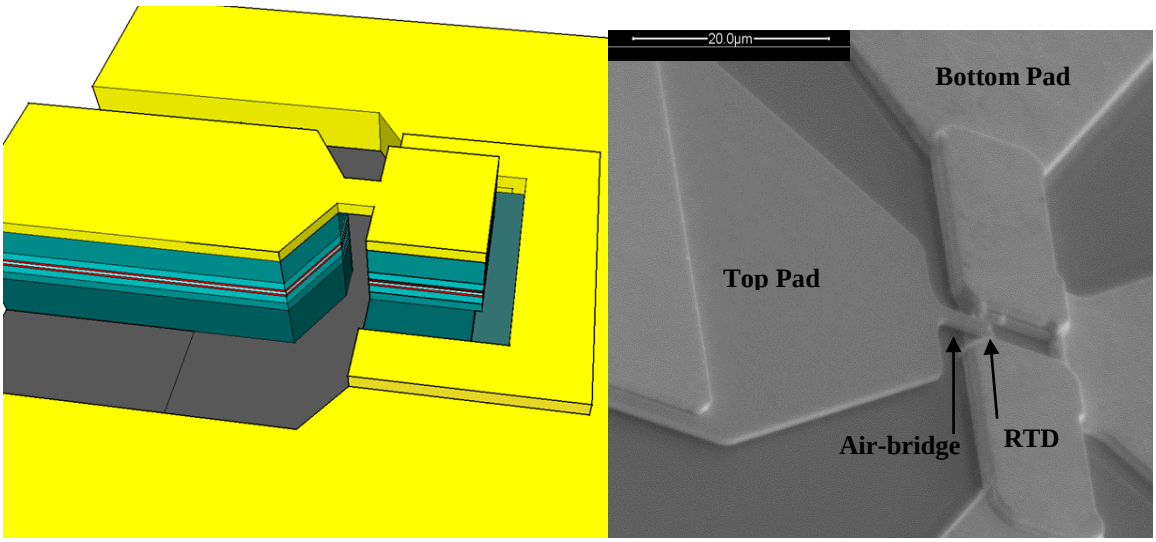


Figure 2.9: 3D schematic and SEM images of the fabricated device with a mesa size of 2×2 and 1×2 μm^2 respectively, showing the active device, air-bridge and bond pads.

The fabrication process ends-up with two main mesas, the passive and active areas. The passive mesa refers to no current passing through such an area, which is beneath the signal line of the CPW, see figure (2.8), whilst the current flows in the active mesa of the RTD and to avoid any variation in the characteristics of the diode, this area was passivated using photoresist layer as shown in figure (2.7). The 3D schematic of an ultimately fabricated RTD involving the active device and bond pads is depicted in figure (2.9).

2.4 Device Structures and Characteristics

Among all heterostructure tunneling diodes, double barriers InGaAs/AlAs RTDs, have been intensively investigated[37, 61, 144, 145]. This includes numerical modeling, improvement in fabrication process and significant progress in THz wave applications. To satisfy the increasing demands in high data rates wireless communications, downscaling of device sizes to submicron features is required to further minimize the intrinsic RTD capacitance, providing high speed operation beyond 1 THz [67, 146]. To this end, achieving a useful indoor propagation distance necessitates a high output power

source at such frequencies. This can be accomplished in two ways: first by boosting the peak current density (J_P) and second by reducing the electron intraband transit time. Thus, investigating and improving the DC characteristics of the resonant tunneling diodes is significantly important for RF circuit implementations. Previous related work using pseudomorphic InGaAs/AlAs/InAs and thin and deep quantum well InGaAs/AlAs RTDs demonstrated high current densities of 4.5 and 14.5mA/µm^2 respectively [115, 128] as well as tens of femtoseconds transit times[127, 128]. There is a compromise to be struck between achieving high J_P and the complexity of the epitaxial growth process, for example using graded spacers or cap layers or/and emitter layer with quaternary materials for lower voltage bias[8, 132].

This work, however, shows that high current density RTDs can be obtained with relatively uncomplicated epitaxial layer structures. It also concentrates on a comparative investigation of five different diodes epitaxial structures at the attempt of improving the performance of the devices. All the RTDs were grown by Prof. Missous at the UoM, an In-rich quantum well sandwiched between two AlAs barriers was utilized in this project. The epilayer of these devices were grown on lattice-matched semi-insulating InP substrates using Solid Source Molecular Beam Epitaxy (SSMBE). Figure (2.10) depicts the epitaxial stack the RTD samples, which are denoted as XMBE#276, #277, #300, #302 and #327, relying on the variation in their DBRTD structures and both spacer regions.

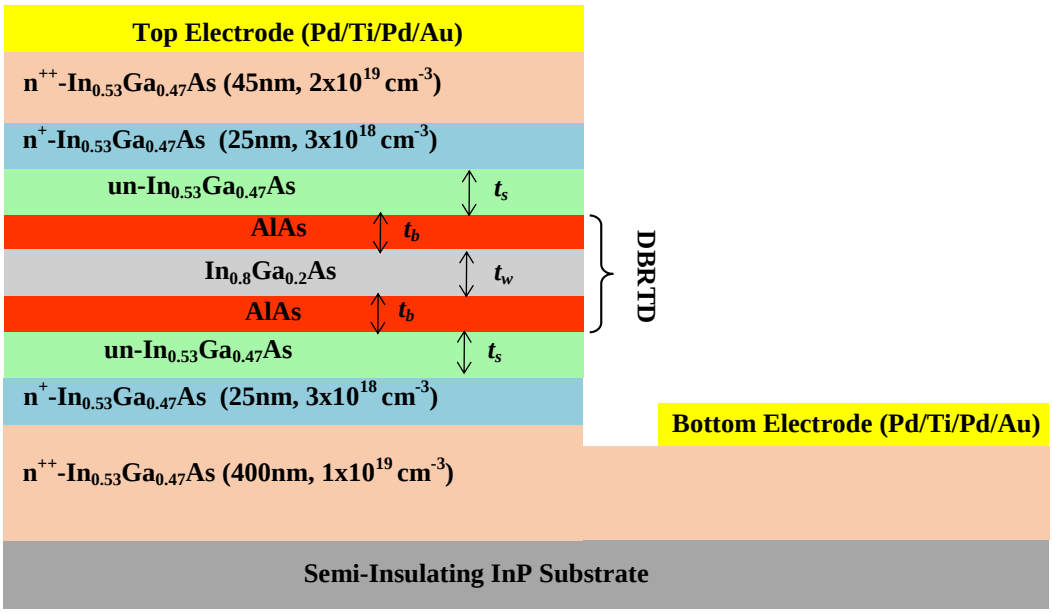


Figure 2.10: Typical RTD structure including layer dimensions of the double barrier quantum well layers and spacers regions which are varied in the five structures investigated.

The undoped layers of the RTD samples from the top collector spacer to bottom emitter spacer consist of $In_{0.53}Ga_{0.47}As$ collector spacer, AlAs collector barrier, $In_{0.8}Ga_{0.2}As$ quantum well, AlAs emitter barrier and $In_{0.53}Ga_{0.47}As$ emitter spacer respectively. Dimensions of the DBQW and spacer layers are tabulated in Table (2.2). All other layers' thicknesses are indicated in figure (2.10) and are kept similar for all RTD samples. First of all, the role of each layer function is discussed. It is well-known that metal-semiconductor contact resistance plays an important role in limiting the high frequency operation of devices. Therefore, the highly doped $In_{0.53}Ga_{0.47}As$ cap layers are specified to minimize the series resistance of the diode. The doping profile of these layers almost reaches the upper limit of InGaAs material[147].

TABLE 2.2: DIMENSIONS OF THE DBQW AND SPACER LAYERS OF DIFFERENT RTD STRUCTURES.

DESIGN PARAMETERS	RTD SAMPLE				
	276	277	300	302	327
t_s (nm)	20	20	5	5	5
t_b (nm)	1.6	1.3	1.2	1.1	1.1
t_w (nm)	4.5	4.5	4.5	4.5	3.5

Both emitter (bottom) and collector (top) spacers are deliberately undoped to prevent diffusion of donor generated from the heavily doped regions to the subsequent layers during the growth process, for instance from the n^+-$In_{0.53}Ga_{0.47}As$ into the AlAs barrier. This is due to the fact that diffusion of impurities to such regions will increase carriers scattering events, resulting in a degradation of the current density of the device[148]. Furthermore, the transport time of the carriers across the collector depletion region increases with the thickness of the spacer; however, this is inversely proportional to the value of the intrinsic capacitance of the device. The reduction in ionized impurity scattering as the width of the spacer layers gets thicker, leads also to improving the PVCR. The is however at the expense of decreasing the peak current density due to a suppression of current stream in the thick spacers[149]. A trade-off between these parameters is therefore required. An increase in the oscillation frequency of a resonant

tunneling diode oscillator to 1.42THz was recently reported by optimizing the collector spacer thickness[150].

Emitter and collector layers are responsible for emitting and collecting carriers respectively. The conceptual framework of the DBQW layers was already discussed in section 2.2.2. Furthermore, the dependency of the RF parameter values extraction on the structure of the RTDs and their mesa sizes are highly useful for MMIC implementations based RTDs and this matter is discussed later in this chapter.

2.4.1 DC Characteristics

Once the fabrication process was successfully performed, the devices were then measured; figure (2.11) illustrates typical SEM images of a fabricated RTD device with a mesa size of 1×2μm^2, showing the air-bridge and top and bottom bond pads. The forward bias current densities of the diode samples XMBE#300, #302 and #327 as well as for samples XMBE#276 and #277 are depicted in figures (2.12) (2.13) respectively.

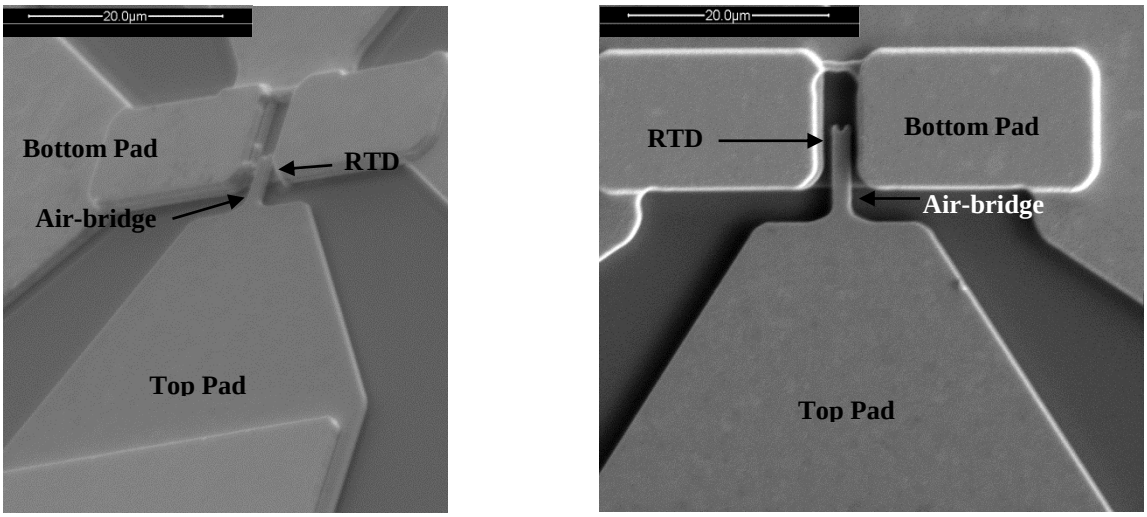


Figure 2.11: SEM images of an RTD with a mesa size of 1×2μm^2.

As expected, sample #327 has the highest J_P of 10.8mA/μm^2 due to the thin well and barriers, followed by sample #302 as shown in Table (2.3). The key DC characteristics parameters are tabulated in Table (2.3) including J_P, PVCR and the absolute value of the negative differential conductance (G_{RTD}). The parameter G_{RTD} can be approximately expressed as a function of the voltage span (ΔV) and current width (ΔI) (i.e. $G_{RTD} = (3/2)(\Delta I/\Delta V)$[7]. ΔV and ΔI being the voltage and current difference between the peak

and valley voltages and currents respectively, which can be basically extracted from the device's I-V characteristic. Apart from the peak current density of the devices, all other parameters are calculated for 4μm^2 device areas.

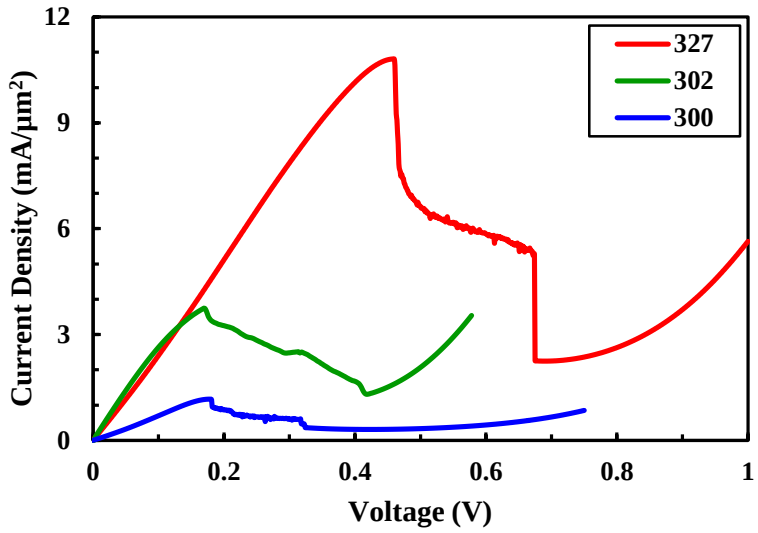


Figure 2.12: Current density of the RTD samples XMBE#327, #302 and #300.

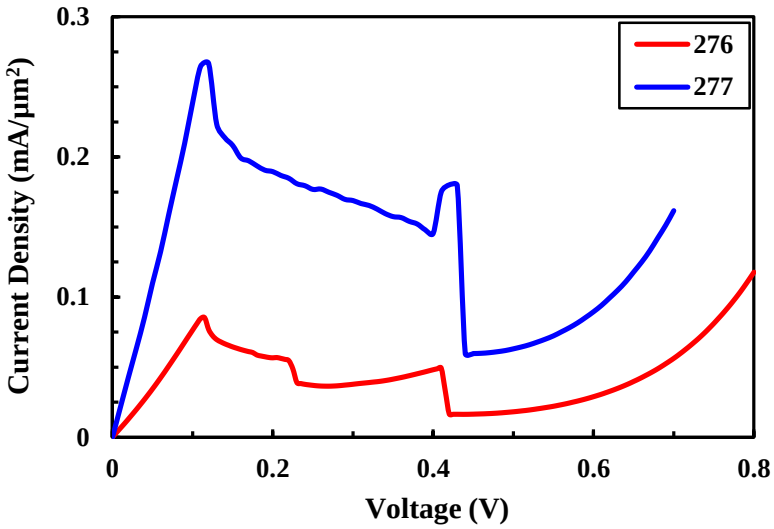


Figure 2.13: Current density of the RTD samples XMBE#276 and #277.

A thicker barrier, t_b (1.6nm) from the collector side of sample #276, can suppress additional current through the collector barrier [140], as compared with sample #277 contributing to the increase in PVCR. However, this is at the expense of a reduction in J_P. For high G_{RTD}, the width of the barriers for sample #302 was grown with a thickness of 1.1nm, providing a significant increase in current density. Table (2.3) shows good device characteristics including a high PVCR of 5.2 exhibited by sample #276 despite its

very low current density. A comparable PVCR value was achieved for sample #327 with a remarkable increase in J_P and G_{RTD} obtained through decreasing both well and barriers thicknesses.

TABLE 2.3: FORWARD BIAS DC CHARACTERISTICS OF THE DIFFERENT RTD STRUCTURES WITH 4μm^2 MESA SIZE.

DC CHARACTERISTICS	RTD SAMPLE				
	276	277	300	302	327
J_P (mA/μm^2)	0.08	0.26	1.1	3.7	10.8
PVCR	5.2	3.2	3.8	3	4.9
$\lvert G_{RTD} \rvert$ (mS)	1.4	3.8	19.6	76	260

Interestingly, the experimental data indicates that a high PVCR can still be obtained in relatively thick barriers and wells. Since a thick spacer region of 20nm for sample #276 offers less carrier scattering events, the PVCR has been improved. More importantly, further reduction in valley current of sample #276 is due to the existence of a wide collector barrier thickness of 1.6nm. These parameters have led to an additional increase in the PVCR feature. Generally, the incoherent tunneling mode caused by scattering mechanisms occurs because of interactions with impurities or/and defects encountered by the injected electrons[151]. Such an RTD characteristic emphasizes that this performance is undeniably important in implementation of RF circuit amplifiers with sub-milliwatt level DC power consumption[76, 152]. Conversely, this sample would not be suitable as a terahertz emitter due to its rather low estimated output power.

There is a trade-off between achieving a high J_P and the dependency of PVCR on spacer and DBQW dimensions. A well-designed asymmetrical RTD structure could effectively be a compromise between these key parameters, for example a thin t_b with a wide spacer layer from the emitter side alongside relatively thick t_b with a moderate spacer thickness from the collector side would contribute to increase in J_P whilst maintaining a high PVCR. It is known that reducing the quantum well thickness makes the separation

between the first and second resonant levels inside the well larger thereby improving the PVCR and with a considerable increase in J_P. Boosting of these two parameters was achieved for sample #327 which had a relatively simple epitaxial structure. Accordingly, a high G_{RTD} of 260mS was obtained. The structure's simplicity mainly refers to the fact that no graded or quaternary layers were used. Both of these would be extremely difficult to control in a manufacturing environment since the exact compositions and grading would need to be achieved over very small distances. The structures presented in this work rely exclusively on timing of shutter opening/closing without any change in temperature of the effusion cells during growth, making the structures much more reproducible. This is highly important for tunnel devices whose characteristics tend to exponentially depend on thicknesses.

Asymmetrical I-V characteristic of the RTDs were observed, mainly attributed to the existence of both "normal" and "inverted" InGaAs-AlAs interfaces and potentially any unintentional variation in barrier thickness which are possible in these multi-interface structures as depicted in figure (2.14). As the transmission probability of the RTDs is exponentially dependent on the barrier thicknesses[93], this might exacerbate asymmetry effect. Lower doping profile in the n^+-$In_{0.53}Ga_{0.47}As$ ohmic bottom layer compared with the top one could also have a small effect on the I-V symmetry. A similar behaviour has been previously reported by Wolak and Sugiyama[108, 129]. Furthermore, Tsao *et al* quantitatively investigated the characteristics of various GaAs/AlAs RTD structures and surprisingly claimed that the most symmetric I-V characteristics were found from asymmetric RTD barrier thicknesses on both sides of the quantum well[153].

Since precisely controlling the thickness of the DBQW and doping concentration as well as effectively balance between their impacts on the I-V characteristics are rather difficult, symmetric I-Vs for the resonant tunneling diodes cannot be straightforwardly attained. However, as long as the major contribution of these devices is the negative differential resistance, asymmetric I-Vs would be preferred, providing excellent characteristics in one of the bias directions.

As the current density of the RTDs is extremely sensitive to the barrier thickness, J_P achieved in reverse bias is three times that obtained in the forward bias directions. From figure (2.14), it can be seen that the peak voltages in reverse biases are pushed up compared with those observed in forward biases. This undoubtedly confirms that the

barrier from the collector side of the forward bias (top) seems to be slightly thinner, offering interesting characteristics for asymmetrical device structure, such as high PVCR and wide ΔV. However, physical modeling might be indispensable to further investigate this type of behaviour.

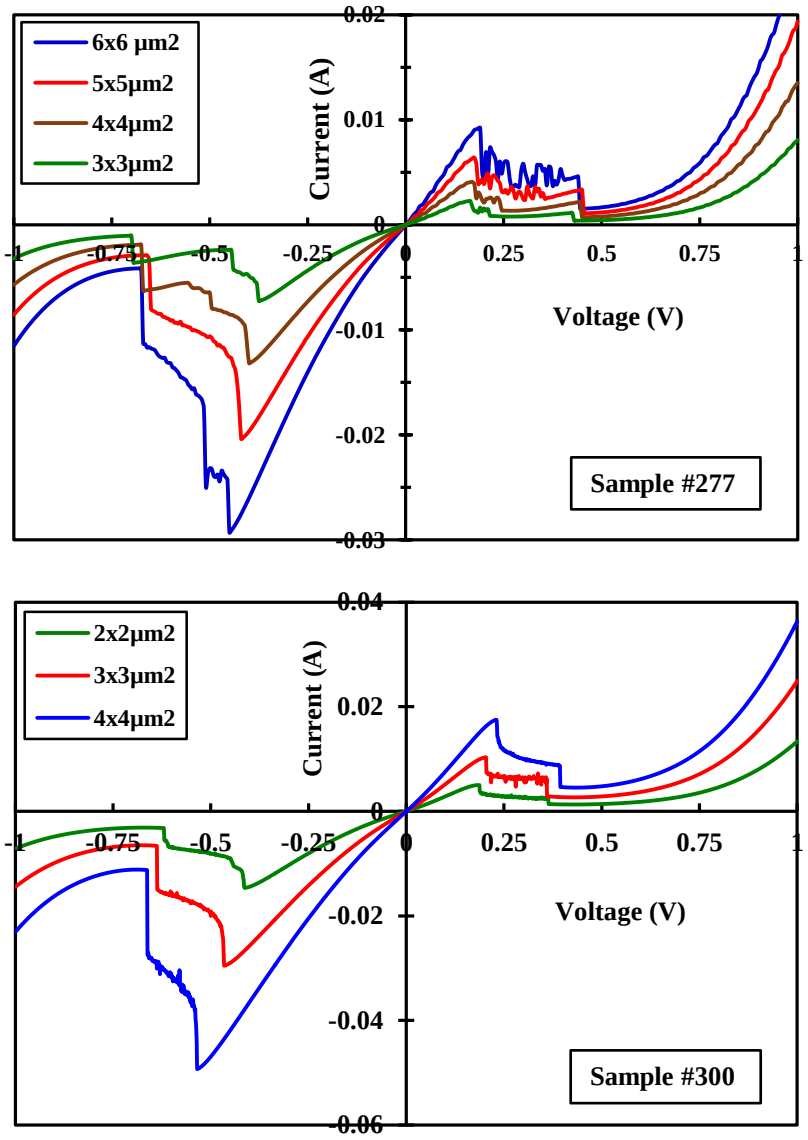


Figure 2.14: I-V characteristics of the RTD sample XMBE#277 and #300 with various mesa sizes, showing different characteristics in forward and reverse biases.

A degradation of the peak to valley current ratio as the size of the diode gets smaller can be noticed throughout the DC characteristics of the tunneling devices. It has been experimentally demonstrated[154] and the argument for the reduction in this figure of merit is attributed to a parasitic sidewall current. Thus, smaller undercut profile with

appropriate surface passivation is one of the potential ways used to improve scalability of the submicron devices[131, 154, 155], maintaining the PVCR value for small devices.

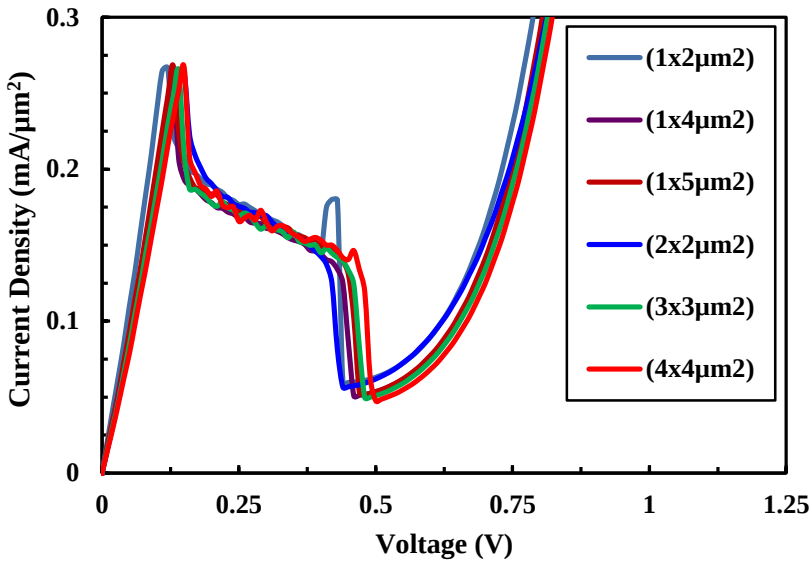


Figure 2.15: Current density of RTD sample XMBE#277 showing a very small variation in the valley current for small mesa diodes in comparison with large ones.

In this work, a small degradation in the PVCR was observed with scaling the RTDs down to small feature sizes as shown in figure (2.15). This is due to the consequence of an approximately isotropic side-wall (less undercut profile) achieved by the dry etching process. Table (2.4) and (2.5) summarize the forward and reverse biases DC characteristics of the RTD samples XMBE#276, #277, #300, #302 and #327 respectively. Both forward and reverse biases show a significant increase in the current width (ΔI) attributed to thin barriers and wells, resulting in an outstanding improvement in the G_{RTD} as depicted in Table (2.4) and (2.5). By contrast, this has contributed to a decrease in the voltage span (ΔV) which is considered detrimental to the output power of high frequency oscillators. To avoid repetitive discussions of the forward bias characteristic, the rest of this section is predominantly concerned with the remarkable RTD features obtained in the reverse bias direction.

Taking advantage of In-rich quantum well, a relatively low peak voltage is achieved in reverse bias voltage; however, it notably increases with reducing barrier or/and well widths. In reverse bias, samples #276, #277 and #300 have a J_P that is three times higher than those obtained in the forward direction. This is not the case for the RTD sample #302 whose peak current density is just about double. Once more, the reason is most

likely due to the unintentional variation in the thickness of the barriers and other aforementioned impacts.

TABLE 2.4: SUMMARY OF FORWARD BIAS DC CHARACTERISTICS FOR DIFFERENT RTD STRUCTURES WITH A MESA SIZE OF 4μm^2.

RTD SAMPLE	DC CHARACTERISTICS					
	$\|\Delta V\|$ (V)	$\|\Delta I\|$ (mA)	V_P (V)	J_P (mA/μm^2)	PVCR	$\|G_{RTD}\|$ (mS)
276	0.32	0.3	0.11	0.08	5.2	1.4
277	0.28	0.7	0.12	0.26	3.2	3.8
300	0.26	3.4	0.18	1.1	3.8	19.6
302	0.2	10.2	0.21	3.7	3	76
327	0.19	33	0.53	10.8	4.9	260

TABLE 2.5: SUMMARY OF REVERSE BIAS DC CHARACTERISTICS FOR DIFFERENT RTD STRUCTURES WITH A MESA SIZE OF 4μm^2.

RTD SAMPLE	DC CHARACTERISTICS					
	$\|\Delta V\|$ (V)	$\|\Delta I\|$ (mA)	$\|V_P\|$ (V)	J_P (mA/μm^2)	PVCR	$\|G_{RTD}\|$ (mS)
276	0.38	1.2	0.32	0.33	6.7	4.7
277	0.31	3.2	0.4	0.94	6.2	15.5
300	0.27	10.4	0.41	3.3	4.6	57.7
302	0.2	16.6	0.37	6.4	2.7	124.5
327	0.12	44	0.71	14.3	4.2	550

More interestingly, the promising PVCR values obtained with low J_P characteristics for the device samples #276 and #277 are greatly beneficial for radio frequency MMIC implementations with ultra-low DC power consumption. For example, several RF amplifier circuit topologies, which consume sub-milliwatt level DC power, have been recently reported using either conventional tunnel diodes or double barrier RTDs as active loads[76, 152, 156]. As far as the requirement for good characteristics of the RTDs

including J_P, PVCR and G_{RTD} are concerned, samples #302 and #327 would be chosen for oscillator circuit design and implementations.

TABLE 2.6: ROOM TEMPERATURE OPERATION OF INGAAS/ALAS RTD STRUCTURES GROWN AT THE UNIVERSITY OF MANCHESTER COMPARED WITH STATE OF ART.

REPORTED IN	DESIGN PARAMETERS AND TECHNOLOGY				DC CHARACTERISTICS		
	INGAAS/ALAS (nm)	SPACER (nm)	RTD EPILAYER	DEVICE SIZE (μm^2)	J_P ($mA/\mu m^2$)	PVCR	$\lvert G_{RTD}\rvert$ ($mS/\mu m^2$)
#302 (REVERSE BIAS)	$In_{0.8}Ga_{0.2}As/AlAs$ 4.5/1.1	5	SIMPLE	2	6.4	2.7	29
XMBE#327 (FORWARD BIAS)	$In_{0.8}Ga_{0.2}As/AlAs$ 3.5/1.1	5	SIMPLE	2	10.8	4.8	95
XMBE#327 (REVERSE BIAS)	$In_{0.8}Ga_{0.2}As/AlAs$ 3.5/1.1	5	SIMPLE	2	14.3	4.2	185
[129]	$In_{0.8}Ga_{0.2}As/AlAs$ 4.5/1.2	N/A	SIMPLE	2×3	1.46	7.7	9
[129]	$In_{0.8}Ga_{0.2}As/AlAs$ 4.5/1.2	N/A	SIMPLE	2×3	4.09	3.8	~40
[130]	$In_{0.8}Ga_{0.2}As/AlAs$ 4.5/1.4	2	SIMPLE	N/A	12.9	1.5	66
[134]	$In_{0.9}Ga_{0.2}As/AlAs$ 3/1	12	COMPLEX	N/A	18	~2.1	38
[134]	$In_{0.9}Ga_{0.2}As/AlAs$ 3/1	6	COMPLEX	N/A	23	~1.8	67
[8]	$In_{0.9}Ga_{0.2}As/AlAs$ 2.5/1	6	COMPLEX	N/A	34	~2.2	66
[135]	$In_{0.9}Ga_{0.2}As/AlAs$ 2.5/1	12	COMPLEX	N/A	50	1.7	77

From RTD oscillator's perspective, both current difference and voltage span are favoured to be as large as possible, to ensure high RF power delivered to the load. Relevant quantitatively analysis is discussed for all RTD samples in section 2.6.4. Unlike the resonant tunneling diodes studied in this work and grown by the MBE technique, RTDs reported in literature has been mainly grown using MOVPE technology. Similarly, those device structures were optimized to achieve as high a current density and PVCR characteristics as possible. However, there are several fundamental differences related to exploiting emitter and collector with quaternary materials or/and graded layers in comparison with the devices investigated in this research. Comparison between DC characteristics of the $In_{0.8}Ga_{0.2}As/AlAs$ RTD sample XMBE#327 and #302 and recently published works are tabulated in Table (2.6). The simplicity of the RTD samples with excellent figure of merits achieved is evidence that these devices are suitable for low cost *mm*-wave/THz applications. The MBE grown XMBE#327 RTD exhibits a double PVCR value compared with previously reported works.

The most prominent finding is the high G_{RTD} obtained for the same sample, which is the highest reported to date and is greatly promising for sub-micrometer scale devices used in integrated RTD based circuits. Basically, these results are achieved as a direct consequence of the excellent grown conditions and materials used alongside appropriate fabrication steps throughout the process flow. Furthermore, the excellent G_{RTD} obtained for the RTD sample XMBE#327 can enable manufacturing RTD transmitters with small stabilizing resistor of <6Ω, improving the circuit performance in terms of lower noise operation and high DC-to-AC conversion efficiency. This is particularly useful for implementing ICs with relatively large RTD sizes ranging from several to a few micrometres (i.e. whose G_{RTD} is ≥ 0.4S).

2.4.2 Self-Heating Effect

Since an efficient RTD circuit design requires low DC bias voltage, reduction of the peak voltage of the devices is highly desirable. From the experimental I-V data, shifting of the peak voltage with peak current density of the diode was observed. Though such influence was briefly discussed in[157], clarifying it has not been quantitatively presented. This previous work claimed that a drop-in voltage at the contact layer could be the reason behind this behaviour. However, in practice, the contact resistance (and of course the

overall resistance) of the RTDs decreases as device dimension increases, so there must be other sources causing this behaviour. In this work, the measured data reveals different trends for each RTD sample which are extremely peak current density dependent. Figure (2.16) shows that only a small deviation occurs in V_P with device sizes for the low current density RTD sample #276. However, a significant variation in I-V characteristics was found for the high current density sample #327 at the peak voltage as depicted in figure (2.17).

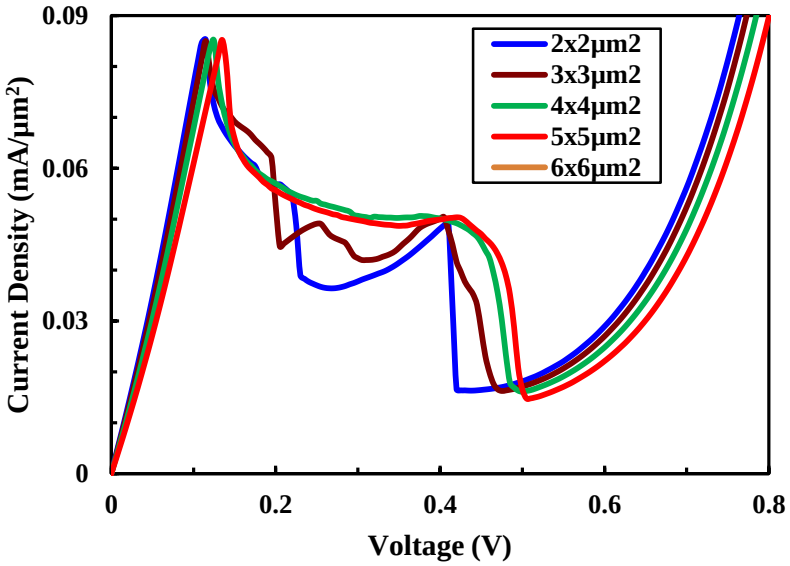


Figure 2.16: Current density of RTD sample XMBE#276 with different device sizes showing only a small variation in the peak voltage.

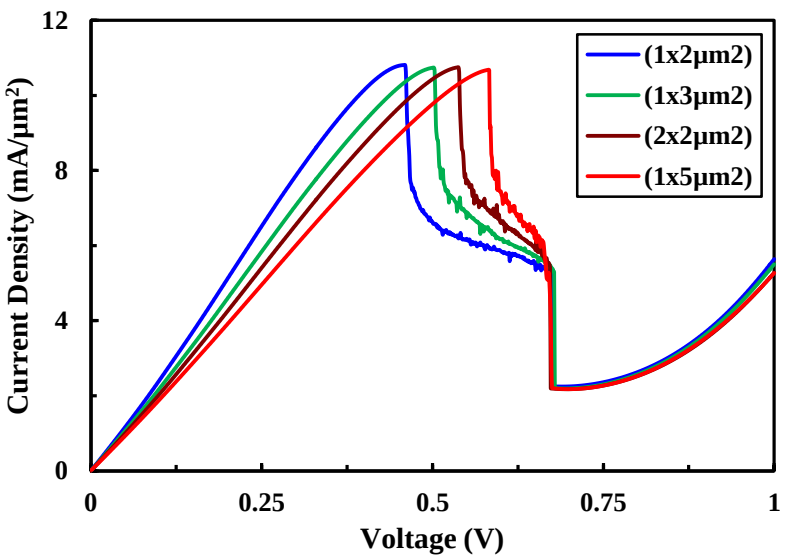


Figure 2.17: Deviation in the peak voltage of the RTD sample #327 for various device sizes.

Deviation in V_P with mesa size was found to be negligibly small for devices with low J_P (samples: #276, #277 and #300). On the other hand, this increase in peak voltage rises considerably for high peak current density RTDs (samples: #302 and #327) as shown in figure (2.18). The RTD samples #302 and #327 have deviation in V_P in the range of 14 and 36mV/μm^2 respectively. These findings are interpreted as follows: the diodes with high J_P (and higher areas) are heated up due to the high current passing through them, causing excess carrier scattering and in particular throughout the entire doped layers. Reduction in the mobility of the electrons consequently occurs, leading to an additional parasitic resistance associated with the series resistance of the diode which further increases with mesa size of the device. A polynomial fit to the RTDs peak voltage was used to estimate the parasitic resistance (R_{par}).

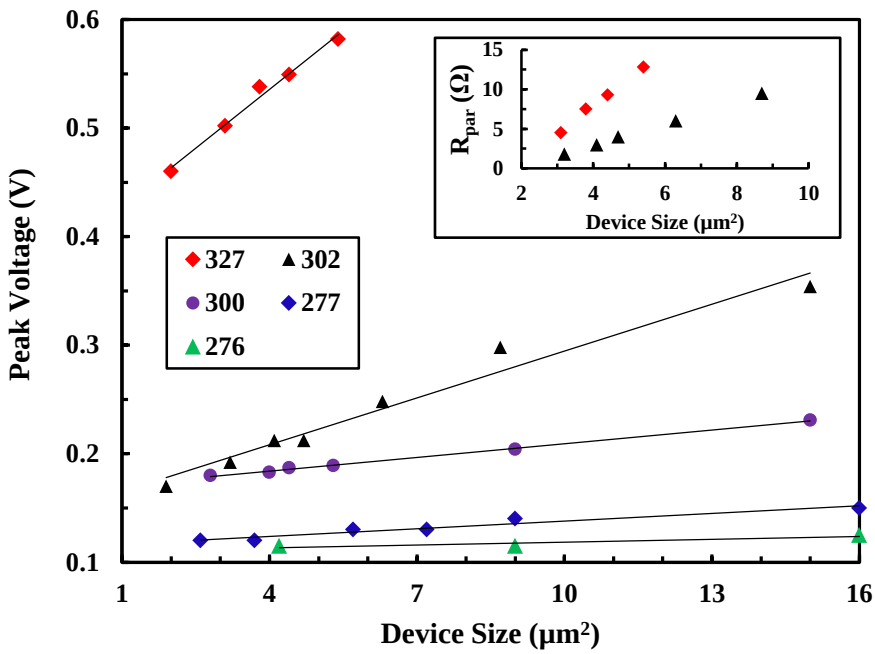


Figure 2.18: Peak voltage of the InGaAs/AlAs RTDs as a function of device sizes for different peak current density samples. The peak voltages were obtained from the measured I-V characteristics of the diodes. Inset: estimated parasitic resistance as a function of diode size for RTD samples XMBE#302 and 327 (all other samples were excluded from the graph due their very low associated R_{par}).

To accurately evaluate this associated resistance, the intrinsic series resistances of the devices were taken into account in the modeled IV curves. The simulation data shows that R_{par} is in the range of 1.4 to 3.6 Ω/μm^2 for samples XMBE#302 and 327 respectively as depicted in figure (2.18); all other diode samples had very low parasitic resistances depending on their current densities (i.e. < 0.5 Ω/μm^2). To support this

explanation, a 1µm width TLM (transmission line model) air-bridge structure using Pd/Ti/Pd/Au with thickness of 10/20/20/700 nm were fabricated. The measured data showed that an air-bridge passing a 100mA current has a very low voltage drop of 3.8mV/µm. This multilayer air-bridge can handle a current exceeding 100mA for a 30µm length. With this in mind, the self-heating resistance is clearly caused by the RTDs themselves. Therefore to minimize the variation in peak voltage and thus ensure very small additional resistance for high current density diodes, submicron devices are necessary.

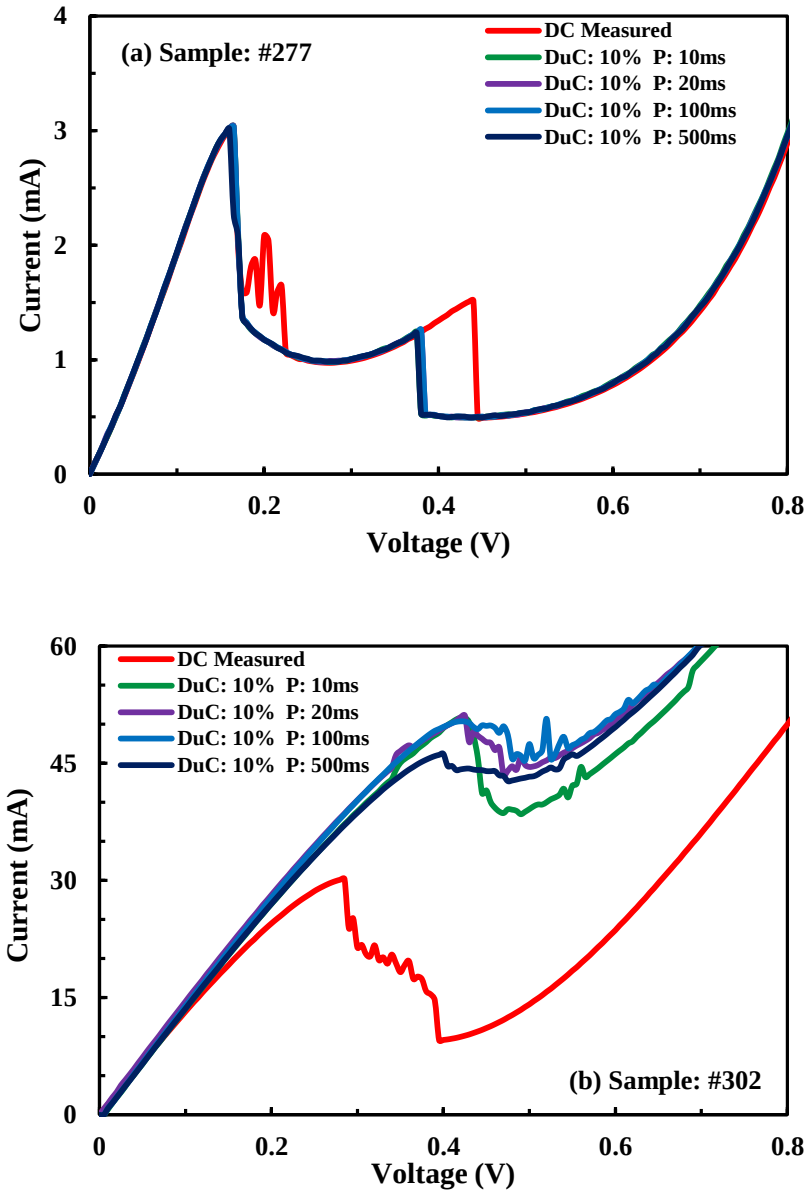


Figure 2.19: RTD I-V characteristic with various pulse widths of the applied DC voltage (a) Sample #277 with 11.4µm^2 mesa size, (b) Sample #302 with a mesa size of 8µm^2.

Further measurements using pulsed DC voltage bias (P) were carried out and from which the self-heating problem was clearly seen. The time period of the voltage was varied from 10 to 500ms with a duty cycle (DuC) of 10%. These measurements did not show any significant differences in the current-voltage characteristics of the low current density devices, for example RTD sample #277 as shown in figure (2.19, a). Note that the set-up oscillations present at DC are absent during pulse measurements. On the contrary, the high current density device sample #302 shows a marked trend in which higher current (less resistance) was obtained as depicted in figure (2.19, b). The enhancement in J_P was about 60% with a duty cycle and period time of 10% and 10ms respectively. However, it is noticeable that the PVCR decreases, particularly with long period times. Different duty cycles were also tried but did not reveal any further information.

Due to equipment limitations, large mesa area devices of sample #327 could not be measured. To the best of our knowledge, RTD structure designs, in which the self-heating issue effect is insignificant, has not been reported to date. However, the importance of minimizing V_P is paramount for relatively large device sizes as well as for low DC power dissipation in RTD integrated circuits. While further increase of the doping profile in the top cap layer can reduce the specific contact resistance and hence minimize voltage drop at the interface, minimizing the spreading resistance is far more important for lowering the peak voltage and yielding efficient high frequency performances. A graded InGaAs emitter layer is an alternative way exploited to reduce the bias voltage due to occurrence of the alignment between the resonant state in the well and conduction band edge of the emitter at a low bias voltage[131]. This is; however, at the expense of an increase in complexity of the growth process.

2.4.3 Integrated Nickel Chromium Stabilized Resistor

Resistors are widely used in MMIC designs for a number of purposes, such as feedback, biasing, matching circuits and terminations. Since this project is involved with design and characterizations of high frequency integrated circuits, biasing and stabilizing resistors are required for circuit implementations. There are mainly two kinds of thin-film resistors utilizing resistive metal alloy such as Tantalum Nitride (TaN) and Nickel Chromium (NiCr). NiCr facility is readily available at the University of Manchester and

so this material was used in this work. In-depth discussion related to the advantageous of NiCr resistors over other materials is presented in chapter 3. Generally speaking, the value of the resistance can be theoretically determined by altering the geometry of the thin film. A NiCr resistor is often realised in RTD oscillators to suppress the low frequency oscillation due to parasitic elements coming from the DC set-up cables. To do so, the resistor's value should be sufficiently low to reduce the DC power dissipation; however, this would degrade the extracted radio-frequency power of the circuit. This trade-off is indispensable and hence the influence of an integrated resistor on the characteristic of the resonant tunneling diodes was investigated.

A 25Ω NiCr shunt resistor (R_{sh}) with a 50Ω/□ sheet resistance (R_{sheet}) was sputtered into both sides of the coplanar waveguide (CPW) in parallel with the RTD sample #302 as shown in figure (2.20). A 200nm Si_3N_4 dielectric layer was fabricated underneath the NiCr material, so as to avoid shorting the passive device's epilayer with interconnecting metal. It is apparent from the graph depicted in figure (2.21) that the negative conductance region almost vanishes for a 4μm^2 device size, meaning that a 25Ω resistor is an overestimate to suppress the low frequency parasitic oscillation. Thus, an optimized R_{sh} value was found to be consistent with theoretical analysis in the literature as R_{sh} is constrained by G_{RTD} (i.e. $R_{sh} < 1/|G_{RTD}|$) [8, 158].

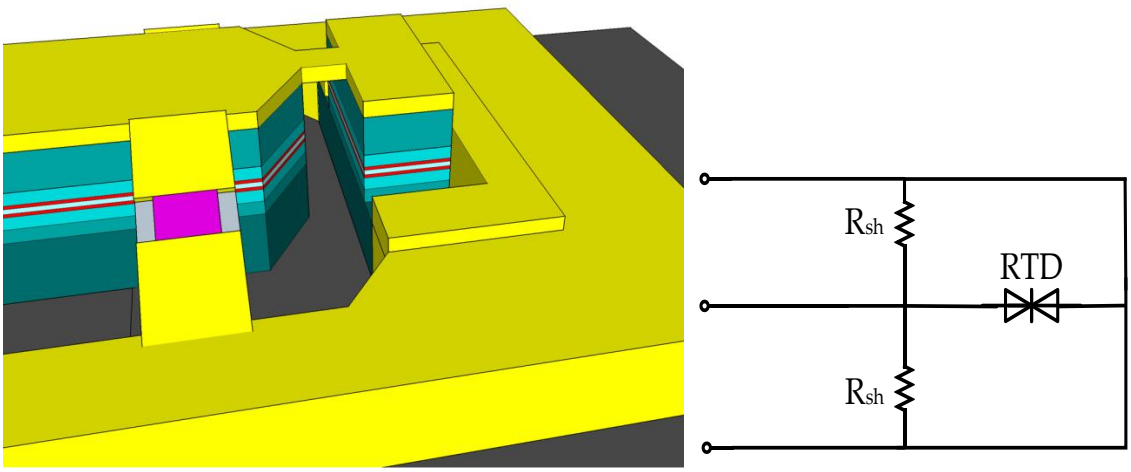


Figure 2.20: 3D schematic of the NiCr thin film resistor integrated on both sides of the coplanar waveguide and the resonant tunneling diode along with a circuit diagram represents the configuration of the fabricated structure.

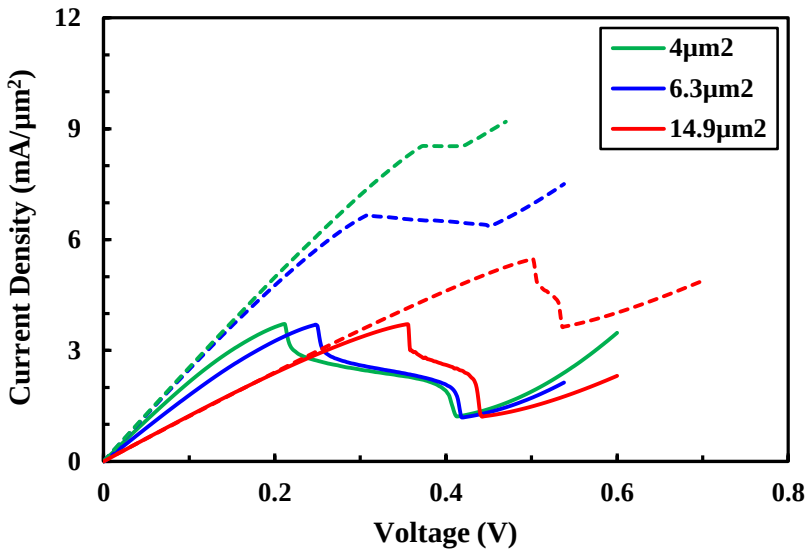


Figure 2.21: Current density of different RTD mesa sizes for sample #302 with and without a 25Ω NiCr shunt resistor plotted in dashed and solid lines respectively.

A large deviation in V_P is not only caused by self-heating problems of the RTDs but due largely to current dividing between the resistor and diode, leading to the peak current density to occur at higher V_P.

2.5 Transmission Line Model (TLM) Measurements

To facilitate the DC and RF measurements of the electronic devices, contacts made of metals are used to electrically connect the devices to the outside world. In such a case, the contact resistance between the metal and semiconductor must be reduced to provide high performance operation particularly at ultra-high frequencies. An ohmic contact is commonly exploited in electronic devices, offering very low contact resistance (a small voltage drop at the interface) by allowing a linear current voltage characteristic in both forward and reverse bias directions. To ensure introducing ohmic contacts at metal-semiconductor interface, heavily doped layers beneath the metal are utilized with a doping level in the range of > 10^{19} cm^{-3}. This avoids forming a Schottky barrier contact by providing a thin depletion region width where the field emission transport mechanism is dominant[159].

Assessment of the quality of the metal-semiconductor junction is still required for contact resistance evaluation. With this in mind, the transmission line model was previously proposed by Berger[160] and a schematic drawing for the TLM structure is shown in figure (2.22). This structure is composed of a series of metal contact pads deposited on

the highly doped InGaAs cap layer. In this work, the dimensions of each pad were chosen to be 50µm×100µm and the TLM test structures were fabricated for both top and bottom contacts. These pads are separated by a distance d_1, which is predefined in the mask design with 5µm and consistently increased up to reaching 40µm separation distance. In fact, the governing current passes out and into the following pad occur within a shorter pad's length called the effective transfer length (L_T).

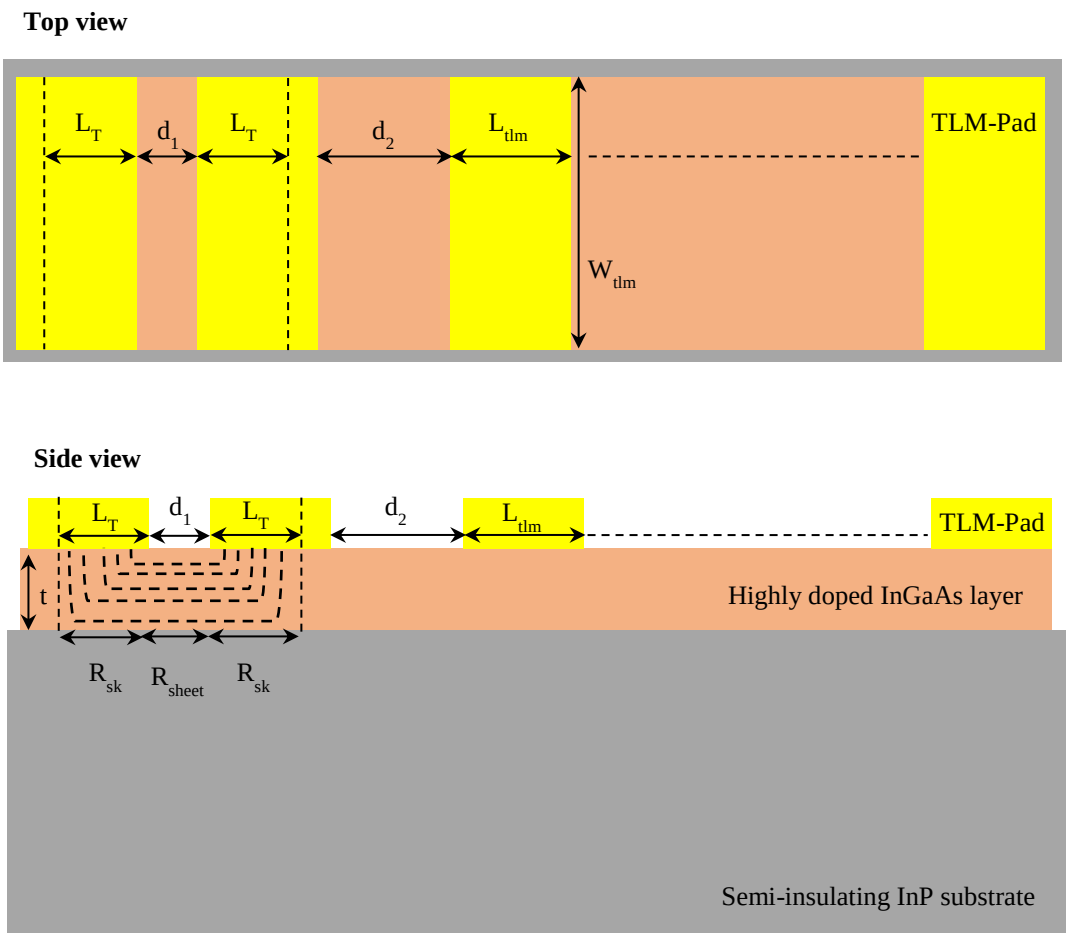


Figure 2.22: A generic schematic for top and side views of the transmission line model structure used in this work. Note that the drawing is not to scale.

From figure (2.22), two types of sheet resistance are involved in the TLM structure; the sheet resistance under the effective contact area of the metal pad (R_{sk}) and the one between two adjacent pads denoted as R_{sheet}. From this explanation, the total resistance between two neighbouring TLM pads can be express as[161]:

$$R_T = 2R_{sk}\frac{L_T}{W_{tlm}} + R_{sheet}\frac{d_1}{W_{tlm}} \tag{2.9}$$

All the symbols above are indicated in figure (2.22) and both of the sheet resistances can be given by ρ/t (in Ω/□), where ρ (in Ω.m) is predominantly related to the resistivity of the InGaAs cap layer. For the sake of simplicity, equation (2.9) is rearranged to become[161]:

$$R_T = 2R_{cont} + R_{sheet}\frac{d_1}{W_{tlm}} \tag{2.10}$$

R_{cont} being the contact resistance of the pads and is evaluated under the assumption of a constant sheet resistance. Accordingly, equation (2.10) can be plotted where the y-axis represents the total resistance as a function of the separation distance between the metal pads. To maximize the accuracy of the measurements, 4-point probe technique[162, 163] was used to test the fabricated TLM structure. Further discussion regarding the extraction procedure of the contact and sheet resistances and the effective transfer length from the measured data is stated in[161]. The most important parameter is the specific contact resistance of the structure, which is given by[161]:

$$\rho_c = R_{cont}L_T W_{tlm}[sinh(\frac{L_{tlm}}{L_T})\Big/\cosh(\frac{L_{tlm}}{L_T})] \tag{2.11}$$

Since this mathematical expression $sinh(\frac{L_{tlm}}{L_T})/cosh(\frac{L_{tlm}}{L_T})$ is equal to 1, the specific contact resistance is formulated by $\rho_c = R_{cont}L_T W_{tlm}$. To measure the uniformity of the contact resistance across the sample, many TLM structures were fabricated employing the non-alloyed ohmic contact scheme of Pd/Ti/Pd/Au for both upper anode and lower cathode electrodes. In spite of the fact that molybdenum-based contacts to n-type InGaAs give a low ρ_c of (1.1±0.9) Ω.μm^2 as reported by Baraskar[164, 165], transmission line model measurements for Pd/Ti/Pd/Au scheme used in this work showed an equivalent ρ_c value of approximately 1.3Ω.μm^2, essentially comparable.

As example several TLM measurements for the bottom contact of the RTD sample XMBE#277 are shown in figure (2.23). The experimental results which overlap each other exhibit a linear characteristic, emphasizing that the metal-semiconductor junction is indeed an ohmic contact. The slope of the line is related to the sheet resistance divided by the width of the metal pad (W_{tlm}), from which R_{sheet} was found to be 5.4Ω/□.

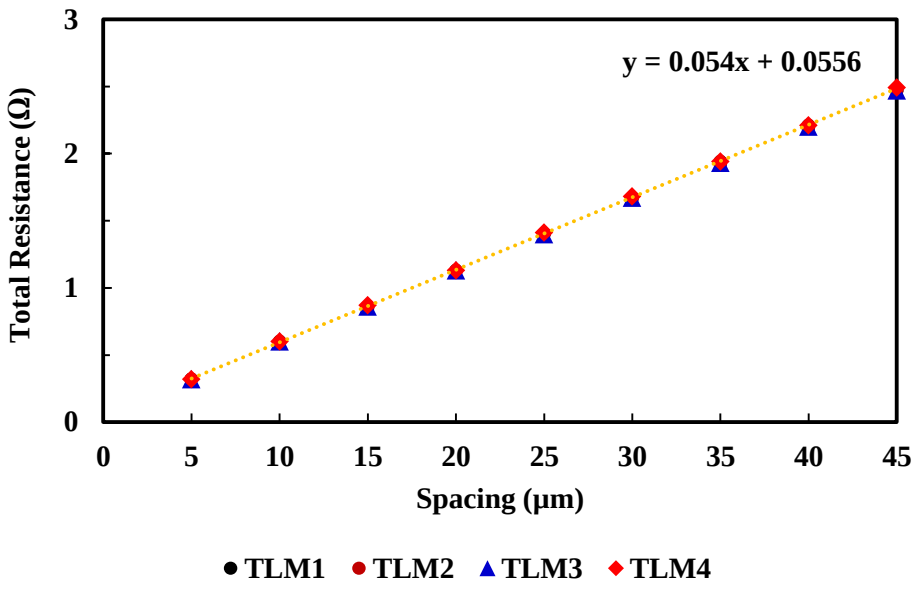


Figure 2.23: TLM measurements for the bottom contact of the RTD sample XMBE#277.

2.6 RF Characteristics of the DBQW Resonant Tunnelling Diodes

Though the DC characteristics of the resonant tunneling diodes are paramount in the assessment of the devices' suitability for high frequency operation, radio frequency characteristics are far more significant for tailoring to the various applications. This is due to the fact that the equivalent circuit components of the tunneling devices are typically frequency dependent parameters, resulting in reduction in the switching speed and predicted RF output power of the RTD oscillators. Therefore, this section is dedicated to analysing and discussing the RF characteristics of RTD samples XMBE#276, #277, #300, #302 and #327. The analysis is mainly constrained to the description procedure of the equivalent circuit extraction and capacitance-voltage characteristics of the devices. Furthermore, the estimation of transport time in the double barrier quantum well RTDs and relevant topics are presented here.

2.6.1 Series Resistance Evaluation

The series resistance of the resonant tunneling diode, R_s is a composite of three elements: ohmic contact resistance, resistance due to epi-layer ($R_{epi-layers}$) contacts and spreading resistance (R_{spr}) introduced by the current flowing through the bottom ohmic layer in a horizontal path. The top contact resistance is extracted from the transmission line model measurement for the devices using (ρ_c/RTD_{Area}). The bottom contact of all RTDs was defined with a size of 10×20μm^2, providing very small contact resistance and so was

neglected. $R_{epi-layers}$ was then simply calculated from $R = \rho l / RTD_{Area}$, where ρ, l and RTD_{Area} are the resistivity, material thickness and cross-sectional area of the diode respectively. Additionally, the spreading resistance is approximated as[8]:

$$R_{spr} = \frac{1}{\pi \sigma d_{th}} ln\left(\frac{a}{a_{mesa}}\right) \tag{2.12}$$

Where σ is the conductivity of the bottom ohmic layer, $a = a_{mesa} + D_{spr}$ and d_{th}, a_{mesa} and D_{spr} are the length and thickness indicated in figure (2.24). From this, the calculated series resistance of the RTD can be simply obtained from:

$$R_s = \frac{\rho_c}{RTD_{Area}} + R_{epi-layers} + R_{spr} \tag{2.13}$$

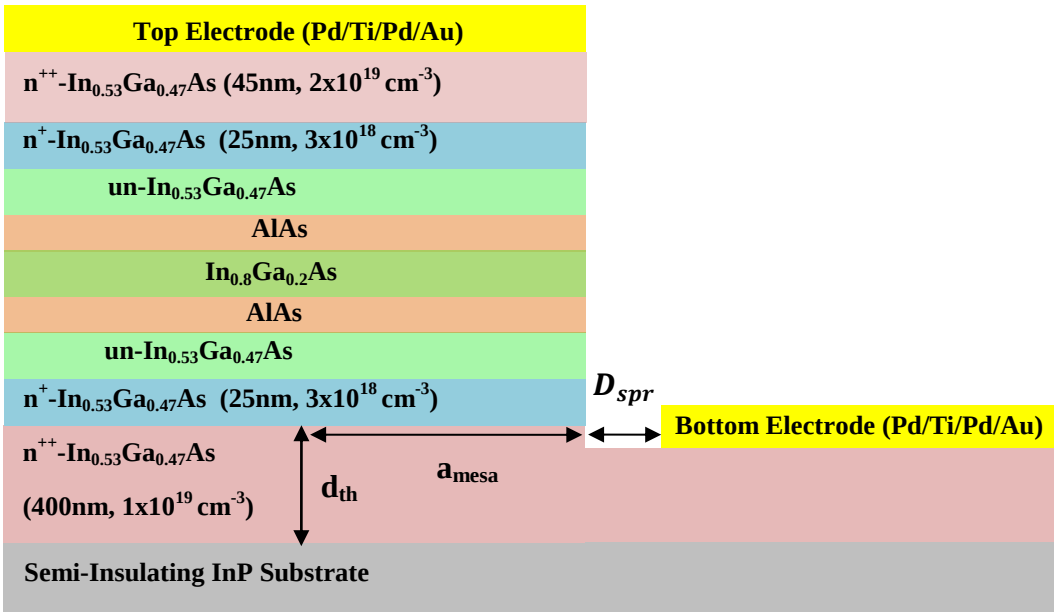


Figure 2.24: Cross section of an RTD showing the epi-layers and contacts on semi-insulating InP substrate investigated in this work.

In this work, D_{spr} was defined to be 2µm. For an RTD with a mesa size of 2×2µm^2 and with a corresponding structure depicted in figure (2.24), the calculated R_{spr} and $R_{epi-layers}$ were found to be 1.2Ω and 0.15Ω respectively. The extracted top contact resistance was 0.33Ω and this yields a series resistance of ~1.7Ω. A comparable value was obtained from the S-parameter measured data as will be discussed in detail in the following section. Since $R_{epi-layers}$ value is often trivial, the diodes are largely

degraded by their top contact and spreading resistances. To mitigate the contact resistance effect, heavily doping the ohmic layers along with high electron mobility properties of the material used is preferred. Furthermore, D_{spr} parameter must be as small as possible to ensure low device spreading resistance; hence high-performance device in the *mm*-wave/THz frequency bands.

2.6.2 C-V Extraction and Analytical Considerations

To accurately estimate the cut-off frequency of the resonant tunneling diodes, extraction of the values of the intrinsic equivalent circuit components is imperative. To this end, the RTD samples were fabricated into one port 50Ω characteristic impedance with GSG (ground signal ground) coplanar waveguide layouts. However, the ultimate layout circuits of the RTDs are mostly realized without CPWs as those supplementary structures are not needed in the final circuit. De-embedding techniques are therefore used to remove the parasitic elements associated with the additional transmission lines, such as CPWs, microstrip and coplanar strip lines (CPS)[166, 167]. Open, short and actual CPWs were fabricated with standard 50µm signal line width and 35µm separation distance as shown in figure (2.25).

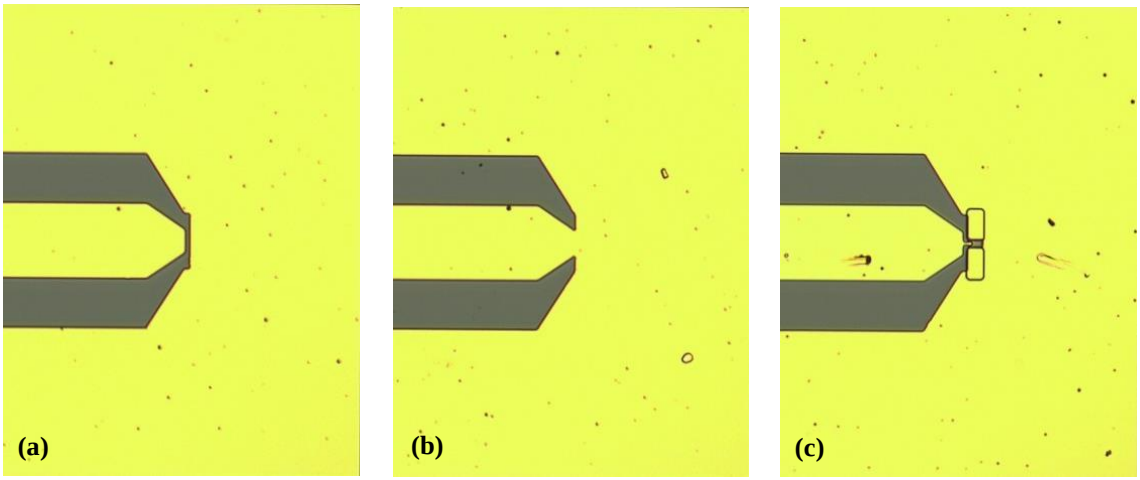


Figure 2.25: Microscope images of: (a) open CPW (b) short CPW (c) actual diode in the CPW configuration (Note: the images are not scalable).

In this project, the S-parameter measurements were performed on-wafer using a Vector Network Analyzer (VNA, Anritsu 37369A) up to 40GHz. The measuring equipment was first calibrated, contributing to eliminating the impact of the GSG probe. It is noteworthy mentioning that due to self-oscillation issues in the NDR region, care was taken to

produce stable scattering parameters data, through attenuating the input RF power to about -30 dBm[168]. The well-known equivalent circuit of the open and short modes is represented by a capacitor and an inductor respectively and their values strongly rely on the CPW dimensions and length as depicted in figure (2.26).

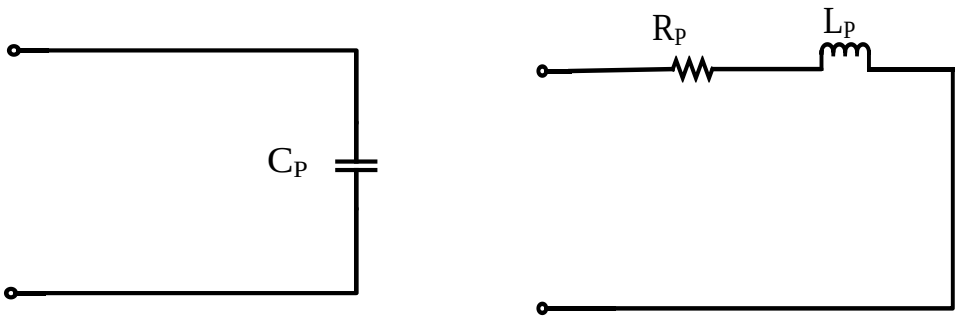


Figure 2.26: Equivalent circuit of: (a) open CPW (left hand side) (b) short CPW (right hand side).

The series resistance of the short mode is negligibly small and so it was excluded from the equivalent circuit elements. To carefully extract the pad capacitance(C_P), pad inductance (L_P) and intrinsic capacitance of the diode(C_{RTD}), two steps of de-embedding technique was utilized here[166]. From the measured scattering parameters, C_P and L_P of the open and short configurations can be given by:

$$C_P = \frac{Im(Y_{11_{Open}})}{\omega} \tag{2.14}$$

$$L_P = \frac{1}{\omega\left(Im\left(Y_{11_{Open}} - Y_{11_{Short}}\right)\right)} \tag{2.15}$$

Where Y is the Y-parameter computed from the measured data of S-parameter and ω is the angular frequency. The capacitance of the devices is expressed as:

$$C_{RTD} = \left[\left(\frac{1}{\omega}\right)\frac{1}{\dfrac{1}{Im\left(Y_{11_{total}} - Y_{11_{Open}}\right)} + \dfrac{1}{Im\left(Y_{11_{Open}} - Y_{11_{Short}}\right)}}\right] \tag{2.16}$$

From equation (2.14) and (2.15), C_P and L_P were found to be 23fF and 43pH respectively. Figure (2.27) shows good agreement between the equivalent circuit model

of the open and short structures built in Keysight-ADS and the measured data, validating the approach used in this work. Since the capacitance and inductance of the pads do not change with the DC voltage applied, the measurement was carried out at zero-bias voltage and -30dBm RF input power.

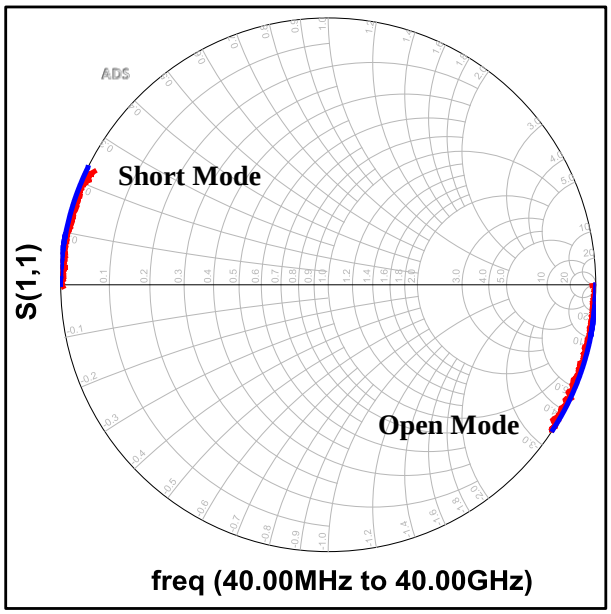


Figure 2.27: Equivalent circuit model and measured data of open and short CPW configurations (red and blue lines are for the measured and simulated data respectively).

The measured result indicates that the series resistance of the short mode is very small because the reflection coefficient response is on the circumference of the Smith chart. In the literature, equivalent circuit of the double barrier RTDs has been widely studied in various ways in terms of parameter extraction, for example Spice model[169, 170] and S-parameter fitting with circuit parameters[171, 172]. In fact, continuous scaling of the lateral dimensions of the devices to further extend their high frequency operation would undoubtedly minimize the size of the equivalent circuit parameters. This in turns makes the de-embedding method more complicated due to the existence of several parasitic elements. This is problematic for >100GHz frequency measurements in which the effects of the fringing capacitances between the air-bridge finger and InGaAs bottom ohmic layer as well as between the bridge and CPW are not trivial[173]. However, up to 40GHz a simple equivalent circuit model and straightforward extraction approach are adequate especially with relatively large emitter device sizes (i.e. 4μm^2). The well-known equivalent circuit parameter of the resonant tunneling diodes involving the pad elements is depicted in figure (2.28).

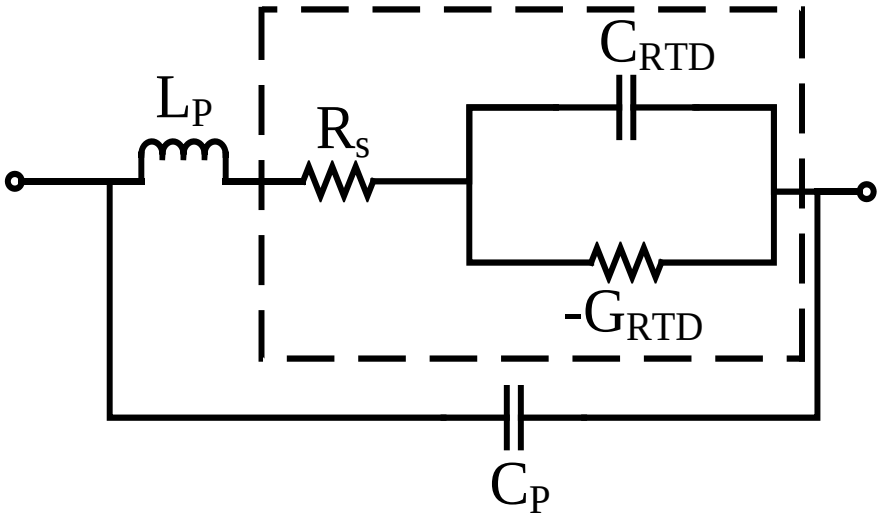


Figure 2.28: Typical equivalent circuit of the RTDs including the embedded parasitic elements and the intrinsic device equivalent circuit (dash lines).

For the RTDs, C_{RTD} includes both the depletion region (C_{dep}) and quantum capacitances (C_Q) as theoretically given by $C_{RTD} = C_{dep} + C_Q$[8]. The depletion region capacitance (as a parallel plate) can be estimated using $C_{dep} = \varepsilon_o \varepsilon_r RTD_{Area}/d$, where ε_o, ε_r and d are the free space permittivity, the relative dielectric constant and thickness of the double barriers quantum well region including emitter and collector spacers respectively[174]. An increase in the negative charge in the accumulation region and quantum well, which counter balances the positive charge in the depletion region, is the main reason behind introducing such an associated quantum capacitance[95, 175]. Figure (2.29) shows an example regarding the equivalent circuit model validated through a fitting approach with the experimental reflection coefficient data up to 40GHz for the RTD sample XMBE#277 with a mesa size of 2μm^2. The measured and simulated results are in very good agreement.

R_s was first calculated and then used to fit with the measured data. Additionally, the derived $R_s + R_{RTD}$ (R_{RTD} is the junction resistance of the RTDs in the positive differential region (PDR) calculated from $\partial V/\partial I$ of the measured I-V characteristic, is well matched to the extracted values from the S_{11} data. However, there are some drawbacks correlated with the accuracy of the simple equivalent circuit of the tunnelling devices. Two terminal devices operating in the terahertz regime have been experimentally demonstrated to have frequency dependent series resistances[176].

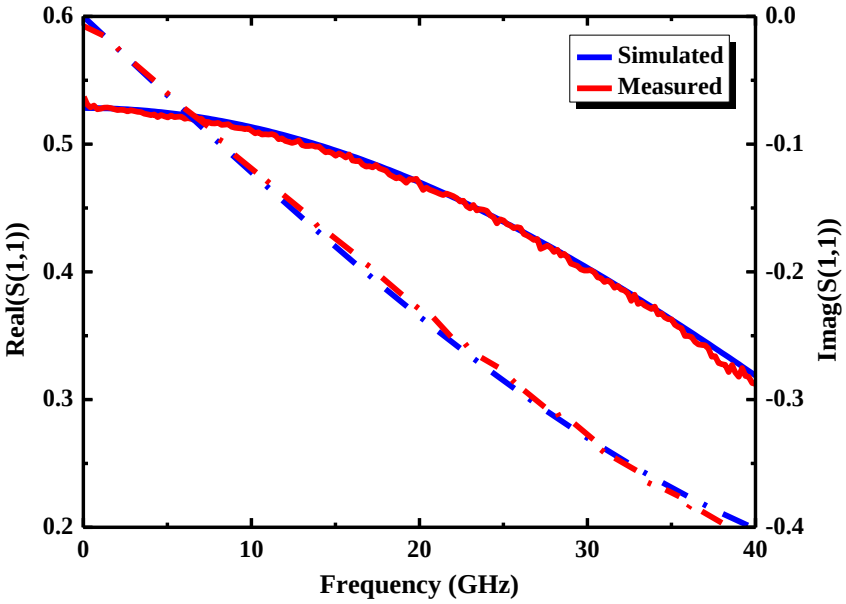


Figure 2.29: Real and imaginary parts of the equivalent circuit and S-parameters measurement of the RTD sample #277 with a mesa size of 2μm^2 (sold and dash lines are the real and imaginary parts of the S_{11} respectively). The diode was biased at the positive differential resistance.

This dependency was attributed to two major reasons; firstly, the electromagnetic (EM) field impacts which interacts with the diode itself and the surrounding additional pads. Therefore, previous reported work claimed that there is a difficulty to fully understand the geometry-dependent EM field with a conventional series resistance model[177]. However, to analytically extract the *mm*-wave/THz diode's equivalent circuit model including losses caused by the EM field interaction, numerical methods are necessary, which is out of the scope of this thesis. Thinning the structure buffer layer has been suggested to be one of the possible ways to minimize field-coupling issue[173].

The additional downside is that the spreading resistance of the device increases with frequency due to a decrease in the bottom ohmic conductivity as the frequency gets higher[178]. An effective approach used to remedy this is to further minimize the distance between the ohmic InGaAs layer and the bottom electrode to submicron scale. As conventional i-line photolithography technology is restricted to ~1μm resolution, optimizing this key distance can be achieved through exploiting a trilayer soft reflow technique as reported previously[145]. In practice, the impact of both aforementioned issues is insignificant for parameters extraction below 100GHz measurements, supporting the procedure of the equivalent circuit parameters carried out in this work.

From the small signal equivalent circuit of the RTD, the theoretical maximum oscillation frequency has been derived by Brown *et al*[124]. As the quantum inductance does not have a significant effect on the upper operating frequency limit, the RTD input impedance, $Z_{in(RTD)}$ is obtained from the circuit shown in figure (2.28) and given by:

$$Z_{in(RTD)} = R_s + \frac{G_{RTD}}{G_{RTD}^2 + \omega^2 C_{RTD}^2} - j\frac{\omega C_{RTD}}{G_{RTD}^2 + \omega^2 C_{RTD}^2} \tag{2.17}$$

The upper operating frequency limit can be theoretically found by setting the real part of $Z_{in(RTD)}$ to zero which means the second term of the real part can compensate the series resistance of the circuit[179].

$$f_{max} = \frac{|G_{RTD}|}{2\pi C_{RTD}}\sqrt{\frac{1}{R_s|G_{RTD}|} - 1} \tag{2.18}$$

It might be necessary to highlight that f_{max} is the frequency at which the net negative differential resistance of the RTD becomes zero, resulting in the real part of the input resistance turning into a positive value. This basically results in the RTD no longer working as an active device[26, 93]. From equation (2.18), minimizing the passive elements including R_s and other parasitic components is of paramount importance in ensuring an efficient operation in the *mm*-wave/THz regions. Due to the 5 nm spacer thicknesses for sample #300, a large value of C_{RTD} was obtained. For both, the thin barrier RTD sample #302 and the 3.5nm well thickness device #327, there is a decrease of their respective capacitances, leading to a significantly increase in f_{max} exceeding 0.8 and 1.6THz respectively as illustrated in Table (2.7). Note that all RF parameters tabulated in Table (2.7) are calculated for 4μm^2 device areas and in the middle of the NDR region. This is an important consideration for manufacturing and commercial applications and a key advantage of RTDs for achieving such high f_{max} values utilizing a relatively large device size compared with other technologies (i.e. HEMTs and HBTs), for instance where extremely small, nanometer scale gate lengths are required for HEMTs and thin base and collector contacts for HBTs.

TABLE 2.7: RF CHARACTERISTICS OF DIFFERENT RTD STRUCTURES FOR FORWARD BIAS DIRECTION.

RTD SAMPLE	DESIGN PARAMETERS			RF CHARACTERISTICS		
	t_s(nm)	t_b (nm)	t_w (nm)	Rs (Ω)	C_{RTD} (fF)	f_{max} (THz)
276	20	1.6	4.5	2.2	30	0.13
277	20	1.3	4.5	2.2	30	0.22
300	5	1.2	4.5	1.6	36	0.48
302	5	1.1	4.5	2	33	0.86
327	5	1.1	3.5	1.6	30	1.64

It has amply demonstrated that the intrinsic capacitance of the double barrier RTDs is a voltage dependent parameter[68, 180], therefore capacitance-voltage characteristic of such tunneling devices needs to be prudently extracted. From the measured reflection coefficient, the capacitance of the RTD sample XMBE#277 were obtained and plotted as a function of voltage bias as depicted in figure (2.30). The experimental data shows that two maxima value of C_{RTD} which can be noticed at zero voltage bias and the NDR region. A similar trend has been previously reported[68, 168]. The first maximum is caused by the depletion region capacitance, which gets smaller with higher external applied voltage due to broadening in the width of the depletion region. This is why, C_{RTD} decreases up to pre-peak voltage before starting to increase owing to the extra quantum capacitance. This associated capacitance comes from the charge pile-up in the quasi-bound states located in the triangular–well which is formed just before the barrier from the emitter side.

Due to the high peak voltage in reverse bias direction, the depletion region capacitance further decreases in comparison with the one obtained in the forward bias. As the resonant tunneling diodes are predominantly biased in the NDR region feature, reducing the impact of C_Q is indispensable for high switching speed well into ultrahigh frequencies. A graded spacer layer would effectively reduce the amount of accumulated charge in the quasi-bound state. This would also promote the quantum-based resonant

phenomena to occur at a low bias voltage as demonstrated in[131]. Moreover, the measured input impedance of the RTDs, $Z_{in(RTD)}$should exhibit a negative value in the NDR region. Figure (2.31) shows the real part of $Z_{in(RTD)}$ for sample #277 with a mesa size of 4μm^2 biased at various voltages.

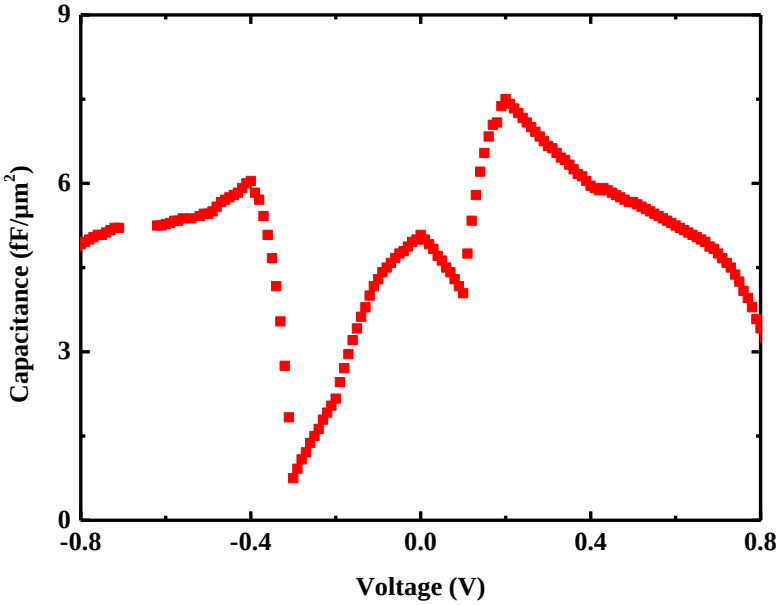


Figure 2.30: C-V characteristic of the RTD sample XMBE#277, the capacitance was evaluated at 40GHz frequency measurement.

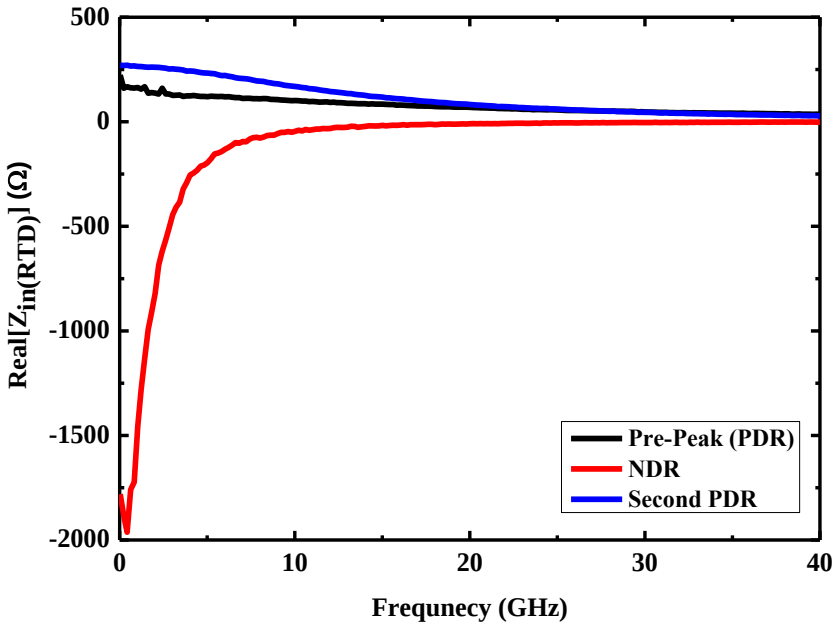


Figure 2.31: Real part of the measured input impedance of the RTD sample XMBE#277 with a mesa size of 4μm^2 biased at different applied voltages.

As expected, the diode gives positive resistance behaviour at pre-peak and second PDR regions. However, the finding reveals that the negative resistance vanishes at low frequencies reaching 40GHz. The contradiction between the estimated operating frequency of the device (>200GHz) and the available negative resistance is largely attributed to the self- oscillation at low frequencies (2-3GHz).

2.6.3 Intrinsic Capacitance of High J_P Tunneling Devices

High current density tunneling devices normally exceeding 5mA/µm^2 and this is among the most appealing feature required for *mm*-wave/THz regime operations. Since the characterization of an electronic device must be the first step towards integrated circuits implementation, this study has involved various RTD structures in terms of their equivalent circuit parameters extraction. Whilst performing the reflection coefficient measurements of the RTDs, the experimental data provided particular unexpected outcomes. To help in better understanding these, comparison and analysis consideration among the measured S_{11} were carried out and can be translated into several steps. Figure (2.32) shows the S-parameter data with different applied voltages plotted on a Smith chart for the RTD sample #277 with a mesa size of 1×2µm^2.

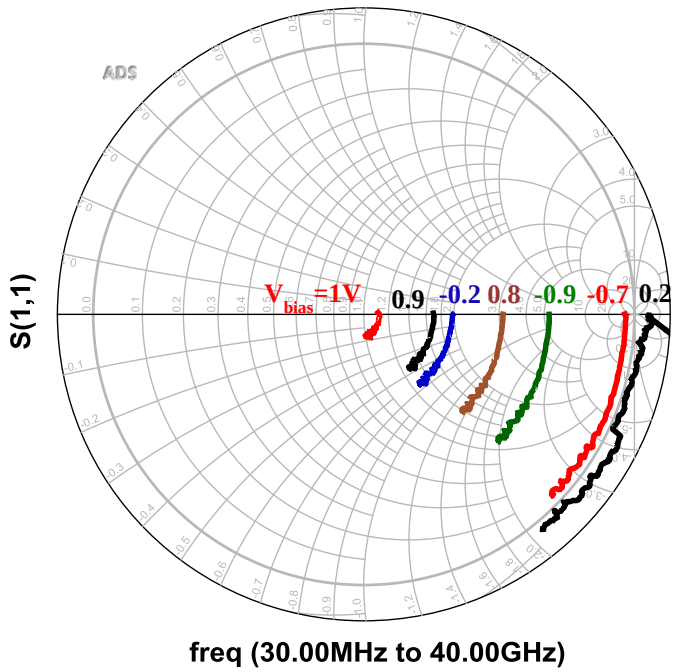


Figure 2.32: Measured S-parameter response at different voltage bias for the RTD sample #277 with a mesa size of 1×2µm^2. Each applied voltage is shown in the figure with corresponding data.

The results clearly indicate that the diode exhibits a capacitive behaviour when it is biased in the PDR or/and beyond the NDR region, as expected. Outside unit circle measurement was also observed at 0.2V external voltage bias due to the impact of the negative differential resistance with junction resistance (R_{RTD}) of ~ -900Ω as shown in figure (2.33). Less capacitive effect at high applied voltage (≥0.9V) is obvious as a consequence of broadening in the depletion region width. As the series resistance of the RTD is small, R_{RTD} was calculated by taking the first derivative of the measured I-V characteristic of the device.

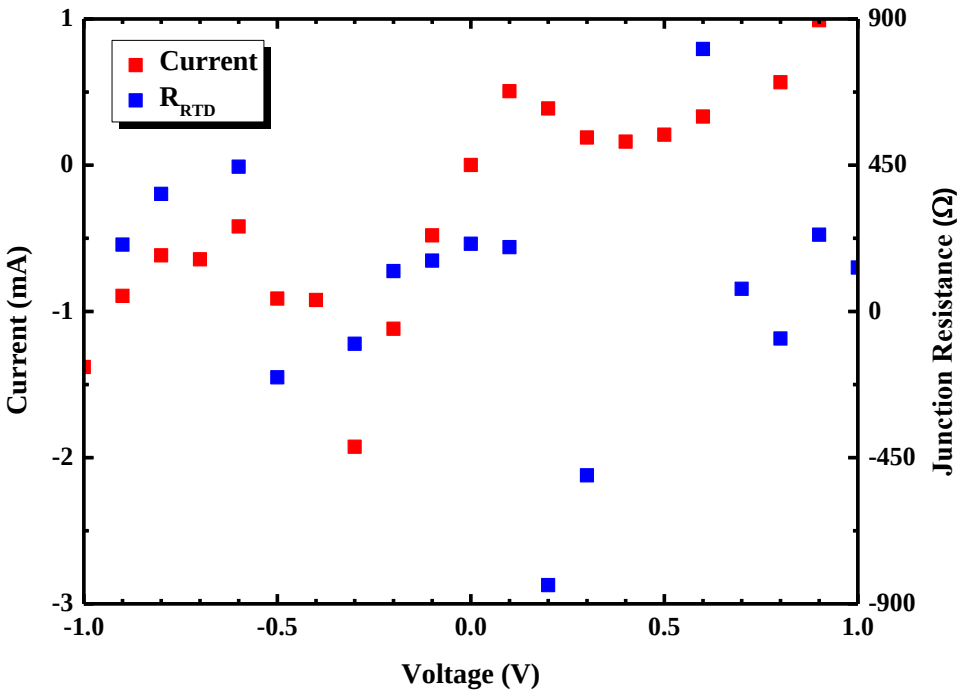


Figure 2.33: Discrete I-V characteristic and junction resistance of the RTD sample #277 with a mesa size of 1×2μm^2.

For the small device sizes, the S-parameter response of sample #277 are as predicted; however, large scale features showed a few unexpected results at first glance. Figure (2.34) illustrates the experimental data of the S_{11} and discrete I-V characteristics of sample #277 with an emitter size of 5×5μm^2. These can be prominently seen when the diode shows inductive and capacitive behaviours in both PDR and NDR regions. To fully clarify these findings, each measured point of the scattering parameter was compared with the corresponding device's current and junction resistance, R_{RTD} as depicted in figure (2.34).

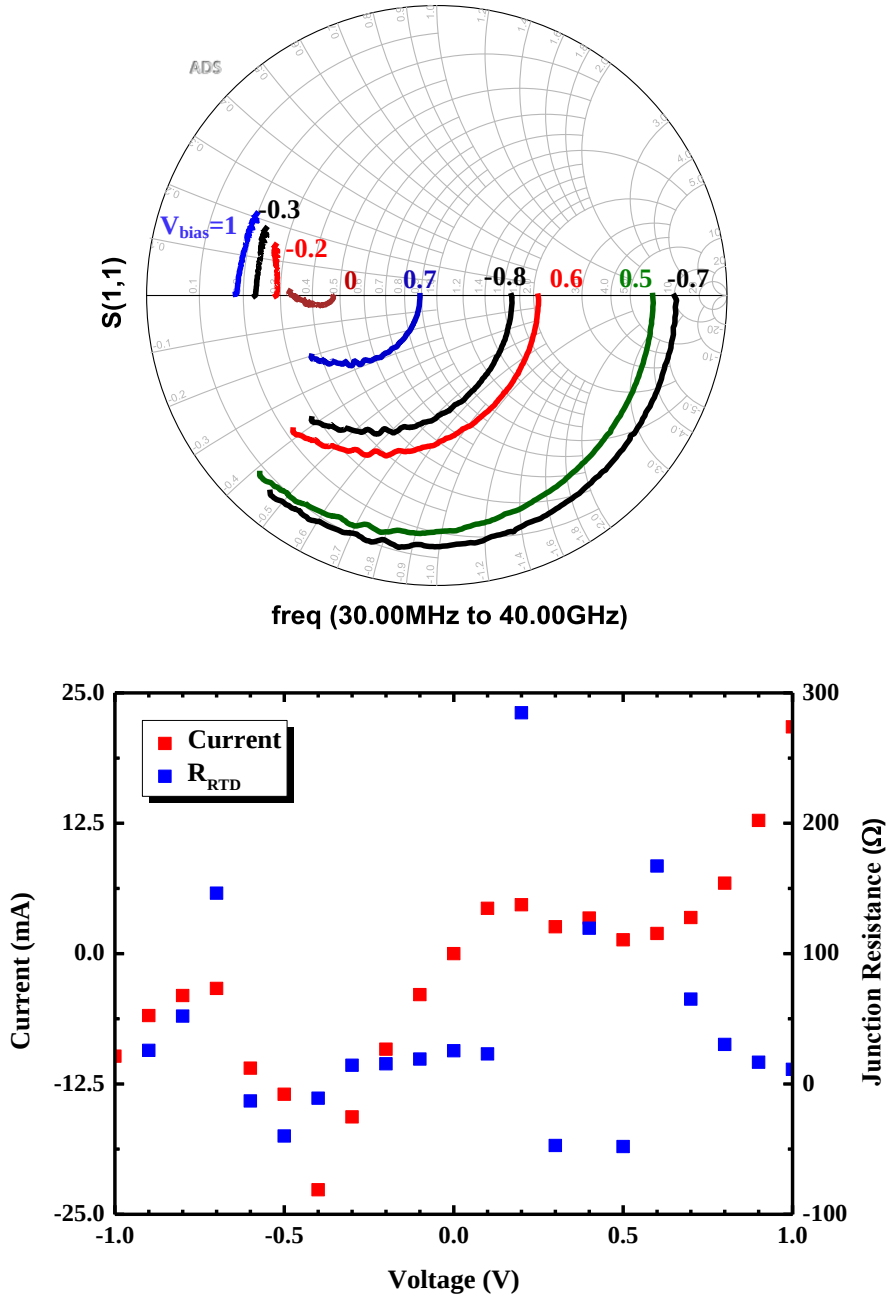


Figure 2.34: Measured S-parameter response at different voltage bias for the RTD sample #277 with a mesa size of 5×5μm^2 alongside its discrete I-V characteristics and junction resistance.

The discrete R_{RTD} ranges from 10 to a few tens of ohms at the positive differential resistance, emphasizing that the RTD acts as a short circuit at certain bias voltages (i.e. 1, -0.2 and -0.3V); hence the impact of the intrinsic capacitance disappears. A mathematical analysis can help to further highlight this undesirable outcome. Additionally, the device exhibits negative resistance values reaching -50Ω in the NDR region; nevertheless, they are insufficiently small to demonstrate a response which goes outside the unit circuit of the chart especially with the inherent self-oscillation problem. From the RTD equivalent

circuit presented in figure (2.28), the extrinsic input impedance of device including the active device and surrounding bond pads can be written as:

$$Z_{in(extrinsic)} = \frac{1}{j\omega C_P + [1/(j\omega L_P + R_s + \frac{1}{|G_{RTD}| + j\omega C_{RTD}})]} \tag{2.19}$$

For a relatively large device size, large negative or/and positive conductance (less resistive) is provided and so $G_{RTD} \gg \omega C_{RTD}$ at frequencies ≤40GHz, yielding $Z_{in(extrinsic)}$ to become:

$$Z_{in(extrinsic)} = \frac{1}{j\omega C_P + [1/(j\omega L_P + R_s + \frac{1}{|G_{RTD}|})]} \tag{2.20}$$

For the sake of simplicity, $R_{RTD} \simeq R_s + \frac{1}{|G_{RTD}|}$ so that equation (2.20) can be rearranged to be:

$$Z_{in(extrinsic)} \simeq \frac{R_{RTD}^2 + \omega^2 L_P^2}{R_{RTD} - j(\omega L_P - \omega^2 L_P^2 C_P - \omega R_{RTD}^2 C_P)} \tag{2.21}$$

Since this term $(-\omega^2 L_P^2 C_P - \omega R_{RTD}^2 C_P) \ll \omega L_P$, the latter formula can be rewritten as:

$$Z_{in(extrinsic)} \simeq \frac{R_{RTD}^3 + \omega^2 L_P^2 R_{RTD}}{R_{RTD}^2 + \omega^2 L_P^2} + j\frac{\omega L_P R_{RTD}^2 + \omega^3 L_P^3}{R_{RTD}^2 + \omega^2 L_P^2} \tag{2.22}$$

According to these particular conditions, equation (2.22) reveals that the extraction of the equivalent circuit parameters is independent of C_{RTD}. Therefore, the extrinsic input impedance of the device is dominated by inductance of the pad under the assumption of neglecting the small participation introduced by 23fF C_P in comparison with a 43pH L_P. This evidently is the reason behind the measured inductive behaviour of the S-parameter data. Such an issue would become rather worse for high current density RTDs despite their respective micrometre-scale mesa sizes. Figure (2.35) presents the measured reflection coefficient response for RTD samples #300 and #302 with a mesa size of size of 1×2μm^2. The current densities of these RTD samples are 1.1 and 3.7mA/μm^2. Unsurprisingly, the relatively small device sizes of the samples show an inductive behaviour in a few measured points, again attributed to their very low junction resistance.

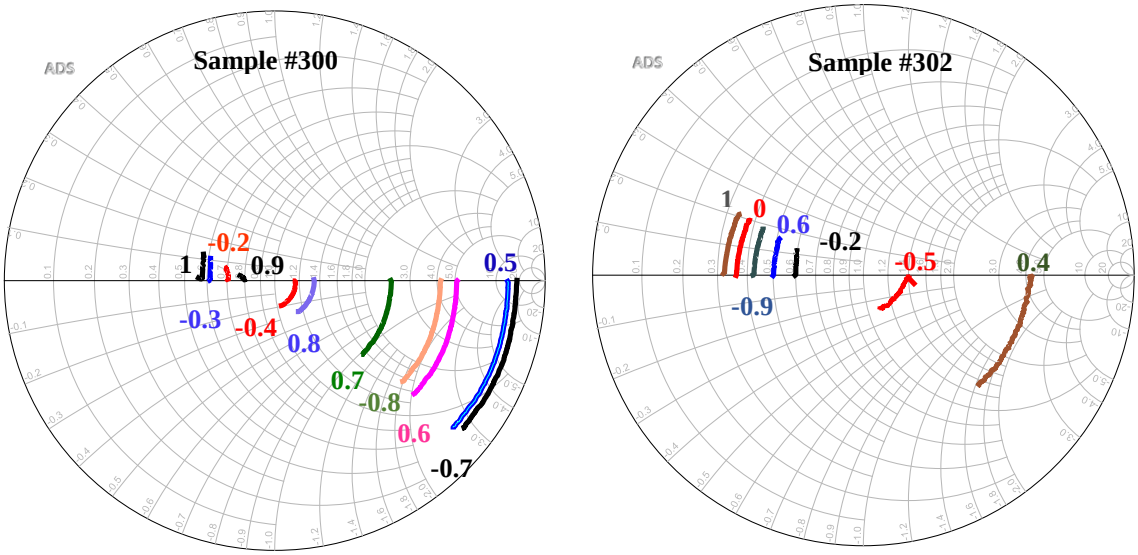


Figure 2.35: Measured S-parameter response at different voltage bias for the RTD samples #300 and #302 with a mesa size of 1×2μm^2.

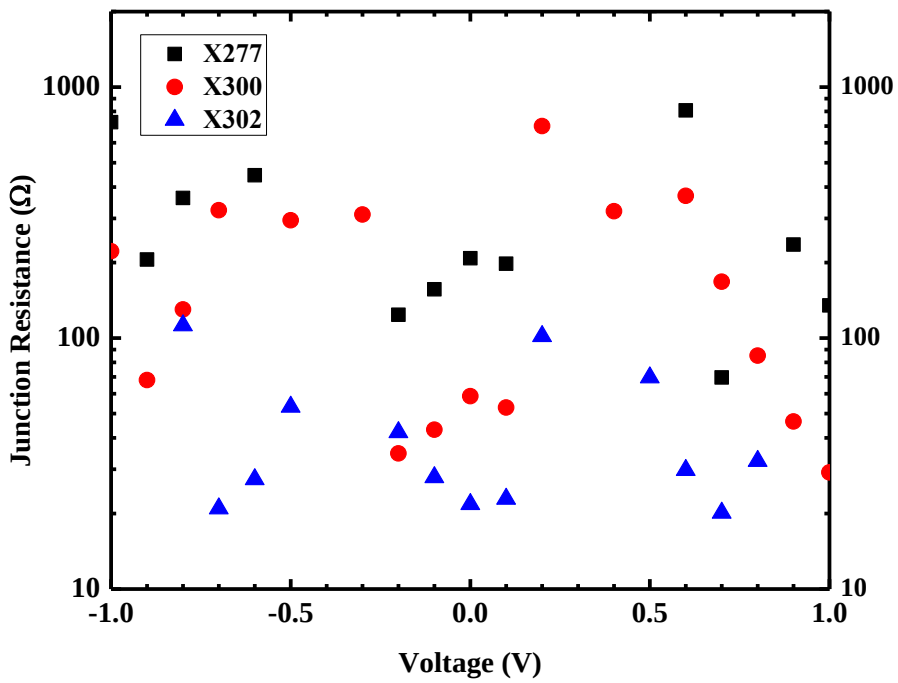


Figure 2.36: A semi log-scale of the discrete junction resistance of RTD samples #277, #300 and #302 with a mesa size of 1×2μm^2, showing a very low junction resistance of roughly 20-30Ω in the PDR for high current density devices.

Due to the high J_P of sample #302, the inductive response tends to be more robust and moves toward the short circuit point of the chart (i.e. zero normalized impedance) as shown in figure (2.35). Since the current density of the tunneling devices is exponentially barrier and quantum well thicknesses dependent, the junction resistance of the samples

shows a similar trend. RTD sample #302 has an R_{RTD} of roughly 20-30Ω in the PDR region and of course these values become even lower for larger device sizes as depicted in figure (2.36). All the aforementioned experimental findings imply that it is rather difficult to evaluate the intrinsic capacitance of high J_P RTDs. However, there are two fundamental ways that can be employed to estimate C_{RTD} as a function of dc applied voltages. Firstly, sub-micrometer feature sizes are required to ensure reasonable junction resistance values across the high current characteristic of the PDR region. This could contribute to a further reduction in the influence of high conductance feature on the extraction of the equivalent circuit (in other words, the condition $G_{RTD} \leq \omega C_{RTD}$ illustrated in equation (2.19) must be satisfied).

An alternative approach is based on the estimation of C_{RTD} at some measured points in which the device provides high R_{RTD} and a mathematical model can be then used to obtain the entire C-V characteristic. This model was demonstrated by S. Diebold *et al*[68], utilizing the Gaussian distribution function to smooth the second maxima of C_{RTD} occurring at the peak voltage due to the accumulated charge in the quasi-bound states. In this work, the second technique was employed; thereby C_{RTD} was extracted and tabulated in Table (2.7). Small device sizes of ≤2μm^2 were used, exploiting S-parameter fitting approach in the first and second PDR regions. Since the high current density RTDs sample #300, #302 and #327 have a spacer thickness of 50nm, the depletion region capacitance assumed to be similar at zero voltage bias. Nevertheless, submicron devices are still required to carefully evaluate the intrinsic capacitance of the RTDs.

2.6.4 Estimation of Transport Time and RF Power for DBQW RTDs

Assessments of the suitability of the RTD structures for use as terahertz emitter requires an estimation of carriers' transit time in both DBQW and collector depletion region. The quantum capacitance formula is given by $C_Q \simeq |G_{RTD}|\tau_{RTD}$, where τ_{RTD} is the transit time through the double barriers quantum well (τ_{dwell}) and collector depletion region (τ_{dep}) [175]. Under this consideration, the carrier transit time in a resonant tunneling diode is expressed as[8]:

$$\tau_{RTD} = \tau_{dwell} + \frac{\tau_{dep}}{2} \tag{2.23}$$

The key factor of $\frac{\tau_{dep}}{2}$ has been mathematically derived for collector depletion region transit time in the analysis of transistors[181]. It would be worthwhile highlighting that continuous downscaling of a high G_{RTD} RTD to < 1μm^2 can contribute to an increase in the quantum capacitance over the depletion region one. From the aforementioned explanation, C_Q and τ_{RTD}in an RTD for small signal analysis at low frequency (where $\omega\tau_{dwell},\ \omega\tau_{dep}/2 \ll 1$) can be approximately given by[182]:

$$C_Q \simeq \left(\tau_{dwell} + \frac{\tau_{dep}}{2}\right) G_{RTD} \tag{2.24}$$

The evaluation of the term $\tau_{dwell} + \tau_{dep}/2$ has been found from the measured data of the extracted intrinsic capacitance values of the RTDs. C_Q was first obtained as stated in[182] from which τ_{RTD} was then estimated as shown in Table (2.8). It is important to point out that a moderate spacer thickness is necessary as a compromise between an optimum transport time across the depletion region and the capacitance of the device. Regardless of limitation in high frequency operation caused by parasitic elements of the diodes, the intrinsic high frequency limit due to both tunneling and depletion region delay times is given by [7]:

$$f_{int-limit} = \frac{1}{4(\tau_{dwell} + \frac{\tau_{dep}}{2})} \tag{2.25}$$

From a first glance of the data in Table (2.8), RTD samples XMBE#302 and #327 should be suitable for relatively high output power oscillators as a result of their high current density and so further discussion in this section is mainly concentrated on these samples. Due to the dependency of the delay time in double barriers RTDs on a negative differential resistance, a relatively low frequency operation limit was obtained for samples #276 and 277. As expected, sample #327 has the highest $f_{int-limit}$ followed by sample #302 as a result of their thinner well and barriers. These particular RTDs are promising candidates for *mm*-wave/THz applications. Further reduction in the thickness of the quantum well would significantly increase $f_{int-limit}$.

TABLE 2.8: CALCULATED TRANSIT TIME AND INTRINSIC HIGH FREQUENCY LIMIT FOR THE RTD SAMPLES.

RTD SAMPLE	t_s (nm)	t_b (nm)	t_w (nm)	P_{max} (μW)	τ_{RTD} (fs)	$f_{int\text{-}limit}$ (THz)
276	20	1.6	4.5	18	1880	0.13
277	20	1.3	4.5	37	800	0.31
300	5	1.2	4.5	166	410	0.61
302	5	1.1	4.5	380	260	0.96
327	5	1.1	3.5	1200	92	2.7

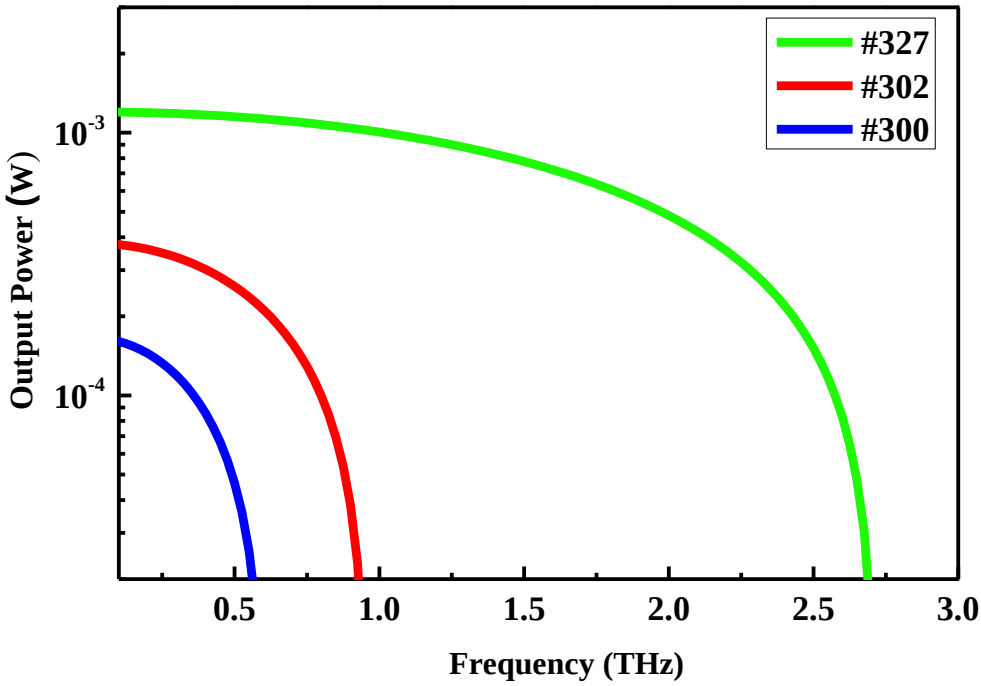


Figure 2.37: Calculated output power as a function of operating frequency for RTD samples #327, #302 and #300.

For an efficient THz RTD emitter, the difference between peak and valley voltages (ΔV) is a key driver in maximizing the RF output power. With this in mind, producing a peak resonance at lower bias voltage is also important for low dc power consumption. The maximum output power was calculated using $P_{max} = (3/16)\Delta I \Delta V$ [183], and was found to be 1.2mW for diode sample #327 for a device size of 4μm^2. However, in practice, the actual output power is degraded as a consequence of a decrease in G_{RTD} with frequency (i.e. long transit delay time), so the above formula becomes[184]:

$$P_{RF-actual} = \left(\frac{3}{16}\right) \Delta I \Delta V \cos \omega \tau_{RTD} \tag{2.26}$$

Accordingly, figure (2.37) shows the predicted output power as a function of frequency for devices #300, #302 and #327 with different barriers and well thicknesses. As depicted in Table (2.8), sample #327 can theoretically operate up to 2.7THz. This clearly emphasizes that high J_P RTDs with an adequately large value of PVCR have the potential for switching beyond 2THz.

2.7 Summary

This work presented systematic experimental study of InGaAs/AlAs RTDs designed to improve the diode characteristics involving five different device structures. A promising high peak to valley current ratio of 5.2 was obtained for a very low current density device (sample #276). A comparable PVCR value was achieved for sample #327 with a remarkable increase in J_P and G_{RTD} obtained through decreasing both well and barrier thicknesses. As expected, the measured results show a significant increase in the current density with thinner barriers and quantum well widths. This is, however, at the expense of an increase in the peak voltages for high peak current density devices. A 36mV/μm^2 voltage deviation was found for a diode sample #327 with a peak current density of 10.8 mA/μm^2, which was attributed to self-heating of the diodes and confirmed using pulsed dc voltage tests. More importantly, the promising PVCR values achieved with low J_P characteristics for the devices from samples #276 and #277 are very promising for radio frequency MMIC implementations with ultra-low DC power consumption.

The most prominent result is the very high G_{RTD} of 185mS/μm^2 obtained for RTD sample #327, which is the highest reported to date. An estimated high frequency operation limit of 2.7THz with a P_{max} of 1.2mW was deduced for the same device sample, opening the way to *mm*-wave/THz regime IC implementations. To demonstrate how the self-oscillation at low frequency can be eliminated, a 25Ω resistor was integrated in parallel with the diodes. The experimental findings suggest that the partially stabilizing resistor is limited by the absolute value of the negative differential resistance. The equivalent circuit of the diodes was validated using on-wafer S-parameter measurements up to 40 GHz. Furthermore, the mathematical analysis and measured results revealed that the extrinsic

input impedance of relatively large feature size RTDs (>4μm^2) is dominated by inductance of the pad, exhibiting an inductive response on the Smith chart and thus making the C-V extraction difficult. This issue become rather worse for high current density RTDs (sample #302 and #327 due to their R_{RTD} values being ≤20Ω in the PDR region) despite their respective micrometre-scale mesa sizes, emphasizing that sub-micron devices are actually necessary.

CHAPTER 3: MODELING AND CHARACTERIZATION OF PASSIVE ELEMENTS

3.1 Introduction

In earlier chapters, an overview of resonant tunneling diodes and their characteristics were discussed. As one of the major goals of this thesis is to realise RTD integrated circuits operating at high frequencies, as well as modeling and designs of optoelectronic integrated circuits for high data rate communication systems, passive components are certainly required. Furthermore, the values and high frequency behaviour of such elements have a significant impact on overall ICs performance. This chapter is, therefore, devoted to fully describe the design procedure, modeling and characterizations of the passive components including resistors, capacitors, spiral inductors and coplanar waveguides. In this project, the modules were built using the Momentum simulation tool embedded in Agilent ADS software.

3.2 MMIC Technology

The technology chosen to implement the RTD circuits in this project is the Monolithic Microwave Integrated Circuit (MMIC) technology. The term Monolithic comes from the Greek word meaning “as a single stone,” where all the circuit components, both passive and active, can be fabricated on the same material substrate. The indication from the term IC is that the semiconductor material does not only comprise active devices, for example RTDs and transistors, but it also includes passive elements with their interconnections to realise a whole circuit[185]. Due to their monolithic capability, MMICs have received a great deal of attention and are widely used in manufacturing of solid-state electronic circuits. The reason is largely due to their advantages compared with equivalent hybrid microwave integrated circuits (MIC), where packaged transistors and passives are mounted on alumina substrates.

The small dimension of the MMICs ranging from 1 to 10 mm^2, offers the facility of fabricating thousands of circuits on a single 4 inch wafer so that the reduction in the mass production cost can be further lowered[185]. Unlike hybrid MICs, monolithic integration

approach is compatible with many applications in which compact and light designs are actually needed, for instance mobile cell phones and portable computers[185]. Furthermore, minimizing the parasitic elements of the MMICs comes from the fact that there is no longer any requirement for bond wire connections, contributing to eliminating any undesirable performance and embedding the active devices within the printed circuit. This advantage of such a technology is highly beneficial in providing excellent performance in broadband applications. In addition, only a few photolithographic process steps are required in MMICs for circuit integration which are realised using the same mask plates. This further enables the reproducibility of MMICs; however, there is a drawback that has to be addressed from the outset. Checking the correct functionality of the circuits can only be carried out after the whole fabrication process is entirely completed. This tends to raise the manufacturing cost if errors in the mask designs propagate to the actual fabrication process. In fact, the low-cost of MMICs can only be ensured, if high numbers of chips are needed and the design produces a high-yielding circuit. Thus, an accurate electromagnetic model for all active and passive components together with accurate evaluation of all parasitics is imperative before starting the unit fabrication[186]; otherwise, the fabrication process must be repeated several times from scratch for proper circuit functionality.

3.3 ADS Momentum Simulator

ADS electromagnetic (EM) simulation is a model based on 2D component layout with the capability of providing a 3D perspective of radio frequency current flow in the transmission lines and far-field radiation patterns, so it is known as a 2.5D simulator. Furthermore, the EM simulation tool can this take into account the coupling impact of the neighbouring transmission lines. This translates into a more accurate module which can be straightforwardly extended to predict the circuit performance prior to actual fabrication and practical results[187]. In fact, the EM model has two main simulators; momentum RF and momentum microwave, the latter mode was used in this work. It is due to the fact that this mode utilizes full-wave Green's functions, which are frequency dependent and incorporate the losses in the ground plane of the prime elements caused by the high frequency operation. The setting of the momentum was set as follows. Since the transmission lines in the simulator are divided into small cells during the simulation process, the mesh was selected to be at the highest simulation frequency. This is to

ensure a sufficient mesh density of cells per wavelength, resulting in a better simulation performance. The only downside of too dense mesh is that the execution time of the simulation process increases. The electrical and physical parameters of the conductor, dielectric and lossy layers were defined in the simulator, such as dimensions, conductivity and relative permittivity. In fact, the relative permittivity (ε_r) is a frequency dependent complex parameter as given by:

$$\varepsilon_r(f) = \varepsilon_r'(f)(1 - j\,tan\,\delta(f)) \tag{3.1}$$

$\varepsilon_r'(f)$ is the real part of the $\varepsilon_r(f)$ and $\delta(f)$ is the angle between the real and imaginary parts. Note that the imaginary part represents the losses caused by the substrate. In ADS momentum, the built in Svensson/Djordjevic model can be chosen[187], so the frequency dependency of ε_r will be taken into account over the simulated frequency region. For coplanar waveguide configuration, a finite substrate thickness was employed, meaning that the model is analysed with no ground plane at the back of the structure. This eliminates the additional parasitics associated with the grounded coplanar structures (GCPW). A 625μm thickness of semi-insulating InP substrate with ε_r of 12.5 and as low as loss tangent ($tan\,\delta$) of ~0.002 was used in this simulation[188]. These parameters were defined at a low frequency of 1GHz and the variation in their values is basically based on Svensson/Djordjevic model embedded in the simulator.

3.4 Performance of the Passive Components

Passive components are extensively exploited for many purposes in electronic circuits, such as DC blocking, biasing, filtering and matching circuits. These components determine the power output, cut-off frequency, bandwidth and other fundamental characteristics of the system. Accordingly, their performance and reliability are paramount in the integrated circuits particularly in high-frequency operation. The values and performance of the passive elements are strongly dependent on the actual dimensions and fabrication process instead of design equations. This implies that the equivalent circuit models, in which the non-ideal nature is included, are required. It can help to avoid substantial errors in the design and make the simulation results more accurate and closer to the actual measured results. In this project, all the passive components were

individually fabricated and then the scattering parameter measurements were on-wafer performed up to 40GHz employing an Anritsu 37369A VNA. The verification of the equivalent circuits was then experimentally validated using a fitting approach with the S-parameter data.

3.4.1 MMIC Nickel Chromium Resistors

There are predominantly two different approaches to realise a resistor in MMICs. The first one can be fabricated using the active semiconductor layer under the MMIC surface, or by implanting known impurities into the semiconductor active layer. However, the issue accompanying this type of resistor is the high temperature coefficient of resistance (TCR), which is about 3000 ppm/°C[189]. This would cause nonlinear behaviour at high temperatures. The material used for realization of an integrated resistor should have high resistivity, low TCR and high handling current capability. As an alternative approach, a thin-film of resistive metal alloy is often utilized in circuits, for instance Tantalum Nitride (TaN) or Nickel Chromium (NiCr). Due to their rather low TCR compared with semiconductor active layer resistors, the resistive metals are preferred for use in MMIC applications[143, 189]. NiCr resistors are fairly easy to fabricate, their sheet resistance controlled by varying the geometrical size and they have a low TCR of 77 ppm/°C contributing to stable operations over a wide range of temperatures[190]. Nevertheless, active semiconductor layer resistors have a sheet resistance, R_{sheet} within a few hundred ohms per square, making them beneficial for high value resistors. A typically sheet resistance of thin film films ranging from 20 to 50 Ω/□ implies that such a resistor is feasible for relatively small values. At UoM, only the NiCr capability is readily available, so this alloyed material was used in this project.

The prime resistance value is theoretically determined by altering the dimensions of the thin film using $R_{NiCr} = \frac{\rho l}{tw} = R_{sheet}\frac{l}{w}$, where the ρ, *l*, *t* and *w* are the resistivity, material length, thickness and width of the resistive metal respectively. The equivalent circuit model of the resistor including prime and additional parasitic components is depicted in figure (3.1). The series inductance, L_s due to length of the NiCr is computed by the following empirical relationship[191].

$$L_s(pH) = \left[L_{R1} + \frac{L_{R2}}{w} - \frac{L_{R3}}{w^2}\right] l \tag{3.1}$$

The parallel capacitors, C_{sub1} and C_{sub2} are introduced because of capacitive interaction between the metal and ground plane and expressed as[191]:

$$C_{sub1,sub2}(fF) = 10^{-3}[C_{R1} + C_{R2}w]l \tag{3.2}$$

The parameters $L_{R1}, L_{R2}, L_{R3}, C_{R1}$ and C_{R2} can be manipulated to get simulation fit with measurement results. The parallel parasitic capacitance, C_P has a trivial impact on the model performance, and hence was neglected.

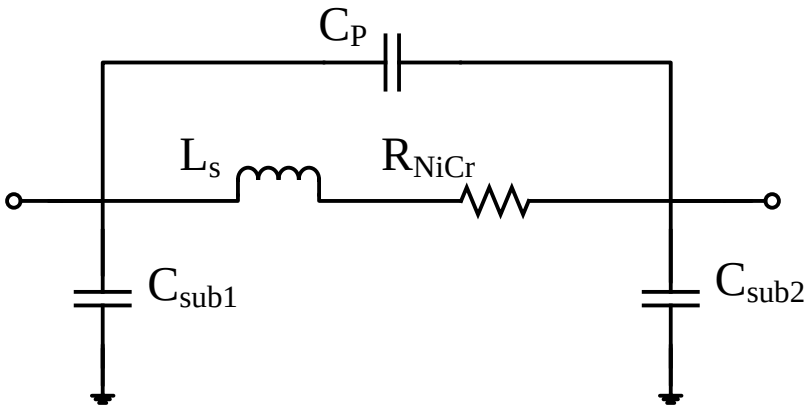


Figure 3.1: A typical equivalent circuit for NiCr resistor showing the prime and parasitic elements.

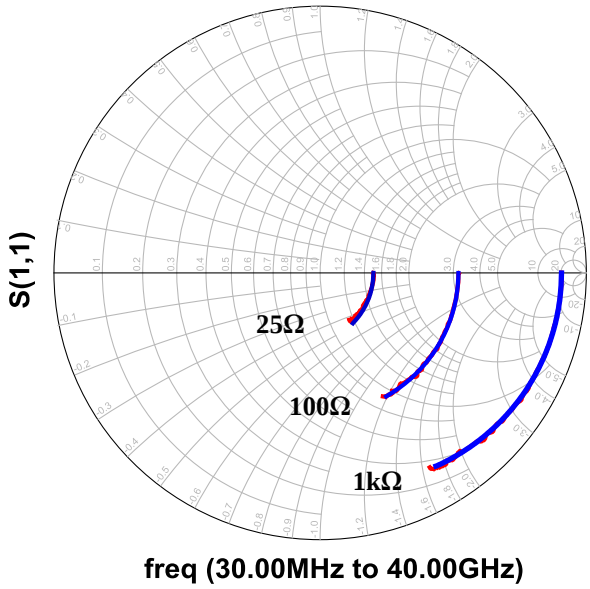


Figure 3.2: Simulated and measured results of reflection coefficient response (S_{11}) for various values of NiCr resistor (red and blue lines are for experimental and model results respectively).

In this work, NiCr resistors with various values ranging from 25 to 1kΩ were deposited on 200nm Si_3N_4 dielectric layer. The measured sheet resistance was found to be 50Ω/□ with a thickness of 120nm. Figure (3.2) shows good agreement between the modeled and

experimental results for 25, 100 and 1kΩ NiCr resistors. Comparable resistor values were also calculated from the slopes of the measured I-V characteristics. Furthermore, the extraction of C_{sub1} and C_{sub2} were carried out based on the S-parameter measurements and found to be 10 to 15fF depending on the resistors' value. Since the resistors were fabricated with a 15µm width, a negligibly small L_s was obtained, in line with equation (3.1); however, C_{sub1} and C_{sub2} values are expected to increase, necessitating an optimum dimension for a given NiCr resistor design.

3.4.2 MMIC Metal-Insulator-Metal (MIM) Capacitors

In general, capacitance is defined in terms of the ability of a passive component to store charge and this determines its impedance to radio frequency signals. Passing of RF signals can be through charging and discharging of the capacitors. In MMICs technology, there are two main ways to form a capacitor, such as the interdigital and MIM capacitors. Figure (3.3) shows generic interdigital capacitors whose values are strongly dependent on the separation distance between each two adjusted metal fingers, which are separated by a few microns. This type of capacitor is often realised in a similar manner to interconnect metallization used for transmission lines. The advantage of the interdigital capacitors does not solely come from the fabrication process simplicity where a single metal layer is needed but it is also due to the fact that its capacitance value is approximately insensitive to process variations[185, 192]. The fringing capacitance has fairly low values reaching ~1 pF, accordingly this is deemed to be not a helpful for *mm*-wave RTD oscillators in which the required capacitance is >5pF.

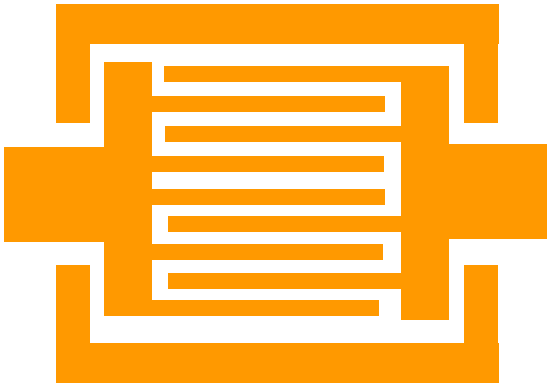


Figure 3.3: A top view schematic of an interdigital capacitor for MMIC applications.

On the contrary, the MIM capacitor values up to 200 pF can be achieved due to their construction from a layer of dielectric material sandwiched between two relatively large plates of metal as depicted in figure (3.4). There are many materials that are widely used as an insulator layer, namely Si_3N_4, SiO_2, benzocyclobutene (BCB), polyimide and a combination of a number of these layers. The effective overlapped area between the two parallel plates determines the capacitance of the structure whose expression is given by $C = \varepsilon_o \varepsilon_r \, wl/d$ where $\varepsilon_o$and ε_r are the dielectric constant of free space and relative permittivity of the dielectric respectively and all other parameters are indicated in figure (3.4).

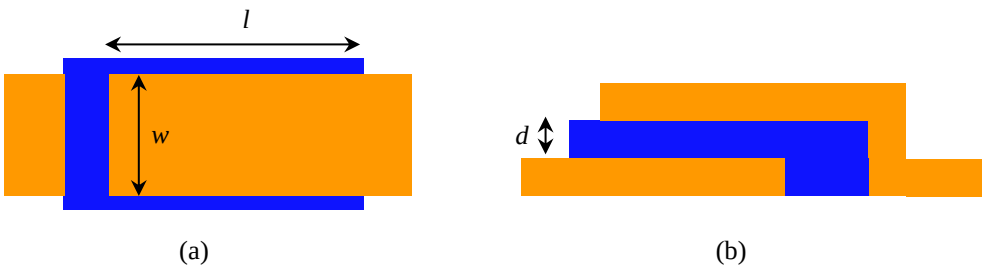


Figure 3.4: The schematic of MIM capacitor: (a) top view, (b) cross section view.

The relative dielectric constant of Si_3N_4 is between 7 to 7.5, while it is typically 2.7, 3.9 and 4.5 for BCB, SiO_2 and polyimide materials respectively. It is worth mentioning that the breakdown voltage and high frequency operation of MIM capacitors is determined by how high ε_r of the insulating material is and its thickness, favoring the use of Si_3N_4 over others. A low loss tangent of around 0.0003 for Si_3N_4 is another advantage that leads to further reduction in parasitic losses in integrated circuits[192].

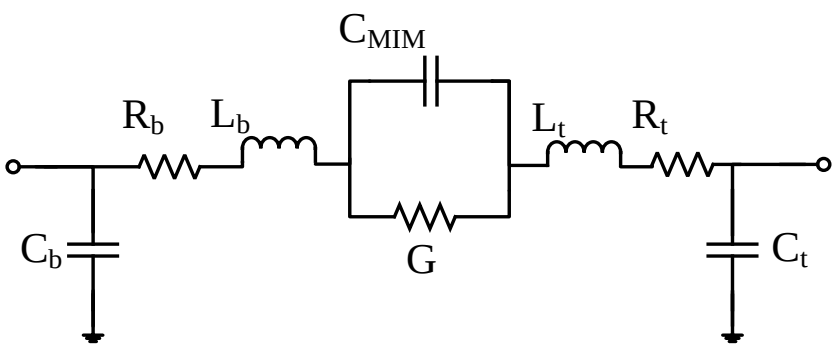


Figure 3.5: Equivalent circuit model for MIM capacitor used in this work involving the prime and parasitic elements.

There are various models for performance characteristic of MIM capacitors that were demonstrated, the well-known equivalent circuit model employed in this project was reported by L. Wang *et al*[193] as shown in figure (3.5). The value of the prime capacitance, C_{MIM} and the parasitic components can be determined by the physical dimensions of the top and bottom plates of the capacitor, such as the length and width of the plates in addition to the dielectric material type and its thickness. The frequency dependent conductance loss, G due to the dielectric is expressed as:

$$G = \omega C_{MIM} tan\delta \tag{3.3}$$

The parasitic resistances, inductances and capacitances caused by the top and bottom plates are denoted as $R_{t,}$ R_b, L_t, L_b, C_t and C_b respectively. According to the transmission line equations, $L_{t,b}$ and $C_{t,b}$ can be given by[194]:

$$L_{t,b} = \frac{0.4545 Z_o\, l}{c} \tag{3.4}$$

$$C_{t,b} = \frac{0.5 \varepsilon_{eff}\, l}{Z_o} \tag{3.5}$$

Where l, Z_o, c and ε_{eff} are the plate's length of the MIM capacitor, 50Ω characteristic impedance, speed of light and effective permittivity of the substrate respectively. As the MIM capacitors are normally designed with a square shape, their series resistances are trivial. Further increase in the width dimension can also reduce the parasitic inductances [192]. This is particularly important in high speed operation in which the associated parasitics degrade the circuit performance. In this work, various capacitor values have been fabricated and measured ranging from 1 to 20pF with a 200nm Si_3N_4 dielectric thickness.

The S-parameters response of the measured and equivalent circuit model results show a good agreement over the measured frequencies as depicted in figure (3.6). Form the fitting approach, $C_{t,b}$ and $L_{t,b}$ were estimated to be 55fF and 100pH respectively for a 1pF C_{MIM}. It was observed that the conductance loss is negligibly small, attributed to rather low tangent loss of Si_3N_4. As the value of the MIM capacitor gets larger, it does exhibit a short circuit at lower frequencies (i.e. S_{11}< -10dB) as shown in figure (3.7). The experimental results also demonstrated that the reflection coefficient of 5 and 10 pF

capacitors starts gradually rising with frequency, which is due to increase in the impedance of the parasitic inductances.

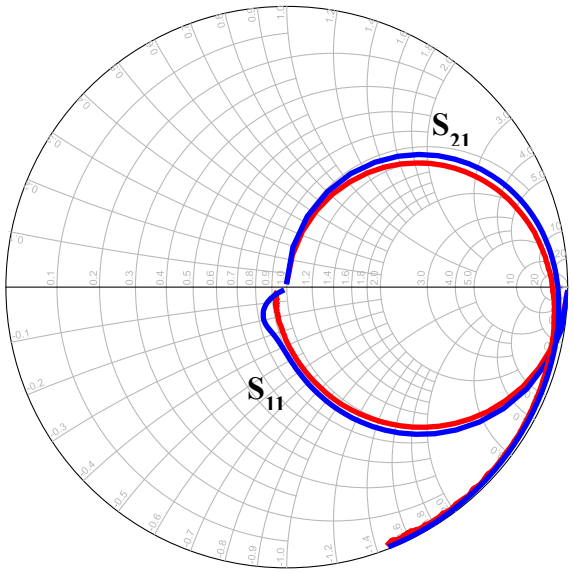


Figure 3.6: Measured (red) and simulated (blue) S-parameters response of 1pF MIM capacitor in the frequency range of 0.03-40 GHz.

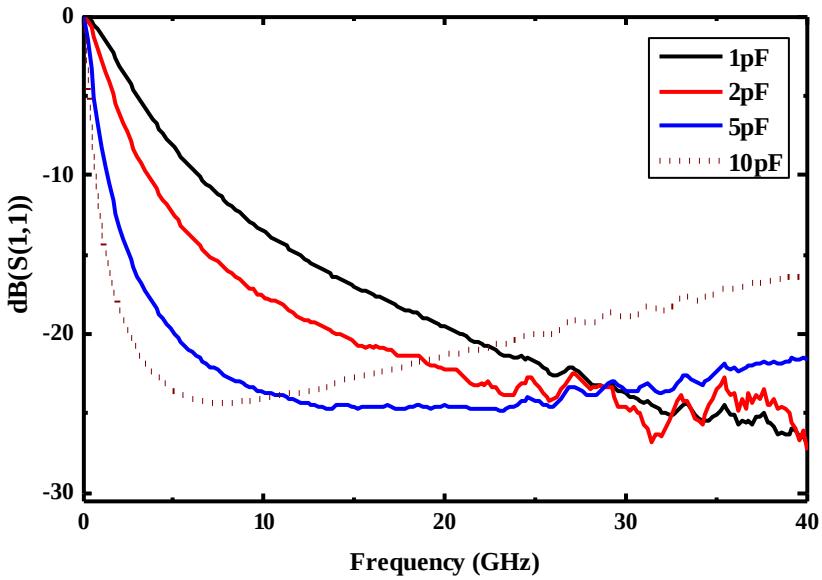


Figure 3.7: Measured reflection coefficient response of different MIM capacitors.

3.4.3 MMIC Spiral Inductors

On chip inductors have become progressively more valuable in high frequency integrated circuits particularly in CMOS and other technologies[195]. In ultra-high speed digital communication transceivers with a data rate over 100Gb/s, spiral inductors are highly

useful and so were investigated in the *mm*-wave regime[196]. Since the performance of a spiral inductor degrades in high frequency operation, a minimum quality factor exceeding 10 is still a challenge to achieve[195, 197]. An ADS momentum model was built in an attempt at improving the quality factor without significantly maximizing the size of the element. In general, planar inductors are fabricated by laying out one tract of metal with an overlapped interconnection transmission line. The most common inductors used in integrated circuits are square spirals whose cross-section view is shown in figure (3.8). The total inductance is determined by the sum of the self and mutual inductances as well as the number of turns (n_L) and physical dimensions of the inductor, such as outer diameter(D_L), inner diameter (d_L), track width (W_L), separation between tracks (S_L) and the overall length of the track (P_L)[198].

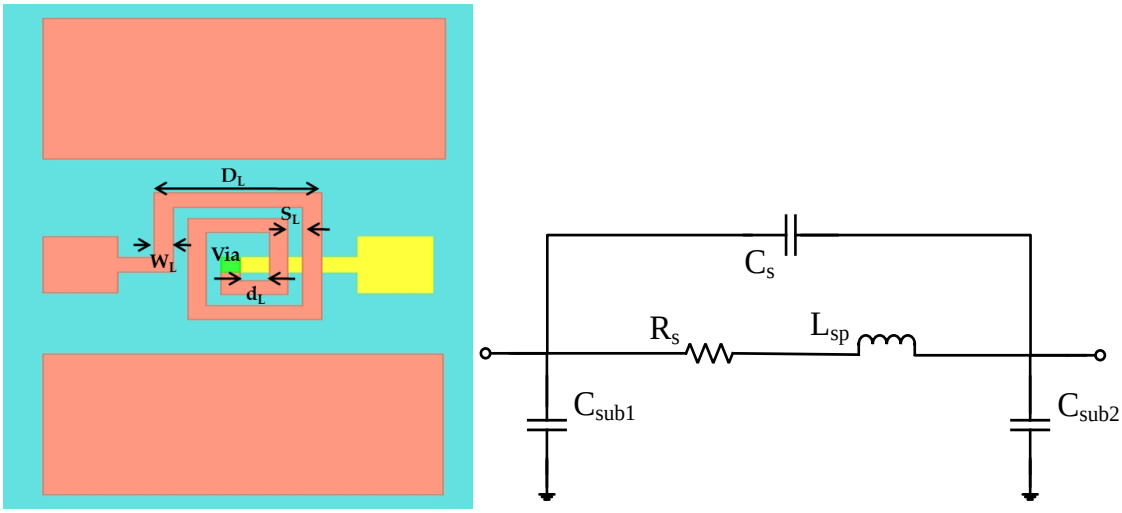


Figure 3.8: Cross section view of spiral inductor along with its equivalent circuit model including both prime and associated parasitic components.

The inductance of the spiral can be basically calculated from[199]:

$$L = k_{L1}\frac{\mu_o n_L^2 (D_L + d_L)}{1 + k_{L2}\psi} \tag{3.6}$$

$$\psi = \frac{D_L - d_L}{D_L + d_L} \tag{3.7}$$

Where μ_o, k_{L1} and k_{L2} are free space permeability and the latter two of which are layout-dependent factors. For square planar inductors, k_{L1} and k_{L2} are 2.34 and 2.75 respectively[199]. The prime element is the inductance, L_{sp} and the other parasitics due

to fringing and length of the track effects can be calculated using a π model extraction procedure[197]:

$$L_{sp} = -\frac{1}{\omega} imag\left(\frac{1}{Y_{21}}\right) \tag{3.8}$$

$$R_s = real\left(\frac{-1}{Y_{21}}\right) \tag{3.9}$$

$$C_{sub1} = imag\left(\frac{Y_{11} + Y_{21}}{\omega}\right) \tag{3.10}$$

$$C_{sub2} = imag\left(\frac{Y_{12} + Y_{22}}{\omega}\right) \tag{3.11}$$

It is noteworthy to mention that C_s and $C_{sub1,2}$ are caused by the inter-turn crossover and the interaction between the metal and the two ground planes respectively. The effective parameter in designing a spiral inductor is achieving a high quality factor which is formulated as the ratio of the imaginary part to real part of Y_{21} as given by[200]:

$$Q_f = \frac{imag(1/Y_{21})}{real(1/Y_{21})} \tag{3.12}$$

From equation (3.12), lowering the series resistance of the inductor is the key for a good Q_f, thereby reduce the noise figure of the integrated circuits. Spiral inductors with 3 and 7µm track widths were fabricated and tested. The equivalent circuit model and measured results for a 0.5nH inductor with 3µm track width are well-matched as depicted in figure (3.9). As can be observed that S_{11} exhibits an inductive behaviour and the S_{21} response does not intersect with the centre line of the chart, from which the self-resonant frequency (SRF) is evidently higher than the equipment frequency limitation. An extended frequency sweep for the equivalent circuit model revealed that this planar inductor has an SRF of 78GHz. It is noteworthy to point out that such inherent phenomenon occurs due to the existence of an associated capacitive effect which in turn cancels the inductive reactance at a certain frequency. This means that the inductive response is no longer obtainable, implying that these passive elements cannot be used at frequencies ≥ SRF. A 9Ω track length series resistance and C_s and $C_{sub1,2}$ values of 7, 23fF respectively were extracted from the measured data. The inductor has a Q_f of 25, which was estimated at high frequencies (i.e. >20GHz). Further increase in metal thickness of the tract can effectively boost the quality factor.

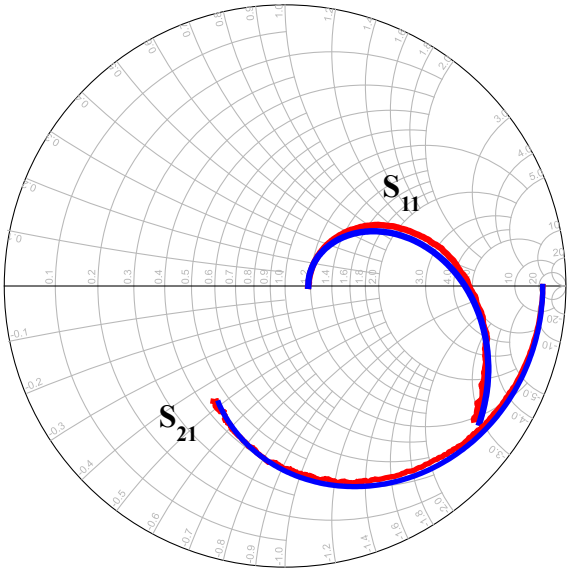


Figure 3.9: Measured (red) and simulated (blue) S-parameters response of 0.5nH spiral inductor in the frequency range of 0.03-40GHz.

An alternative approach is to optimize the inner diameter of the inductor in which the majority of the magnetic flux variation passes through a sufficiently large space would offer much less eddy current losses for higher quality factor and low noise circuit operation[197]. Table (3.1) illustrates comparison among various measured spiral inductors in terms of their series resistances, quality factors and self-resonant frequencies.

TABLE 3.1: COMPARISON AMONG IMPORTANT FACTORS FOR DIFFERENT SPIRAL INDUCTOR VALUES WITH A TRACT WIDTH OF 3μm.

PARAMETERS	SPIRAL INDUCTOR WITH 3μm TRACK WIDTH			SPIRAL INDUCTOR WITH 7μm TRACK WIDTH	
	0.5 (nH)	2.5 (nH)	6 (nH)	2.5 (nH)	6 (nH)
R_s (Ω)	9	22	46	11	18
Q_f	25	10	7	11	9
SRF (GHz)	78	25	14	23	12

Unsurprisingly, the experimental data shown in Table (3.1) indicates that R_s decreases for 7μm track width inductors; however, this has led to a slight decrease in self-resonant

frequency, which is related to an increase in inter-turn crossover capacitance. Due to the significantly increased series resistance with inductor values, the quality factor reduces. Generally speaking, minimizing an inductor footprint necessitates that the outer diameter must be made as small as possible. This essentially involves shrinking the metal track width and turn-to-turn spacing (S_L) and so improving in SRF; however, such an approach contributes to reduce the quality factor[196]. It was reported that a wide turn-to-turn separation distance diminishes the dependency of the inductance on the frequency variation[201] and this requires optimizing the inner diameter to further boost the quality factor. Therefore, the performance of the inductors is strongly dimensions-dependent emphasizing that their layouts have to be carefully designed.

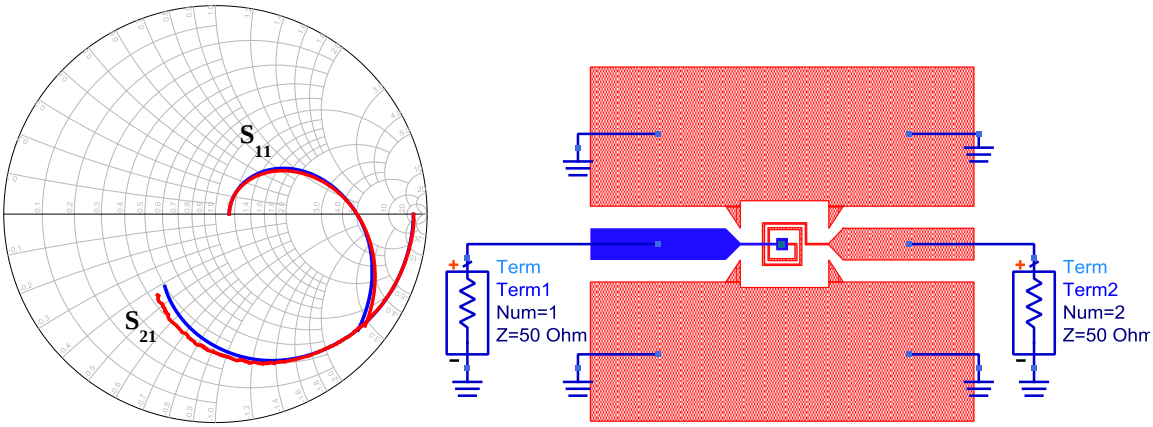


Figure 3.10: Measured (red) and EM simulation (blue) S-parameters response of 0.5nH spiral inductor in the frequency range of 0.03-40GHz plotted on a Smith chart alongside the layout of the spiral inductor shown in ADS-schematic.

A 2.5D simulations embedded in ADS-momentum tools was used for evaluating the S-parameters of the planar inductors. The module was performed by fitting with measured results as shown in figure (3.10). The measured and simulated results show very good agreement, validating the model employed in this project. Later on in this work, the module will be used in the prediction of circuit performances and to aid in further developments in layout of specific device based circuits.

3.4.4 MMIC Coplanar Waveguide (CPW)

The Coplanar waveguide was first introduced by Cheng P. Wen in 1969[202] and since then, a number of researches have been dedicated to its development. CPWs are normally

designed to connect the active devices (i.e. transistors and diodes) and passive components in either parallel or series configuration. In this work, CPWs are realised as an inductor to determine the oscillation frequency of oscillator circuits through resonating with the capacitance of the active devices. A conventional CPW structure consists of a strip of single conductor located between two finite width ground planes as shown in figure (3.11). As indicated in the 3D schematic, w is the signal line width, s is the gap distance between signal line and ground plane, g is the ground plane width, d is the thickness of the conductor and the length of the CPW is denoted as l.

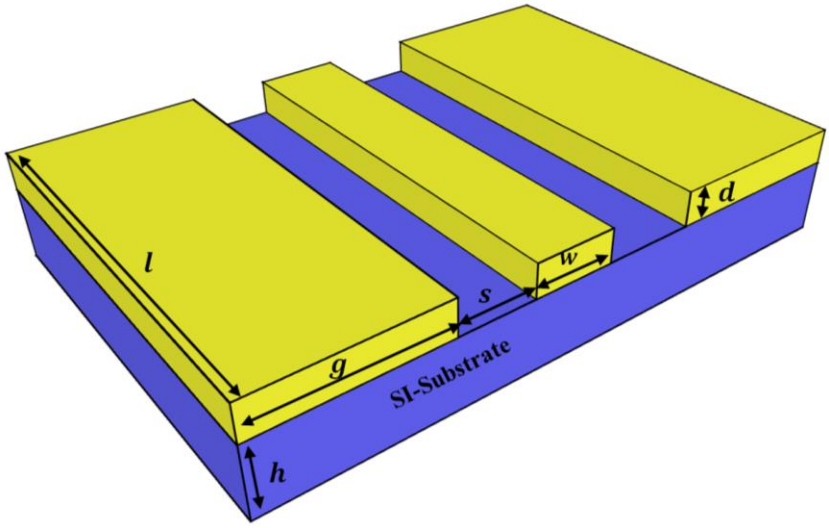


Figure 3.11: A generic 3D schematic of a CPW structure sitting on a semi-insulating substrate.

The simplicity of the CPW fabrication process comes from the requirement for merely a single mask step. Unlike conventional microstrip technology, there is no need for via holes for proper circuit operation in coplanar configurations. The characteristic impedance is determined by engineering the geometry of the conductor and separation distance, resulting in freedom in lessening the frequency dispersion of the CPWs. A high dielectric constant material is preferred as a substrate in order to suppress field radiation loss through the air. There are numbers of design rules that must be maintained for such a component, for example the width of the ground planes (g) should be double of the gap distance between signal line and ground plane. This is to reduce the radiation loss caused by a narrow ground plane structure. Furthermore, the thickness of the substrate, h must exceed the factor $w + 2s$, so that the impact of finite dielectric substrate can be ignored[185]. The thickness of the transmission line metal (d) is determined by at least three times the skin depth of the film. The skin depth of the metal is given by[203]:

$$\delta = \sqrt{\frac{\rho}{\pi\, f\, \mu_o \mu_r}} \tag{3.13}$$

Where ρ is the metal resistivity, f is the lowest operating frequency required and μ_o and μ_r are the free space permeability and relative permeability respectively. The key driving in estimating the skin depth at the lowest operating frequency of the integrated circuits is to ensure that the RF signal does not suffer from significant attenuations. For instance, for gold the resistivity is ρ= 2.44x10^{-8} Ω.m, the free space permeability μ_o= 4πx10^{-7} H/m, the relative permeability μ_r=1, at a frequency f =50 GHz, there parameters result in a skin depth of 0.35µm. The metal film thickness should therefore be at least 1.05 µm. The characteristic impedance, Z_o of a finite ground coplanar waveguide (FG-CPW) on a finite substrate and also the closed-form equations for effective dielectric constant, ε_{eff} can be expressed as[204]:

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k_1')}{K(k_1)} \tag{3.14}$$

Where $K(k_1)$ is the complete elliptic integral function of the first type and $K(k_1')$ its complementary function. These equations can be used in the typical implementations of CPW circuits in order to calculate the characteristic impedance and physical dimensions of the structure. The electromagnetic wave propagates along the CPW signal line within the dielectric of the substrate and the air, meaning that the wave travels in two different dielectrics media. Of course, these dielectrics have dissimilar propagation speed due to the difference in their permittivity. The effective dielectric constant, ε_{eff} is thus employed through analysing the CPW structures, which mostly acts the average of both ε_r media(i.e. the substrate and air)[143]. To calculate the characteristic impedance of the coplanar waveguides, the modulus of the complete integrals was demonstrated to be[204].

$$k_1 = \frac{w}{w+2s} \sqrt{\frac{g(w+2s+g)}{(s+g)(w+s+g)}} \tag{3.15}$$

$$k_2 = A \frac{sinh(\pi w/4h)}{sinh[(\pi(w+2s)/4h]} \tag{3.16}$$

$$k_{1,2}' = \sqrt{1 - k_{1,2}^2} \tag{3.17}$$

Where A is given by:

$$A = \sqrt{\frac{1 - sinh^2\left[\frac{\pi(w+2s)}{4h}\right] / sinh^2[\frac{\pi(w+2s+2g)}{4h}]}{1 - sinh^2(\frac{\pi w}{4h}) / sinh^2[\pi(w+2s+2g)/4h]}} \tag{3.18}$$

In this work, the CPW dimensions are calculated using the "LineCalc" tool embedded in Keysight-ADS software. This simulator is an analysis and synthesis tool which is designed to compute the physical dimensions and electrical parameters of transmission lines including strip and microstrip lines as well as CPW and GCPW structures.

3.4.5 Dispersion and Attenuation Characteristics in CPWs

It is well-known that the dimensions of the centre line and separation between ground planes and the centre line beside ε_{eff} and the thickness of the substrate determine the value of the characteristic impedance of the transmission lines. In this section, investigation of the impact of the variation parameters on the high frequency performance of the CPWs is broadly covered. The ability of eliminating the unwanted modes from propagating in such a configuration, due to the existence of two ground planes on both sides of the centre conductor, is indeed very valuable [205]. Losses in CPWs are often caused by three main sources: conductor losses, dielectric losses and change in the effective dielectric constant with frequency. It was stated in the literature[206] that as long as the ratio of the signal line width to ground to ground spacing $(w + 2s)$ is in the range of 0.4 to 0.7, the conductor loss constant of the transmission line is insignificant.

It has been argued that the dispersion caused by surface wave is very small, if the thickness of the substrate is much greater than the same factor $(w + 2s)$[207]. However, the substrate thickness, h is constrained by fulfilling the condition $(h \leq \frac{\lambda_g}{4})$, which is required to prevent high order modes from propagating (λ_g is defined as $c/f\sqrt{\varepsilon_{reff}}$)[208]. Furthermore, the loss tangent $(tan\delta)$ of the substrate plays a substantial role in terms of reducing dielectric losses, which can be estimated using[206]:

$$\alpha_d(N_P/m) = \frac{(\varepsilon_{reff} - 1)\varepsilon_r tan\delta}{(\varepsilon_r - 1)\varepsilon_{reff}\lambda_g} \tag{3.19}$$

A low loss tangent substrate is preferred to mitigate losses particularly at ultra-high frequency operation. All the electronic devices used in this work were grown on a lattice matched semi-insulting InP substrate, which has a $tan\delta$ of ~0.002. Due to the large number of the electric and magnetic field lines in the air, the effective dielectric constant of the CPW is normally low compared with the conventional transmission lines, leading to an increase in the characteristic impedance of CPWs[209]. The relationship which determines such a change is given by[207].

$$\varepsilon_{reff}(f) = \left(\varepsilon_{reff} + \frac{\sqrt{\varepsilon_r} - \varepsilon_{reff}}{\left(1 + a\left(\frac{f}{f_{TE}}\right)\right)^{-1.8}} \right)^2 \tag{3.20}$$

The surface wave mode cut-off frequency (f_{TE}) is expressed as:

$$f_{TE} = \frac{c}{4h\sqrt{\varepsilon_r - 1}} \tag{3.21}$$

$$\varepsilon_{reff} = \sqrt{\frac{\varepsilon_r + 1}{2}} \tag{3.22}$$

Where c and a are speed of light in vacuum and factor related to CPW dimensions which can be calculated using approximated equations presented in[210] respectively. An InP substrate with an ε_r of 12.5 and thickness of 625µm was utilized to evaluate the variation in ε_{reff} with frequency for various CPW dimensions as shown in figure (3.12). The calculated results reveal that narrow transmission lines exhibit less frequency dispersion than wide ones because their ε_{reff} approximately does not change for wide range of frequencies. An increase in ε_{reff} with frequency inevitably contributes to the appearance of alteration in characteristic impedance; hence losses due to reflections will be presented. This is followed by simulating the dependency of Z_o on structure's dimensions at 100GHz as depicted in figure (3.13). The model results show that a 50Ω characteristic impedance can be obtained at certain w and s values. On top of that, the impedance of the coplanar exponentially increases with the width of the signal line. A similar trend has been recently demonstrated[211, 212].

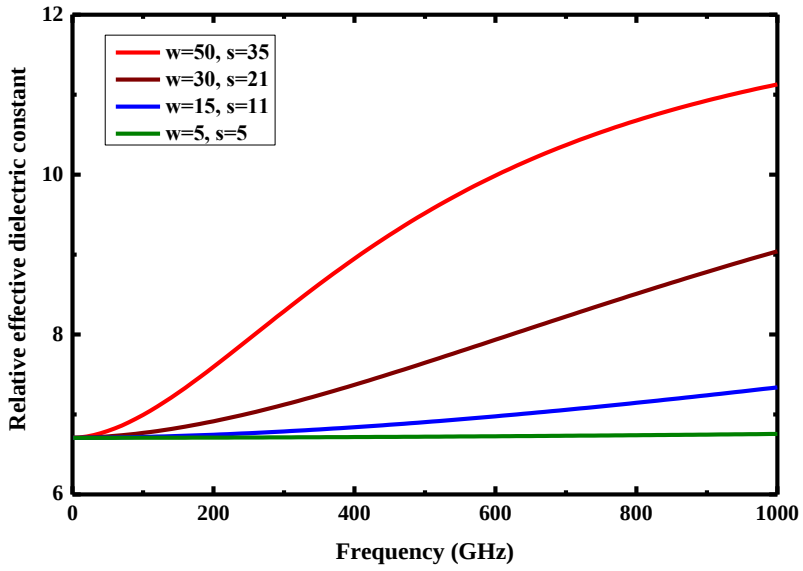


Figure 3.12: Relative effective dielectric constant versus frequency for different CPW dimensions sitting on an InP substrate. The surface wave cut-off frequency (f_{TE}) was found to be 35GHz. No that the width of the w and s parameters are in micrometre-scale.

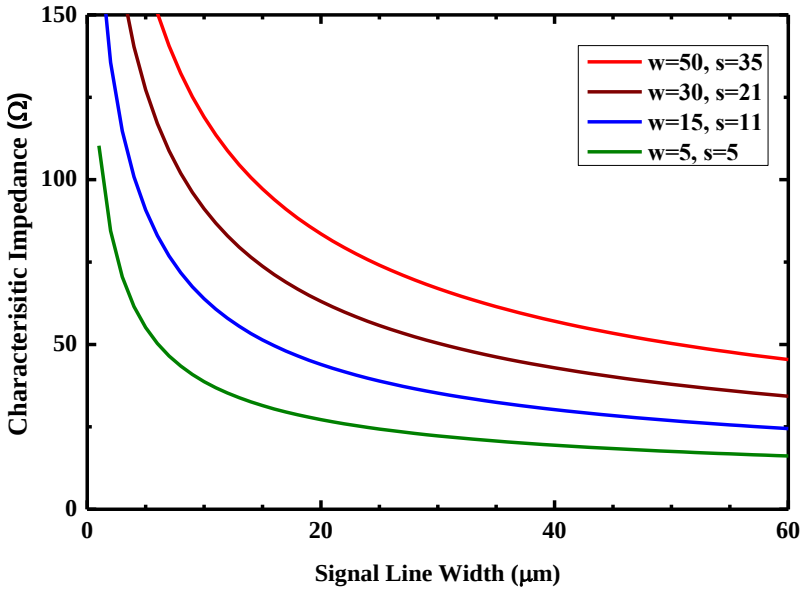


Figure 3.13: Simulation results of the characteristic impedance of the CPW with various dimensions, the structure is sitting on an InP substrate with an ε_r of 12.5.

According to the findings, providing a good matching between the RF measuring equipment and the integrated circuits requires maintaining the fabricated transmission line dimensions to be as close to the designated ones. This is fairly feasible with i-line photolithography technique, in which the process can achieve 1μm resolution. Thus far, all the CPWs were modeled under the assumption that ε_r of the semi-insulating substrate

is constant. In the real-world, this crucial parameter does change with frequency, resulting in a different transmission line performance.

The characteristic impedance of similar dimensions was extracted as a function of relative dielectric constant as shown in figure (3.14). The ε_r was assumed to be in range of 12.5 at low frequency to 9.6 at high frequency. The conductor used, in this study, is gold with a thickness of 1µm. A narrow signal line width provides high Z_o, nearly reaching 70Ω at an ε_r of 9.6 (at high frequency), in comparison with lower impedance introduced by wide lines. The reason is due to the fact that narrow conductor lines have large series resistance, which can be compensated by depositing a sufficiently thick metal (>1µm). However, this might not be necessary as narrow transmission line CPWs exhibit much less influence in frequency dispersions. Furthermore, several micrometre coplanar dimensions would present a negligibly small associated parasitics, considered desirable for an integrated circuit operating beyond microwave frequencies.

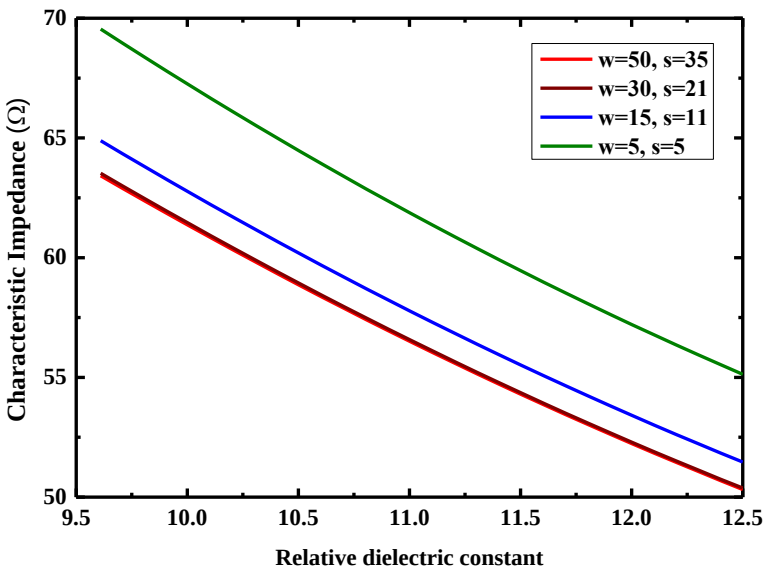


Figure 3.14: Dependence of the characteristic impedance of the CPWs on relative dielectric constant for various structures' dimensions.

3.5 Summary

The importance of MMIC technology and a brief description of 2.5D momentum module developed in this project were presented here. The main objective of this chapter is to experimentally study the equivalent circuit parameters of the passive elements including NiCr resistors, MIM capacitors, spiral inductors and CPW transmission line

configurations. NiCr resistors with various values ranging from 25 to 1kΩ were fabricated and tested. A 50Ω/□ measured sheet resistance was obtained for a NiCr thickness of 120nm and experimental results were well-matched with the equivalent circuit models involving all potential parasitics in the circuits. Since the resistors were fabricated with a 15µm width, a negligibly small L_s was obtained. For the MIM capacitors, the measured results demonstrated that the capacitors become short circuits at lower frequencies (i.e. S_{11}<< -10dB) when their values get higher, as expected.

A quality factor of 25 with a 9Ω track length series resistance for a 0.5nH spiral inductor was extracted. Further increase in metal thickness of the tract can effectively boost the quality factor. As expected, the experimental data revealed that R_s decreases with increase in the width of the inductors; however, this has led to a slight decrease in self-resonant frequency due mainly to an increase in inter-turn crossover capacitance. Nevertheless, reducing the track length resistance was interpreted into improving the quality factor. In general, boosting SRF requires minimizing the inductor footprint and this necessitates that the outer diameter must be made as small as possible, which can be simply performed by shrinking the metal track width and turn-to-turn spacing. For the CPW characterizations, the calculated results showed that narrow transmission lines exhibited less frequency dispersion than wide ones as a result of a very small variation in their ε_{reff} for wide range of frequencies. However, these narrow signal lines CPWs have a high Z_o reaching 70Ω at an ε_r of 9.6 (at high frequency). This is caused by a large series resistance associated with narrow conductor lines, implying that such an issue can be compensated by depositing a sufficiently thick metal, roughly exceeding 1µm.

CHAPTER 4: DEVELOPMENT OF HIGH FREQUENCY RTD BASED CIRCUITS

4.1 Introduction

In previous chapters, literature review and characterizations of resonant tunneling diodes were investigated in detail as a preface regarding the feasibility and usefulness of the tunneling devices for microwave and THz applications. Therefore, chapter four concentrates on two fundamental aspects of the RTD based circuits. This involves modeling a high frequency oscillator and microwave amplifier utilizing an integrated RTD biased in its NDR region. To fulfill the oscillation requirements, a stabilizing circuit with proper operation must be used, so an associated discussion is presented here as well. High output power capability and limitations in the *mm*-wave/THz regime oscillators and what strategies can be exploited to address these issues are discussed.

Furthermore, the reflection-based amplifiers using RTDs as active loads are covered in this chapter too, including their working principle and the designed module built in Keysight-ADS software. The key outcome of this study is the realization of a µW level DC power consumption amplifier operating in K-band frequencies. This is followed by optimization of the integrated circuit's parameters aiming for high performance amplifier operation.

4.2 Requirements for RTDs Oscillator Design

In general, an RTD oscillator consists of three main elements, the RTD device, resonator and stabilizing circuit as shown in figure (4.1). As long as the net negative differential resistance of an RTD is greater than zero, the device is still able to be used in the circuit. The resonators act as an inductor, L_{os} and are often realized using antennas and transmission lines, for example microstrip lines, CPS and CPWs. In this project, CPWs were used due to their fabrication process simplicity as no via holes are required compared with conventional transmission lines. The stabilizing circuit or normally known as decoupling circuits are predominantly fabricated with a parallel combination of resistor, R_{sh} and capacitor C_{cp}. The voltage bias, V_{bias} of the oscillator circuit depicted in

figure (4.1) sets the diode in the negative differential resistance region. The parasitics caused by the DC biasing cable are denoted as R_b and L_b.

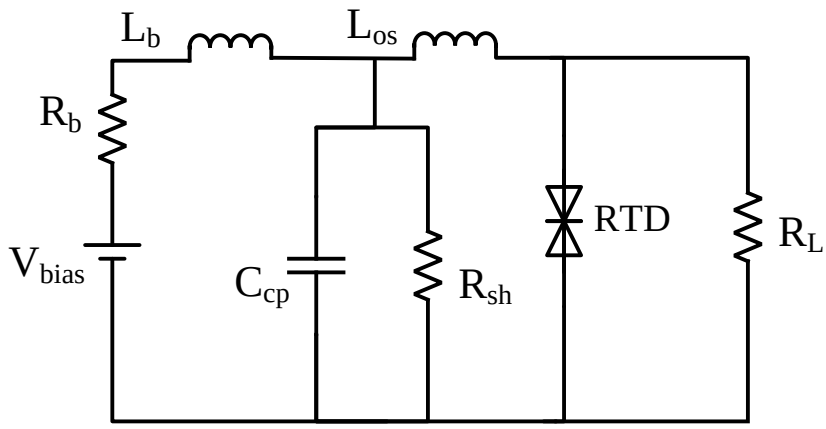


Figure 4.1: A single RTD oscillator topology with shunt resistor, R_{sh} and decoupling capacitor, C_{cp}.

The inductance of the CPW and the intrinsic capacitance of the RTD determine the high frequency oscillation by resonating at a certain frequency in accordance with their respective values. To theoretically analyze the circuit operation and for the sake of simplicity, the effect of the parasitic elements was neglected. From the oscillator circuit, the derived susceptance (i.e. the imaginary part of the admittance) is set to zero to sustain the oscillation as given by:

$$2\pi f_{osc} C_{RTD} - \frac{1}{2\pi f_{osc} L_{os}} = 0 \tag{4.1}$$

The oscillation frequency can be then expressed as:

$$f_{osc} = \frac{1}{2\pi\sqrt{C_{RTD} L_{os}}} \tag{4.2}$$

In practice, the oscillation frequency would be slightly different from the one given by equation (4.2) due to the additional parasitics not included in the formula. Thus, choosing the inductor value is not arbitrary as such a crucial parameter relies on the tuning in the CPW conductor length. The maximum operating frequency and RF power of the RTDs are the most important quantities in the circuits design; the former is given by $f_{max} = (|G_{RTD}|/2\pi C_{RTD})\sqrt{(1/R_s|G_{RTD}|) - 1}$, which can be rearranged to become:

$$f_{max} = \frac{3\Delta I}{4\pi C_{RTD}\,\Delta V}\sqrt{\frac{2\Delta V}{3\Delta I\,R_s} - 1} = \frac{1}{2\pi C_{RTD}}\sqrt{\frac{3\Delta I}{2\Delta V R_s} - \frac{9\Delta I^2}{4\Delta V^2}} \tag{4.3}$$

f_{max} deduced from equation (4.3) can give a good indication about how far the upper oscillation frequency is affected by the device capacitance, series resistance beside current difference and voltage span. In order to further maximize f_{max}, the trade-off between the mesa area and series resistance has to be effectively balanced. The spacer thickness can be made thicker, contributing to a decrease in C_{RTD} without the need to minimize the mesa area. This can also assist in improving the PVCR as a result of a reduction in ionized impurity scattering events. However, thick spacers increase the carriers' transit time in the collector depletion region and reduces the peak current density, due to a suppression of current stream in thick spacers[92]. In-depth discussion for optimization of an RTD structure was already presented in chapter two and will not be repeated here.

4.3 DC Stability of Oscillator Circuit

In addition to the self-capacitance of the RTD and the inductance of the resonator, other conditions must be satisfied to sustain the oscillation. This is simply due to a plateau-like current oscillation in the NDR region of the device, resulting in the radio frequency to be distributed between low and designed frequencies[6]. To remedy this problem, a stabilizing circuit RC combination was employed in this work. The shunt resistor, R_{sh} is to suppress the parasitic bias oscillation at low frequency (2-3GHz). For the intrinsic equivalent circuit of an RTD integrated with a resonator, the real part of the admittance is given by:

$$Real(Y_{in}) = \frac{1}{R_{sh}} - \frac{G_{RTD}}{(1-\omega^2 L_{os} C_{RTD})^2 + (\omega L_{os} C_{RTD})^2} \tag{4.4}$$

To sustain the oscillation at the desired frequency, $Real(Y_{in})$ must be negative, providing instability status for proper circuit operation. However, the real part of the admittance is positive at low frequencies, contributing to suppression of the parasitic oscillation and the circuit is stable (no oscillation) and this gives $(Y_{in}) = [(1/R_{sh}) - G_{RTD}] > 0$. To do so, this condition $R_{sh} < 1/G_{RTD}$ has to be fulfilled. It is important to point out that

R_{sh} must be sufficiently low to achieve bias stability requirement and reduce the DC power consumption of the oscillator (i.e. this enables an enhancement in the DC to RF conversion efficiency) but large enough to boost the extracted RF power of the circuit, [213]. However, the shunt resistor still consumes power so that a decoupling capacitor is connected to act as a short circuit at high frequency, avoiding RF power being dissipated by the resistor. The value of the decoupling capacitor can be calculated by:

$$(2\pi f_{osc} C_{cp})^{-1} < 0.1 \tag{4.5}$$

Since the negative conductance is expressed as $G_{RTD} = 3\Delta I/2\Delta V = 3\Delta JA/2\Delta V$ and this equation can be rearranged to be:

$$R_{sh} < \frac{2\Delta V}{3\Delta J RTD_{Area}} \tag{4.6}$$

The maximum RTD size, RTD_{Amax} for a given shunt resistor must be fulfilled in order to stabilize the oscillator with the maximum RTD mesa area[214].

$$RTD_{Amax} < \frac{2\Delta V}{3\Delta J R_{sh}} \tag{4.7}$$

For the InGaAs/AlAs RTD sample XMBE#300 with 4μm^2 whose DC characteristic are summarized as $\Delta V = 0.26\text{V}$, $\Delta J = 0.85\text{mA}/\mu\text{m}^2$ and with a shunt resistor $R_{sh} = 20\Omega$, the maximum RTD size based on the stability criteria is:

$$RTD_{Amax} < 10.2\mu m^2$$

The RTD_{Amax} calculated for this particular RTD is larger than the device size (i.e. 4μm^2), meaning that the shunt resistor of 20Ω is adequate to DC stabilize the oscillator circuit. Hence, the parasitic oscillation is suppressed and the RF power is expected to rise. Equation (4.7) also suggests that large device sizes require a small R_{sh}, which is relatively difficult to fabricate.

4.4 Modeling of Single RTD Integrated Oscillators

Since one of the main objectives of this project is to realize a high frequency oscillator utilizing the resonant tunneling diodes as an active device, modeling of such an

integrated circuit prior to fabrication process is very important including all the DC characteristics required for high performance RTD oscillator, which was extensively discussed in chapter two. As a primary example to investigate the performance of high frequency oscillator circuit based electromagnetic modelling, InGaAs/AlAs RTD sample XMBE#230 was used. The device was grown on a semi-insulating InP substrate using Solid Source Molecular Beam Epitaxy (SSMBE) and its epitaxial stack is shown in Table (4.1).

TABLE 4.1: EPITAXIAL LAYER FOR RTD SAMPLE XMBE#230.

Layer	Material	Doping (cm^{-3})	Thickness (Å)
Top Ohmic	$In_{0.53}Ga_{0.47}As$	2×10^{19} (Si)	450
Collector	$In_{0.53}Ga_{0.47}As$	3×10^{18} (Si)	250
Spacer	$In_{0.53}Ga_{0.47}As$	Undoped	200
Barrier	AlAs	Undoped	12
Well	$In_{0.8}Ga_{0.2}As$	Undoped	45
Barrier	AlAs	Undoped	12
Spacer	$In_{0.53}Ga_{0.47}As$	Undoped	200
Emitter	$In_{0.53}Ga_{0.47}As$	3×10^{18} (Si)	250
Bottom Ohmic	$In_{0.53}Ga_{0.47}As$	1×10^{19} (Si)	4000
Substrate	InP		

The measured I-V characteristic of a diode with a mesa size of 9μm^2 is depicted in figure (4.2). Table (4.2) shows the room temperature DC characteristics of the diode. This device has a large G_{RTD} of 29mS and a high peak current density of 1.2 mA/μm^2 with a very high PVCR of 9.4 in the reverse bias direction and thus higher output power can be expected. These characteristics can be easily improved further by reducing the thicknesses of the well and barrier. The self-capacitance of the diode was extracted after the parasitic bond capacitance and inductance were de-embedded[215]. Validation of the equivalent circuit of the device was then verified using a fitting model with the measured scattering data. To this end, the estimated intrinsic capacitance in the middle of the NDR was found to be ~6 fF/μm^2. Accordingly, the key- parameter, f_{max} of this device is 220 GHz, evaluated employing the extracted values of the equivalent circuit. To further

extend such a figure of merit to reach THz frequencies, ~1 μm^2 device size is required, which is relatively feasible with the standard i-line photolithography technique

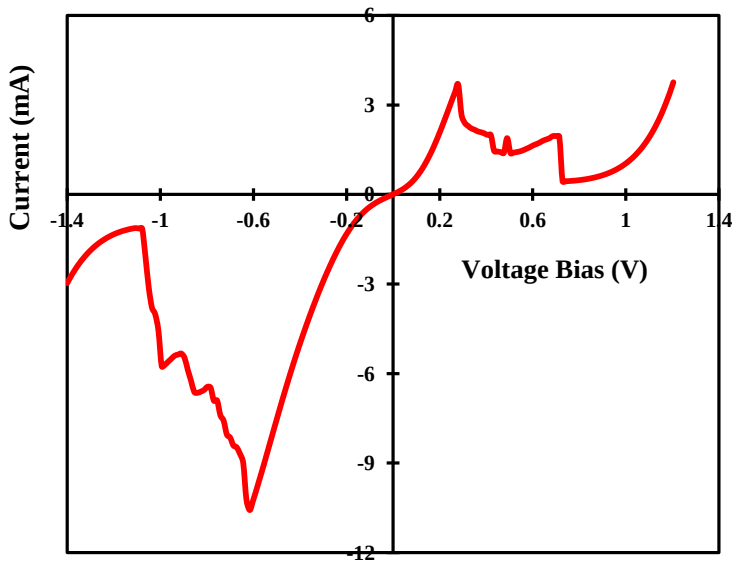


Figure 4.2: I-V characteristic of the InGaAs/AlAs RTD device sample XMBE#230 with a mesa area of 9 μm^2.

TABLE 4.2: DC CHARACTERISTICS FOR THE RTD SAMPLE XMBE#230 WITH A MESA AREA 3×3μm^2 AT ROOM TEMPERATURE.

RTD Sample XMBE#230	|ΔV| (V)	|ΔI| (mA)	|G_{RTD}| (mS)	PVCR	J_P (mA/μm^2)	P_{max} (μW)
Forward bias	0.45	3.5	11.6	8.4	0.41	295
Reverse bias	0.49	9.45	29	9.4	1.2	868

To connect the passive and active components of the oscillator and determine the oscillation frequency of the circuit, a CPW resonator was used. In this work, the dimensions of the CPWs are computed using "LineCalc" tool embedded in Keysight-ADS from Agilent Technologies. There are some parameters which must be defined to obtain the physical dimension of the resonator, such as ε_r, thickness and loss tangent of the substrate as well as skin depth of the conductor. The characteristic impedance of the CPW was set to be 50Ω to match the standard equipment setup. Furthermore, the electrical length, βl should be < 90°, thereby ensuring an inductive reactance for the shorted coplanar structure. The first step of the RTD oscillators design is to calculate the

oscillation frequency, given in equation (4.2), the wavelength of the generated RF signal can be then expressed by:

$$\lambda = \frac{c}{f_{osc}\sqrt{\varepsilon_{eff}}} \tag{4.8}$$

Where c is the speed of light and ε_{eff} is the average of the relative dielectric constant between the substrate and air. The input impedance of the short end CPW is theoretically computed by the well-known relationship of the transmission line impedance[203]:

$$Z_{in\,(CPW)} = Z_o \frac{Z_L + jZ_o \tan \beta l}{Z_o + jZ_L \tan \beta l} \tag{4.9}$$

Of course, the inductance of the oscillator does not solely rely on physical length of the CPW. This is due to the fact that the current passes through the conductor film at the end of the slots, leading to a magnetic energy to be stored behind the termination[216]. An inductive reactance is thus situated beyond the slots, denoted as L_{sc} and the effective length extension, l_{ext} based on this inherent phenomenon can be given by[47]:

$$l_{ext} \simeq \frac{w + 2s}{8} \tag{4.10}$$

The inductance of this extension length is expressed as:

$$L_{sc} = \frac{Z_o \beta l_{ext}}{2\pi f_{osc}} \tag{4.11}$$

w being the signal line width and s is the gap distance between signal line and ground plane of the CPW. In the radio frequency signals, there is a 2π phase variation in every single wavelength, the phase velocity is; thus, formulated as $\beta = 2\pi/\lambda$[217]. From equations (4.9), (4.10) and (4.11), the total physical length of the shorted CPW, taking the impact of l_{ext} extension into account, becomes[6]:

$$l = \frac{\lambda}{2\pi} \tan^{-1}\left[\frac{2\pi f_{osc} Z_o (L_{os} - L_{sc})}{Z_o^2 + 4\pi^2 f_{osc}^2 L_{sc} L_{os}}\right] \tag{4.12}$$

The resonator length at various oscillation frequencies was calculated using ADS tools and a comparable result was found from equation (4.12). It is important to mention that the major behavior of the shorted transmission line stubs with narrow center conductor width is inductive at high frequency[143]. There is no available built in model for the

tunneling devices in the CAD used, the RTD was, thus, implemented exploiting a SDD2P (Symbolically Defined Devices Two Ports) block with a 9th order polynomial equation. The realized module utilized the reverse bias direction of the measured I-V characteristic as depicted in figure (4.3) to take advantage of the high DC performance obtained in the reverse bias compared with the forward bias direction. A plateau-like current oscillation in the NDR region of the experimental data is caused by the bias equipment setup.

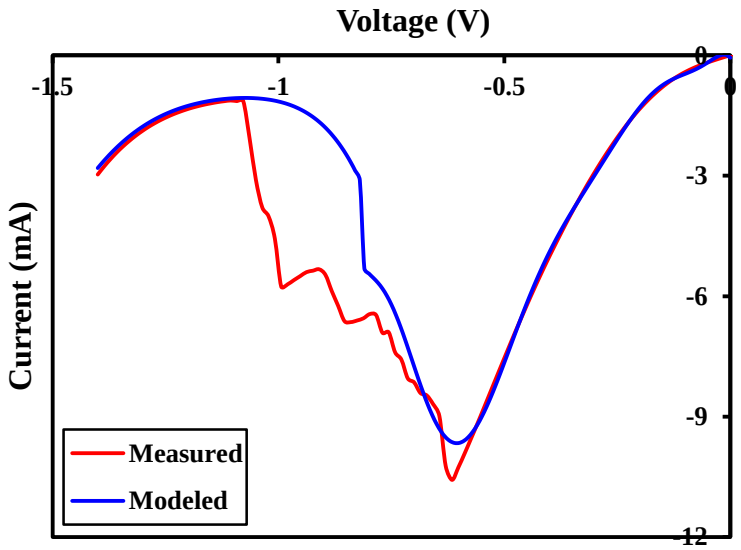


Figure 4.3: Measured IV characteristic for the RTD XMBE#230 with 9µm mesa size in comparison with 9th order polynomial fitting equation modeled in Keysight-ADS.

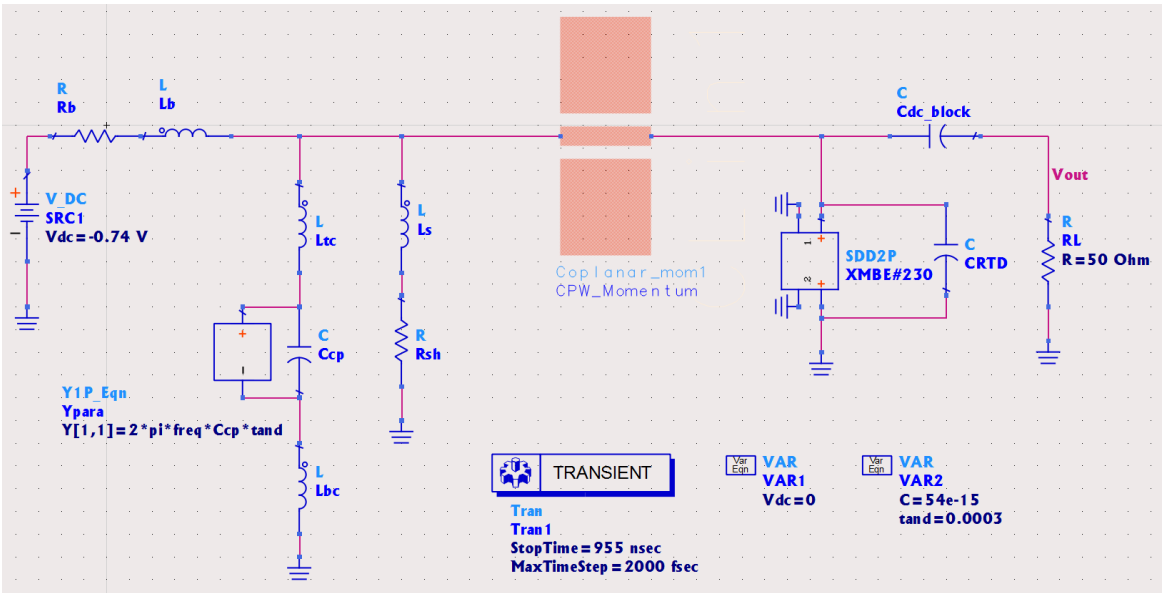


Figure 4.4: A schematic of the designed RTD oscillator circuit in ADS software, using InGaAs/AlAs RTD device sample XMBE#230 with a mesa area of 9µm^2.

In the module used, the intrinsic equivalent circuit of the RTD was made up of a dynamic current source connected in parallel with C_{RTD} as shown in figure (4.4). This implies that such a configuration is implemented under the assumption of involving both the series and junction resistances of the device in the measured I-V characteristic (i.e. $\frac{\partial V}{\partial I} + R_s$). In this work, the stabilizing circuit is realized with a combination of shunt resistor, R_{sh} and decoupling capacitor, C_{cp} to suppress the parasitic oscillation and prevent RF power being dissipated by R_{sh} at the operating frequency. To avoid considerable errors in the design and make the simulation results close to the actual practical data, the non-ideal nature of the passive components was taken into account. This is largely because the values and performance of these elements depend on the fabrication process instead of only design equations. The equivalent circuit models for R_{sh} used here is the one proposed by S. Renu *et al*[191], which includes a series inductance denoted as L_s due to the length of the NiCr. Furthermore, the MIM capacitance is represented by the equivalent circuit reported by L. Wang *et al*[193], comprising the prime lumped component as well as the top and bottom metals' inductances (L_{ct} and L_{bc} respectively). It also takes the effect of the substrate's loss tangent into account, which is given by: $G_{MIM} = \omega C_{cp} tan\delta$, where ω is the angular frequency and $tan\delta$ is the loss tangent of the insulating material used.

The dimensions of the decoupling capacitance have been optimized to alleviate the non-ideal behavior of the components, for example the additional inductance and resistance of the metals. In-depth discussion and analysis regarding the extraction of the equivalent circuit parameters' model for the passive elements was elaborated in chapter three. The parasitic of the dc bias set-up, R_b and L_b shown in figure (4.4), were estimated to be 1 Ω and 1nH respectively. The RTD sample #230 is biased at the centre of the NDR region and a load resistor with a 50Ω is used to match the input impedance of the measuring equipment with a dc block capacitance (C_{dc}). The circuit was simulated at 100GHz operating frequency by the transient simulation tool with the following components values: R_{sh}=21 Ω, C_{cp}=20 pF. Since the entire circuit will be monolithically integrated on the InP substrate with an ε_r of 12.5, the CPW inductor of L_{os}=47pH was calculated, corresponding to 1.15mm wavelength signal at 100GHz frequency. With this in mind, the electrical length of the transmission line was found to be ~30.5°, so the estimated physical length of the resonator is 97µm.

A 2D electromagnetic model built in ADS-momentum was used to simulate the CPW resonator, facilitating the coupling impact of the neighbouring transmission lines and the losses in the ground plane to be involved in the simulation. This model was already validated using fabricated passive components as presented in the previous chapter. Figure (4.5) shows the output voltage signal across the load resistor, R_L over a 5 ns and 0.1 ns time span. The sinusoidal wave has 224 mV peak to peak voltages. To extract the RF output power, a Fast Fourier Transform (FFT) was then taken as depicted in figure (4.6). The resulting power at the fundamental frequency of 100 GHz is 100 µW (-10dBm). It is also apparent from the spectrum that the first harmonic occurs at 201GHz with an extremely low power of 0.05µW.

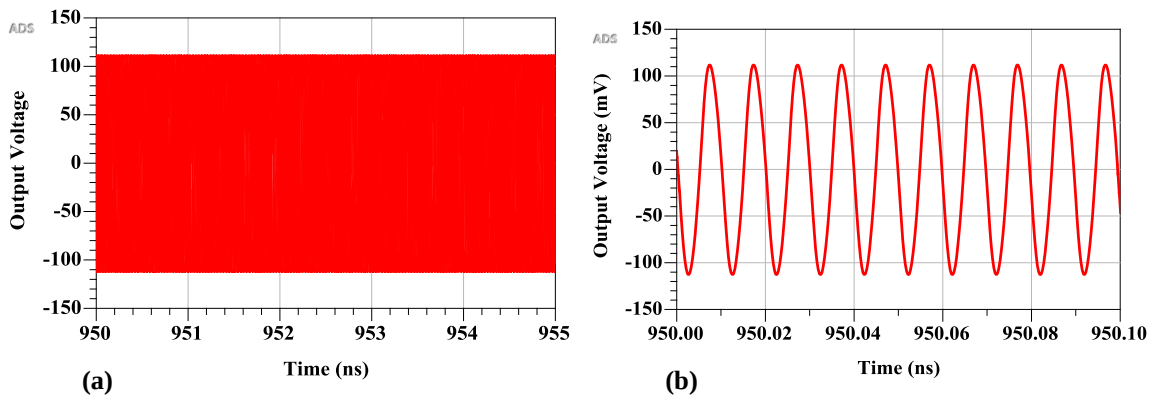


Figure 4.5: Simulation result of the output voltage across the load (a) over 5 ns time span (b) over 0.1 ns time span.

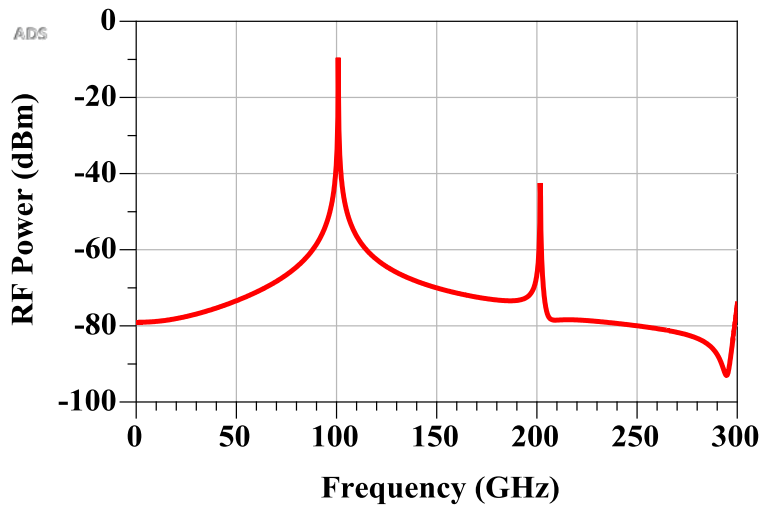


Figure 4.6: The spectrum of the output voltage signal across the load of the RTD oscillator modelled in ADS using device sample #230 with 9 µm^2 mesa size.

Unsurprisingly, the simulated oscillation frequency is clearly shifted from the calculated one as this mainly due to the parasitic components associated with the circuit model. The maximum output power can be theoretically achieved when the condition ($G_L = G_{RTD}$) occurs for single RTD oscillator, where G_L is the conductance of the load. It is well-known that the negative conductance of the RTD decreases with frequency, thus; the latter condition should be satisfied at the desired operating frequency. One of the most important features of RTD oscillators and still considered a challenge is the circuit DC-to-AC efficiency. This key-factor was calculated to be 2% including the power dissipated in the shunt resistance.

4.4.1 Variations in Circuit Parameters and Performance

The designated operating frequency is 100 GHz but higher frequencies can be also investigated. This approach is to investigate the effect of the parasitic components caused by the embedded circuit on the oscillator performance in terms of high RF power. To examine the oscillator's performance in the frequencies beyond 100 GHz, the relationship between the oscillation frequency and the RF power was then studied. The resonator inductance (L_{cpw}) value was changed in the range of 68 pH to 25 pH, corresponding to a CPW length ranging from 137 to 54 µm respectively. Note that all other component values used throughout the simulation setup were maintained similar to the ones given in the previous section. The outcome from the simulation result was that the output power decreases with increasing the oscillation frequency as depicted in figure (4.7).

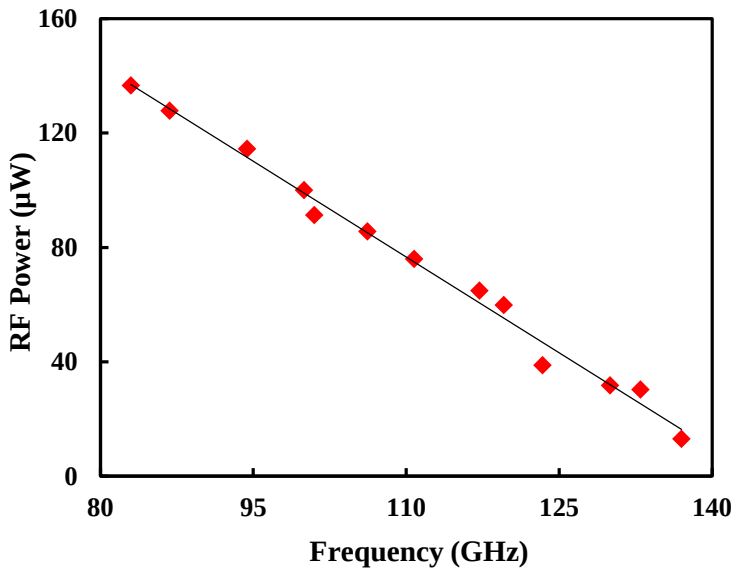


Figure 4.7: RF power of the RTD oscillator versus fundamental oscillation frequency simulated in ADS.

The main reason behind this behavior is attributed to the reduction in the negative differential resistance with the operating frequency. This was reflected into a decrease in the obtained output power, significantly emphasizing the importance of high G_{RTD} RTDs for promoting the oscillator characteristics. On the basis of this consideration, maximizing the performance of the oscillator requires further thinning in the barriers and quantum well of the RTD structure for ultrafast transit delay time as stated in the following formula $P_{RF-actual} = (3/16)\Delta I\ \Delta V\ cos\ \omega\tau_{RTD}$[184]. The RTD oscillator reported here gives a potential power output of 30 µW at 133 GHz, which is relatively low for this particular RTD. This could be due to mismatching between the conductance of the load and RTD. More importantly, low RF power was most likely exacerbated as result of the parasitic elements of the passive components.

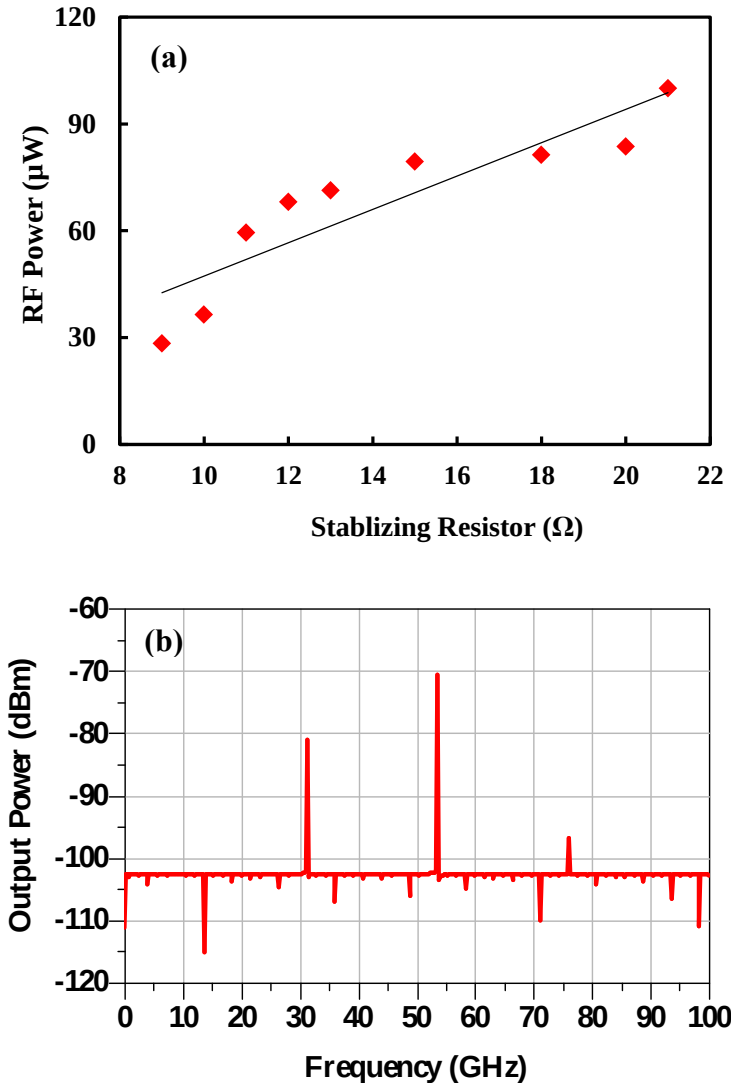


Figure 4.8: Simulated result for the RTD oscillator, the device used is sample #230 with 9 µm^2 mesa size (a) RF power versus the stabilizing resistor when $R_{sh} < 1/|G_{RTD}|$, (b) The extracted spectrum when $R_{sh} > 1/|G_{RTD}|$.

Since the variation in the stabilizing resistor has a strong influence on the circuit performance, the oscillator model was simulated with different R_{sh} values. Figure (4.8, a) shows that the extracted power increases with the stabilizing resistor values. However, higher R_{sh} (i.e. $R_{sh} > 1/|G_{RTD}|$) leads to a disappearance of the oscillation at 100GHz frequency because the stability status cannot be satisfied at low frequencies as depicted in figure (4.8, b). Consequently, the power was distributed between the designed frequency and low biasing oscillation, as is observed in the spectrum. Note that stability status (or no oscillation status) is achieved by ensuring that the real part of the admittance of an RTD positive. In other words, the stabilizing resistor must be constrained by $R_{sh} < 1/|G_{RTD}|$ for proper circuit operation.

4.5 Double RTD Oscillator Circuits and Layouts

High current density RTDs with sub-micrometer scale are necessary for good performance IC oscillators. However, single RTD oscillators are still limited by the voltage and current differences (ΔV and ΔI) of the discrete diodes. An alternative topology is to integrate multiple RTD elements to increase the available output power without the need for extremely high J_P RTDs. This technique is actually based on combining the RF power of the discrete devices at the port termination. Figure (4.9) shows the circuit configuration with double RTD oscillators. Each single device is individually biased with its own stabilizing circuit.

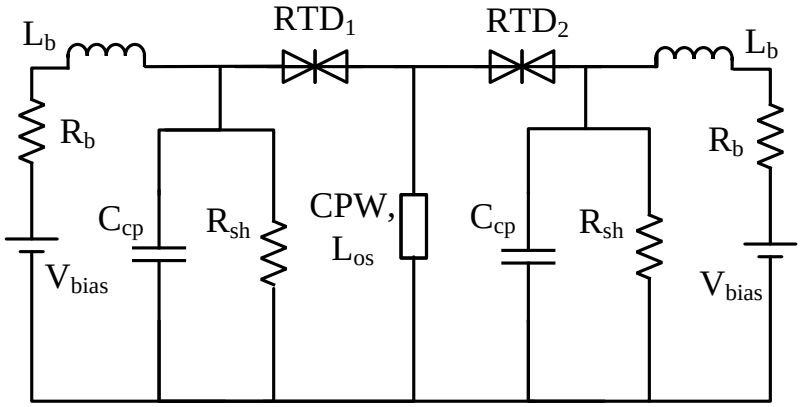


Figure 4.9: Schematic of 2RTDs integrated oscillator, including the stabilizing circuits and parasitic due to the biasing cables.

To maintain the designed operating frequency, the mesa sizes of both RTDs must be the same, necessitating extra care to be taken during the fabrication process. When the

external DC voltage is applied, the CPW acts as a short circuit, allowing a coupling configuration for the RTDs thereby each diode can be separately biased. At the desired frequency, the small signal equivalent circuit is often simplified with the main intrinsic components of the RTDs and inductor of the resonator as depicted in figure (4.10).

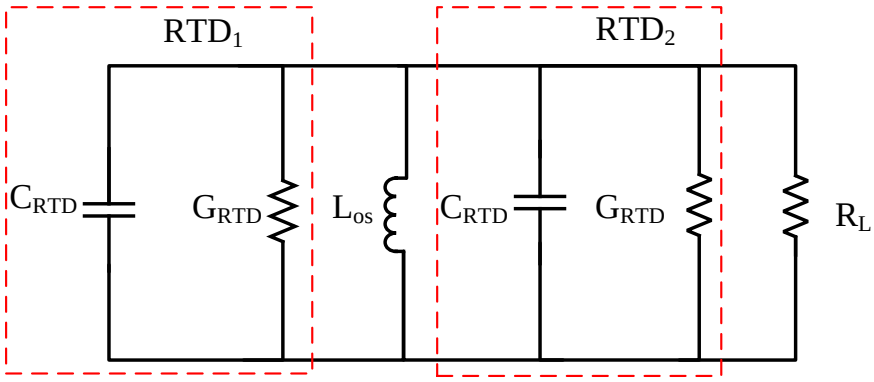


Figure 4.10: Small signal equivalent circuit of the RTD oscillator with 2 integrated elements.

Since two active devices are integrated with a CPW resonator, the oscillation frequency can be rewritten to be:

$$f_{osc} = \frac{1}{2\pi\sqrt{(C_{RTD1} + C_{RTD2})L_{os}}} \tag{2.13}$$

Assuming that the RTDs are identical and their respective capacitances $C_{RTD1} = C_{RTD2} = C_{RTD}$, f_{osc} becomes $1/(2\pi C_{RTD}\sqrt{L_{os}})$. The extracted $G_{RTD}$of each integrated tunneling device is preferred to be half of the load conductance so as to deliver the maximum amount of power to the load ($G_L = G_{RTD}/2$). As the RTD performance is the major underpinning in oscillator's circuit implementation, high current density devices sample XMBE#327 and #302 were chosen. The DC characteristics of those samples are summarized in Table (4.3) and (4.4). The data indicates that a single RTD element from sample #327 with a mesa size of 2×2μm^2 is theatrically able to provide 1.2mW. For sample #302, two integrated devices with power combining technique is needed to provide an equivalent RF power given by the former RTD sample. Nevertheless, both samples are very useful in *mm*-wave/THz regime applications, for example imaging and high wireless data communications, in which the actual distance between a transmitter and receiver ranges from a few centimeters to several meters. The promising results of

the RTDs characterized in chapter two are a great motivator to move forward in demonstrating an RTD oscillator operating in microwave and *mm*-wave frequencies.

TABLE 4.3: DC CHARACTERISTICS FOR RTD SAMPLE XMBE#302 WITH DIFFERENT MESA SIZES AT ROOM TEMPERATURE.

Device Size (μm^2)		|ΔV| (V)	|ΔI| (mA)	$\lvert G_{RTD} \rvert$ (mS)	PVCR	J_P (mA/μm^2)	P_{max} (μW)
Forward Bias	1×2	0.3	4.6	23	2.8	3.7	258
	1×3	0.2	7.9	59	3	3.7	296
	2×2	0.2	10.2	76	3	3.7	382
Reverse Bias	1×2	0.2	7.7	57	2.7	6.4	288
	1×3	0.2	12.9	96	2.7	6.4	484
	2×2	0.2	16.6	124	2.7	6.4	622

TABLE 4.4: DC CHARACTERISTICS FOR RTD SAMPLE XMBE#327 WITH DIFFERENT MESA SIZES AT ROOM TEMPERATURE.

Device Size (μm^2)		|ΔV| (V)	|ΔI| (mA)	$\lvert G_{RTD} \rvert$ (mS)	PVCR	J_P (mA/μm^2)	P_{max} (μW)
Forward Bias	1×2	0.24	17	106	4.8	10.8	765
	1×3	0.2	26.5	209	4.9	10.8	994
	2×2	0.19	33.7	266	4.9	10.8	1200
Reverse Bias	1×2	0.19	22	174	4.2	14.3	783
	1×3	0.16	33.6	315	4.2	14.3	1008
	2×2	0.12	41.4	517	4.2	14.3	931

A mask for 30 and 100GHz oscillators was designed in Keysight-ADS, involving different RTD mesa sizes (i.e. 1×2, 1×3 and 2×2μm^2). The physical length of the CPWs was calculated for each oscillator in accordance with the capacitance of the integrated RTDs and the designed frequency. To effectively balance the trade-off between the stability status of the circuit at low frequency and high-power capability at high frequency, various values of the stabilizing resistors were used. The mask is mainly

constructed of seven steps and an example of the RTD oscillator using a device size of $2\times2\mu m^2$ is depicted in figure (4.11).

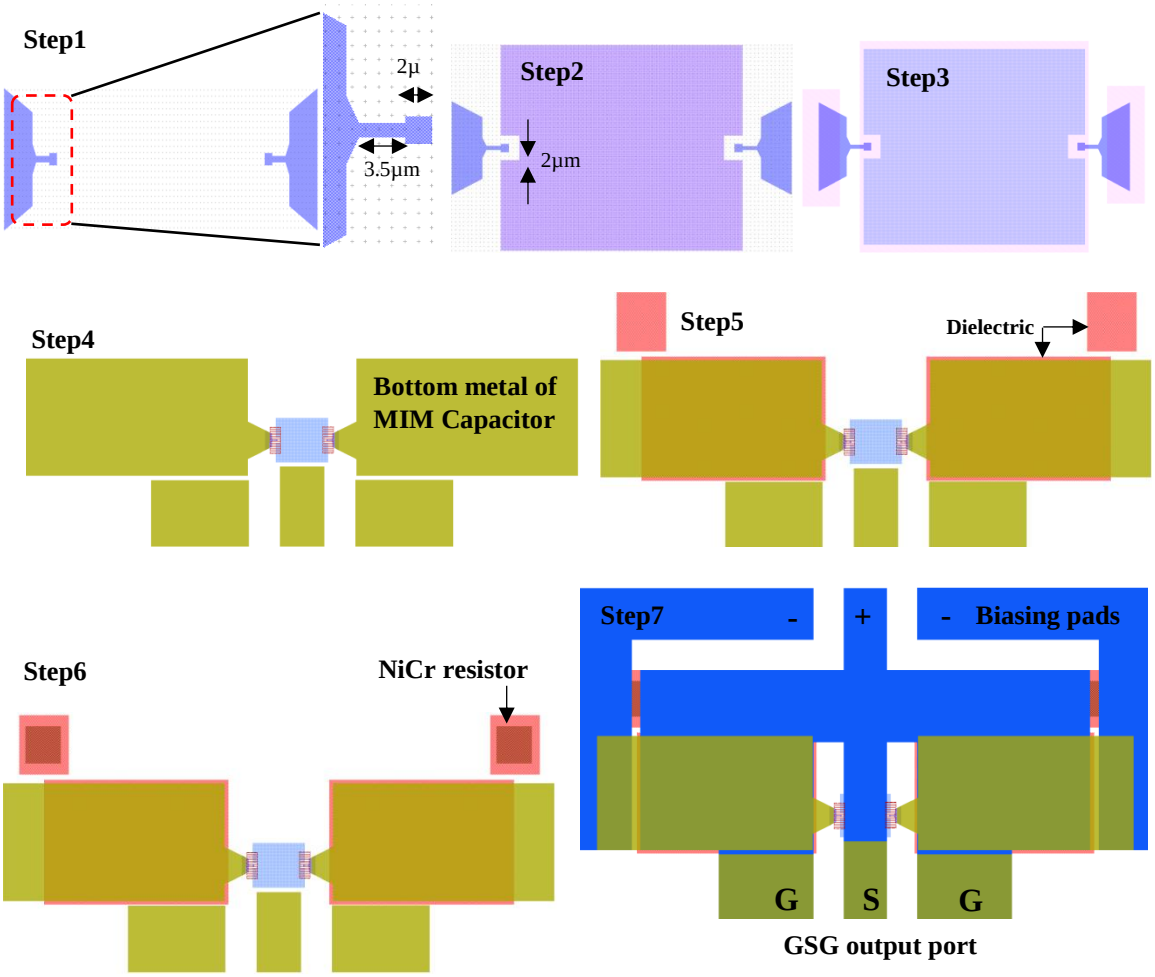


Figure 4.11: Top view of photo-mask designed for 100GHz RTD oscillator showing the process step by step. The RTD size is $2\times2\ \mu m^2$ as defined by the mask pattern.

The basic process of the ICs starts by depositing the collector metal contact, so defining the designed area of both RTDs which can be performed after lifting-off the metallization (step#1). A self-aligned diode mesa is formed using a dry etching process with vertical side walls down to the heavily doped $In_{0.53}Ga_{0.47}As$ cap layer. The emitter metal contact is then deposited with a 2µm spreading distance between the device's epilayer and the bottom contact as shown in figure (4.11) step#2. This allows wet etching of the self-aligned air-bridges and device isolation to be carried out (step#3). As the conventional wet etching does etch the materials in both directions (i.e. vertically and laterally), the defined area of the RTDs was protected to ensure that the active layers of the devices not be etched (step#3). It is important to point out that the undercut profile also occurs

underneath the top pad and bottom contacts of the RTDs, which would contribute to breaking the connection with next overlapped metal step; that is why, these areas were protected (step#3). Up to this stage, each IC is totally isolated from the neighboring devices.

The next step is to perform the bottom metal of the MIM capacitors (step#4). This is followed by sputtering a Si_3N_4 dielectric layer with thickness of 200nm for the capacitors and acts as a platform for the ready thin film resistor (step#5). A NiCr resistor with a thickness of 120nm is required for the 50Ω/□ sheet resistor which can then be sputtered (step#6), facilitating a stabilizing circuit for the integrated oscillators. The final stage (step#7) is the metallization of the CPW resonator and interconnection between the resistor and other components as well as being a top metal for the MIM capacitor. After lifting-off the metal and passivating the active layers of the RTDs and NiCr resistors, the oscillator circuits is then ready to be experimentally tested. In this mask, different dimensions of the stabilizing resistors have been designed ranging from 8 to 18Ω depending on G_{RTD} and mesa sizes of the RTDs. As the oscillator is aimed to operate at 30 and 100GHz frequencies, the values of the coupling capacitors were chosen to be 5 and 20pF respectively.

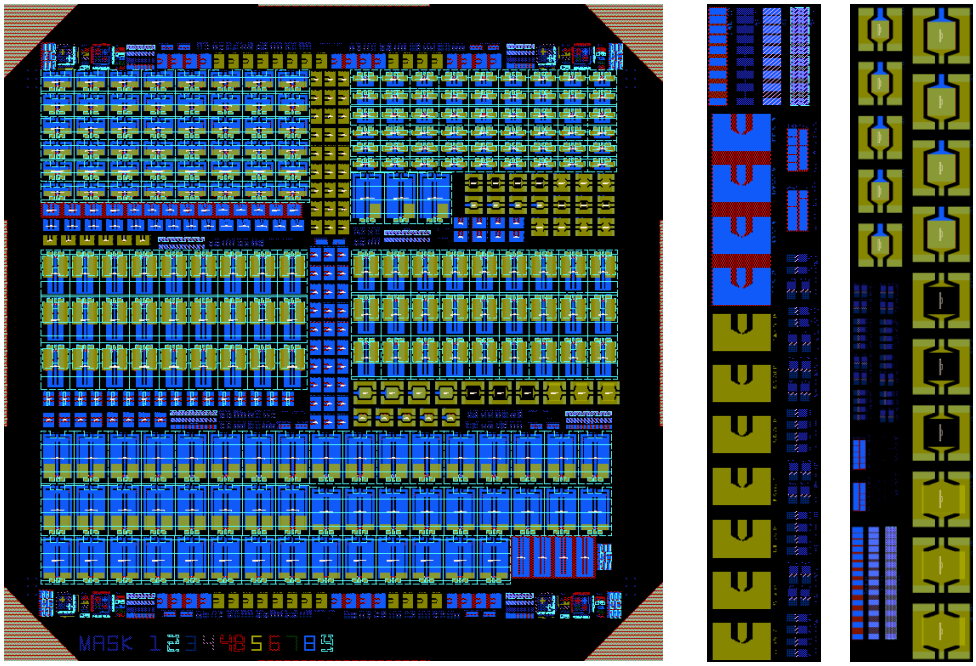


Figure 4.12: Photo-mask for the RTD oscillators designed for this project. Left side: the complete mask with a total area of 13×13mm^2 including the IC of the various oscillators, alignment marks and process control monitoring (PCM). Right side: Close-up view of two PCM cells containing RTDs with different sizes, TLM pads, MIM capacitors and air-bride test.

In the mask design, other than RTDs, capacitors and resistors integrated in the circuits, there are a few discrete components known as process control monitor (PCM) structures as shown in figure (4.12). Such elements are used to test all the components individually, so avoiding any errors in the fabrication process. Furthermore, TLM structures were added to evaluate the quality and uniformity of the RTD's ohmic contact as well as to extract the sheet resistance of the NiCr resistors. Unfortunately, towards the end of this project, the clean room was out of commission due to water flood and the fabrication process had to be delayed. At the time in which the writing up of this thesis was on-going, the experimental results have not been completed yet. However, the research was not interrupted as an alternative approach of an RTD based circuit was investigated for use in microwave frequencies as will be amply presented in the following sections.

4.6 Possibility of Microwave ICs using Tunneling Devices

The unallocated millimeter and sub-millimeter wave regions are becoming more attractive for a wide field of applications, for instance wireless data systems, imaging and security. However, low current density RTDs with a J_P of <2mA/μm^2 are not that beneficial or/and unable to switch well at such an ultra-high frequency. Therefore, the use of those tunneling devices is highly important in integrated circuits particularly those operating in microwave frequency bands, mainly below 30GHz as discussed below. To satisfy the promise of the on-coming Internet of Things (IoT) technology, low-cost high bandwidth electronic chips built in smart phones are becoming indispensable. This technique would be compatible with the 5th generation internet technology planned to start from a low speed of ~6GHz to frequencies reaching 28GHz[218]. A significant challenge in developing an efficient IC is the requirement for a very low DC power consumption. This reflects into a decrease in the temperature of the device and thus allows for no recharge of the battery for many hours.

The potential solution to fulfil this key-factor is to reduce the supply voltage of the circuit; thus, the resonant tunneling diode is a good candidate in realizing a compact, room temperature operation RF amplifiers, transmitters and zero-biased receivers. Accordingly, amplifier-based circuits exploiting an RTD as an active device can be monolithically integrated with the transceiver systems, enabling manufacturability of high-speed quantum-based ICs. To this end, this research is concerned with modeling of an RTD based amplifier operating at frequencies beyond 20GHz.

4.7 Reflection based Amplifiers

The negative differential resistance feature of the RTDs can be utilized to compensate the transmission line losses, resulting in actual gain. This certainly offers the capability of realizing an amplifier without the need of using three terminal devices. The first attempts at making an RTD amplifier was recently demonstrated[73-75] including a report of an integrated RTD with a FET transistor[72]. Basically, there are two main ways to realize an amplifier based RTD; active transmission line amplifier and RF signal reflections-based amplifier. This work focuses on the latter approach as a result of the simplicity of the circuit configuration in which a few components are often sufficient for IC implementations.

A significant minimization in the size and noise performance of the chip is an advantage of the reflection-based amplifiers over the conventional transmission line types. As the name of the amplifier implies, the RF incident signal is reflected suitably terminated ports to ensure high gain at the output node. A related theoretical analysis involving the well-known equivalent circuit of the transmission line and how the losses are cancelled by an RTD active load was presented in chapter one.

4.7.1 Principle of Amplifier Operation

The RTD based amplifier normally incorporate a single bandwidth limit branch coupler and two identical RTDs as shown in figure (4.13). It is important to briefly describe the branch coupler in terms of its principle of operation and some other key factors. First of all, the incoming signal is applied to the input port and is then divided into two equal parts that are 90° out of phase. The amplified signal (due to the negative resistance) is afterwards reflected by the by-pass capacitance, C_{bp}. The signals at the RTD ports can be then combined in phase at output port with 270° phase difference in comparison to the input signal at the input port. Furthermore, the reflected amplified signals are 180° out of phase at the input port and so they cancel each other[219]. In order to eliminate the low frequency parasitic oscillation, a by-pass capacitance is used to act as a short circuit at the unwanted frequencies[152]. The voltage gain of the amplifier is defined by the magnitude of the reflection coefficient between the coupler and RTDs as expresses below:

$$\Gamma = \frac{Z_{RTD} - Z_{out}}{Z_{RTD} + Z_{out}} \tag{4.14}$$

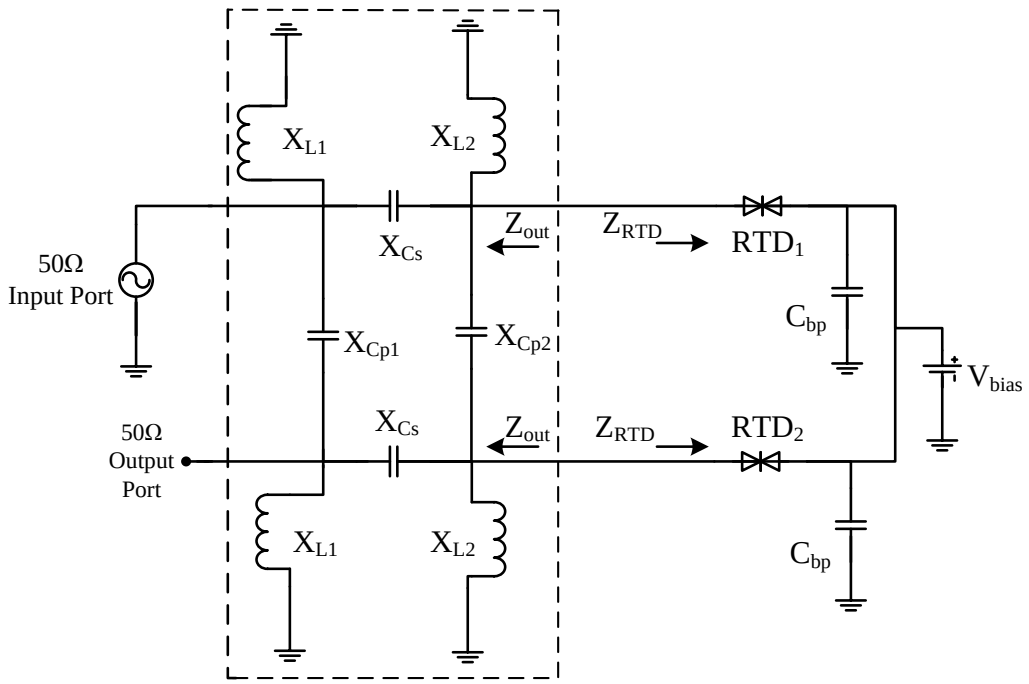


Figure 4.13: Schematic circuit of the reflection-based amplifier model. Dash lines are for the lumped element which represents the single branch coupler.

Due to the two RTDs loaded at the termination of the coupler and operated in their NDR regions, the refection will be larger than 1. The value of these impedances must be almost similar to mitigate losses caused by mismatching effect. The motivation in realizing the reflection-based amplifier configuration is that there is no need for a bulky matching circuit. The reason is mainly attributed to the fact that the output impedance of the lumped element coupler is component values dependent. To do this, the components of the coupler can be optimized to match Z_{RTD}. A lumped element based single branch coupler was previously reported for MMIC applications[220]. At microwave frequencies, it is more common to realize this type of coupler using simple interconnected length of transmission lines

4.7.2 Modeling of Lumped-Element Coupler

Practically, a branch-line coupler is basically composed of four microstrip lines, their lengths are one-quarter wavelength at the desired frequency and two of which have the same characteristic impedance of the input and output ports. The impedance of other ports are commonly formulated as $Z_o/\sqrt{2}$[143, 185]. To characterize a branch-line coupler, two key features are required to be considered: coupling factor and directivity as expressed by[221]:

$$CF = 10log\frac{P_1}{P_3} \tag{4.15}$$

$$D_{coupler} = 10log\frac{P_3}{P_2} \tag{4.16}$$

P_1 being the input power to port1, whereas P_2 and P_3 are the output power from port 2 and 3 respectively. The coupling factor should be 3dB to provide even power split between port 3 and 4 and decent couplers have a directivity of 30-35dB, which is important to ensure that the output power at port 2 is trivial compared to port 3[221]. To examine a coupler response, a model was realized in Keysight-ADS employing ideal transmission lines with an operating frequency of 25GHz as shown in figures (4.14).

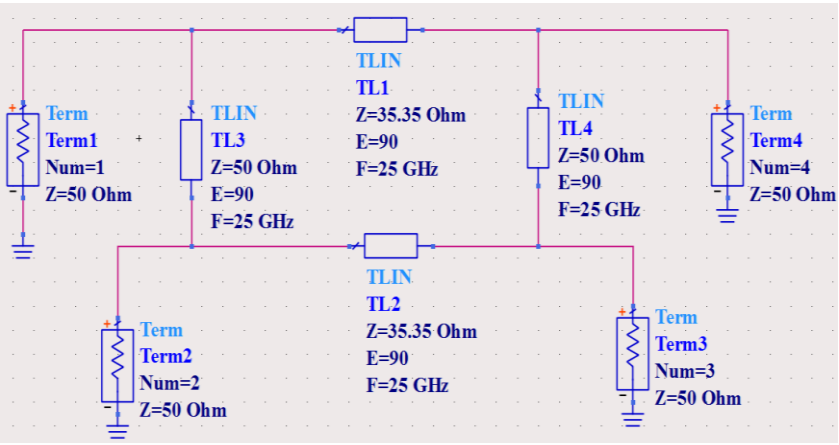


Figure 4.14: Single branch coupler built in Keysight-ADS with ideal transmission lines.

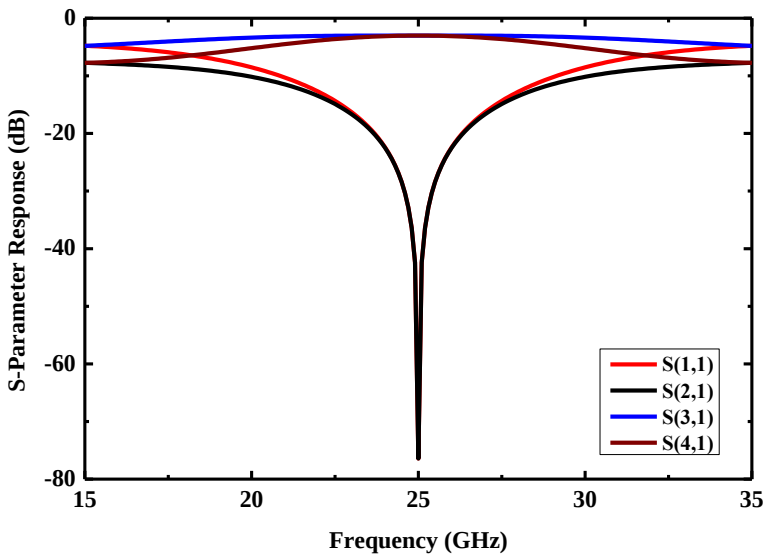


Figure 4.15: S-parameters simulation result of single branch coupler modeled in ADS using ideal transmission lines at 25GHz.

As each stub should give $\pi/2$ phase shift for proper coupler operation, the electrical length was set to be 90°. The simulation results reveal that the input power is evenly split at ports 3 and 4 over a fairly narrow range of frequencies with a center operating frequency of 25GHz, providing large bandwidth as depicted in figure (4.15). The performance of the reflection at port 1, S_{11} and the power received at port 2, S_{21} is excellent as they both are much less than -10dB. In practice, it is rather difficult to achieve such findings due to the impact of the losses and parasitics neglected at this stage. Moving forward to the actual circuit configuration, the coupler was modeled by LC passive elements as shown in figure (4.16). These integrated elements are carefully tuned to obtain ~3dB coupling factor with a directivity of > 30dB.

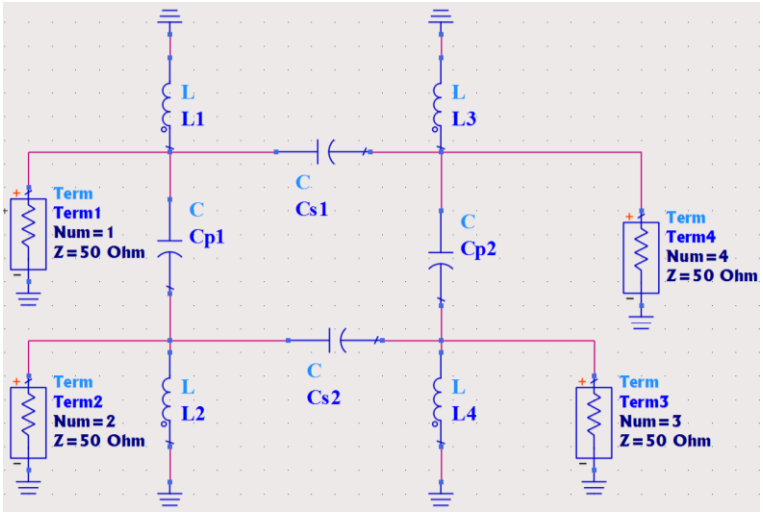


Figure 4.16: ADS model of a single branch coupler using lumped element operating at 25GHz.

As clearly indicated in figure (4.17), the performance of the coupler is moderately comparable to the first one built using ideal transmission lines. The coupling factor and directivity can be calculated from the S-parameter responses using the formula $CF = |S_{31}|$ and $D_{coupler} = |S_{31} - S_{21}|$ respectively. These crucial parameters were evaluated to be 3.1 and 57dB at the operating frequency, contributing to an outstanding performance for the coupler's circuit. This was achieved by the excellent result obtained; S_{11} and ports isolation (S_{21}), both of which have a response much lower than -10 dB at 25GHz and the 3dB power split S-parameters (S_{31} and S_{41}) was accomplished for the branch coupler. It was found that the values of the lump elements are relatively small and can be mathematically estimated from:

$$X_{Cs1} = X_{Cs2} = \frac{Z_o}{\sqrt{2}} \tag{4.17}$$

$$X_{Cp1} = X_{Cp2} = Z_o \tag{4.18}$$

$$X_{L1} = X_{L2} = X_{L3} = X_{L4} = \frac{Z_o}{2.41} \tag{4.19}$$

Note that these equations are only valid when all ports have 50Ω characteristic impedances.

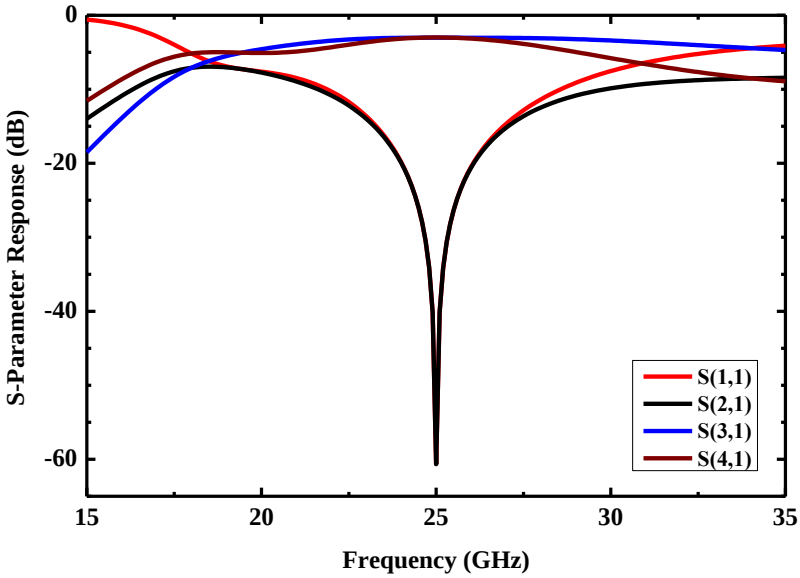


Figure 4.17: S-parameters simulation result of a single branch coupler modeled in ADS using LC lumped-element operating at 25GHz.

The dimensions of the coupler chip are scaled down in size with frequency because of the decrease in the LC component values. This is generally preferred up to a certain frequency, in which the unavoidable parasitics are much smaller than actual circuit components. Beyond this point, a coplanar waveguide based directional coupler would be required. Alternatively, a multilayer MMIC coupler is indispensable as was demonstrated for wide-band amplifier up to 60GHz[222]. Such a feasible approach might be useful to experimentally investigate the coupler performance in the future. The next step is to focus on designing the whole amplifier circuit and studying whether it can support high gain and required functionality.

4.7.3 RTD Amplifier: Simulation Results and Discussion

The main objective in this section is to model a novel K-band reflection-based amplifier utilizing the NDR advantage of double barriers InGaAs/AlAs RTDs. The device sample XMBE#277 with 1×2.4μm^2 mesa area was used because of its low current density of

0.26mA/μm^2. This is primarily to ensure low dc power consumption characteristic while maintaining high gain at the output port. The measured forward I-V characteristics of the diode alongside its junction resistance (R_{RTD}) is depicted in figure (4.18).

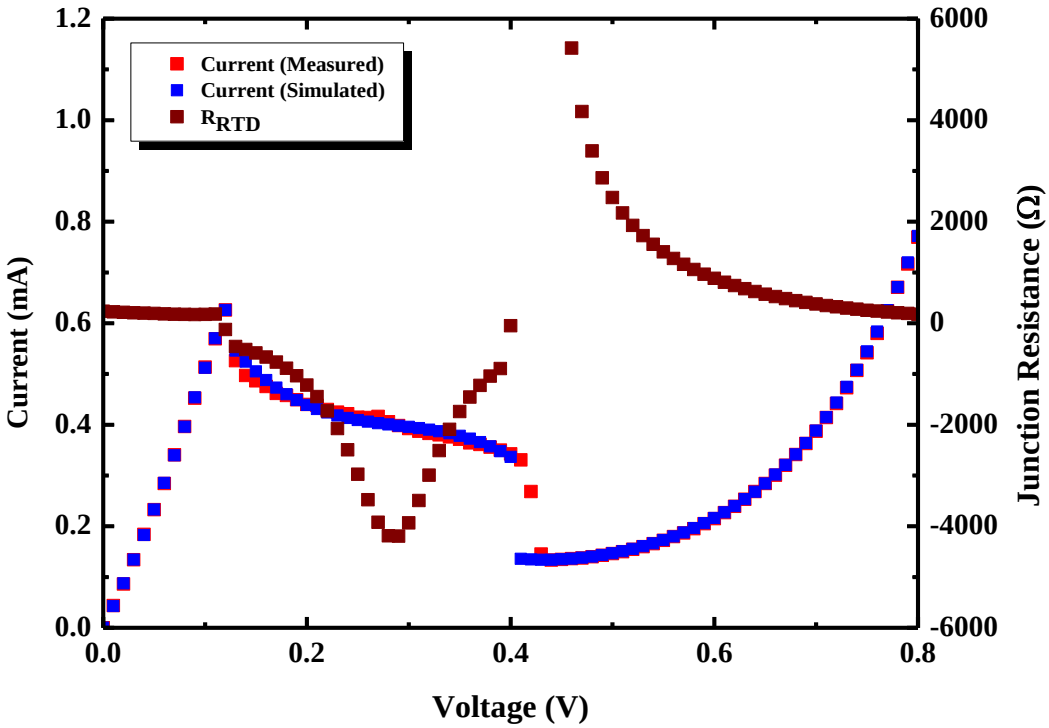


Figure 4.18: Forward I-V characteristic (measured and simulated) and junction resistance of the InGaAs/AlAs RTD device sample XMBE#277 with a mesa area of 1×2.4μm^2.

For the sake of simplicity, the RTD was represented exploiting SDD2P block with polynomial equation in parallel with the junction capacitance of the device, C_{RTD}. This is to realize the RTD in Keysight-ADS as well as to extract the modeled R_{RTD}, obtained by $R_{RTD} = \partial V/\partial I$. The measured and simulated data show an excellent agreement as depicted in figure (4.18). Though the total resistance of the diode is equal to $R_{RTD} + R_s$, the series resistance is very small in comparison with R_{RTD} ; hence it was neglected. The device provides a negative resistance over the entire NDR feature, reaching nearly -4000Ω in the middle of the region. Validation of the equivalent circuit of the device has been verified using a fitting model with the measured scattering data. The junction capacitance of the RTD sample #277 was accurately extracted to be 6fF/μm^2 as discussed in chapter two. The actual S_{11} of the intrinsic device (i.e. after de-embedding the surrounding parasitics of the pads) is found outside the unit circle of the Smith chart ($|S_{11} > 1|$) or in other words, it is >0dB in x-y graph, implying that the reflected power

is greater than the incident ones as shown in figure (4.19). This is due to the negative resistance of the RTD, emphasizing that the device is able to generate a power within the measured frequencies.

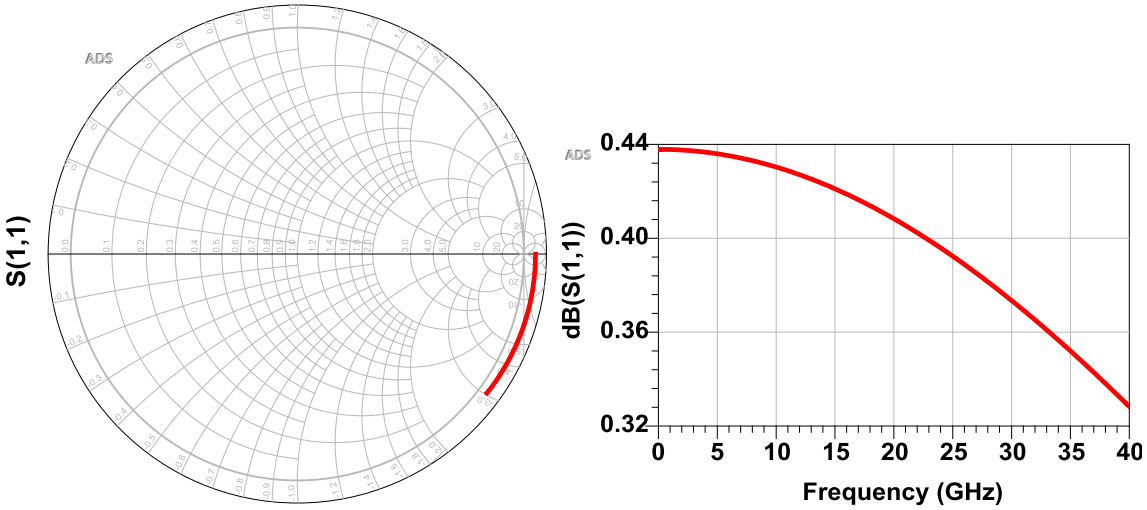


Figure 4.19: Left and right sides: measured S_{11} for intrinsic device sample #277 with a mesa area of $1\times2.4\mu m^2$ biased in the NDR region plotted in smith chart and x-y graph respectively.

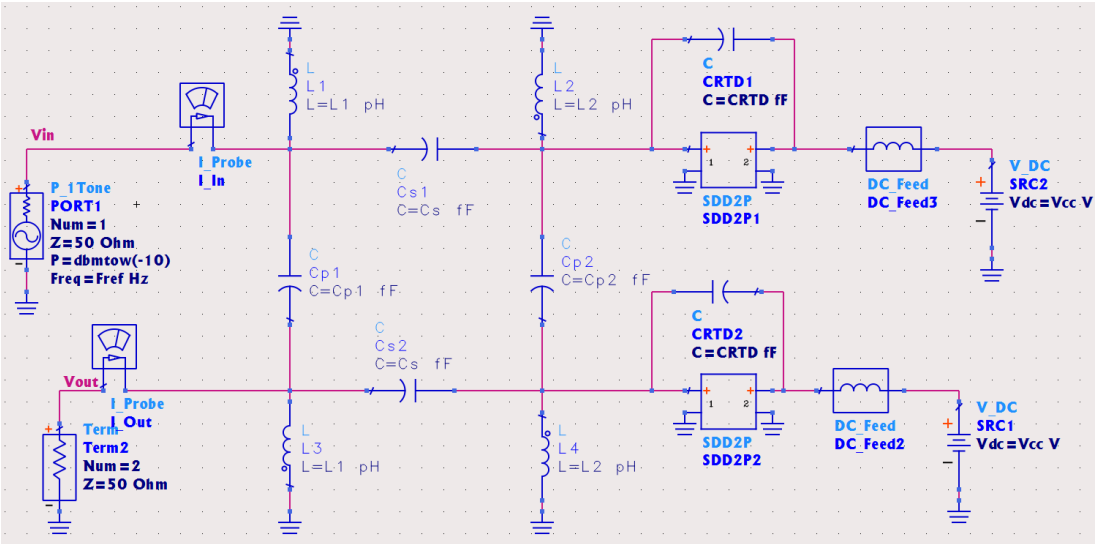


Figure 4.20: An ADS amplifier model of a reflection-based amplifier showing two integrated RTDs with lumped-elements coupler.

Since the input impedance of the RTD used does not match with the standard 50Ω, the lumped-elements of the coupler had to be optimized. The inductance of the coupler is in the range of 200-380pH, while the capacitance is between 30 and 125fF for effective operation of the circuit. According to the extracted parameters of the coupler and RTD,

both circuits were incorporated to realize a reflection-based amplifier as depicted in figure (4.20). In this work, harmonic balance simulation tool was exploited to simulate the circuit. Strong evidence for the proper operation of the amplifier was found from the achieved high-power gain of 32 dB at 25.3GHz as shown in figure (4.21). The RTDs were both biased in the NDR region, at 0.32V with bias current of about 0.4 mA corresponding to a low dc power consumption of 256µW. The key FOM (figure of merit) for low power RF applications is gain in dB over dc power consumed (in mW) in integrated circuit. Owing to a promising FOM of 125dB/mW, such a quantum-based amplifier is considered very attractive and feasible for RF applications with low dc power consumption.

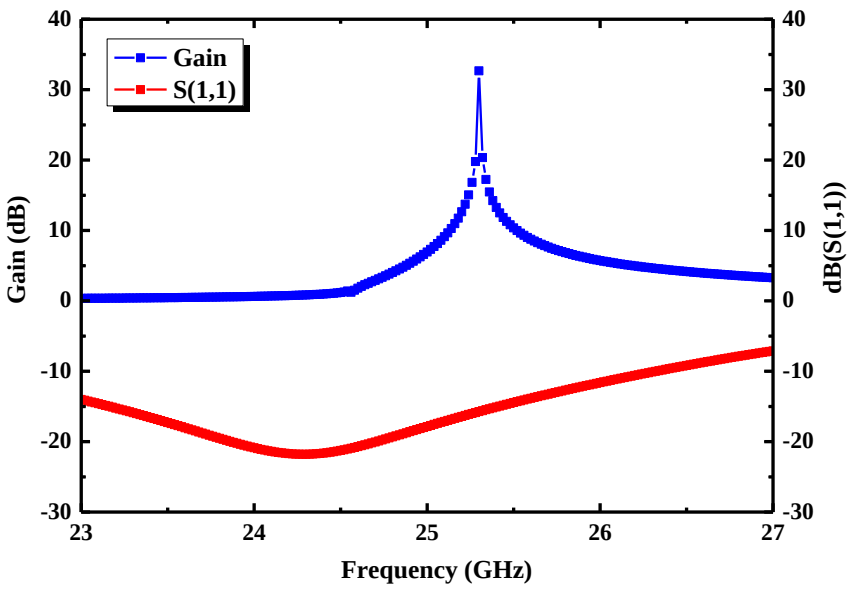


Figure 4.21: Simulated gain and return loss of the amplifier using RTD sample #277 with mesa area of $1\times2.4\mu m^2$. The two identical diodes are biased at 0.32V and the obtained reflection coefficient was between the 50Ω input port and the coupler.

Power gain dependent voltage bias were also studied to further examine the effect of variation in the resistance of the RTDs on such transmission characteristic as shown in figure (4.22). The simulated results indicate that the gain vanishes at an external voltage close to the peak and valley voltages, confirming that the performance of the amplifier strongly relies on the absolute value of the negative resistances. Nevertheless, the gain is relatively flat from 0.2 to 0.4V giving a comfortable process window for the circuit's operation.

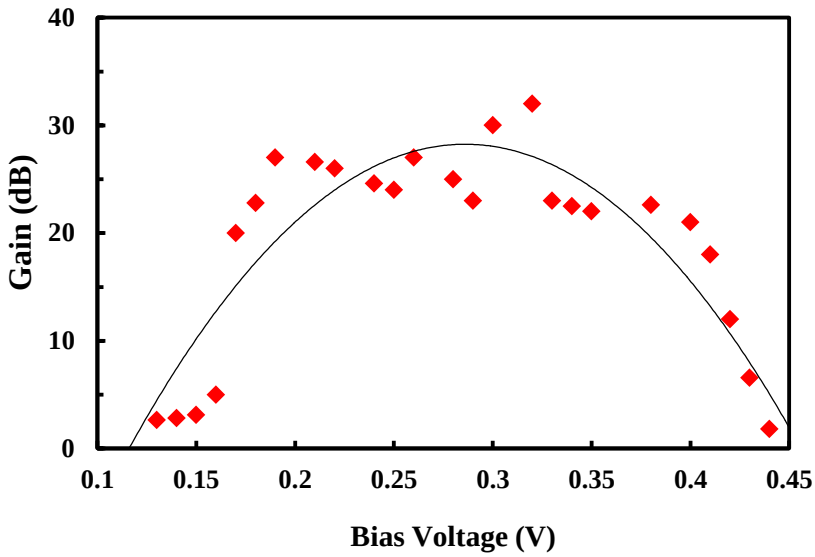


Figure 4.22: Simulated transmission gain of the amplifier versus the applied bias voltage, which was varied over the entire NDR region.

TABLE 4.5: COMPARISON OF RADIO FREQUENCY AMPLIFIERS BASED TUNNELING DEVICES AND OTHER TECHNOLOGIES.

REPORTED IN	TECHNOLOGY	FREQUENCY (GHz)	GAIN (dB)	DC POWER CONSUMPTION (mW)	FOM (dB/mW)
[223]	Two FET transistors incorporated one coupler	6.2	8.1	N/A	N/A
[224]	0.25μm GaN multiple transistors	10	27	750	0.036
[225]	180nm CMOS LNA	5	10.2	0.8	12.8
[226]	130nm CMOS LNA	5.1	10.3	1.03	10
[152]	Reflection based amplifier with 0.8μm^2 RTD	5.7	11.5	0.47	24.5
This work	Reflection based amplifier with 2.4μm^2 RTD	25.3	32	0.256	125

A comparison between the works demonstrated using tunneling devices and other technologies is tabulated in Table (4.5). As the two terminal tunneling devices are able to

provide a gain with rather low power consumption in comparison with transistor-based circuits, the usefulness of such a compact, low cost manufacturing and room temperature operation IC is significant.

4.8 Summary

Electromagnetic modelling of double barriers InGaAs/AlAs RTD sample #230 have been carried out using 9μm^2 mesa devices with a peak current density of 1.2mA/μm^2 integrated with a coplanar waveguide resonator. A 100 GHz oscillator was realized and achieved an output power of 100μW through exploiting the negative differential resistance feature of the diode. The RTD oscillator reported here gives a potential power output of 30 μW at 133 GHz. The circuit modelling was performed using advanced design system software. To ensure practical circuit's performance, all parasitic elements associated with the passive components were taken into account. The influence of the stabilizing resistance on the extracted power was also investigated and it was found out that the extracted power increases with the stabilizing resistor values and constrained by the factor $R_{sh} < 1/|G_{RTD}|$.

Modeling and theoretically analysing of a novel K-band reflection-based amplifier was performed utilizing the NDR feature of the InGaAs/AlAs RTD. A 2.4μm^2 mesa area device was fabricated and measured and on-wafer probe S-parameter measurements up to 40GHz were carried out. Verification of the diode's equivalent circuit was experimentally validated and then employed to realize a K-band reflection-based amplifier. The model was realized including a lumped element branch coupler with two active loads RTDs. Due to constructively combining the in- phase electromagnetic waves at the amplifier's output port, a high gain of 32 dB was achieved at 25.3GHz while maintaining a very low DC power consumption of 256μW. This corresponds to a record figure of merit of 125dB/mW to date, validating the excellent performance of the amplifier. Since the power gain of the amplifier relies on the absolute value of the negative resistances, the simulated results revealed that a relatively flat gain was achieved from the peak to valley voltages offering a comfortable window for IC operation.

CHAPTER 5: III-V HBT TRANSISTORS AND PIN-PD: FUNDAMENTALS AND THEORY OF OPERATIONS

5.1 Introduction

A major part of this research on high speed devices is concerned with the design of an InP/InGaAs based photoreceiver. The backgrounds and state of the art performances of InP based heterojunction bipolar transistors (HBT) and PIN-photodiode are covered in this chapter. Firstly, HBT's DC and RF operating principles and figures of merit are discussed, for example I-V curves of a common emitter transistor, Gummel plots and unity current gain cut-off frequency. A comparison between HBT technology and conventional BJTs in terms of capability of high-speed operation with much less relaxed feature sizes is also discussed.

Additionally, chapter five presents an overview of the most common parameters of the PIN-diodes. This involves an associated discussion describing the device's structure and its band diagram besides briefly highlighting the material systems used in growing such photodiodes.

5.2 Primer on Homojunction Bipolar Junction Transistors

The bipolar junction transistor, BJT is a three-terminal electronic device, composed of two back-to-back unified PN-junctions. The three semiconductor layers making up the transistor are known as emitter, base and collector, where the doped base layer is sandwiched between the other two opposite polarity layers. The most commonly used BJT type is the NPN structures, in which the base is doped with p-dopant, while the emitter and collector are doped with n-dopants. The reason is simply attributed to the high mobility of electrons in the base region, resulting in high-speed device operation. The primary electron conducting carriers are emitted by the emitter and pass through the base region until they are collected by the collector[227]. In a homojunction BJT, all three regions of the transistor are basically made of the same semiconductor material. Several configurations can be realised in the transistors, however the common emitter

(CE) configuration is the most often preferred topology due to its ability to amplify both current and voltage signals. This terminology is due to fact that the emitter output side of the circuits are connected to ground[227].

The following analysis of a CE BJT is discussed first to set the scene for further enhancement made possible by the HBT itself. For moderate transistor gain, the emitter is heavily doped, followed by a lower doped base and a much lower doping in the collector region. In the active mode of operation, the emitter-base (EB) junction is forward biased, enabling a large number of electrons to be injected into the base layer. These electrons become minority carriers in the base due to the majority p-type dopants, contributing to the occurrence of some recombination process. This event can be mitigated by growing a thin base layer with a thickness that is much smaller than the diffusion length of the electrons. The residual carriers would then diffuse across the base width due to an electrostatic field caused by a concentration gradient. When the electrons reach the edge of the depletion region of the reversely biased base-collector (BC) junction, they are accelerated across the wide depletion region by the applied electric field and will be then collected in the collector layer[227].
The relatively small amount of the input voltage (BE-voltage) can lead to very large induced changes in the collector current because of the exponential dependence between them. This indeed leads into achieving a current gain, making the transistors one of the most valuable electronic devices[228]. However, there are a few undesirable mechanisms that have detrimental impacts on the gain of the BJT as summarized by[229]:

1. Recombination of the injected electrons from the emitter with the holes, either in the base layer or in the forward biased EB space charge region, introducing two small currents I_r and I_s respectively.
2. The reverse injected holes from the p-type base region into the emitter provides a hole current of I_p.
3. Due to the reverse biased BC junction, a small thermally generated e-h pairs causes a number of holes to be swept into the base from the n-type collector region, giving rise to a small current, I_{CBO}.

Figure (5.1) depicts the schematic drawing and energy band diagram of an NPN-BJT, showing the contribution of these currents. The currents of the emitter, base and collector terminals can be expressed as:

$$I_E = I_n + I_p + I_s \tag{5.1}$$

$$I_C = I_n - I_r + I_{CBO} \tag{5.2}$$

$$I_B = I_p + I_r + I_s - I_{CBO} \tag{5.3}$$

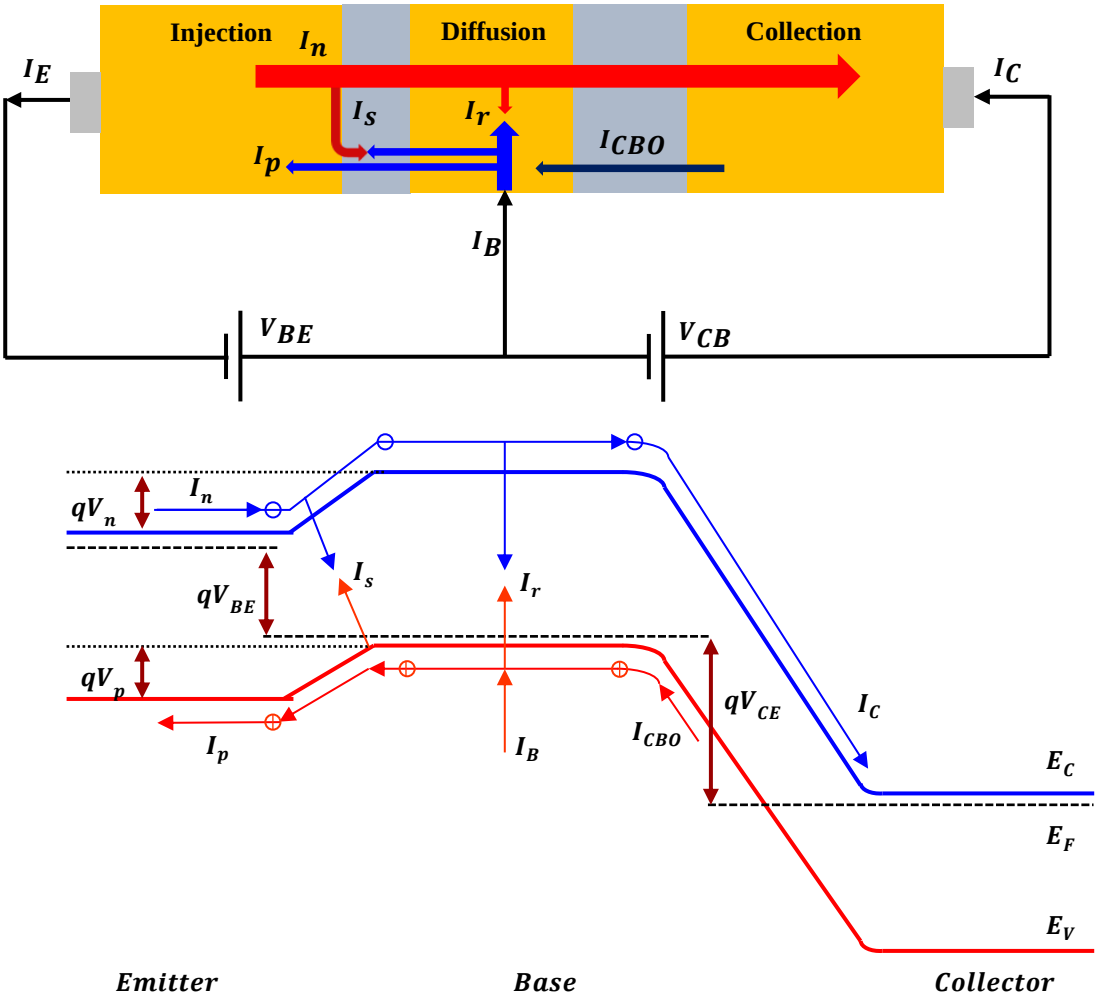


Figure 5.1: Schematic drawing and energy band diagram of an NPN homojunction bipolar transistor, showing (in red) the mechanisms that have detrimental impacts on the gain of the device.

The well-known figure of merit for common emitter BJT is the current handling capability or current gain, β which is formulated as:

$$\beta = \frac{I_C}{I_B} = \frac{I_n - I_r + I_{CBO}}{I_p + I_r + I_s - I_{CBO}} \tag{5.4}$$

Since the base width, W_b is often grown to be approximately one tenth of the electron diffusion length, the impact of the recombination events in the base layer can be safely ignored (i.e. $I_r \simeq 0$). Beside this, I_p is typically $\gg I_s$ and the thermally generated I_{CBO} is trivial, so both can be neglected in the following analysis[230]. The emitter injection efficiency is defined as the ratio of the electron injected current from the emitter to the total emitter current as expressed by:

$$\gamma_e = \frac{I_n}{I_n + I_p} \tag{5.5}$$

The maximum current gain, β_{max} can be theoretically achieved by further reduction in the minor leakage currents.

$$\beta_{max} = \frac{I_n}{I_p} \tag{5.6}$$

To evaluate β_{max}, the electrons and holes injection current densities, J_n and J_p expressions based on the Boltzmann's approximation are used[231]:

$$J_n = N_D v_{nb}\, exp\left(\frac{-qV_n}{kT}\right) = \frac{qN_D D_n}{W_b} exp\left(\frac{-qV_n}{kT}\right) \tag{5.7}$$

$$J_p = N_A v_{pe}\, exp\left(\frac{-qV_p}{kT}\right) = \frac{qN_A D_p}{W_e} exp\left(\frac{-qV_p}{kT}\right) \tag{5.8}$$

N_D, N_A are (assumed) uniform doping levels in the emitter and base respectively and v_{nb} and v_{pe} are the mean speeds, due to the combined impacts of both drift and diffusion, of electrons at the emitter-end of the base, and of holes at the base-end of the emitter respectively. D_n and D_p are the diffusion coefficients of the minority carriers in the base and emitter and W_b and W_e are the width of the base and emitter respectively. V_n, V_p, k, T and q are the barrier to electrons and to holes, the Boltzmann's constant, temperature in Kelvin and charge of electron respectively. Therefore β_{max} can be rewritten to become:

$$\beta_{max} = \frac{I_n}{I_p} = \frac{N_D D_n W_e}{N_A D_p W_b} exp\left(\frac{q(V_p - V_n}{kT}\right) \tag{5.9}$$

For homojunction transistors, the barrier to electrons and to holes is similar (i.e. $V_p - V_n = 0$) because the epitaxial layer is made up from the same semiconductor material, β_{homo} is then given by:

$$\beta_{BJT} = \frac{N_D D_n W_e}{N_A D_p W_b} \tag{5.10}$$

Evidently, equation (5.10) reveals that the common emitter gain of a homojunction transistor is predominantly determined by the thickness and doping concentration of the emitter and base. With this in mind, much higher doping of the emitter than the base with an extremely thin base layer is the only viable option that would be utilized to maximize the gain through allowing more injected electrons to arrive at the collector region. This helps to enhance the emitter injection efficiency due to a reduction in the number of the reverse injected holes from the base into the emitter. However, low base doping profile can lead to degradation in DC and RF performance of the device. This is due to the resulting large sheet resistance, from which a low cut-off frequency and a low early voltage would be the consequences[232]. Furthermore, a heavily doped emitter results in an increase in the EB-depletion region capacitance, limiting the high-frequency operation of the transistor.

5.3 Heterojunction Bipolar Transistors

Heterojunction bipolar transistors (HBTs) are grown with dissimilar semiconductor materials. In general, the emitter is constructed from a larger band gap material than the base, facilitating to further reduce the injected minority carriers from the base into the emitter and hence, improve the emitter injection efficiency. This then leads to the possibility of doping the base to a much higher level than the emitter (in contrast to BJTs) which is, of course, preferred for lower contact and sheet resistances and hence allows for very high-frequency performance. Unlike homojunction transistors, in a well-designed high gain HBT, the interface recombination current in the forward space charge region, I_s can be as small as $I_n/10^3$ and I_n should be much larger than the bulk recombination current in the base layer, I_r[233]. As stated in[234], I_r density is given by:

$$J_r = \gamma n_e(0) \frac{W_b}{\tau_n} \tag{5.11}$$

$n_e(0)$ and τ_n being the injected electron concentration at the emitter-end of the base and the average electron life-time in the base. γ is a factor between 0.5 and 1 indicating how much electron concentration in the base differs from the electron concentration at the emitter-end of the base hence the current gain of an HBT is written as:

$$\beta = \frac{1}{\gamma}\frac{\upsilon_{nb}\tau_n}{W_b} \tag{5.12}$$

In 1970, Ladd *et al* investigated the impact of the doping concentration on the minority carriers' lifetime, deducting that the electrons' life time in the base decreases with increase in the doping profile[235]. As long as the carriers' lifetime is still equal or lower than 10^{-10} sec, no significant gain reduction is noticeable and this can be maintained by keeping the base thickness to 1000Å or less, avoiding electron-hole recombination events[234]. Carrier transport in an HBT does have two types of diffusion-based processes across the junctions due to the existence of the heterointerfaces. This largely depends on the energy band diagram of the emitter-base heterojunction and these are presented in the following sections.

5.3.1 Abrupt Emitter-Base Interface

In the abrupt interface HBTs, discontinuities are basically introduced at the emitter-base interface as depicted in figure (5.2). The major disadvantage in such a structure is that a prominent notch, ΔE_c is created in the conduction band between the emitter and base, resulting in accumulating the injected electrons, thus, increasing the recombination losses (i.e. degrading the gain of the device). Additionally, the potential spike, ΔE_B causes an increase in the required voltage bias, V_{BE} by the order of $\Delta E_B/q$ for a given current density. This leads to an increase in the offset voltage of the transistor as will be discussed further in this chapter. On the basis of this consideration, equation (5.9) can be rewritten to become:

$$\beta_{HBT} = \frac{N_D D_n W_e}{N_A D_p W_b} exp\left(\frac{\Delta E_g - \Delta E_B}{kT}\right) \tag{5.13}$$

Where $q(V_p - V_n) = \Delta E_g - \Delta E_B$, since the notch depth is small compared with kT, $\Delta E_B = \Delta E_C$ and $\Delta E_g - \Delta E_C = \Delta E_V$ and this yields:

$$\beta_{HBT} = \beta_{BJT}\, exp\left(\frac{\Delta E_V}{kT}\right) \tag{5.14}$$

β_{BJT} being the current gain of a common emitter bipolar junction transistor as well as ΔE_C and ΔE_V representing the conduction and valance band discontinuities respectively.

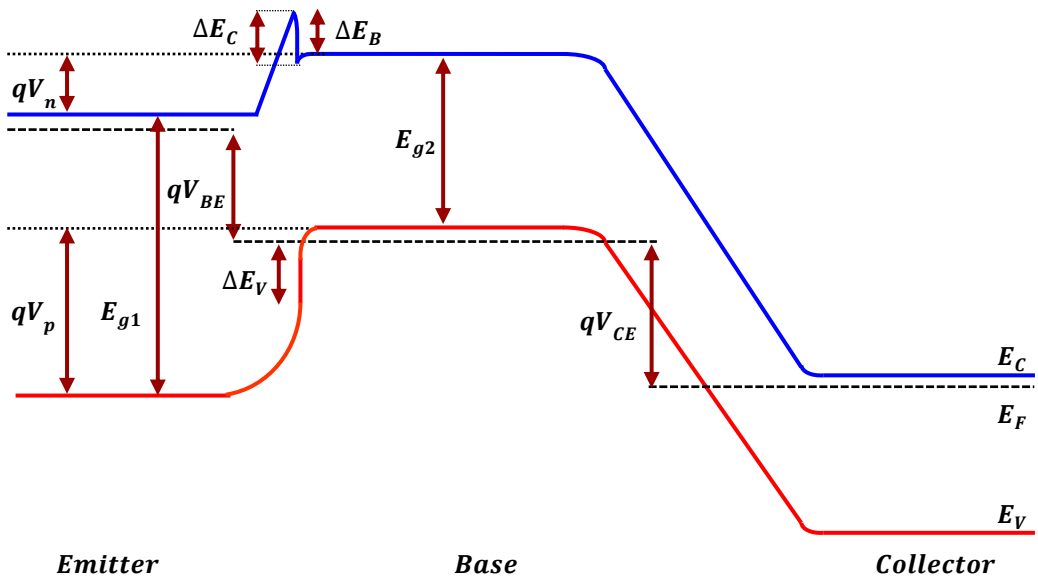


Figure 5.2: Band Diagram of a wide bandgap emitter Npn-HBT, showing the barrier potential spike.

Despite the disadvantage of the potential spike, it acts as a ballistic "launching ramp" for the electrons in the conduction band. As a result, the carriers that overcome the barrier go into the base region with significantly higher kinetic energy that could be for the homojunction structures. This helps to improve the ballistic transport of the carriers across the base, from which the electron velocity would reach 10^8cm/s favored for high-frequency response[234].

5.3.2 Graded Base-Emitter Interface

The increase in the offset voltage due to the potential spike can be remedied by exploiting a graded emitter-base interface structure. This is simply composed of a compositionally graded wide gap emitter layer, yielding a smooth monotonically varying bandgap edge. Figure (5.3) shows the band diagram of a smooth emitter-base heterointerface and thus, equation (5.9) can be modified to be[234]:

$$\beta_{HBT} = \frac{N_D D_n W_e}{N_A D_p W_b}\, exp\left(\frac{\Delta E_g}{kT}\right) \tag{5.15}$$

Note that: $q(V_p - V_n) = \Delta E_g$, where ΔE_g is the difference of energy band gaps of emitter and base.

$$\beta_{HBT} = \beta_{BJT}\, exp\left(\frac{\Delta E_g}{kT}\right) \tag{5.16}$$

However, a graded emitter HBT has relatively slower electron transport properties than the heterostructures based abrupt interfaces. The reason is due to the fact that there is a lack of electron ballistic characteristics. To compromise this trade-off, an alternative approach was demonstrated by Kurishima *et al*, in which the effect of a compositionally-graded InGaAs base layer was experimentally studied[236]. This approach is to introduce a built-in field in the base region, providing an enhancement in current gain and high-frequency performance in comparison with the conventional uniform band gap base HBTs.

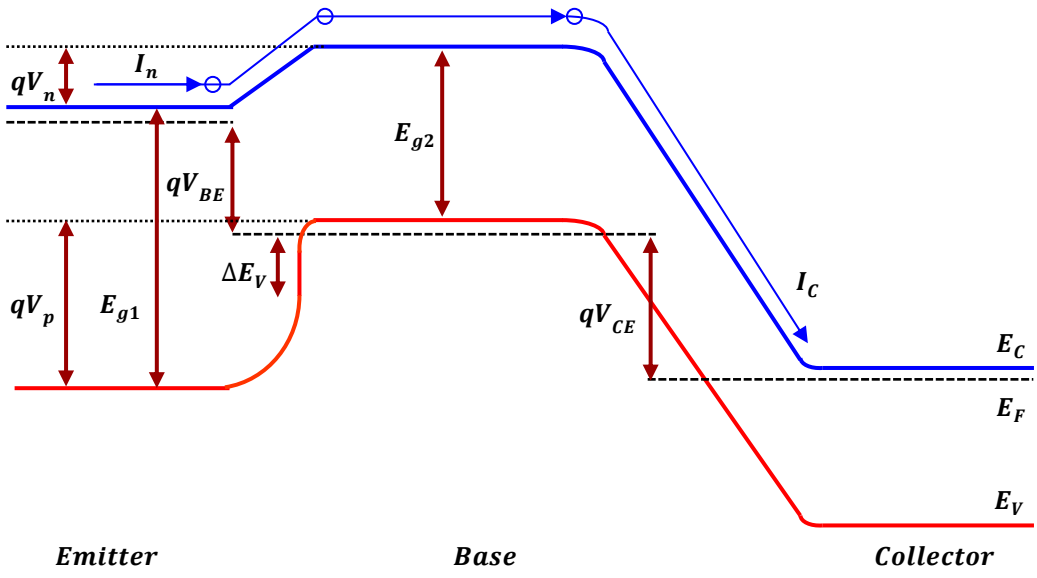


Figure 5.3: Band Diagram of a graded heterojunction bipolar transistor.

5.3.3 Advantages of HBTs over Other transistor Technologies

HBT technology has some prominent advantageous over silicon BJTs, which can be stated as:

1. The emitter injection efficiency is vastly improved as a consequence of introducing the large hole barrier in the valence band.

2. The lower base resistance leads to much better high-frequency performance due to the ability of heavily doping the base without sacrificing the current gain.
3. The large emitter energy band-gap assists to transistor to operate at higher temperatures compared with bipolar devices.
4. Since the voltage drop in the emitter-base region is low in HBTs, less amount of current crowding might be exhibited in the emitter.

In comparison with a GaAs or InP-based field effect transistors (FETs), heterojunction bipolar devices have high transconductance thereby higher early voltage, higher current density, less $1/f$ noise and are unrestrained from sub-micrometre scale requirements[230]. For HEMT transistors, the output current is quadratically proportional, in the best case, to the input voltage. In contrast, these input and output parameters have an exponential relationship in HBT devices. As reported in[237], for a 2µm emitter width HBT transistor with a current density of 0.5mA/µm^2, the transconductance reaches 40S/mm while it is ~1S/mm for an InAlAs-InGaAs HEMT whose total supply and spacer thickness is 200Å. This highlights the high gain feature of heterojunction devices.

The turn on voltage of the HBTs relies on several factors, such as the doping profile and band gap of the material used, making their characteristics unaffected by variations in the fabrication process. This significantly increases the yields and reliability of large-scale ICs, in which integration of hundred thousands of transistors per chip is required. By contrast, the dependency of the HEMTs threshold voltage on processing parameters such as supply layer thickness would produce severely varying threshold voltage values across a wafer, giving a rise to difficulties in achieving matched devices[98]. In addition to this, the effective area of HEMT devices is calculated by the product of the gate width and channel thickness and because of the limitation in the increase of the channel thickness, this result in requirements for wide gates to accomplish high current handling capacity. This implies that a single HBT transistor occupies an area of approximately three times less than a HEMT for the same operating current values[98].

5.3.4 HBT Material Systems

For Npn HBT transistors, a large ΔE_C does not merely provide a high electron barrier, leading to an increase in V_{BE} (i.e. large offset voltage), but it also limits the current gain

of the device. On the other hand, a large ΔE_V is actually desirable due to the reduction in reverse injection holes from the base into the emitter region[230]. For these reasons, the HBTs semiconductor materials must be carefully chosen; the band discontinuities of the common III-V systems are listed in table (5.1)[238, 239].

TABLE 5.1: EXPERIMENTAL BAND DISCONTINUITIES FOR COMMON III-V MATERIAL SYSTEMS.

Heterojunction material	E_{g1} (eV)	E_{g2} (eV)	ΔE_C	ΔE_V	$\frac{\Delta E_C}{\Delta E_V}$
$Si_{1-x}Ge_x/Si$ $(x \rightarrow 10\text{-}16\%)$	1.12-0.41x+0.008x^2	1.12	0.025 (x~16%)	0.12 (x~16%)	4.8
$InP/In_{0.53}Ga_{0.47}As$	1.35	0.76	0.25	0.34	1.36
$Al_{0.3}Ga_{0.7}As/GaAs$	1.86	1.42	0.28	0.15	0.54
$In_{0.49}Ga_{0.51}P/GaAs$	1.92	1.42	0.12	0.38	3.17
$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$	1.45	0.76	0.53	~0.17	0.32

Among all the GaAs-based material combinations used for HBT epitaxial layer designs, AlGaAs/GaAs systems were intensively studies owing to their high current gain and good high-frequency performance[238]. However, InP-based HBTs particularly InP/InGaAs technology have received a great deal of interest due to their use in photodetector ICs operating in the telecom optical wavelength ranging from 1.3 to 1.55µm. These standard wavelength bands are low loss windows utilized in long haul fibre optic telecommunications. The superior carrier transport and high current capability are the most prevailing advantages of InP/InGaAs devices along with the possibility of monolithically integrating InP-based HBT amplifiers with other optoelectronic devices. From the silicon industrial point of view, SiGe/Si HBTs come into contention with the III-V transistors basically due to the beneficial economy of scale of Si-based mainstream CMOS technology in the realms of RF integrated circuits. Furthermore, the downscaling of SiGe HBTs is easily performed because of the mature nanometre scale Si-processes achieved over years of work by commercial vendor including IBM, Hitachi and others[240, 241].

Despite the advantages of SiGe technology, the electron drift velocity in the InGaAs collector region in the InP-based HBTs is still three times higher than that in SiGe devices. Very high carrier diffusivity in the case of InP transistors offers much faster base transit time compared with SiGe, resulting in improving the frequency bandwidth by at least double for a comparable emitter sizes[241]. The other downside in SiGe is the low breakdown voltage of Si material, which is usually less than 2V for an HBT with a unity gain cut-off frequency, f_T of 100GHz[242, 243]. For a comparable base doping profile, InP based HBTs have a base sheet resistance of 650Ω/□[244] in comparison with 4KΩ/□ for SiGe devices[245]. This invariably translates into an improvement in the maximum frequency oscillation of the transistor, f_{max} and hence high switching speed capabilities with relaxed lateral geometry HBTs.

For HBTs designer, high breakdown voltages (BV_{CEO}) characteristic is preferred for several reasons. Firstly, it is desirable for high power microwave applications, in which the biasing voltages usually exceed 6V. Secondly, in IC designs, there are many additional passive components incorporated with the transistors, implying that a low breakdown voltage is a challenge because of the requirement to protect the circuits from voltage spikes. A double heterojunction bipolar transistor (DBHT) as an alternative approach has been proposed to mitigate low BV_{CEO} issue and for ultra-high speed operation. Unlike the base layer, both emitter and collector are made of a similar semiconductor material in DHBTs, allowing a double hetero-interfaces to be formed[246]. Taking the advantage of high mobility properties of the ternary materials, a typical DHBT epitaxial structure can be grown with an InGaAs base layer sandwiched between two lattice-matched InAlAs emitter and collector regions. The band diagram of the InAlAs-InGaAs DHBT is depicted in figure (5.4). As was earlier discussed in this chapter, a large difference in the band gap between the emitter and base material is desirable for high current gain capability as long as the band discontinuity in the valence band, ΔE_V is larger than that in conduction band, ΔE_C.

However, for InAlAs-InGaAs devices, ΔE_V is just 0.17eV compared with 0.53 ΔE_C that in turn will result in a large energy barrier for electrons at both emitter-base and base-collector heterojunctions[246]. This leads to a reduction in the number of electrons which are able to overcome the potential barrier at the B-C interface; consequently, the electrons will bounce back and recombined in the base region. Thereby deterioration in

the current gain of the transistor and enlarging the knee voltage (i.e. wide saturation region) are the outcome. Such an inherent phenomenon is known as the current blocking problem[247]. Both InP and InAlAs have been intensively studied as a collector layer to investigate the severe effect of the current blocking issue in DHBTs[247-249] and the findings emphasized that devices with InAlAs collectors suffer from pronounced carrier blocking. Contrarily, InP/InGaAs-based DHBTs are much less influenced by this phenomenon due to their favourable conduction band and valence band discontinuities[250].

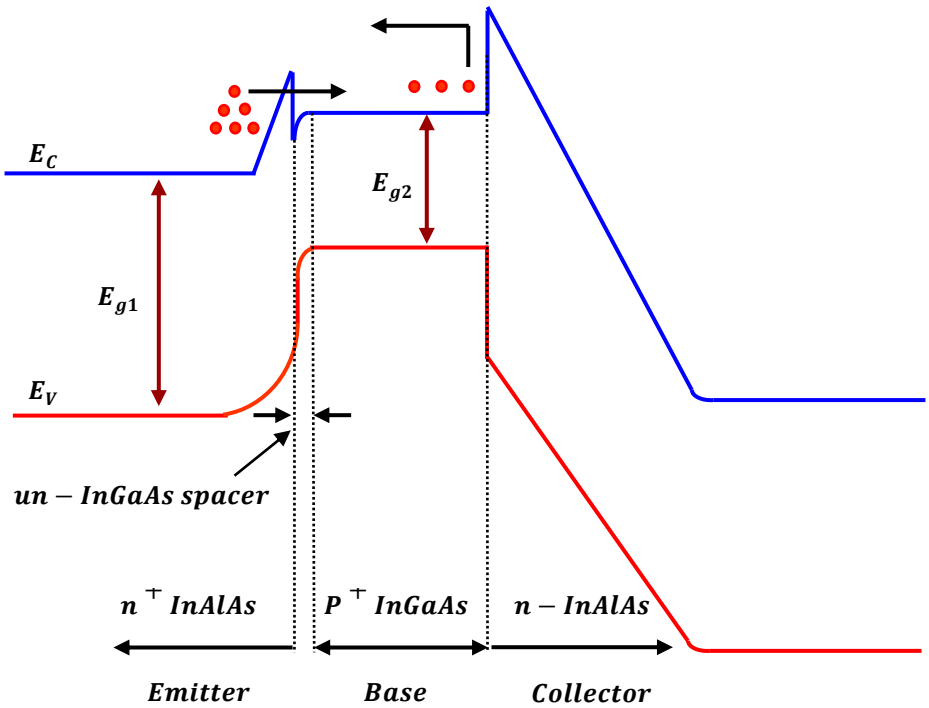


Figure 5.4: Equilibrium band diagram of InAlAs-InGaAs DHBT with no setback layer. The band energy shows a large potential barrier for electrons at B-C heterojunction causing a current blocking effect.

Mckinnon *et al* demonstrated an InAlAs-InGaAs DHBT with composite collector, which involves a low band gap setback layer grown on the collector, hence helping to alleviate the deleterious current blocking impact[247]. Another approach was devoted by McAlister *et al* and ended-up with exploiting a dipole doping in InP-InGaAs DHBT; hence improving the DC and RF performance of the transistor[250]. In 2010, further results were reported by Professor Missous *et al* using all-ternary InAlAs-InGaAs DHBT where current blocking was fully eliminated[251]. In the aforementioned study, a combination of doping interface dipoles and composite setback collector layers were used and culminated in an optimum epitaxial heterostructure able to support a high

current density without introducing current blocking. It is noteworthy to mentioning that a well-designed single heterojunction, SHBT has a BV_{CEO} exceeding 4V, which is considered adequate for optoelectronic integrated circuits as the photoreceiver based HBTs is often biased with a standard external voltage of 3.3V. Therefore, this project will be only concerned with SHBT devices through an in-depth analysis related to their characteristics and performances at high frequency operation.

5.4 HBT DC Characteristics

The DC characteristics are the underpinning parameter of most solid-state electronic devices in terms of primarily assessing the quality or/and evaluation of the exploitation of the devices in circuit implementations. In this section, a brief description of the fundamental DC characteristics of the HBT is presented. This includes highlighting the most regularly used characteristics of the common emitter HBT, such as turn-on voltage, early and breakdown voltages as well as output conductance and Kirk effect.

5.4.1 Output I-V characteristics of the Common Emitter HBT

Figure (5.5) shows a typical I-V characteristic for a common emitter SHBT. The most important part in the curve is the active mode or also known as the operating region, in which the emitter-base diode and base-collector diode are forward biased, $V_{BE} > 0$ and reverse biased $V_{BC} < 0$ respectively.

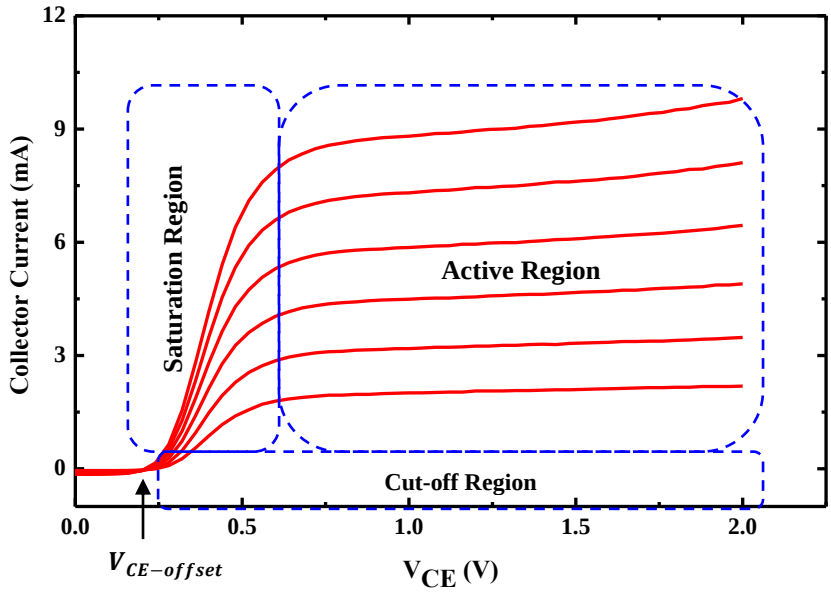


Figure 5.5: Typical I-V characteristic for a fabricated common emitter SHBT transistor, showing the three common modes of operations.

In the active mode, the transistor operates as an amplifier and this region is ideally linear and has a high breakdown voltage. The saturation mode is when both emitter-base and base-collector diodes are in forward bias, giving rise to a high current passing through the device with very small voltage drop between the emitter and collector terminals (i.e. low V_{CE}). In general, observation of a wide saturation region can reveal that there is an existence of current blocking effect or/and high emitter and collector resistances. Finally, the cut-off mode refers to both diodes being in reverse bias condition, creating wide depletion at the heterointerfaces (no noticeable current flow in the transistor).

5.4.2 HBT Turn-on Threshold and Offset Voltage

The required emitter-base voltage, V_{BE} for a desired collector current density characteristic is called the turn-on voltage. The importance of V_{BE} is prominent in ICs, in which matching the turn-on voltage of the HBTs across the wafer is necessary for a high yield process and to maximize the circuit performance. The inability to provide similar V_{BE} for multi-element integration will lead to degradation in the circuit's gain and signal to noise ratio[252]. The turn-on voltage is theoretically calculated using:

$$V_{BE} = \frac{E_{g2}}{q} - \frac{kT}{q} ln\left(\frac{q^2 \mu_n N_C N_V D_n}{J_C}\right) - \frac{kT}{q} ln(R_{sheet}) \tag{5.17}$$

E_{g2}, μ_n, D_n, N_C and N_V are the energy gap of the base, the mobility of the electrons in the base, the minority carrier diffusion coefficient, the conduction and valence effective density of states respectively and R_{sheet} is the base sheet resistance. The collector-emitter offset voltage, $V_{CE-offset}$ is the parameter used to characterize both device heterojunctions. It is determined by the difference between emitter-base and base-collector turn-on voltages. $V_{CE-offset}$ is due to the presence of several contributions, such as potential barrier for electrons at the emitter-base interface, collector space-charge region recombination currents and external voltage drops between contacts and the intrinsic device[253]. For InP-InGaAs HBTs, the offset voltage is less than 0.25V with a narrow saturation region, but with a well-designed epilayer structure and precisely controlled growth process can offer a solid foundation in developing a low DC power consumption and high-speed operation heterojunction device.

5.4.3 Transconductance and Output Conductance

Since the integrated circuits based on HBTs are often connected to a load, low output impedance is required for fast charging of the load capacitance and for high voltage gain. This implies that the transconductance of the transistor, g_m must be large, or in other words, a small change in V_{BE} must give a large variation in the collector current. The importance of the transconductance feature basically comes from achieving a small input voltage swing circuit operation[254]. This parameter can be evaluated from:

$$\frac{1}{g_m} = \frac{dV_{BE}}{dI_C} = \frac{1}{g_{m0}} + R_E + \frac{R_B}{\beta} \tag{5.18}$$

Where $g_{mo} = qI_C/kT$ and is the intrinsic transconductance. R_E and R_B are the emitter and base resistances respectively and the impact of R_E is dominant at higher currents. In the active mode operation, irrespective of the V_{CE} value, the deviation in the collector current should be small in order to provide a good linearity and high voltage gain. The low output conductance (g_o) of the HBTs is the key-parameter in attaining these important characteristics, with g_o given by:

$$g_o = \frac{dI_C}{dV_{CE}} = \frac{I_C}{V_a} \tag{5.19}$$

V_a is the early voltage of the transistor and is expressed as:

$$V_a = \frac{I_C}{(\frac{dI_C}{dV_{CE}})} = -W_B(\frac{dV_{CE}}{dW_B}) \tag{5.20}$$

The dependency of g_o on the base width, W_B is described by V_a where the early voltage is defined as the point at which the extrapolated plot lines of $I_C - V_{CE}$ intercepts the negative V_{CE} axis. For an HBT, V_a can be as high as 8V, which is 10 to 20 times higher than that in its Si-BJT counterpart as a result of the heavily doped base layer, contributing to further minimizing the impact of the base width modulation[254].

5.4.4 Breakdown Voltage and Kirk Effect

In HBTs, there are three main breakdown sources which are commonly introduced by the emitter-base junction breakdown, V_{eb0}, base-collector junction breakdown, V_{cb0} and

collector-emitter junction breakdown, V_{ce0}. All three make a contribution in determining the device's breakdown; however, the most prominent one is the base-collector breakdown, which is due largely to an avalanche multiplication mechanism and an increase in the reverse injected current from the collector region[26]. As high breakdown voltage is needed for high linearity and high-power operation, lightly doped and thick collector layer can effectively enable high V_{cb0}. However, this is at the expense of a compromise in the RF performance because of an increase in the collector transit time. To alleviate this impact, the collector width can be increased to a certain thickness in which the high-frequency response of the transistor is not limited by its transit time. Another crucial phenomenon in bipolar transistors is the Kirk effect. When the current density of a device increases, the electric field across the base-collector junction gets lower until it reaches zero. The reason behind this behaviour is because of high-frequency response screening effect of the mobile carriers crossing the B-C junction. The absence of the electric field results in allowing the majority carriers from the base side to diffuse into the collector side, which in turn contribute to a reduction in the current gain of the device. The current density at which the impact of the Kirk effect takes place is given by[255]:

$$J_{kirk} = qN_D v_{sat}(1 + \frac{2\varepsilon(|V_{BC}| + V_{bi(bc)}}{qN_D W_C^2}) \tag{5.21}$$

$V_{bi(bc)}$, N_D, W_C and v_{sat} are the built-in potential at the base-collector junction at thermal equilibrium, the collector doping concentration, the collector thickness and the saturation velocity of electrons in the collector region respectively. Note that, a typical I-V curve of an HBT which has a soft knee is distinctly suffering from the Kirk effect and this can be easily determined due to the concomitant precipitous rise in the output conductance. To alleviate this undesirable effect, the doping profile in the collector layer must be increased. However, this will reduce the breakdown voltage and increase the base-collector capacitance, affecting the high frequency performance; thus this trade-off should be carefully balanced.

5.4.5 Gummel Plots

A simultaneous method to display the collector current, I_C and base current, I_B versus the base-emitter voltage, V_{BE} on a semi-logarithmic scale is known as a Gummel plot and an

example is depicted in figure (5.6). This experimental plot is indispensable in device characterizations as it reflects on assessing the quality of the device junctions, while maintaining the base-collector voltage, V_{BC} at a constant value. There are many device parameters that can be basically obtained from the Gummel plot, such as the ideality factors, series resistances, leakage current, collector saturation current and the linearity of the DC current gain of the device at different biasing conditions. The ideality factors for both base and collector currents are given by[233]:

$$n_B = \frac{q}{kT}\frac{\Delta V}{\Delta(InI_B)} \tag{5.22}$$

$$n_C = \frac{q}{kT}\frac{\Delta V}{\Delta(InI_C)} \tag{5.23}$$

Where ΔV and $\Delta(InI_B)$ are extracted from the linear region of the forward Gummel plot. The graphs shown in figure (5.6) indicate three main regions:

A. **Low Current Non-Ideal Region:** It is due to the impact of the recombination process which occurs at low V_{BE} value in the emitter-base space charge region presumably due to the presence of defects. This event increases the ideality factor toward 2 and correspondingly decreases the current gain.
B. **Ideal Region:** At a moderate bias voltage, the base current increases which gives a linear rise in the collector current. Based on the material system of the device and transport mechanism, the ideal factor ranges from 1 to 2.
C. **High Injection Region:** Further increase in the DC biasing voltage enables high carrier injection hence resistive effects become dominant.

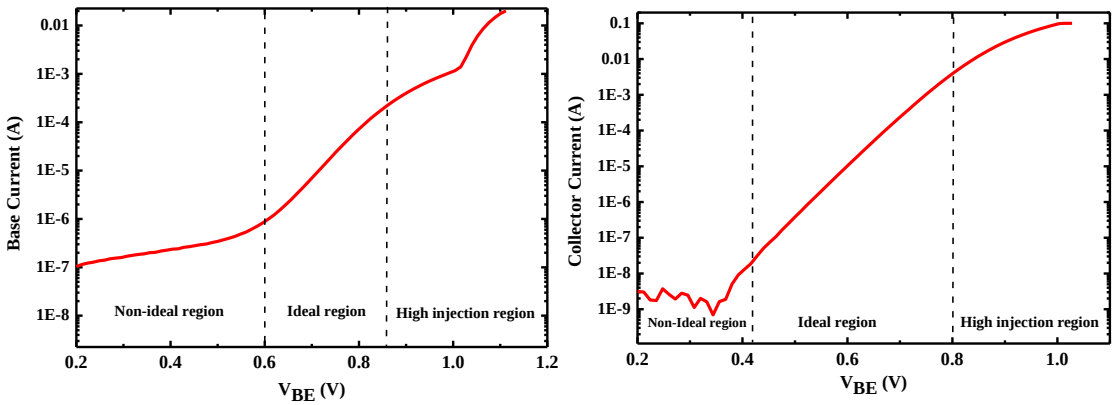


Figure 5.6: Measured forward Gummel plot of InP/InGaAs HBT sample F17D2102A with a 10×10μm^2 mesa size, showing three main regions in accordance to the applied base-emitter external voltage.

From the Gummel plot, the calculated ideality factors are 1.72 and 1.18 for base and collector junctions respectively. The degradation in n_B is primarily attributed to several recombination sources, such as in the emitter-base space charge region and surface recombination component on the extrinsic base surface. In spite of the fact that InP/InGaAs has much lower surface recombination velocity compared with AlGaAs/GaAs based devices[238], large spreading distance between the HBT active layers and base contact exceeding 1µm would exaggerate this inherent phenomenon. Furthermore, the surface parasitic process is extremely material dependent and governs the base current[256]. In the linear region, the current gain can be obtained by drawing a straight vertical line at any portion of V_{BE}; however, other regions are not suitable for current gain evaluation due to high recombination and series resistance effects.

Base and collector Reverse Saturation Currents: These experimental currents are commonly extracted from the linear region of the forward Gummel plots. When straight extended lines from I_B and I_C are extrapolated to zero bias, the points at which these lines intercept the y-axis are known as the base reverse saturation current, I_{bo} and collector saturation current, I_{co} respectively. As a result, the base and collector currents can be theoretically estimated by:

$$I_B = I_{bo}\left(exp\left(\frac{qV_{BE}}{kTn_B}\right) - 1\right) \tag{5.24}$$

$$I_C = I_{co}\left(exp\left(\frac{qV_{BE}}{kTn_C}\right) - 1\right) \tag{5.25}$$

5.5 HBT RF Figure of Merits

The requirement for HBT devices with a good performance at microwave frequencies is the underpinning parameter in designing the integrated circuits and electronic systems. Generally, the transistors have a number of elements causing various frequency responses; therefore, the performance of the devices is frequency-dependent particularly in high-speed operation. To this end, the radio frequency input signals encounter four main consecutive regions before arriving at the collector terminal. The carriers firstly enter the emitter-base space charge region (i.e. depletion layer capacitance) and they will then pass through the base region with a combination of diffusion or/and drift mechanism

and the delay in the base predominantly relies on the layer's thickness and mobility of the carriers. In this region, some minority carriers recombine and the signal is attenuated accordingly.

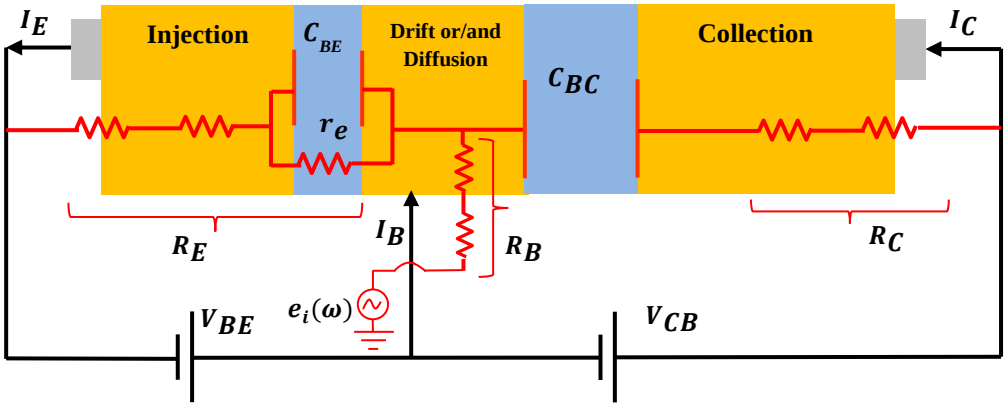


Figure 5.7: Simplified cross-sectional view of an N-p-n HBT device showing various components responsible for carriers' delay time.

The carriers will then transport across the base-collector depletion region under the applied electric field within a period of time. After that, they will ultimately pass across the collector region, giving rise to a collector transit time. There is an appreciable resistance between the emitter and external terminal of the collector, so an RC delay time is actually encountered[230]. All the aforementioned transitions are described in figure (5.7). On the basis of these considerations, the unity-gain cut-off frequency, f_T (the frequency at which the common-emitter current gain is unity) is one of the most important figures of merit for HBTs, which is interpreted into the capability of the device to efficiently operate at high frequency.

$$f_T = \frac{1}{2\pi\tau_{EC}} = \frac{1}{2\pi(\tau_{EB} + \tau_B + \tau_{BC} + \tau_C)} \tag{5.26}$$

$\tau_{EC}, \tau_{EB}, \tau_B, \tau_{BC}$ and τ_C are the total transit time from emitter to collector, emitter-base junction capacitor charging time, base transit time, base-collector depletion region transit time and collector resistance-capacitance charging time (collector delay time) respectively[257]. These crucial quantities do not solely rely on the design of the epilayer structure in terms of the material system and layers thicknesses but they are also affected

by the predefined dimensions of the phase-shift mask and fabrication process as given by the following expression:

$$\tau_{EB} = \frac{kT}{qI_E}(C_{BE}) \tag{5.27}$$

This delay time refers to the time required to a change in the base voltage by charging the emitter-base capacitance, C_{BE} through the total emitter resistance. Due to the inverse proportionality of emitter current to τ_{EB}, HBTs devices are driven with high current densities, facilitating high power operations. The base transit time, τ_B is expressed as:

$$\tau_B = \frac{W_B^2}{\eta D_n} \tag{5.28}$$

W_B and D_n are the base width and minority carrier diffusion constant in the base region and $\eta = 2$ for a uniformly doped base layer. Finally, the base-collector depletion region delay time, τ_{BC} and collector transit time, τ_C are given by:

$$\tau_{BC} = \frac{X_C}{2V_{sat}} \tag{5.29}$$

$$\tau_C = C_{BC}(\frac{kT}{qI_E} + R_E + R_C) \tag{5.30}$$

Where V_{sat} is the saturation velocity of the carriers in the collector layer, whereas the base-collector depletion width and capacitor are denoted as X_C and C_{BC}. To maximize f_T, it is compulsory that each time constant illustrated in equation (5.26) must be minimized; nevertheless, HBTs offer enormous improvements compared with Si-based BJTs. For instance, the base transit time can be reduced by thinning the base layer without incurring the expense of high base resistance, due to the ability of heavily doping the base[228]. Additionally, with further support from the high mobility properties of III-V semiconductor compounds, there is a consequent increase of the diffusion constant and hence a decrease in τ_B. In reality, such properties are restricted by the maximum electric field applied, which should be lower than the negative differential mobility of the material.

The ballistic transport across the base region in abrupt emitter-base heterointerfaces can increase the carrier's saturation velocity, corresponding to a reduction in τ_{BC}. However, this can be most likely beneficial when precluding the electrons from entering the high-energy and low-mobility section in the conduction band structure[230]. Unlike BJT devices, the low emitter doping profile in HBTs reflects into a reduction in C_{BE} for small τ_{EB} delay time value. To assess the HBT performance, the unity-gain cut-off frequency, f_T is derived using h-parameters; however, the later cannot be directly used at microwave frequencies due to the requirements for open and short terminals, which is rather difficult to achieve in practical devices[258]. Therefore, h-parameters are often converted into scattering parameters as given by:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{5.31}$$

From the graph of $|h_{21}(f)|$ versus frequency in logarithmic scale, the cut-off frequency is obtained from the intercept point between an extended straight line with a -20dB/decade roll-off and the x-axis. Another important figure of merit is the maximum frequency of oscillation, f_{max}, defined as the frequency at which the power gain of the transistor drops to one[255].

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{5.32}$$

R_B is the lateral base resistance from the contact to the active layers of the device. The base resistance can be mitigated by shrinking the emitter width and minimizing the spreading distance between the contact and base active region. A decrease in R_B benefits from a highly doped base layer; however, this might degrade the device gain and give rise to an increased C_{BE}. An effective way to improve f_{max} without sacrificing f_T and breakdown voltage is to reduce the base-collector depletion capacitance, C_{BC} by scaling down the base-collector area. Of particular interest are the two simultaneous methods to describe the power gain of amplifiers from the measured S-parameters data, which are the maximum available gain (MAG) and unilateral power gain (U) as stated in the following equations:

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| (k - \sqrt{k^2 - 1}\,) \tag{5.33}$$

$|S_{21}/S_{12}|$ is the maximum stable gain (MSG), whereas k is the stability factor and is given by:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{12}||S_{21}|} \tag{5.34}$$

Where D is the determinant of the scattering matrix formulated as $D = S_{11}S_{22} - S_{12}S_{21}$. The amplifier is unconditionally stable when $k > 1$; however, a problem arise if $k < 1$, where MAG cannot be evaluated due to the existence of an imaginary part. In such case, the maximum stable gain, $|S_{21}/S_{12}|$ is commonly utilized as a figure of merit for the transistor. The absence of MAG implies that the device is unstable and must be stabilized by connecting a supplementary shunt resistor at the input or output port[258]. It is worth pointing out that MAG and MSG are identical when either concurrent conjugate matching exists (i.e. zero reflected power at the transistor input/output port) or $k = 1$. For amplifier design, a zero reverse transmission gain is preferred (i.e. $S_{12} = 0$), which can be achieved by adding a lossless external feedback network, resulting in unilateralized transistor circuit. The MAG of the unilateralized amplifier known as Mason's unilateral gain (U), which is the highest power gain the two port would ever provide and is related to the S-parameters of the original transistor[258].

$$U = \frac{|(S_{21}/S_{12}) - 1|^2}{2k|(S_{21}/S_{12})| - Re(S_{21}/S_{12})} \tag{5.35}$$

A practical question emerges regarding the two definitions for the power gain, which one of them (MAG/U) makes better sense in device characterizations. For a transistor operating at a few gigahertz frequencies, MAG may not exist because of instability issue($k < 1$). Conversely, U can be attainable at relatively low frequencies with resulting unconditionally stable operation of the transistor circuit even though the device itself is potentially unstable[258]. As a standpoint, both of the power gain expressions are of importance and might be required for full characterizations and can aid in understanding the performance of the device.

Owing to the f_T and f_{max} relationships, these key parameters are predominantly maximized by a well-designed vertical device epilayer structure and optimized lateral HBTs process respectively. In recent years, InP-based HBTs have received a great deal of attention as a result of their impressive high frequency response. This is due also to the extensive improvements in growth techniques and fabrication process, allowing precise control in the material composition with monolayer thickness precisions and dramatic reduction in lateral device dimensions. Many researchers have demonstrated outstanding work in terms of achieving a cut-off frequency exceeding 200GHz. In 2004, sub-micron scale emitter size for InP/InGaAs SHBT was reported by Yu *et al* with an f_T/f_{max} of 215/687GHz[259].

As an alternative approach, the complex transferred-substrate processing technique was used by Lee *et al* which in turns provides an f_T and f_{max} of 162 and 820GHz respectively[260]. Whilst optimizing the device structure, an advanced geometry processing has been also pursued for a long time, resulting in Hafez *et al* demonstrating the highest f_T of 604GHz[261] and Rodwell *et al* accomplished an outstanding f_{max} of 1.08THz (considered the highest to date)[262]. A SiGe-based HBT with 100nm emitter junctions was reported with a f_T/f_{max} of 300/350GHz[242], however, this is still lower than f_T/f_{max} of over 450GHz achieved for an InP-based devices with a much relaxed geometry of 0.5µm emitter width.

5.6 Overview of PIN-Photodiodes

Photodetectors are key elements in lightwave receiver systems, serving as converters of the incident light from optical power into electrical current. There are a number of electronic devices that have been demonstrated over the last three decades for high-speed optical transmission; however, the most widely used devices are the avalanche photodiodes (APDs) and PIN photodiodes[26]. These photodetectors are normally categorized by their own structures and principle of operation. APDs can provide up to 5-10 optical power sensitivity higher than that given by PINs due to their multiplication gain characteristic[82]. They are invariably suitable for weak light signals in trunk-lines and local area networks without an integrated preamplifier. Nevertheless, for long-haul fibre optics, this comes at the cost of the epitaxial layer complexity, high bias voltages

(>25V) and difficulties in monolithic integration with HBTs. Conversely, the simple design structure and low-cost manufacturing capability offered by PIN-PDs are considered as very promising for use in the field of optical receiver applications[14].

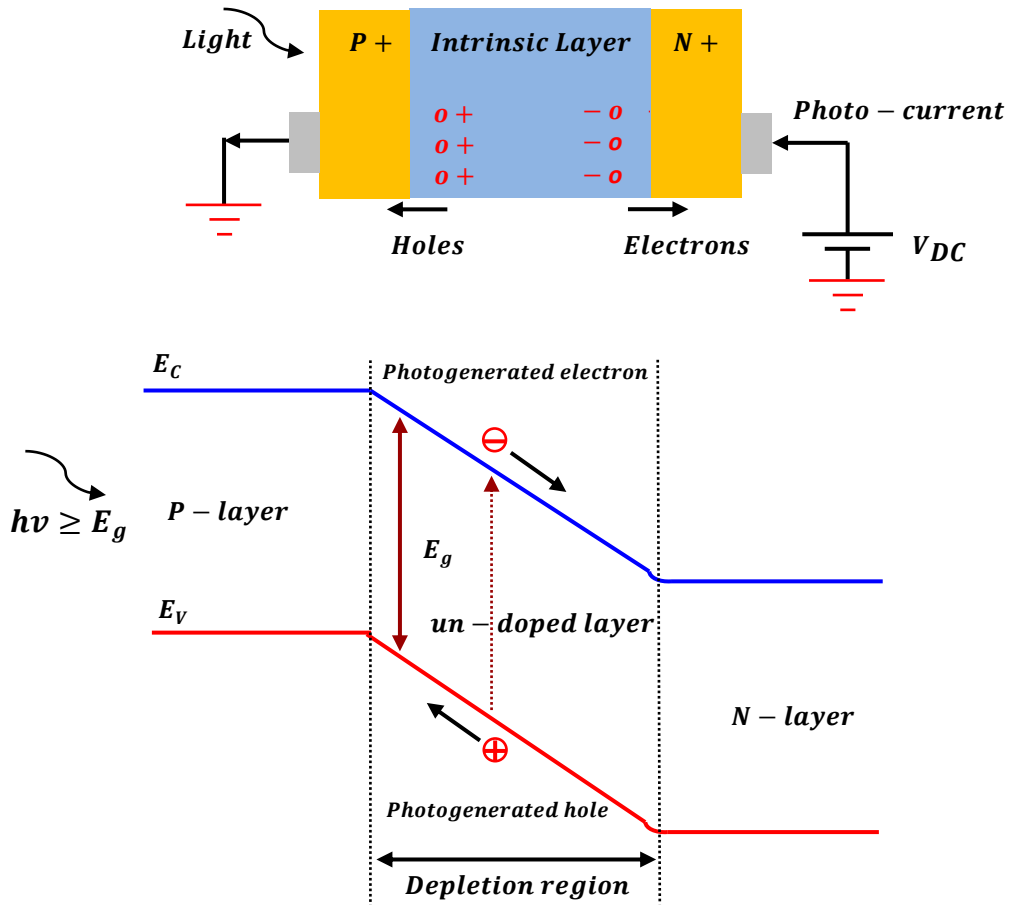


Figure 5.8: A simplified schematic drawing and energy band diagram of a PIN-Photodiode, showing the mechanism of the photo-current generation.

The structure of the P-I-N diode basically consists of an intrinsic (undoped) layer sandwiched between two heavily doped P-type and N-type layers as shown in figure (5.8). The working configuration is principally based on biasing the PIN-PD in the reverse bias direction. This makes the highly resistive intrinsic layer free of mobile carriers particularly when a high electric field is applied. When the diode is illuminated by light photons whose energy is equal or greater than the bandgap of the intrinsic layer, an absorption event occurs. This is when the photons enter the intrinsic area, contributing to releasing electrons from the valence band into the conduction band and leaving holes behind in the valence states. The generated electron-hole pairs will be then moved by the electric field in different directions where the electrons and holes are collected at the (n+)

and (p+) sides respectively, resulting in photocurrent flows in the device[263] as shown in figure (5.8).

5.7 PIN Diode: Material System and Characteristics

For optoelectronic integrated receivers, silicon material represents the prominent platform for use in photodetector implementations. The increasing interest in Si-based circuits is to utilize optics for short transmission in data centers rather than use metallic interconnections and to further reduce the cost and footprint of ICs[264]. Traditionally, the realized photodetectors are based on various band gap and absorption semiconductor materials employed for corresponding spectral ranges. For example, Si-based devices are the favourable choice for the visible wavelength region, while GaAs materials are preferred in the wavelength range between 0.6 to 0.9µm[78]. Unfortunately, silicon has a very low optical response at long wavelengths ($\lambda > 1\mu m$) due to its relatively large indirect band gap properties. Small bandgap materials such as germanium provide a higher absorption coefficient at 1.2µm wavelength or higher as shown in figure (5.9).

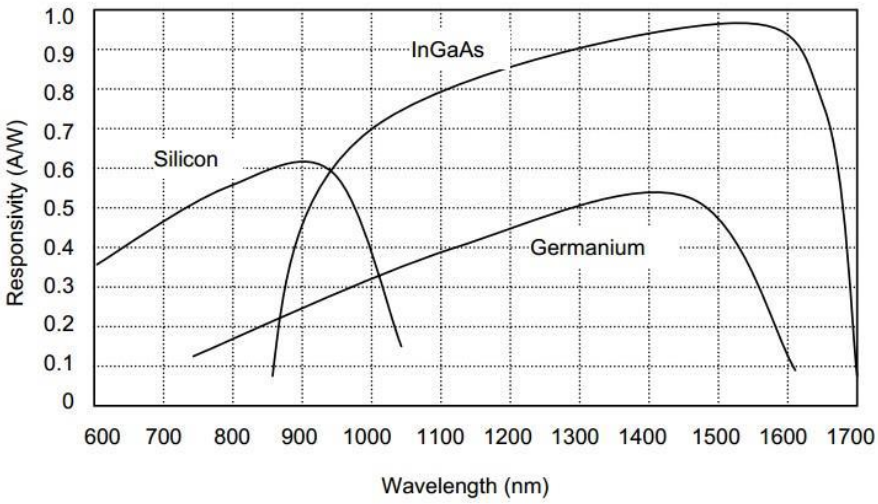


Figure 5.9: Responsivity as a function of light wavelength for several material systems based PIN-Photodiodes[263].

However, pure germanium has a 4% lattice mismatch with silicon, contributing to producing misfits in the lattice structure. This inherent issue directly degrades the device performance in terms of a decrease in the photodetector sensitivity by increasing the dark current (i.e. leakage current)[265, 266]. By contrast, III-V material systems, for example InGaAs, are the preferred choice for the standard telecommunication wavelength of 1.30

to 1.55μm since their energy bandgaps can be simply engineered in accordance to the required wavelengths. In this work, $In_{0.53}Ga_{0.47}As$ is used as an intrinsic layer, which exhibits a remarkable performance in high power and high-frequency photodetector applications due to its high saturation velocity and low effective mass for carriers compared with silicon technology[267].

To assess a detector response, consideration of two fundamental characteristics is required, which are responsivity and quantum efficiency. The first parameter represents how efficiently a photodiode deals with converting light into an electrical signal. It is theoretically calculated by the ratio of average photo-current, I_{ph} in Ampere to the incident power of light, P_{ph} in Watt at a given wavelength.

$$R_{es} = \frac{I_{ph}}{P_{ph}} \tag{5.36}$$

The percentage of the absorbed photons in the intrinsic layer is the key-factor in determining the amount of the generated photo-current. The ability of high absorption properties for light is translated into a large number of the generated carriers. However, under this condition $hv \geq E_g$where h and v are the Planck constant and incident photon frequency respectively, with some of the photons unable to create electron-hole pairs. From this definition, the ratio of the number of the absorbed photons with the capability of generating carriers to the incident optical power is known as the quantum efficiency, η and is given by[263]:

$$\eta = \frac{1.24R_{es}}{\lambda\ (in\ \mu m)} \tag{5.37}$$

Unlike APDs, PIN-PDs have a unity internal gain; thus, the variation in η ranges from zero to one. The responsivity and quantum efficiency of the photodetectors are extremely important parameters and are material and epitaxial structure dependent characteristics. As shown in figure (5.9), InGaAs-based devices can provide responsivities as high as 0.9 to 0.95A/W in the wavelength range 1.3-1.55μm. However, this figure of merit drops at long wavelengths since the energy of photons is low, creating fewer carriers. Likewise, short wavelengths are often absorbed in large bandgap layers formed on the top of the intrinsic region, resulting in a decrease in the device's responsivity. In this research, a semiconductor laser operating at 1.55μm was used as a light source. Note that the

transmitted optical signal via an optical fibre is often modulated with a stream of optical pulses acting as a carrier for the information signal. A high-performance photodiode is defined by the capability of detecting billions of optical pluses per second, giving rise to a concept called telecommunication data rate. In recent literature, the number of Giga bit per second (Gb/s) and the optical bandwidth of the photodiode are key to meet the rapidly increasing demands for high data rate capacity[268, 269].

As an optical architecture standard, 2.5Gb/s GPON is in full deployment and the next generation 10Gb/s EPON (IEEE 802.2av, ratified September 2009) started deployment in late 2013[80, 83]. This means that the need for ultra-high speed photodiodes is now imperative to satisfy the previous requirements of the fibre optic communication systems. In the early 1990s, InGaAs PIN-PDs were reported with 0.6 and 0.55 responsivity and quantum efficiency respectively and the device was successfully tested in a 4Gb/s InP/InGaAs optical receiver at 1.5µm wavelength[270]. Meanwhile, Gutierrez *et al* demonstrated an InAlAs/InGaAs PIN-HBT optical receiver with a 9GHz bandwidth using an integrated PIN diode with a mesa size of 100µm^2[271]. The same authors achieved a 20GHz bandwidth for a similar PIN by further reduction in the device mesa size. This enhancement in performance offered a data rate capacity of 20Gb/s[272]. For the developments in high Gb/s are mainly classified into two parts; either epilayer structure design in terms of layer thickness and material system or fabrication process improvement for small feature sizes. The superior material combination of InP/InGaAs based ICs is one of the best candidates for use in monolithically integrated PIN-HBT optical receivers. Utilizing the former mentioned semiconductor compound, a 37GHz optical bandwidth was demonstrated in 2006, which is adequate for over 50Gb/s data rate communication[273]. Design procedure of high-speed optoelectronic integrated circuit (OEIC) and relevant discussion and analysis is presented in the next chapter in details.

5.8 Summary

This chapter presented a detailed study of an integrated InP/InGaAs HBT and PIN devices. This started from their principle of operation and looking into more details in their DC and RF figure of merits and possible ways of maximizing them. For the HBT device, the characteristics of the common emitter configuration was discussed including I-V curve, Gummel plots, turn-on threshold voltage and transconductance. More

importantly, assessing the high-frequency performance of HBTs was presented concentrating on how to extract and qualify f_T and f_{max}. Later in this chapter, state of the art performances of InP based PIN-PD were covered and compared with the conventional Si based devices. This highlighted the ability of photodiodes to effectively operate at 1.55µm wavelength for 2.5Gb/s GPON and 10Gb/s EPON optical communication systems.

CHAPTER 6: CHARACTERIZATION AND DEVELOPMENT OF OEICs FOR FTTH SYSTEMS OPERATING AT 10Gb/s AND BEYOND

6.1 Introduction

An overview of the background theory and the widely used figure of merits for PIN-PD and HBT transistors were covered in the previous chapter. For this research, the initial step in developing an InP/InGaAs based photoreceiver was to characterize active discrete devices needed here namely, PINs and HBTs and passive devices. The full process flow involved mask design procedures and a reproducible fabrication process of all devices. Next the DC and RF characteristics of PIN-PD are obtained, followed by the development of full electrical and optical equivalent circuit models. This is basically started from extraction parameters of the models for a top illuminated photodiode. Validation of the electrical equivalent model is verified by comparison with experimental data and this was carried out for various device mesa sizes and biases.

As HBTs and other active electronic devices are dependent on their epilayer structure design, the impact of several physical parameters such as base thickness and its doping profile have been investigated utilizing the commercially available Silvaco-Atlas software. To implement the final photoreceiver, detailed characterizations of the HBT including extraction of small/large signal model parameters and realization of an HBT-UCSD model in Keysight were undertaken. As a standpoint, chapter six takes HBT and PIN-PD model results further focusing on the design and development of an optoelectronic integrated photoreceiver (OEIC) for > 10Gb/s data rate systems. This will aggregate the earlier concepts of the IC design presenting the whole receiver system stage by stage and together with front-end amplifier as a model in Keysight-ADS. The photoreceiver figure of merit is discussed here including the amplifier gain, bandwidth and other features. This is followed by analysing the simulation results and briefly describing the mask design procedure of the circuits. Finally, the optimization of the IC performance, particularly for high-frequency operation via bandwidth enhancement techniques and other relevant discussions are presented.

6.2 Epilayer Structure of the PIN-PD

Designing a good InP/InGaAs PIN photodiode is extremely important for high-speed optical systems since the aim is to achieve as high as possible responsivity and quantum efficiency while maintaining high performance for frequency-dependent characteristics. Many parameters were thus considered in this work, starting from epitaxial layer design to well-established photo-mask and fabrication process. Firstly, the absorption layer thickness of the photodiode was carefully chosen to reduce carrier's transit time across the layer in conjunction with minimizing the depletion region capacitance. For monolithic integration, DC and RF performance of the HBTs device should be also maximized, implying that a trade-off must be struck in the whole photoreceiver application including the PIN-PDs and HBTs. Note that a thin intrinsic layer of ≤40nm can, of course, lead to a reduction in the collector transit time of the HBTs but this comes at the cost of high B-C junction capacitance which degrades the high-speed capability of the device (low f_T and f_{max}). An additional downside is that the RC time constant of the PIN-PD will be dominant over carrier transit time leading to a reduction in the -3dB bandwidth. The photodiode would also suffer from high leakage current (i.e. high dark current with low responsivity) resulting in degradation of the device's sensitivity.

TABLE 6.1: EPI-LAYERS FOR THE SAMPLE F17D2102A GROWN BY MBE.

LAYER	MATERIAL	THICKNESS (nm)	DOPING (cm^{-3})
CAP-LAYER	$In_{0.53}Ga_{0.47}As$	150	(Si) 1.5×10^{19}
EMITTER1	$In_{0.53}Ga_{0.47}As$	150	(Si) 5×10^{17}
EMITTER2	InP	40	(Si) 5×10^{17}
SPACER	$In_{0.53}Ga_{0.47}As$	5	Undoped
BASE	$In_{0.53}Ga_{0.47}As$	65	(Be) 2.5×10^{19}
COLLECTOR	$In_{0.53}Ga_{0.47}As$	800	Undoped
SUB-COLLECTOR	$In_{0.53}Ga_{0.47}As$	500	(Si) 1×10^{19}

The epitaxial stack structure studied throughout this project was grown on lattice-matched semi-insulating InP substrates using Solid Source Molecular Beam Epitaxy

(SSMBE) and is shown in Table (6.1). The PIN-PDs were formed utilizing the base, collector and sub-collector regions of the structure. An $In_{0.53}Ga_{0.47}As$ intrinsic layer with a width of 800nm can provide good quantum efficiency for the photodiode without incurring a detrimental impact on f_T or/and f_{max} of the transistor. Furthermore, a moderate absorber thickness offers a relatively high breakdown voltage required for high power integrated circuit operation. This also ensures that both devices can switch well into the high frequency operation necessary to demonstrate an OEIC for > 10Gb/s data rate optical systems.

6.2.1 PIN-Photodiode's Layout Design and Fabrication

Due to the additional grown layers on the top of the PIN-PD epilayer required to finalize HBT's structure, the fabrication process commenced with etching away the surrounding area up to the p^+-InGaAs base layer. With this in mind, an entirely compatible process was used for both HBT and PIN devices as briefly discussed here and will be further highlighted later in this chapter. A photo-mask for discrete PIN-PDs was designed in Keysight-ADS with various window sizes, starting from 40 down to 20µm. Beside the actual photodiodes' devices, the mask is composited of a few dummy and test structures, such as open and shorts modes as well as various via dimensions and TLM test structures. The photo-mask was built with five steps in total and an example of a device with 20µm window size is shown in figure (6.1). The first two steps are basically devoted to defining the top P-type and the bottom N-type mesa areas (step#1 and #2), which contribute to electrically isolating each discrete PIN from other neighbouring devices. The ring top contact and bottom contact can be then defined (step#3) and all the pattern dimensions are indicated in figure (6.1).

By lifting-off the non-alloyed ohmic contact scheme of Pd/Ti/Pd/Au with a ~1µm total thickness, a dielectric combination of SiO and Al_2O_3 is sputtered everywhere, allowing the active layers to be passivated and to facilitate the interconnecting routing. The dielectric layer acts as an antireflection (AR) coating for the photodiodes, providing better responsivity performance. This step is followed by opening the vias with a predefined size of $1.5\times2.5\mu m^2$ (step#4). A metallization can be eventually deposited, representing the interconnections and bond-pads for on-wafer probing measurements (step#5) and by lifting-off the latter scheme, the devices are ready to be experimentally

tested. Figure (6.2) and (6.3) show a 3D schematic and an ultimate fabricated PIN-PD respectively, including the active device layers, both contacts and the GSG bond-pads.

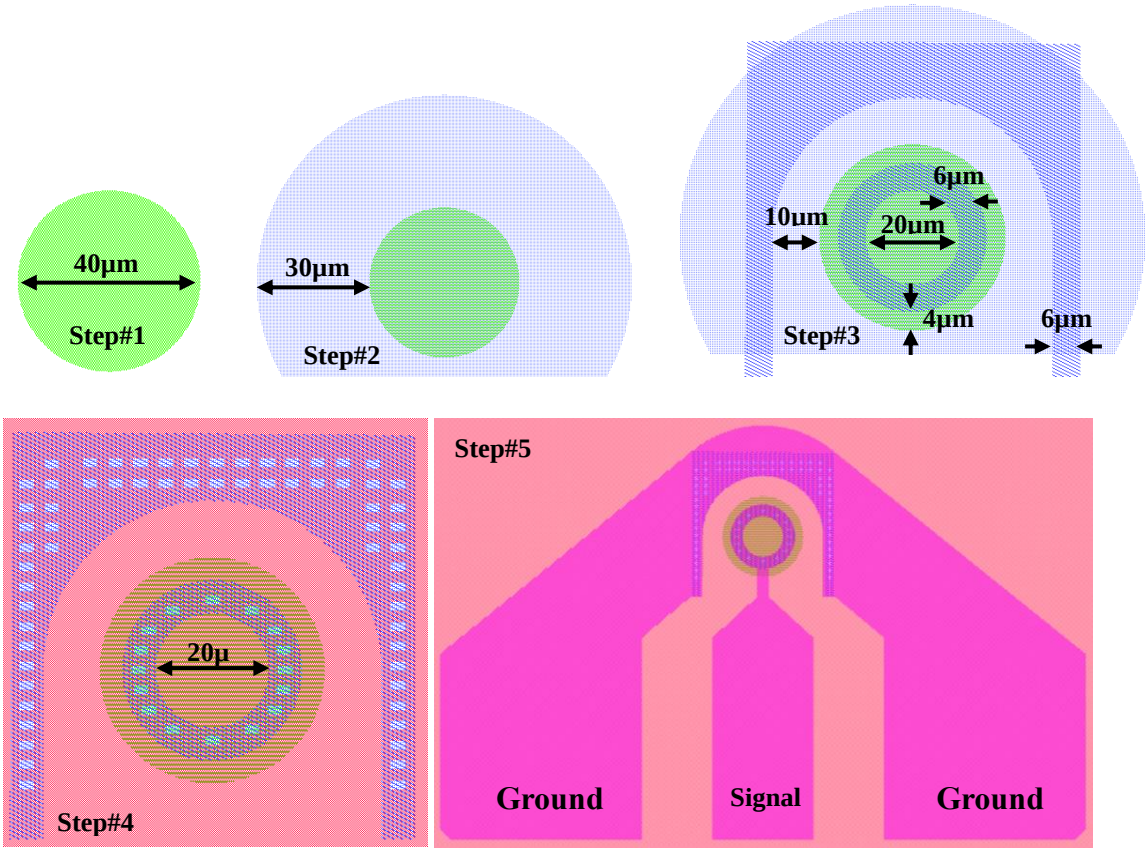


Figure 6.1: Top view of the PIN photo-mask designed by Agilent-ADS software showing the process step by step for 20µm window size as defined by mask pattern.

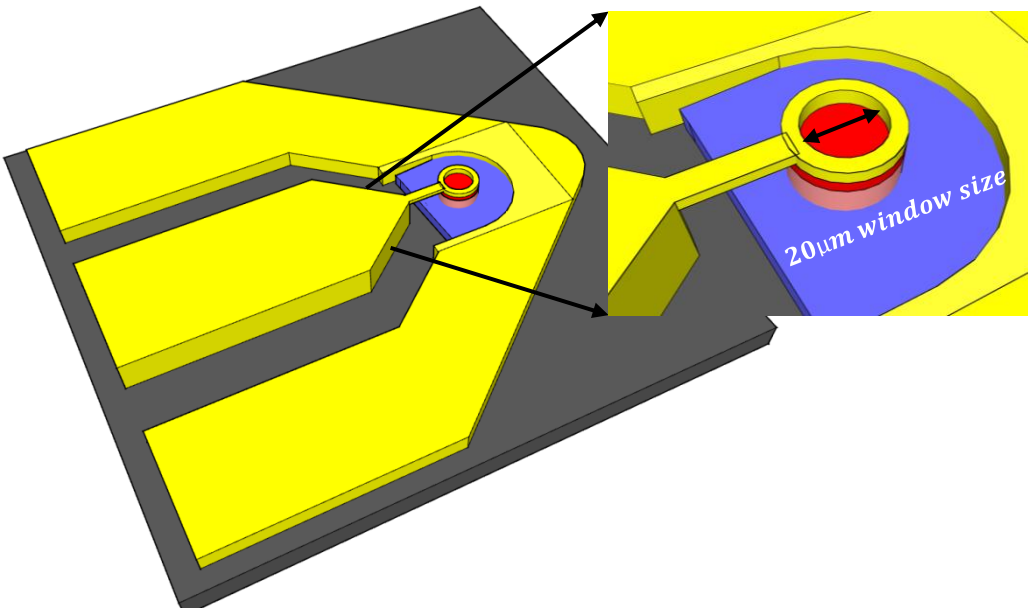


Figure 6.2: 3D schematic of the fabricated PIN-Photodiode with a window size of 20µm, showing the contacts and CPW transmission line for measurements.

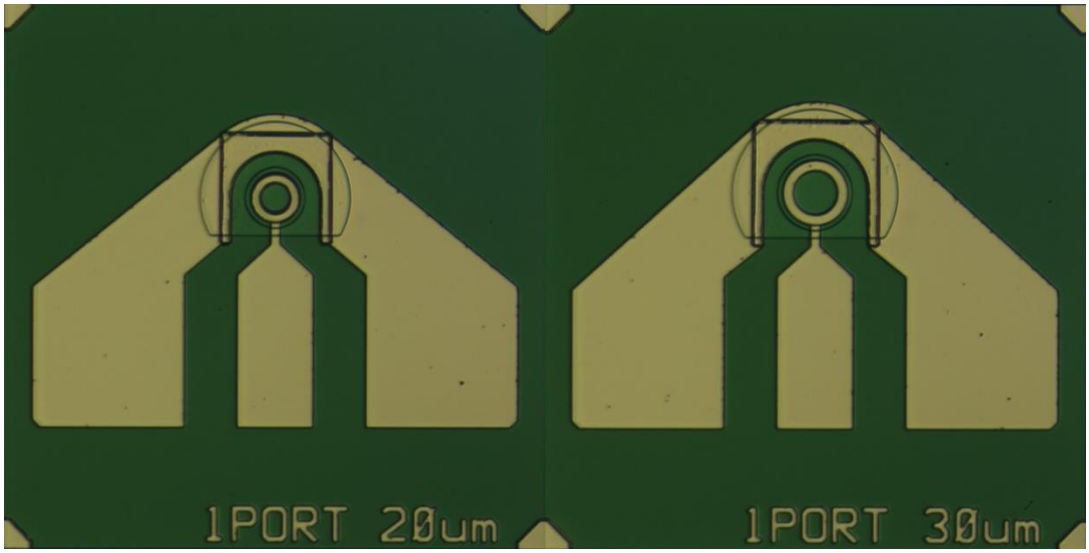


Figure 6.3: Photomicrograph of the fabricated PIN-PD discrete devices with a window size of 20 and 30µm.

6.2.2 Evaluation of DC Characteristics

Once the fabrication process was successfully accomplished, the PIN-PDs with different window sizes were tested. In order to fully characterize the devices, the measurements were performed with and without illumination hitting the diodes. A single mode fibre was used for the measurement set-up with a Keysight 8703A lightwave component analyser (LCA).

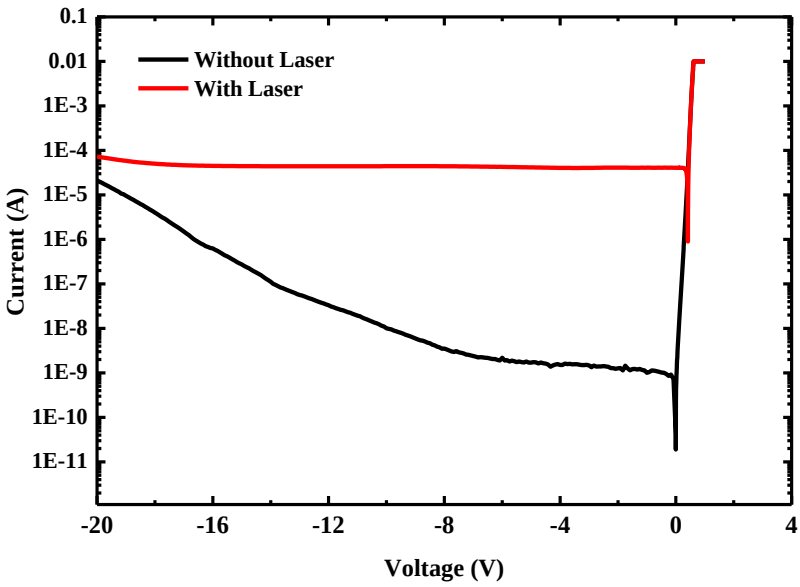


Figure 6.4: Measured I-V characteristics for a 20µm window size PIN diode with and without illumination. The device was tested without antireflection coating at a laser wavelength of 1.55µm and with -11dBm power of light.

Figure (6.4) shows the measured room-temperature I-V characteristic for a PIN with a window size of 20µm. The dark current of ~1.5nA was achieved at an external applied voltage of -5V. The low leakage current is attributed to the well-designed epitaxial structure and high-quality material. The measured photo-current was 41.5µA at -11dBm optical power and λ=1.55µm, corresponding to a 0.5 A/W and 0.45 DC responsivity and quantum efficiency respectively without antireflection coatings. Similar measured parameters were found for devices whose window sizes are 30 and 40µm. The responsivity and quantum efficiency of the PIN-PDs can be improved by roughly 20% once the AR coating is deposited.

6.2.3 Equivalent Circuit Extraction and RF Performance

This section mainly focuses on extraction procedures of the equivalent circuit parameters for PIN-photodiodes. It is well-known that the model elements are dependent on device mesa size, epilayer design and even biasing conditions. The electrical equivalent circuit model of two terminal devices have been widely demonstrated for solid state electronic and optoelectronic devices[274-276].

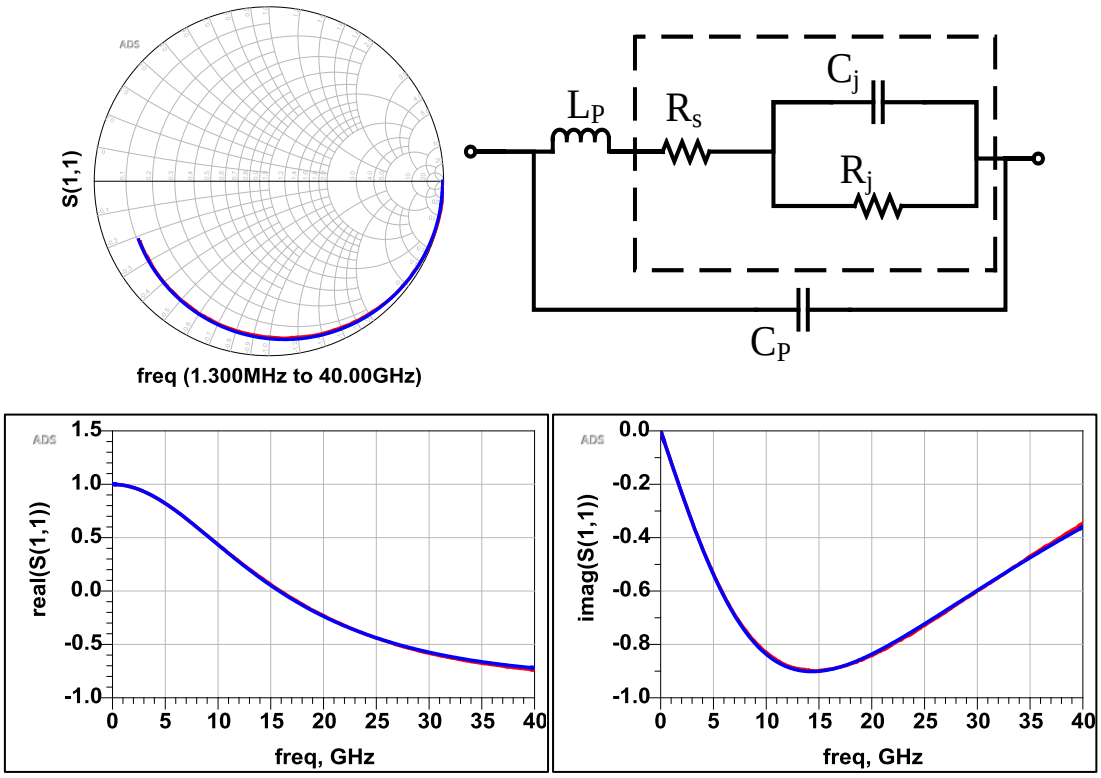


Figure 6.5: Electrical equivalent circuit of the PIN-PDs involving both the embedded parasitic and the intrinsic device components (dash lines) alongside the measured (red) and simulated (blue) results of S_{11} plotted on Smith chart as well as real and imaginary parts for a PIN-PDs with a window size of 20µm. The diode was biased at -5V where the intrinsic layer is fully depleted.

The S-parameter measurements was carried out using on-wafer probing technique up to 40GHz for unilluminated PINs, allowing the parameter values to be accurately extracted without involving the impact of carrier delay time across the absorption layer. The electrical equivalent circuit model and the experimental and modeled S_{11} for a photodiode with a window size of 20µm is shown in figure (6.5). By sweeping the DC voltage bias, the C-V characteristic can be simply obtained, emphasizing that the fully-depleted capacitance (C_j) is noticeable at -5V as depicted in figure (6.6). As this voltage is strongly dominated by the depletion region thickness, a similar value was observed for various devices regardless of their mesa sizes. Unsurprisingly, the C-V results show a variation in the junction capacitance depending on the diode mesa sizes. Fitting approach with the measured S-parameter data was employed, accordingly the intrinsic series resistance, R_s and junction resistance, R_j of the device were extracted to be 5Ω and >10kΩ respectively.

Pad parasitic, C_P and L_P of 10fF and 50pH were obtained from open and short CPW structures respectively. For monolithic OEICs, the undoped collector layer does not solely play a pivotal role in minimizing the base-collector capacitance of the HBT, but also serves as the absorption layer for the photodiode. The depletion region capacitance can be reduced through growing a relatively thick intrinsic InGaAs layer; however, this leads to an increase in the carrier's transit time of the PIN-PDs and collector delay time for HBTs.

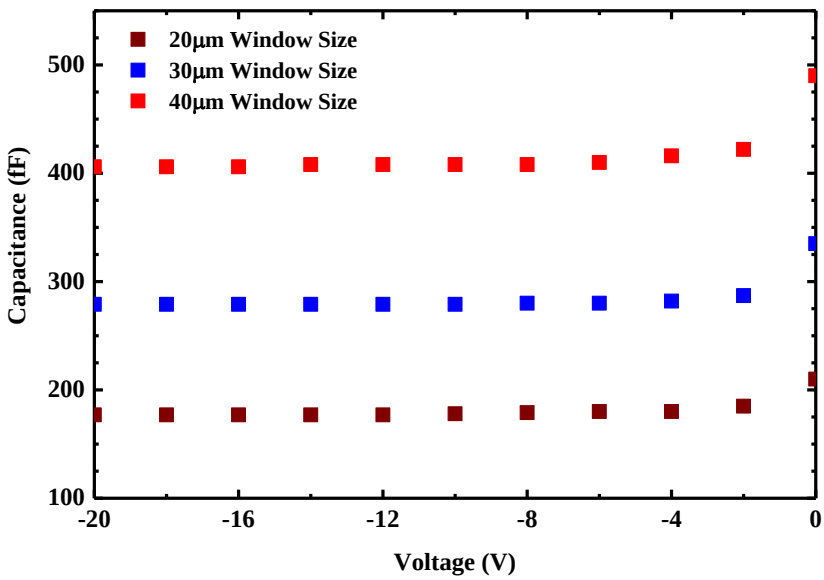


Figure 6.6: Measured C-V characteristics of the fabricated PIN diodes with different window sizes without illumination.

Since the trade-off between the high-frequency performance of the transistors and responsivity of PIN-PDs needs to be carefully balanced, an intrinsic layer with 800nm thickness was grown. For illuminated photodiodes, the generated electron-hole pair transport across the depletion region with a certain velocity relying on the applied electric field. This physical-based transit time causes an additional capacitance limiting the high-speed response of the devices. It is of vital importance to point out that fully electrical equivalent circuit models reported in the literature do not actually provide a proper clarification for the transit time capacitance in illuminated PIN-PDs[277, 278]. This inherent phenomenon becomes much inferior with high input optical power level in which the impact of the induced-stored charge in the photodiodes is significant[279]. In this research, an opto-electrical equivalent circuit was modeled in which both RC time constant and carrier transit time are taken into account as shown in figure (6.7).

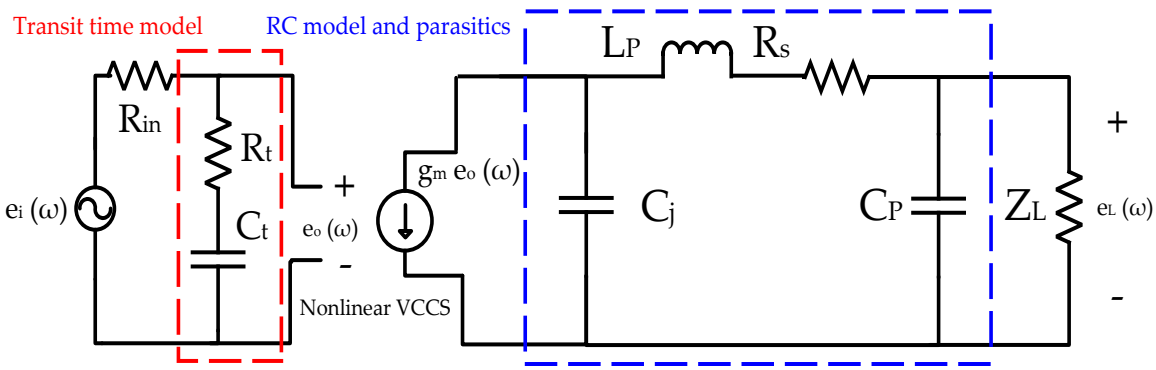


Figure 6.7: Small signal opto-electrical equivalent circuit model for the PIN-photodiodes including both carrier transit time and RC models.

From now on, the high-frequency analysis and discussion will be predominantly concentrated on a 20µm PIN-PD. For the opto-electrical model, the transit delay time denoted as R_tC_t is caused by transport of the created carriers due to drifting in a high electric field. In such a case, deterioration in the speed of carriers in accordance with the depletion region width and the electric field applied would be dramatically pronounced. Owing to RC time constant and delay time effects, the -3dB electrical bandwidth can be formulated as[280]:

$$f_{3dB} = \sqrt{\frac{1}{f_t^{-2} + f_{RC}^{-2}}} \tag{6.1}$$

f_{RC} is given by $1/2\pi(R_L + R_s)C_j$, from the extracted equivalent circuit values, the RC limited -3dB bandwidth is ~17.7GHz. The transit time model, R_tC_t was combined with a nonlinear voltage controlled current source (VCCS), whose main function is to convert the input optical signal into an ac photocurrent, $i_{ph(\omega)}$ expressed as $g_m e_o(\omega)$, where g_m is the dc transconductance[279]. The generated photocurrent flows through the circuit elements. To theoretically estimate the term $g_m e_o(\omega)$, it was evident from the measured optical response with different PIN mesa sizes that $i_{ph(\omega)}$ can be formulated as $g_m e_o(\omega) \backsimeq P_{ph}R_{es}(\omega)$. P_{ph} and $R_{es}(\omega)$ being the incident power of light in Watt and the frequency-dependent responsivity of the photodiode. At $\omega/2\pi \ll f_{3dB}$, $g_m e_o(\omega)$ is approximately equal to the dc photocurrent of the device for a given optical power. The use of an approximated symbol with $i_{ph(\omega)}$ is due largely to the reflected/absorbed P_{ph} at the surface/in the p^+-base region of the devices. By defining the optical power with the voltage generator $e_i(\omega)$ whose impedance R_{in} is 50Ω, the optical response of the circuit was derived and expressed as:

$$20log\left|\frac{e_o(\omega)}{e_i(\omega)}\right| = 20log\left(\sqrt{\frac{1+\omega^2C_t^2R_t^2}{[1+\omega^2C_t^2(R_t^2+R_{in}^2)]}}\right) \tag{6.2}$$

For the sake of simplicity, $g_m e_o(\omega)$ is considered as a source for the following RC model circuit, the relative frequency response can be calculated as:

$$20log\left|\frac{e_L(\omega)}{e_o(\omega)}\right| = 20log\left(g_m\sqrt{\frac{1}{\omega^2(C_P^2+C_j^2)+\omega^4C_P^2C_j^2(R_s^2+L_P^2\omega^5)}}\right) \tag{6.3}$$

The evaluation of the term R_tC_t has been assessed in three steps as follows: the actual absorption layer thickness, D of ~850nm was first calculated from the device respective capacitance C_j at -5V. This gives an electric field of ~58kV/cm, producing an average electron-hole drift velocity (v_s) of ~0.55×10^7 cm/s, which is reasonable for an undoped InGaAs layer and comparable with previous published papers[281]. The -3dB carrier transit time bandwidth is represented by the physical parameter of the PIN-PD structure[280].

$$f_t \backsimeq \frac{3.5v_s}{2\pi D} \backsimeq \frac{1}{2\pi R_tC_t} \tag{6.4}$$

A calculated f_t of 36GHz gives R_t and C_t of 50Ω and 88fF respectively. This resulting f_t demonstrates that the photodiode is evidently limited by its RC time constant. All the extracted or/and evaluated values of opto-electrical circuit parameters were used in the model, providing a well-matched fitting between the simulated and measured data as shown in figure (6.8). A measured -3dB bandwidth of 18GHz for the 20µm PIN-PD was obtained which is a good performance for this relatively large mesa size. This is theoretically adequate for up to 25Gb/s operation (i.e. 7GHz bandwidth is sufficient for 10Gb/s) and appealing for low cost monolithically integrated photoreceiver circuit modules. Measured optical bandwidths of 11.8 and 7.8GHz were achieved for 30 and 40µm photodiodes respectively, offering an outstanding feasibility for the forthcoming generation 10Gb/s EPON optical communication systems.

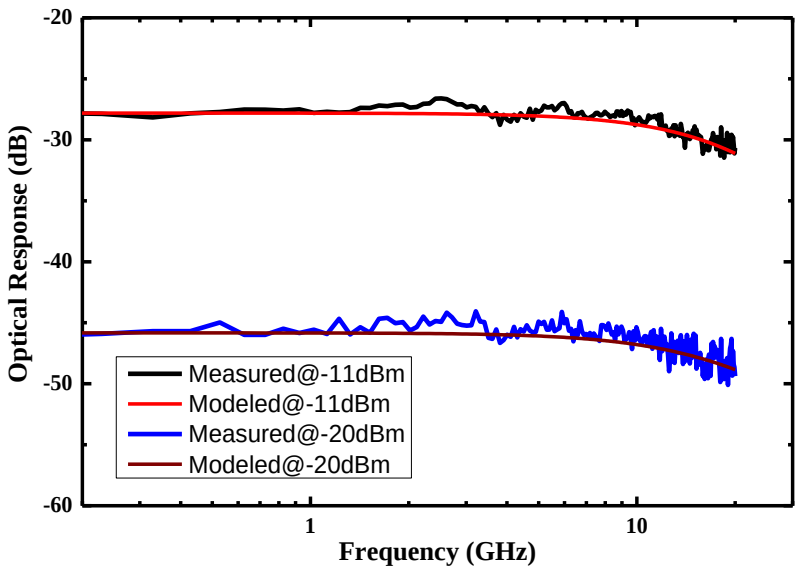


Figure 6.8: Simulated and measured small signal response of the PIN-PD with a window size of 20µm and at a several incident optical power.

The optical bandwidth is expected to be further increased with reduction in the photodiode mesa size and optimum absorption layer thickness. By doing this, the RC limit constant and physical based R_tC_t carriers' delay time are significantly minimized for ultra-high speed operations.

6.3 Vertically Illuminated Photodiodes Compared with Other Technologies

The main endeavour in optical receiver systems is how to maximize the bandwidth of the photodetectors without significantly sacrificing the whole OEIC performance. Based on

this, for the discrete and integrated photodiodes, there are two main ways used to illuminate the photodiodes with a fibre optic namely vertical (both top and bottom) and side illumination methods. The top illuminated devices are the most common and practical way in photoreceivers; however, the down side of this approach is attributed to the trade-off between the carrier transit time and RC limiting factor as well as between the responsivity and high-frequency response of the photodiode. An efficient PIN/APD discrete device does not only require an optimum intrinsic layer thickness but it also necessitates utilizing a semiconductor material with high absorption coefficient. Since the carriers' transport is restricted by the saturation velocity, a bandwidth exceeding ~30GHz is rather difficult to achieve. An alternative approach known as double pass scheme was proposed[281], in which a highly reflective material/metal grown deposited on the top of the substrate or at the back of the device. Such an additional layer reuses the unabsorbed photons which are reflected back towards the intrinsic layer, allowing another absorption opportunity which improves the device's quantum efficiency without increasing the undoped layer width.

The second way is the edge illuminated device or called waveguide photodiode (WGPD), where the light beam is sent through the device's edge. The photons then move into the intrinsic layer in a horizontal path which, in such circumstance, acts as a double core multimode waveguide because it is located between two transparent P and N-type layers. In practise, the intrinsic layer is normally thin (≤1μm); however, its length is in order of several tens of micrometres. The light laterally moves towards the end of the waveguide, providing a very long absorption distance thereby improve the quantum efficiency to about 0.8-0.9. The absorption events will, of course, create an electrical signal (i.e. electron-hole pair generation) which vertically transports across a moderate active layer width with a very small transit time[281]. The use of this promising technique is attractive by firstly maximizing the bandwidth and secondly allowing independence between the quantum efficiency and bandwidth but this is a rather complicated method and adds cost to receiver systems as a mechanism launch light at an angle must be provided. Despite addressing most of the major drawbacks of the vertical illumination method, WGPD optical bandwidth is still limited by the RC time constant, evidently still requiring small device feature sizes. This reduces the overall capacitance of the photodiodes but comes at the cost of an increase in the series resistance.

To get rid of such a trade-off, a new device scheme was proposed in fabricating the photodiodes known as mushroom-like mesa structure[282]. Here, the width of the absorption layer is made thinner compared with the above and underneath highly doped layers, leading to a reduction in the respective capacitance without undesirable influence on the contact resistance of the device. However, the fabrication process of the mushroom mesa photodiodes necessitates particular care to control the excessive undercut profile and does not actually provide scalable device characteristics due to the difficulties in precisely controlling the inner diameter of the intrinsic layer. It is well-known that photodiodes with small window sizes/side-illuminated become indispensable for the sake of smaller depletion capacitance/shorter delay time across the absorption layer. The use of such technologies is at the expense of an increase in manufacturing cost and difficulty of associated fibre optic alignment. Therefore, a surface illuminated, low cost HBT-PIN based OEICs receiver is undeniably the best approach for high performance10Gb/s EPON optical transmission systems.

6.4 Transistor Mask Design and Layout

Layout design for desirable electronic device performance necessitates avoiding any needless lengths or lines on the circuits that would affect the high-frequency response. However, this is constrained by the resolution of the photolithography technology used and clean room facilities. Throughout the work of this PhD research, photo-mask designs for HBT devices was built using Keysight-ADS software with different number of transistors' emitter sizes, 10×10 down to 4×9μm^2. Since no finger devices or small features were involved, a simple process was utilized instead of the standard self-aligned ones as will be discussed in this section. The mask also included dummy and test structures, such as open and shorts modes as well as various via dimensions and TLM test structures. The full fabrication process is constructed from six steps in total and an example of a 10×10μm^2 emitter size HBT fabrication is shown in figure (6.9). The first three steps are dedicated to defining the emitter, base and collector mesa sizes (step#1, #2 and #3), allowing the transistors to be electrical isolated from other neighbouring devices. The isolation is performed down to the semi-insulating substrate surface where the resistivity of the InP substrate is much higher than those exhibited by the doped active layers. As the highly doped InGaAs base and sub-collector layers do not act as etch-stop layers, the mesa etching time must be carefully adjusted to ensure that the

etching process stops where the base and collector electrodes are to be defined. The contact to all terminals can be then defined with a 1µm emitter-base and 1.5µm base-collector contacts spacing. This is to improve the yield process by avoiding short circuits among the contacts (step#4) as depicted in figure (6.9).

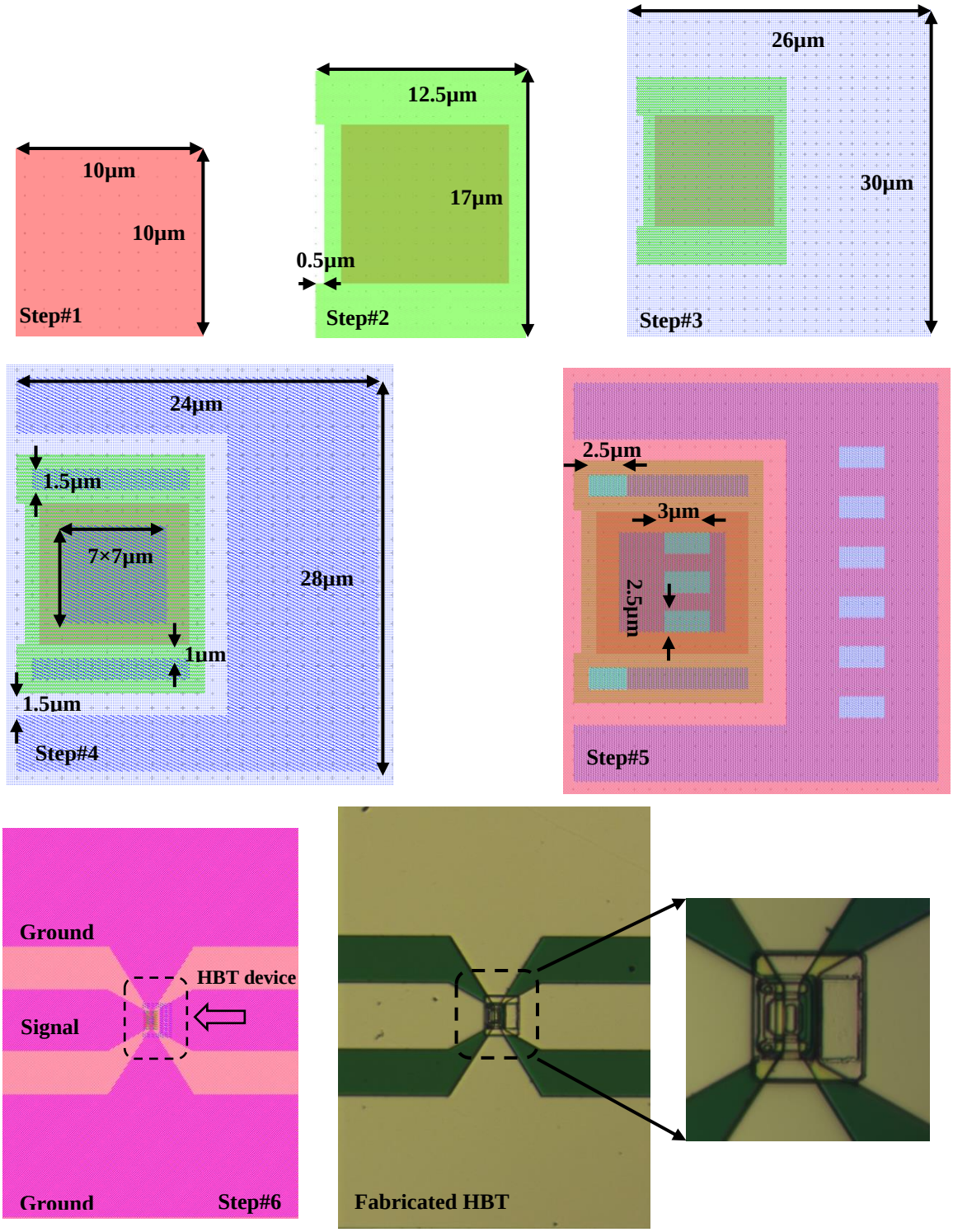


Figure 6.9: Top view of the HBT photo-mask designed in Agilent-ADS software presenting the process flow step by step for a 10×10 µm^2 emitter size HBT as defined by mask patterns along with photomicrograph of the fabricated HBT discrete devices with the same emitter size.

Due to the horizontal undercut profile, the separation between the base contact and emitter mesa is approximately 1.5µm. This latter spreading distance plays a pivotal role in determining the high-speed performance of the HBTs. A detailed investigation regarding the pronounced effect of the contact spacing on f_{max} will be discussed later in this chapter. After lifting-off the metallization, a dielectric is sputtered everywhere in order to passivate the active layers and facilitate the interconnect routing, followed by opening the predefined vias with different sizes (step#5). The final step is to deposit the metallization scheme of the interconnections and bond-pads for on-wafer probing measurements and by lifting-off this metal, the devices are ready to be tested (step#6). All these steps are depicted in figure (6.9) showing the pattern dimensions designed in the mask and alongside photomicrograph of the fabricated 10×10µm^2 HBT discrete devices. The dimensions of the coplanar waveguide were established to provide the standard 50Ω characteristic impedance necessary to match with the VNA microwave measurements.

6.5 Device Structure and Fabrication

The HBT epitaxial layers shown in Table (6.1) utilised a small band-gap heavily doped InGaAs top cap layer to alleviate the series resistance of the emitter contact. A 5nm spacer layer was employed to reduce the potential spike and dopant out-diffusion at the emitter-base interface, resulting in lower offset voltage in the I-V characteristics of the devices. This is also beneficial in maintaining a low sheet resistance value at the base layer to maximize the high-frequency response. Generally, the challenge in growing a high-quality epitaxial structure for HBTs is to grow a very highly doped base layer with a doping concentration reaching 4×10^{19} cm^{-3} using Beryllium (Be) and making the base as thin as 40nm. The main reason for utilizing a thin spacer layer and 4×10^{19} cm^{-3} dopant level in base of the HBT devices is to satisfy the requirements for a very low out-diffusion in the emitter. The high diffusivity of Be-dopants leads to a high out-diffusion into the emitter region during the growth process[283], which in turns contributes to the formation of a homojunction between the original emitter layer and the new diffused p-doped layer in the emitter. This has a severe impact on the current gain of the device and gives rise to a high collector ideality factor. To address this issue, Carbon (C) has been used as a dopant in the literature because its out-diffusion is less than that of Be[284, 285]. However, C-doping leads to multiple difficulties in InGaAs layers, for example the

SSMBE technique uses graphite as a typical source for carbon, but this comes at the expense of high melting points compared with other commonly employed solid sources in MBE hence special design of effusion cell is required. Furthermore, a Be doped layer with a doping density of 2×10^{19} cm^{-3} exhibited a resistivity similar to that of $4\text{-}5\times10^{19}$ cm^{-3} C doping [230], as result of the smaller hole mobility in heavily carbon doped InGaAs and thus carbon as a dopant in InGaAs does not actually outperform Be.

The use of an undoped collector layer not only helps to increase the breakdown voltage and minimize the base-collector capacitance, but also serves as the absorption layer for the photodiode. Due to the trade-off between high-frequency performance of HBTs and responsivity of PIN-Photodiodes, the intrinsic layer was designed to be 800nm. The process commenced with fabricating and testing both the HBTs and PINs to be integrated in the front-end receiver. The individual devices were fabricated using standard i-line photolithography and wet etching process to first create the emitter mesa with a size of $10\times10\mu m^2$. This size was chosen so that a low cost, high yielding process is developed for 10Gb/s and greater integrated photoreceivers. This was followed by etching away the surrounding area to the p+-InGaAs base layer. In the same manner, base and collector mesas were defined, allowing both devices (HBT and PIN-PD) to be completely isolated from other neighbouring devices. Next, a combination of SiO and Al_2O_3 was sputtered for passivation and interconnect routing. The final step was the interconnect metal, including ground plane, input/output RF and DC biasing pads. The metallization of PINs and HBTs contacts used the non-alloyed ohmic contact scheme of Pd/Ti/Pd/Au with a total thickness of ~1µm. To reduce the extrinsic series resistance of the base while maintaining high a yield process, the spreading distance between the base contact and the device structure was optimized to be 1.5µm.

Figure (6.10) shows a 3D schematic of a fabricated HBT transistor, highlighting the active device layers and emitter, base and collector contacts. Once the fabrication process was successfully accomplished, the HBT devices were measured and an example of a I_C-V_{CE} characteristics for a common emitter device with a $10\times10\mu m^2$ emitter size is depicted in figure (6.11). The HBT used has a breakdown voltage of approximately 4.5V and a dc current gain, β of ~65 at a bias condition V_{CE}=2V and I_C=10mA. The measured base sheet resistance was found to be 592Ω/□ extracted from the TLM measurements.

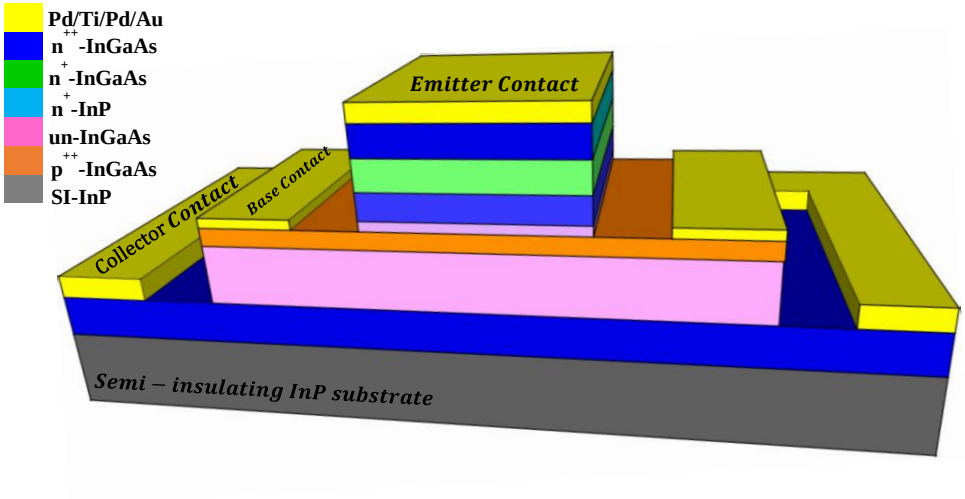


Figure 6.10: 3D schematic of the fabricated HBT transistor with an emitter size of 10×10μm^2, indicating the active device layers and emitter, base and collector contacts.

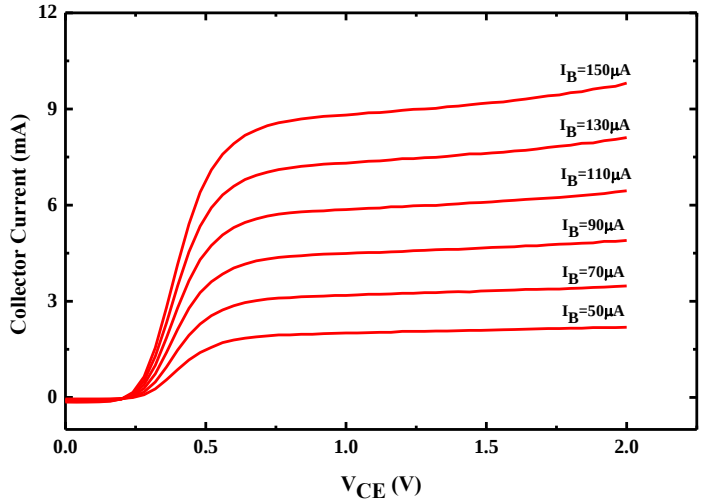


Figure 6.11: Measured I-V characteristics of the common emitter InP/InGaAs HBT sample F17D2102A with a 10×10μm^2 mesa size.

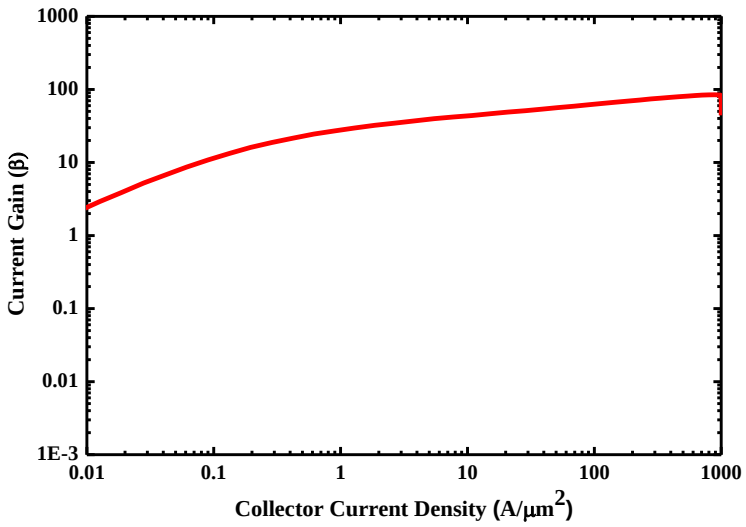


Figure 6.12: Current gain versus collector current density measured at room-temperature for HBT sample F17D2102A with a 10×10μm^2 mesa size.

Figure (6.12) shows the room temperature measurements of the current gain as a function of collector current density. The transistor reveals good linearity over at least two to three orders of magnitude of collector current; nevertheless, low current gain is observed at low collector current density. This might be due to surface recombination component on the surface of the spreading distance between the emitter and base contacts. Reducing these contacts spacing can effectively alleviate this effect, thereby leading to high-speed operation improvement. This requires exploitation of a self-aligned technique, in which several metallization and lift-off schemes are used. As a standpoint, for unity gain cut-off frequency greater than 100GHz, small transistor feature sizes ($\leq 4\times4\mu m^2$) with about 0.5µm or less contacts spacing are indispensable.

6.6 HBT Physical Modelling

As stated in chapter five, the doping profile of spacer layer and its thickness play a pivotal role in establishing the DC characteristics for the HBTs. To further highlight this effect, the commercially available software Silvaco-ATLAS was used in this work[286]. This physical based software is not only able to provide insight into DC and small signal AC analysis but it can also predict transient performance of electronic devices. This is performed with physically analysing the internal device parameter characteristics including conduction and valence band energies, electric fields, electron and hole concentrations. Furthermore, Silvaco-ATLAS offers a wide range of terminal characteristics in particular I-V curves, frequency response and high-frequency scattering parameters. A number of statements must be defined to correctly model a structure in the ATLAS simulator:

- Definition of physical dimensions: The fabricated or designed device structure in relation to individual layer thickness, doping profile and electrodes are required using the statements: MESH, REGION, ELECTRODE and DOPING.
- Material specification: The physical properties of the semiconductor materials used to build the epilayer structure of the device are defined by the following statements: MATERIAL, MODELS, CONTACT and INTERFACE statements.
- Models: The numerical methods in ATLAS are used to solve the structure based on a specific model using METHOD and Output statements. It is recommended that an initial guess for some variables is necessary with particular models such as Newton, GUMMEL

and BLOCK methods which can assist to circumvent convergence problems during the simulation run.

- Solution condition: To obtain the device DC and AC characteristics, the device is solved under specific biasing conditions. The outcome is initially solved and recalled afterwards using LOG, SOLVE, LOAD and SAVE statements.
- Result extraction: The simulation results can be ultimately plotted using TONYPLOT command.

As the existing database of ATLAS has been primarily designed for Silicon based devices, it is imperative to define the physical properties of III-V materials, for example energy bandgap, mobility, affinity and carrier's effective mass. Other than basic parameters, physical models might be important to specify (i.e. concentration and electric field dependent mobility models and recombination mechanisms) since they have a substantial impact on the device performance. In this work, the epitaxial stack layer of HBT sample F17D2102A tabulated in Table (6.1) was modeled in the two-dimensional ATLAS simulation tool with adaptive meshing steps, which gets denser in thin layers. This is to avoid uncertainty or/and convergence errors in the simulation results. The energy band diagram was simulated as shown in figure (6.13).

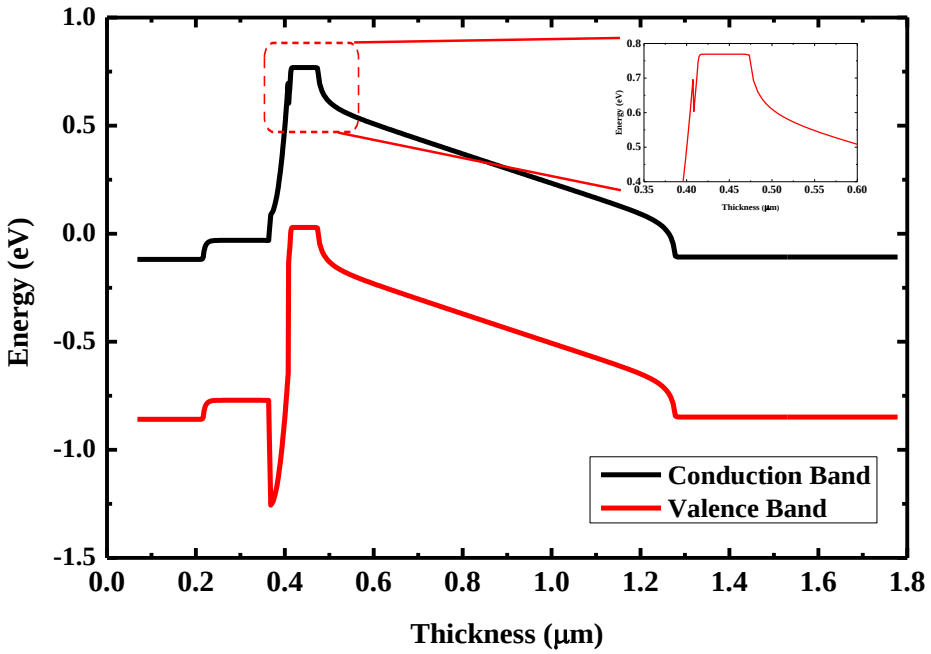


Figure 6.13: Energy band diagram of HBT sample F17D2102A with a 5nm undoped spacer layer.

The structure was modeled under the assumption that the 5nm spacer is intentionally undoped, allowing further to minimize the potential spike at the E-B heterojunction. However, in practice, Be out-diffusion can contribute to undesirable effect on the DC characteristics of the device. Figure (6.14) shows the impact of various doping levels in the spacer layer on the energy band structure at the emitter-base interface. It can be observed that the potential spike increases as the doping concentration gets higher, leading to a higher offset voltage in the I-V characteristics. However, a highly doped spacer may increase the current gain of the transistor due to a reduction in recombination event in such a layer. This can also contribute to improving high frequency performance benefiting from carrier ballistic transport.

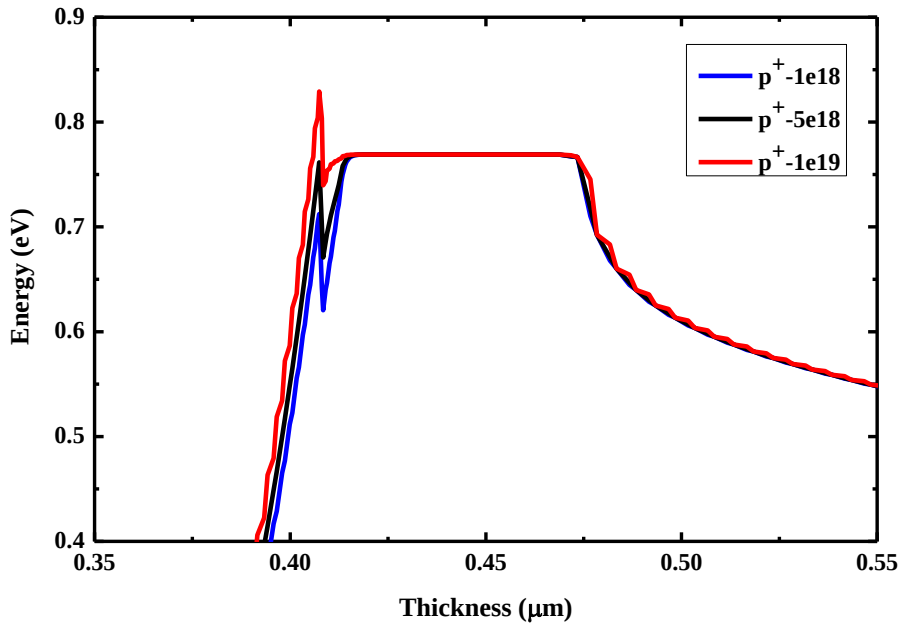


Figure 6.14: Energy band diagram of HBT sample F17D2102A showing the effect of various doped spacer on the height of the potential spike.

6.7 HBT Characterizations

For solid state electronic devices, the analysis of the experimental results is of vital importance to ascertain the quality of the devices and to allow understanding of measured data. Moreover, it is highly useful in accurately modeling the electronic devices, which eventually provide good agreements with the acutal measured results. This section thus, presents the fundamental and widely used characterisation techniques for HBT transitors, namely DC and RF features.

6.7.1 High-Frequency Measurements and De-embedding Techniques

In this work, the high frequency measurements were performed using on-wafer probing techniques. Two ports S-parameter measurements were carried out employing Anritsu 37369A VNA up to 40GHz and the instrument was controlled by ICCAP software from Keysight. To minimize errors in high frequency and achieve as accurate results as possible, a number of calibration steps prior to commencement with DUT (Device under Test) measurements need to be carried out. Systematic errors due to cable losses and non-ideal probe impedance (i.e. $Z_o = 50 \pm jX$ instead of 50Ω) must be eliminated by establishing a reference plane for the scattering data up to probe tips with neither error nor losses introduced. There are a few calibration methods that can be utilized to remove the systematic errors for reliable and repeatable measurements, these methods are SHORT-OPEN-LOAD-THRU (SOLT), THRU-REFLECT-LINE (TRL) and LINEREFLECT-MATCH (LRM) or LINE-REFLECT-REFLECT-MATCH (LRRM). The advantages and disadvantages of these various methods are broadly discussed in[287, 288].

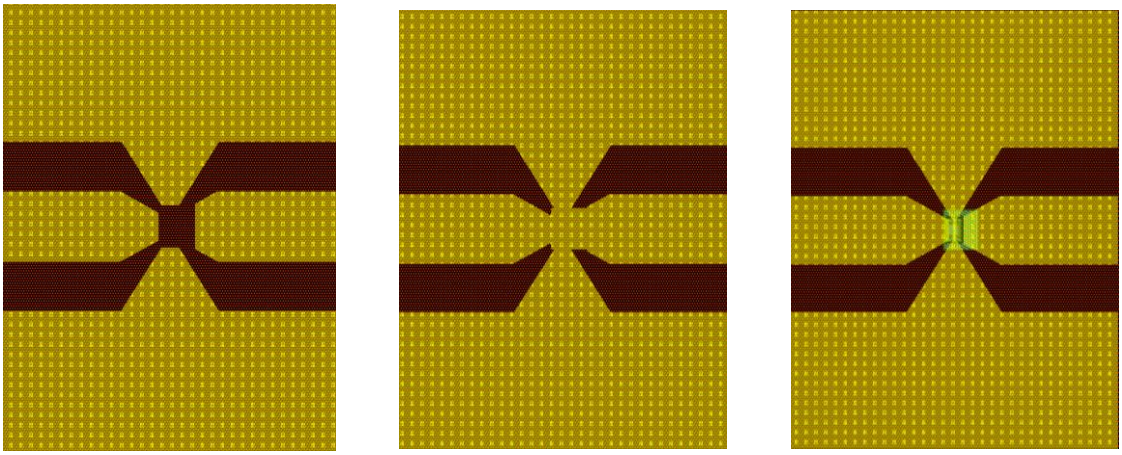


Figure 6.15: The fabricated layout for two step de-embedding method, including open and short dummies and actual device.

Since a coplanar waveguide structure is required for direct probe measurements, which causes an additional pad capacitance and interconnect inductance, de-embedding techniques are inevitably required. This is to assess the intrinsic device performance by a procedure including two or three steps[167, 215]. Despite the high accuracy of the three-step de-embedding technique, the two-step one was used in this research as it is less complicated and can yield acceptable error margins. To perform the de-embedding steps, open and short structures were fabricated alongside the actual device as depicted in figure (6.15).

Step1: The measured two ports S-parameter data are firstly converted into Y-parameters using Keysight-ADS software to simplify the mathematical de-embedding procedure as described in the following set of equations:

$$Y_{DO} = Y_{Actual} - Y_{Open} \tag{6.5}$$

$$Y_{SO} = Y_{Short} - Y_{Open} \tag{6.6}$$

Y_{Actual} being the Y-parameters of the actual device involving the impact of the bond-pads, while Y_{Open} and Y_{Short} are the Y-parameters of the open and short dummies respectively.

Step2: Z-parameters of Y_{DO} and Y_{SO} are obtained by $Z_{DO} = [Y_{DO}]^{-1}$ and $Z_{SO} = [Y_{SO}]^{-1}$ followed by calculating the Z-parameters of the DUT as given by:

$$Z_{DUT} = Z_{DO} - Z_{SO} \tag{6.7}$$

The Z_{DUT} of the two-port are ultimately converted into S-parameters, which represents the de-embedded measured results of the DUT. The equivalent circuit diagram of all the above steps is shown in figure (6.16).

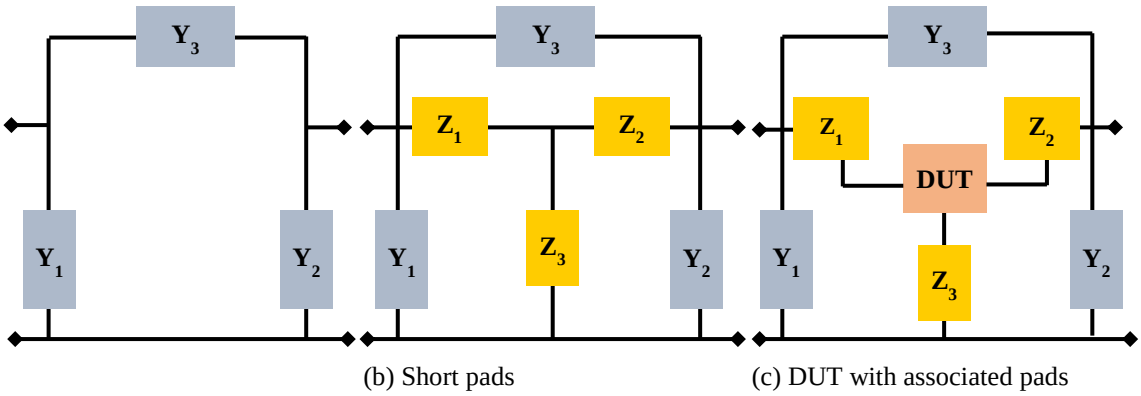


Figure 6.16: Equivalent circuit diagrams for two steps de-embedding technique, representing the device under test and the additional parasitic elements of the open and short dummies.

Before applying the de-embedding routine, the scattering data performance of the actual HBT is noticeably resistive and inductive with the capacitive bond-pads. However, this behaviour becomes approximately resistive (and slightly capacitive), asserting that a parasitic inductance can be used to compensate the uncertainty error in the de-embedding process.

6.7.2 HBT Empirical Modeling

The empirical models for transistors are of significance in characterization and circuit simulation where the performance of a single HBT is modeled using a list of physical

based parameters. The parametrical modeling methods falls into two main types; small-signal (or known as linear model) and large-single (or non-linear model). In the first category, the variations in the input signal are small, allowing the characteristics of the devices to be approximately independent on the input signal size.

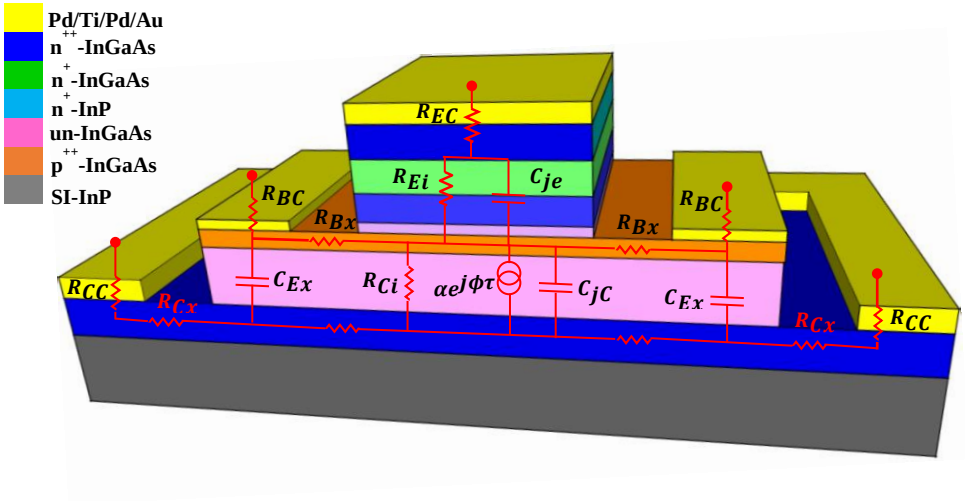


Figure 6.17: 3D schematic of an HBT device structure onto which is superimposed the small signal model elements.

The performance of the HBT can be, therefore, represented by linear electrical components and equations. In such a scenario, the extraction of the small signal model parameters is simply carried out from the measured S-parameters data or applying a numerical optimization approach until an agreement between the experimental and simulated results is successfully accomplished[289, 290]. The linear model can offer great accuracy; however, it suffers from validation difficulties over certain large signal operating conditions. This implies that the large-signal model is actually necessary, in which the non-linear electrical elements exhibited in the device performance are taken into account. A 3D schematic diagram of an HBT structure on which are superimposed the electrical elements of the small-signal equivalent circuit model is depicted in figure (6.17).

6.7.3 Limitations of Gummel-Poon Model

The first commonly utilized large-signal model adequate for silicon bipolar transistors is the Gummel-Poon model, which was introduced in the late 1960s[291]. The SPICE Gummel-Poon (SGP) is still the standard model in most of the SPICE simulation software due to its enhancement in modeling early effect, Webster effect and partitioning

of the base-collector capacitance into intrinsic and extrinsic components[292]. Despite the good success of the SGP model in silicon-based BJTs parametrical modeling, it does not take into account several remarkable characteristics prevalent in HBTs. These are the excess stored charge at the heterojunctions caused by the band discontinuities and the velocity modulation effect of the III-V materials, in which a decrease in the carrier drift velocity occurs due to high applied electric fields[293]. Furthermore, the collector delay time is paramount in determining the RF characteristics of the HBTs, distinctly affected by the velocity overshoot of the III-V material properties. However, Gummel-Poon model presumes that the unity gain cut-off frequency, f_T enhances as the biasing conditions and collector current density get higher[255]. The dependency of the device's gain on the collector current is not included in the model[294], emphasizing that Gummel-Poon model is solely valid for Si-based BJTs. Due to these marked limitations, this model was not employed in this work.

6.7.4 Large Signal UCSD HBT Model

To overcome the limitations of the Gummel-Poon model, extensive efforts have been devoted that have culminated into different proposed models, including a modified Gummel-Poon model[295] as well as an advanced model which take the self-heating and impact ionization effects into account[296]. A milestone HBT model reported by Camnitz *et al* and then developed at the University of California, San Diego (UCSD) with cooperation from industry and known as the UCSD HBT model, is the most appropriate physically based model for use in heterojunction device characterizations. This large-signal model is widely used by several commercial simulators, such as Silvaco, SPICE and recently Keysight-ADS software from Agilent and called AGILENTHBT model as shown in figure (6.18)[297]. Intrinsic and extrinsic portions of the device overlap the layer structure to relate these elements to the physically-based source. The implemented UCSD model was used to supplement developments by Agilent technologies to improve the capabilities of the model in terms of mathematical consistency and numerical simplicity. In this model, the potential spike at the heterointerfaces is taken into account to deal with the effect of the current gain variation on the current density of the HBT. Additionally, degradation in high-frequency parameters response due to Kirk effect and self-heating issue can be modeled as well.

The UCSD large signal model utilises π-topology to represents the intrinsic device elements and likewise in Gummel-Poon model as shown in figure (6.18).

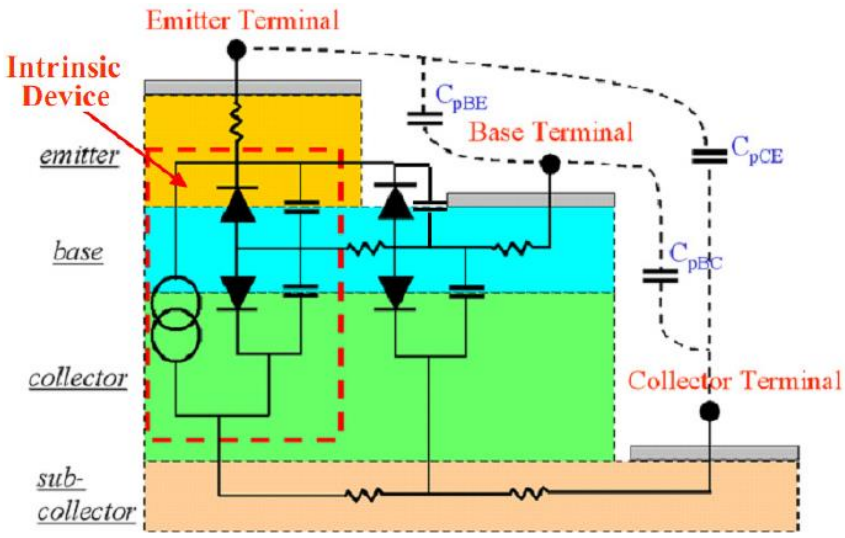


Figure 6.18: HBT transistor overlapped large signal UCSD Model, showing the intrinsic and extrinsic portions of the device[297].

6.8 UCSD-HBT Model Parameter Extraction

The complete large-signal UCSD-AGILENTHBT model, depicted in figure (6.19), consists of a large number of geometry-dependent and physically-based parameters as tabulated in Table (6.2). In this work, there is no need to define some of the variables particularly those that were already excluded from the HBT performance, for example the parameters associated with the parasitic capacitance and inductance of the pads.

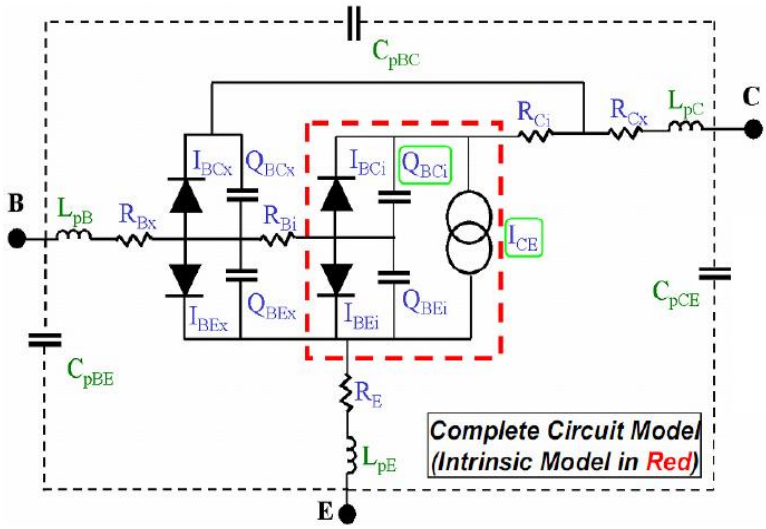


Figure 6.19: Large-signal topology of the AGILENTHBT model[297].

This helps to further reduce both the complexity and the time-consuming execution of the simulation routine, while still maintaining the accuracy of the modeling results. The UCSD modeling parameters are classified into eight different groups as illustrated in Table (6.2) and in-depth description of these variables is given in Appendix-B. In this work, the biasing conditions of the HBT transistor is relatively low in the simulation set-up so that the impact of the thermal effects is negligibly small; therefore, the associated parameters were ignored. From the integrated circuits modeling perspective, the first step is to extract the DC and RF parameters for the discrete devices. To do so, several approaches have been demonstrated in the literature[289, 298]. However, this research was primarily concerned with performing the DC and RF measurements at various biasing conditions. The extraction method was commenced with the de-embedding of the parasitic components surrounding the HBT transistor, followed by accurately modeling the common emitter I-V characteristic and forward and reverse Gummel plots. These curves were employed to extract the "*DC-Current*" parameters as well as to roughly evaluate the device's resistances.

TABLE 6.2: UCSD-AGILENTHBT MODELING PARAMETERS.

Tnom=25.0	Nrh=2.0	Gkdc=0.0	Abcx=0.75	Fextc=0.8	Lpc=0.0 H	Egc=1.5 V	Rth1=1000.0
Re=2.0 Ohm	Isc=1.0e-13 A	Ik=1.0 A	Tfb=1.0e-12 sec	Tkrk=1.0e-12 sec	Lpe=0.0 H	Xtir=3.0	Cth1=5.0e-10
Rci=1.0 Ohm	Nc=2.0	Cje=4.0e-14 F	Fextb=0.2	Ikrk=0.025 A	Xrb=0.0	Xtic=3.0	Xth1=0.0
Rcx=5.0 Ohm	Abel=0.0	Vje=1.3 V	Tfc0=2.0e-12 sec	Ikrktr=1.0e-6 A	Xrc=0.0	Xtirh=4.0	Rth2=0.0
Rbi=15.0 Ohm	Vaf=500.0 V	Mje=0.3	Tcmin=5.0e-13 sec	Vkrk=3.0 V	Xre=0.0	Xtik3=0.0	Cth2=0.0
Rbx=5.0 Ohm	Var=1000.0 V	Cemax=1.0e-13 F	Itc=0.006 A	Vkrk2Inv=0.2	Tvje=0.0	Eaa=0.0 V	Xth2=0.0
Is=1.0e-25 A	Isa=1.0e+10 A	Vpte=1.0 V	Itc2=0.008 A	Gkrk=4.0	Tvpe=0.0	Eab=0.0 V	Kf=0.0
Nf=1.0	Na=1.0	Mjer=0.05	Vtc0Inv=0.3	Vktr=1.0 V	Tvjc=0.0	Xtfb=0.0	Af=1.0
Isr=1.0e-15 A	Isb=1.0e+10 A	Abex=0.0	Vtr0=2.0 V	Vkmx=1.0 V	Tvpc=0.0	Xtcmin=0.0	Ffe=1.0
Nr=2.0	Nb=1.0	Cjc=5.0e-14 F	Vmx0=2.0 V	Fexke=0.2	Tnf=0.0	Xtfc0=0.0	Kb=0.0
Ish=1.0e-27 A	Ikdc1=1.0 A	Vjc=1.1 V	VtcminInv=0.5	Tr=1.0e-09 sec	Tnr=0.0	Xitc=0.0	Ab=1.0
Nh=1.0	Ikdc2Inv=0.0	Mjc=0.3	Vtrmin=1.0 V	Cpce=1.0e-15 F	Ege=1.55 V	Xitc2=0.0	Fb=1.0 Hz
Ise=1.0e-18 A	Ikdc3=1.0 A	Ccmax=9.0e-14 F	Vmxmin=1.0 V	Cpbe=1.0e-15 F	Xtis=3.0	Xtkrk=0.0	Imax=10.0 A
Ne=2.0	VkdcInv=0.1	Vptc=3.0 V	VtcInv=0.1	Cpbc=1.0e-15 F	Xtih=4.0	Xikrk=0.0	AllParams
Isrh=1.0e-15 A	Nkdc=3.0	Mjcr=0.03	Vtc2Inv=0.1	Lpb=0.0 H	Xtie=3.0	Xvkrk=0.0	
Resistances: 5		DC Currents: 26		Depletion Charge: 14		Delay Charge: 25	
Parasitics: 6		Temp, DC & R's: 22		Temp., Charges: 12		Noise: 6	

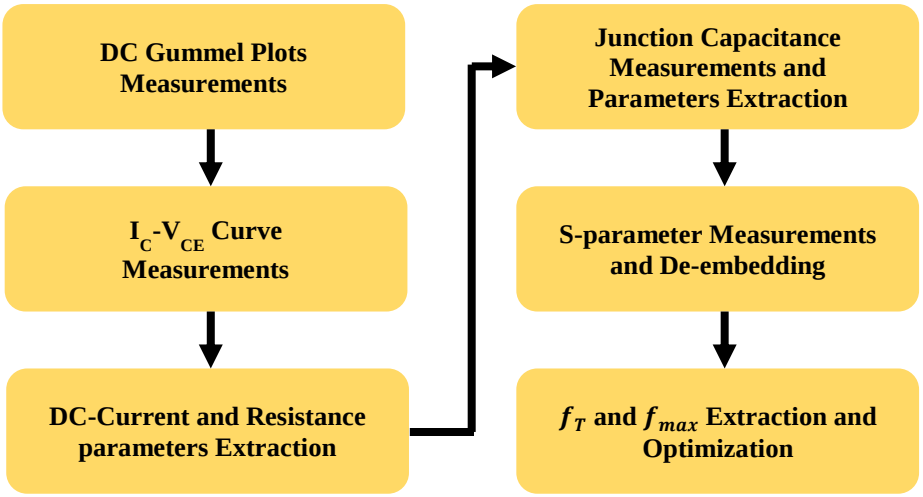


Figure 6.20: Flow chart representing the parameters extraction and modeling procedure used in this work.

The accurate values of the emitter, base and collector resistances were then found from the fabricated TLM test structures and S-parameter measurements. Afterwards, the parameters and their accompanying "*capacitances*" were obtained from the measured B-E and B-C junction capacitances under the appropriate bias voltage. The "*depletion charge*" and "*delay charge*" variable parameters can be calculated as well. The RF figures of merit, f_T and f_{max} curves were eventually simulated using numerical optimizations to eliminate any unintentional error which might be introduced during the parameter extraction procedure. This was reflected into achieving a good agreement between the simulation and experimental results as presented in the following sections. The extraction procedure and HBT modeling steps carried out in this research are shown in the flow chart in figure (6.20). Note that the way forward/reverse Gummel plots, emitter/base/collector resistance and base-emitter/base-collector capacitance curves were tested and how their respective parameters were obtained are discussed in the following sections.

6.8.1 DC Current Parameters Extraction

The measured forward and reverse Gummel plots are typically used to extract "*DC - Current*" parameters as illustrated in figure (6.21) in which the extractable DC parameters with a given recommended region are highlighted. The detailed description of the all parameters is listed in Appendix B. Once all variables were obtained, an optimization routine was performed with a tolerance error of 10-15% to consistently

achieve good matching with the measured results. As a rule of thumb, multiple variables could be affected by the curve's behavior due to unavoidable fluctuations or difficulties in recognizing the suitable region, in such a scenario, it is advisable to activate only one parameter and disable the others in the tuning process. This offers the opportunity to look into the maximum sensitivity of one variable without being disturbed with the effect of the others. For instance, this can be performed by setting Ish to 1×10^{-26} and Nh to 5 while extracting Ise and Ne from the forward Gummel plot, so further minimizing the influence of Ish and Nh on I_B [299].

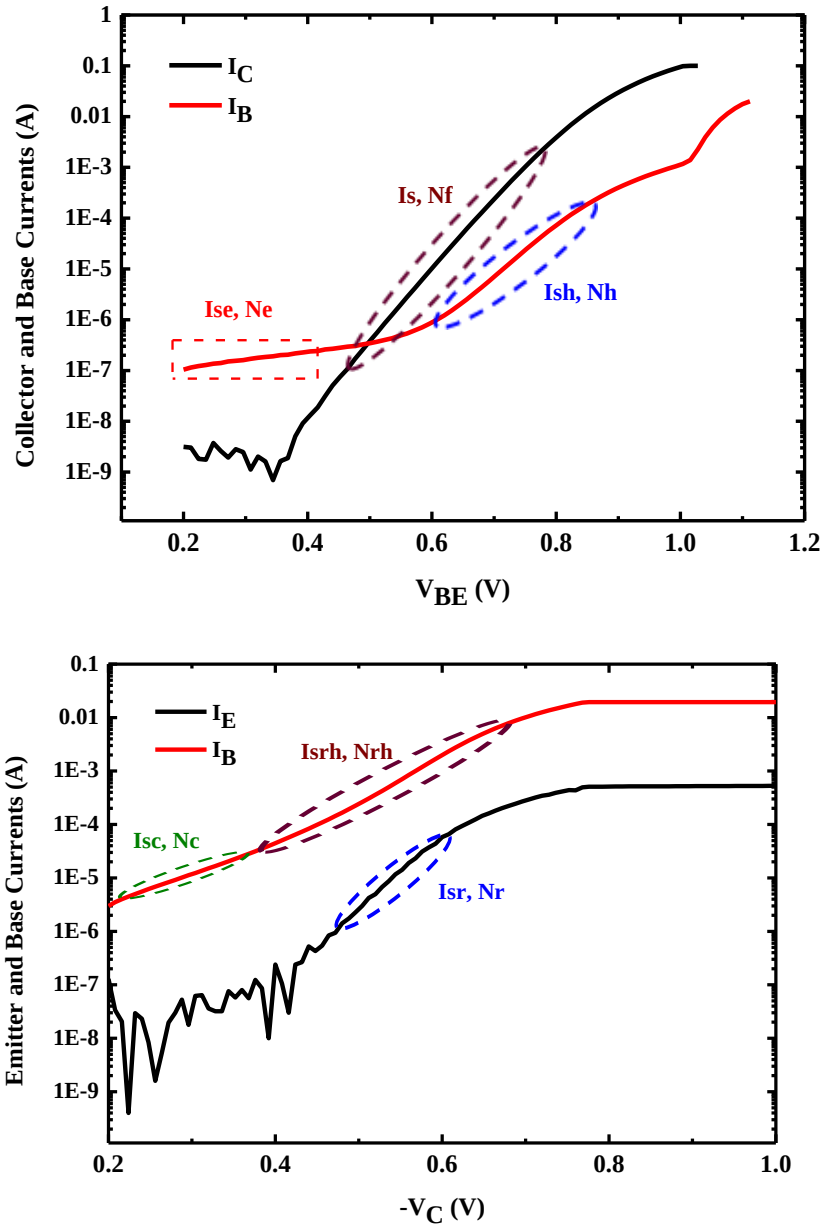


Figure 6.21: Forward (top) and reverse (bottom) Gummel plots showing the list of extractable parameters from the traces of I_C, I_B and I_E graphs with a recommended region for each parameter.

6.8.2 Extraction of Emitter, Base and Collector Resistances

As stated in the previous section, the resistances of the emitter and collector can be roughly estimated from the forward Gummel plot. However, the incorporated self-heating effects could contribute to creating an uncertainty in evaluating the actual resistances values. The S-parameter measurements were therefore employed to extract the devices resistances, which was carried out by overdriving the transistor with a high base current of ~5mA, known as "*Over Driven I_B*" demonstrated by Lee *et al*[300].

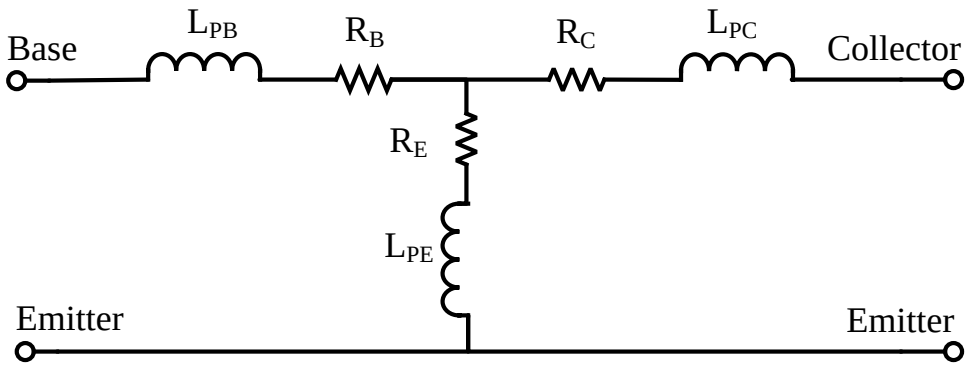


Figure 6.22: Equivalent circuit model for HBT device for high base current or over driven I_B.

The idea is to forwardly bias the emitter-base and base-collector junctions (i.e. operating in saturation region, $V_{CE} \simeq 0$), leading to linearly but asymmetrically distributing the base current between the collector and emitter. In practise, this forces the dynamic junction resistance of the HBT to be approximately zero for high external base currents[301], in other words, the resistive behaviour of the resulting data is due solely to series resistances of the device. However, there is still an additional small capacitive contribution in the *Over Driven* equivalent circuit model, requiring an inductance (L_{PB}, L_{PE} and L_{PC}) to be connected in series with the model to get rid of the remaining capacitive effect as depicted in figure (6.22). Hence, this model can be exerted to evaluate the emitter, base and collector resistances as follows:

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_B + R_E + j\omega(L_{PB} + L_{PE}) & R_E + j\omega L_{PE} \\ R_E + j\omega L_{PE} & R_C + R_E + j\omega(L_{PC} + L_{PE}) \end{bmatrix} \tag{6.8}$$

Emitter Resistance: The emitter resistance is of importance in determining both the emitter-base junction capacitor charging time, τ_{EB} and the transconductance of the device, g_m. It is highly useful for DC and RF characteristics to keep the emitter

resistance in the order of several Ohms which is made up of a combination of the contact and epitaxial layer structure resistances as shown in figure (6.17).

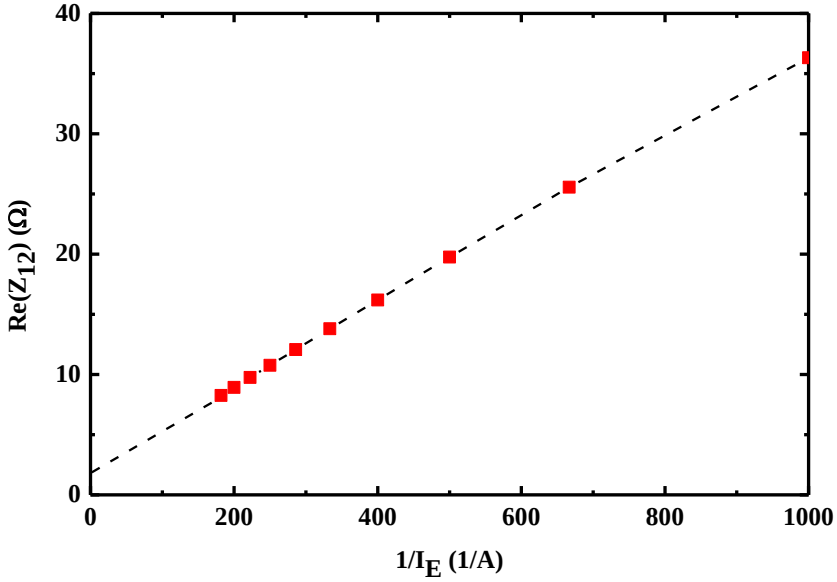


Figure 6.23: Extraction of the emitter resistance, showing R_E value at the intercept of $real(Z_{12})$ with y-axis.

The total emitter resistance can be approximately given by the real part of the small signal two-port Z-parameters network.

$$real(Z_{12}) \simeq R_E + \frac{1}{\delta I_E} \tag{6.9}$$

δ being a constant of proportionality. To extract R_E, the *Over Driven* HBT was tested with various I_E values, $real(Z_{12})$ can be then plotted as a function of $1/I_E$ and the extrapolated line at which the term $(1/I_E)$ is equal to zero gives the emitter resistance as depicted in figure (6.23). This extraction method was reported by Maas *et al*, which is often performed at low frequencies ranging from 3 to 10GHz[298]. For a similar objective, various alternative approaches have been demonstrated[290, 301]. Even though the mesa size of the HBT device is 10×10μm^2 with a heavily doped InGaAs cap and emitter layers, the contact resistance is inevitably dominant over the negligibly small epi-layer resistance component, indicating an overall low emitter resistance of 2.4Ω.

Base Resistance: The design of the HBT base layer for low resistance and small transit time value in terms of thickness and doping profile as well as emitter-base contact spacing is not only fundamental in maximizing f_{max} but also in overall device performance. Irrespective of the resistance of the metal interconnections, the total base resistance can be expressed as $R_B = R_{BC} + R_{BX} + R_{BI}$, where R_{BC}, R_{BX} and R_{BI} are the contact resistance, extrinsic and intrinsic resistances of the base respectively. R_{BC} is often extracted from the TLM measurements as earlier discussed in chapter two. The specific contact resistance of the base contact was found to be ~38Ω/μm^2 and $R_{BC} = 38/B_{area}$ where B_{area} is the area of the base contact. The extrinsic base resistance is due to the lateral path of the current through the base-emitter contact separation. However, the intrinsic resistance component is caused by the base current which horizontally enters the base and does not arrive at the other side of the active device mesa because of the occurrence of recombination events at various locations in the base region. Thus, R_{BI} is not literally a physical resistance, but it is doping profile dependent instead[299]. The participation of the extrinsic and intrinsic components in the overall base resistance is based on the well-known partitioning of 20 and 80% respectively[233]. In this work, the measurement set-up of the *Over Driven* HBT was performed and the resulting two-port Z-parameters given in equation (6.8) was used to extract the base resistance as shown in figure (6.24).

$$R_B \simeq real(Z_{11} - Z_{12}) \tag{6.10}$$

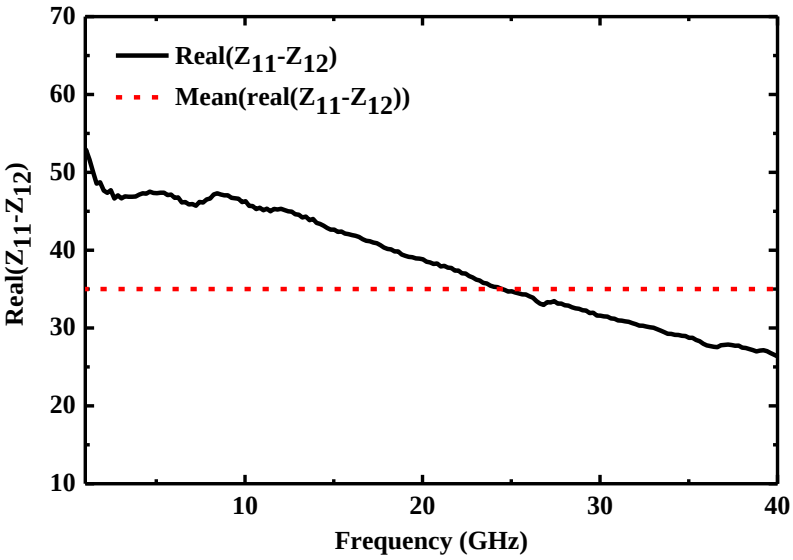


Figure 6.24: Base resistances extraction procedure used in this work.

Collector Resistance: The collector resistance, R_C is made up of two main parts: the contact resistance, R_{CC} and spreading resistance, R_{CX} (this results from the epitaxial layer resistance being negligible and so was disregarded). The extracted collector resistance based on the *Over Driven* HBT over a range of frequencies is depicted in figure (6.25).

$$R_C \simeq real(Z_{22} - Z_{12}) \tag{6.11}$$

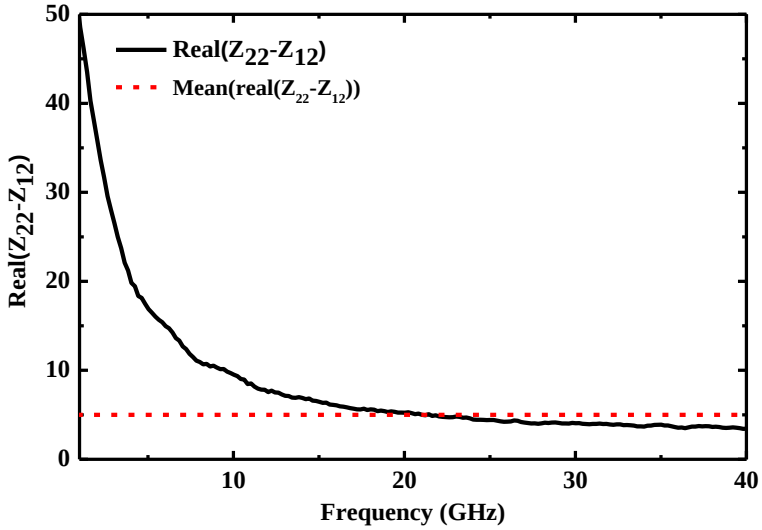


Figure 6.25: Collector resistances extraction procedure used in this work.

6.8.3 Extraction of Junction Capacitances

The HBT BE and BC depletion capacitances and their related parameters were extracted from the measured S-parameter data at constant mid-range frequency between 2-10GHz. To accurately evaluate the device capacitances, both diodes are reverse biased in the "*cold*" operation as reported by K. Lee *et al* [300], in which very small amount of current flows through the junctions and impact of the series resistance, dynamic resistance and transconductance is at minimum level. As a consequence, the small signal equivalent circuit model of the HBT can be approximately represented by only capacitive elements as shown in figure (6.26). According to the physical origin of depletion and diffusion capacitances, the first one is evidently appreciable under reverse bias due to the existence of a wide depletion region; however, in the positive applied voltage, the diffusion capacitance gets higher. This is reflected into the requirement for forward biasing both diode junctions to fully characterize the transistor at high voltage bias where the capacitances are at their maximum values.

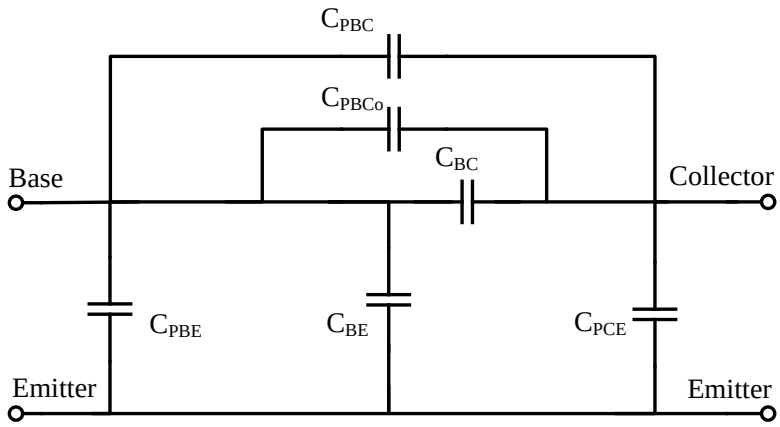


Figure 6.26: Small-signal equivalent circuit model for HBT biased in the "cold" mode operation.

Base-Emitter Junction Capacitance, C_{BE}: The measured data provides a set of UCSD-AGILENTHBT model parameters, for example C_{je} is the depletion capacitance at zero bias voltage as shown in figure (6.27). This figure also shows the additional extractable variables with a given recommended regions. Note that an inclusive description of the other parameters is presented in Appendix B. The typical extracted C_{BE} was obtained using the equation $imag(Y_{11} + Y_{12}) = \omega(C_{BE} + C_{PBE})$ and the approximated formula is given by:

$$C_{BE} \simeq \frac{imag(Y_{11} + Y_{12})}{\omega} \tag{6.12}$$

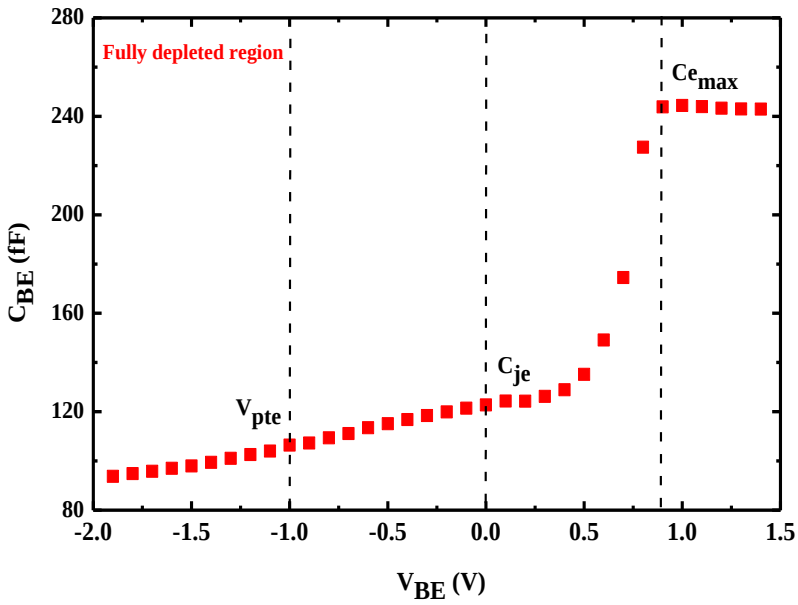


Figure 6.27: Base-emitter junction capacitance, showing the extractable parameters for UCSD model used in this work.

Base-Collector Junction Capacitance, C_{BC}: In a similar trend (see figure (6.28)), the set of extractable parameters that can be obtained from the measured C_{BC} are C_{jc}, A_{bcx}, Cc_{max}, V_{ptc} and M_{jcr}. The following equations describe C_{BC} relation: $imag(-Y_{12}) = \omega(C_{BC} + C_{PBC} + C_{PBCo})$.

$$C_{BC} \simeq \frac{imag(-Y_{12})}{\omega} \tag{6.13}$$

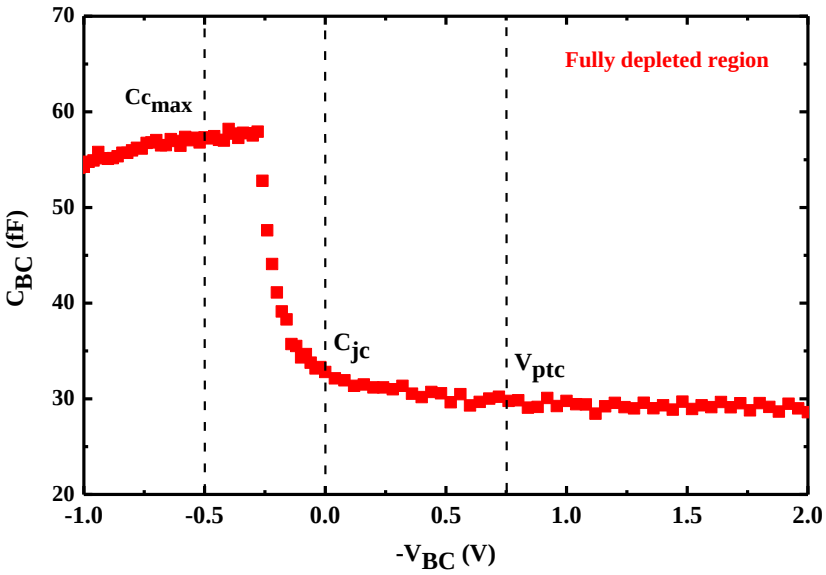


Figure 6.28: The measured base-collector junction capacitance under a range of biasing voltages.

6.8.4 Evaluation of HBT Transit Times

For UCSD-AGILENTHBT, there are a number of transit time parameters that are often used in the model. However, the most commonly involved ones are the p-type base transit time, τ_B and the delay time across the collector layer, τ_C. As given in equation (5.28), $\tau_B = W_B^2/2D_n$. HBT sample F17D2102A has a 65nm base thickness as tabulated in Table (6.1), corresponding to ~2250 cm^2/Vsec minority carriers mobility (i.e. electrons) experimentally evaluated for a heavily doped p-type base region with a concentration of 2.5×10^{19} cm^{-3}[302]. As a result, the base transit time was computed to be 370fsec and used as an initial estimation in the model, which represents the variable T_{FB}. The collector delay time can be roughly calculated by $\tau_C = C_{BC}((kT/qI_E) + R_E + R_C)$. The estimated collector delay time was used as a starting point for TC_{min} parameter to get the measured S-parameters to fit with the simulated ones.

6.8.5 Extraction and Analysis of f_T and f_{max}

Whilst maximizing f_T is predominantly controlled by optimizing the vertical device structure, f_{max} is critically dependent on both lateral HBTs process and base-collector layer design. For a high f_{max} transistor, the key-driver in the fabrication process is to minimise the base resistance and base-collector capacitance. Several interesting ways were proposed to boost f_{max}, such as hexagonal emitter formation for less under-cut profiles[303] and an emitter overhang technique to separate the base-emitter contacts[15]. However, these approaches are methods to improve the poor yield of the self-aligned process for small feature HBT sizes.

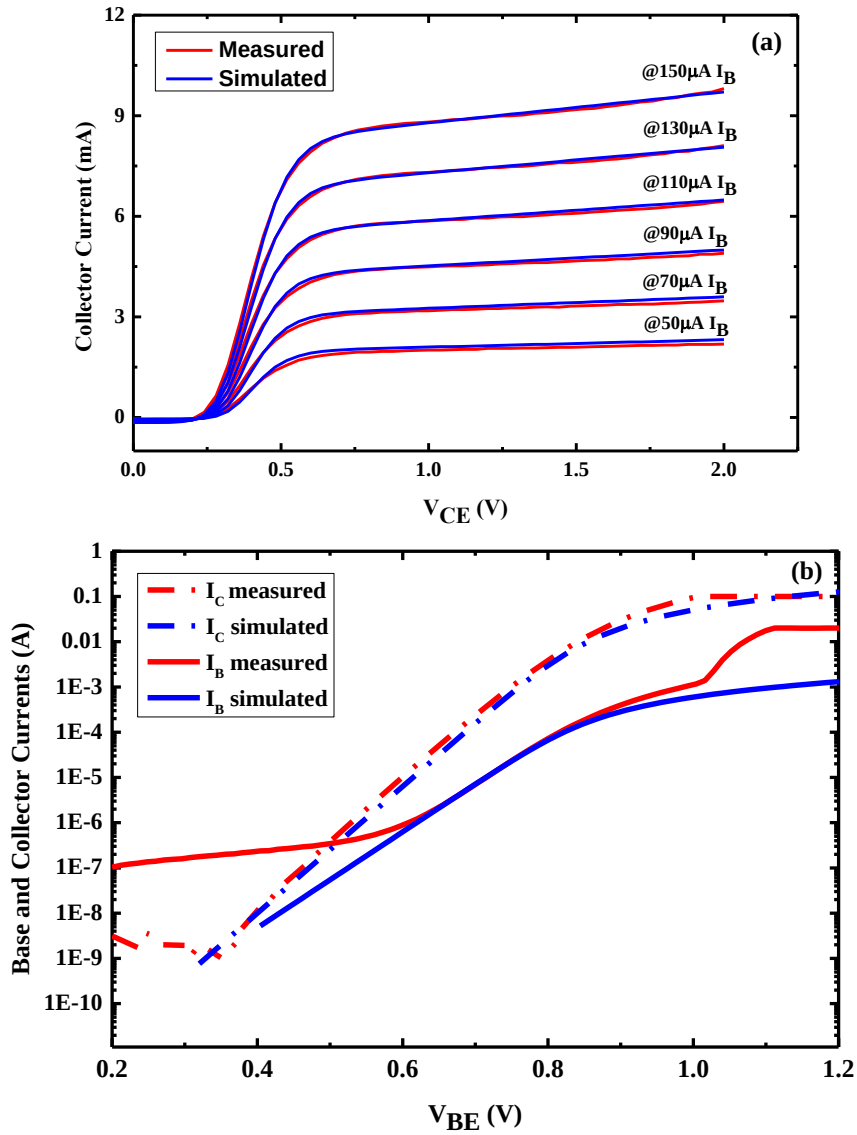


Figure 6.29: Measured and simulated characteristics of the common emitter InP/InGaAs HBT with a 10×10μm^2 mesa size, (a) output I-V characteristic with various I_B values, (b) Base and collector forward Gummel plots.

In this work, a standard non-self-aligned technique was used for large emitter devices. This methodology does simplify the process in terms of depositing the contacts and interconnecting metals in a single step, offering a low cost and less time-consuming process. After the parameter extraction procedure for the UCSD-AGILENTHBT model was accomplished, an optimization/tuning step was carried out to obtain good agreement between the simulated and measured results. This was successfully achieved for DC characteristics, like common emitter $I_C - V_{CE}$ curve and Gummel plots as shown in figure (6.29). The HBT used had a DC current gain, β of about 65 at a bias condition V_{CE}=2V and I_C=10mA and a breakdown voltage of 4.5V. The unified UCSD model for the fabricated InP/InGaAs transistor was then verified for both DC and microwave characteristics with various voltage biases. Furthermore, the measured S-parameter data matched well with the simulated ones as shown in figure (6.30).

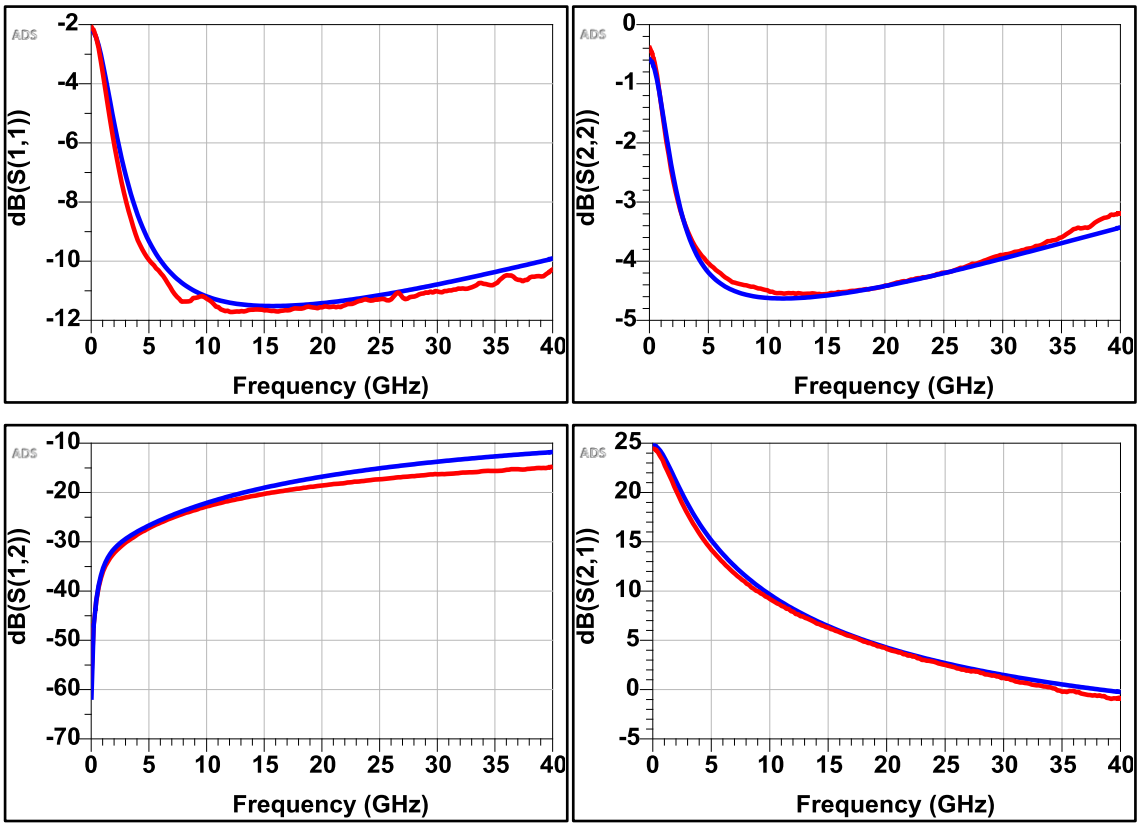


Figure 6.30: S-parameter responses in log-scale magnitude of the InP/InGaAs HBT with a 10×10μm^2 mesa size, red and blue lines refer to the measured and simulated results respectively.

Due to the specific design of the InP-InGaAs epilayer structures and considering the trade-off between high performance PIN and the heterostructure transistor, a 10×10μm^2 emitter mesa size HBT demonstrated an f_T and f_{max} of 54 and 57GHz respectively as

can be seen in figure (6.31). Moreover, Mason's unilateral gain (U) of ~60GHz was obtained with moderate C_{be} and C_{bc} values of 50 and 27fF respectively. These parameters are ample for low cost integrated optical receivers up to 20Gb/s. Further minimizing the HBT mesa area to 4×4μm^2 can effectively lead to over 100 GHz cut-off frequencies. To avoid short-circuiting the base-emitter electrodes, the spacing contact between these was optimized to be 1.5μm. This is to achieve a high yield process whist not significantly degrading the unilateral power gain of the HBTs.

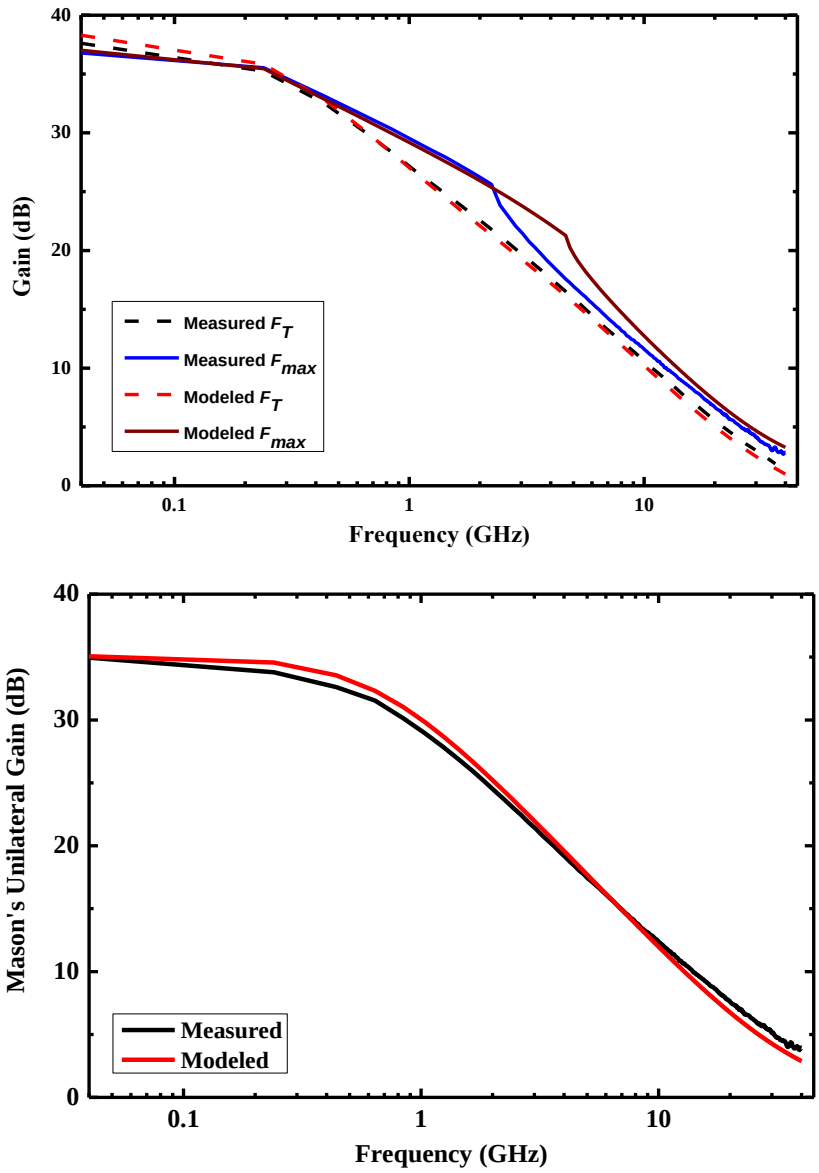


Figure 6.31: Measured and simulated characteristics of the common emitter InP/InGaAs HBT with a 10×10μm^2 mesa size at V_{CE}=2V and I_C=10mA where f_T and f_{max} (top) and Mason's unilateral gain, U (bottom).

The common emitter characteristic and figures of merit f_T and f_{max} for the modeled and measured results show good agreement as depicted in figure (6.31). This validates the accuracy of the parametrical extraction procedure used and can thus be extended further towards aiding in the prediction of integrated circuit performance. Table (6.3) shows a performance comparison between the designed and measured parameters of the presented HBT and previously reported devices. The implied unity gain cut-off frequency and the maximum frequency of oscillation of the fabricated 10×10μm^2 InP/InGaAs HBT device are higher than that demonstrated in[304] and comparable with published work[273, 305] despite its large emitter size. It is believed that this comes from the well-designed HBT structure which, for example, prudently balances C_{bc} and carrier transit time through the base-collector depletion region. The data tabulated also gives an overview on comparable f_T and f_{max} achieved for smaller HBT sizes. Of course, micrometre-scale feature size devices exhibit higher cut-off frequencies because of their much-reduced capacitances which provide ultra-fast switching speed well into frequencies exceeding 100GHz.

TABLE 6.3: PERFORMANCE COMPARISON OF THIS WORK'S HBT AND RECENTLY PUBLISHED WORKS.

REF.	TECHNOLOGY	EMITTER SIZE (μm^2)	PROCESS	f_T/f_{max} (GHz)
[15]	InP/InGaAs	1×5	emitter-overhang self-aligned	130/220
[273]	InP/InGaAs	4×12	self-aligned	80/40
[305]	InP/InGaAs	3×8	self-aligned	70/40
[272]	InAlAs/InGaAs	5×5	self-aligned	67/123
[306]	InP/InGaAs	1.6×10	T-shape emitter self-aligned	150/220
[304]	InP/InGaAs	3×8	self-aligned	46/42
THIS WORK	**InP/InGaAs**	**10×10**	**Standard process**	**54/57**

6.9 Optical Transceiver System

A fibre optic communication system is generally constructed from three basic components: an optical transmitter for the light source, an optical fibre acting as a transmission line and an optical receiver. To send a message signal to a certain distance, it is required that the coherent light source to be modulated/encoded using a pseudo-random bit stream (PRBS) in place of data stream, which will be then coupled into the fibre optic. As such the system is, of course, digital, the encoded optical signal travels along the transmission line in a digital pulse form, offering reliable and efficient delivery for high data rate communication. This is due mainly to the very low dispersion and attenuation of the fibre optic[307]. At the receiving end, a PIN or an APD photodiode converts the variation in the optical signal into corresponding electrical current flowing through the subsequent low noise preamplifier circuit. The resulting digital voltage form is eventually passed on to a decision circuit implemented using a clock data recovery circuit, providing a synchronized signal within a standard digital format.

Since 1.55µm wavelength exhibits a minimum attenuation for light, it is considered a favoured choice particularly with erbium-doped fibre amplifier (EDFA) technology, of which the gain spectrum is within 1.525-1.57µm[79]. A deleterious factor that might affect the optical system performance in high-speed operation is the dispersion limit defined as the broadening of the digital pulses in the time domain, contributing to a distortion in the transmitted signal because of the receipt overlapped pulses at the receiver. This undesirable outcomes is called inter-symbol-interference (ISI) issue[308]. For single mode fibre (SMF) operating at 1.55µm, the overall chromatic dispersion is approximately 17 ps/nm/km. To minimize the impact of the inherent dispersion issue, optical compensation techniques are often implemented in the optical link[308].

6.10 Overview of Recent Photoreceiver Integration Techniques

As an optical architecture standard, 2.5Gb/s GPON and the next generation 10Gb/s EPON, OEICs are undisputedly the key-components in fibre optic communication systems including the front-end transimpedance amplifiers (TIAs) and PIN/avalanche photodiodes. Since their electrical/optical bandwidth and conversion gain dominate the entire characteristics of the receivers[15], improving these crucial parameters are paramount in enhancing the high data rate capability of the optical systems. For

photoreceiver circuit implementations, HEMTs and HBTs transistors have been extensively investigated by integrating PIN/avalanche photodiodes with TIAs[12, 14-16]. The requirement for extremely small HEMT gate length (typically < 0.1µm) to achieve over 100GHz cut-off frequencies[309, 310] in comparison with the fairly relaxed emitter area of HBTs makes the heterojunction transistors arguable more attractive for low cost and high volume manufacturing as they require much less stringent lithography. There are mainly two approaches in integrations of OEICs: monolithic and hybrid forms. The first scheme offers the ability to exploit the base-collector heterojunction layers for the formation of the photodiodes, contributing to a simple epitaxial growth process and so circumventing both regrowth and complex fabrication sequence along with packaging simplification[273, 311].

The downside of a shared layer between two different devices is that a trade-off between the collector depletion region of HBTs and carrier transit time of photodiodes needs to be effectively balanced. The benefit from the hybrid integration scheme is to independently optimize the epitaxial layers of the photodiodes and HBTs thereby accomplishing an optimum performance for each device individually[312]. However, this approach has disadvantages including increase in epitaxial growth complexity, large IC sizes and inevitable extra parasitic elements due to bond wire connections[14, 305]. For these reasons, monolithically integrated circuits are preferred over hybrid ones for ultrahigh speed photoreceivers.

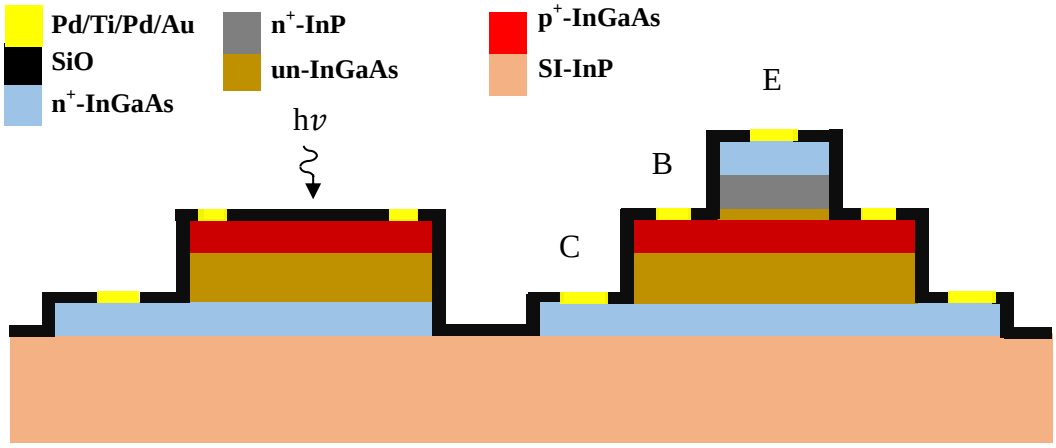


Figure 6.32: Schematic cross section of the monolithic IC used in this work showing a PIN-PD and HBT on left and right sides respectively, both of which are sitting on a semi-insulating InP substrate. Note: the drawing is not to scale.

Among three terminal heterojunction devices, InP/InGaAs based OEICs have been widely studied for beyond 10Gb/s data rates at 1.55µm wavelength operation[272, 273, 310]. In general, GaAs-based photoreceivers are used for short wavelength (0.8-0.9µm), while InP-based devices are for wavelengths ranging from 1.3 to 1.6µm[78]. This work is concerned with design, characterization and modelling of high speed InP/InGaAs PIN-SHBT based OEIC photoreceivers. Figure (6.32) shows a simplified schematic of the PIN with a window size monolithically integrated with the HBT transistor used in this work. More importantly, full-scale characterizations of the receivers using CAD tools prior to fabricating the circuits are invaluable in the prediction of prospective performances and to aid in further optimisation. In-depth discussion and analysis for the OEIC model is presented in the following sections.

6.11 Transimpedance Amplifier Topology

For long-haul fiber optics, the use of preamplifiers is paramount in improving the photoreceiver sensitivity. This becomes more pronounced with the integrated unity internal gain PIN-PD because it is rather difficult for the decision circuits to efficiently reshape the received signal. Note that the sensitivity of the photodetectors is defined as the average of optical power required to ensure a bit-error-rate (BER) of 10^{-9} at a given data communication rate. Beside the requirement for high sensitivity characteristic, some other figures of merit are also important including large bandwidth, flat gain response and wide dynamic range. There are two basic topologies used to realize the front-end amplifiers; the high impedance (HZ) and transimpedance (TIA) configurations. The first design is implemented with a large biasing resistor, in other words, the input admittance of the amplifier is governed by its overall input capacitance, which tends to further minimize the circuit noise[78]. This; however, involves integrating a large biasing resistor value exceeding a few kilo Ohms, increasing the chip dimensions.

On the other hand, the extensively reported research into TIA amplifiers feedback resistor, R_f and integrated with a photodiode in OEICs comes from their benefits including wide bandwidth and dynamic range in comparison with the HZ topology. Of practical interest is that a well-designed TIA is able to match the noise performance of the HZ amplifier[78]. It is of vital importance pointing out that the feedback resistor value is the key factor in determining the photoreceiver performance. Large R_f can

efficiently boost the TIA gain and sensitivity; however, this will degrade the frequency bandwidth and result in a reduction to the high bit rate capacity, requiring a reasonable feedback resistor value for proper circuit operation. The effective transimpedance gain of the TIA without photodiode is calculated from the S-parameter data[313].

$$Z_{eff} = 20\,log\left(|Z_o|\frac{|S_{21}|}{|1 - S_{11}|}\right) \tag{6.14}$$

Where Z_o is the 50Ω characteristic impedance of the standard measurement set-up and S_{21} and S_{11} are the S-parameters response of the front-end amplifier.

6.11.1 TIA Input and Output Stages

The purpose of this section is to describe in detail the design of the front-end amplifier stage by stage, concentrating on theoretical analysis and circuit design aspects. Irrespective of the integration technique and HBT or HEMT based transimpedance amplifiers, there are various ways used for circuit implementation in terms of input/output configurations and number of amplification stages. The holistic TIA circuits are fundamentally split into two stages; the input stage, in which the electrical signal is amplified, while a unity voltage gain emitter follower is normally employed in the second stage. As high TIA gain is required to improve the overall sensitivity of the photoreceiver, more than one transistor can be integrated. However, this increases the circuit complexity and consequently degrades the high-frequency performance due to the multiple device capacitances. Since every single HBT introduces two poles in the transfer function excluding the impact of the parasitic components, several integrated HBTs will exacerbate the roll-off curve of the frequency bandwidth.

The emitter follower stage is responsible for two major contributions: firstly, it acts as a buffer stage, enabling a 50Ω output impedance, Z_{out} at the output port. Secondly, the use of this configuration is also to prevent the DC biasing voltage from appearing at the output port, which shifts the level of the desired output signal (this the level shifting stage). This can be alternatively achieved with assistance from an additional integrated resistance to balance the circuit operation. In the literature, base-emitter diodes were demonstrated in emitter follower buffers instead of the use of relatively bulky

resistors[309]. In practice, level shifting diodes are simply implemented by shorting the base and collector contacts, which creates a PN junction device. The TIA module realized here uses the InP/InGaAs HBT large signal model with 10×10μm^2 emitter size which were fully characterized in earlier chapters. Beside this, all the possible parasitics associated with the prime active/passive elements were carefully considered, further reducing simulation errors and providing a model result that agreed well with the actual measured data. Figure (6.33) shows the transimpedance amplifier configuration utilized in this work designed with three transistors and a feedback resistor.

The common-emitter transistor, Q_1 represents a gain stage, while Q_2 and Q_3 are implemented as two emitter-follower buffer stages. Furthermore, R_f provides a shunt-shunt feedback to the base of Q_3 and it is necessary to optimize its values for the overall gain and bandwidth of the photoreceiver. These key parameters are also affected by the biasing and mesa size of Q_1.

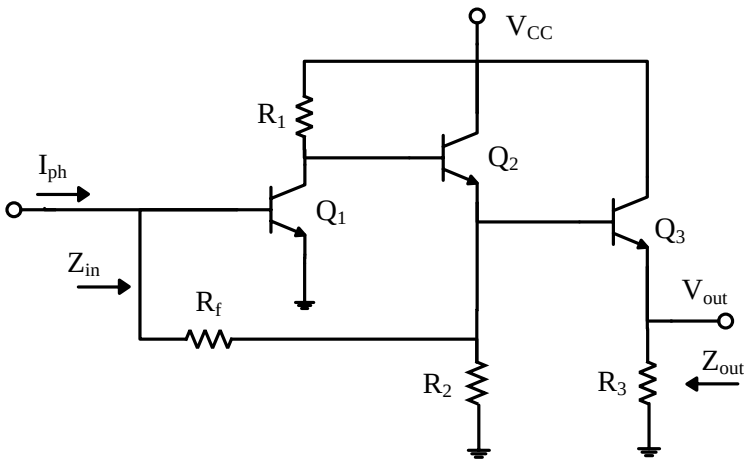


Figure 6.33: Circuit diagram of the transimpedance front-end amplifier used in this work, showing only the prime components.

A PIN-PD introduces two poles to the front-end amplifier; the first pole emerges from the depletion capacitance while the second one is due fundamentally to the carrier transit time effect. The challenge in designing a wide bandwidth OEIC is the presence of a relatively large capacitance of the PIN diodes, in most cases exceeding 150fF, loaded on the TIA's input impedance. Therefore, a common base input stage configuration with a very low input impedance was reported to address this issue[314]; however, in such a scenario, additional transistors are required to boost the circuit's gain. For a less complex

design, the shunt feedback topology at the base node of Q_1 was used to further lower the input impedance of the amplifier. The direct consequence is to push the dominant pole caused by PIN-PD into high frequencies, offering an efficient high-speed capability. The first emitter follower transistor, Q_2 has a fundamental role in achieving a good flatness gain-frequency response, thanks to its high input impedance characteristic. Of note, this simply helps to isolate the parallel-feedback loop from the input capacitance of the output buffer, helping to eliminate the Miller capacitance loading to the previous stages. The resulting advantage further mitigates the influence of the physical based capacitance on the frequency bandwidth. In mid-band gain operation, the impact of the parasitic components is negligibly small and the inductance and capacitance of the prime elements are assumed to be short circuits with very low series resistance. This does not only help to simplify the cumbersome derivation of the transfer function but it also gives a prediction of the available gain of the circuit prior to the module results. Figure (6.34) depicts the small signal equivalent circuit of the TIA diagram used in this work, involving the shunt-shunt feedback topology which allows converting the detected photocurrent into corresponding electrical voltage signal.

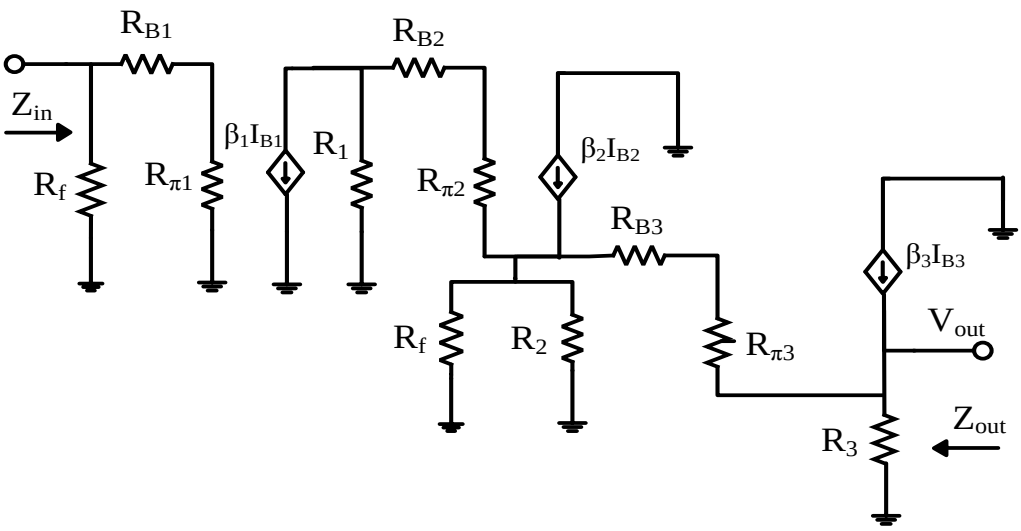


Figure 6.34: Mid-band small signal equivalent circuit of the front-end amplifier used in this work, obtained by the well-known π hybrid model.

$R_{B1} = R_{B2} = R_{B3} = R_B$ is the base resistance of a given transistor while $R_\pi = \beta r_e$ and the emitter and collector resistances were ignored throughout the analysis due to their low respective values. The input impedance, Z_{in} and output impedance, Z_{out} were firstly derived, taking advantage of the shunt-shunt feedback topology (i.e. voltage-shunt

feedback) in the circuit shown in figure (6.34). Note that both impedances decrease by the factor $(1 + R_M\beta_f)$ where R_M and β_f are the feedback-independent transimpedance gain and feedback factor respectively. According to the given circuit, $\beta_f = (-1/R_f)$ as well as Z_{in} and Z_{out} can be expressed as:

$$Z_{in} = \frac{R_f \| (R_{B1} + R_{\pi 1})}{1 + R_M\beta_f} \tag{6.15}$$

$$Z_{out} = \frac{\left(\frac{\left[\left(\frac{(R_1 + R_{B2} + R_{\pi 2})}{1 + \beta_2} \| (R_f \| R_2) \right) + R_{B3} + R_{\pi 3} \right]}{1 + \beta_3} \right) \| R_3}{\left(1 + R_M\beta_f\right)} \tag{6.16}$$

In a lossless transmission line system, the relation of the voltage gain (S_{21}) can be formulated by the mid-band gain, A_m when satisfying two major conditions: the output port must be matched with circuit and the source impedance is 50Ω[315]. To this end, the relation of S_{21} and return loss, S_{11} are given by:

$$S_{21} = 20log(2A_m) = 20\,log\left(\frac{\left(\frac{2R_M}{1 + R_M\beta_f} \right)}{Z_o} \right) \tag{6.17}$$

$$S_{11} = 10\,log\left(\frac{Z_{in} - Z_o}{Z_{in} + Z_o} \right) \tag{6.18}$$

The DC current gain, β of the transistors was obtained from the model in accordance to the simulated base and collector currents, whereas other predefined parameters used in the simulation are tabulated in Table (6.4).

TABLE 6.4:: MODEL PARAMETERS OF THE TRANSIMPEDANCE AMPLIFIER USED IN THIS WORK.

PARAMETER	V_{CC} (V)	R_f (Ω)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
VALUE	3.3	100	500	250	350

To maximize the bandwidth and gain, the transistor Q_1 was biased at its peak f_T cut-off frequency and so the modeled front-end amplifier showed a transimpedance gain of

~36dBΩ with an electrical bandwidth of 10GHz as depicted in figure (6.35). The figure also exhibits the return loss with a response of less than -10dB over a wide range of frequencies (up to 20GHz), emphasizing that the amplifier is well-matched with a 50Ω source impedance. Moreover, the electrical bandwidth result is evidently suitable for an optical system operating with a bit rate up to 15Gb/s. The circuit performance can be improved by optimizing the model parameters, broadening the bandwidth without significantly sacrificing other figure of merits.

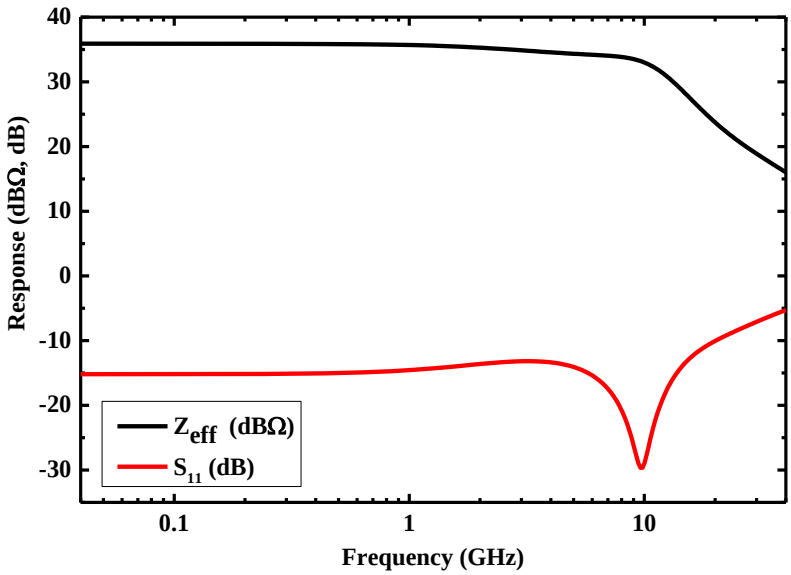


Figure 6.35: Simulation result of front-end amplifier, showing the transimpedance gain, Z_{eff} and return loss responses as a function of operating frequency using 10×10μm^2 InP/InGaAs HBTs.

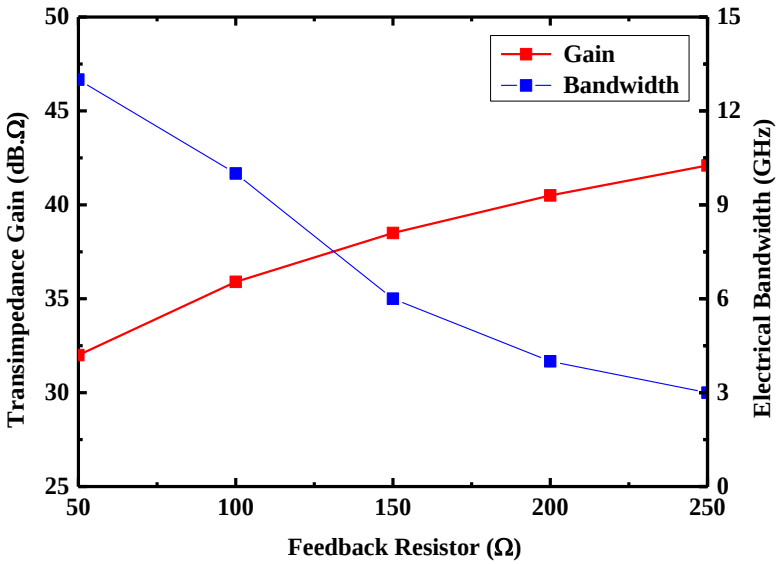


Figure 6.36: The variation effect of feedback resistor on the transimpedance gain and electrical bandwidth of front-end amplifier, an InP/InGaAs HBTs with a 10×10μm^2 mesa was used in the simulation. All other parameters were kept constant throughout the simulation run.

The DC power dissipation in the whole circuit including the resistors and transistors is approximately 22.6mW. The direct dependency of the transimpedance gain and bandwidth on the feedback parameters was investigated; unsurprisingly high gain and narrow bandwidth are observed with a large feedback resistor values as shown in figure (6.36). A 32dBΩ with a bandwidth of 14GHz was achieved at an R_f value of 50Ω. These outstanding results offer an opportunity to integrate a relatively large size and low-cost manufactured HBT, with the aim to be used in EPON optical communication systems. Other than manipulating the feedback parameters, the use of a small transistor feature size with a high cut-off frequency can effectively enhance the high-speed capability. This allows incorporating many HBT devices in the amplification stage with no severe impact on the frequency response since their respective junction capacitances would not exceed a few femto-Farads. However, this is constrained by two substantial factors: the available photolithography technique and low-yield process of micrometer-scale devices. It is of importance to mention that in real-world applications, there is no requirement for 50Ω input impedance in hybrid/monolithic integration scheme as the input impedance of the incorporated photodiode is mesa size and epilayer structure dependent at fully depleted condition.

6.11.2 Group Delay

To prudently assess the quality of a distributed amplifier characteristic, an additional parameter called the group delay, τ_g is required in particular for ultra-high speed operations. It is basically a measure of the linearity of the phase distortion as a function of frequency or in other words defined as the actual transit time of an electrical signal through the whole IC from the input to output port. In practice, variation in group delay should be equal of less than a quarter of a single bit duration time, ensuring that the phase distortion is maintained at an acceptable level[316] (i.e. the eye of the eye diagram is at least half open as will be discussed later in this chapter). The group delay is calculated from the phase of the gain transfer function as given by:

$$\tau_g = \left(\frac{-1}{360^\circ}\right)\left(\frac{d\theta}{df}\right) \tag{6.19}$$

Where θ is the phase of the S_{21} of the TIA amplifier, which is strongly affected by the capacitance and inductance of the transistors themselves and surrounding bond-pads.

This gives an insight on how important it is to minimize the parasitic sources associated with unnecessary wide and long wiring connections. Figure (6.37) shows the group delay simulation result of the TIA circuit with different feedback resistor values. The modeling results demonstrated that the amplifier has a group delay variation of 12psec up to 10GHz bandwidth at 100Ω R_f and expectedly the deviation in τ_g reduces when the feedback resistance gets lower.

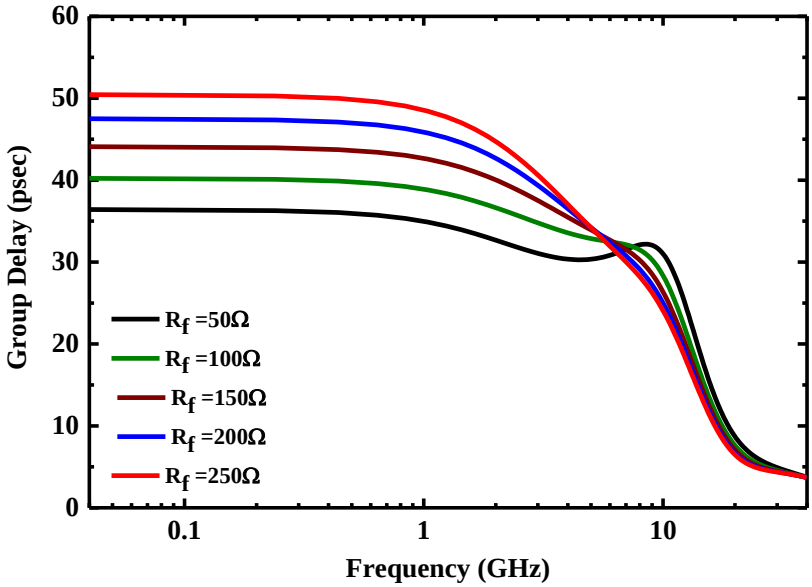


Figure 6.37: Simulated group delay of the transimpedance amplifier with various values of the feedback resistor while keeping other parameters constant in the model. An InP/InGaAs HBTs with a 10×10μm^2 mesa sizes was used in the simulation.

The reason is distinctly attributed to a reduction in the nonlinear distortion by the factor $(1/(1+R_M\beta_f))$ where $\beta_f = 1/R_f$, resulting in a 5.4psec group delay variation at 50Ω R_f. However, this is at the expense of a decrease in the overall transimpedance gain thereby moderate feedback parameters must be chosen. A wideband front-end amplifier with a more than 25% deviation in τ_g produces jitter in the eye, which tends to increase the signal reshaping difficulties at the decision circuits. This issue is more severe at high optical power of >5dBm, in which the photoreceivers often encounter a high voltage swing hence the circuit might not operate linearly. Relevant discussion and analysis are presented in the following sections mainly focusing on how this inherent problem can be alleviated.

6.11.3 Bandwidth Enhancement Techniques

Traditionally, the demand for a high bit rate data communication can be satisfied by using either small HBT feature sizes ($1\times5\mu m^2$) or sub-micrometer scale gate length HEMT devices of <30nm. In fact, the costly lithography techniques required is the major impediment facing the fabrication process of low-cost consumer market high-speed optoelectronic circuits. Therefore, passive peaking techniques were demonstrated as an alternative approach to enhance the electrical bandwidth of the amplifiers, further pushing the performance limits of solid state devices[317]. An appealing characteristic of this method is that the improvement in high-frequency response comes with no additional power being dissipated in the circuit[78]. To this end, a number of peaking techniques have been reported and the most common ones are the use of capacitive and inductive elements[317-319]. As stated in the previous section, the emitter-base diodes are used as a level shifting component in the photoreceivers; however, their respective series resistances degrade the bandwidth performance of the TIAs. A parallel connected peaking capacitance is thus indispensable for extending the -3dB bandwidth, which can be improved by factor of two without considerable degradation in the transimpedance gain or/and its flatness as well as noise characteristics of the amplifier[78]. In fact, this is largely due to a dominant pole created by the inserted capacitance and which is located at high-frequency relying on the emitter-base diode's characteristic and optimum value of the capacitor.

In this work, a supplementary series inductive peaking technique was used to broaden the -3dB bandwidth response of the circuit as shown in figure (6.38). Since the reactive inductance is a frequency-dependent parameter, a peak resonance is inevitably introduced at a certain frequency when the effects of the prime capacitive components and inductive peaking cancel each other.

From the small-signal equivalent circuit of the photoreceivers, the derived L_{sp} is approximately given by [320]:

$$L_{sp} = \frac{C_j(R_s + Z_{in})^2}{2} \tag{6.20}$$

Here C_j and R_s are the depletion capacitance and series resistance of the PIN-PD. Owing to equation (6.20), a small inductor, L_{sp} can be obtained by reducing the intrinsic

capacitance of the photodiode. To do so, small PIN-PD mesa sizes or/and mushroom-like structures are necessary; otherwise, the amplifier's input impedance must be decreased. This does not solely minimize the noise performance of the circuit but it allows further extension in the -3dB bandwidth and a reduction in the overall chip size. In this research, the resulting model involves all the associated parasitics of the passive elements, which were broadly investigated in chapter three and not shown in the schematic circuit, figure (6.38). The prime components used in the simulation were optimized for high-speed performance and listed in Table (6.5).

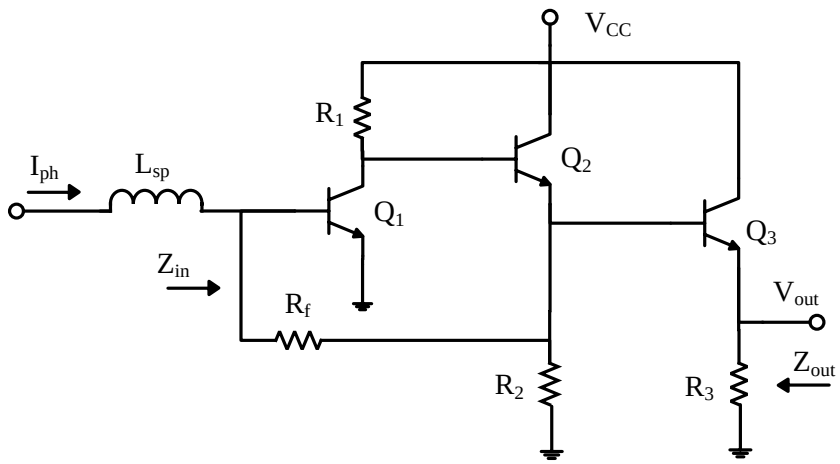


Figure 6.38: A schematic circuit of the modeled transimpedance amplifier with an integrated peaking inductor, showing only the prime elements.

TABLE 6.5: MODEL PARAMETERS OF THE TIA WITH AN INTEGRATED PEAKING INDUCTOR USED IN THIS WORK.

PARAMETER	V_{CC} (V)	L_{sp} (nH)	R_f (Ω)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
VALUE	3.3	2	180	100	450	500

The amplifier showed a transimpedance gain of 40dBΩ with an electrical bandwidth of 11GHz without L_{sp} and with an overall DC power consumption of 30mW. A moderate integrated peaking inductor of 2nH led to widening in the -3dB bandwidth to 18GHz, which is enhanced by >60% as shown in figure (6.39). The corresponding transimpedance gain product is 1.8THz.Ω and can be further increased with larger inductor values. A 2nH peaking inductor is thus preferred for the design presented here since larger L_{sp} values will result into an increase in the group delay and a deleterious

impact on the overall performance of the photoreceiver. To clarify this, the group delay response with different peaking inductor was simulated as depicted in figure (6.40). Undoubtedly, small variation in τ_g is attainable when L_{sp} gets smaller regardless of the feedback parameters and better results can be achieved by lowering R_f. As a conclusion, the modeling results obviously reveal that the use of single feedback loop with peaking inductor technique has a reasonably decent performance but frankly has transimpedance gain and group delay dependency drawback at least with the relatively large HBT devices employed here.

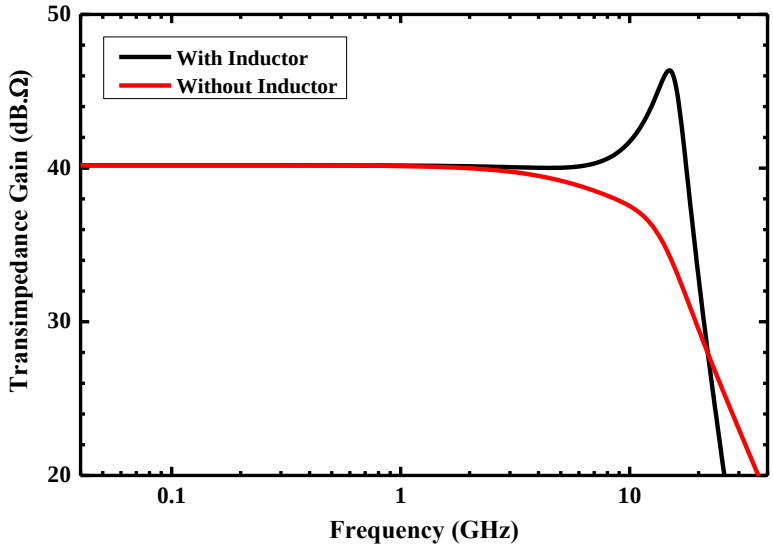


Figure 6.39: Simulation result of transimpedance gain response as a function of operating frequency using 10×10μm^2 InP/InGaAs HBTs with and without peaking inductor.

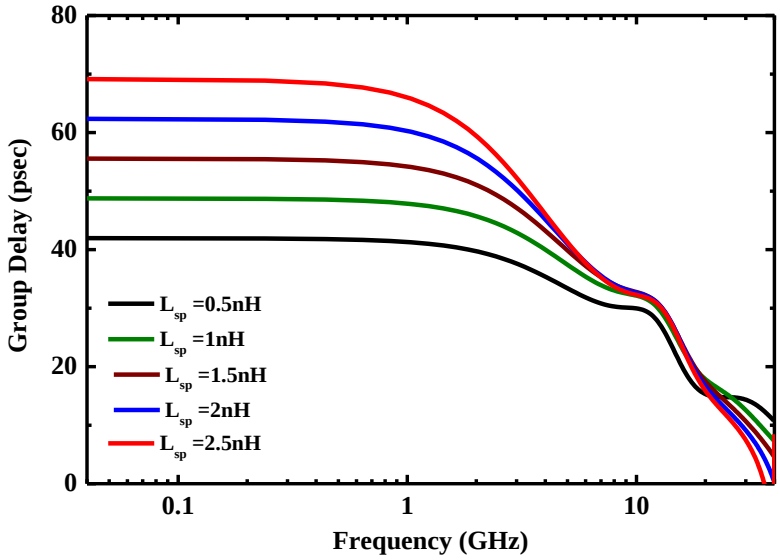


Figure 6.40: Simulated TIA's group delay with different peaking inductor values. An InP/InGaAs HBTs with a 10×10μm^2 mesa sizes was used in the simulation run.

6.11.4 Multiple Feedback Loops TIA

The well-known challenge in designing a wide bandwidth photoreceivers is the relatively high capacitance of the photodiodes loaded on the TIA's input impedance and this can be alleviated by either using a common base configuration in the first stage or/and a single feedback loop. Furthermore, a high gain TIA is a key-driver in the capability of converting the weak photocurrents, providing better sensitivity performance. These imperative requirements are impeded by the limitations of the conventional circuit configurations as they still suffer from a poor overload performance at a high optical power of >0dBm due to the use of a large R_f for high gain and low noise operation[321]. This predominantly occurs in short-haul intercity communication systems, in which an EDFA amplifier is not used. At the optical overloading point, the front-end amplifier starts to saturate, resulting in a narrow dynamic range feature (could be less than 16dB). In fact, the dynamic range figure of merit depends on many factors, for example the transmission distance and sensitivity and transimpedance gain of the photoreceivers. A low reliability and unity amplification characteristic are the direct consequences of a compressed dynamic range. An effective way used to broaden the dynamic range without sacrificing the sensitivity is based on incorporating an automatic gain control (AGC) circuit with a single feedback loop TIA amplifier (SFB-TIA). The basic function of the AGC circuit is to adjust the overall IC gain, which is reduced and boosted at high and low optical power conditions respectively[322]. However, AGCs circuits are DC power hungry and increase the complexity in designing the whole photoreceiver compared with conventional designs. A new circuit configuration was thus proposed involving multiple feedback loop network (MFB), which improves the optical overload performance and achieves a large bandwidth without undesirable effects on the other characteristics[321, 323].

TABLE 6.6: A COMPARISON AMONG DIFFERENT TIA AMPLIFIER TECHNOLOGIES.

TIA TOPOLOGIES	OVERLOAD PERFORMANCE	POWER CONSUMPTION	DESIGN COMPLEXITY
SFB-TIA	Poor	Low (≤30mW)	Simple
MFB-TIA	Good (~2dBm)	High (~100mW)	Simple
AGC-TIA	Superior (≥4dBm)	Very High (>300mW)	Complicated

Table (6.6) shows a comparison study among various TIA technologies that have been recently used in developing optoelectronic integrated circuits capacity. In this research, a MFB-TIA was modeled in an attempt to widen the bandwidth and achieve as minimum a group delay variation as possible since no peaking techniques are required. Figure (6.41) shows the circuit diagram of the MFB-TIA and the corresponding mid-band small signal equivalent circuit. A similar design was reported in recent years but with SiGe BiCMOS technology[321].

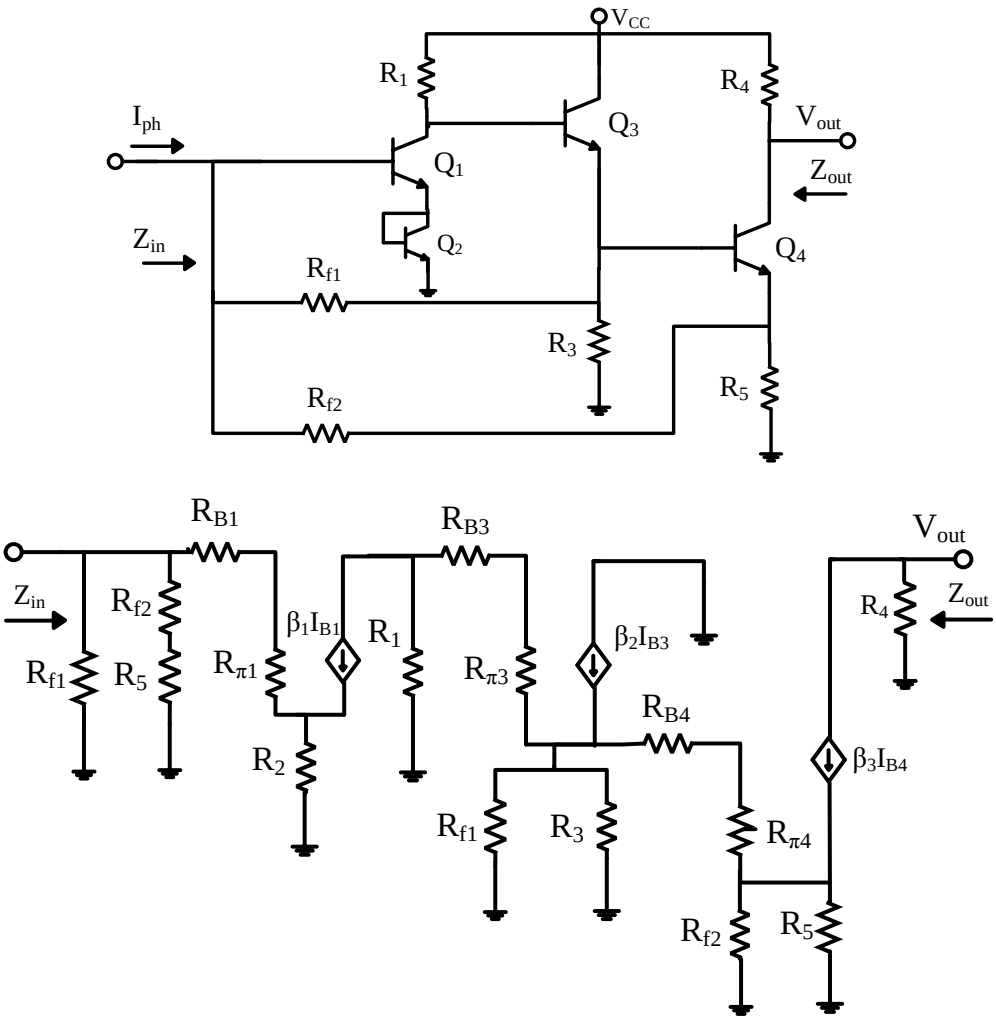


Figure 6.41: Circuit diagram of the multiple feedback loops TIA amplifier alongside its mid-band small signal equivalent circuit used in this work, obtained by the well-known π hybrid model and showing only the prime elements.

The schematic uses shunt-shunt and shunt-series feedbacks through R_{f1} and R_{f2} resistors respectively. The gain stage Q_1 is connected to Q_2 in order to facilitate a convenient level shifting and emitter degeneration characteristic (i.e. improve the circuit linearity and

further reduce the input impedance without a noticeable influence on the overall transimpedance gain). Of course, the size and biasing conditions of the first stage play a pivotal role in determining the noise performance and -3dB bandwidth of the preamplifier. Moreover, a proper R_1 value can help to decrease the group delay response[324]. The use of the wideband buffer transistor, Q_3 is to mitigate the capacitive loading effect at the collector of Q_1 and enhance the optical overloading performance. An appropriate design for the output stage, Q_4 necessitates that a comparable R_4 and R_5 should be chosen, allowing a reasonable voltage drop at the terminals of R_4 and subsequently dividing the received photocurrent between the two feedback resistors. This results in almost identical small signal networks at the base and emitter nodes of Q_4 or in other words, the aggregate transimpedance from input to output ports can be roughly formulated as $R_{f1}\|R_{f2}$[321].

For the sake of simplicity, the level shifting Q_2 was compensated by a resistor R_2 as shown in the small signal equivalent circuit. Note that input impedance decreases by the factor $(R_M\beta_{f1}A_i\beta_{f2})$ where R_M and A_i are the feedback-independent transimpedance gain for the shunt-shunt and shunt-series topologies respectively while β_{f1} and β_{f2} are feedback factors of the aforementioned feedback loops. According to the mid-band equivalent circuit, the derived $\beta_{f1} = (1/R_{f1})$ and $\beta_{f2} = (R_5/(R_5 + R_{f2})$ values and thus Z_{in} can be expressed as:

$$Z_{in} \simeq \frac{R_{f1}\|(R_{f2} + R_5)\|[R_{\pi 1} + (1 + \beta_1)R_2]}{R_M\beta_{f1}A_i\beta_{f2}} \tag{6.21}$$

Equation (6.21) gives a general indication of a rather low Z_{in} offered by a MFB topology compared with the widely used SFB-TIAs, and this is reflected into less capacitive loading effect emerging from a large integrated PIN-PDs. The output impedance is mainly dominated by the shunt-series loop.

$$Z_{out} \simeq R_4\left(1 + A_i\beta_{f2}\right) \tag{6.22}$$

More importantly, evaluating the overload optical current, I_{ov} can be estimated at the point when the transistor Q_1 enters saturation condition[321].

$$I_{ov} = \frac{V_{BE3}}{R_{f1} \| R_{f2}} + \frac{V_{BE4}}{R_{f2}} \tag{6.23}$$

The I_{ov} expression quantifies an additional degree of freedom in designing the MFB-TIA, from which a larger overload current is achievable by choosing $R_{f1} < R_{f2}$ and as long as the term $R_{f1} \| R_{f2}$ is maintained constant. As a result, a low noise and a good gain can be attained with wide range of feedback resistor values before incurring an undesirable impact on the optical overload response. This study found that the model of the multiple feedback loop circuit has an approximately flat transimpedance gain of 45dBΩ (~178Ω) with an electrical bandwidth exceeding 18GHz as shown in figure (6.42). The corresponding transimpedance gain product is 3.2THz.Ω and can be definitely extended with the use of smaller transistor features.

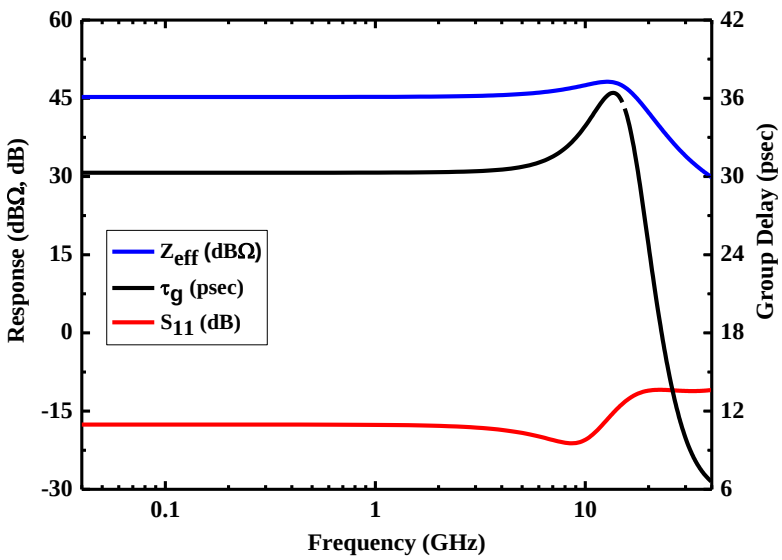


Figure 6.42: Simulation results of MFB-TIA amplifier, showing the transimpedance gain(Z_{eff}), return loss response and group delay as a function of operating frequency. A 10×10μm^2 InP/InGaAs HBTs was exploited in the model.

Furthermore, the return loss response is lower than -10dB while the deviation in the group delay is 11.7psec up to 20GHz. The promising -3dB bandwidth and group delay are satisfactory for supporting an optical system with 20Gb/s and beyond. However, the monolithic integrated PIN-PD will reduce the bandwidth slightly. The circuit consumes an overall DC power of 120mW, of course much higher than that required for SFB-TIAs. The step by step detailed of the single and multiple feedback TIA-modules realized in Keysight-ADS is given in Appendix C.

6.12 Monolithic Optoelectronic Integrated Circuit

In the previous sections, a detailed performance analysis of different TIA circuits was investigated and now it is time to present the practical photoreceiver implementation. By doing this, one of the main contributions of this research is the endeavor to comprehensively study the performance of practical OEIC circuits based an integrated PD-HBTs. This includes exploring both single and multiple feedback loop preamplifiers in terms of high Gb/s capability and other figure of merits. Henceforth, for the sake of convenience, a 20µm window size PIN-PD was utilized in the OEICs due to its low depletion capacitance compared with other large devices, translating into a wide optical bandwidth.

6.12.1 Simulation Results and Discussion

Figure (6.43) shows the circuit design of the OEICs used in this work, including the front-end amplifiers incorporated with the PIN-PD and integrated series peaking inductor (L_{sp}) with SFB-TIA.

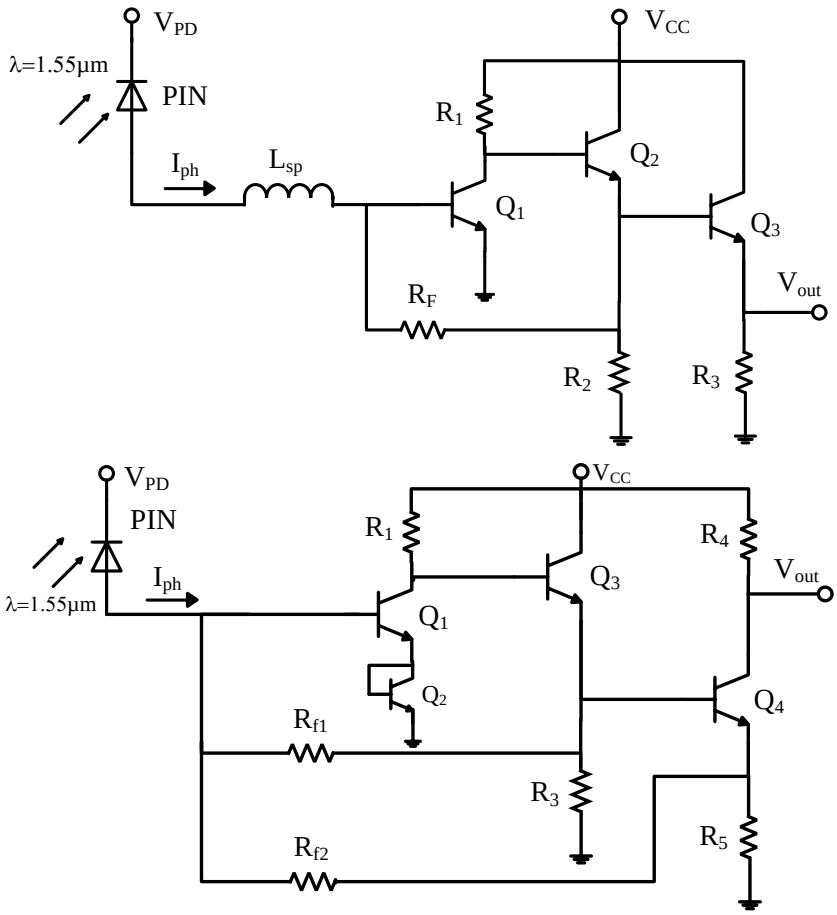


Figure 6.43: A schematic circuit of the modeled photoreceiver of SFB (top) and MFB-TIAs (bottom) showing only prime elements. A 10×10µm^2 InP/InGaAs HBTs was used in the work.

The opto-electrical equivalent circuit model of the PIN-PD discussed in the previous chapter was employed here. It is well-known that the photodiodes are often used in their fully-depleted condition at which the width of the intrinsic layer is almost bias-independent. To this end, the extracted equivalent circuit parameters of the PIN-PD at V_{PD}=5V and with a laser wavelength of 1.55µm have been used. Additionally, the passive elements of the OEICs shown in figure (6.43) were optimized to achieve as high an optical bandwidth as possible. The simulated optimization procedure was performed to be consistent with the high cut-off frequency biasing condition of the integrated circuits especially for the gain stage transistor. The challenge encountered throughout the simulation approach is how to efficiently boost high-speed operation while maintaining a low DC power consumption in the photoreceivers. The realized OEIC circuit was biased at a standard collector voltage of 3.3V; however, the opto-electrical model of the top-illuminated PIN-PD had a 41µA photocurrent (I_{ph}).

The first step was to simulate the SFB photoreceiver with and without supplementary series peaking inductor to establish what enhancement is reflected into the -3dB bandwidth response. The model results demonstrate that the circuit has an opto-electrical bandwidth of 15 and 9GHz with and without an integrated inductor respectively at a power dissipation of about 30mW as shown in figure (6.44). A 2nH peaking inductor led to widening in the -3dB bandwidth by >65%. The obtained bandwidth is theoretically sufficient for up to 20 Gb/s data rate operation.

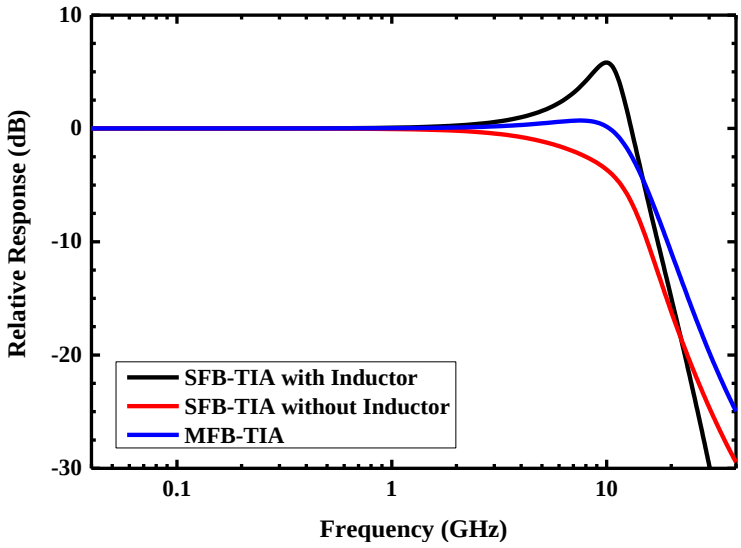


Figure 6.44: Opto-electrical frequency response of the modeled photoreceiver for TIAs with SFB and MFB loops. A peaking inductor was only used with the SFB preamplifier and the whole IC was realized with a 20µm window size PIN-PD and 10×10µm^2 InP/InGaAs HBTs.

In practice, the requirement for a small L_{sp} is simultaneously correlated with achieving a low group delay variation and its feasibility in theory is based on decreasing the intrinsic capacitance of the photodiode or/and input impedance of the TIA. Moreover, the most interesting finding is that a similar optical bandwidth of 14GHz was accomplished employing the alternative MFB circuit as depicted in figure (6.44). This encouraging result evidently proves that 20Gb/s might be obtainable with large 10×10μm^2 InP/InGaAs HBTs irrespective of bandwidth peaking methods. Nevertheless, an experimental validation for the approach is still required to test this methodology in practical applications.

To fully characterize the photoreceiver circuit performance, the conversion gain was evaluated, which is the product of transimpedance gain and responsivity of the photodiode. Predictably, a high conversion gain ranging from 90 to 120V/W was found for multiple feedback loop receiver as a result of the figure of merit (i.e. 45dBΩ Z_{eff}) in comparison with 50-100V/W for the single feedback circuit over a wide band of frequencies as shown in figure (6.45). Such a key-factor is expected to improve by ~20% with the addition of AR coating layer deposited on the PIN's window optical aperture. An increase in the feedback resistor can aid to boost the conversion gain response but at the cost of a detrimental effect on the frequency bandwidth.

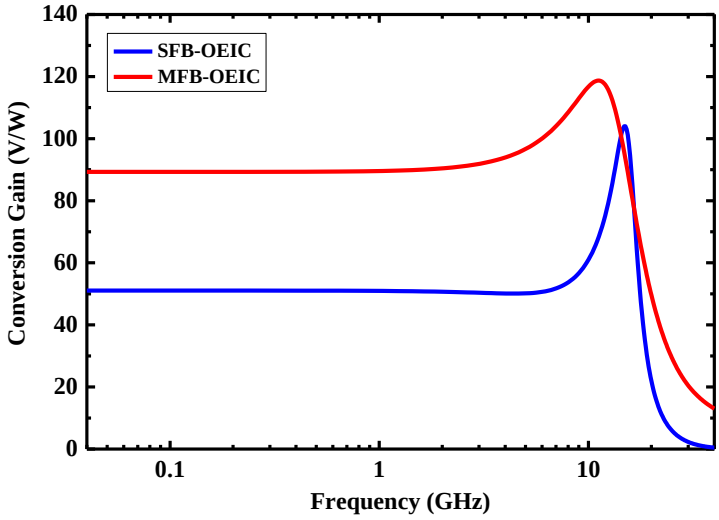


Figure 6.45: Conversion gain performance as a function of frequency for the modeled photoreceiver with SFB and MFB loops. A 2nH peaking inductor was used with the SFB preamplifier module.

To convey a message signal on an optical carrier, it is imperative to modulate the properties of the carrier with respect to the transmitted signal in terms of frequency,

polarization and intensity. The most often used fibre optic systems employ a simple binary modulation method known as On-Off keying (OOK), in which the data is represented by '0's and '1's in accordance to their voltage level and data encoding system used. There are two basic modulation formats of the resulting pulse sequences; return-to-zero (RZ) and non-return-zero (NRZ) schemes. Unlike the NRZ format, RZ requires an approximately double bandwidth as that used by NRZ and this is due to the fact that RZ uses narrow pulse duration time[78]. In Keysight-ADS, either an embedded transit or channel simulator tool can be utilized to simulate the photoreceiver when transmitting a NRZ 2^{15}-1 pseudo-random bit stream (PRBS) pattern applied from a bit stream generator. Because of a limitation in pattern generator capability, a NRZ 2^{15}-1 PRBS pattern was applied instead of the widely exploited 2^{31}-1 ones; however, in practice, no significant difference would be noticeable between these patterns. Figure (6.46) and (6.47) illustrate the eye diagram simulation output with SFB and MFB loops circuits respectively.

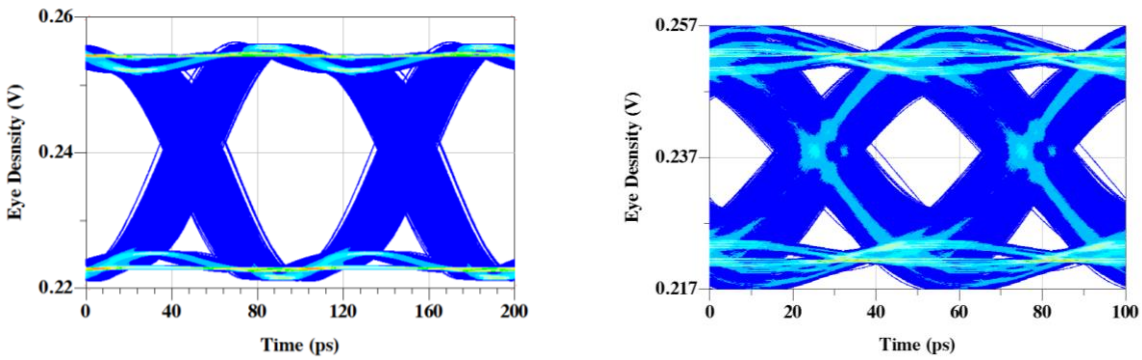


Figure 6.46: Simulated eye diagram of the SFB loop photoreceiver at a bit rate of 10Gb/s (left) and 20Gb/s (right).

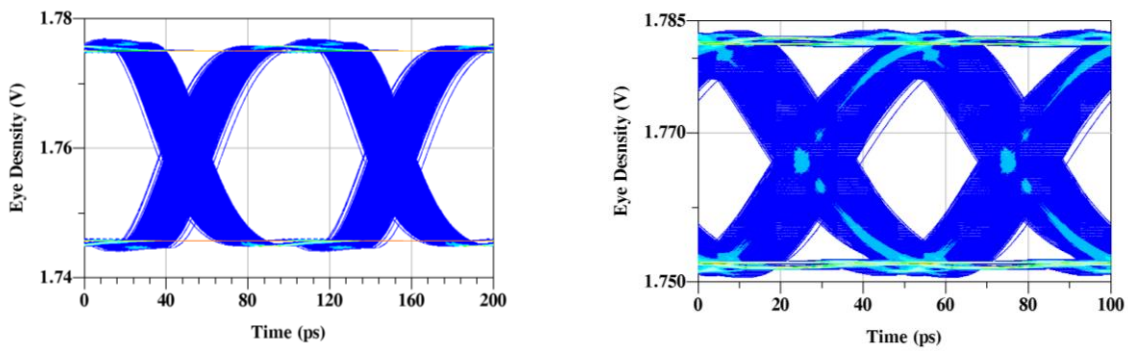


Figure 6.47: Simulated eye diagram of the MFB loop photoreceiver at a bit rate of 10Gb/s (left) and 20Gb/s (right).

Clearly an open eye diagram with no inter-symbol interference (ISI) was observed for 10 and 20 Gb/s operation in both photoreceiver responses. To achieve comparable results to the actual data, the simulation was performed at 10^{-9} bit error rate. The results show negligibly small overshoot or/and undershoot distortion, which is often caused by interruption in the signal path. Additionally, the calculated root mean square jitter of the overlapped bit stream for the single and multiple feedback loops is 4ps at 20Gb/s while producing an open eye width of >29ps. This has been undeniably benefited from good timing synchronization and a rather small jitter effect.

6.12.2 Layout Design

Once the desired results of the module have been demonstrated, the next step was the layout design for the entire integrated circuits, such as TIAs and OEICs. Since high-frequency and low power dissipation operation were the ultimate objective of the project, extra care was needed in designing the layout, which involves the following guidelines:

1. The neighboring passive and active components should be reasonably close to each other.

2. The width of the NiCr resistor is required to be ≥15µm, avoiding self-heating issue of the thin film resistors.

3. It might be important to maintain the thickness of the interconnection metals within ≥1µm, which in-turns reduce their associated inductance and series resistance.

4. All the ground pads must be electrically unified with the width of the crossover interconnecting metals to be as thin as 2-4µm resulting in a decrease in the parasitic capacitance.

5. Various via sizes were designed to enable good contact between the overlapped metal schemes.

An example of the designated layouts for the TIA front-end-amplifier and OEIC with a total die size of 696×690 and 825×690µm^2 respectively are shown in figure (6.48) and (6.49). The input and output ports of both circuits were intended for GSG probing measurements in a 50Ω characteristic impedance and accordingly the dimensions of CPW transmission lines were defined. Other than OEICs, there are a few discrete process control monitoring (PCM) components and structures included in the mask design, for example HBTs, PIN-PDs, various values of NiCr resistors and spiral inductors and many

TLM structures for emitter, base and collector ohmic contacts. The first fabrication run showed that several mask steps in the processing needed to be optimized, such as the isolation process of the HBTs and the integrated PIN-PD must be separately carried out.

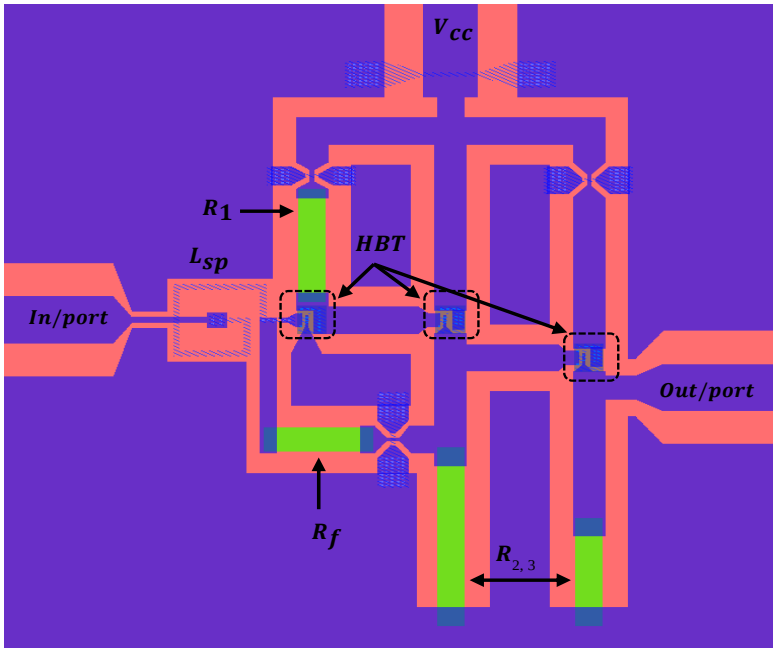


Figure 6.48: Photo-mask of the TIA's layout with SFB loop showing the HBT devices, resistors, spiral peaking inductor and input/output ports.

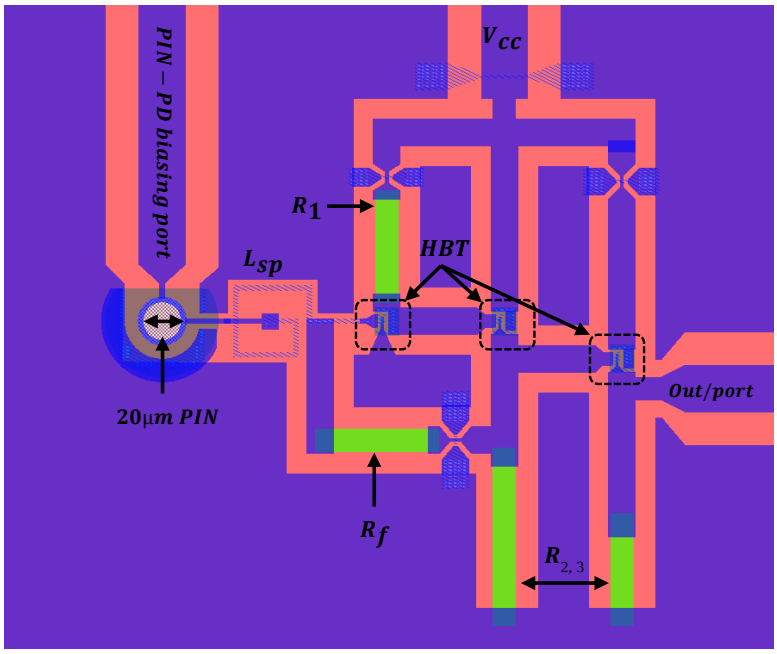


Figure 6.49: Photo-mask of the single feedback loop OEIC's layout including the TIA preamplifier, spiral peaking inductor and 20μm window size PIN-PD.

Of note, a close visual inspection in the first run revealed a flaw in the process which led to deterioration in the predicted results. This was due to the extended isolation etching time. The fact that the isolation process was performed all the way to the InP substrate introduces a high leakage current degrading the characteristics of the photodiode. By the time the photo-mask was optimized and processed towards the end of this research period, unfortunately, the clean room was out of action due to a water flood issue and the fabrication process had to be postponed. A photomicrograph of a fabricated OEIC with single feedback loop topology is shown in figure (6.50).

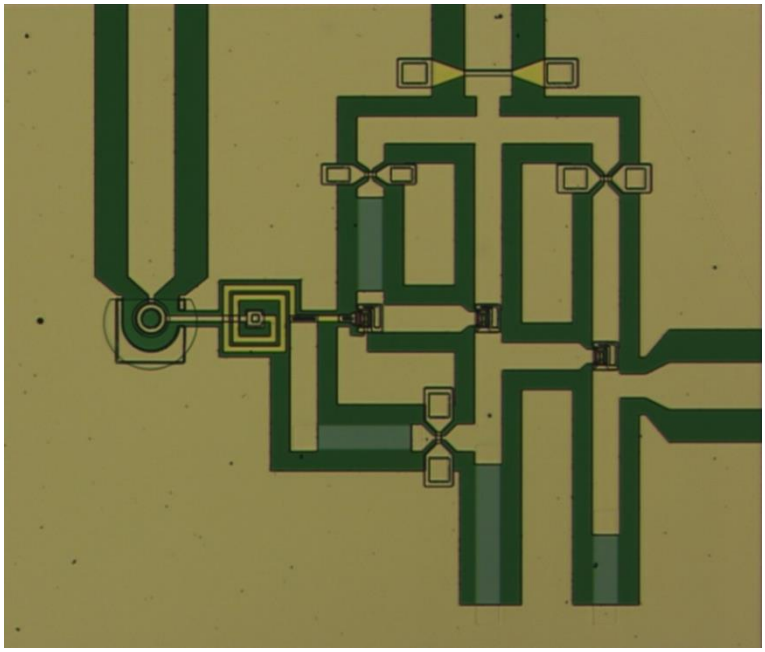


Figure 6.50: Photomicrograph of a fabricated SFB loop OEIC's showing the TIA preamplifier, spiral peaking inductor and 20µm window size PIN-PD.

Even though the objective was to demonstrate a fully integrated photoreceiver, the module and its relevant data discussed in this chapter were based on actual results from fabricated discrete devices (both passive and active). This involves several aspects in relation with the realized module in terms of using fully electrical equivalent circuits for NiCr resistors and 2.5 EM momentum modelling tool to accurately model spiral inductors, in which the coupling impact of the neighboring transmission lines was considered. These latter results provide a good demonstration of what can be expected from the IC design built throughout this project.

6.13 Comparison with State of Art

In contrast to the MBE grown InP/InGaAs HBT studies in this research, there are numerous demonstrations in the literature concentrating on efficient optoelectronic integrated circuits as tabulated in Table (6.7).

TABLE 6.7: STATE OF ART OF RECENTLY REPORTED WORKS OF OPTOELECTRONIC INTEGRATED CIRCUITS OPERATING AT 1.55μm WAVELENGTH.

REPORTED IN	RECEIVER TECHNOLOGY	RECEIVER TOPOLOGY	BANDWIDTH (GHz)	BIT RATE (Gb/s)	Sensitivity (dBm)
[325]	InAlAs/InGaAs 1μm gate length HEMT	PIN-TIA (Monolithic)	~7.3	10	-17.3
[16]	InAlAs/InGaAs 1μm gate length HEMT	PIN-TIA (Monolithic)	>5	10	-19.2
[326]	SiGe HBT	APD+TIA (Hybrid)	9.9	10	-29.5
[327]	InGaP/GaAs HBT	PIN+TIA (Hybrid)	~10	10	-19
[328]	0.18μm CMOS	PD+TIA (Hybrid)	7.2	10	-16.4
[272]	InAlAs/InGaAs 25μm^2 HBT	PIN+TIA (Monolithic)	16	20	-18
[329]	InAlAs/InGaAs/InP DHBT	PIN-TIA+ Limiting Amplifier (Monolithic)	37	40	-9.4
[330]	InP HEMT	EDFA+UTC-PD +TIA (Hybrid)	N/A	40	-27.5
[331]	InAlAs/InGaAs HEMT	WGPD+Diff Distributed Amp (Hybrid)	40	40	-8.4
[15]	InP/InGaAs 5μm^2 HBT	PIN+TIA (Monolithic)	50	>40	-12.7
[309]	0.1μm gate length InP HEMT	UTC-PD+TIA (Hybrid)	43	50	-7.6
[332]	InAlAs/InGaAs ≤0.3μm gate length HEMT	WGPD+TWA (Monolithic)	40	60	-12
THIS WORK	**InP/InGaAs 10×10μm^2 HBT**	**PIN+TIA (Monolithic)**	**15**	**20**	**N/A**

Of course, photoreceivers-based an HEMT and CMOS technologies necessitate sub-micrometer scale gate lengths compared with the relaxed HBT dimensions used here.

However, the process dependent HEMT characteristics and stringent lithography required in CMOS make these devices not a natural choice for high-speed and low-cost manufacturing OEICs. For example, 0.18µm CMOS and 1µm gate length InAlAs/InGaAs HEMT based photoreceivers have -3dB bandwidth of about 6GHz[325, 328]. On the other hand, a reported 5µm^2 emitter size InP/InGaAs HBT exhibited an f_T and f_{max} of 130 and 220GHz respectively[15]. The HBT based OEIC module presented in this work showed a high-frequency performance comparable to reported results [275,303] despite its large mesa size. Furthermore, the simplicity of the HBT processing used throughout this PhD research and promising figure of merits achieved (f_T =54GHz and f_{max} =56GHz) with a reasonable power dissipation of the fully integrated photoreceiver of 30mW which evidently support the conclusion that these devices are suitable for high-performance and low-cost next generation single chip PIN-TIA 10Gb/s EPON fibre-optic systems.

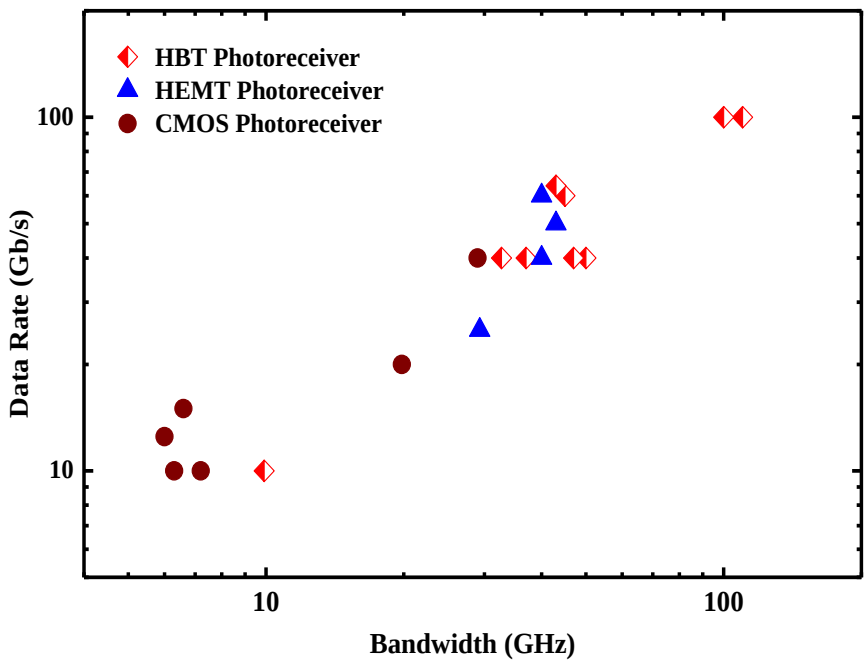


Figure 6.51: Comparison of the reported optical receiver performances in terms of their bandwidth and date rates[13, 15, 83, 309, 317, 326, 328, 329, 331-341].

The most recent optical receiver performance presented in literature show an exponential increase in data rate capability for HBTs, HEMTs and CMOS ICs used in optical communications links. This has been achieved as a result of extensive reduction in lateral HBT dimensions and gate lengths of HEMTs and CMOS devices as shown in figure

(6.51). The reason is due to a the rapidly growing demands for ultra-high data rates optical systems operating beyond 10Gb/s.

6.14 Summary

A detailed study and analysis of the performance of a low-cost PIN-PD and HBT transistor combination for use in optoelectronic integrated circuits was described in this chapter. The base and collector regions of the transistor were designed to form a PIN photodiode which has a DC responsivity and quantum efficiency of 0.5 A/W and 0.45 respectively without antireflection coating and at a wavelength of 1.55µm. The experimental data revealed that the photodiode has a low dark current of ~1.5nA under a fully depleted condition (external applied voltage of -5V). A measured -3dB bandwidth of 18GHz for the 20µm PIN-PD were obtained and the 10×10µm^2 emitter size HBT had a breakdown voltage of approximately 4.5V and a DC current gain, $\boldsymbol{\beta}$ of ~65 at a bias condition $\boldsymbol{V_{CE}}$=2V and $\boldsymbol{I_C}$=10mA. This relatively large device had a Mason's unilateral gain of ~60GHz and exhibited measured $\boldsymbol{f_T}$ and $\boldsymbol{f_{max}}$ of 54 and 57GHz respectively. The measured base sheet resistance was found to be 592Ω/□ extracted from the TLM measurements and attributed to the heavily doped base layer and optimised fabrication process. In addition, the Silvaco physical model employed in this research showed that the use of a thin undoped spacer layer can help to reduce the potential spike at the emitter-base heterojunction, facilitating high current gain at a given bias condition.

The HBT large signal device model was successfully realized in Keysight-ADS software using the UCSD-AGILENTHBT model, which showed excellent agreement characteristics with measured results. For the photodiodes, an opto-electrical equivalent circuit, that takes all physically based parameters into account, was used, contributing to achieving an excellent agreement with the measured data for various PIN mesa sizes. For the monolithically integrated InP/InGaAs PIN-HBTs photoreceiver model, an SFB loop TIA module was implemented in Keysight-ADS with a three-stage preamplifier which has a transimpedance gain of 40dBΩ and consumes an overall DC power of 30mW. The preamplifier exhibited a -3dB electrical bandwidth of 18 and 11GHz with and without a 2nH integrated spiral inductor, which led to enhancing the bandwidth by >60%. This corresponds to a good transimpedance-gain product of 1.8THz.Ω. In addition, the

optical/electrical response of the whole OEIC utilizing 10×10μm^2 HBTs and a 20μm window size PIN-PD offers a bandwidth of ~15GHz, adequate for up to 20 Gb/s data rate operation. For large frequency bandwidth, an MFB topology is required at least with the large HBT feature size used here, providing a small variation in the group delay response due to unnecessary for use an integrated peaking inductor.

A detailed study of the performance analysis of the MFB-TIA found that such a circuit has a transimpedance gain of 45dBΩ with an electrical bandwidth exceeding 18GHz. This corresponds to a high 3.2THz.Ω transimpedance gain product. The use of MFB-TIA has contributed to an increase in the overall DC power consumption to 120mW, however, the deviation in the group delay decreased to 11.7psec up to 20GHz. The promising -3dB bandwidth and group delay are suitable for supporting an optical system with 20Gb/s data rate. Furthermore, a bit stream generator with an NRZ 2^{15}-1 PRBS pattern was used to evaluate both SFB and MFB OEIC and the simulation results revealed that clear open eye diagrams with no observation of ISI for 10 and 20 Gb/s operation were obtained. The evaluated root mean square jitter of the overlapped bit stream for both photoreceiver ICs is 4ps at 20Gb/s while producing an open eye width of >29ps.

CHAPTER 7: CONCLUSION AND FUTURE WORKS

7.1 Conclusion

This final chapter fulfils a dual role: firstly, it is devoted to providing a brief summary regarding the conclusions of the project's main achievements and research undertaken and secondly, proposed ideas and possible future directions of research are discussed to further extend the field.

7.1.1 RTD and Related Circuits

The resonant tunnelling diode is the fastest room temperature solid state semiconductor device for use as a compact THz source due to its operational principle based on quantum mechanical tunnelling. The highest fundamental frequency of the RTD oscillator reported to date is reaching 2THz using highly compressive indium rich quantum wells. The low voltage operation of the RTD at room temperature reduces the power dissipation of the integrated circuit. The negative differential resistance and low bias requirements make this device unique for *mm* and sub-*mm* wavelengths applications. Developments in the MBE techniques have led to achieving highly uniform and smooth monolayer films, enabling high yield DBQW-RTD reproducibility and manufacturability. RTDs with mesa sizes of ~1μm^2 are easy to fabricate using the low-cost i-line lithography technology facility at the University of Manchester. Such device sizes can exhibit a cut-off frequency exceeding 1THz while still maintaining an excellent current density, giving it superior performance abilities, far surpassing those of deep submicron feature CMOS and HEMT based solid state devices.

This work presented an experimental study of double barriers InGaAs/AlAs RTDs designed to improve the diode characteristics and exploring five different device structures covering a parameter space allowing for both high and low current density devices for applications as oscillators or amplifiers. A very good high peak to valley current ratio of 5.2 was obtained for a low current density device, RTD sample #276. More interestingly, these PVCR values were obtained with low J_P characteristics of 0.08 and 0.26mA/μm^2 for samples #276 and #277 and are extremely beneficial for radio frequency MMIC implementations with ultra-low DC power consumption. As expected from the design of the RTDs, the measured results show a significant increase in the

current density resulting from thinner barriers and quantum well widths, for example sample #327 has the highest J_P of 10.8mA/μm^2 followed by sample #302. This is, however, at the somewhat unavoidable cost of an increase in the peak voltages for the high peak current density devices. Deviation in V_P with mesa size of the RTDs was found to be negligibly small for devices with low J_P (samples: #276, #277 and #300). A 36mV/μm^2 voltage deviation was observed for diodes with a peak current density of 10.8mA/μm^2 and is attributed to the self-heating of the diodes. This inherent issue was clarified using pulsed dc voltage tests to verify our proposed explanation for this variation.

To accurately evaluate the cut-off frequency of RTDs, careful extraction procedures of the intrinsic equivalent circuit parameters were performed employing the commercially available software package Keysight-ADS. This model was then validated through excellent matching with actual S-parameter data obtained from on-wafer probing up to 40GHz. An estimated high frequency operational limit of 2.7THz was deduced for RTD sample #327. As far as the requirement for desired characteristics of the RTDs are concerned (including J_P, PVCR and G_{RTD}), samples #302 and #327 would be favored for use in oscillator circuit design and characterizations. From such circuit's perspective, current difference (ΔI) and voltage span (ΔV) are required to be as large as possible, to ensure high RF power is available to the load. The simple epitaxial design of the RTD samples explored avoid quaternary materials or/and graded layers making them easier to manufacture; The highest current density sample XMBE#327 (J_P of 10.8mA/μm^2) still maintained an excellent PVCR ~5, one of the highest ever reported for such a high current density making the diode suitable for low-cost *mm*-wave/THz regime applications. The promising PVCR achieved in this work is more than double of those demonstrated in the literature. Additionally, a more significant result is that a very high G_{RTD} of 95mS/μm^2, the highest to date was reported for the same RTD sample #327 simultaneously achieving both high PVCR and large negative differential conductance. These findings primarily owe much to the combination of excellent grown conditions and material used alongside a well-established photo-mask and developed fabrication process.

Due to occurrence of self-oscillations at low frequencies (2-3GHz) caused by interactions between the DC set-up cables and the RTD's intrinsic capacitance, a stabilizing circuit is

thus required. To fully eliminate this issue, a 25Ω resistor was integrated in parallel with the diodes, cancelling the low-frequency oscillation and allowing the circuit to resonate at the desired operating frequency. The experimental results suggested that the partially stabilizing resistor is limited by the absolute value of the negative differential resistance. Furthermore, an electromagnetic modelling of a 9μm^2 InGaAs/AlAs RTD sample #230, whose J_P is 1.2mA/μm^2, was performed by integrating with a coplanar waveguide resonator. A 100 GHz oscillator was realized in the model and achieved an output power of 100μW. It is also apparent from the spectrum that the first harmonic occurs at 201 GHz with an extremely low power of 0.05 μW. Higher stabilizing resistor, R_{sh} (i.e. $R_{sh} > 1/|G_{RTD}|$) has led to suppression of the oscillation at 100GHz because the stability conditions cannot be satisfied at low frequencies. All the passive components used in realizing the ICs were experimentally characterized, including NiCr resistors, spiral inductors, parallel plate capacitors and CPW transmission lines.

The unique NDR feature of the RTDs can be employed to compensate for the resistive losses of an active transmission line circuit and provided gain at the output port of an amplifier depending on several factors such as R_{RTD} value (i.e. a small G_{RTD} is preferred here) and good matching between the RTDs and branch couplers. In this project, modeling and theoretical analysis of a novel K-band reflection-based amplifier was performed utilizing InGaAs/AlAs RTD sample #277 with a mesa size of 1×2.4 μm^2. The model was built using a lumped element branch line coupler with two active RTD loads. Due to constructively combining the amplified in- phase electromagnetic waves at the output port, a high gain of 32 dB was simulated at 25.3 GHz while maintaining a very low DC power consumption of 256μW. This corresponds to a record figure of merit of 125dB/mW to date, validating the excellent performance of the amplifier. Power gain dependent voltage bias were subsequently studied and ascertained that the amplifier's gain vanishes at an external voltage close to the peak and valley of the NDR region. However, the flatness of the gain is relatively good as long as the diode provides a negative resistance, giving a comfortable process window for the circuit's operation.

7.1.2 HBTs and Optoelectronic Integrated Circuits

An overview of HBT and PIN-PD material system and their figures of merit were covered in this thesis. Extensive characterization study was performed followed by building an InP/InGaAs SHBT and PIN-PD modules. Those devices were fabricated and

then tested at the University of Manchester facility. The implemented model includes extraction of the equivalent circuit parameters with the main purpose of determining the high-frequency capability of the HBT and PIN-PD. A large-signal built-in AGILENTHBT model was used to simulate the heterostructure transistor and a good agreement was found between the simulated and measured results. Due to the specific design of the InP/InGaAs epilayer structures and considering the trade-off between high performance PIN and HBT to fulfil yielding optimum 10 to 20Gb/s OEICs, a 10×10μm^2 emitter mesa size transistor demonstrated an f_T and f_{max} of 54 and 57GHz respectively. The room temperature measurement for the PIN photodiode I-V characteristic with a window size of 20μm showed a low dark current of ~1.5nA for an external applied voltage of -5V. The achieved low leakage current under fully-depleted condition is primarily imparted to the well-designed epitaxial structure and high-quality material. The measured photo-current was 41.5μA at -11dBm optical power with a laser wavelength of λ=1.55μm, corresponding to a 0.5 A/W and 0.45 DC responsivity and quantum efficiency respectively without antireflection coatings and these latter parameters can be improved by roughly 20% by depositing an AR coating on the photodiode's aperture.

The full electrical equivalent circuit models of the illuminated photodiodes do not actually provide a proper clarification for the transit time capacitance. Of course, this would become much worse when the input optical power level is high and at which point the impact of the induced-stored charge in the photodiodes can no longer be ignored. With this in mind, an opto-electrical model with a nonlinear voltage controlled current source was utilized here, taking into account the effects of RC time constant and carrier transit time, from which, the extracted RC limited -3dB bandwidth and -3dB carrier transit time bandwidth were ~17.7 and 36GHz respectively. This emphasizes that the high-speed operation of the vertically illuminated photodiode is obviously limited by its RC time constant. The optical bandwidth is expected to further increase through either shrinking the mesa size or/and optimizing the absorption layer thickness.

The encounraging findings of the AGILENTHBT and PIN-PD opto-elelctrical models were put forward into simulating a monolthically integrated photoreceivers with single and multiple feedback loops, providing an aid to understanding of the simulation results prior to measured data. In both designs, an input stage with shunt feedback topology was used to minmize the input impedance of the reamplifier, resulting into an enhancement in

high-frequency operation. The SFB-TIA front-end amplifier exhibited a 32dBΩ transimpedance gain with a bandwidth of 14GHz; predictably high gain and narrow bandwidth were observed with a large feedback resistor value. To further extend the -3dB bandwidth, a series peaking inductor technique was used and led to widening the bandwidth to 18GHz (i.e. an improvement of >60%), which corresponds to transimpedance gain product of 1.8THz.Ω. However, further increase in the peaking inductor value has a deleterious impact on the group delay variation and overall performance of the photoreceiver thereby this trade-off should be effectively balanced. As the conventional SFB-TIA has low optical overload response, an MFB-TIA circuit was thus investigated. Such a circuit configuration does not only offer relatively high overload optical current but it also has a large bandwidth irrespective of peaking techniques. The MFB-TIA circuit provided a gain of 45dBΩ with an electrical bandwidth exceeding 18GHz while producing deviation in the group delay of 11.7psec up to 20GHz. An OOK NRZ 2^{15}-1 PRBS patterns were applied to the SFB and MFB photoreceivers and it was found that the eye diagrams were clearly open with no observation of inter-symbol interference for 10 and 20 Gb/s operation responses. The results showed negligibly small overshoot or/and undershoot distortion, asserting that these promising results are adequate for supporting 10Gb/s EPON optical systems.

7.2 Future Works

This research provided a solid foundation and presented a wide-ranging study on characterizing and designing RTD based circuits and monolithic integrated optoelectronic ICs. Whist covering many aspects in this thesis, there are still a number of potential explorations to further extend this work in the future and in particular:

7.2.1 Low DC Power RF Circuits

Since various RTD devices have been fully characterized in terms of their DC and RF parameters and IC amplifiers designed using Keysight-ADS software, the next step is to fabricate amplifier IC operating beyond 50GHz. In fact, the main objective is to demonstrate a low cost, sub-milliwatt power consumption and narrow band amplifier-based quantum device. For this stage, Keysight-ADS momentum and 3D simulator EMPro commercial software can be used to accurately model the lumped-element branch line coupler at different operating frequencies starting from 5 up to 100GHz. Thinning

the substrate thickness to 100µm or lower will be needed to minimize the platform losses for low noise figure properties and to further mitigate the effects of associated parasitics. Once the required modeling results are optimized, the amplifier can be fabricated utilizing RTD samples XMBE#276, #277 and #300, the circuits' FOM measurement will be then performed and compared with the state of art. Moreover, an interesting IC that would be useful to implement is a low power consumption full duplex bidirectional amplifier. Such circuits are highly useful in wireless transceiver systems, retrodirective antenna arrays and RFID tags. They can be mostly implemented by incorporating two identical one port amplifiers and a single branch coupler. Additionally, physical RTD modeling is extremely beneficial and insightful in terms of DC and RF modeling utilizing Silvaco Atlas particularly prior to the costly growth and fabrication process.

7.2.2 *mm*-wave/THz ICs

Due to the rapidly growing trends in data rates for wireless communications, an implementation of an ultra-high speed RTD transmitter capable of operating beyond 20Gb/s becomes indispensable. To this end, design an offset slot antenna with variety of slot antenna lengths and widths to obtain a number of fundamental oscillation frequencies were carried out on CST Microwave Studio software as shown in figure (8.1). This was to implement an RTD emitter operating at 250 and 500GHz radiating from the substrate with coupled hemispherical silicon lens.

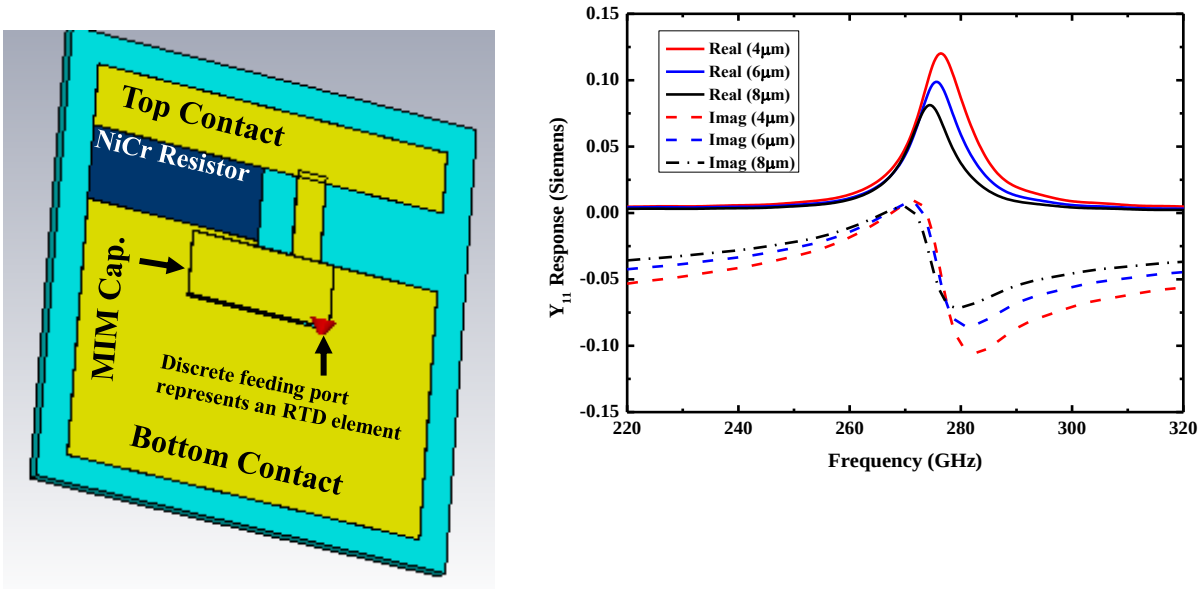


Figure 7.1: 3D structure of an offset slot antenna modeled using CST-MS with different slot width alongside the real and imaginary parts of Y_{11} response showing a resonant frequency of ~275GHz.

Once, the model was optimized and fulfilled the circuit's requirement regarding wide frequency bandwidth and low return loss, a mask design was built; however, those designs were not presented in this work as fabrication results have not been finished yet.

The excellent experimental results obtained for RTD sample XMBE#327 can allow us to manufacture a high RF power RTD oscillator with a small stabilizing resistor of <6Ω, improving the circuit performance in terms of lower noise operation with an enhancement in the efficiency of the oscillators. The design depicted in figure (8.1) can be also used for room temperature operating imaging applications. Since the peak of the antenna's radiation conductance (i.e. real part of Y_{11}) increases when the slot width gets smaller, low impedance is attainable at high frequency (high power capability due to well-matched with integrated RTD). Furthermore, a mW scale power transmitter will be pursued by integrating multi-elements array configuration RTD oscillators using power combining method with either MIM coupling stub or mutual injection locking technique. For the imaging applications, an alternative array configuration using a dipole antenna for several frequency peaks will be designed and tested. This technique was recently reported by Tokyo Institute of Tech. group and has achieved an output power of about 135µm at 0.92THz with ten-integrated oscillators[49].

7.2.3 HBTs and Implementation of OEICs

Even though this thesis has covered an extensive study focusing on developing a low cost photoreceiver based HBTs operating at 1.55µm wavelength, there are still several important tasks to do in future. The first logical step will be to fabricate and examine the designed SFB and MFB TIA amplifiers and photoreceivers. The current HBT process might be unable to provide small device feature sizes with adequate HBT performances required to boost the cut-off frequency. Therefore, a self-aligned process will be used to scale the emitter size down to nearly 1×5µm^2, which is expected to maximize the f_T and f_{max} to roughly >200GHz. As self-aligned small devices have in general poor yield, an adaptation of a Si_3N_4 process as proposed by Ren *et al*[342] will be exploited to improve the yield process, in which a layer of Si_3N_4 is sputtered on the side wall of the emitter to cover the active layers. This process is often performed before depositing the base metallization scheme and so would assist in reducing the risk of shorting of emitter and base ohmic contacts. For the PIN-PDs, the depletion capacitance (RC time constant) can

be lowered up to at least 30% by decreasing the mesa size of the device. This can undoubtedly help to extend the optical bandwidth and it is favoured over the use of mushroom-like structure or waveguide-illumination technique. When the small sizes process for the HBTs and PIN-PDs are achieved, an optimized low-cost TIA and photoreceiver can be then manufactured aiming to operate beyond 40Gb/s. Another possible option to attempt is that of designing an automatic gain control circuit with different amplifier's configurations, for instance common base input stage and differential output configuration. The idea is to compare the photoreceiver characteristics namely the overload optical current, dynamic range, group delay and noise performance, giving an in-depth investigation and an aid to fully understanding the response of the actual measured data.

APPENDIX

APPENDIX-A: RTD CIRCUITS' MODULE

- **How to extract a spectrum using FFT-Function in Keysight-ADS:**

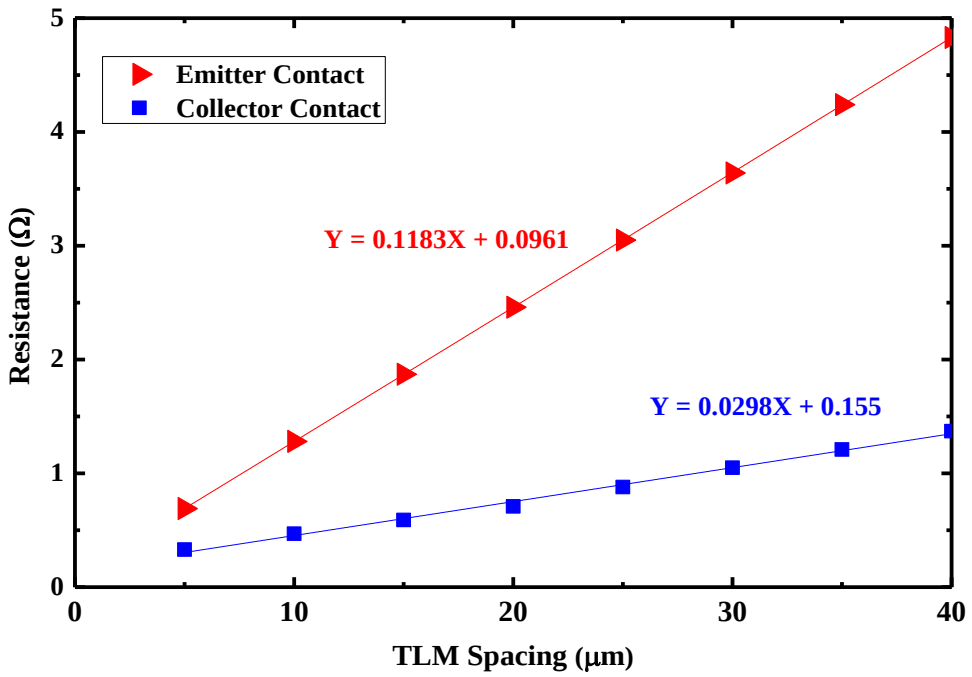
$$P_{out} = fs(V_{out}, 1MHz, 500GHz)$$

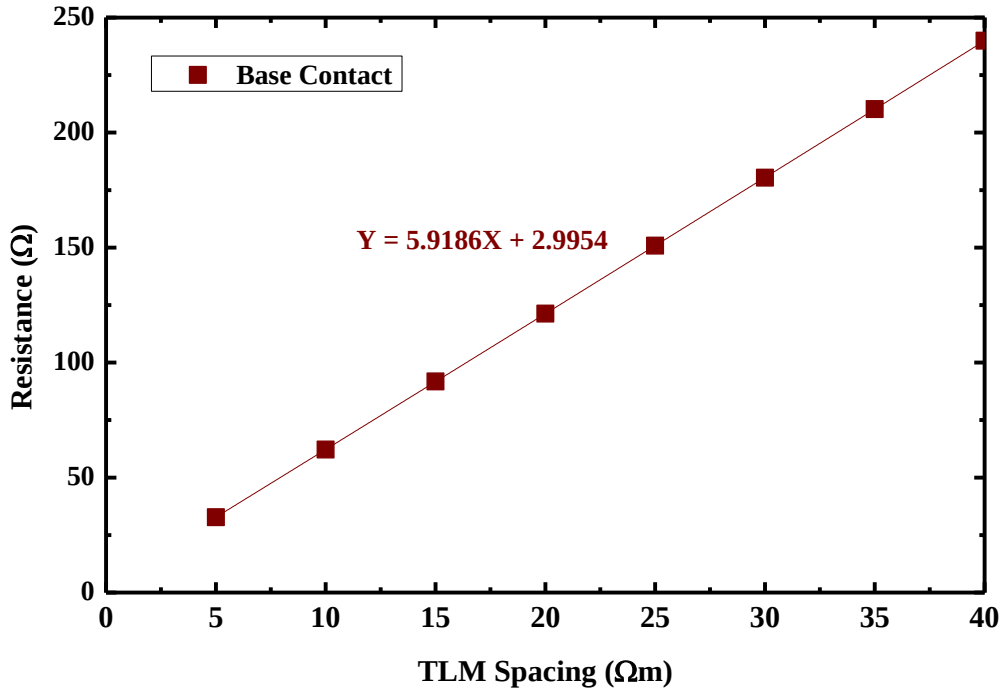
- **How to extract gain of an RTD amplifier in Keysight-ADS:**

$$P_{in} = 0.5 * real(V_{in} * conj(I_{in}))$$
$$P_{out} = 0.5 * real(V_{out} * conj(I_{out}))$$
$$P_{in-dB} = 10 * log(abs(mix(P_{in}, \{1\}, MIX)))$$
$$P_{out-dB} = 10 * log(abs(mix(P_{out}, \{1\}, MIX)))$$
$$Gain_{dB} = (P_{out-dB}) - (P_{in-dB})$$

APPENDIX-B: HBT PARAMETRICAL MODEL AND EXPERIMENTAL DATA

1. Measured results of TLM for HBT sample F17D2102A with an emitter area of 10×10μm^2:





2. HBT Physical Model for device F17D2102A with an emitter area of 10×10μm^2:

```
# (c) Silvaco Inc., 2017
# single hetrostructure bipolar transitor.

go atlas

## EpiLayer Thickness
set t_ohmic1          =0.15
set t_emitter1        =0.15
set t_emitter2        =0.04
set t_spacer          =0.005
set t_base            =0.065
set t_collector       =0.8
set t_subcollector    =0.5

## Doping Concentrations
set d_ohmic1       =1.5e19
set d_emitter1     =5e17
set d_emitter2     =5e17
set d_base         =2.5e19
set d_subcollector  =1e19

## Device Size, Mesa Area
set d_emitter_mesa     =0.25
set d_basemesa_min     =0.5
set d_basemesa_max     =0.75
set d_collectormesa_min     =1
set d_collectormesa_max     =1.25

##Device Thickness
set A=$t_ohmic1
set B=$A+$t_emitter1
set C=$B+$t_emitter2
```

```
set D=$C+$t_spacer
set E=$D+$t_base
set F=$E+$t_collector
set G=$F+$t_subcollector

####--------------------Device Mesh--------------------####
mesh          width=1

x.mesh loc=0.00                      spac=0.01
x.mesh loc=$d_collectormesa_max      spac=0.01
#x.mesh loc=$d_emitter_mesa           spac=0.01
#x.mesh loc=$d_basemesa_min           spac=0.01
#x.mesh loc=$d_basemesa_max           spac=0.01
#x.mesh loc=$d_collectormesa_min      spac=0.01
#x.mesh loc=$d_collectormesa_max      spac=0.01

y.mesh loc=0            spac=0.005
y.mesh loc=$A           spac=0.002
y.mesh loc=$B           spac=0.005
y.mesh loc=$C           spac=0.001
y.mesh loc=$D           spac=0.001
y.mesh loc=$E           spac=0.005
y.mesh loc=$F           spac=0.005
y.mesh loc=$G           spac=0.005

####-------------------Device Region-------------------####
region num=1  name=ohmic1        material=InGaAs    x.comp=0.47
y.max=$A      x.min=0 x.max=$d_collectormesa_max
region num=2  name=emitter1      material=InGaAs    x.comp=0.47
y.min=$A             y.max=$B      x.min=0 x.max=$d_collectormesa_max
region num=3  name=emitter2      material=InP
y.min=$B             y.max=$C      x.min=0 x.max=$d_collectormesa_max
region num=4 name=spacer         material=InGaAs    x.comp=0.47
y.min=$C             y.max=$D      x.min=0 x.max=$d_collectormesa_max
region num=5  name=base          material=InGaAs    x.comp=0.47
y.min=$D             y.max=$E      x.min=0 x.max=$d_collectormesa_max
region num=6  name=collector     material=InGaAs    x.comp=0.47
y.min=$E             y.max=$F      x.min=0 x.max=$d_collectormesa_max
region num=7  name=subcollector  material=InGaAs    x.comp=0.47
y.min=$F             y.max=$G      x.min=0 x.max=$d_collectormesa_max
region num=8  name=Etch1         material=SiO2
x.min=$d_emitter_mesa  x.max=$d_basemesa_max  y.min=0.0  y.max=$D
region num=9 name=Etch2          material=SiO2
x.min=$d_basemesa_max  x.max=$d_collectormesa_max  y.min=0.0  y.max=$F

####---------------------Electrode---------------------####
electrode num=1 name=emitter x.min=0.0 x.max=$d_emitter_mesa    y.max=0
electrode num=2 name=base x.min=$d_basemesa_min
x.max=$d_basemesa_max    y.min=$D y.max=$D
electrode num=3 name=collector x.min=$d_collectormesa_min
x.max=$d_collectormesa_max    y.min=$F y.max=$F

####----------------------Doping----------------------####
doping        reg=1         uniform       n.type        conc=$d_ohmic1
doping        reg=2         uniform       n.type
conc=$d_emitter1
doping        reg=3         uniform       n.type
conc=$d_emitter2
doping        reg=5         uniform       p.type        conc=$d_base
doping        reg=7         uniform       n.type
conc=$d_subcollector
```

```
####----------------------Material---------------------####

material name=ohmic1        eg300=0.74     affinity=4.5  taun0=3e-10
taup0=1e-8   mun=3000 mup=100
material name=emitter1      eg300=0.74     affinity=4.5  taun0=3e-10
taup0=1e-8   mun=5000 mup=150
material name=emitter2      eg300=1.344    affinity=4.38 taun0=1e-8
taup0=1e-9   mun=3000 mup=150
material name=spacer        eg300=0.74     affinity=4.5  taun0=3e-10
taup0=1e-8   mun=11000 mup=250
material name=base          eg300=0.74     affinity=4.5  taun0=3e-10
taup0=1e-8   mun=3000 mup=100
material name=collector     eg300=0.74     affinity=4.5  taun0=3e-10
taup0=1e-8   mun=11000 mup=250
material name=subcollector  eg300=0.74     affinity=4.5  taun0=3e-10
taup0=1e-8   mun=3000 mup=100

output band.param con.band val.band

model  srh fldmob  print
model material=InGaAs evsatmod=1
model material=InP evsatmod=1

solve init
save outf=HBT.str
tonyplot  HBT.str
solve v3=0.0001
solve v3=0.001
solve v3=0.01
solve v3=0.1
solve v3=2
solve v2=0.0001
solve v2=0.001
solve v2=0.01
solve v2=0.1
solve vstep=0.05 vfinal=0.4 electrode=2

log outf=HBT_IV.log

solve
solve vstep=0.05 vfinal=1.5 electrode=2

save outfile=HBT_IV.str
tonyplot HBT_IV.str
tonyplot HBT_IV.log -set HBT_gummel.set
tonyplot HBT_IV.log -set HBT_IV_dccurrentgain.set

extract init infile="HBT_IV.log"
extract name="Ic" y.val from curve(v."base",i."collector") where
x.val=1.5
extract name="Ib" y.val from curve(v."base",i."base") where x.val=1.5
extract name="betamax" $Ic/$Ib

quit

method gummel  newton trap  vsatmod.inc=0.01

solve
solve local vcollector=2.0

log outf=HBT.log master
```

```
solve vbase=0.025
solve vbase=0.1

method  newton  trap autonr vsatmod.inc=0.01 itlim=50

solve vbase=0.2 vstep=0.1 name=base vfinal=1.4
solve vbase=1.45 vstep=0.025 name=base vfinal=1.5


tonyplot HBT.log

go atlas

mesh     infile=HBT.str

solve init
solve vbase=0.01
solve vbase=0.05
solve vbase=0.70

contact  name=base current

log outfile=HBT_IV.log
solve ibase=1.0e-6
solve vcollector=0.01
solve name=collector vcollector=0.05 vstep=0.05 vfinal=0.50
solve name=collector vcollector=0.60 vstep=0.20 vfinal=2.00
solve ibase=2.0e-6
solve vcollector=1.99
solve name=collector vcollector=1.90 vstep=-0.20 vfinal=0.7
solve name=collector vcollector=0.65 vstep=-0.05 vfinal=0.0
solve ibase=3.0e-6
solve vcollector=0.01
solve name=collector vcollector=0.05 vstep=0.05 vfinal=0.90
solve name=collector vcollector=1.00 vstep=0.20 vfinal=2.0
solve ibase=4.0e-6
solve vcollector=1.99
solve name=collector vcollector=1.90 vstep=-0.20 vfinal=1.1
solve name=collector vcollector=1.05 vstep=-0.05 vfinal=0.0
tonyplot HBT_IV.log -set hbtex07_IV.set

quit
```

3. Parameter Definition of UCSD- AGILENTHBT

PARAMETER	Name Description and Comments Units Default	Units	Default
Tnom	Nominal temperature (temperature at which the room temperature parameters are extracted)	°C	25
Re	Emitter resistance	Ohm	2.0
Rci	Intrinsic collector resistance	Ohm	1.0
Rcx	Extrinsic collector resistance	Ohm	5.0
Rbi	Intrinsic base resistance	Ohm	15.0
Rbx	Extrinsic base resistance	Ohm	5.0

Is	**Collector-Emitter current: Forward collector saturation current**	**A**	**1.0e-25**
Nf	**Collector-Emitter current: Forward collector current ideality factor**	**None**	**1.0**
Isr	**Collector-Emitter current: Reverse emitter saturation current**	**A**	**1.00e-15**
Nr	**Collector-Emitter current: Reverse emitter current ideality factor**	**None**	**2.0**
Ish	**Base-Emitter current: Ideal base-emitter current**	**A**	**1.0e-27**
Nh	**Base-Emitter current: Ideal base-emitter current ideality factor**	**None**	**1.0**
Ise	**Base-Emitter current: Non-ideal base-emitter current**	**A**	**1.0e-18**
Ne	**Base-Emitter current: Non-ideal base-emitter current ideality factor**	**None**	**2.0**
Isrh	**Base-Collector current: Ideal base-collector saturation current**	**A**	**1.0e-15**
Nrh	**Base-Collector current: Ideal base-collector current ideality factor**	**None**	**2.0**
Isc	**Base-Collector current: Non-ideal base-collector saturation current**	**A**	**1.0e-13**
Nc	**Base-Collector current: Non-ideal base-collector current ideality factor**	**None**	**2.0**
Abel	**Base-Emitter current: Portion of base-emitter current allocated to extrinsic region**	**None**	**0.0**
Vaf	**Forward Early voltage**	**V**	**500**
Var	**Reverse Early voltage**	**V**	**1000**
Isa	**Base-emitter heterojunction saturation current (BE barrier effects)**	**A**	**1.0e+10**
Na	**Base-emitter heterojunction ideality factor**	**None**	**1.0**
Ne	**Base-Emitter current: Non-ideal base-emitter current ideality factor**	**None**	**2.0**
Isrh	**Base-Collector current: Ideal base-collector saturation current**	**A**	**1.0e-15**
Nrh	**Base-Collector current: Ideal base-collector current ideality factor**	**None**	**2.0**
Isc	**Base-Collector current: Non-ideal base-collector saturation current**	**A**	**1.0e-13**
Nc	**Base-Collector current: Non-ideal base-collector current ideality factor**	**None**	**2.0**
Abel	**Base-Emitter current: Portion of base-emitter current allocated to extrinsic region**	**None**	**0.0**
Vaf	**Forward Early voltage**	**V**	**500**
Var	**Reverse Early voltage**	**V**	**1000**
Isa	**Base-emitter heterojunction saturation current (BE barrier effects)**	**A**	**1.0e+10**
Na	**Base-emitter heterojunction ideality factor**	**None**	**1.0**
Isb	**Base-collector heterojunction saturation current (BC barrier effects)**	**A**	**1.0e+10**
Nb	**Base-collector heterojunction ideality factor**	**None**	**1.0**
Ikdc1	**I-V knee effect: Slope of q3 function**	**A**	**1.0**
Ikdc2Inv †	**I-V knee effect: Transition width of Ic**	**A^{-1}**	**infinity** †
Ikdc3	**I-V knee effect: I-V knee effect critical current**	**A**	**1.0**
VkdcInv	**I-V knee effect: Transition width of Vcb**	**V^{-1}**	**0.1**
Nkdc	**I-V knee effect: Maximum value of q3**	**None**	**3.0**
Gkdc	**I-V knee effect: Exponent of q3 factor in base current**	**None**	**0.0**
Ik	**High injection roll-off current**	**A**	**1.0**
Cje	**Base-emitter capacitance: zero-bias capacitance**	**F**	**4.0e-14**

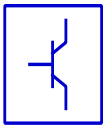
Vje	**Base-emitter capacitance: built-in voltage**	**V**	**1.3**
Mje	**Base-emitter capacitance: grading factor**	**None**	**0.3**
Cemax	**Base-emitter capacitance: maximum value in forward bias**	**F**	**1.0e-13**
Vpte	**Base-emitter capacitance: punch-through voltage**	**V**	**1.0**
Mjer	**Base-emitter capacitance: grading factor beyond punchthrough**	**None**	**0.05**
Abex	**Base-emitter capacitance: ratio between extrinsic and total base-emitter regions**	**None**	**0.0**
Cjc	**Base-collector capacitance: zero-bias capacitance**	**F**	**5.0e-14**
Vjc	**Base-collector capacitance: built-in voltage**	**V**	**1.1**
Mjc	**Base-collector capacitance: grading factor**	**None**	**0.3**
Ccmax	**Base-collector capacitance: maximum value in forward bias**	**F**	**9.0e-14**
Vptc	**Base-collector capacitance: punch-through voltage**	**V**	**3.0**
Mjcr	**Base-collector capacitance: grading factor beyond punch-through**	**None**	**0.03**
Abcx	**Base-collector capacitance: Ratio between extrinsic and total base-collector regions**	**None**	**0.75**
Tfb	**Base delay: Intrinsic base transit time**	**sec**	**1.0e-12**
Fextb	**Base delay: Fraction of base delay charge allocated to B-C junction**	**None**	**0.2**
Tfc0	**Collector delay: Low current transit time**	**sec**	**2.0e-12**
Tcmin	**Collector delay: High current transit time**	**sec**	**5.0e-13**
Itc	**Collector delay: Midpoint in Ice between Tfc0 and Tcmin**	**A**	**0.006**
Itc2	**Collector delay: Width in Ic between Tfc0 and Tcmin**	**A**	**0.008**
Vtc0Inv	**Collector delay: Rate of change of Tfc0 with Vcb**	**V^{-1}**	**0.3**
Vtr0	**Collector delay: Transition width in Vcb to Vmx0**	**V**	**2.0**
Vmx0	**Collector delay: Maximum Vcb for Tfc0**	**V**	**2.0**
VtcminInv	**Collector delay: Rate of change of Tcmin with Vcb**	**V^{-1}**	**0.5**
Vtrmin	**Collector delay: Transition width in Vcb to Vmxmin**	**V**	**1.0**
Vmxmin	**Collector delay: Maximum Vbc for Tcmin**	**V**	**1.0**
VtcInv	**Collector delay: Rate of change of Itc with Vcb**	**V^{-1}**	**0.1**
Vtc2Inv	**Collector delay: Rate of change of Itc2 with Vcb**	**V^{-1}**	**0.1**
Fextc	**Collector delay: Fraction of collector delay charge allocated to B-C junction**	**None**	**0.8**
Tkrk	**Kirk effect delay: Kirk effect delay time**	**sec**	**1.00e-12**
Ikrk	**Kirk effect delay: Critical current for Kirk effect**	**A**	**0.025**
Ikrktr	**Kirk effect delay: Transition width to Ikirk=0**	**A**	**1.00e-06**
Vkrk	**Kirk effect delay: Rate of change of Ikrk with Vcb**	**V**	**3.0**
Vkrk2Inv	**Kirk effect delay: Rate of change of Tkrk with Vcb**	**V^{-1}**	**0.2**
Gkrk	**Kirk effect delay: Exponent of Kirk effect delay**	**None**	**4.0**
Vktr	**Kirk effect delay: Transition width in Vcb to Vkmx**	**V**	**1.0**
Vkmx	**Kirk effect delay: Maximum Vcb**	**V**	**1.0**
Fexke	**Fraction of Kirk effect charge allocated to the B-C junction**	**None**	**0.2**

Tr	**Reverse transit time**	**sec**	**1.0e-09**
Cpce	**Parasitic / fringing collector-emitter capacitance**	**F**	**1.0e-15**
Cpbe	**Parasitic / fringing base-emitter capacitance**	**F**	**1.0e-15**
Cpbc	**Parasitic / fringing base-collector capacitance**	**F**	**1.0e-15**
Lpb	**Parasitic base inductance**	**H**	**0.0**
Lpc	**Parasitic collector inductance**	**H**	**0.0**
Lpe	**Parasitic emitter inductance**	**H**	**0.0**
Xrb	**Temperature exponent for Rbi and Rbx**	**None**	**0.0**
Xrc	**Temperature exponent for Rci and Rcx**	**None**	**0.0**
Xre	**Temperature exponent for Re**	**None**	**0.0**
Tvje	**Rate of change in temperature of Vje**	**V/K**	**0.0**
Tvpe	**Rate of change in temperature of Vpte**	**V/K**	**0.0**
Tvjc	**Rate of change in temperature of Vjc**	**V/K**	**0.0**
Tvpc	**Rate of change in temperature of Vptc**	**V/K**	**0.0**
Tnf	**Rate of change in temperature of Nf**	**K^{-1}**	**0.0**
Tnr	**Rate of change in temperature of Nr**	**K^{-1}**	**0.0**
Ege	**Effective emitter band gap parameter**	**V**	**1.55**
Xtis	**Temperature exponent for Is**	**None**	**3.0**
Xtih	**Temperature exponent for Ish**	**None**	**4.0**
Xtie	**Temperature exponent for Ise**	**None**	**3.0**
Egc	**Effective collector bandgap parameter**	**V**	**1.5**
Xtir	**Temperature exponent for Isr**	**None**	**3.0**
Xtic	**Temperature exponent for Isc**	**None**	**3.0**
Xtirh	**Temperature exponent for Isrh**	**None**	**4.0**
Xtik3	**Temperature exponent for Ikdc3**	**None**	**0.0**
Eaa	**Temperature dependence of Isa**	**V**	**0.0**
Eab	**Temperature dependence of Isb**	**V**	**0.0**
Xtfb	**Temperature exponent for Tfb**	**None**	**0.0**
Xtcmin	**Temperature exponent for Tcmin**	**None**	**0.0**
Xtfc0	**Temperature exponent for Tfc0**	**None**	**0.0**
Xitc	**Temperature exponent for Itc**	**None**	**0.0**
Xitc2	**Temperature exponent for Itc2**	**None**	**0.0**
Xtkrk	**Temperature exponent for Tkrk**	**None**	**0.0**
Xikrk	**Temperature exponent for Ikrk**	**None**	**0.0**
Xvkrk	**Temperature exponent for Vkrk**	**None**	**0.0**
Rth1	**Thermal resistance #1**	**K/W**	**1000.0**
Cth1	**Thermal capacitance #1**	**J/K**	**5e-10**

Xth1	**Temperature exponent for Rth1**	**None**	**0.0**
Rth2	**Thermal resistance #2**	**K/W**	**0.0**
Cth2	**Thermal capacitance #2**	**J/K**	**0.0**
Xth2	**Temperature exponent for Rth2**	**None**	**0.0**
Kf	**Flicker (1/f) noise coefficient**	**None**	**0.0**
Af	**Flicker (1/f) noise exponent**	**None**	**1.0**
Ffe	**Flicker (1/f) noise frequency exponent**	**None**	**1.0**
Kb	**Burst (popcorn) noise exponent**	**None**	**0.0**
Ab	**Burst (popcorn) noise corner frequency**	**None**	**1.0**
Fb	**Burst noise corner frequency**	**Hz**	**1**
Imax	**Explosion current**	**A**	**10**
wBvbe	**Base-emitter reverse voltage (warning)**	**V**	**0.0**
wBvbc	**Base-collector reverse voltage (warning)**	**V**	**0.0**
wBvbc	**Base-collector reverse voltage (warning)**	**V**	**0.0**
wVbcfwd	**Base-collector forward bias (warning)**	**V**	**0.0**
wIbmax	**Maximum base current (warning)**	**A**	**0.0**
wIcmax	**Maximum collector current (warning)**	**A**	**0.0**
wPmax	**Maximum power dissipation (warning)**	**W**	**0.0**
Version	**Model version/revision (1.0 = ADS2003C, 2.0 = ADS2004A)**	**None**	**2.0**
AllParams	**Data Access Component (DAC) Based Parameters**	**None**	**None**

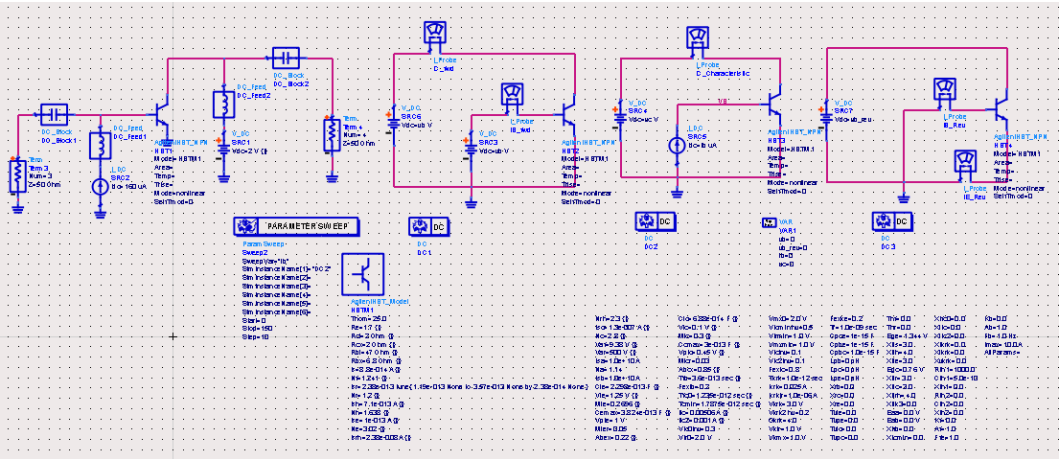
4. AGILENTHBT model related Circuits in Keysight-ADS

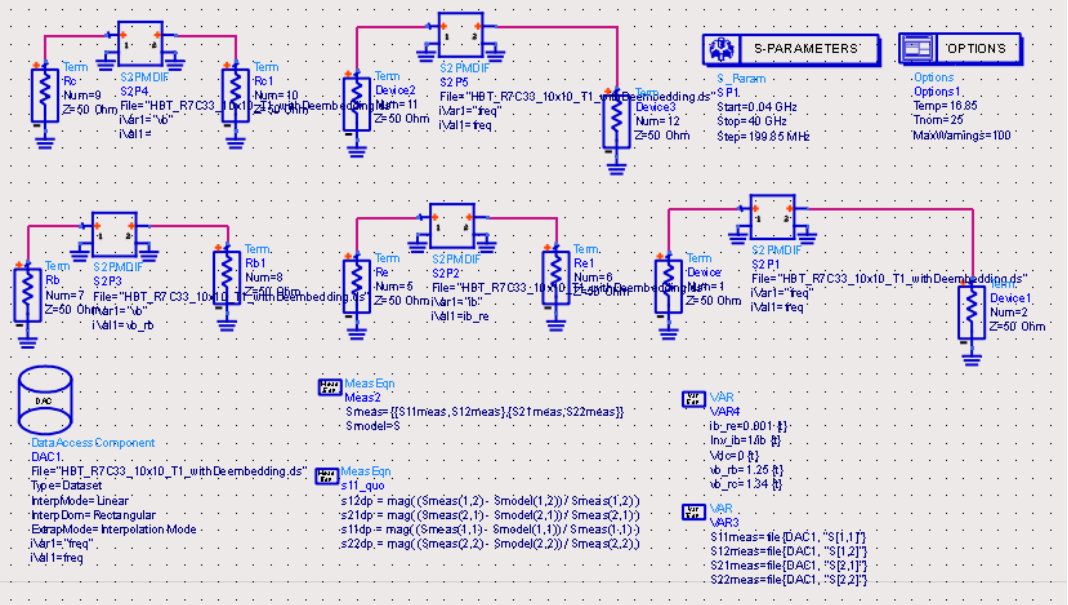
- **UCSD modelling parameters for HBT sample F17D2102A with an emitter area of 10×10μm^2:**



AgilentHBT_Model
HBTM1

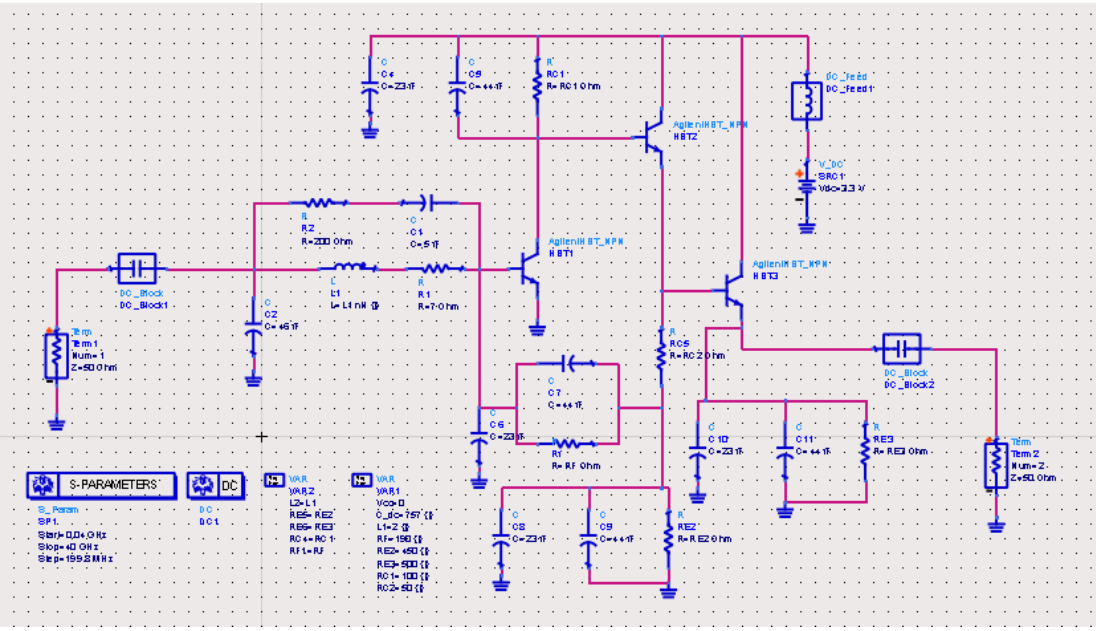
Tnom=25.0	Nrh=2.3	Cjc=5e-014 F	Vmx0=2.0 V	Fexke=0.2	Tnf=0.0	Xtfc0=0.0	Kb=0.0
Re=1.7 Ohm	Isc=1.3e-007 A	Vjc=0.1 V	VtcminInv=0.5	Tr=1.0e-09 sec	Tnr=0.0	Xitc=0.0	Ab=1.0
Rci=2 Ohm	Nc=2.8	Mjc=0.3	Vtrmin=1.0 V	Cpce=1e-15 F	Ege=1.344 V	Xitc2=0.0	Fb=1.0 Hz
Rcx=2 Ohm	Vaf=9.38 V	Ccmax=3e-013 F	Vmxmin=1.0 V	Cpbe=1e-15 F	Xtis=3.0	Xtkrk=0.0	Imax=10.0 A
Rbi=47 Ohm	Var=500 V	Vptc=0.3 V	VtcInv=0.1	Cpbc=1.0e-15 F	Xtih=4.0	Xikrk=0.0	AllParams=
Rbx=6.8 Ohm	Isa=1.0e+10 A	Mjcr=0.03	Vtc2Inv=0.1	Lpb=0 pH	Xtie=3.0	Xvkrk=0.0	
Is=8.8e-014 A	Na=1.14	Abcx=0.7	Fextc=0.8	Lpc=0 pH	Egc=0.76 V	Rth1=1000.0	
Nf=1.241	Isb=1.0e+10 A	Tfb=3.6e-013 sec	Tkrk=1.0e-12 sec	Lpe=0 pH	Xtir=3.0	Cth1=5.0e-10	
Isr=2.38e-013	Cje=2.48e-013 F	Fextb=0.2	Ikrk=0.025 A	Xrb=0.0	Xtic=3.0	Xth1=0.0	
Nr=1.2	Vje=1.25 V	Tfc0=1.235e-012 sec	Ikrktr=1.0e-06 A	Xrc=0.0	Xtirh=4.0	Rth2=0.0	
Ish=7.1e-013 A	Mje=0.2696	Tcmin=1.7875e-012 sec	Vkrk=3.0 V	Xre=0.0	Xtik3=0.0	Cth2=0.0	
Nh=1.638	Cemax=4e-013 F	Itc=0.00506 A	Vkrk2Inv=0.2	Tvje=0.0	Eaa=0.0 V	Xth2=0.0	
Ise=1e-013 A	Vpte=1 V	Itc2=0.001 A	Gkrk=4.0	Tvpe=0.0	Eab=0.0 V	Kf=0.0	
Ne=3.02	Mjer=0.05	Vtc0Inv=0.3	Vktr=1.0 V	Tvjc=0.0	Xtfb=0.0	Af=1.0	
Isrh=2.38e-008 A	Abex=0.23	Vtr0=2.0 V	Vkmx=1.0 V	Tvpc=0.0	Xtcmin=0.0	Ffe=1.0	



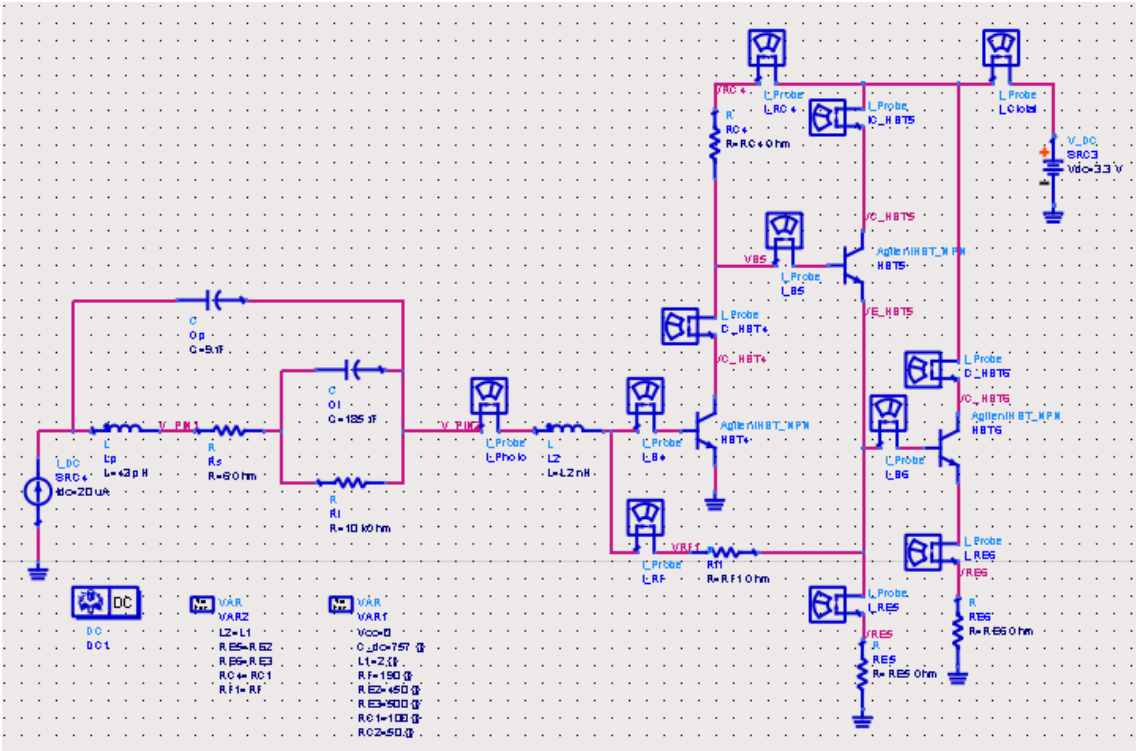


APPENDIX-C: TIA AND OEIC IN KEYSIGHT-ADS

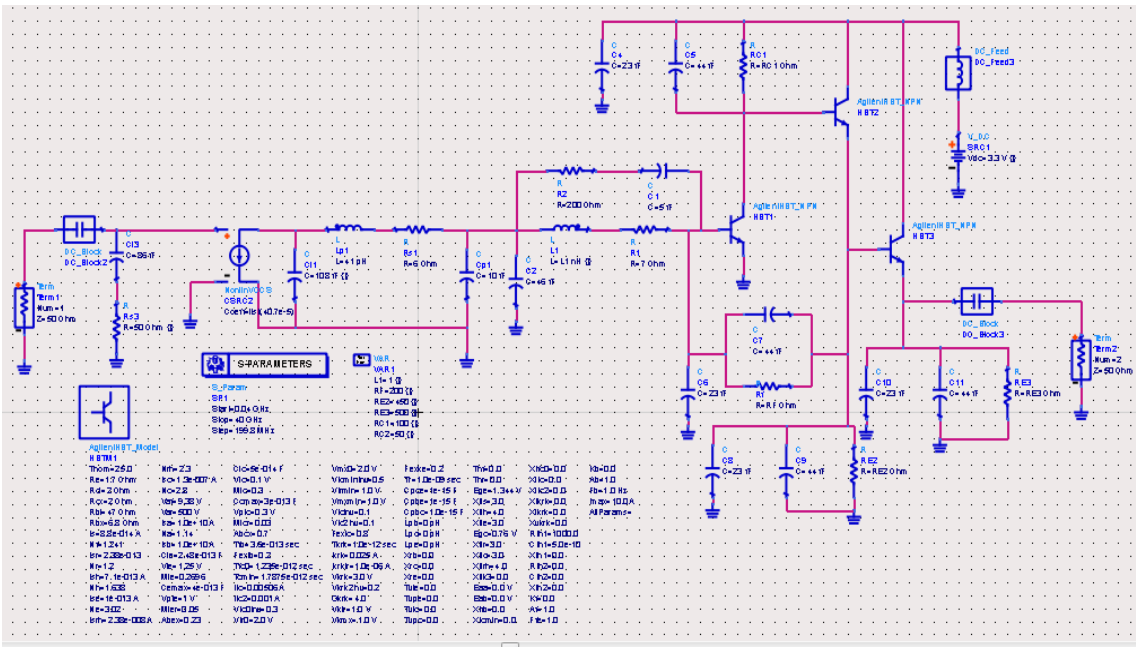
- **TIA integrated circuit:**



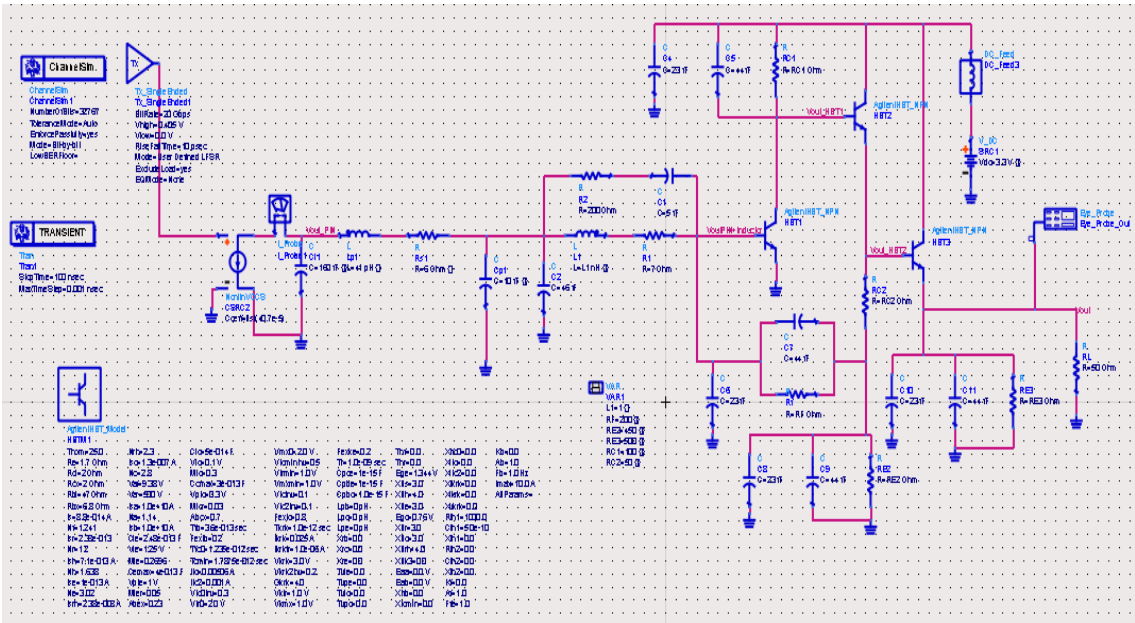
- **How to calculate TIA's DC power consumption:**



- **OEIC for optical bandwidth simulation:**



- **OEIC with channel simulator tool:**



REFERENCES

[1] R. Tsu and L. Esaki, "Tunneling in a finite superlattice," *Applied physics letters,* vol. 22, no. 11, pp. 562-564, 1973.

[2] T. Miyamoto, A. Yamaguchi, and T. Mukai, "Terahertz imaging system with resonant tunneling diodes," *Japanese Journal of Applied Physics,* vol. 55, no. 3, p. 032201, 2016.

[3] M. Seo *et al.*, "InP HBT IC technology for terahertz frequencies: Fundamental oscillators up to 0.57 THz," *IEEE Journal of Solid-State Circuits,* vol. 46, no. 10, pp. 2203-2214, 2011.

[4] S.-J. Yeon, M. Park, J. Choi, and K. Seo, "610 GHz InAlAs/In 0.75 GaAs metamorphic HEMTs with an ultra-short 15-nm-gate," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 613-616: IEEE.

[5] W. Snodgrass, B.-R. Wu, K. Cheng, and M. Feng, "Type-II GaAsSb/InP DHBTs with Record fT= 670 GHz and Simultaneous fT, fMAX> 400 GHz," in *2007 International Electron Devices Meeting, Washington DC, December 10-12, 2007, Pages 663-666*, 2007: Institute of Electrical and Electronics Engineers.

[6] J. Wang, "Monolithic microwave/millimetrewave integrated circuit resonant tunnelling diode sources with around a milliwatt output power," PhD thesis, University of Glasgow, 2014.

[7] M. Asada, S. Suzuki, and N. Kishimoto, "Resonant tunneling diodes for sub-terahertz and terahertz oscillators," *Japanese Journal of Applied Physics,* vol. 47, no. 6R, p. 4375, 2008.

[8] H. Kanaya, T. Maekawa, S. Suzuki, and M. Asada, "Structure dependence of oscillation characteristics of resonant-tunneling-diode terahertz oscillators associated with intrinsic and extrinsic delay times," *Japanese Journal of Applied Physics,* vol. 54, no. 9, p. 094103, 2015.

[9] R. Izumi, S. Suzuki, and M. Asada, "1.98 THz resonant-tunneling-diode oscillator with reduced conduction loss by thick antenna electrode," in *Infrared, Millimeter, and Terahertz Waves (IRMMW-THz), 2017 42nd International Conference on*, 2017, pp. 1-2: IEEE.

[10] A. Y. Tang, V. Drakinskiy, K. Yhland, J. Stenarson, T. Bryllert, and J. Stake, "Analytical extraction of a Schottky diode model from broadband S-parameters," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 5, pp. 1870-1878, 2013.

[11] Y. Akahori, Y. Akatsu, A. Kohzen, and J. Yoshida, "10-Gb/s high-speed monolithically integrated photoreceiver using InGaAs pin PD and planar doped InAlAs/InGaAs HEMTs," *IEEE photonics technology letters,* vol. 4, no. 7, pp. 754-756, 1992.

[12] K. Yamashita, Y. Oihawa, T. Yamamoto, H. Ohnishi, T. Mihawa, and H. Hamano, "High-performance 10-Gbit/s optical receiver using avalanche photodiode and heterojunction bipolar transistor ICs," in *Optical Fiber Communication. OFC 97., Conference on*, 1997, pp. 16-17: IEEE.

[13] M. Lang *et al.*, "20-40 Gb/s 0.2µm GaAs HEMT chip set for optical data receiver," *IEEE Journal of Solid-State Circuits,* vol. 32, no. 9, pp. 1384-1393, 1997.

[14] K. Yang, A. L. Gutierrez-Aitken, X. Zhang, G. Haddad, and P. Bhattacharya, "Design, modeling, and characterization of monolithically integrated InP-based (1.55/spl mu/m) high-speed (24 Gb/s) pin/HBT front-end photoreceivers," *Journal of lightwave technology,* vol. 14, no. 8, pp. 1831-1839, 1996.

[15] D. Huber *et al.*, "InP-InGaAs single HBT technology for photoreceiver OEIC's at 40 Gb/s and beyond," *Journal of lightwave technology,* vol. 18, no. 7, p. 992, 2000.

[16] W. Kuebart *et al.*, "High sensitivity InP-based monolithically integrated pin-HEMT receiver-OEIC's for 10 Gb/s," *IEEE Transactions on Microwave Theory and Techniques,* vol. 43, no. 9, pp. 2334-2341, 1995.

[17] T. Nagatsuma, "Generating millimeter and terahertz waves," *IEEE Microwave Magazine,* vol. 10, no. 4, pp. 64-74, 2009.

[18] W.-T. W. Group, "521-2002 - IEEE Standard Letter Designations for Radar-Frequency Bands," 2009.

[19] A. ITU Radio Regulations. (2008) Volume 1. (2008). Available: http://life.itu.int/radioclub/rr/art02.htm

[20] T. T. A. Terahertz. Available: Available: http://spectrum.ieee.org/aerospace/military/the-truth-about-terahertz

[21] R. Letizia, M. Mineo, and C. Paoloni, "Photonic crystal-structures for THz vacuum electron devices," *IEEE Transactions on Electron Devices,* vol. 62, no. 1, pp. 178-183, 2015.

[22] B. Williams, S. Kumar, Q. Hu, and J. Reno, "Resonant-phonon terahertz quantum-cascade laser operating at 2.1 THz ($\lambda\sim$ 141 μm)," *Electronics Letters,* vol. 40, no. 7, pp. 431-433, 2004.

[23] H. Eisele, A. Rydberg, and G. I. Haddad, "Recent advances in the performance of InP Gunn devices and GaAs TUNNETT diodes for the 100-300-GHz frequency range and above," *IEEE Transactions on Microwave Theory and Techniques,* vol. 48, no. 4, pp. 626-631, 2000.

[24] K. Chang, W. F. Thrower, and G. M. Hayashibara, "Millimeter-wave silicon IMPATT sources and combiners for the 110-260-GHz range," *IEEE Transactions on Microwave Theory and Techniques,* vol. 29, no. 12, pp. 1278-1284, 1981.

[25] *http://terasense.com/products/sub-thz-imaging-cameras/,* TeraSense terahertz imaging.

[26] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John wiley & sons, 2006.

[27] K. S. J. Murphy *et al.*, "Millimetre wave aviation security scanner," in *Security Technology, 2002. Proceedings. 36th Annual 2002 International Carnahan Conference on*, 2002, pp. 162-166: IEEE.

[28] F. Xin, H. Su, and Y. Xiao, "Terahertz imaging system for remote sensing and security applications," in *Antennas and Propagation (APCAP), 2014 3rd Asia-Pacific Conference on*, 2014, pp. 1335-1338: IEEE.

[29] R. Appleby and R. N. Anderton, "Millimeter-wave and submillimeter-wave imaging for security and surveillance," *Proceedings of the IEEE,* vol. 95, no. 8, pp. 1683-1690, 2007.

[30] E. Pickwell and V. Wallace, "Biomedical applications of terahertz technology," *Journal of Physics D: Applied Physics,* vol. 39, no. 17, p. R301, 2006.

[31] I. McAuley *et al.*, "Millimetre-wave and terahertz imaging systems with medical applications," in *2006 Joint 31st International Conference on Infrared Millimeter Waves and 14th International Conference on Teraherz Electronics*, 2006, pp. 371-371: IEEE.

[32] D. Vavriv, "MM-wave meteoradars: development, design, and research data," in *Applied Electromagnetics and Communications, 2003. ICECom 2003. 17th International Conference on*, 2003, pp. 13-17: IEEE.

[33] J. Yang *et al.*, "The superconducting spectroscopic array receiver (SSAR) for millimeter-wave radio astronomy," in *Millimeter Waves, 2008. GSMM 2008. Global Symposium on*, 2008, pp. 177-179: IEEE.

[34] S. C. Reising *et al.*, "Microwave and millimeter-wave radiometers for CubeSat deployment for remote sensing of the earth's atmosphere," in *2014 39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, 2014, pp. 1-1: IEEE.

[35] T. Kleine-Ostmann and T. Nagatsuma, "A review on terahertz communications research," *Journal of Infrared, Millimeter, and Terahertz Waves,* vol. 32, no. 2, pp. 143-171, 2011.

[36] T. S. Rappaport *et al.*, "Millimeter wave mobile communications for 5G cellular: It will work!," *IEEE access,* vol. 1, pp. 335-349, 2013.

[37] N. Oshima, K. Hashimoto, D. Horikawa, S. Suzuki, and M. Asada, "Wireless data transmission of 30 Gbps at a 500-GHz range using resonant-tunneling-diode terahertz oscillator," in *Microwave Symposium (IMS), 2016 IEEE MTT-S International*, 2016, pp. 1-4: IEEE.

[38] E. R. Brown, C. D. Parker, K. M. Molvar, and K. D. Stephan, "A quasioptically stabilized resonant-tunneling-diode oscillator for the millimeter-and submillimeter-wave regions," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 40, no. 5, pp. 846-850, 1992.

[39] E. Brown, C. Parker, A. Calawa, M. Manfra, and K. Molvar, "A quasioptical resonant-tunneling-diode oscillator operating above 200 GHz," *IEEE Transaction on Microwave Theory and Techniques,* vol. 41, no. 4, pp. 720-722, 1993.

[40] A. Molnar *et al.*, "Submm-wave monolithic RTD oscillator arrays to 650 GHz," in *Electron Devices Meeting, 1996. IEDM'96., International*, 1996, pp. 940-942: IEEE.

[41] N. Orihashi, S. Suzuki, and M. Asada, "One THz harmonic oscillation of resonant tunneling diodes," *Applied physics letters,* vol. 87, no. 23, p. 233501, 2005.

[42] S. Suzuki and M. Asada, "Proposal of resonant tunneling diode oscillators with offset-fed slot antennas in terahertz and sub-terahertz range," *Japanese Journal of Applied Physics,* vol. 46, no. 1R, p. 119, 2007.

[43] M. Shiraishi, S. Suzuki, and M. Asada, "High-power operation of terahertz oscillators with resonant tunneling diodes using offset-fed slot antennas and array configuration," in *2012 37th International Conference on Infrared, Millimeter, and Terahertz Waves*, 2012.

[44] J. Wang, L. Wang, C. Li, B. Romeira, and E. Wasige, "28 GHz MMIC resonant tunnelling diode oscillator of around 1mW output power," *Electronics Letters,* vol. 49, no. 13, pp. 816-818, 2013.

[45] M. Asada and S. Suzuki, "Theoretical analysis of coupled oscillator array using resonant tunneling diodes in subterahertz and terahertz range," *Journal of Applied Physics,* vol. 103, no. 12, p. 124514, 2008.

[46] K. Kasagi, S. Suzuki, and M. Asada, "Array configuration using resonant-tunneling-diode terahertz oscillator integrated with patch antenna," in *Infrared, Millimeter, and Terahertz waves (IRMMW-THz), 2015 40th International Conference on*, 2015, pp. 1-2: IEEE.

[47] S. Suzuki and M. Asada, "Coherent power combination in highly integrated resonant tunneling diode oscillators with slot antennas," *Japanese Journal of Applied Physics,* vol. 46, no. 12L, p. L1108, 2007.

[48] S. Suzuki, N. Orihashi, and M. Asada, "Mutual injection locking between sub-THz oscillating resonant tunneling diodes," *Japanese journal of applied physics,* vol. 44, no. 11L, p. L1439, 2005.

[49] K. Kasagi, S. Fukuma, S. Suzuki, and M. Asada, "Proposal and fabrication of dipole array antenna structure in resonant-tunneling-diode terahertz oscillator array," in *Infrared, Millimeter, and Terahertz waves (IRMMW-THz), 2016 41st International Conference on*, 2016, pp. 1-2: IEEE.

[50] J. Lee, J. Lee, and K. Yang, "An On–Off Mode RTD Oscillator Operating at Extremely Low Power Consumption," *IEEE Transactions on Nanotechnology,* vol. 11, no. 5, pp. 863-865, 2012.

[51] T. Maekawa, H. Kanaya, S. Suzuki, and M. Asada, "Frequency increase in terahertz oscillation of resonant tunnelling diode up to 1.55 THz by reduced slot-antenna length," *Electronics Letters,* vol. 50, no. 17, pp. 1214-1216, 2014.

[52] S. Suzuki, K. Urayama, and M. Asada, "Coherent power combination in multi-element sub-terahertz resonant tunneling diode oscillators coupled with metal–insulator–metal stub structure," *Applied physics express,* vol. 1, no. 9, p. 093001, 2008.

[53] K. Urayama, S. Aoki, S. Suzuki, M. Asada, H. Sugiyama, and H. Yokoyama, "Sub-terahertz resonant tunneling diode oscillators integrated with tapered slot antennas for horizontal radiation," *Applied Physics Express,* vol. 2, no. 4, p. 044501, 2009.

[54] S. Suzuki, K. Hinata, M. Shiraishi, M. Asada, H. Sugiyama, and H. Yokoyama, "RTD oscillators at 430–460 GHz with high output power (~ 200 μW) using integrated offset slot antennas," in *Indium Phosphide & Related Materials (IPRM), 2010 International Conference on*, 2010, pp. 1-4: IEEE.

[55] M. Shiraishi *et al.*, "High output power (~ 400 μW) oscillators at around 550 GHz using large area RTD and optimized antenna structure," in *Compound Semiconductor Week (CSW/IPRM), 2011 and 23rd International Conference on Indium Phosphide and Related Materials*, 2011, pp. 1-4: IEEE.

[56] Y. Ikeda, S. Kitagawa, K. Okada, S. Suzuki, and M. Asada, "Direct intensity modulation of resonant-tunneling-diode terahertz oscillator up to~ 30 GHz," *IEICE Electronics Express,* vol. 12, no. 3, pp. 20141161-20141161, 2015.

[57] K. Ishigaki, K. Karashima, M. Shiraishi, H. Shibayama, S. Suzuki, and M. Asada, "Direct modulation of THz-oscillating resonant tunneling diodes," in *2011 International Conference on Infrared, Millimeter, and Terahertz Waves*, 2011.

[58] K. Ishigaki, M. Shiraishi, S. Suzuki, M. Asada, N. Nishiyama, and S. Arai, "Direct intensity modulation and wireless data transmission characteristics of terahertz-oscillating resonant tunnelling diodes," *Electronics letters,* vol. 48, no. 10, pp. 582-583, 2012.

[59] M. F. Tadao Nagatsima, Ai Kaku, Daiki Tsuji and Shunsuke Nakai, "Terahertz Wireless Communications Using Resonant Tunneling Diodes as Transmitters and Receivers," *Proceeding ICTRS,* pp. 41-46, 2014.

[60] M. K. J. Lee, and K. Yang,, "An InP-based RTD triple-push oscillator operating at over 1 THz," *in IEEE Int. Conf. Indium Phosphide Related Mat,* 2015.

[61] J. Lee, M. Kim, and K. Yang, "A 1.52 THz RTD Triple-Push Oscillator With a-Level Output Power," *IEEE Transactions on Terahertz Science and Technology,* vol. 6, no. 2, pp. 336-340, 2016.

[62] M. Kim, J. Lee, J. Lee, and K. Yang, "A 675 GHz Differential Oscillator Based on a Resonant Tunneling Diode," *IEEE Transactions on Terahertz Science and Technology,* vol. 6, no. 3, pp. 510-512, 2016.

[63] T. Mukai, M. Kawamura, T. Takada, and T. Nagatsuma, "1.5-Gbps wireless transmission using resonant tunneling diodes at 300 GHz," in *Tech. Dig. Optical Terahertz Science and Technology 2011 Meeting*, 2011.

[64] T. Shiode, T. Mukai, M. Kawamura, and T. Nagatsuma, "Giga-bit wireless communication at 300 GHz using resonant tunneling diode detector," in *Asia-Pacific Microwave Conference (APMC 2011): 25 Years, The*, 2011, p. 1122: Engineers Australia.

[65] T. J. Chung and W.-H. Lee, "10-Gbit/s Wireless Communication System at 300 GHz," *ETRI Journal,* vol. 35, no. 3, pp. 386-396, 2013.

[66] K. Minoguchi, K. Okada, S. Suzuki, and M. Asada, "Proposal and fabrication of resonant-tunneling-diode terahertz oscillator with structure for high frequency modulation," in *Infrared, Millimeter, and Terahertz Waves (IRMMW-THz), 2013 38th International Conference on*, 2013, pp. 1-2: IEEE.

[67] N. Oshima, K. Hashimoto, S. Suzuki, and M. Asada, "Wireless data transmission of 34 Gbit/s at a 500-GHz range using resonant-tunnelling-diode terahertz oscillator," *Electronics Letters,* vol. 52, no. 22, pp. 1897-1898, 2016.

[68] S. Diebold *et al.*, "Modeling and Simulation of Terahertz Resonant Tunneling Diode-Based Circuits," *IEEE Transactions on Terahertz Science and Technology,* vol. 6, September 2016.

[69] K. Maezawa, J. Pan, D. Wu, Y. Kakutani, J. Nakano, and M. Mori, "Possibility of THz detection with resonant tunneling super regenerative detectors based on extremely high order harmonics," *IEICE Electronics Express,* vol. 10, no. 20, pp. 20130676-20130676, 2013.

[70] G. Keller, A. Tchegho, B. Munstermann, W. Prost, F.-J. Tegude, and M. Suhara, "Triple barrier resonant tunneling diodes for microwave signal generation and detection," in *2013 European Microwave Integrated Circuit Conference*, 2013.

[71] K. Z. Ariffin, S. Muttlak, M. Abdullah, R. Abdullah, Y. Wang, and M. Missous, "Asymmetric Spacer Layer Tunnel In0. 18Ga0. 82As/AlAs (ASPAT) Diode using double quantum wells for dual functions: Detection and oscillation," in *Millimeter Waves and THz Technology Workshop (UCMMT), 2015 8th UK, Europe, China*, 2015, pp. 1-4: IEEE.

[72] A. Cidronali *et al.*, "MMIC applications of heterostructure interband tunnel devices," *IEEE transactions on microwave theory and techniques,* vol. 51, no. 4, pp. 1351-1367, 2003.

[73] K. Maezawa, T. Sakamoto, K. Kasahara, and M. Mori, "Possibility of terahertz amplification by active transmission lines loaded with resonant tunneling diode pairs," *Japanese Journal of Applied Physics,* vol. 48, no. 12R, p. 124503, 2009.

[74] J. Lee, J. Lee, J. Park, and K. Yang, "5 GHz low-power RTD-based amplifier MMIC with a high figure-of-merit of 24.5 dB/mW," in *Indium Phosphide and Related Materials (IPRM), 2013 International Conference on*, 2013, pp. 1-2: IEEE.

[75] J. Mata-Contreras, T. Martin-Guerrero, and C. Camacho-Peñalosa, "Active composite right/left-handed transmission line-based mixers," in *MELECON 2006-2006 IEEE Mediterranean Electrotechnical Conference*, 2006, pp. 276-279: IEEE.

[76] S. Muttlak, O. Abdulwahid, J. Sexton, and M. Missous, "Modeling of high gain and μW level power consumption resonant tunneling diode based amplifiers," in *Millimetre Waves and Terahertz Technologies (UCMMT), 2017 10th UK-Europe-China Workshop on*, 2017, pp. 1-4: IEEE.

[77] I. J. Bahl and P. Bhartia, *Microwave solid state circuit design*. John Wiley & Sons, 2003.

[78] J. Gao, *Optoelectronic integrated circuit design and device modeling*. John Wiley & Sons, 2011.

[79] R. Ramaswami, K. Sivarajan, and G. Sasaki, *Optical networks: a practical perspective*. Morgan Kaufmann, 2009.

[80] K. Tanaka, A. Agata, and Y. Horiuchi, "IEEE 802.3 av 10G-EPON standardization and its research and development status," *Journal of Lightwave Technology*, vol. 28, no. 4, pp. 651-661, 2010.

[81] C.-H. Lee, W. V. Sorin, and B. Y. Kim, "Fiber to the home using a PON infrastructure," *Journal of lightwave technology*, vol. 24, no. 12, pp. 4568-4583, 2006.

[82] H. T. J. Meier, "Design, characterization and simulation of avalanche photodiodes," ETH Zurich, 2011.

[83] P. Angelini *et al.*, "Record− 22.5-dBm Sensitivity SOA-PIN-TIA Photoreceiver Module for 40-Gb/s Applications," *IEEE Photonics Technology Letters*, vol. 27, no. 19, pp. 2027-2030, 2015.

[84] R. D. Bespalko, "Transimpedance amplifier design using 0.18 um CMOS technology," 2007.

[85] I.-T. R. G.989.1, "40-Gigabit-capable passive optical networks (NG-PON2): General requirements," *SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS*, 2013.

[86] H. Lin, D. Liu, Y. Luo, F. Effenberger, and N. Cheng, "TWDM-PON: System, Standards, and Key Technologies," in *Asia Communications and Photonics Conference*, 2014, p. ATh2F. 1: Optical Society of America.

[87] K. W. Kobayashi, "State-of-the-art 60 GHz, 3.6 k-Ohm transimpedance amplifier for 40 Gb/s and beyond," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE*, 2003, pp. 55-58: IEEE.

[88] S. M. Sze, "High-speed semiconductor devices," *New York, Wiley-Interscience, 1990*.

[89] J. M. L. Figueiredo, "Optoelectronic Properties of Resonant tunnelling Diode," PhD Thesis, University of Glasgow, 2000.

[90] T. P. Broekaert and C. G. Fonstad, "In0. 53Ga0. 47As/AlAs resonant tunneling diodes with peak current densities in excess of 450 kA/cm2," *Journal of applied physics*, vol. 68, no. 8, pp. 4310-4312, 1990.

[91] M. Tsuchiya and H. Sakaki, "Dependence of resonant tunneling current on well widths in AlAs/GaAs/AlAs double barrier diode structures," *Applied physics letters*, vol. 49, no. 2, pp. 88-90, 1986.

[92] M. Zawawi, "Advanced In0.8Ga0.2As/AlAs resonant tunneling diodes for applications in integrated mm-waves MMIC oscillators," University of Manchester, 2015.

[93] H. Mizuta and T. Tanoue, *The physics and applications of resonant tunnelling diodes*. Cambridge university press, 2006.

[94] L. L. Chang, L. Esaki, and R. Tsu, "Resonant tunneling in semiconductor double barriers," *Applied physics letters*, vol. 24, no. 12, pp. 593-595, 1974.

[95] Y. Hu and S. Stapleton, "Capacitance of a resonant tunneling diode," *Japanese Journal of Applied Physics,* vol. 31, no. 1R, p. 23, 1992.

[96] D. Neculoiu, I. Sztojanov, and T. Tebeanu, "An investigation of the IV relationship of double barrier resonant tunneling diodes in oscillating conditions," in *Semiconductor Conference, 1997. CAS'97 Proceedings., 1997 International*, 1997, vol. 2, pp. 345-348: IEEE.

[97] K. Araki, "Analysis of barrier transmission in resonant tunneling diodes," *Journal of applied physics,* vol. 62, no. 3, pp. 1059-1069, 1987.

[98] P. Roblin and H. Rohdin, *High-speed heterostructure devices: from device concepts to circuit modeling*. Cambridge university press, 2002.

[99] E. Koenig, C. Huang, and B. Jogai, "Independence of peak current from emitter spacer layer width in AlGaAs/GaAs resonant tunneling diodes," *Journal of applied physics,* vol. 68, no. 11, pp. 5905-5907, 1990.

[100] J. H. Smet, T. P. Broekaert, and C. G. Fonstad, "Peak-to-valley current ratios as high as 50: 1 at room temperature in pseudomorphic In0. 53Ga0. 47As/AlAs/InAs resonant tunneling diodes," *Journal of applied physics,* vol. 71, no. 5, pp. 2475-2477, 1992.

[101] T. Inata, S. Muto, Y. Nakata, T. Fujii, H. Ohnishi, and S. Hiyamizu, "Excellent negative differential resistance of InAlAs/InGaAs resonant tunneling barrier structures grown by MBE," *Japanese journal of applied physics,* vol. 25, no. 12A, p. L983, 1986.

[102] J. C. Bean, *Materials and Technologies" in High-Speed Semiconductor Devices*. New York: John Wiley & Sons, 1990.

[103] K. Ismail, B. Meyerson, and P. Wang, "Electron resonant tunneling in Si/SiGe double barrier diodes," *Applied physics letters,* vol. 59, no. 8, pp. 973-975, 1991.

[104] S.-Y. Park *et al.*, "Si/SiGe Resonant Interband Tunneling Diodes Incorporating $\delta $-Doping Layers Grown by Chemical Vapor Deposition," *IEEE Electron Device Letters,* vol. 30, no. 11, pp. 1173-1175, 2009.

[105] S.-Y. Chung, R. Yu, N. Jin, S.-Y. Park, P. R. Berger, and P. E. Thompson, "Si/SiGe resonant interband tunnel diode with f/sub r0/20.2 GHz and peak current density 218 kA/cm/sup 2/for K-band mixed-signal applications," *IEEE electron device letters,* vol. 27, no. 5, pp. 364-367, 2006.

[106] T. Shewchuk, P. Chapin, P. Coleman, W. Kopp, R. Fischer, and H. Morkoc, "Resonant tunneling oscillations in a GaAs-AlxGa1− xAs heterostructure at room temperature," *Applied Physics Letters,* vol. 46, no. 5, pp. 508-510, 1985.

[107] M. Tsuchiya, H. Sakaki, and J. Yoshino, "Room temperature observation of differential negative resistance in an AlAs/GaAs/AlAs resonant tunneling diode," *Japanese Journal of Applied Physics,* vol. 24, no. 6A, p. L466, 1985.

[108] E. Wolak, E. Özbay, B. Park, S. Diamond, D. M. Bloom, and J. S. Harris Jr, "The design of GaAs/AlAs resonant tunneling diodes with peak current densities over 2× 105 A cm− 2," *Journal of applied physics,* vol. 69, no. 5, pp. 3345-3350, 1991.

[109] A. Forster, J. Lange, D. Gerthsen, C. Dieker, and H. Luth, "The effect of growth temperature on AlAs/GaAs resonant tunnelling diodes," *Journal of Physics D: Applied Physics,* vol. 27, no. 1, p. 175, 1994.

[110] M. A. M. Zawawi and M. Missous, "Design and fabrication of low power GaAs/AlAs resonant tunneling diodes," *Solid-State Electronics,* vol. 138, pp. 30-34, 2017.

[111] T. Inata, S. Muto, Y. Nakata, S. Sasa, T. Fujii, and S. Hiyamizu, "A pseudomorphic In0. 53Ga0. 47As/AlAs resonant tunneling barrier with a peak-to-valley current ratio of 14 at room temperature," *Japanese Journal of Applied Physics,* vol. 26, no. 8A, p. L1332, 1987.

[112] E. R. Brown *et al.*, "High-speed resonant-tunneling diodes made from the In0. 53Ga0. 47As/AlAs material system," in *High-Speed Electronics and Device Scaling*, 1990, vol. 1288, pp. 122-136: International Society for Optics and Photonics.

[113] N. Shimizu, T. Nagatsuma, T. Waho, M. Shinagawa, M. Yaita, and M. Yamamoto, "In0. 53Ga0. 47As/AlAs resonant tunnelling diodes with switching time of 1.5 ps," *Electronics Letters,* vol. 31, no. 19, pp. 1695-1697, 1995.

[114] T. P. Broekaert, W. Lee, and C. G. Fonstad, "Pseudomorphic In0. 53Ga0. 47As/AlAs/InAs resonant tunneling diodes with peak-to-valley current ratios of 30 at room temperature," *Applied physics letters,* vol. 53, no. 16, pp. 1545-1547, 1988.

[115] T. Broekaert and C. Fonstad, "Extremely high current density, low peak voltage, pseudomorphic In/sub 0.53/Ga/sub 0.47/As/AlAs/InAs resonant tunneling diodes," in *Electron Devices Meeting, 1989. IEDM'89. Technical Digest., International*, 1989, pp. 559-562: IEEE.

[116] D. Pawlik *et al.*, "Benchmarking and improving III-V Esaki diode performance with a record 2.2 MA/cm 2 peak current density to enhance TFET drive current," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 27.1. 1-27.1. 3: IEEE.

[117] W. Prost *et al.*, "High performance III/V RTD and PIN diode on a silicon (001) substrate," *Applied Physics A,* vol. 87, no. 3, pp. 539-544, 2007.

[118] A. Freundlich, M. Vilela, A. Bensaoula, and N. Medelci, "Very high peak current CBE grown InGaAs tunnel junction for InP/InGaAs tandem cells fabricated on InP, GaAs, and Si substrates," in *Photovoltaic Specialists Conference, 1993., Conference Record of the Twenty Third IEEE*, 1993, pp. 644-649: IEEE.

[119] P. Thomas *et al.*, "Performance evaluation of In 0.53 Ga 0.47 As Esaki tunnel diodes on silicon and InP substrates," *IEEE Transactions on Electron Devices,* vol. 62, no. 8, pp. 2450-2456, 2015.

[120] K. Majumdar *et al.*, "Mapping Defect Density in MBE Grown In0.53Ga0.47As Epitaxial Layers on Si Substrate Using Esaki Diode Valley Characteristics," *IEEE Transactions on Electron Devices,* vol. 61, no. 6, pp. 2049-2055, 2014.

[121] E. Brown, J. Söderström, C. Parker, L. Mahoney, K. Molvar, and T. McGill, "Oscillations up to 712 GHz in InAs/AlSb resonant-tunneling diodes," *Applied Physics Letters,* vol. 58, no. 20, pp. 2291-2293, 1991.

[122] J. Söderström *et al.*, "Growth and characterization of high current density, high-speed InAs/AlSb resonant tunneling diodes," *Applied physics letters,* vol. 58, no. 3, pp. 275-277, 1991.

[123] J. Söderström, E. Yu, M. Jackson, Y. Rajakarunanayake, and T. McGill, "Two-band modeling of narrow band gap and interband tunneling devices," *Journal of Applied Physics,* vol. 68, no. 3, pp. 1372-1375, 1990.

[124] E. Brown, T. Sollner, C. Parker, W. Goodhue, and C. Chen, "Oscillations up to 420 GHz in GaAs/AlAs resonant tunneling diodes," *Applied physics letters,* vol. 55, no. 17, pp. 1777-1779, 1989.

[125] X. Shi *et al.*, "Enhancing power density of strained In0. 8Ga0. 2As/AlAs resonant tunneling diode for terahertz radiation by optimizing emitter spacer layer thickness," *Superlattices and Microstructures,* vol. 112, pp. 435-441, 2017.

[126] J. O. H. Matsuzaki, H. Sugiyama, T. Kobayashi, and T. Enoki, *Inst. Phys. Conf. Ser.,* vol. 170,, pp. 63,, 2002.

[127] H. Sugiyama, H. Matsuzaki, Y. Oda, H. Yokoyama, T. Enoki, and T. Kobayashi, "Metal-organic vapor-phase epitaxy growth of InP-based resonant tunneling diodes with a strained In0. 8Ga0. 2As well and AlAs barriers," *Japanese Journal of Applied Physics,* vol. 44, no. 10R, p. 7314, 2005.

[128] H. Kanaya, S. Suzuki, and M. Asada, "Terahertz oscillation of resonant tunneling diodes with deep and thin quantum wells," *IEICE Electronics Express,* vol. 10, no. 18, pp. 20130501-20130501, 2013.

[129] H. Sugiyama, H. Matsuzaki, Y. Oda, H. Yokoyama, T. Enoki, and T. Kobayashi, "InP-based strained In 0.8 Ga 0.2 As/AlAs resonant tunneling diodes with high peak-current density and large peak-to-valley current ratio grown by metal-organic vapor-phase epitaxy," in *Indium Phosphide and Related Materials, 2003. International Conference on*, 2003, pp. 211-214: IEEE.

[130] A. Teranishi, S. Suzuki, H. Sugiyama, H. Yokoyama, and M. Asada, "Resonant tunneling diodes with very high peak current density using thin barrier and high emitter doping," in *Device Research Conference, 2008*, 2008, pp. 265-266: IEEE.

[131] S. Suzuki, M. Asada, A. Teranishi, H. Sugiyama, and H. Yokoyama, "Fundamental oscillation of resonant tunneling diodes above 1 THz at room temperature," *Applied physics letters,* vol. 97, no. 24, p. 242102, 2010.

[132] A. Teranishi, K. Shizuno, S. Suzuki, M. Asada, H. Sugiyama, and H. Yokoyama, "Fundamental oscillation up to 1.08 THz in resonant tunneling diodes with high-indium-composition transit layers for reduction of transit delay," *IEICE Electronics Express,* vol. 9, no. 5, pp. 385-390, 2012.

[133] H. Kanaya, H. Shibayama, R. Sogabe, S. Suzuki, and M. Asada, "Fundamental oscillation up to 1.31 THz in resonant tunneling diodes with thin well and barriers," *Applied Physics Express,* vol. 5, no. 12, p. 124101, 2012.

[134] H. Kanaya, R. Sogabe, T. Maekawa, S. Suzuki, and M. Asada, "Frequency increase in resonant-tunneling-diode terahertz oscillators using optimum collector spacer," in *Indium Phosphide and Related Materials (IPRM), 26th International Conference on*, 2014, pp. 1-2: IEEE.

[135] T. Maekawa, H. Kanaya, S. Suzuki, and M. Asada, "Oscillation up to 1.92 THz in resonant tunneling diode by reduced conduction loss," *Applied physics express,* vol. 9, no. 2, p. 024101, 2016.

[136] D. Li *et al.*, "Repeatable low-temperature negative-differential resistance from Al0. 18Ga0. 82N/GaN resonant tunneling diodes grown by molecular-beam epitaxy on free-standing GaN substrates," *Applied physics letters,* vol. 100, no. 25, p. 252105, 2012.

[137] M. Nagase, T. Takahashi, and M. Shimizu, "Resistance switching memory operation using the bistability in current–voltage characteristics of GaN/AlN resonant tunneling diodes," *Japanese Journal of Applied Physics,* vol. 55, no. 10, p. 100301, 2016.

[138] Z. Vashaei, C. Bayram, R. McClintock, and M. Razeghi, "Effects of substrate quality and orientation on the characteristics of III-nitride resonant tunneling diodes," in *SPIE OPTO*, 2011, pp. 79451A-79451A-10: International Society for Optics and Photonics.

[139] L. a. Yang, H. He, W. Mao, and Y. Hao, "Quantitative analysis of the trapping effect on terahertz AlGaN/GaN resonant tunneling diode," *Applied physics letters,* vol. 99, no. 15, p. 153501, 2011.

[140] L. a. Yang, Y. Li, Y. Wang, S. Xu, and Y. Hao, "Asymmetric quantum-well structures for AlGaN/GaN/AlGaN resonant tunneling diodes," *Journal of applied physics,* vol. 119, no. 16, p. 164501, 2016.

[141] A. M. El-Gabaly, D. Stewart, and C. E. Saavedra, "2-W Broadband GaN Power-Amplifier RFIC Using the $ f_ {T} $ Doubling Technique and Digitally Assisted Distortion Cancellation," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 1, pp. 525-532, 2013.

[142] S. Lee, H. Park, K. Choi, and Y. Kwon, "A broadband GaN pHEMT power amplifier using non-Foster matching," *IEEE Transactions on Microwave Theory and Techniques,* vol. 63, no. 12, pp. 4406-4414, 2015.

[143] S. P. Marsh, *Practical MMIC design*. Artech House, 2006.

[144] W. Zhang, E. Brown, T. Growden, P. Berger, and R. Droopad, "A Nonlinear Circuit Simulation of Switching Process in Resonant-Tunneling Diodes," *IEEE Transactions on Electron Devices,* vol. 63, no. 12, pp. 4993-4997, 2016.

[145] M. A. M. Zawawi, K. W. Ian, J. Sexton, and M. Missous, "Fabrication of Submicrometer InGaAs/AlAs Resonant Tunneling Diode Using a Trilayer Soft Reflow Technique With Excellent Scalability," *IEEE Transactions on Electron Devices,* vol. 61, no. 7, pp. 2338-2342, 2014.

[146] K. Jacobs, B. Stevens, O. Wada, T. Mukai, D. Ohnishi, and R. Hogg, "A Dual-Pass High Current Density Resonant Tunneling Diode for Terahertz Wave Applications," *IEEE Electron Device Letters,* vol. 36, no. 12, pp. 1295-1298, 2015.

[147] T. Ren, Y. Zhang, R. Xu, J. Zhou, C. Yang, and Z. Jin, "A 340-400 GHz Zero-Biased Waveguide Detector Using an Self-Consistent Method to Extract the Parameters of Schottky Barrier Diode," *Applied Computational Electromagnetics Society Journal,* vol. 30, no. 12, 2015.

[148] T. Daniels-Race and S. Yu, "Effect of spacer layer thickness on tunneling characteristics in asymmetric AlAs/GaAs/AlAs double barrier structures," *Solid-state electronics,* vol. 38, no. 7, pp. 1347-1349, 1995.

[149] Y. Zhang, C. Han, J. Gao, Z. Zhu, B. Wang, and Y. Zeng, "Influence of spacer layer thickness on the current-voltage characteristics of pseudomorphic AlAs/In0. 53Ga0. 47As/InAs resonant tunnelling diodes," 2008.

[150] H. Kanaya, R. Sogabe, T. Maekawa, S. Suzuki, and M. Asada, "Fundamental oscillation up to 1.42 THz in resonant tunneling diodes by optimized collector spacer thickness," *Journal of Infrared, Millimeter, and Terahertz Waves,* vol. 35, no. 5, pp. 425-431, 2014.

[151] J. Genoe *et al.*, "Capacitances in double-barrier tunneling structures," *IEEE Transactions on Electron Devices,* vol. 38, no. 9, pp. 2006-2012, 1991.

[152] J. Lee, J. Lee, and K. Yang, "Reflection-type RTD low-power amplifier with deep sub-mW DC power consumption," *IEEE Microwave and Wireless Components Letters,* vol. 24, no. 8, pp. 551-553, 2014.

[153] A. Tsao, V. Reddy, D. Miller, K. Gullapalli, and D. Neikirk, "Effect of barrier thickness asymmetries on the electrical characteristics of AlAs/GaAs double barrier resonant tunneling diodes," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* vol. 10, no. 2, pp. 1042-1044, 1992.

[154] G. Ternent and D. J. Paul, "SPICE modeling of the scaling of resonant tunneling diodes and the effects of sidewall leakage," *IEEE Transactions on Electron Devices,* vol. 59, no. 12, pp. 3555-3560, 2012.

[155] K. Nomoto, K. Taira, T. Suzuki, I. Hase, H. Hiroshima, and M. Komuro, "Diameter dependence of current–voltage characteristics of ultrasmall area AlSb–InAs resonant tunneling diodes with diameters down to 20 nm," *Applied physics letters,* vol. 70, no. 15, pp. 2025-2027, 1997.

[156] S. Khaledian, F. Farzami, D. Erricolo, and B. Smida, "A full-duplex bidirectional amplifier with low DC power consumption using tunnel diodes," *IEEE Microwave and Wireless Components Letters,* vol. 27, no. 12, pp. 1125-1127, 2017.

[157] P. Fay, J. Lu, Y. Xu, N. Dame, D. H. Chow, and J. N. Schulman, "Microwave performance and modeling of InAs/AlSb/GaSb resonant interband tunneling diodes," *IEEE Transactions on Electron Devices,* vol. 49, no. 1, pp. 19-24, 2002.

[158] Y. Koyama, R. Sekiguchi, and T. Ouchi, "Oscillations up to 1.40 THz from Resonant-Tunneling-Diode-Based Oscillators with Integrated Patch Antennas," *Applied physics express,* vol. 6, no. 6, pp. 064102-064102-3, 2013.

[159] A. Piotrowska, A. Guivarc'h, and G. Pelous, "Ohmic contacts to III–V compound semiconductors: a review of fabrication techniques," *Solid-State Electronics,* vol. 26, no. 3, pp. 179-197, 1983.

[160] H. Berger, "Models for contacts to planar devices," *Solid-State Electronics,* vol. 15, no. 2, pp. 145-158, 1972.

[161] G. Reeves and H. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Electron device letters,* vol. 3, no. 5, pp. 111-113, 1982.

[162] L. B. Valdes, "Resistivity measurements on germanium for transistors," *Proceedings of the IRE,* vol. 42, no. 2, pp. 420-427, 1954.

[163] R. Hall, "Minimizing errors of four point probe measurements on circular wafers," *Journal of Scientific Instruments,* vol. 44, no. 1, p. 53, 1967.

[164] A. Baraskar *et al.*, "Ex situ Ohmic contacts to n-InGaAs," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena,* vol. 28, no. 4, pp. C5I7-C5I9, 2010.

[165] A. K. Baraskar *et al.*, "Ultralow resistance, nonalloyed Ohmic contacts to n-In Ga As," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* vol. 27, no. 4, pp. 2036-2039, 2009.

[166] M. Koolen, J. Geelen, and M. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Bipolar Circuits and Technology Meeting, 1991., Proceedings of the 1991*, 1991, pp. 188-191: IEEE.

[167] H. Cho and D. E. Burk, "A three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Transactions on Electron Devices*, vol. 38, no. 6, pp. 1371-1375, 1991.

[168] T. Wei, S. Stapleton, and O. Berolo, "Scattering parameter measurements of resonant tunneling diodes up to 40 GHz," *IEEE Transactions on Electron Devices*, vol. 42, no. 7, pp. 1378-1380, 1995.

[169] G. Antonini, "SPICE equivalent circuits of frequency-domain responses," *IEEE Transactions on Electromagnetic Compatibility*, vol. 45, no. 3, pp. 502-512, 2003.

[170] S. F. Nafea and A. A. Dessouki, "An accurate large-signal SPICE model for Resonant Tunneling Diode," in *2010 International Conference on Microelectronics*, 2010, pp. 507-510: IEEE.

[171] K. Fobelets, R. Vounckx, J. Genoe, G. Borghs, H. Grönqvist, and L. Lundgren, "High-frequency capacitances in resonant interband tunneling diodes," *Applied physics letters*, vol. 64, no. 19, pp. 2523-2525, 1994.

[172] R. Miles, G. Millington, R. Pollard, D. Steenson, J. Chamberlain, and M. Henini, "Accurate equivalent circuit model of resonant tunnelling diodes," *Electronics Letters*, vol. 27, no. 5, pp. 427-428, 1991.

[173] A. Y. Tang and J. Stake, "Impact of eddy currents and crowding effects on high-frequency losses in planar Schottky diodes," *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3260-3269, 2011.

[174] Q. Liu, A. Seabaugh, P. Chahal, and F. J. Morris, "Unified AC model for the resonant tunneling diode," *IEEE Transactions on Electron Devices*, vol. 51, no. 5, pp. 653-657, 2004.

[175] R. Lake and J. Yang, "A physics based model for the RTD quantum capacitance," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 785-789, 2003.

[176] J. Bruston *et al.*, "Development of 200-GHz to 2.7-THz multiplier chains for submillimeter-wave heterodyne receivers," in *UV, Optical, and IR Space Telescopes and Instruments*, 2000, vol. 4013, pp. 285-296: International Society for Optics and Photonics.

[177] U. V. Bhapkar and T. W. Crowe, "Analysis of the high frequency series impedance of GaAs Schottky diodes by a finite difference technique," *IEEE transactions on microwave theory and techniques*, vol. 40, no. 5, pp. 886-894, 1992.

[178] L. E. Dickens, "Spreading resistance as a function of frequency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 15, no. 2, pp. 101-109, 1967.

[179] E. Brown, "High-speed resonant-tunneling diodes," in *VLSI Electronics Microstructure Science*, vol. 24: Elsevier, 1994, pp. 305-350.

[180] A. Matiss, A. Poloczek, W. Brockerhoff, W. Prost, and F.-J. Tegude, "Large-signal analysis and AC modelling of sub micron resonant tunnelling diodes," in *Microwave Integrated Circuit Conference, 2007. EuMIC 2007. European*, 2007, pp. 207-210: IEEE.

[181] F. Trofimenkoff and O. Nakahara, "Collector depletion region transit time," *Proceedings of the IEEE*, vol. 52, no. 1, pp. 86-87, 1964.

[182] N. Orihashi, S. Hattori, S. Suzuki, and M. Asada, "Experimental and theoretical characteristics of sub-terahertz and terahertz oscillations of resonant tunneling diodes integrated with slot antennas," *Japanese Journal of Applied Physics,* vol. 44, no. 11R, p. 7809, 2005.

[183] C. Kim and A. Brandli, "High-frequency high-power operation of tunnel diodes," *IRE Transactions on Circuit Theory,* vol. 8, no. 4, pp. 416-425, 1961.

[184] H.-J. Song and T. Nagatsuma, *Handbook of Terahertz Technologies: Devices and Applications*. CRC Press, 2015.

[185] I. D. Robertson and S. Lucyszyn, *RFIC and MMIC Design and Technology* (no. 13). Iet, 2001.

[186] N. B. Ahmad, "Modelling and design of Low Noise Amplifiers using strained InGaAs/InAlAs/InP pHEMT for the Square Kilometre Array (SKA) application," 2012.

[187] A. Technologies, "Theory of operation for momentum," *ADS 2011 Help.,* 2011.

[188] G. M. Rebeiz, "Millimeter-wave and terahertz integrated circuit antennas," *Proceedings of the IEEE,* vol. 80, no. 11, pp. 1748-1770, 1992.

[189] S. Vinayak, H. Vyas, K. Muraleedharan, and V. Vankar, "Ni–Cr thin film resistor fabrication for GaAs monolithic microwave integrated circuits," *Thin Solid Films,* vol. 514, no. 1-2, pp. 52-57, 2006.

[190] R. Driad, M. Krieg, N. Geldmacher, J. Rüster, and F. Benkhelifa, "Investigation of NiCr Thin Film Resistors for InP-Based Monolithic Microwave Integrated Circuits (MMICs)," *Journal of The Electrochemical Society,* vol. 158, no. 5, pp. H561-H564, 2011.

[191] R. Sharma, S. Vinayak, D. Rawal, A. Kumar, and U. Ray, "RF parameter extraction of MMIC nichrome resistors," *Microwave and Optical Technology Letters,* vol. 39, no. 5, pp. 409-412, 2003.

[192] S. Arshad, "Low-Power Wideband InP-Based Low Noise Amplifiers for the Square Kilometre Array Radio Telescope," PhD Theses, University of Manchester, 2009.

[193] L. Wang, R.-M. Xu, and B. Yan, "MIM capacitor simple scalable model determination for MMIC application on GaAs," *Progress In Electromagnetics Research,* vol. 66, pp. 173-178, 2006.

[194] D. M. Pozar, "Microwave Engineering 3e," *Tramsmission Lines and Waveguides,* pp. 143-149, 2005.

[195] G. Haobijam and R. P. Palathinkal, *Design and analysis of spiral inductors*. Springer, 2014.

[196] T. O. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30-100-GHz inductors and transformers for millimeter-wave (Bi) CMOS integrated circuits," *IEEE transactions on microwave theory and techniques,* vol. 53, no. 1, pp. 123-133, 2005.

[197] N. P. Aryan, *Design and Modeling of Inductors, Capacitors and Coplanar Waveguides at Tens of GHz Frequencies*. Springer, 2014.

[198] P. Shepherd, "Analysis of Square-Spiral Inductors for Use in MMIC's (Short Paper)," *IEEE transactions on microwave theory and techniques,* vol. 34, no. 4, pp. 467-472, 1986.

[199] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of solid-state circuits,* vol. 34, no. 10, pp. 1419-1424, 1999.

[200] S. Arshad, "Low-Power Wideband InP-Based Low Noise Amplifiers for the Square Kilometre Array Radio Telescope," The University of Manchester, 2009.

[201] Y. Cao *et al.*, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *IEEE Journal of solid-state circuits,* vol. 38, no. 3, pp. 419-426, 2003.

[202] C. P. Wen, "Coplanar waveguide: A surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 17, no. 12, pp. 1087-1090, 1969.

[203] R. N. Simons, *Coplanar waveguide circuits, components, and systems*. John Wiley & Sons, 2004.

[204] G. Ghione and C. U. Naldi, "Coplanar waveguides for MMIC applications: Effect of upper shielding, conductor backing, finite-extent ground planes, and line-to-line coupling," *IEEE transactions on Microwave Theory and Techniques,* vol. 35, no. 3, pp. 260-267, 1987.

[205] P. Bhartia and P. Pramanick, "A New Microstrip Dispersion Model (Short Papers)," *IEEE Transactions on Microwave Theory and Techniques,* vol. 32, no. 10, pp. 1379-1384, 1984.

[206] A. Gopinath, "Losses in coplanar waveguides," *IEEE Transactions on Microwave Theory and Techniques,* vol. 7, no. 30, pp. 1101-1104, 1982.

[207] M. Y. Frankel, S. Gupta, J. A. Valdmanis, and G. A. Mourou, "Terahertz attenuation and dispersion characteristics of coplanar transmission lines," *IEEE Transactions on Microwave Theory and Techniques,* vol. 39, no. 6, pp. 910-916, 1991.

[208] U. L. Rohde and M. Rudolph, *RF/microwave circuit design for wireless applications*. John Wiley & Sons, 2013.

[209] R. E. Collin, *Foundations for microwave engineering*. John Wiley & Sons, 2007.

[210] G. Hasnain, J. Whinnery, and A. Dienes, "Dispersion of picosecond pulses in coplanar transmission lines," *IEEE Transactions on Microwave Theory Techniques,* vol. 34, pp. 738-741, 1986.

[211] S. Diebold *et al.*, "Modeling and Simulation of Terahertz Resonant Tunneling Diode-Based Circuits," *IEEE TRANSACTIONS ON TERAHERTZ SCIENCE AND TECHNOLOGY,* vol. 6, SEPTEMBER 2016.

[212] S. Diebold *et al.*, "A fully-scalable coplanar waveguide passive library for millimeter-wave monolithic integrated circuit design," in *Microwave Conference (EuMC), 2011 41st European*, 2011, pp. 293-296: IEEE.

[213] K. Hinata, M. Shiraishi, S. Suzuki, and M. Asada, "High power THz oscillators with offset-fed slot antenna and high current density resonant tunneling diodes," in *Infrared, Millimeter, and Terahertz Waves, 2009. IRMMW-THz 2009. 34th International Conference on*, 2009, pp. 1-2: IEEE.

[214] L. Wang, "Reliable design of tunnel diode and resonant tunnelling diode based microwave sources," PhD thesis, University of Glasgow, 2012.

[215] J. Cha, J. Cha, and S. Lee, "Uncertainty analysis of two-step and three-step methods for deembedding on-wafer RF transistor measurements," *IEEE Transactions on Electron Devices,* vol. 55, no. 8, pp. 2195-2201, 2008.

[216] K. Beilenhoff, H. Klingbeil, W. Heinrich, and H. L. Hartnagel, "Open and short circuits in coplanar MMIC's," *IEEE Transactions on Microwave Theory and Techniques,* vol. 41, no. 9, pp. 1534-1537, 1993.

[217] E. Da Silva, *High frequency and microwave engineering*. Newnes, 2001.

[218] E. Korczynski, " integrated 5G chip directions." Solid State Technology

[219] V. Doychinov, "Quantum Barrier Devices for Sub-Millimetre Wave Detection," PhD thesis, University of Leeds, 2015.

[220] R. W. Vogel, "Analysis and design of lumped-and lumped-distributed-element directional couplers for MIC and MMIC applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 40, no. 2, pp. 253-262, 1992.

[221] S. Y. Liao, "Microwave devices and circuits," *Englewood Cliffs: Prentice-Hall, 1985, 2nd ed.*, vol. 1, 1985.

[222] T. Imaoka, S. Banba, A. Minakawa, and N. Imai, "Millimeter-wave wide-band amplifiers using multilayer MMIC technology," *IEEE transactions on microwave theory and techniques,* vol. 45, no. 1, pp. 95-101, 1997.

[223] S.-J. Chung, S.-M. Chen, and Y.-C. Lee, "A novel bi-directional amplifier with applications in active Van Atta retrodirective arrays," *IEEE transactions on microwave theory and techniques,* vol. 51, no. 2, pp. 542-547, 2003.

[224] D. Kim, D.-H. Lee, S. Sim, L. Jeon, and S. Hong, "An X-band switchless bidirectional GaN MMIC amplifier for phased array systems," *IEEE Microwave and Wireless Components Letters,* vol. 24, no. 12, pp. 878-880, 2014.

[225] C.-P. Chang, J.-H. Chen, and Y.-H. Wang, "A fully integrated 5 GHz low-voltage LNA using forward body bias technology," *IEEE Microwave and Wireless Components Letters,* vol. 19, no. 3, pp. 176-178, 2009.

[226] D. Wu, R. Huang, W. Wong, and Y. Wang, "A 0.4-V low noise amplifier using forward body bias technology for 5 GHz application," *IEEE Microwave and Wireless Components Letters,* vol. 17, no. 7, pp. 543-545, 2007.

[227] P. R. Gray, P. Hurst, R. G. Meyer, and S. Lewis, *Analysis and design of analog integrated circuits*. Wiley, 2001.

[228] P. Houston, "High-frequency heterojunction bipolar transistor device design and technology," *Electronics & communication engineering journal,* vol. 12, no. 5, pp. 220-228, 2000.

[229] M. S. Tyagi, *Introduction to semiconductor materials and devices*. John Wiley & Sons, 2008.

[230] J. D. F. Sexton, *Fabrication and characterisation of high-speed indium phosphide-based heterojunction bipolar transistors*. 2005.

[231] J. M. Feldman, "The physics and circuits properties of transistors," 1972.

[232] J. M. Early, "Effects of space-charge layer widening in junction transistors," *Proceedings of the IRE,* vol. 40, no. 11, pp. 1401-1406, 1952.

[233] T. Tauqeer, "Low Power, High Speed InP-Based Digital Intergrated Circuits for Ultra Wide Band Communicatiopn Systems," The University of Manchester, 2009.

[234] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proceedings of the IEEE,* vol. 70, no. 1, pp. 13-25, 1982.

[235] G. Ladd and D. L. Feucht, "Performance potential of high-frequency heterojunction transistors," *IEEE Transactions on Electron Devices,* vol. 17, no. 5, pp. 413-420, 1970.

[236] K. Kurishima, H. Nakajima, S. Yamahata, T. Kobayashi, and Y. Matsuoka, "Effects of a compositionally-graded InxGa1-xAs base in abrupt-emitter InP/InGaAs heterojunction bipolar transistors," *Japanese journal of applied physics,* vol. 34, no. 2S, p. 1221, 1995.

[237] W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs*. Wiley New York, 1999.

[238] B. Jalali and S. Pearton, *InP HBTs: growth, processing, and applications*. Artech House Publishers, 1995.

[239] P. Ashburn, *SiGe heterojunction bipolar transistors*. John Wiley & Sons, 2004.

[240] J. D. Cressler, "Emerging application opportunities for SiGe technology," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, 2008, pp. 57-64: IEEE.

[241] V. Palankovski and S. Selberherr, "Analysis of high speed heterostructure devices," in *Microelectronics, 2004. 24th International Conference on*, 2004, vol. 1, pp. 115-122: IEEE.

[242] M. Khater *et al.*, "SiGe HBT technology with f/sub max//f/sub T/= 350/300 GHz and gate delay below 3.3 ps," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 247-250: IEEE.

[243] J. Bock *et al.*, "3.3 ps SiGe bipolar technology," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 255-258: IEEE.

[244] Z. Griffith *et al.*, "Transistor and circuit design for 100-200-GHz ICs," *IEEE Journal of Solid-State Circuits,* vol. 40, no. 10, pp. 2061-2069, 2005.

[245] Z. Griffith *et al.*, "Ultra high frequency static dividers> 150 GHz in a narrow mesa InGaAs/InP DHBT technology," in *Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting*, 2004, pp. 176-179: IEEE.

[246] M. S. Hybertsen, "Band offset transitivity at the InGaAs/InAlAs/InP (001) heterointerfaces," *Applied physics letters,* vol. 58, no. 16, pp. 1759-1761, 1991.

[247] W. McKinnon, R. Driad, S. McAlister, A. Renaud, and Z. Wasilewski, "Temperature independent current blocking due to hot electrons in InAlAs/InGaAs double heterojunction bipolar transistors with composite collectors," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 16, no. 2, pp. 846-849, 1998.

[248] W. McKinnon, "One-flux analysis of current blocking in double-heterostructure bipolar transistors with composite collectors," *Journal of applied physics,* vol. 79, no. 5, pp. 2762-2770, 1996.

[249] O. Sugiura, A. Dentai, C. Joyner, S. Chandrasekhar, and J. Campbell, "High-current-gain InGaAs/InP double-heterojunction bipolar transistors grown by metal organic vapor phase epitaxy," *IEEE electron device letters,* vol. 9, no. 5, pp. 253-255, 1988.

[250] S. McAlister, W. McKinnon, R. Driad, and A. Renaud, "Use of dipole doping to suppress switching in indium phosphide double heterojunction bipolar transistors," *Journal of applied physics,* vol. 82, no. 10, pp. 5231-5234, 1997.

[251] M. Mohiuddin, T. Tauqeer, J. Sexton, R. Knight, and M. Missous, "Elimination of current blocking in ternary InAlAs-InGaAs-InAlAs double heterojunction bipolar transistors," *IEEE Transactions on Electron Devices,* vol. 57, no. 12, pp. 3340-3347, 2010.

[252] C. Chang and F. Kai, "GaAs high-speed devices," *Physics Technology and Circuit,* 1994.

[253] R. J. Knight, "The development of a novel all ternary InAlAs/InGaAs double heterojunction bipolar transistor (DHBT) for the design, simulation and fabrication of a static divide-by-2 frequency divider," 2012.

[254] M. Kim, A. Oki, G. Gorman, D. Umemoto, and J. Camou, "GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1286-1303, 1989.

[255] W. Liu, *Handbook of III-V heterojunction bipolar transistors*. Wiley New York, 1998.

[256] W. Liu and J. Harris, "Diode ideality factor for surface recombination current in AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 39, no. 12, pp. 2726-2732, 1992.

[257] D. Cui, D. Pavlidis, S. S. Hsu, and A. Eisenbach, "Comparison of DC and high-frequency performance of zinc-doped and carbon-doped InP/InGaAs HBTs grown by metalorganic chemical vapor deposition," *IEEE Transactions on Electron Devices*, vol. 49, no. 5, pp. 725-732, 2002.

[258] J. D. Cressler and G. Niu, *Silicon-Germanium heterojunction bipolar transistors*. Artech house, 2003.

[259] K. C. D. Yu, K. Lee, B. Kim, H. Zhu, K. Vargason, J. M. Kuo, P. Pinsukanjana, and Y. C. Kao,, "Ultra high-speed 0.25μm emitter InP-InGaAs SHBTs with fmax of 687 GHz," *in 2004 International Electron Devices Meeting, 13-15 Dec. 2004, San Francisco, CA, USA, 2005, pp. 557-60*, pp. 57-60.

[260] Q. Lee, S. Martin, D. Mensa, R. Smith, J. Guthrie, and M. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors," *IEEE Electron Device Letters*, vol. 20, no. 8, pp. 396-398, 1999.

[261] W. Hafez and M. Feng, "Experimental demonstration of pseudomorphic heterojunction bipolar transistors with cutoff frequencies above 600 GHz," *Applied Physics Letters*, vol. 86, no. 15, p. 152101, 2005.

[262] M. Rodwell *et al.*, "Submicron lateral scaling of HBTs and other vertical-transport devices: towards THz bandwidths," 2000.

[263] M. Azadeh, *Fiber optics engineering*. Springer, 2009.

[264] L. Vivien *et al.*, "42 GHz pin Germanium photodetector integrated in a silicon-on-insulator waveguide," *Optics express*, vol. 17, no. 8, pp. 6252-6257, 2009.

[265] J. M. Fedeli *et al.*, "High-performance waveguide-integrated germanium PIN photodiodes for optical communication applications," in *2014 7th International Silicon-Germanium Technology and Device Meeting (ISTDM)*, 2014, pp. 131-132: IEEE.

[266] M. Oehme, J. Werner, E. Kasper, M. Jutzi, and M. Berroth, "High bandwidth Ge p-i-n photodetector integrated on Si," *Applied physics letters*, vol. 89, no. 7, p. 071117, 2006.

[267] P. S. Menon, A. A. Ehsan, and S. Shaari, "Modeling and Optimization of Three-Dimensional Interdigitated Lateral pin Photodiodes Based on In0. 53Ga0. 47As Absorbers for Optical Communications," in *Advances in Photodiodes*: InTech, 2011.

[268] J.-W. Shi, Y.-H. Cheng, J.-M. Wun, K.-L. Chi, Y.-M. Hsin, and S. D. Benjamin, "High-speed, high-efficiency, large-area pin photodiode for application to optical interconnects from 0.85 to 1.55 μm wavelengths," *Journal of Lightwave Technology,* vol. 31, no. 24, pp. 3956-3961, 2013.

[269] G. Wang, T. Tokumitsu, I. Hanawa, K. Sato, and M. Kobayashi, "Analysis of high speed pin photodiode S-parameters by a novel small-signal equivalent circuit model," *IEEE microwave and wireless components letters,* vol. 12, no. 10, pp. 378-380, 2002.

[270] S. Chandrasekhar, A. Dentai, C. Joyner, B. Johnson, A. Gnauck, and G. Qua, "4 Gbit/s pin/HBT monolithic photoreceiver," *Electronics Letters,* vol. 26, no. 22, pp. 1880-1882, 1990.

[271] A. Gutierrez-Aitken, K. Yang, X. Zhang, G. Haddad, and P. Bhattacharya, "9 GHz bandwidth InP-based integrated PIN-HBT photoreceiver," in *Indium Phosphide and Related Materials, 1995. Conference Proceedings., Seventh International Conference on*, 1995, pp. 357-360: IEEE.

[272] A. Gutierrez-Aitken, K. Yang, X. Zhang, G. Haddad, P. Bhattacharya, and L. Lunardi, "16-GHz bandwidth InAlAs-InGaAs monolithically integrated pin/HBT photoreceiver," *IEEE Photonics Technology Letters,* vol. 7, no. 11, pp. 1339-1341, 1995.

[273] W.-k. Huang *et al.*, "37-GHz bandwidth monolithically integrated InP HBT/evanescently coupled photodiode," *IEEE photonics technology letters,* vol. 18, no. 12, pp. 1323-1325, 2006.

[274] S. G. Muttlak, O. S. Abdulwahid, J. Sexton, M. J. Kelly, and M. Missous, "InGaAs/AlAs Resonant Tunneling Diodes for THz Applications: An Experimental Investigation," *IEEE Journal of the Electron Devices Society,* vol. 6, no. 1, pp. 254-262, 2018.

[275] A. Stohr, A. Malcoci, A. Sauerwald, I. C. Mayorga, R. Gusten, and D. Jager, "Ultra-wide-band traveling-wave photodetectors for photonic local oscillators," *Journal of Lightwave Technology,* vol. 21, no. 12, pp. 3062-3070, 2003.

[276] H. Jiang and P. Yu, "Equivalent circuit analysis of harmonic distortions in photodiode," *IEEE Photonics Technology Letters,* vol. 10, no. 11, pp. 1608-1610, 1998.

[277] J.-J. Jou, C.-K. Liu, C.-M. Hsiao, H.-H. Lin, and H.-C. Lee, "Time-delay circuit model of high-speed pin photodiodes," *IEEE Photonics Technology Letters,* vol. 14, no. 4, pp. 525-527, 2002.

[278] J. Zhang and D. R. Conn, "State-space modeling of the PIN photodetector," *Journal of lightwave technology,* vol. 10, no. 5, pp. 603-609, 1992.

[279] G. Wang, T. Tokumitsu, I. Hanawa, Y. Yoneda, K. Sato, and M. Kobayashi, "A time-delay equivalent-circuit model of ultrafast pin photodiodes," *IEEE Transactions on Microwave Theory and Techniques,* vol. 51, no. 4, pp. 1227-1233, 2003.

[280] K. Kato, S. Hata, K. Kawano, and A. Kozen, "Design of ultrawide-band, high-sensitivity pin protodetectors," *IEICE Transactions on Electronics,* vol. 76, no. 2, pp. 214-221, 1993.

[281] K. Kato, "Ultrawide-band/high-frequency photodetectors," *IEEE transactions on Microwave Theory and Techniques,* vol. 47, no. 7, pp. 1265-1281, 1999.

[282] I.-H. Tan, J. E. Bowers, E. L. Hu, B. Miller, and R. Capik, "New approach for high-speed, high-sensitivity photodetectors," in *Seventh International Conference on Indium Phosphide and Related Materials*, 1995, pp. 365-368: IEEE.

[283] S. R. Bahl, N. Moll, V. M. Robbins, H.-C. Kuo, B. G. Moser, and G. E. Stillman, "Be diffusion in InGaAs/InP heterojunction bipolar transistors," *IEEE Electron Device Letters,* vol. 21, no. 7, pp. 332-334, 2000.

[284] R. Metzger, M. Hafizi, R. Wilson, W. Stanchina, J. Jensen, and L. McCray, "Be diffusion at the emitter-base junction of graded AlInAs/GaInAs heterojunction bipolar transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* vol. 10, no. 6, pp. 2347-2350, 1992.

[285] S.-i. Tanaka, H. Shimawaki, K. Kasahara, and K. Honjo, "Characterization of current-induced degradation in Be-doped HBTs based in GaAs and InP," *IEEE Transactions on Electron Devices,* vol. 40, no. 7, pp. 1194-1201, 1993.

[286] D. S. Atlas, "Atlas User's Manual," *Silvaco International Software, Santa Clara, CA, USA,* 2015.

[287] A. Davidson, E. Strid, and K. Jones, "Achieving greater on-wafer S-parameter accuracy with the LRM calibration technique," in *ARFTG Conference Digest-Winter, 34th,* 1989, vol. 16, pp. 61-66: IEEE.

[288] D. Rytting, "Advances in microwave error correction techniques," *in RF & Microwave Measurement Symposium and Exhibition,* 1987.

[289] M. Sotoodeh *et al.,* "Stepping toward standard methods of small-signal parameter extraction for HBTs," *IEEE Transactions on Electron Devices,* vol. 47, no. 6, pp. 1139-1151, 2000.

[290] U. Schaper and B. Holzapfl, "Analytical parameter extraction of the HBT equivalent circuit with T-like topology from measured S-parameters," *IEEE transactions on microwave theory and techniques,* vol. 43, no. 3, pp. 493-498, 1995.

[291] H. Gummel and H. Poon, "An integral charge control model of bipolar transistors," *Bell System Technical Journal,* vol. 49, no. 5, pp. 827-852, 1970.

[292] M. Rudolph, *Introduction to modeling HBTs*. Artech House Norwood, MA, 2006.

[293] T. Ishibashi, "Nonequilibrium electron transport in HBTs," *IEEE Transactions on Electron Devices,* vol. 48, no. 11, pp. 2595-2605, 2001.

[294] M. Iwamoto *et al.,* "Large-signal HBT model with improved collector transit time formulation for GaAs and InP technologies," in *Microwave Symposium Digest, 2003 IEEE MTT-S International,* 2003, vol. 2, pp. 635-638: IEEE.

[295] M. Rudolph, R. Doerner, K. Beilenhoff, and P. Heymann, "Scalable GaInP/GaAs HBT large-signal model," *IEEE Transactions on microwave theory and techniques,* vol. 48, no. 12, pp. 2370-2376, 2000.

[296] T. Kim and K. Yang, "A new large-signal InP/InGaAs Single HBT model including self-heating and impact ionization effects," in *Microwave Symposium Digest, 2002 IEEE MTT-S International,* 2002, vol. 3, pp. 2141-2144: IEEE.

[297] K. TECHNOLOGIES, "AgilentHBT_Model," *USA, Available: http://edadocs.software.keysight.com/pages/viewpage.action?pageId=6262855*.

[298] S. Maas and D. Tait, "Parameter-extraction method for heterojunction bipolar transistors," *IEEE Microwave and guided wave letters,* vol. 2, no. 12, pp. 502-504, 1992.

[299] M. Mohiuddin, "InGaAs/InAlAs double heterojunction bipolar transistors for high-speed, low-power digital applications," PhD thesis, The University of Manchester, 2010.

[300] K. Lee, K. Choi, S.-H. Kook, D.-H. Cho, K.-W. Park, and B. Kim, "Direct parameter extraction of SiGe HBTs for the VBIC bipolar compact model," *IEEE Transactions on Electron Devices,* vol. 52, no. 3, pp. 375-384, 2005.

[301] Y. Gobert, P. Tasker, and K. Bachem, "A physical, yet simple, small-signal equivalent circuit for the heterojunction bipolar transistor," *IEEE Transactions on Microwave Theory and Techniques,* vol. 45, no. 1, pp. 149-153, 1997.

[302] Y. Betser, D. Ritter, G. Bahir, S. Cohen, and J. Sperling, "Measurement of the minority carrier mobility in the base of heterojunction bipolar transistors using a magnetotransport method," *Applied physics letters,* vol. 67, no. 13, pp. 1883-1884, 1995.

[303] S. Yamahata, K. Kurishima, H. Ito, and Y. Matsuoka, "Over-220-GHz-f/sub T/-and-f/sub max/InP/InGaAs double-heterojunction bipolar transistors with a new hexagonal-shaped emitter," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1995. Technical Digest 1995., 17th Annual IEEE*, 1995, pp. 163-166: IEEE.

[304] L. Lunardi, S. Chandrasekhar, A. Gnauck, C. Burrus, A. Dentai, and J. Rios, "15 Gbit/s pin/HBT optoelectronic integrated photoreceiver module realised using MOVPE material," *Electronics Letters,* vol. 31, no. 14, pp. 1185-1186, 1995.

[305] L. Lunardi *et al.*, "A 12-Gb/s high-performance, high-sensitivity monolithic pin/HBT photoreceiver module for long-wavelength transmission systems," *IEEE photonics technology letters,* vol. 7, no. 2, pp. 182-184, 1995.

[306] H. Masuda *et al.*, "High performance inp/ingaas hbts for 40-gb/s optical transmission ics," *IEICE Transactions on Electronics,* vol. 82, no. 3, pp. 419-427, 1999.

[307] N. Duan, "Avalanche photodiodes with low noise, high speed and PIN photodetectors with high output power," 2006.

[308] J. C. Rasmussen, "PMD and chromatic dispersion compensation for 40 Gbit/s optical networks," in *Lasers and Electro-Optics Society, 2005. LEOS 2005. The 18th Annual Meeting of the IEEE*, 2005, pp. 704-705: IEEE.

[309] H. Fukuyama *et al.*, "Photoreceiver module using an InP HEMT transimpedance amplifier for over 40 Gb/s," *IEEE journal of solid-state circuits,* vol. 39, no. 10, pp. 1690-1696, 2004.

[310] G. Mekonnen *et al.*, "37 GHz bandwidth InP-based photoreceiver OEIC suitable for data rates up to 50 Gb/s," *IEEE Photonics Technology Letters,* vol. 11, no. 2, pp. 257-259, 1999.

[311] S. Chandrasekhar, L. M. Lunardi, A. Gnauck, R. Hamm, and G. Qua, "High-speed monolithic pin/HBT and HPT/HBT photoreceivers implemented with simple phototransistor structure," *IEEE photonics technology letters,* vol. 5, no. 11, pp. 1316-1318, 1993.

[312] K. Pedrotti, N. Sheng, R. Pierson, C. Farley, M. Rosker, and M. Chang, "Monolithic ultrahigh-speed GaAs HBT optical integrated receivers," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1991. Technical Digest 1991., 13th Annual*, 1991, pp. 205-208: IEEE.

[313] R. Montgomery, A. Feygenson, P. Smith, R. Yadvish, R. Hamm, and H. Temkin, "A 28 GHz transimpedance preamplifier with inductive bandwidth enhancement," in *IEDM Tech. Digest*, 1992, pp. 423-425.

[314] T. Vanisri and C. Toumazou, "Integrated high frequency low-noise current-mode optical transimpedance preamplifiers: Theory and practice," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 6, pp. 677-685, 1995.

[315] S.-S. Lu, Y.-S. Lin, H.-W. Chiu, Y.-C. Chen, and C.-C. Meng, "The determination of S-parameters from the poles of voltage-gain transfer function for RF IC design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 1, pp. 191-199, 2005.

[316] E. Cohen *et al.*, "75 GHz InP HBT distributed amplifier with record figures of merit and low power dissipation," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 392-394, 2006.

[317] J. Kim and J. F. Buckwalter, "Bandwidth enhancement with low group-delay variation for a 40-Gb/s transimpedance amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1964-1972, 2010.

[318] Z. Lu, K. S. Yeo, J. Ma, M. A. Do, W. M. Lim, and X. Chen, "Broad-band design techniques for transimpedance amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 3, pp. 590-600, 2007.

[319] F.-T. Chien and Y.-J. Chan, "Bandwidth enhancement of transimpedance amplifier by a capacitive-peaking design," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 8, pp. 1167-1170, 1999.

[320] M. Gould, T. Baehr-Jones, R. Ding, and M. Hochberg, "Bandwidth enhancement of waveguide-coupled photodetectors with inductive gain peaking," *Optics Express*, vol. 20, no. 7, pp. 7101-7111, 2012.

[321] R. A. Aroca and C. A. T. Salama, "Wide dynamic range parallel feedback transimpedance amplifier for 10 Gb/s optical links," *Analog Integrated Circuits and Signal Processing*, vol. 48, no. 3, pp. 167-174, 2006.

[322] H. Ikeda, T. Ohshima, M. Tsunotani, T. Ichioka, and T. Kimura, "An auto-gain control transimpedance amplifier with low noise and wide input dynamic range for 10-Gb/s optical communication systems," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 9, pp. 1303-1308, 2001.

[323] M.-C. Chiang, S.-S. Lu, C.-C. Meng, S.-A. Yu, S.-C. Yang, and Y.-J. Chan, "Analysis, design, and optimization of InGaP-GaAs HBT matched-impedance wide-band amplifiers with multiple feedback loops," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 6, pp. 694-701, 2002.

[324] K. Ohhata, T. Masuda, K. Imai, R. Takeyari, and K. Washio, "A wide-dynamic-range, high-transimpedance Si bipolar preamplifier IC for 10-Gb/s optical fiber links," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 1, pp. 18-24, 1999.

[325] Y. Akatsu, Y. Miyagawa, Y. Miyamoto, Y. Kobayashi, and Y. Akahori, "A 10 Gb/s high sensitivity, monolithically integrated pin-HEMT optical receiver," *IEEE photonics technology letters*, vol. 5, no. 2, pp. 163-165, 1993.

[326] H. Matsuda *et al.*, "High performance of 10-Gb/s APD/preamplifier optical-receiver module with compact size," *IEEE Photonics Technology Letters*, vol. 15, no. 2, pp. 278-280, 2003.

[327] D. Sieniawski, "Low cost 10 Gb/s receiver module," in *Electronic Components & Technology Conference, 1998. 48th IEEE*, 1998, pp. 181-183: IEEE.

[328] J.-D. Jin and S. S. Hsu, "A 75-dBΩ 10Gb/s Transimpedance Amplifier in 0.18μm CMOS Technology," *IEEE Photonics Technology Letters,* vol. 20, no. 24, pp. 2177-2179, 2008.

[329] K. Krishnamurthy, R. Vetury, Y.-z. Liu, M. Rodwell, and R. Pullela, "40 Gbit/s optical receiver module with high conversion gain and sensitivity," *Electronics Letters,* vol. 39, no. 24, pp. 1738-1739, 2003.

[330] N. Shimizu *et al.*, "40 Gbit/s monolithic digital OEIC composed of unitravelling-carrier photodiode and InP HEMTs," *Electronics Letters,* vol. 36, no. 14, pp. 1220-1221, 2000.

[331] C. Schramm *et al.*, "High-bandwidth balanced photoreceiver suitable for 40-gb/s RZ-DPSK modulation formats," *IEEE Journal of selected topics in quantum electronics,* vol. 11, no. 1, pp. 127-134, 2005.

[332] H.-G. Bach, A. Beling, G. G. Mekonnen, and W. Schlaak, "Design and fabrication of 60-Gb/s InP-based monolithic photoreceiver OEICs and modules," *IEEE Journal of selected topics in quantum electronics,* vol. 8, no. 6, pp. 1445-1450, 2002.

[333] J.-S. Youn, M.-J. Lee, K.-Y. Park, and W.-Y. Choi, "10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector," *IEEE journal of quantum electronics,* vol. 48, no. 2, pp. 229-236, 2012.

[334] K. Ohhata, T. Masuda, E. Ohue, and K. Washio, "Design of a 32.7-GHz bandwidth AGC amplifier IC with wide dynamic range implemented in SiGe HBT," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 9, pp. 1290-1297, 1999.

[335] C. H. Fields *et al.*, "110+ ghz transimpedance amplifier in inp-hbt technology for 100 gbit ethernet," *IEEE Microwave and Wireless Components Letters,* vol. 20, no. 8, pp. 465-467, 2010.

[336] J. S. Weiner *et al.*, "An InGaAs-InP HBT differential transimpedance amplifier with 47-GHz bandwidth," *IEEE journal of solid-state circuits,* vol. 39, no. 10, pp. 1720-1723, 2004.

[337] N. Kashio, K. Kurishima, K. Sano, M. Ida, N. Watanabe, and H. Fukuyama, "Monolithic integration of InP HBTs and uni-traveling-carrier photodiodes using nonselective regrowth," *IEEE Transactions on Electron Devices,* vol. 54, no. 7, pp. 1651-1657, 2007.

[338] Z. M. Nosal and T. P. Broekaert, "InP HBT transimpedance amplifier for 43 Gb/s optical link applications," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, 2003, vol. 1, pp. 117-120: IEEE.

[339] H.-Y. Jung, J.-M. Lee, and W.-Y. Choi, "A high-speed CMOS integrated optical receiver with an under-damped TIA," in *Photonics Conference (IPC), 2015*, 2015, pp. 347-350: IEEE.

[340] L. Szilagyi, R. Henker, and F. Ellinger, "A 0.68 pJ/bit inductor-less optical receiver for 20 Gbps with 0.0025 mm2 area in 28 nm CMOS," in *System-on-Chip Conference (SOCC), 2015 28th IEEE International*, 2015, pp. 35-39: IEEE.

[341] C. Schow, L. Schares, S. Koester, G. Dehlinger, R. John, and F. Doany, "A 15-Gb/s 2.4-V optical receiver using a Ge-on-SOI photodiode and a CMOS IC," *IEEE photonics technology letters,* vol. 18, no. 19, pp. 1981-1983, 2006.

[342] F. Ren, C. Abernathy, S. Pearton, L. Yang, and S. Fu, "Novel fabrication of self-aligned GaAsAlGaAs and GaAsInGaP microwave power heterojunction bipolar transistors," *Solid-state electronics*, vol. 38, no. 9, pp. 1635-1639, 1995.