Application and Evaluation of GaN Technology in High Performance DC-DC Converters

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Contents

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A, B	Characteristic equation coefficients
A_C	Material contact area
C_{in}	Input capacitor
C_o	Output capacitor
C_{oss_Sa1}, C_{oss_Sa2}	Device output capacitance of S_{a1} and S_{a2}
C_{oss_D}	Sum of parasitic capacitance of D_a, D_b and D_0
C_a, C_b	Switched capacitors in phase *a* and *b*
C_{T2}, C_{T3}, C_{T4}	Effective capacitances of soft-switching converter resonant circuits during sub-periods 2, 3, 4
C_S	Snubber capacitance
D	Main transistor duty ratio
D_a, D_b	Switched diodes in phase *a* and *b*
D_0	Switched diode between phase *a* and *b*
D_{aux0}	Diode in the auxiliary circuit
E_{sw}	Switching energy
E_{on}, E_{off}	Switching energy during turn-on and turn-off
f	Switching frequency
i_{in}, i_{out}	Converter input and output currents
i_{Lin}	Input inductor current
i_{La}, i_{Lb}	Output inductor currents of phase *a* and *b*
i_{Laux}	Auxiliary inductor current
i_{ds}	Transistor drain current
i_{DSa1}, i_{DSa2}	Drain currents of S_{a1} and S_{a2}
$i_{Channel\_Sa1}$, $i_{Channel\_Sa2}$	Channel currents of S_{a1} and S_{a2}
i_{Lin_avg}, i_{La_avg}, i_{Lb_avg}	DC currents of L_{in}, L_a and L_b
i_{Lo_avg}	DC current of the output inductors
i_{oss_Da}, i_{oss_Db}, i_{oss_D0}	Parasitic capacitive currents of D_a, D_b and D_0
i_{oss_Sa1}, i_{oss_Sa2}, i_{oss_Sb1}, i_{oss_Sb2}	Parasitic capacitive currents of S_{a1}, S_{a2}, S_{b1} and S_{b2}
i_{oss_Sauxa}, i_{oss_Sauxb}	Parasitic capacitive currents of S_{auxa} and S_{auxb}
i_{error}	Quantization error in the current measurement
Δi_{Lin}, Δi_{La}, Δi_{Lb}	Ripple currents of the input and output inductors

Δi_{Lo}	Output inductor current ripple
Δi_o	Output capacitor current ripple
$\Delta i_{L\text{-}rms}$	RMS value of the inductor ripple current
K	Material thermal conductivity
K_{dy}	Dynamic on-resistance increase coefficient
L_{in}	Input inductor
L_a, L_b	Output inductors of phase *a* and *b*
L_{aux}	Auxiliary inductor
N	Transformer/coupled inductor turns ratio
P_{in}	Converter input power
P_o	Converter output power
P_{sw}	Average Switching loss
P_{on}, P_{off}	Instantaneous power losses during turn-on and turn-off
P_{con}, $P_{con\text{-}rev}$	Transistor conduction and reverse conduction losses
$P_{con\text{-}D}$	Diode forward conduction loss
Q_{oss_MOSFET}	Output charge of the Si MOSFET
Q_{rr_MOSFET}, Q_{rr_diode}	Reverse recovery charge of the Si MOSFET and diode
R_{DC}	Inductor winding DC resistance
R_{AC}	Inductor winding AC resistance
$R_{ds(on)}$	Transistor on-state DC resistance
$R_{(1us)}$	Dynamic on-state resistance 1 μs after turn-on
R_S	Snubber resistance
R_θ	Thermal resistance
$R_{JC\text{-}D}$, $R_{JC\text{-}S}$	Diodes and transistors junction-to-case thermal resistance
R_{PCB}, R_{copper}, R_{TIM1}, R_{TIM2}, R_{HSA}	Thermal resistance of copper bar, thermal interface material and heatsink
R_{error}	Quantization error in the calculated resistance
S_1, S_2	Top and bottom device in converter leg
S_{a1}, S_{a2}	Top and bottom device in leg *a*
S_{b1}, S_{b2}	Top and bottom device in leg *b*
S_{auxa}, S_{auxb}, S_{aux0}	Soft-switching converter auxiliary transistors
t_{off1}, t_{off2}	Transistor off-state time

t_0-t_8	Transition times of converter sub-periods
T_1, T_2, T_3, T_4, T_5	Durations of converter sub-periods 1, 2, 3, 4, 5
T	Switching period
T_M	Thickness of material
T_{sw}	Switching time
$T_{con\text{-}rev}$	Transistor reverse conduction time
$T_{con\text{-}D}$	Diode conduction time
T_{DT}	Dead time between the top and bottom transistors
T_J	Devices junction temperatures
T_{case}	Components case temperatures
$T_{Ambient}$	Ambient temperature
V_{in}, V_o	Converter input and output voltages
V_C	Switched capacitor voltage
ΔV_{Cin}, ΔV_{Co}, ΔV_C	Ripple voltages of the input, output and switch capacitors
ΔV_{Ca}, ΔV_{Cb}	Ripple voltages of C_a and C_b
V_f	Forward voltage drop of diodes and transistors
V_{GSa1}, V_{GSa2}	Gate-to-source voltage of S_{a1} and S_{a2}
V_{GSb1}, V_{GSb2}	Gate-to-source voltage of S_{b1} and S_{b2}
V_{GSauxa}, $V_{GSauxb,}$, V_{GSaux0}	Gate-to-source voltage of S_{auxa} , S_{auxb} and S_{aux0}
V_{gs}	Transistor gate-to-source voltage
V_{ds}	Transistor drain-to-source voltage
$V_{ds(on)}$	Transistor on-state voltage
V_{DSa1}, V_{DSa2}	Drain-to-source voltage of S_{a1} and S_{a2}
V_{Lin}	Input inductor voltage
V_{La}, V_{Lb}	Output inductor voltages of phase *a* and *b*
$V_{DC\text{-}link}$	DC link voltage
V_{oss}	Device output capacitor voltage
V_1-V_8	Key voltage values in experimental waveforms
V_{error}	Quantization error in the voltage measurement
ω_{T2}, ω_{T3}, ω_{T4}	Angular frequency of the converter resonant circuits during sub-periods 2, 3, 4
δ	Auxiliary transistor S_{auxa} and S_{auxb} duty ratio
δ_2	Auxiliary transistor S_{aux0} duty ratio

List of abbreviations

2DEG	Two-dimensional electron gas
APM	Auxiliary power module
BTP	Bridgeless totem pole
BJT	Bi-polar junction transistor
CCM	Continuous conduction mode
CRM	Critical conduction mode
DCM	Discontinuous conduction mode
DUT	Device under test
DPT	Double pulse test
DAB	Dual active bridge
DFM	Design for manufacturing
EV	Electric vehicle
EMI	Electromagnetic interference
FOM	Figure of merit
GIT	Gate injection transistors
GaN	Gallium Nitride
HEMT	High electron mobility transistor
IC	Integrated circuit
JFET	Junction gate field-effect transistor
MOSFET	Metal–oxide–semiconductor field-effect transistor
OBC	On-board charger
PFC	Power factor correction
PSFB	Phase shift full bridge
PCB	Printed circuit board
PHEV	Plug-in hybrid electric vehicle
Si	Silicon Carbide
SC	Switched capacitor
SL	Switched inductor
SJ	Super junction
SPICE	Simulation program with integrated circuit emphasis
TIM	Thermal interface material

TI	Texas Instruments
TCM	Triangular current mode
WBG	Wide band gap
V2G	Vehicle to grid
ZVS	Zero voltage switching
ZCS	Zero current switching

Abstract

This research has investigated the potential of emerging GaN power transistors to meet some of the power conversion challenges that are being posed by transport electrification. The switching performance, driving requirements and on-state characteristics of an example high current GaN HEMT are examined practically followed by the development and demonstration of a high-step-down-ratio DC-DC converter that includes a soft-switching capability.

The GS66516T 650 V/60 A HEMT from GaN Systems that represents a typical GaN HEMT model, was shown to achieve a turn-on speed of 9.2 A/ns with a current overshoot of 32% and a turn-off speed of 94.7 V/ns with a voltage overshoot of 45%, resulting in a total switching loss of less than 150 μJ at 400 V, 40 A. The significance of the driver selection and parasitic component optimization were highlighted and the ultra-low turn-off loss mechanism of the GaN HEMT was identified.

The dynamic on-state resistance of three GaN devices were measured over a range of conditions that are often encountered in converter applications. Significant variations were observed between device types. An increase in dynamic on-state resistance of 20~30% was observed for the GaN Systems device within 3 μs of turn-on after 50 μs of 400 V stress voltage. The dynamic on-state resistance was largely insensitive to temperature but depended on the switching energy. During continuous operation, an increase of 50.4% in average on-state resistance of the GaN Systems device was observed when operating at 400 V, 10 A, 400 kHz and 0.5 duty ratio.

The switched-capacitor, step-down DC-DC converter topology was extended to an interleaved configuration, enabling increased output currents, and its performance was evaluated in a 270-28 V, 200 kHz, 1.2 kW prototype, paying particular attention to the switching waveforms. Furthermore, a multi-layer assembly was used to provide compact electrical and thermal connections. The efficiency of 92.6% represented a five percentage point increase over an equivalent silicon design. A soft-switching topology was then developed to control the switching losses and dv/dt levels by adding a small auxiliary circuit. The converter overall efficiency remained similar due to the introduced auxiliary losses but the converter reliability was significantly improved due to the reduced stress in the GaN transistors.

Declaration

No portion of the work referred to in the thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

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Chapter 1

Introduction

1.1 Background

The advance of technology and the drive for more sustainable forms of energy use in the field of transportation, industrial automation, internet services, entertainment and electronic consumer goods has led to an ever-increasing demand on electrical power. Up to 2018, the electricity production in the UK had increased by 38.4% to 1473.5 TWh compared to 2010, of which 30.9% was consumed for industrial use, 35.1% for domestic use, 1.6% for transportation and 32.4% for other services [1].

The increasing use of electrical power has intensified the demand for reliable and cost-effective technologies and systems to manage and convert the power according to the demands of different applications. This is producing an ever-growing range of conversion requirements in terms of voltage and current, however, achieving high efficiency and small equipment size remain important for all applications, especially for mobile and transport systems.

In addition to the increasing demands from applications, the power electronic industry is undergoing a period of revolutionary change due to the emergence of new power semiconductor technologies based on wide bandgap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN). These materials offer the prospect of new devices with lower on-state losses, faster switching speeds, higher blocking voltages and increased junction temperatures than existing silicon devices.

Whilst these new devices offer the opportunity of making a step-change in converter performance, there are many unknowns and challenges including, the detailed characteristics of the devices, the most-effective driving techniques, the best packaging and interconnection techniques and the most suitable converter topologies.This work identified some emerging challenges for WBG-based converter applications and demonstrated the performance benefits in a GaN-based DC-DC converter case.

1.2 Aim and objectives

The aim of this research was to investigate how WBG devices particularly GaN devices could enable performance improvements for power converters in some of the emerging applications in transport systems.

The first objective was to characterize the switching performance and the dynamic on-state resistance of commercial GaN HEMTs rated at 600 V/650 V. These characteristics directly link to the device switching and conduction losses in converter applications.

The second objective was to identify a suitable converter topology for potential high-step-down-ratio DC-DC transportation applications, validate the topology in a converter prototype and demonstrate the performance boost by using WBG technology.

The third objective was to enhance the selected converter topology through the use of soft-switching, and demonstrate the further improvement in the converter performance.

1.3 Thesis structure

Chapter 2 presents a review of the main publications regarding the current status of commercial WBG devices, the characteristics of GaN devices and the application of WBG devices in the hybrid and EV sector.

Chapter 3 describes the experimental characterization of commercial GaN transistors in terms of switching performance and dynamic on-state resistance, requiring the development of testing methodologies. The experimental measurements for switching speed, switching losses and dynamic on-resistance over a range of conditions are presented.

Chapter 4 describes the selection and validation of a WBG-based, high-step-down ratio, DC-DC converter topology including detailed analysis of the device switching waveforms, prototype design and performance evaluation. The superiority of the WBG-solution was assessed by comparison with a conventional Si-solution.

Chapter 5 presents the development and validation of a soft-switching technique for the high step-down-ratio DC-DC converter in Chapter 4. Detailed analysis of the circuit operation was undertaken forming a basis for prototype design. Experimental results for performance comparison with the hard-switching converter were collected and presented.

Chapter 6 presents the conclusions of the research work, its contributions and identifies further research opportunities.

Chapter 2

Literature Review

2.1 Introduction

This chapter introduces the emerging wide-band-gap material and power devices, including the current status and characteristics of GaN power devices, followed by a review of high-performance, high-power-density converters for transportation applications using WBG technology. Several high-conversion-ratio DC-DC converter topologies are also reviewed.

2.2 Emerging device technology

Since the 1960s power semiconductor devices have been based on silicon technology [2]. However, with incremental advances in the device design, manufacturing, fabrication and assembly processes, the performance of Si devices is approaching the theoretical limit of the material. For instance, the Infineon IPB025N10N3G 100V MOSFET has pushed the specific on-state resistance to less than 0.1 Ω/mm^2, which is almost at the theoretical limit of a one-dimensional Si device [3].

2.2.1 WBG material

As alternatives, wide bandgap (WBG) materials such as SiC and GaN have emerged and drawn growing attention for power applications. The material bandgap is used to describe the energy required for an electron to jump from the top of the valence band to the bottom of the conduction band within the semiconductor. Typically, materials with bandgaps greater than that of silicon, 1 eV, are referred to as wide bandgap material [4].

Table 2.1 and Fig. 2.1 show the material properties for Si, SiC (SiC-4H) and GaN which also include the major electrical characteristics for the corresponding semiconductor devices [5]. The wide bandgap and higher critical field of SiC and GaN material indicates that a smaller/thinner die could block a certain voltage, potentially leading to lower on-state voltage and smaller parasitic capacitances. It also means that the device has the potential of operating at higher temperature with lower leakage current [6]. The electron

mobility and electron saturation velocity influence the device on-state resistance [7]. GaN material shows the greatest potential in this aspect, which suggests that GaN-based power devices could offer the smallest on-state resistance associated with high breakdown voltage, exceeding the limits of Si and SiC material shown in Fig 2.1. These features make GaN-based devices the most promising candidate for high frequency applications, but less competitive than SiC-based devices for applications aiming at particularly high ambient temperature [8].

Table 2.1 Material Properties of Si, SiC and GaN [5]

Materials Property	Si	SiC-4H	GaN
Band Gap (eV)	1.1	3.2	3.4
Critical Field (MV/cm)	0.3	2.2	3.3
Electron Mobility (10^3 cm^2V/s)	1.45	0.9	2
Electron Saturation Velocity (10^7 cm/s)	1	2.2	2.5
Thermal Conductivity (W/cmK)	1.5	3.8	1.3

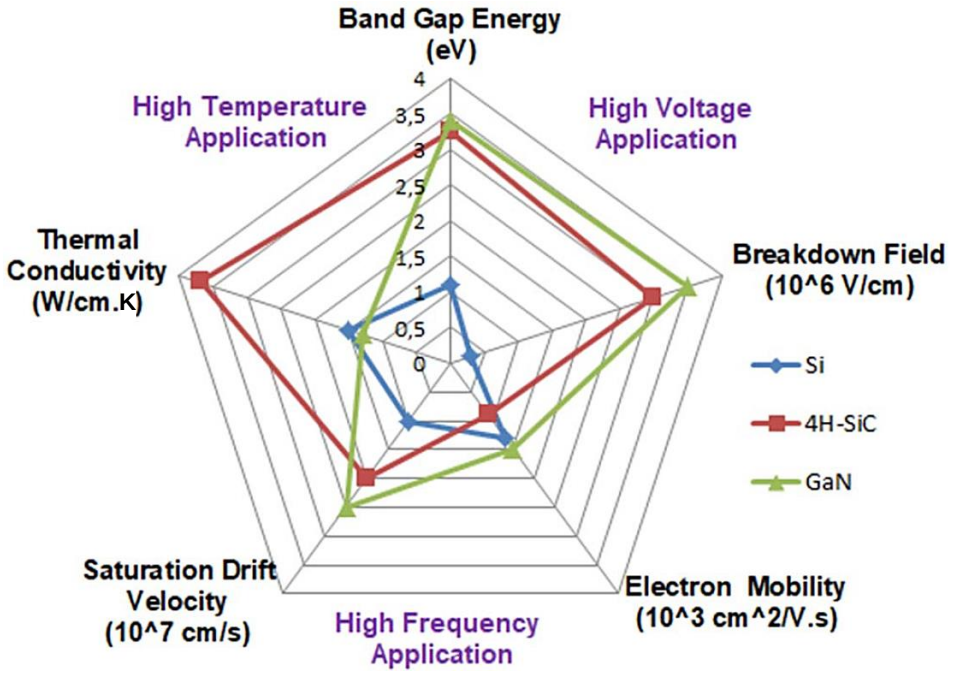


Fig. 2.1. Material properties comparison of Si, SiC and GaN [9]

2.2.2 Off-the-shelf WBG devices

Fig. 2.2 shows the one-dimensional theoretical limit of Si, SiC and GaN, and maps the position of some commercial product samples. It can be seen that current commercial Si MOSFETs are reaching the material one-dimensional theoretical limit, whilst SiC and GaN materials have provided greater opportunity for manufacturers to fabricate devices

with smaller size and better FOM (input charge × on-state resistance) for a given breakdown voltage [9].

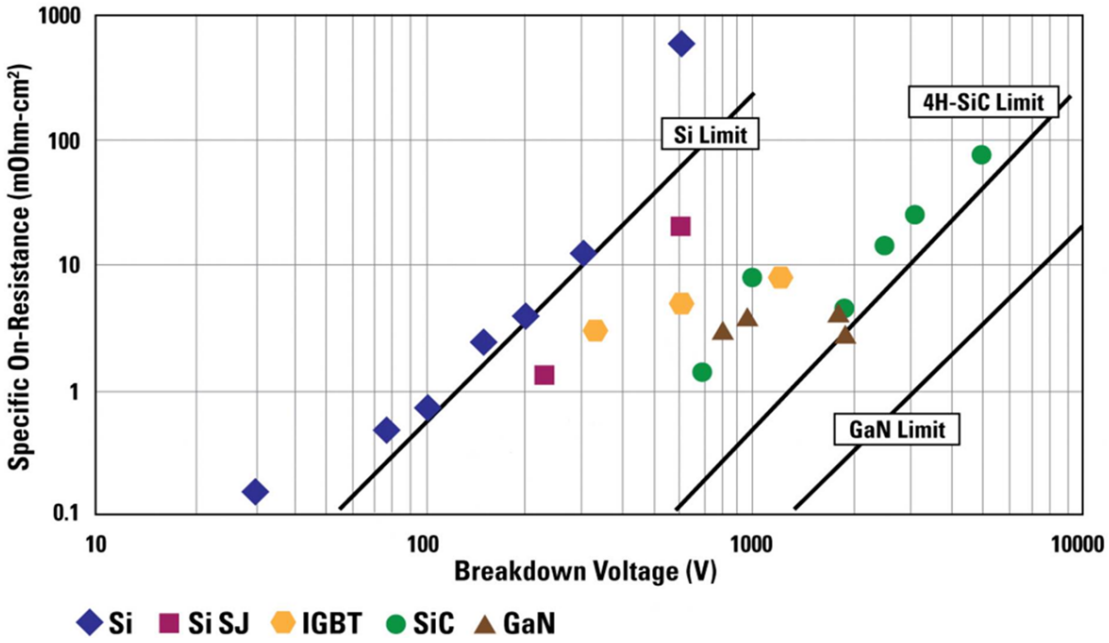


Fig. 2.2. Specific on-resistance vs breakdown voltage for Si, SiC and GaN commercial products and the material one-dimensional limits [9]

A number of commercial WBG power products have been released in recent years and demonstrated very attractive electrical characteristics.

The SiC Schottky diode was the first commercialized SiC power device. The Infineon-IDW15S120 was released in 2001, which successfully extended the breakdown voltage limitation of 200 V for Si Schottky diodes to above 1 kV [10]. The SiC diode is a majority carrier device, and does not have reverse recovery phenomenon. On the other hand, a SiC diode has a higher forward voltage drop than a Si Schottky diode due to the larger band-gap energy, causing higher conduction losses. However, the forward voltage drop shows a positive temperature coefficient, making it suitable for parallel connection [11].

The SiC JFET was commercialized in 2008 by SemiSouth [12]. Although the SiC JFET is easier to implement and has a better gate oxide-semiconductor interface quality than a SiC MOSFET, the normally-on feature in the early devices made it undesirable due to fault protection issues [13]. A cascode configuration with a low-voltage normally-off Si-MOSFET can be used to address this issue. A cascode 1.2 kV SiC JFET was released in 2012 [14].

The SiC MOSFET was first introduced by Cree (Wolfspeed) in 2011 [15]. The initial concerns around the SiC MOSFET such as gate instability and junction robustness at high temperature were quickly overcome in the following years as Cree released their third generation 1.2 kV SiC MOSFET [16]. In addition, major manufactures such as Infineon, STMicroelectronics, ROHM have also developed their own 1.2 kV SiC MOSFET models since 2012 [17]. Up to now, SiC MOSFETs rated at 1.2 kV /90 A and modules rated up to 1.7 kV/225 A are commercially available [18].

Apart from the reduced die size and low parasitic capacitance, SiC MOSFETs also have compelling advantages in terms of the on-state resistance at elevated temperatures due to the wide bandgap, for example only a 20% increase in the DC resistance occurs when the junction temperature increases from 25℃ to 135℃, whereas that of the Si MOSFET increases by 250% [13]. Also, the gate leakage current of SiC MOSFETs remains at a very low level with elevated temperature, whilst that of Si MOSFETs can increase around 100 times when the junction temperature increases from 25℃ to 135℃ [13]. The body diode of SiC MOSFETs normally has a forward voltage drop of around 3 V which is five times that of Si MOSFETs, however the reverse recovery time is much smaller [19].

SiC BJTs became available in 2012 from Fairchild and are currently mainly available from GeneSiC [20]. 1.2 kV/100 A discrete models and 1.2 kV/160 A modules have now been released by GeneSiC. The SiC BJT provides the lowest specific on-resistance, therefore has the smallest chip size and parasitic capacitance for a specific voltage and current. It also has no oxide layer and is capable of operating at a high junction temperature of up to 175℃ [21]. However, as it is a current-controlled device, the SiC BJT tends to a have high driving loss. A current gain of 50-70 was typical in the commercial SiC BJT from Fairchild [13].

The GaN high-electron-mobility transistor (HEMT) was first introduced commercially as a depletion-mode (normally-on) transistor, and was released as an enhancement-mode (normally-off) device in 2009 [22]. The first commercial GaN switch rated at 200 V/3 A was produced by Efficient Power Conversion (EPC) in 2012 [23]. Significant progress has been made since then and a wide range of GaN HEMTs is now commercially available up to 650 V.

Some major GaN device manufacturers and their GaN devices are listed as follows.

Efficient Power Conversion Corporation (EPC) was the first company to introduce the concept and commercialize enhancement-mode GaN power transistors. The company now provides a wide range of GaN FETs (eGaN) and ICs up to 300 V. The third generation eGaN offers the conduction figure of merit of 8.5 nC ×10 mΩ [24].

Panasonic has released a series of enhancement mode 600 V GaN transistors rated up to 26 A, namely X-GaN, providing a figure of merit of 32 nC ×70 mΩ. The company claimed that the new X-GaN products have very low gate leakage and are current-collapse-free due to an additional p-GaN plate near the drain [25].

Infineon has released 400 V and 600 V enhancement-mode GaN transistors rated at up to 31 A with a figure of merit of 4.5 nC ×70 mΩ for the 400 V device and 5.8 nC ×70 mΩ for the 600 V device [26].

Transphorm has produced a series of 600 V GaN devices in cascode configuration up to 47 A. The latest product TP65H035 offers a figure of merit of 9 nC ×35 mΩ [27].

GaN Systems offers 100 V and 650 V GaN power transistors rated up to 60 A, which is the highest current in the market. The device has a figure of merit of 12 nC ×25 mΩ and an ultra-low device parasitic inductance due to the special packaging technique [28].

Other manufacturers such as Cambridge Electronics, Exagan, MicrogaN, Nexperia have also been developing GaN transistors at similar or higher ratings with better performance and lower cost [29-31].

Up to now, most of the GaN manufacturers have focused their development effort on the transistors below 1 kV, as SiC MOSFETs currently dominate the market of 1.2 kV and above. However, some SiC manufacturers such as STMicroelectronics and ROHM have extended their device portfolio to 650 V/100 A, leading to competition with GaN HEMTs in the medium voltage market [32, 33]

2.2.3 Structure of GaN power devices

Unlike SiC or Si MOSFETs, the commercial GaN HEMTs have a lateral structure, shown in Fig. 2.3. The two-dimensional-electron-gas (2DEG) formed between the AlGaN and GaN heterostructure interface has a high concentration of electrons, providing a very low on-state resistance and high current density. To make a good ohmic contact between the

electrodes and 2DEG, recess etching is conducted to allow the ohmic electrodes to pierce through the AlGaN layer creating a short circuit until all the high mobility electrons in the 2DEG layer are depleted [34]. Therefore, a negative voltage on the gate with respect to drain and source electrodes is required to deplete the electrons and turn off the device. However, the depletion-mode transistor is not well suited to many converter applications, and may cause short circuit faults during start-up or under abnormal conditions.

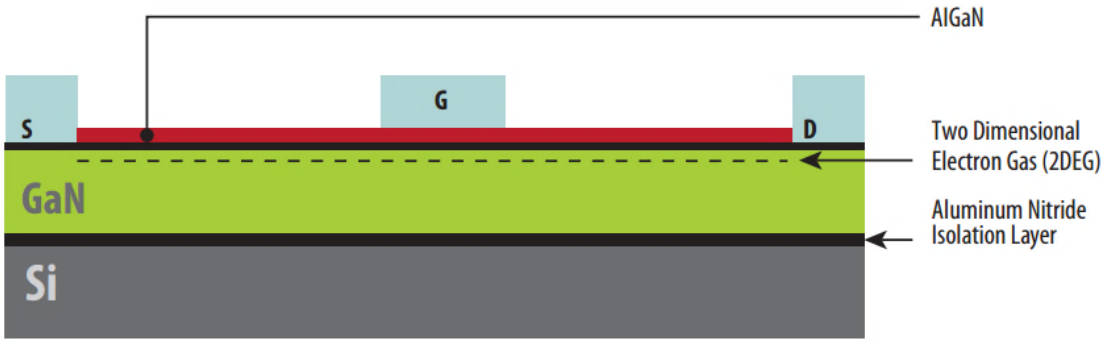
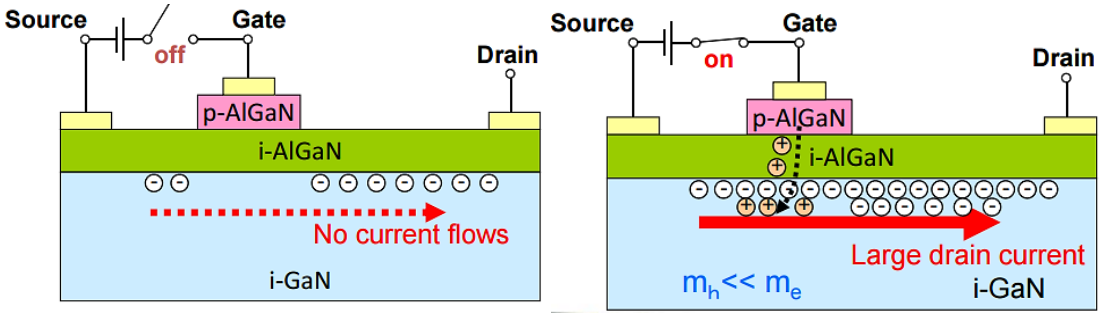


Fig. 2.3. Basic structure of GaN HEMT from EPC [34]



(a) (b)

Fig. 2.4. Normally-off GaN HEMT using GIT at (a) off-state and (b) on-state [35]

To achieve normally-off behaviour, several methods have been proposed. The approach adopted by EPC and Panasonic is the GIT (gate injection transistor) technology – applying a processed gate electrode with p+ extension. As shown in Fig. 2.4 [35], at a gate-source voltage of 0V, the acceptors in the Schottky-type gate metal deplete the 2DEG of the transistor channel and no drain current flows. When the gate-source bias is higher than the threshold voltage, holes from the p-AlGaN are injected into the channel and produce a large number of electrons. The electrons then flow to the drain electrode with high mobility under the drain bias, resulting in a high drain current, whilst the holes stay around

the gate due to their low mobility. The drawback of this method is that the threshold voltage is quite low, normally around +1V (similar to the forward bias voltage of a p-n junction) [36]. Some additional process and surface treatments have been proposed to lift the threshold voltage to around +3V [37-40].

Another widely adopted approach is the cascode configuration in which a depletion mode HEMT is connected in series with a low voltage normally-off Si MOSFET, shown in Fig 2.5. Several generations of commercial cascode GaN transistors up to 600 V are currently available. As the cascode device is controlled via the Si MOSFET, it has the benefits of a robust gate with high threshold voltage and a good compatibility with common Si MOSFET driving solutions. However, the packaging of current commercial cascode GaN transistors causes relatively high parasitic inductance effects. Advanced packaging techniques such as the chip-on-chip technique are therefore in demand [41, 42]. The configuration also has disadvantages such as the mismatch of the parasitic charge between the Si MOSFET and the GaN transistor, which may lead to additional losses and reliability degradation [7, 42].

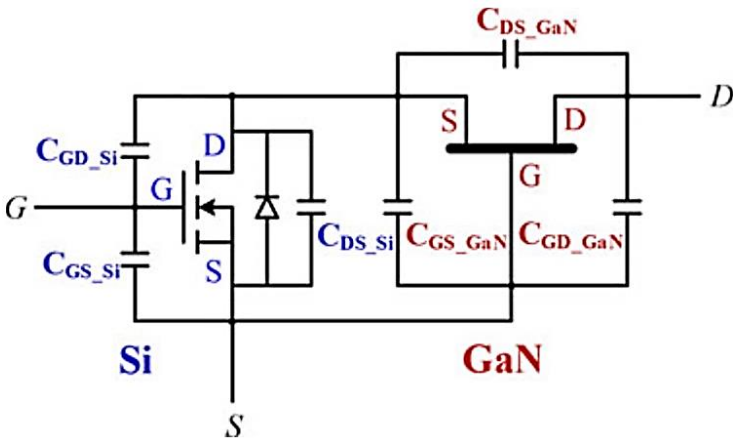


Fig. 2.5. Schematic of cascode GaN transistor [41]

Besides the normally-on nature of the basic GaN HEMT, another limitation to commercializing the technology is that large area and low cost wafers are currently not available. Therefore, unlike SiC devices that are grown on the epitaxial layer of same material, another material is normally used as the substrate for GaN devices without sacrificing too much performance. Si is the most commonly used material due to the low cost and scalability to large diameter processing. However, silicon has a relatively large lattice mismatch with GaN, which can lead to a large number of defects [43, 44]. Applying

an AlN seed layer between the epitaxial layer and the substrate is an effective solution due to the better lattice match between AlN and GaN, which also smooths the rough surfaces and crack formations [45].

Nevertheless, GaN transistors on a GaN substrate remain a long term ambition as this removes the electrical degradation caused by the dislocation (lattice mismatch) and enables the fabrication of vertical GaN transistors which should reduce the leakage current and defect density, and achieve higher breakdown voltage due to the thicker drift region. A comparison of GaN device characteristics on different substrate materials is shown in Table 2.2 [46]. NEXGEN has been researching GaN-on-GaN transistors since 2015 and plans to enter a full-scale production for bulk GaN transistors in 2019 [47].

Table 2.2 Property comparison of GaN on different substrates [46]

Device Area → / Carrier Wafer →	GaN / Si	GaN / SiC	GaN / GaN
Attribute	GaN-on-Si	GaN-on-SiC	GaN-on-GaN
Defect Density [cm^{-2}]	10^9	$5x10^8$	10^3 to 10^5
Lattice Mismatch [%]	17	3.5	0
CTE Mismatch [%]	54	25	0
Layer Thickness [µm]	1-2	2-6	> 40
Reliability	Low	Low	High
Device Types	Lateral	Lateral	Vertical & Lateral

The development of the GaN diode has attracted less interest from manufactures, mostly because the SiC diode is mature and well established in the market. Also, a GaN diode using a lateral AlGaN/GaN structure presents a worse trade-off between the turn-off characteristics and forward voltage drop compared to a SiC Schottky-barrier diode due to the high charge density of the 2DEG [48]. Most of the research on GaN diodes is focused on vertical structures, which provide higher breakdown voltage, better thermal performance, and lower charge density in the drift layer than is present in the 2DEG [49, 50]. Similar to the case with transistors, a vertical diode on bulk GaN will have lower defect density and leakage current, and the thicker drift region should increase the breakdown voltage [50]. However, Some GaN-on-Si Schottky diodes with passivation and

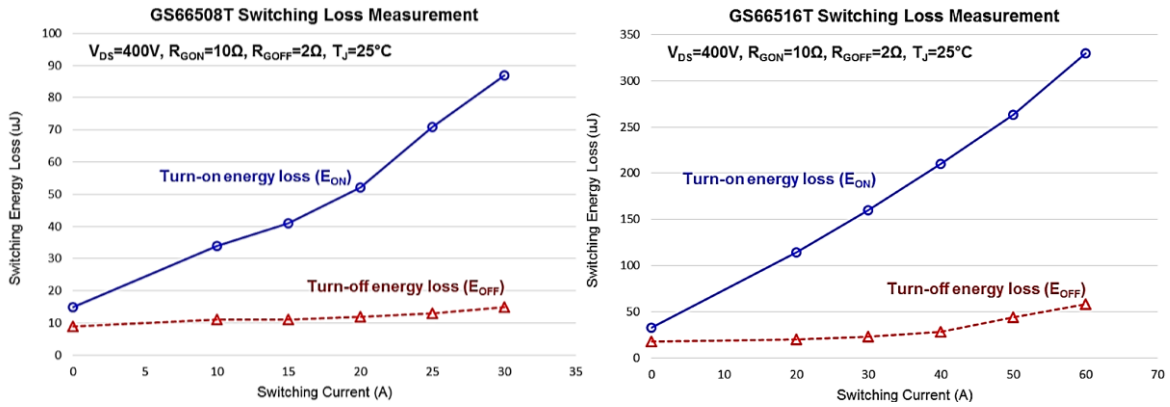
field plate structures have also been demonstrated to exhibit similar performance as bulk GaN-on-GaN diodes [51].

2.3 Characteristics of GaN HEMTs

Due to the superior material property, GaN devices have tremendous potential for enabling high-frequency, high-performance converters. Understanding the characteristics of GaN HEMTs is crucial for exploiting the full device advantages in converter applications.

2.3.1. Switching characteristics

GaN Systems has presented experimental switching test results for their top-cooled 650 V/60 A and 650 V/30 A GaN HEMTs, GS66516T and GS66508T, using a double-pulse-tester (DPT) circuit and a half-bridge synchronous buck converter [52]. The switching losses of the two GaN HEMTS are shown in Fig. 2.6. The total switching loss of the GS66508T, 650 V/30 A, is only around 60 µJ at 400 V 20 A due to the very fast switching speed of 70 V/ns at turn-on and 40 V/ns at turn-off, whilst the switching loss of the GS66516T, 650 V/60 A, is less than 250 µJ at 400 V 40 A.



(a) (b)

Fig. 2.6. Switching losses of the (a) 650 V/30 A and (b) 650 V/60 A GaN HEMTs [52]

The efficiency of a 400-200 V 100 kHz buck converter using the 30 A and 60 A devices operating at 2 kW and 2.4 kW was demonstrated to be above 98.5% and the device junction temperatures were measured to be less than 75℃ with foced-air cooling [52, 53]. The company also released a bottom-cooled version for the 60 A device, GS66516B, and demonstrated its performance in a 400-200 V 80 kHz buck converter using an insulated-

metal-substrate (IMS) half-bridge module. A full-load efficiency of 98.8% was achieved with a device maximum junction temperature of less than 65 ℃ [54]. The thermal configuration for the top-cooled device mounted on a PCB and the bottom-cooled device with an IMS board is shown in Fig. 2.7 [52, 54].

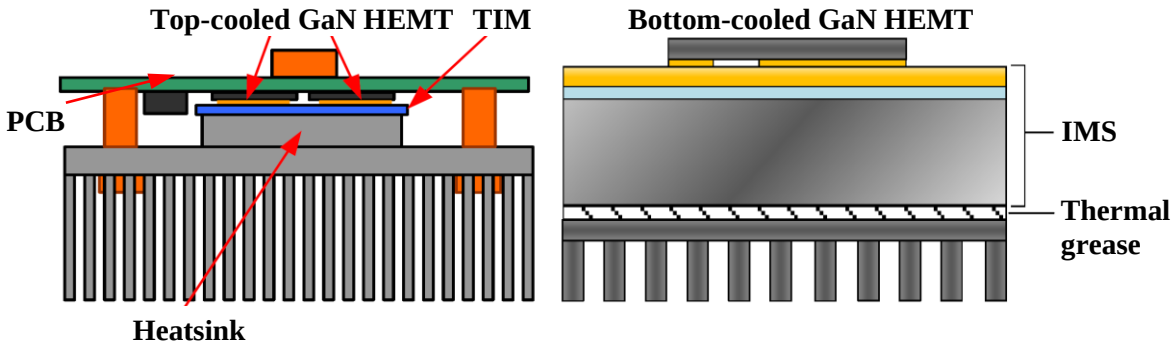


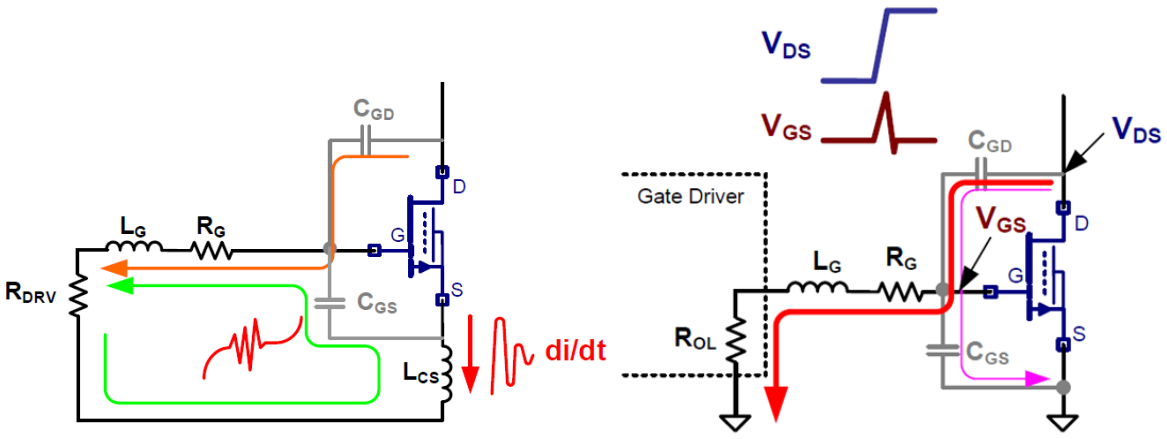
Fig. 2.7. Thermal management of the (a) top-cooled and (b) bottom-cooled GaN HEMTs [52, 54]

The switching characteristic of a 600 V/2 A vertical GaN-on-GaN chip was evaluated in [55]. A turn-on speed of 70 V/ns and turn-off speed of 33 V/ns were demonstrated when switching at 450 V 2 A, which resulted in energy losses of 8.1 µJ and 3 µJ respectively.

A 600 V/ 15 A cascode GaN transistor from Transphorm was characterized in [56]. The switching speeds during turn-on and turn-off at 400 V 10 A were measured to be 87 V/ns and 43 V/ns respectively, resulting in a total energy loss of 70.6 µJ. It was also demonstrated that replacing the upper GaN device with a SiC diode in the DPT circuit reduced the total switching loss by 21 µJ due to the smaller output charge of the freewheeling device.

2.3.2. PCB Design considerations

Although the fast switching speed of GaN HEMTs has reduced the switching energy loss significantly, the effects of circuit parasitic components tend to be magnified under high di/dt and dv/dt. Furthermore, E-mode GaN devices normally feature a low threshold voltage and narrow gate voltage range, which makes the device more vulnerable to gate oscillations [57]. Therefore, an optimised PCB layout controlling the parasitic effects is required to realize the benefits of GaN devices in converter applications.



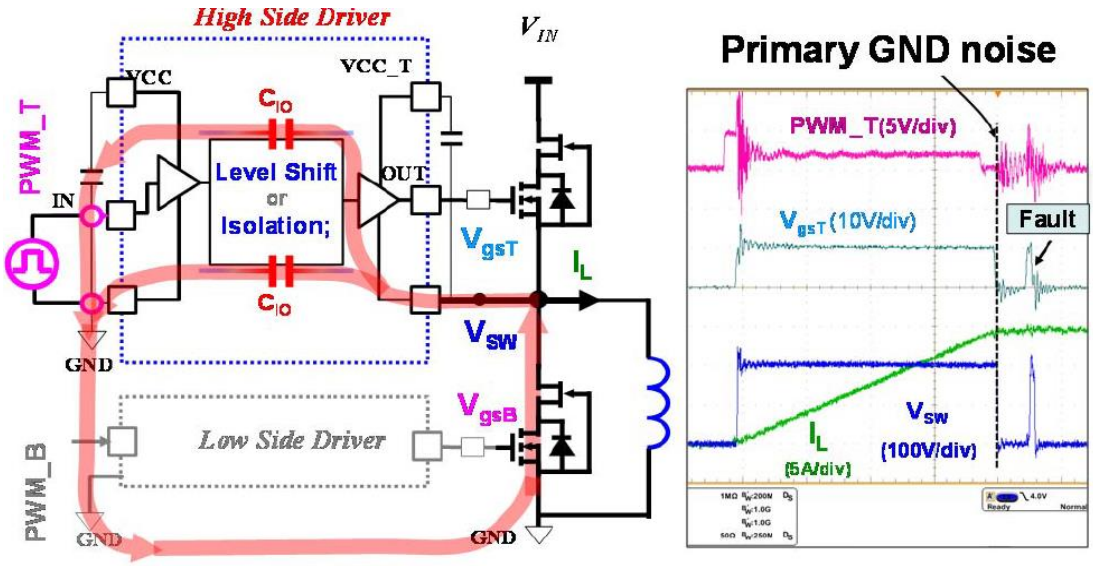
(a) (b)

Fig. 2.8. The effects of high (a) di/dt and (b) dv/dt on GaN HEMTs [58, 59]

The influence of di/dt is illustrated in Fig. 2.8 (a) [58]. During the switching transients, the gate capacitance is charged/discharged and resonates with the gate loop inductance L_G. The induced oscillations may cause the gate source voltage to exceed the threshold voltage or even the gate voltage limit, leading to current shoot-through or device damage. As the common source inductance L_{CS} shares the current path with the power loop, it also reflects the change in the drain current and induces voltage oscillation in the gate loop, which has severe effects under high di/dt.

The effect of dv/dt is also referred to as the Miller effect, and is illustrated in Fig. 2.8 (b) [59]. The turn-on of the high side device causes a fast voltage change at the switching node, which creates a capacitive coupling current through the Miller capacitor C_{GD}, marked in red and purple lines. This coupling current can induce voltage in the gate driving circuit, which may cause gate voltage oscillations or false turn-on of the low side device.

As the Miller effect can have a severe impact on GaN devices due to the high dv/dt, manufacturers have attempted to optimise the Miller charge ratio (Q_{GD} /Q_{GS}) to mitigate the risk. It was demonstrated in [60] that a Miller ratio of less than one can theoretically guarantee dv/dt immunity. In addition, it can be seen from Fig. 2.8 (b) that low gate loop stray inductance, a small turn-off gate resistor and driver pull down resistor will improve immunity to the Miller effect. Therefore, a driver with separate outputs for turn-on and turn-off, and a low pull-down resistance is desirable for driving GaN devices.

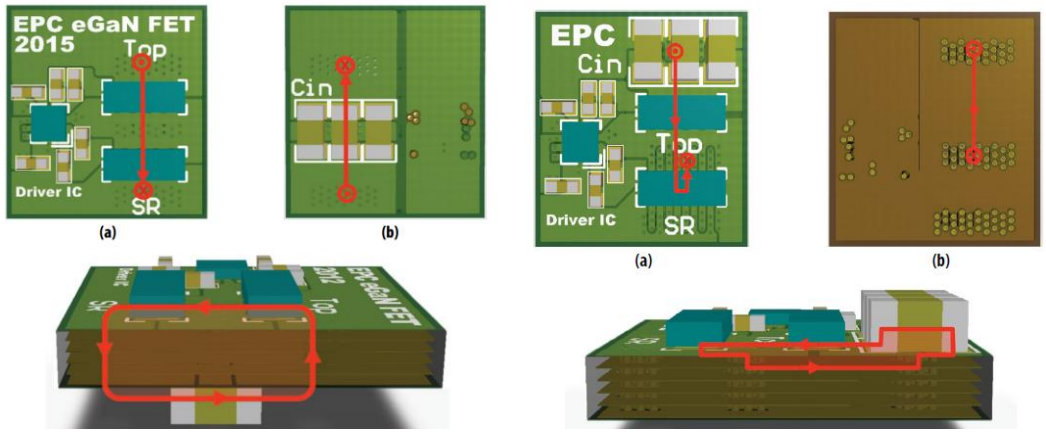


(a) (b)

Fig. 2.9. (a) Common mode noise mechanism due to high dv/dt and (b) its effect on the driving signals [61]

Besides the Miller effect, high dv/dt can also couple capacitive current between the switching node and driving ground. The physical overlap between the switching node and ground planes therefore needs to be avoided in the PCB. In addition, capacitive current can also be coupled through the input-output parasitic capacitance of the gate driver isolation barrier noted as C_{IO} in Fig. 2.9 (a), which may generate significant common mode noise on the primary ground at high dv/dt and trigger unexpected switching events, as shown in Fig. 2.9 (b) [61]. Therefore, an isolator or isolated power supply with high common mode transient immunity (CMTI) is required for driving GaN devices.

To achieve a compact PCB layout for the gate and power loops which minimises the stray inductance and voltage oscillations, a vertical loop design has been shown to be an effective approach. An example is presented in Fig. 2.10 (a). The vertical PCB design using a multi-layer PCB was proposed by EPC which further reduces the loop size and enables an ultra-low stray inductance, shown in Fig. 2.10 (b) [62].



(a) (b)

Fig. 2.10. PCB layouts with (a) vertical loop and (a) multi-layer vertical loop [62]

Another design example using a multi-layer PCB was proposed by GaN Systems, shown in Fig. 2.11 [63]. An interleaved high frequency current is created in the two adjacent PCB layers as marked in green and red, resulting in the magnetic flux cancelling and reducing the stray inductance.

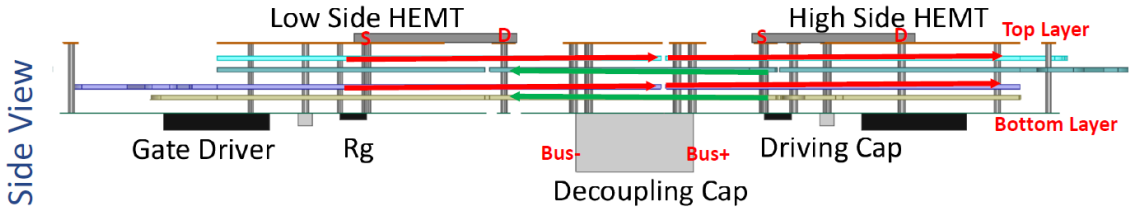


Fig. 2.11. Multi-layer PCB layout design with flux cancelling effect [63]

2.3.3. Dynamic on-resistance

Dynamic on-resistance or current collapse refers to the increase of the on-state resistance of a GaN transistor after a period of high voltage stress during the off-state. The increased resistance reduces back to the DC value after a short period of conduction.

A. Dynamic on-resistance mechanism / trapping effect

The mechanisms of the phenomenon were reported in [64-66]. It is generally attributed to the injected electrons from the gate metal, supplied by the gate leakage current in the off-state. The electrons are then captured by the traps located at the AlGaN barrier surface, AlGaN/GaN hetero-interface, or inside the AlGaN barrier, passivation layer, GaN buffer

and substrate. The electrons are most likely to be trapped near the gate towards the drain where a high electric field occurs. These charges will act like a “virtual gate” but with a negative potential and will tend to deplete the 2DEG, resulting in the increase of the on-state resistance.

It was reported in [64] that the trapping effect at the AlGaN surface has the most direct influence due to the higher defect density at the surface, caused by the improper passivation of the material surface. Another important contribution is the trapping of the electrons which are injected from the gate metal into the AlGaN barrier or into the GaN buffer [67]. Furthermore, the electrons can pass through the buffer layer and eventually get trapped in the substrate. Some of the electrons can also hop from the AlGaN barrier to the trap states located within the passivation layer. Some research also indicated that the trapping can be triggered by the presence of hot electrons in the channel which are detected during the “semi-on state” or the “high power state” rather than the off-state [68, 69]. Due to the high instantaneous power, some electrons may achieve enough kinetic energy to be injected towards the AlGaN barrier or GaN buffer and eventually get trapped. Fig. 2.12 shows where the trapping mechanism may occur in an E-mode GaN HEMT.

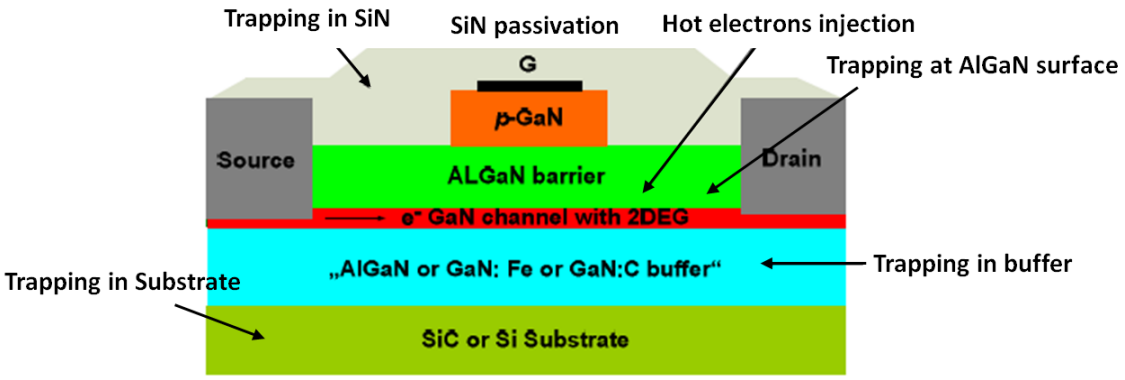


Fig. 2.12. Trapping mechanism in GaN HEMT [64]

The increase in the on-state resistance gradually recovers due to the detrapping mechanism. It was stated in [68-70] that there are at least two mechanisms that dominate the detrapping process depending on the trapping locations. One is a faster, temperature dependent process which is related to the shallow traps located in the AlGaN barrier but very close to the channel. The other is a significantly slower, temperature independent process which corresponds to the deep traps at the surface, buffer, substrate or passivation layer. It was

demonstrated in [68, 69] that the time constants of these two detrapping processes can be in the micro-seconds and seconds time scales respectively.

B. Test method

The measurement of dynamic on-resistance can be challenging since the drain to source voltage swings between hundreds of volts and milli-volts across a switching transient. An auxiliary clamp circuit is normally required to limit the measured drain to source voltage to a reasonable range to avoid the measurement errors caused by overdriving the oscilloscope channel, or the loss of accuracy due to insufficient scale range. In addition, the dynamic on-resistance measurement must take place as soon as possible after the device turns on to be representative of high frequency operation. Therefore, the clamping circuit should have a good dynamic response and a short settling time.

The power device analyser/curve tracer B1505A from Keysight Technologies has a function for dynamic on-resistance measurement. As shown in Fig. 2.13, high voltage power supply HVSMU is used to apply a high-voltage bias up to 3kV in the OFF-state whilst high current power supply HCSMU is used to supply and measure a current up to 20 A in the ON-state. The N1267A enables fast switching between the HCSMU and the HVSMU modules. The HVSMU and the HCSMU modules are synchronized with the device switching from off to on. However, this equipment only allows the observation of on-resistance 20 μs after turn-on [71].

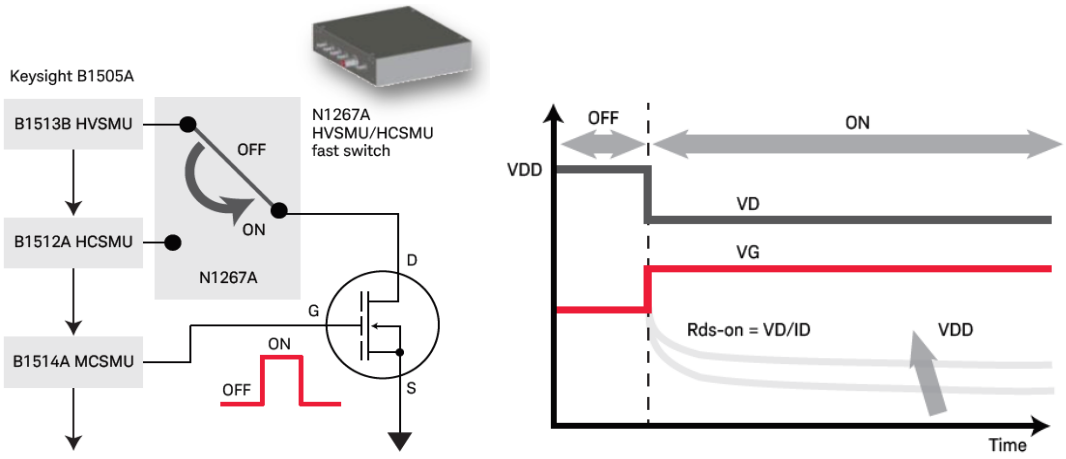


Fig. 2.13. Circuit diagram of Keysight curve tracer B1505A [71]

Candidate voltage clamping circuits were reviewed in [72], shown in Fig. 2.14. Fig. 2.14 (a) is the simplest and uses a Zener diode to limit the measured drain-source voltage. The resistor limits the current drawn from the power circuit to a low value. However, the leakage current through D_2 during the on-state can induce a voltage drop across the resistor, resulting in an error in the measured voltage. Furthermore, the resistor and the parasitic capacitors of the diodes can have a very long time constant. The second circuit, shown in Fig. 2.14 (b), was described in the U.S. patent application 2008/0309355 A1. The gate of the normally-on transistor is connected to a positive voltage source. During the off-state of the DUT, the current flows through the resistor, causing the potential at the source of the transistor to increase until the transistor turns off and the voltage across the gate and source is clamped at V_{CC}-V_{th}. This circuit has a short RC reaction time but it suffers from the voltage overshoot at the turn-off transient of the DUT, which may lead to the failure of the normally-on transistor under the high dv/dt of GaN devices.

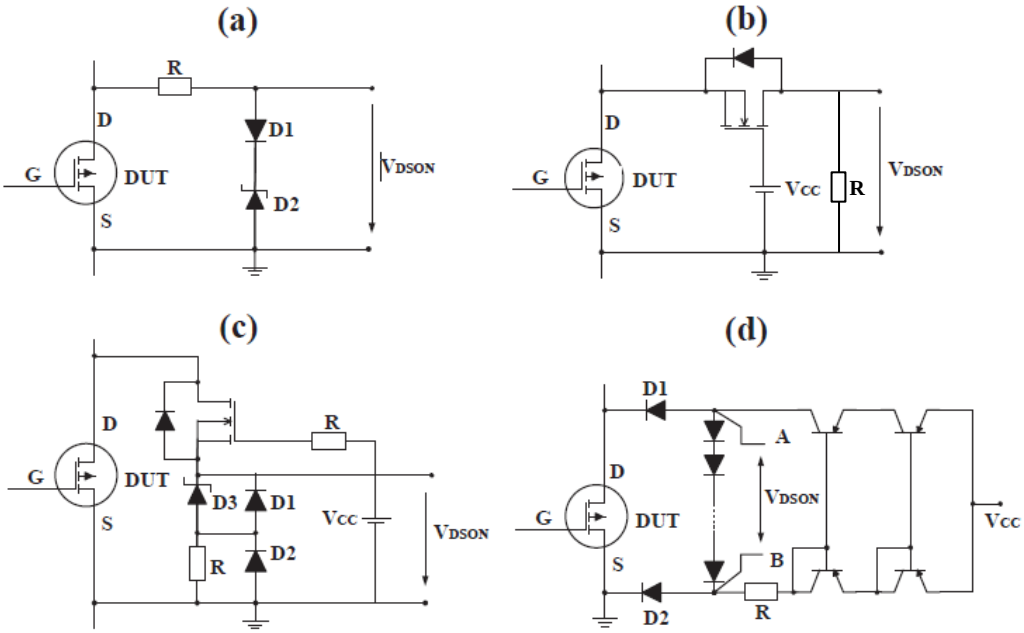


Fig. 2.14. Clamping circuit for dynamic on-resistance measurement [72]

The clamping circuit (c) is a combination of (a) and (b) and was adopted in [73]. It still has the issue of the RC delay caused by the parasitic capacitance of the diodes, which is likely to be the reason why the author only provided the measurement results after 2μs following the turn-on of the DUT. Circuit (d) based on a cascode mirror was used in [74], which demonstrated no significant voltage overshoot and a short RC delay time. The mirror current supplied by V_{CC} flows through D_1 and D_2 during the on-state of the DUT as there

is no voltage bias and flows through a series of Schottky diodes during the off-state. The measurement takes place between A and B where the voltage is clamped at the sum of the voltage drop on the Schottky diodes. The disadvantage of this method is the voltage between A and B has to be measured using a differential probe and the performance may be subject to limited bandwidth. Also, the large number of circuit components may introduce additional parasitic components and influence the accuracy of the measurement.

C. Measurement results of dynamic on-resistance for commercial GaN devices

The dynamic on-resistance of commercial GaN devices has been significantly improved in recent years due to the advances in device fabrication technology, however the effect still imposes challenges for converter design and loss modelling. The GaN device manufacturers have made great effort to quantify the dynamic on-resistance for their devices in the past years.

Recently, GaN Systems has presented measurement results for the dynamic on-resistance for the GS66508T, 650 V/30 A, GaN HEMT [75]. It was demonstrated that the dynamic on-resistance of the GS66508T is independent of temperature. The device was examined in a 200-400 V boost converter for operation at different switching frequencies and load powers. The contribution of the dynamic on-resistance to the device total loss was identified and is summarised in Table 2.3.

Table 2.3 Dynamic $R_{ds(on)}$ contribution to the device total loss at different frequencies and load power [75]

Switching frequency/ Load power		800 W	1200 W	1600 W
20 kHz	Junction temperature	NA	43℃	52℃
	Dynamic $R_{ds(on)}$ loss contribution	NA	14.9%	19.7%
50 kHz	Junction temperature	43℃	51℃	63℃
	Dynamic $R_{ds(on)}$ loss contribution	6%	12.1%	14.3%
100 kHz	Junction temperature	56℃	66℃	85℃
	Dynamic $R_{ds(on)}$ loss contribution	3.0%	6.4%	9.3%
200 kHz	Junction temperature	83℃	103℃	NA
	Dynamic $R_{ds(on)}$ loss contribution	1.2%	3.3%	NA

Two conclusions can be drawn from Table 2.3. First, the dynamic on-resistance loss becomes more dominant with increased power at a certain switching frequency, which is attributed to the increase in loss with current squared. Second, the contribution of the dynamic on-resistance loss reduces with increased frequency at a certain power, because the switching loss becomes the dominant factor at high frequency. Also, as the dynamic on-resistance is independent of the device temperature, its contribution tends to be less at higher junction temperatures due to the increased conduction loss caused by the elevated DC resistance.

A pulse V-I test using a DPT circuit for measuring the GaN Systems device, GS66508T, was reported in [76]. An increase of 49% in the dynamic on-resistance was reported 500 ns after turn-on following a blocking voltage of 400 V for 2 μs. The increase in dynamic on-resistance after continuous switching at 400 V, 8 A with a switching frequency of 250 kHz, 500 kHz and 1 MHz for 100 μs was demonstrated to be 50% , 66% and 82%, respectively. However, the thermal issue was not decoupled from the measurement results, which may lead to an overestimation of the dynamic on-resistance. Another GaN Systems device GS66504B 650 V/15 A was characterized using the pulsed V-I test in [77]. The dynamic resistance increase was demonstrated to be around 40% 1 μs after turn-on following a stress voltage of 400 V for 100 ms. The same device was examined in a 400 V resonant circuit by MIT [78]. The dynamic on-resistance was demonstrated to increase dramatically to around 6.2 times of the nominal DC resistance when switching with a very high frequency of 3 MHz. The device junction temperature was measured to be 80℃.

EPC has also presented dynamic on-resistance test results for their GaN device, EPC2045, 100 V/16 A. An increase of 26.8% and 16% was recorded 50 ns after turn-on following a stress voltage of 100 V and 75 V for 10 μs, respectively [79].

Three EPC GaN devices, EPC 2016C, 100 V/18 A, EPC2034, 200 V/48 A and EPC2047, 200 V/32 A were tested in [80] using a continuous switching test circuit. Increases in on-state resistance of 34%, 149% and 55% were reported for the three devices respectively after continuously switching at 95% of maximum voltage and 50% of maximum current at 120 kHz for 10 ms. The EPC 2025 was characterized in [81] showing an increase of 45% in on-state resistance 2 μs after turn-on following a blocking voltage of 200 V.

2.4 Converter applications of WBG devices for transport applications

The trend to electrify sub-systems in transportation applications has led to an increasing demand for smaller and lighter power converters [82, 83]. In addition, pressure to reduce power converter size has been evident in other applications such as PVs, energy storage systems, telecommunications and wind turbines [84-87].

Increasing the converter switching frequency is an obvious way to minimize size, as the passive components will in theory reduce proportionally. However, several issues such as high switching losses, EMI, control complexity and cost must also be addressed with high switching frequency [88]. WBG devices are a promising candidate for enabling converter miniaturization [82-88]. Significant advances have been reported on the efficiency and power density of converters using WBG technology in recent years. The following sections review the increasing range of power electronic converters that is required for current and future vehicle systems along with the recent advances in converter performance for these applications using WBG devices.

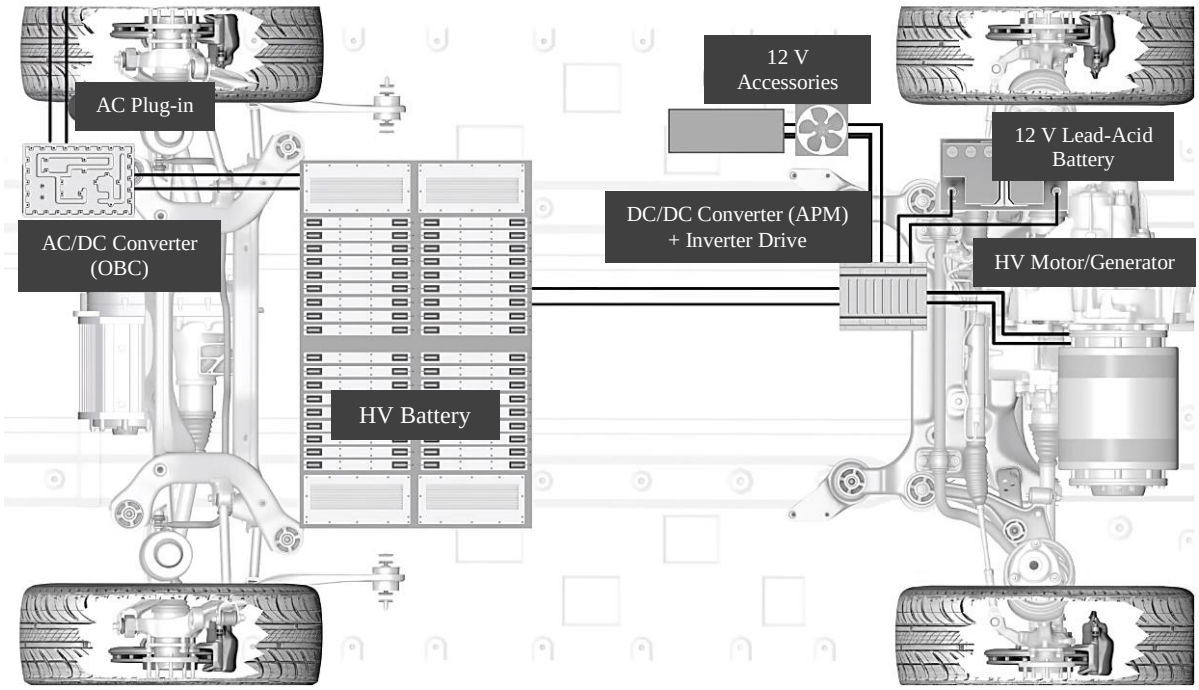


Fig. 2.15. Powertrain of plug-in hybrid electric vehicle (PHEV) [89]

To illustrate some of the main converters required on board a vehicle, the powertrain of a PHEV is shown in Fig. 2.15, which mainly comprises an AC/DC converter used as the on-board charger (OBC), a machine drive inverter and a DC/DC converter serving as the

auxiliary power module (APM). With the increasing power demand due to the additional functionality in EVs such as electric steering, the E-turbo charger and launch assists, a 48 V architecture has started to be introduced, creating a demand for DC/DC converters between 12-48 V [89]. Some high-performance converter applications using WBG technology in a plug-in hybrid electric vehicles (PHEV) are reviewed in detail in this section.

2.4.1. On-board charger (OBC)

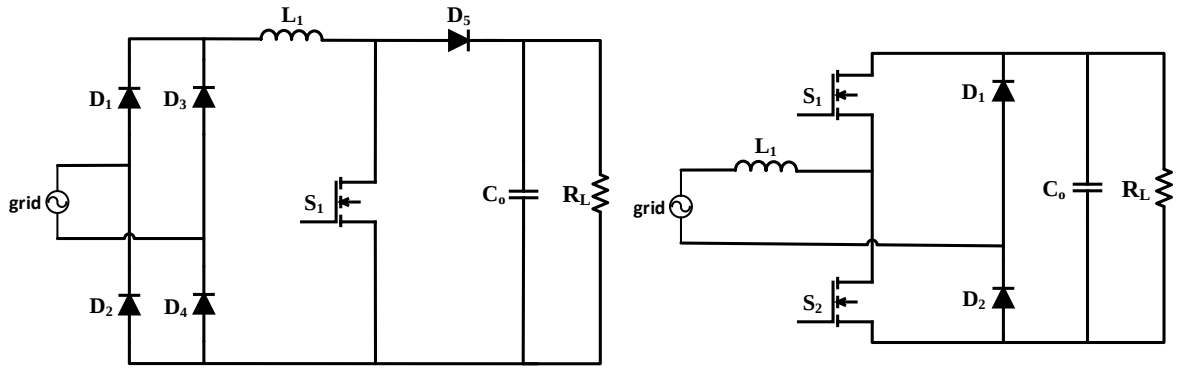
The on-board charger (OBC) provides level 1 and level 2 domestic charging, which requires the conversion of 220 V, 50/60 Hz AC to 250∼400 V DC for the main battery at up to 7.7 kW. Also, there is an emerging requirement for chargers to be bi-directional to enable grid support services to be provided as part of future smart grid concepts [90, 91]. Currently, the state-of-the-art level 2 OBCs in volume production use Si-based technology with a switching frequency of up to 100 kHz, which results in a power density in the range of 3-12 W/in^3 and an efficiency of 92%-94% [92].

As a grid tied application, the OBC should always draw a sinusoidal current in phase with the voltage so that no harmonics are injected into the grid. The two-stage structure is the most widely accepted, where the front-stage AC/DC converter is responsible for power factor correction (PFC) by controlling the grid current and stabilizes the DC link voltage, and the second-stage DC/DC converter is in charge of controlling the output voltage and current for the battery according to the demand of the battery management system (BMS) [93].

A. PFC converters

The conventional single-phase PFC converter comprises a full-bridge rectifier followed by a boost pre-regulator shown in Fig. 2.16 (a), which has the benefits of simple design, high reliability and low cost. However, the converter only enables unidirectional power flow and has high switching and diode conduction losses, which results in bulky heat sinks. The bridgeless totem pole (BTP) PFC rectifier has drawn growing attention in recent years due to its higher efficiency and power density, smaller component count and bi-directional energy flow capability [94]. It consists of a boost inductor, two switches and two rectifier diodes shown in Fig. 2.6 (b). The rectifier diodes can also be replaced by synchronous

MOSFETs. To comply with EMI standards, an EMI filter is normally placed before the boost inductor to minimize the conducted emissions.



(a) (b)

Fig. 2.16. (a) Conventional PFC rectifier and (b) bridgeless totem pole rectifier

However, the conventional Si-based BTP PFC solution has a performance limitation due to the relatively slow reverse recovery speed of the MOSFET body diodes. The high turn-on loss and the risk of cross conduction of the upper and lower MOSFETs due to the slow body diode limit the operation of the BTP PFC to the discontinuous or critical conduction modes, which is not very suitable for high power applications due to the high current ripple and control complexity [94]. A multi-phase interleaved configuration can be used to reach higher power levels, but it introduces more components and adds cost. With the use of WBG devices such as SiC MOSFETs or GaN HEMTs, the BTP PFC can be operated in the continuous conduction mode due to the very low/zero reverse recovery and the fast intrinsic body diode of WBG devices. In addition, higher switching frequencies can be achieved due to the much smaller switching losses, which can reduce the size of the boost inductor and EMI filter.

Major manufacturers such as TI, Cree, Transphorm and GaN Systems have described application examples for BTP PFC converters using WBG technology [88, 94-96]. The main features of these converters are summarized in Table 2.4.

All models were designed to operate in hard-switching CCM at rated power and achieve an efficiency of above 98%. TI, Cree and GaN Systems used WBG devices for the fast switching leg and Si MOSFETs for the rectifier leg to reduce the cost, while Transphorm described an all-GaN solution. TI used three interleaved phases for the fast switching leg

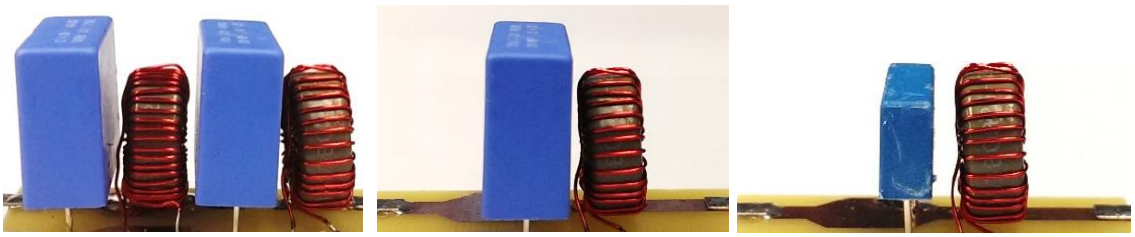
to optimise the efficiency by balancing the device switching and conduction losses depending on the load conditions, known as phase shedding [96]. It can be seen that all the models used a switching frequency of less than 100 kHz, similar to a conventional Si solution, to realize a very high efficiency. The bulky output capacitors used to filter the low frequency AC ripple contributes the most to the total converter volume, followed by the EMI filter.

Table 2.4 Main features of demonstrator PFCs from TI, Cree, Transphorm and GaN Systems [88, 94-96]

Manufacturer	TI	Cree	Transphorm	GaN Systems
Input voltage	85~265 V_{AC}	90~265 V_{AC}	85~265 V_{AC}	176~264 V_{AC}
Output voltage	400~600 V_{DC}	250~450 V_{DC}	385 V_{DC}	400 V_{DC}
Input rated power	6.6 kW	6.6 kW	3.3 kW	3 kW
Switching frequency	100 kHz	67 kHz	100 kHz	65 kHz
Power factor	> 0.99	> 0.99	> 0.98	> 0.99
Peak efficiency	98.9%	98%	98.4%	99.1%
EMI choke	2.5 mH×2	2 mH×2	4 mH×2	1 mH×2
Boost inductor	126 μH	303 μH	554 μH	400 μH
DC link capacitance	900 μF	1125 μF	1880 μF	1880 μF
DC link capacitor configuration	2 in series 14 in parallel	2 in series 9 in parallel	4 in parallel	4 in parallel
Technology	SiC+Si	SiC+Si	GaN	GaN+Si

Several attempts have been made to push the switching frequency of the PFC converter into the MHz range to reduce the size of the passive components. These prototypes are mostly designed for operating in the discontinuous or critical conduction mode with ZVS turn-on to limit the switching losses, where the GaN HEMT is an excellent candidate due to the very small parasitic charge and low turn-off loss. Nevertheless, ZVS turn-on cannot easily be realized in discontinuous mode when the input voltage is larger than half of the output voltage, which can happen periodically in an application such as an on-board charger [97]. Triangular current mode (TCM) control was proposed to address this issue where a variable switching frequency is used to ensure the inductor current is reversed in each cycle to fully discharge the device output capacitance [98].

A 1.2 kW, 1 MHz, interleaved, GaN-based PFC with triangular current mode control was demonstrated using a dual-phase, boost PFC topology [99]. The converter achieved a peak efficiency of 97.9% and a power density of 120 W/in^3 for a conversion ratio of 230 V_{AC} to 380 V_{DC}. It was shown that the EMI filter could be implemented using a one-stage configuration rather than two-stage to realize the same attenuation effect when increasing the switching frequency from 100 kHz to 1 MHz [100]. Fig. 2.17 shows the comparison of the EMI filters for a 100 kHz design, 1 MHz design and 1 MHz design with interleaved operation. Although the EMI filter size has been reduced with interleaved operation, the control of the dual-phase boost PFC converter is more complicated due to the varying frequency. Another 1.2 kW, 1 MHz, GaN-based PFC converter using the bridgeless totem pole topology was demonstrated by the same group, which realized a peak efficiency of 99% and a power density of 200 W/in^3 [101].



(a) (b) (c)

Fig. 2.17. EMI filter for (a) 100 kHz boost PFC, (b) 1 MHz single-phase boost PFC and (c) 1 MHz dual-phase interleaved boost PFC [100]

One of the issues for the bridgeless-totem-pole PFC using TCM control is the switching frequency can become very high at light load conditions and compromise the efficiency. A modified TCM control was presented in [99] and demonstrated in a 3.2 kW, 1 MHz GaN-based bridgeless-totem-pole PFC converter with a power density of 130 W/in^3 and a conversion ratio of 230 V_{AC} to 400 V_{DC}. The converter efficiency was above 97% at 10% load and exceeded 99% from half to full load. Another 3 kW, 1 MHz GaN-based, interleaved, bridgeless-totem-pole PFC converter was demonstrated and achieved a power density of 100 W/in^3 and a peak efficiency of 98.8% [102].

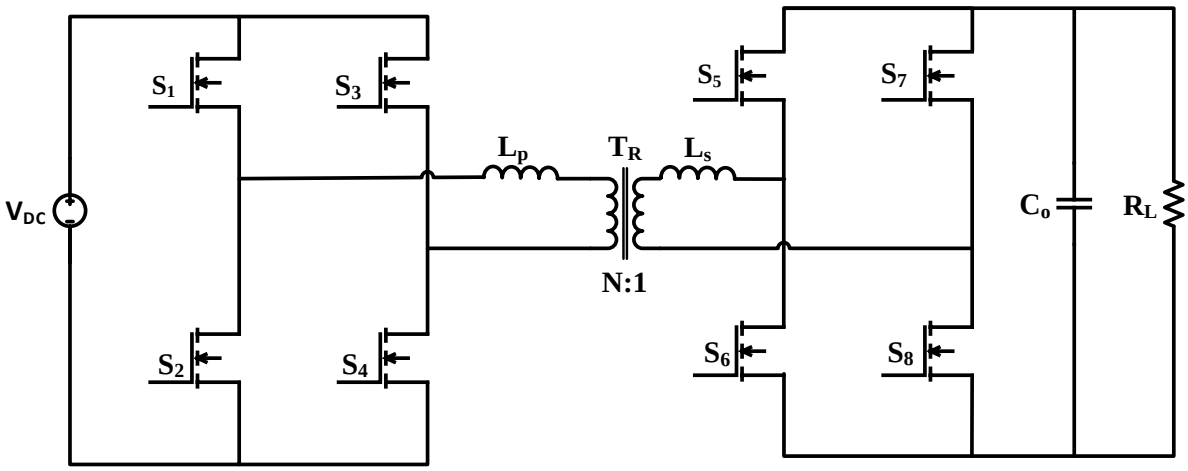
It can be concluded that the GaN-based, bridgeless-totem-pole PFC in discontinuous mode with ZVS turn-on can achieve much higher power density than a commercial PFC in

continuous conduction mode switching at up to 100 kHz with similar efficiency. However the control and design complexity makes it less favoured for industrial applications.

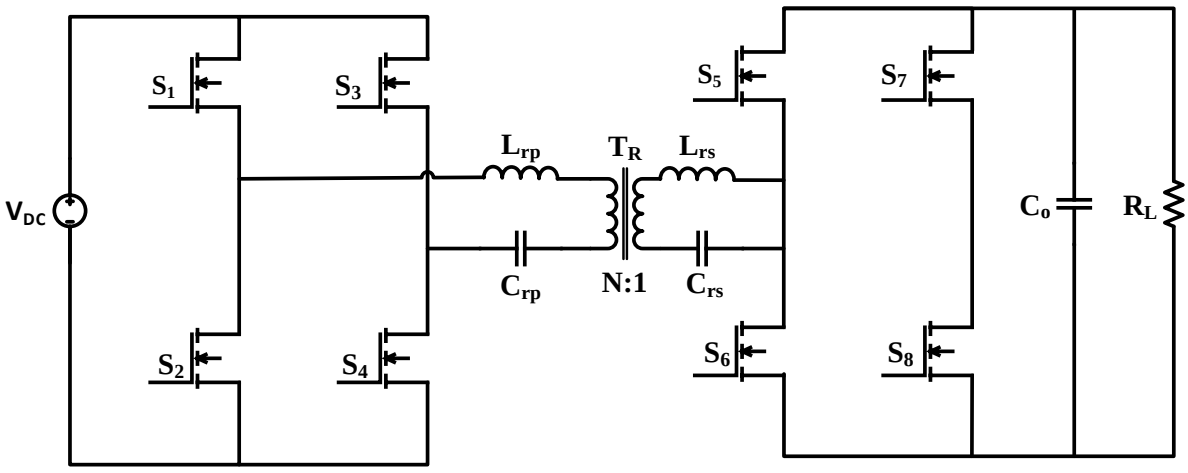
B. Bi-directional isolated DC-DC converters

The DC-DC stage of the OBC converts the output of the PFC converter that is typically 400~650 V_{DC} to the battery voltage of 250~450 V_{DC}, providing galvanic isolation and delivering a power of 3~7.7 kW [103]. With the utilization of the transformer leakage inductance, several isolated DC-DC converter topologies such as the phase-shift, full-bridge (PSFB) and LLC resonant converter have intrinsic soft-switching capability, which helps to enable a high frequency, power dense circuit. However, due to their uni-directional nature, these two topologies are not suitable for future V2G applications [95].

As alternatives, the dual-active-bridge (DAB) and the CLLC converters shown in Fig. 2.18 have been proposed and build on the PSFB and LLC topologies. Both are capable of bi-directional energy transfer and have inherent ZVS turn-on. SiC and GaN devices offer significant advantages over Si MOSFETs for these converters due to their low turn-off loss, fast reverse recovery characteristics, small parasitic charge and low on-state resistance, and have been reported for high-frequency, high-power-density DAB and CLLC converters [90, 94-96].



(a)



(b)

Fig. 2.18. Circuit schematic of (a) DAB and (b) CLLC converters

Cree reported a 6.6 kW CLLC converter for charger applications using SiC MOSFETs, which realized a peak efficiency of 98.1% [95]. One of the challenges for resonant type converters in such applications is the wide range of the battery voltage, leading to large variations in switching frequency. In Cree's design, variable DC link voltage control was implemented instead of variable frequency control to regulate the output voltage, and the converter switching frequency was fixed at the resonant frequency of 200 kHz. This reduced the design and control complexity and increased the overall converter efficiency since the transistor turn-off occurred at a small current equal to the transformer magnetizing current. However, the DC link voltage was boosted to a maximum of 680 V_{DC} by the front-stage PFC to cover the whole battery voltage range, implying that 900 V components need to be used, which is likely to increase the cost and limit the component selection. Also, due to the characteristics of the resonant tank, reverse energy flow can only occur when the battery voltage is higher than 320 V.

In [104], a thorough design study was reported for a 6.6 kW WBG CLLC using variable frequency and variable DC-link voltage control with different WBG devices. A GaN solution was proposed first with a fixed DC link voltage of 400 V and a resonant frequency f_r of 500 kHz, which required a switching frequency f_s of $0.65\sim1.4f_r$ for a battery voltage of 250∼450 V. The peak efficiency of 97.2% was recorded at unity voltage ratio ($f_s = f_r$). To reduce the switching frequency range, a variable DC link voltage of

400~450 V was used, but the improvement was quite limited. To allow a higher DC link voltage, two full-bridge GaN cells on the primary side were connected is series with separate DC link capacitors, which reduced the frequency range significantly. However, the series connection introduced additional conduction losses. The final solution proposed the use of SiC MOSFETs for the primary switches and GaN devices for the secondary switches, which resulted in a peak efficiency of 97.8% and a power density of 43 W/in^3 including the PFC stage. The proposed solutions are summarised in Table 2.5.

Table 2.5 WBG CLLC converters with variable frequency/DC link voltage control [104]

Technology	GaN	GaN	GaN in series	GaN+SiC
Switching frequency	0.65~1.4f_r	0.7~1.37f_r	1~1.07f_r	1~1.07f_r
DC link voltage	400V	400~450 V	500~840 V	500~840 V
Peak efficiency	97.2%	97.3%	97.5%	97.8%

Compared to the CLLC converter with variable frequency and variable DC link voltage, the dual-active-bridge (DAB) converter has a simpler control mechanism by applying phase shift between the primary and secondary switches. However, the main drawback is that the converter may lose ZVS turn-on at light-load conditions, leading to a low light-load efficiency [95]. A comparison of HB (half-bridge)-CLLC, FB (full-bridge)-CLLC, HB-DAB and FB-DAB was presented in [90], based on a 1 kW, 170 kHz 500-300 V SiC prototype. Amongst the four topologies, the CLLC converters showed a relatively flat efficiency curve compared to the DAB converters as ZVS was achieved over the whole load range. HB-based converters presented higher overall efficiency due to the reduced device losses. In addition, the size of the magnetic components in the HB configuration was seen to be smaller, leading to a higher converter power density.

In [105], three 6.6 kW, liquid-cooled DAB converter prototypes for charger applications using Si, SiC and GaN were constructed and compared. It was demonstrated that SiC and GaN-based converters with a switching frequency of 100 kHz showed a higher efficiency than the 40 kHz Si-based converter, but a lower efficiency when switching at 200 kHz due to the increased magnetic components losses and device turn-off losses. However, a significant reduction in the converter volume and weight was still achieved with a switching frequency of 100 kHz. The key performance factors of the Si, SiC and GaN-based DAB converters are summarized in Table 2.6. The GaN-based solution offered the

best power density amongst the three converters due to the small device footprint and top-cooled package. However, it has a higher component count than the Si-based converter.

Table 2.6 key performance factors of the Si, SiC and GaN DAB converters [105]

Converter technology	Si	SiC	GaN
Power (kW)	5.2	6.8	6.6
Switching frequency (kHz)	40	100	100
Volume (L)	1.34	1.02	0.63
Mass (kg)	3.27	2.35	0.69
Power density (kW/L)	3.9	6.7	10.5
Specific power (kW/kg)	1.6	2.9	9.6
Peak efficiency (%)	98.4	99.0	99.0

Another comparison of 7.2 kW DAB converters for the charger application using SiC and GaN was presented in [106]. The two converters showed a similar peak efficiency of around 98%. The reduced transformer size due to the higher switching frequency led to a higher power density for the GaN-based converter, 4 kW/L compared with the 3.3 kW/L for the SiC-based converter. Forced-air cooling was adopted for both converters where the GaN device showed a worse thermal resistance of 2.5 ℃/W over 1.6 ℃/W for the SiC device, and four paralleled GaN devices were therefore required for a single switching cell rather than two paralleled SiC devices to maintain a similar device temperature rise. Nevertheless, it was demonstrated that the GaN-based solution was cheaper than the SiC-based solution.

Transphorm has just published a sample design for a 3.3 kW 100 kHz, GaN-based convection cooled DAB converter [107]. The converter demonstrated a peak efficiency of around 98% for a battery voltage of 350 V and 97% for a battery voltage of 450 V, resulting in a temperature rise of around 50 ℃ in the primary devices. The size of the magnetic components was demonstrated to be smaller than those of a 100 kHz CLLC converter.

2.4.2. Traction drive converters

A six-switch, three-phase inverter is the most common topology for traction drives. A DC/DC converter is sometimes used to boost the battery voltage to the traction inverter

DC-link voltage, which could be up to 700 V. EV traction systems requires a power in the range of 60～100 kW [108]. Therefore, current GaN devices are not suitable for this application, whereas SiC MOSFETs are well-suited as they are largely rated at 1.2 kV and have very good switching characteristics.

A. Non-isolated DC-DC converters

A 60 kW, 75 kHz, 380-600 V SiC-based, dual-phase, interleaved boost converter was demonstrated in [109], realizing a peak efficiency of 98.7% and a power density of 20 kW/L. An inductor and an inter-phase transformer (IPT) were used instead of two separate inductors to minimise the weight and size of the magnetic components. The inductors were potted in an aluminium enclosure mounted on a water-cooled cold plate to provide a good thermal performance. The case temperature rise of the SiC module was measured to be only 18 ℃ due to the fast switching speed and low on-state resistance of the SiC devices. A 12 kW, 90 kHz, 200-400 V, SiC-based, dual-phase interleaved boost converter was demonstrated in [110]. The circuit schematic is shown in Fig. 2.19. A power density of 40 kW/L was achieved by using nano-crystalline, metal tape-wound coupled inductors. However, the inductor core temperature was measured to be 97.8 ℃ due to the poor cooling arrangement, resulting in an overall converter efficiency of 93.8% at 12 kW.

In [111], a 20 kW, 320-600 V, SiC-based, dual-phase interleaved boost converter using forced-air cooling was presented. Soft-switching for both turn-on and turn-off was achieved by introducing an auxiliary circuit, allowing the switching frequency to be increased to 112 kHz while achieving a peak efficiency of 98.8%.

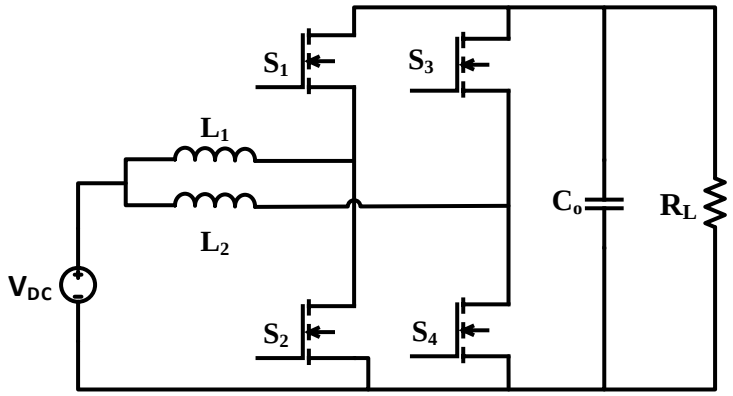


Fig. 2.19. Circuit schematic of dual-phase boost converter

A 17.7 kW, 400-800 V, bi-directional, dual-phase, boost converter using discrete SiC MOSFETs was demonstrated in 2019 [112], which showed a peak efficiency of over 98%. A power density of 55 kW/L and a specific power of 33.3 kW/kg were achieved, which represent state-of-the-art benchmarks for this application. The SiC MOSFETs were directly mounted on the top side of a 3D-printed, liquid-cooled cold plate, which was integrated into the inductor potting compound, so that the inductors and the devices had very effective cooling paths. The dv/dt of the SiC MOSFET was demonstrated to be 30 V/ns, enabling a hard-switching frequency as high as 450 kHz.

B. Motor drive inverters

Conventional EV traction inverters are mostly Si IGBT-based with a relatively low switching frequency. A three-phase inverter drive for a traction motor is shown in Fig. 2.20. However, the maturity of 1.2 kV SiC MOSFETs in recent years has provided very promising alternative solutions for EV motor drives. The superior FOM of SiC MOSFET leads to smaller switching and conduction losses, which potentially increase the inverter efficiency and reduce the size of the cooling system. Air-cooling may be used in some cases instead of liquid-cooling due to the lower losses and the high temperature capability of SiC devices, leading to further system benefits through the removal of the coolant system [113]. Increasing the inverter switching frequency may also be beneficial for reducing the harmonic distortion of the motor drive, which reduces the motor losses, temperature and audible noise [114]. In addition, the relatively slow silicon diode in IGBT modules requires a longer dead time in an inverter leg to avoid cross conduction and current shoot-through, which may cause output current distortion and voltage error [115]. As demonstrated in [115], replacing the silicon IGBT and diode with a SiC MOSFET can reduce the required dead time from 3.5 μs to 0.5 μs, which improved the voltage error from 4.2% to 0.2%. Also, the output torque and flux waveforms are seen to have smaller ripples and a closer correspondence to the references.

A 35 kW, 400 V, all-SiC-based, three-phase inverter with an output line-to-line voltage of 292 V_{rms} at 400 Hz was presented in [116], which reached a power density of 70 kW/L and 50 kW/kg. The converter showed an efficiency of 99% at 35 kW when switching at 25 kHz, demonstrating a loss reduction of around 50% and an efficiency improvement of 8.2% compared to a Si IGBT inverter. The SiC power module was directly soldered onto the heatsink, which used forced-air cooling. Compared to using silicon grease to interface

the heatsink, this method reduced the device junction-to-heatsink thermal resistance from 1.56 ℃/W to 0.58 ℃/W. The estimated junction temperature of the SiC MOSFET was 125 ℃, leaving a safety margin of 50 degrees to the maximum operating temperature. The inverter was used to drive a 1.2 kW PM motor in [117]. It was shown that the motor loss was reduced by 48% by increasing the switching frequency from 25 kHz to 50 kHz due to the lower harmonic distortion and smaller ripple currents, which lowered the winding temperature from 110 ℃ to 86 ℃.

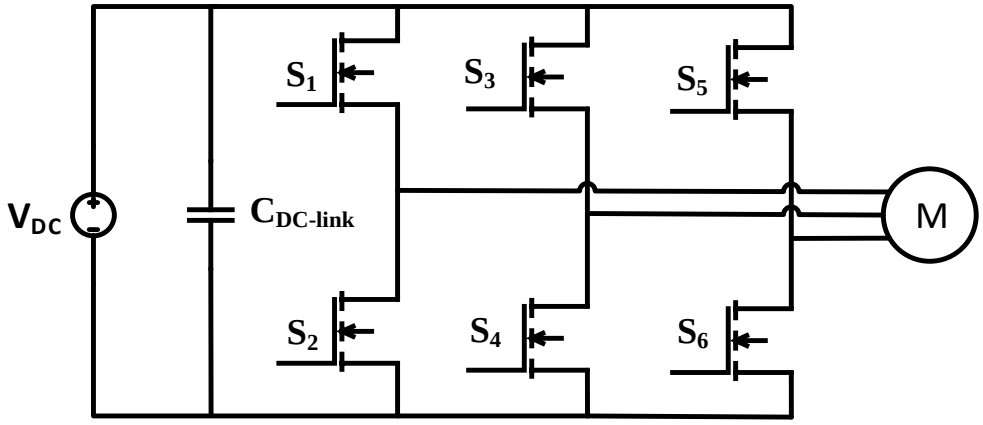


Fig. 2.20. Circuit schematic of three-phase inverter drive

A 100 kW, 400 V, three-phase inverter was demonstrated in [118]. A hybrid module consisting of Si IGBTs and anti-parallel SiC Schottky diodes was used to improve the diode reverse recovery characteristics, which achieved a 70% reduction in the module loss compared to an all-Si power module. A direct cooling method was developed for the hybrid module for better thermal performance. The final prototype with liquid-cooling realized a power density of 14.8 kW/L and a specific power of 10.5 kW/kg. An efficiency of more than 97.5% was achieved at full load conditions. Similar research was conducted in [114], where a relatively low power SiC MOSFET was paired with a Si IGBT to improve the forward and reverse conduction characteristics. Furthermore, the SiC MOSFET could be used as an auxiliary switch to realize ZVS turn-on for the Si IGBT. The proposed hybrid module was demonstrated in a 4 kW, 20 kHz, single-phase inverter and compared with the Si IGBT + SiC diode solution, and was shown to provide a loss reduction of 28% and an efficiency improvement of 0.9% at 4 kW. In addition, the case temperature of the IGBT was seen to reduce from 100 ℃ to 30 ℃ due to the ZVS turn-on and smaller conduction losses.

A highly integrated inverter leg module including the SiC power module, gate drivers, DC link capacitors, a 3-D printed heatsink and a fan was described in [119]. The module was tested in a 5 kW single-phase inverter and achieved an efficiency of over 96% with a switching frequency of 20 kHz. Based on simulation and calculation, the complete 20 kW three-phase inverter using the modular design was predicted to realize a power density of 18.6 kW/L and an efficiency of 99%.

In [120] and [121], a soft-switching, SiC-based, three-phase inverter was proposed and demonstrated at 25 kW. A small resonant inductor was added on the DC side and controlled with a paralleled auxiliary switch to charge and discharge the output capacitance of the main switches. Due to the reduced switching losses, the inverter was able to operate with a switching frequency of 300 kHz while reaching an efficiency of 98.2% at 25 kW. The total volume of the passive components was reduced by 46% compared to a 100 kHz, hard-switching, three-phase inverter, resulting a power density of 9.8 kW/L including the filter inductor. However, the ZVS operation could not be guaranteed with a conventional three-phase inverter PWM control strategy and a space-vector-modulation was proposed to accommodate the soft-switching operation, which greatly increased the design and control complexity.

A 50 kW, three-phase, liquid-cooled inverter using SiC JFETs, was demonstrated in [122], realizing a peak efficiency of 98.5% when switching at 10 kHz and a power density of 8.4 kW/L. Due to the normally-on nature of the SiC JFET, a customized driving circuit with appropriate protection functions was designed and implemented.

2.4.3. Auxiliary power module (APM)

The auxiliary power module (APM) in EVs is responsible for delivering power from the main battery to the 12 V accessories such as LEDs, heating air conditioner, radio and GPS and also to charge the 12 V lead-acid battery. The auxiliary power module typically comprises an isolated unidirectional DC-DC converter [89]. Most APMs are located under the bonnet of the EV to take advantage of the liquid-cooling system. However, space under the bonnet is at a premium and is likely to become more limited as new systems are accommodated such as automatic driving and automatic braking [123]. However, with increasing efficiency, only natural convection or forced-air cooling may be required for the

APM and the unit may be moved from the bonnet area to other places such as under the seats.

The APM converts 400 V to 12 V at power ratings in the range 0.4~2 kW, which is a suitable voltage and power level for GaN devices. Therefore, high performance GaN-based converters can be expected for this application. As many 12 V accessories are user-access applications, galvanic isolation is required for the APM converters. Two bi-directional, isolated DC-DC topologies the FBCLLC and the FBDAB were discussed in section 2.2.1 B, however, these circuits are not well-suited to APM applications. First, as the power level is relatively low, full-bridge topologies are not particularly advantageous due to the device cost. It was demonstrated in [90] that a half-bridge configuration resulted in higher efficiency and smaller magnetic size for a 1 kW, 170 kHz, 500-300 V, SiC-based converter. Second, bi-directional operation is not necessary for APM converters so conventional, isolated topologies such as the LLC converter can be utilized with lower cost and design complexity.

A 1 kW, 380-12 V, 100 kHz, GaN-based, half-bridge, center-tap converter was presented in [124], shown in Fig. 2.21. Low voltage Si MOSFETs were chosen for the synchronous rectifier to reduce the cost. ZVS turn-on of the primary device was lost for a load power below 400 W, leading to a low light-load efficiency. The primary GaN device temperatures were measured to be around 82 ℃ at full load, mainly due to the conduction loss, however the temperature may be improved with a better thermal management.

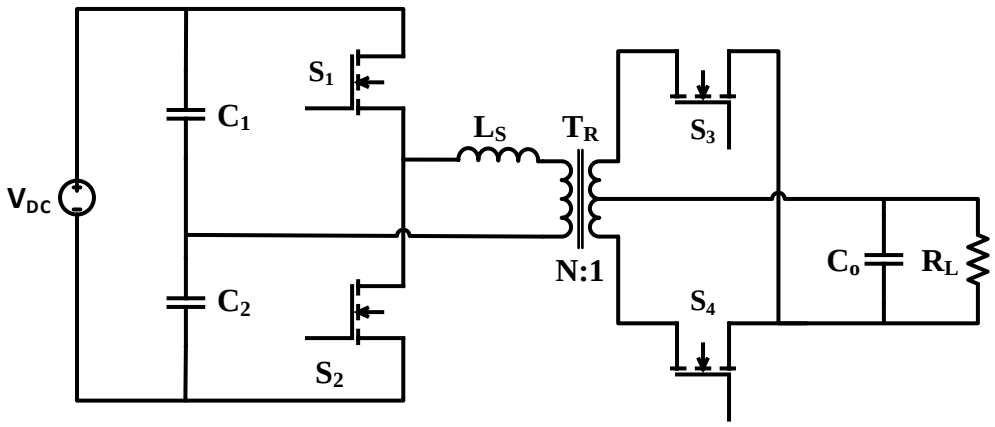


Fig. 2.21. Circuit schematic of half-bridge center-tap DC-DC converter

Compared to full-bridge converters, the half-bridge, center-tap converter imposes twice the voltage on the secondary devices. In addition, the secondary device suffers from an over-voltage transient and ringing at turn off. To address this issue, an active clamp circuit including a low-power Si MOSFET and a capacitor was proposed in [85]. The clamp circuit was connected in parallel with the secondary devices and switched on prior to the turn-off of the main secondary device to supress the voltage transient and to provide soft-switching for the Si MOSFET. The proposed topology was validated in a 1 kW, 400-12 V, 100 kHz GaN-based converter, which achieved a full-load efficiency of 95%, a peak efficiency of 98.3%, and a power density of 1.8 kW/L. The efficiency of the GaN-based prototype was demonstrated to be around 1.2% higher than an equivalent Si-based prototype. At full-load condition, the transformer contributed the most to the total converter loss, followed by the secondary-side device conduction losses.

A 1.5 kW, 500 kHz, 400-12 V, GaN-based, phase-shift, full-bridge (PSFB) converter was demonstrated in [125]. The same active clamp circuit as in [85] was used to supress the voltage overshoot across the secondary devices and recover the resonant energy. In order to address the issue of the loss of ZVS turn-on at light load conditions, a current-doubler-rectifier was proposed for the secondary side. As the output current was divided into two inductors, each inductor current is able to become negative at light load conditions during the freewheeling stage while the rectifier remained in continuous conduction. This negative current was forced to flow through the transformer and discharged the output capacitance of the primary devices in the leading leg. With increased load power, the output inductor current was automatically decoupled from the primary and ZVS of the primary devices was guaranteed solely by the transformer leakage inductance. This method greatly increased the design flexibility, easing the requirement on the leakage inductance and reducing the transformer and duty cycle losses. However, the output inductor losses may be increased due to the large current ripple. The proposed circuit is shown in Fig. 2.22 where S_R and S_C denote the rectifier and clamp switches respectively. The converter can ensure ZVS operation over the whole load range. The final prototype realized an efficiency of over 90% for 200 W, light-load operation and 96% for 1.5 kW, full-load operation, and a power density of 12.5 kW/L.

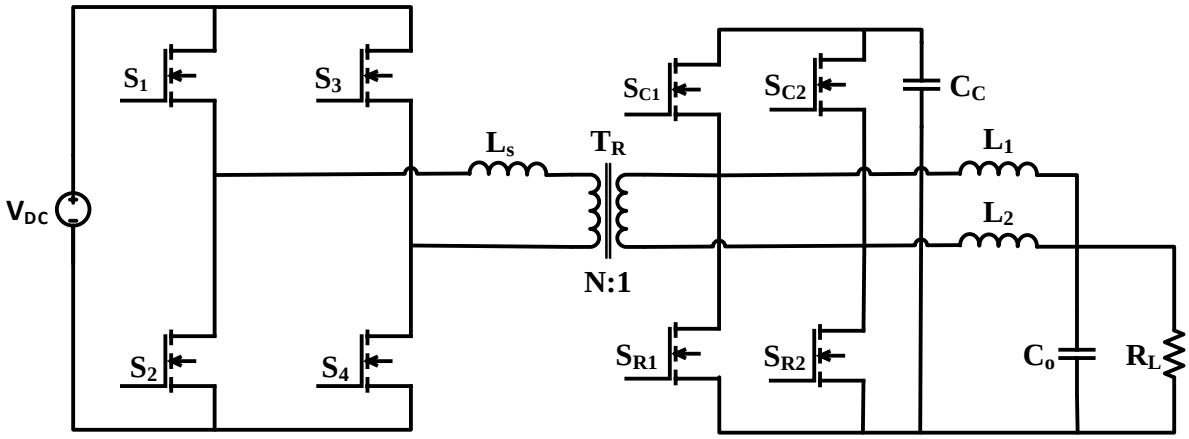


Fig. 2.22. Circuit schematic of active clamp FBPS converter with current-doubler-rectifier

The LLC resonant converter has also been widely studied for APM applications due to the inherent ZVS turn-on and low-current turn-off for the primary devices, and ZCS turn-off for the secondary devices. In addition, unlike charger applications, the APM converter does not have a wide output voltage range, indicating that the modulation range of the switching frequency can be narrowed to around the resonant frequency, which increases the converter efficiency and reduces the control and design complexity. Therefore, the LLC topology has great potential for enabling high performance APM converters.

The GaN device is a very good candidate for the LLC converter due to its high frequency operation capability. A comparison of Si-based and GaN-based 500 W, 380-12 V LLC converters was presented by TI in [126, 127]. A converter loss model was developed and a system optimisation was conducted to select the best resonant inductance, magnetising inductance and resonant capacitance values for a range of switching frequencies and output powers. The results suggested that 325 kHz and 400 kHz were the optimum resonant frequency for the Si-based and GaN-based converters. It was demonstrated that a loss reduction of 19% was realized with the GaN-based solution due to the smaller parasitic capacitance and on-state resistance. The GaN-based prototype achieved a peak efficiency of 97.85% and a power density of 18.7 kW/L.

Despite the benefits of GaN devices, the high RMS current in the secondary devices due to the high conversion ratio still imposes challenges for the uptake of GaN devices in LLC converters for APM applications. To address this issue, a 400-48 V, GaN-based LLC converter with two paralleled, centre tapped, synchronous rectifiers using an integrated

planar transformer was proposed and demonstrated at 1 kW, 1 MHz and compared with Si-based solution [128]. The circuit schematic is shown in Fig. 2.23. The GaN-based design had a magnetizing inductance of 2.5 times larger than the Si-based design and a dead-time of 60 ns shorter, resulting in much lower conduction losses in the primary devices and transformer winding. With the optimised winding arrangement and core shape, the transformer surface temperature was measured to be only 45℃ with forced-air cooling even at 1 MHz. The final prototype achieved a peak efficiency of 97.6% and a power density of 8.5 kW/L.

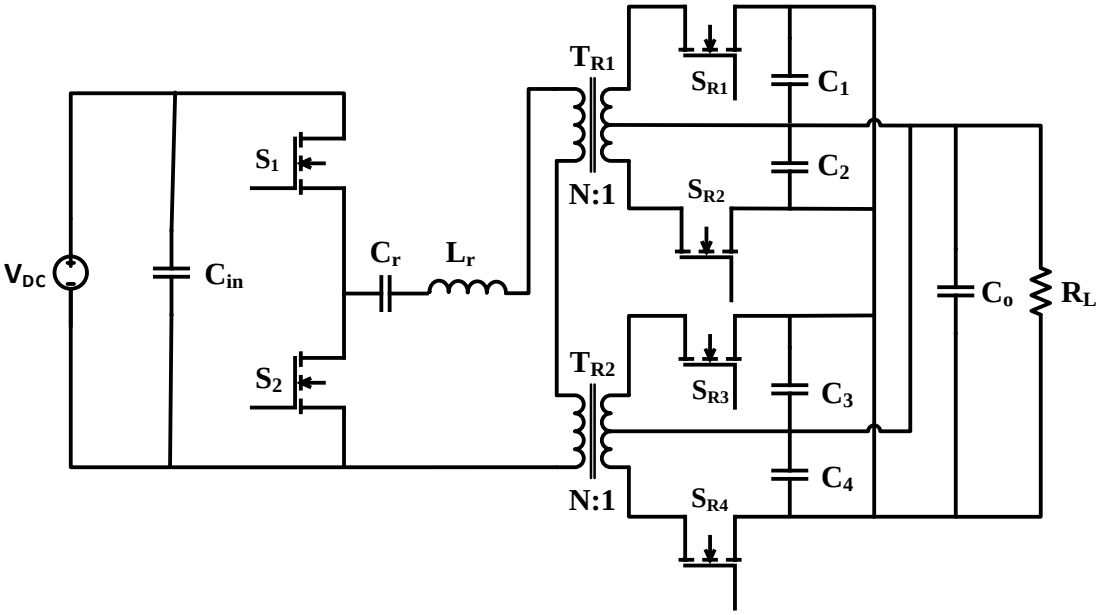


Fig. 2.23. Circuit schematic of LLC converter with integrated transformer

Another GaN-based, 1 kW, 1 MHz, 380-12 V, LLC converter with integrated transformer was demonstrated in [129]. Four paralleled, center-tapped rectifiers were used in the secondary side, which significantly reduced the conduction loss. During the full-load operation, the highest temperature of 68.5℃ occurred on the primary device case, whilst the transformer remained cool due to the optimised design and reduced losses. The converter prototype achieved a peak efficiency of 97% and a very high power density of 42.7 kW/L.

2.5 High-conversion-ratio DC-DC converters

Due to the increasing demand for high step-up/down voltage conversion ratios in transport applications such as 400-48 V, and 270-28 V in electrical vehicles and in aerospace applications, DC-DC converters enabling high conversion ratios have been a research focus. This section reviews the main non-isolated DC-DC converter topologies with inherent capabilities for realizing high conversion ratios.

2.5.1. Cascaded buck/boost converter

The cascaded buck/boost converter consists of multiple, conventional buck/boost converters connected one after the other, and the voltage is stepped up/down stage by stage, for example as demonstrated [130, 131]. The operation principle is straightforward and a modular design can be easily implemented. However, the system efficiency can be low as it is the product of the individual stage efficiencies.

2.5.2. Quadratic buck/boost converter

The quadratic buck/boost converter has a voltage conversion ratio depending on the duty cycle squared, similar to a cascaded buck/boost converter, but it only requires one active switch. A quadratic buck converter is shown in Fig. 2.24. The topology was demonstrated in a 30 W 36-1.5 V, 100 kHz converter prototype, realizing an efficiency of 75% [132].

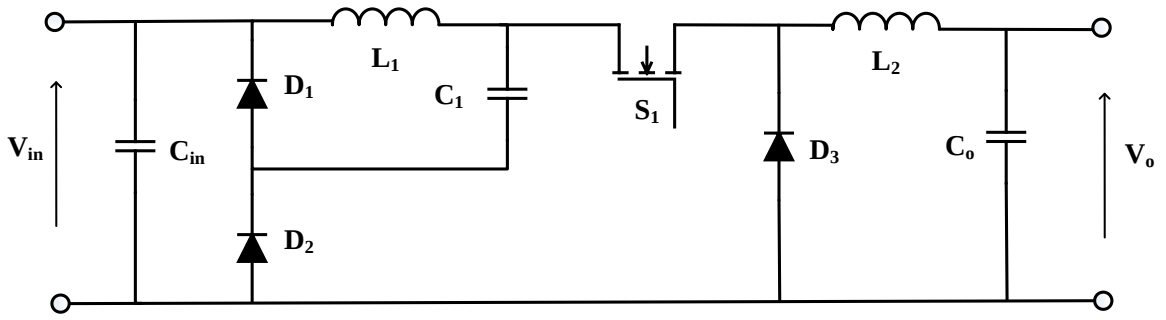


Fig. 2.24. Quadratic buck converter

2.5.3. Switched capacitor/inductor converter

The switched capacitor (SC) and switched inductor (SL) based converter is formed by inserting additional SC/SL cells into conventional converter topologies such as the buck/boost, Cuk, Sepic and Zeta converters [132-134]. The SC/SL are charged and

discharged in each switching cycle to step up/down the voltage. A SL and SC hybrid buck converter are shown in Fig. 2.25. A 36 W, 50 kHz, 12-1.9 V SC buck converter was demonstrated in [133], realizing an efficiency of 89%, which was shown to be higher than that of a cascaded and quadratic converter at the same operating conditions, 85% and 87% respectively.

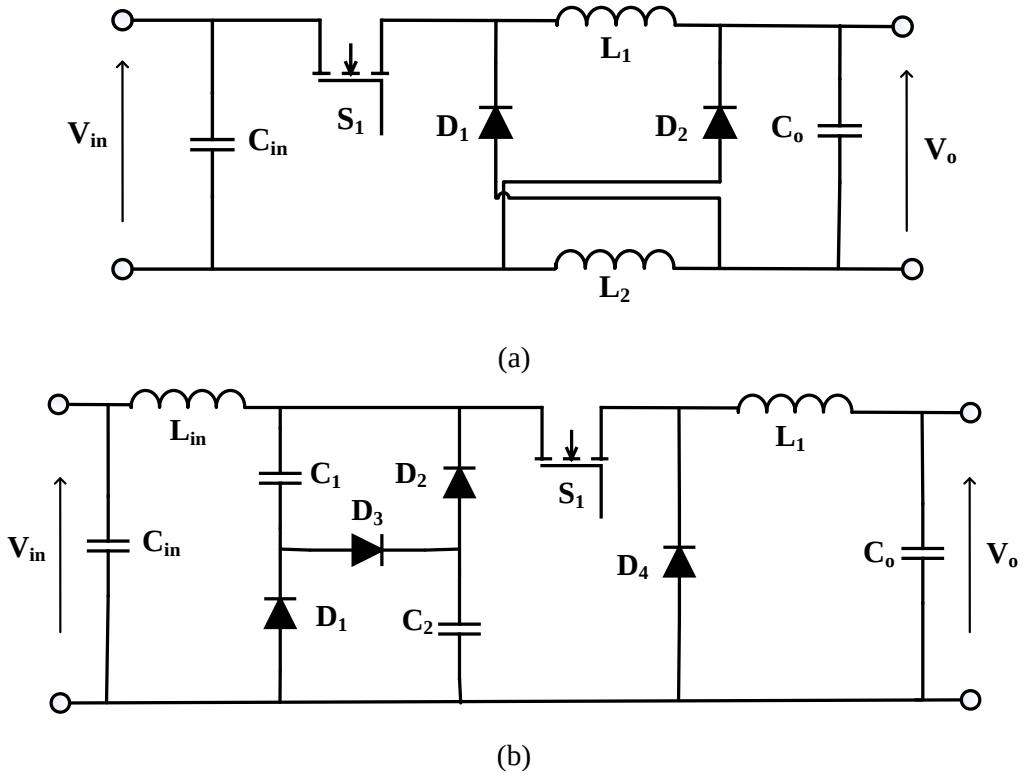


Fig. 2.25. (a) Switched-inductor and (b) switched-capacitor buck converter

2.5.3. Coupled inductor buck/boost converter

Coupled inductors can be introduced into conventional converter topologies to extend the voltage conversion ratio range in a relatively straightforward and low-cost manner. Importantly, an isolation transformer is not required. A coupled inductor buck converter is shown in Fig. 2.26. A 400 W, 50 kHz, 200-24 V bi-directional buck/boost converter using a coupled inductor with a turns ratio of 2:1 was demonstrated in [135], realizing an efficiency of around 93%. However, a voltage overshoot of around 400% was seen during the turn off of the switch due to the leakage inductance of the coupled inductor, which has limited the uptake of this topology.

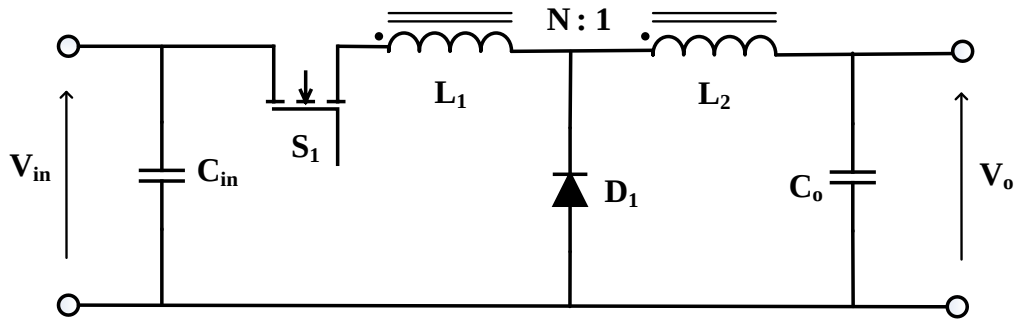


Fig. 2.26. Coupled-inductor buck converter

2.5 Summary of literature review

As Si-based devices are approaching the theoretical one-dimensional material limit, WBG devices are emerging with very promising performance. Taking advantages of the material properties, WBG devices are starting to be manufactured in a small chip size with low on-resistance and low parasitic charge. The SiC MOSFET is currently dominating the 1.2 kV market and above, whilst the GaN HEMT is set to become a very strong contender for applications below 1 kW. GaN HEMTs are mostly fabricated on a Si substrate, however the manufacturers are actively researching the possibility of producing cost-effective GaN devices on purely GaN substrates, which would enable vertical device structures and increased performance.

The GaN HEMTs have a very small resistance and parasitic capacitance, indicating the potential of significantly reducing the device conduction and switching losses. The switching characteristics of the GaN HEMT have been evaluated in recent work and demonstrated to be superior to conventional Si devices. However, many challenges arise associated with the high di/dt and dv/dt. Careful design considerations are required for PCB layout, driving circuit and components selection. Furthermore, the dynamic on-state resistance may be a limitation on the performance of some high-frequency GaN applications.

WBG device converters have been demonstrated to offer performance advantages for EV applications such as on-board chargers, motor drive inverters and auxiliary power modules. Class-leading performance in terms of efficiency and power density has been reported for these and other applications outside the transport sector. Nevertheless, many design challenges remain with regard to the optimum use of WBG devices, including the device

characteristics, the circuit topology selection, the drive circuits and the electrical and thermal interconnections to name just a few.

Chapter 3

Characterization of GaN HEMT

3.1 Introduction

To overcome the lack of detailed data for the early GaN devices that were available at the start of this research project, a programme of work was undertaken to investigate the switching performance and losses, that is the characteristics critical for converter design. However, the much higher switching speeds of GaN devices compared with silicon and the presence of new effects that were not well understood, such as dynamic on-state resistance created a number of challenges. For example, best-practice characterisation techniques were not well-established.

This chapter describes the development of GaN transistor switching test circuits to evaluate gate driver performance, switching behaviour and dynamic on-state resistance. Results are provided for several enhancement-mode devices including the 650 V, 60 A GaN Systems HEMT.

3.2 Measurement of switching characteristics of GaN HEMTs

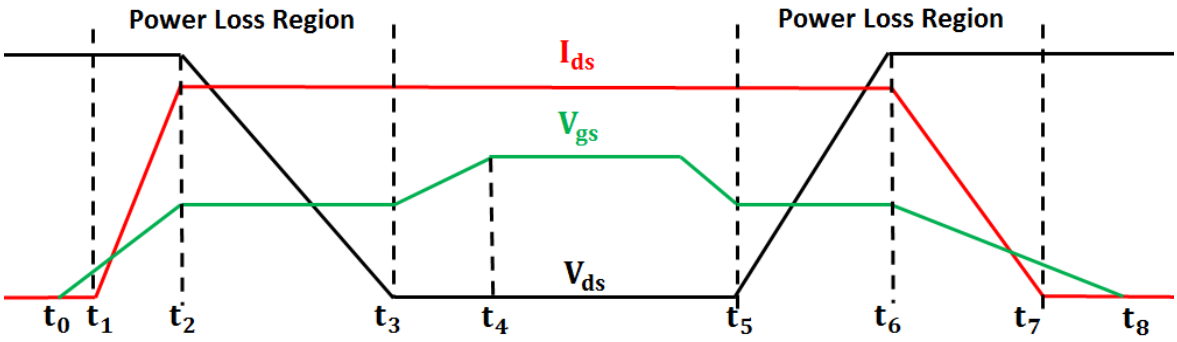
3.2.1 Theory of GaN HEMTs inductive switching

The ideal waveforms for an enhancement-mode GaN HEMTs switching an inductive load are shown in Fig. 3.1.

During t_0~t_1, the drive voltage is applied to the gate of the GaN HEMT and the device input capacitor is charged. The gate-to-source voltage V_{gs} increases until it reaches the threshold voltage at t_1. The period is known as the turn-on delay time. Due to the very low input capacitance of GaN HEMTs, this period is short, meaning a very small turn-on delay time.

During t_1~t_2, the load current starts to increase in the 2DEG channel of GaN HEMT. The gate current continues to charge the input capacitor and the gate voltage V_{gs} increases proportionally to the drain current I_{ds}. The drain current reaches the load current level at t_2.

This duration is known as the current rise time. Due to the very high electron mobility of the 2DEG channel, this time is significantly reduced compared to conventional Si devices, meaning a very high di/dt is likely to occur. The stray inductances including the internal inductance of the device package and the stray inductance of the circuit must therefore be kept as small as possible to minimise parasitic oscillations and voltage overshoots in both the gate and power loops. Excessive voltage on the gate could easily damage the device.



(a) (b)

Fig. 3.1. Ideal inductive switching waveforms of GaN HEMTs during (a) turn-on and (b) turn-off transients

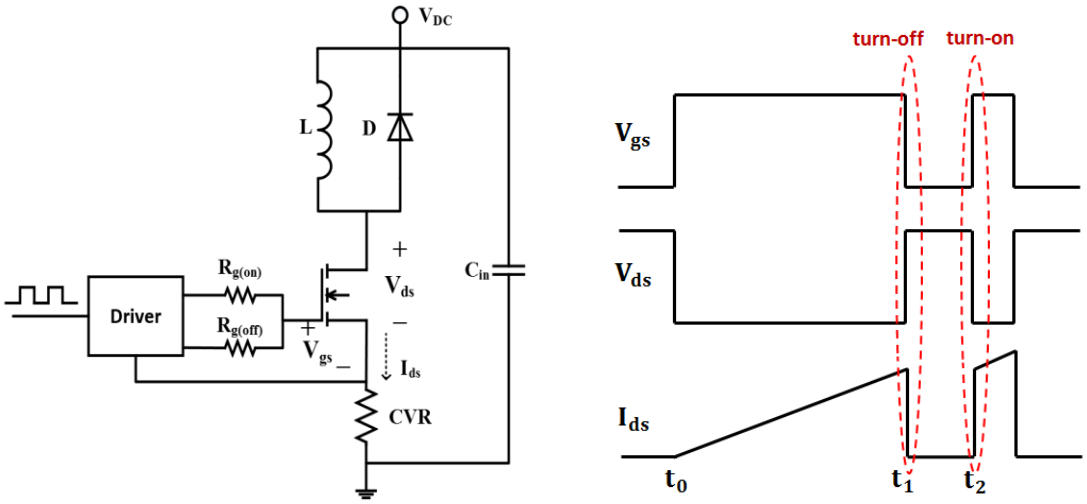
During $t_2 \sim t_3$, as the drain current I_{ds} reaches the load current level, the drain-to-source voltage starts to fall. The gate voltage remains constant and the Miller capacitor is discharged by the gate current. The device output capacitor discharges through the channel causing the fall of the drain-to-source voltage V_{ds}. This period is known as the voltage fall time. Due to the small output charge of GaN HEMTs, a fast discharging rate is likely to occur indicating a high dv/dt. The parasitic effects associated with the device Miller capacitance and the circuit parasitic capacitance between the switching node and the gate driving circuit tend to be more pronounced under high dv/dt. The capacitive current due to high dv/dt may flow through the gate driving circuit, charging or discharging the input capacitor and causing gate voltage oscillations, which could lead to unintended switching actions, device damage and failure of the circuit. The parasitic capacitance therefore needs to be supressed to avoid the capacitive coupling of current into the driving circuitry.

During $t_3 \sim t_4$, the device enters the ohmic region. The losses in the device become conduction loss rather than switching loss. The gate capacitor continues to charge until it reaches the driving voltage.

The turn-off mechanism during $t_5 \sim t_8$ is the reverse of turn-on sub-periods $t_0 \sim t_3$. During the voltage rise period $t_5 \sim t_6$, the circuit stray inductance is likely to resonate with device output capacitance, causing a voltage overshoot and oscillations in $V_{ds,}$ which increase the switching losses and may exceed the voltage limit of the device. Due to the low output capacitance of GaN HEMTs, this effect tends to be more severe, indicating the importance of controlling the stray inductance for GaN-based circuits.

3.2.2 Design and practical implementation of a double-pulse-test circuit

The double-pulse-test (DPT) circuit enables an explicit evaluation of the switching characteristics of a power transistor under typical inductive load conditions. A thorough understanding of the device switching characteristics is essential for loss estimation, parameter design, thermal design and component selection for GaN-based converter applications.



(a) (b)

Fig. 3.2. (a) DPT circuit diagram and (b) typical waveforms

The circuit diagram and typical waveforms of the DPT are shown in Fig. 3.2, where L represents the inductive load, C is the DC-link capacitor and D is the freewheel diode. The transistor turns on at t_0 and the inductor current starts to ramp up. The switching

waveforms during the turn-off transient at the chosen voltage and current can be observed at t_1. The inductor current then freewheels through the diode during $t_1 \sim t_2$, which will cause a slight fall in the inductor current depending on the power dissipation in the freewheeling loop. The transistor turns on again at t_2 and the switching waveforms during the turn-on transient at the required current and voltage can be examined.

The 650 V/60 A GaN HEMT from GaN Systems was selected for detailed practical investigation as it offered the highest current capability of the 600 V GaN devices that were available at the start of this project. The selection of the main components in the test circuit is described in the following sections.

A. Gate driver

The gate driver must deliver and extract the gate charges as rapidly as possible at the switching instants and must minimise unwanted deviations in the gate voltage, for example to prevent false switching or damage to the gate structure. The performance of three candidates was examined during the tests. The main features of the candidate driver ICs are listed in Table 3.1.

Table 3.1 Key parameters of candidate gate drivers

Part no.	Manufacturer	Rise / Fall Time	Source / Sink Current	Pull-down Resistance	Package
EL7155	Intersil	85 ns / 85 ns @10nF	3.5 A / 3.5 A	3.5 Ω	SOIC-8
LM5114	TI	82 ns / 12.5 ns @10nF	1.3 A / 7.6 A	0.23 Ω	SOT-23
FAN3122	Fairchild	23 ns / 19 ns @10nF	7.1 A / 9.7A	10 Ω	SOIC-8

Amongst the three gate drivers, the FAN3122 has the highest output current capability, indicating that it is likely to provide the fastest rising and falling rate at the switching instants. However, a pull-down resistance of 10 Ω is included, which increases the risk of device false turn-on due to the Miller effect, especially when high dv/dt occurs. The LM5114 from Texas Instruments has a much lower pull-down resistor of only 0.23 Ω. In addition, it is assembled in a SOT-23 package with six pins and has a much smaller footprint compared to the SOIC-8, which makes it more compatible with surface-mount GaN HEMTs and the requirement for a very compact, low inductance gate circuit layout. However, the source current capability of this chip is comparatively low, meaning that the device turn-on speed is likely to be compromised.

B. Freewheeling diode

The freewheeling diode will partially determine the turn-on loss in the transistor in the DPT circuit, since the diode output charge will be dissipated in the transistor during turn-on. Therefore, a SiC Schottky Diode C4D10120E 1.2 kV/33 A from Cree was selected for the test circuit. It offers zero reverse recovery current and a very small output charge, and it is assembled in a TO-252-2 surface-mount package, which helps to minimise the additional inductance introduced into the current commutation loop.

C. Current viewing resistor (CVR)

High-fidelity measurement of the transistor current is crucial for accurate loss measurement. A 0.05 Ω SDN-414-05 coaxial current viewing resistor from T&M Research Products was used to measure the drain current due to the high bandwidth of 2 GHz and the ultra-low inductance of around 2 nH. However, it has a maximum energy dissipation limit of 6 J, so is not suitable for the current measurement in continuous operation.

D. Load inductor

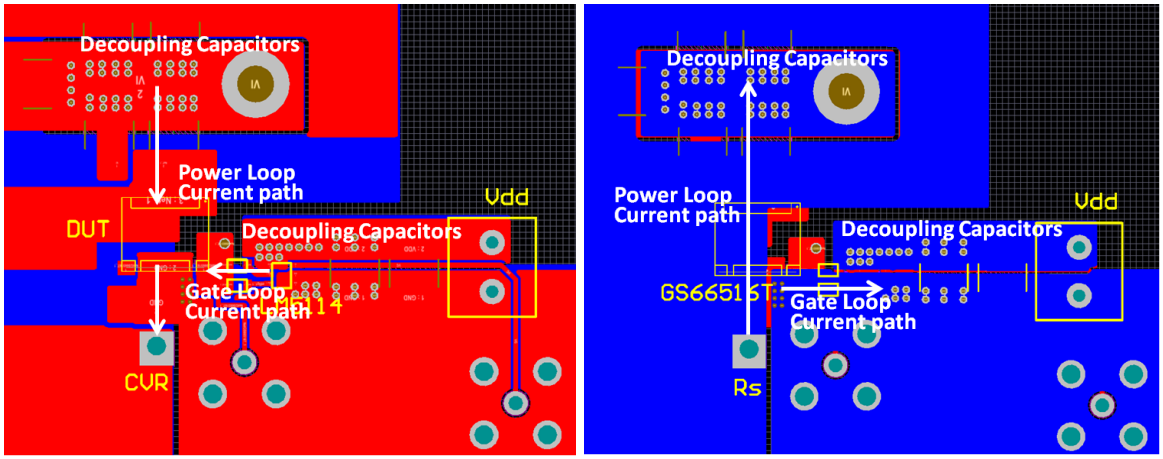
To minimise the overall parasitic capacitance of the inductor, three individual inductors were connected in series. Each separate inductor consisted of a 60 μH component designed using an ETD54 ferrite core with an airgap of 4.4 mm, which had a saturation current of 60 A.

E. PCB layout

A vertical design for the gate driving and power loop was adopted to minimize stray inductance, as shown in Fig. 3.3. Overlapping between the drain and the gate tracks was avoided to minimise capacitive coupling.

F. Capacitors

Two 800 V /80 μF film capacitors were used as DC-link capacitors to stabilize the input voltage. Five 630 V/470 nF and three 1 kV/100nF ceramic capacitors were used as the decoupling capacitors for the power loop. Two 25 V/ 1 μF and two 25 V/100 nF ceramic capacitors were used as the decoupling capacitors for the gate loop, which were placed very close to the driver IC.



(a) (b)

Fig. 3.3. PCB layout of DTP circuit (a) top layer and (b) bottom layer

To ensure an accurate switching loss measurement, the parameter settings of the oscilloscope and probes must be properly adjusted, for example the de-skewing between the oscilloscope channels for the voltage and current measurement, which are undertaken by a high voltage passive probe and a CVR+BNC cable, respectively.

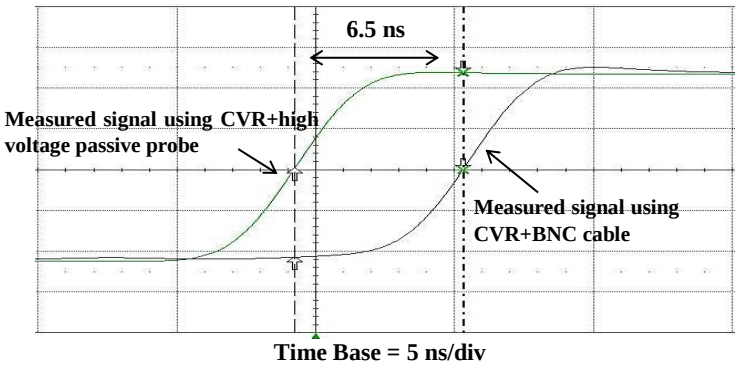
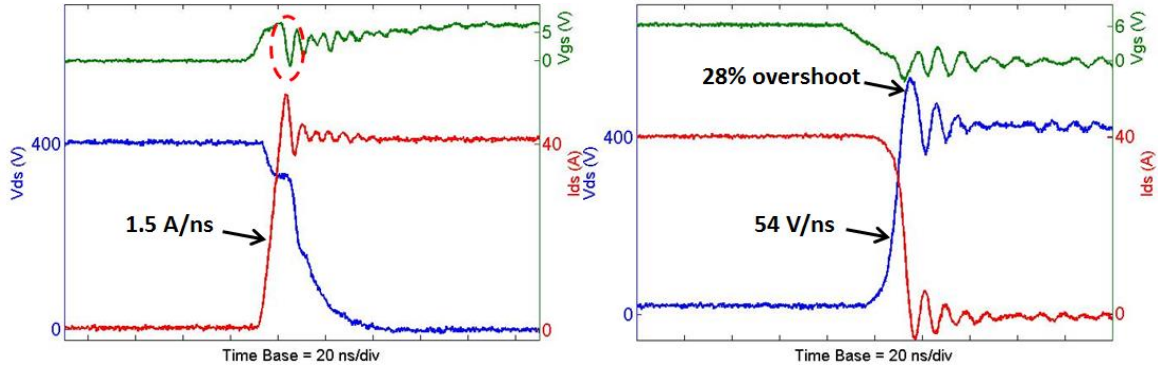


Fig. 3.4. Calibration waveforms before de-skewing

As shown in Fig. 3.4, a mismatch of 6.5 ns was observed between the two channels before de-skewing when measuring the same current signal through the CVR using the current and voltage measurement instruments for the double-pulse-test. This mismatch could significantly influence the switching loss calculation results if the de-skewing is not properly conducted.

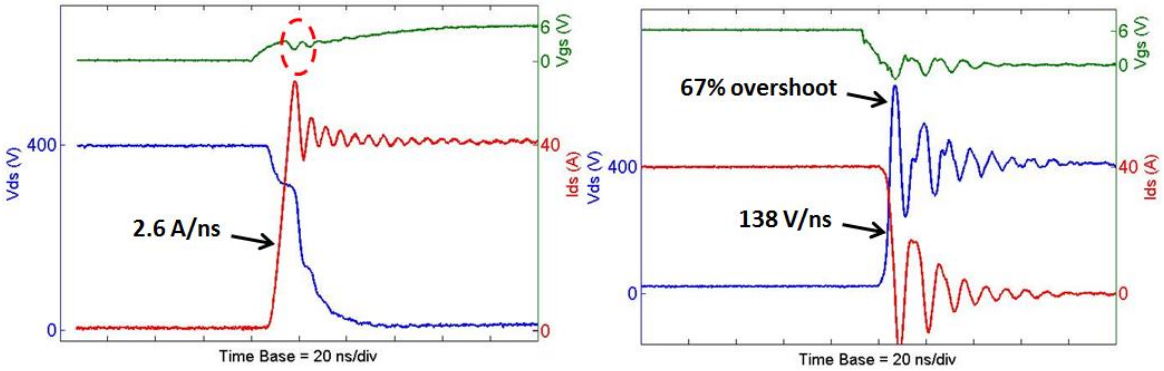
3.2.3 Experimental Results and discussion

The three aforementioned drivers were tested to evaluate the impact of driver characteristics on the switching performance of the DUT. Gate resistors of 10 Ω for turn-on and 1 Ω for turn-off were used for the test. The switching waveforms of the GS66516T GaN HEMT at 400 V, 40 A using the Intersil EL7155 and the TI LM5114 with a gate resistor of R_{on} =10 Ω and R_{off} =1 Ω are presented in Fig. 3.5 and Fig. 3.6. The two test circuit boards with the different drivers have the same PCB layout design.



(a) (b)

Fig. 3.5. Switching waveforms at 400 V, 40 A using Intersil EL7155 with R_{on} =10 Ω and R_{off} =1 Ω during (a) turn-on and (b) turn-off instants



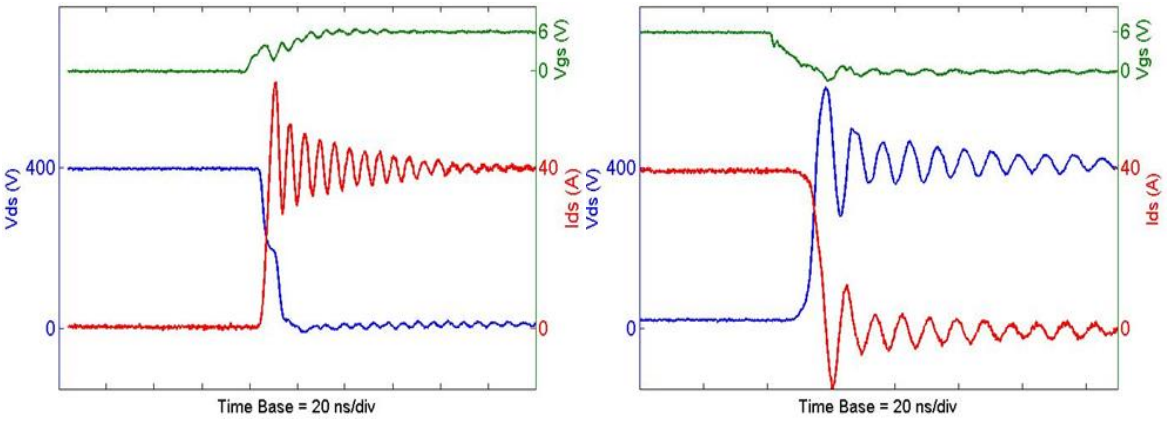
(a) (b)

Fig. 3.6. Switching waveforms at 400 V, 40 A using TI LM5114 with R_{on} =10 Ω and R_{off} =1 Ω during (a) turn-on and (b) turn-off instants

It can be seen from the switching waveforms that the LM5114 provides similar turn-on speed but much faster turn-off speed along with more severe ringing due to the higher sink

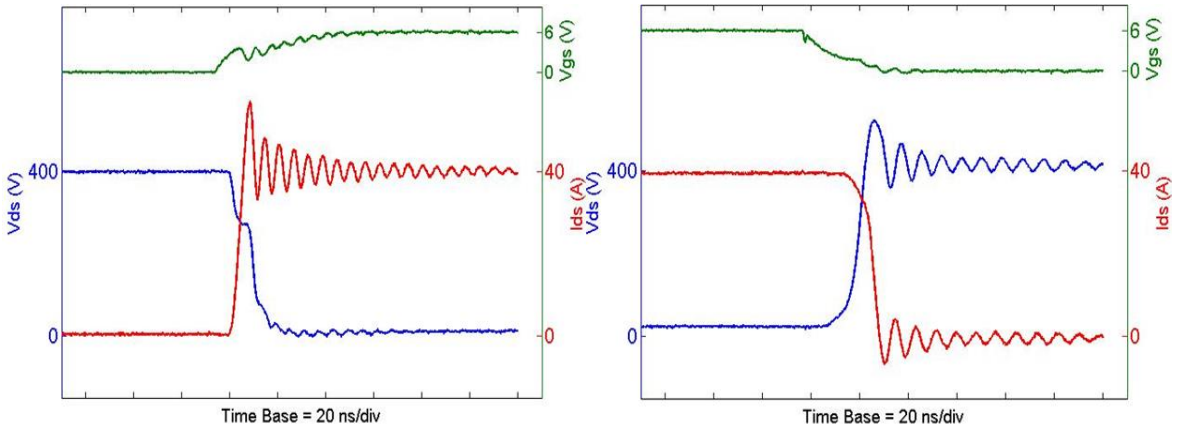
current. The GS66516T GaN HEMT features an ultra-low common source inductance of 200 pH, attributed to the special packaging technique (island technology). Therefore, it can be seen that the gate oscillations due to the high di/dt have been well controlled. In addition, it can be observed from the turn-on waveforms that when the drain voltage starts to decrease rapidly, the device with the EL7155 shows a distinct dip (marked by a red circle) in the gate voltage followed by several oscillations, which suggests this driver provides weaker dv/dt immunity (Miller effect immunity). In contrast, the voltage dip is well suppressed with the LM5114 and the gate voltage is much cleaner with higher dv/dt due to the small pull-down resistance. Therefore, the LM5114 from Texas Instruments is chosen for the next tests.

Based on the switching performance under the previous condition, Fig. 3.6, a smaller turn-on resistor can be chosen as no severe oscillation was observed during the turn-on transient, whilst the turn-off resistor should be increased to slow down the transient and suppress the voltage overshoot due to the resonance between the power loop stray inductance and the transistor output capacitance. Therefore, the test was repeated at 400 V, 40 A with gate resistors of 2 Ω and 5 Ω for turn-on and turn-off using the LM5114. The switching waveforms are shown in Fig. 3.7 and Fig. 3.8.



(a) (b)

Fig. 3.7. Switching waveforms at 400 V, 40 A using TI LM5114 with R_{on} = 2 Ω, R_{off} = 2 Ω during (a) turn-on transient and (b) turn-off transient



(a) (b)

Fig. 3.8. Switching waveforms at 400 V, 40 A using TI LM5114 with R_{on} = 5 Ω and R_{off} = 5 Ω during (a) turn-on transient and (b) turn-off transient

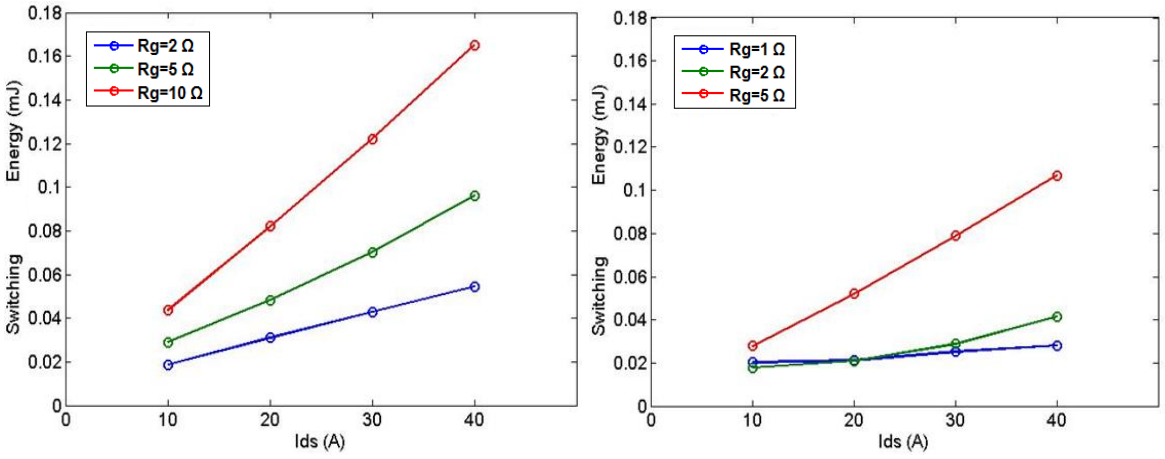
It can be seen that switching waveforms with no significant overshoot and gate ringing were realized when using the gate resistor of 5 Ω. However, the overlap area of current and voltage has increased, implying higher switching losses. The switching speed and duration with different gate resistors are summarized in Table 3.2.

Table 3.2 Switching speed of the GaN Systems HEMT at 400 V, 40 A with different gate resistors

R_{on}	2	5	10	Ω
I_{slew}	12.1	9.2	2.6	A/ns
V_{slew}	41.4	25.1	15.3	V/ns
t_{i_rise}	3	4.1	6.1	ns
t_{v_fall}	8.7	14.4	23.5	ns
I_{ds_pk}	43%	32%	25%	

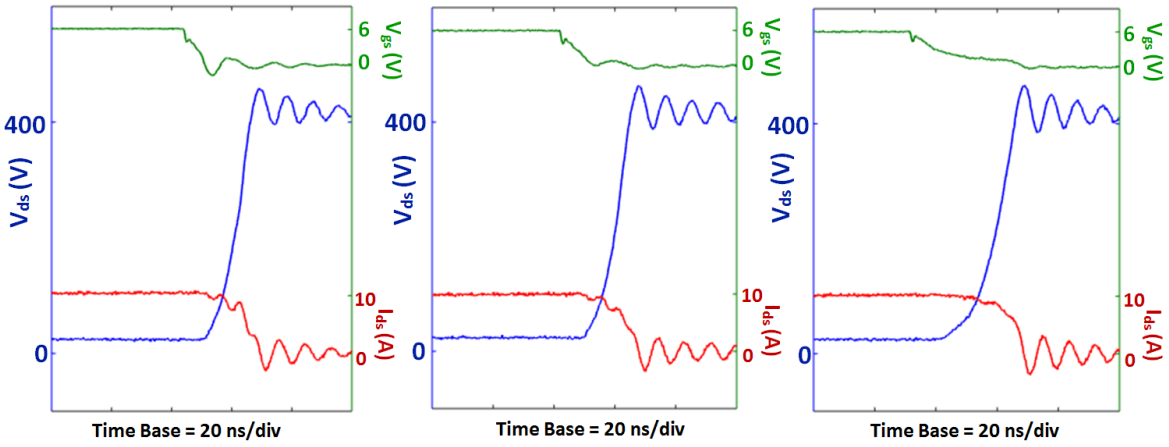
R_{off}	1	2	5	Ω
I_{slew}	10.9	8.2	4.4	A/ns
V_{slew}	138.4	94.7	42.8	V/ns
t_{i_fall}	3.3	4.4	8.1	ns
t_{v_rise}	2.6	3.8	8.4	ns
V_{ds_pk}	67%	45%	21%	

The switching losses with each gate resistor at 400 V and different drain currents were calculated, shown in Fig. 3.9. The switching times for the voltage and current were obtained from the 10% to 90% values.



(a) (b)

Fig. 3.9. Switching losses of GaN Systems HEMT at 400V with different gate resistors for (a) turn-on and (b) turn-off



(a) (b) (c)

Fig. 3.10. Turn-off waveforms of GaN Systems HMET at 400 V, 10 A using TI LM5114 with (a) R_{off} = 1 Ω, (b) R_{off} = 2 Ω and (c) R_{off} = 5 Ω

It can be seen from Fig. 3.9 that both the turn-on and turn-off transients have small switching losses with a sum of less than 200 µJ at 400 V, 40 A. The turn-off loss with relatively low drain current and a small gate resistor remains at around 20 µJ, which is

almost equal to the stored energy in the output capacitor at 400 V based on the datasheet, indicating that the dissipation in the channel is negligible. The switching waveforms for turn-off at 400 V and a low current of 10 A are shown in Fig. 3.10. Due to the ultra-low gate charge of the GaN HEMT, the 2DEG channel is turned off very quickly and the Miller plateau period is not evident with gate resistors of 1 Ω and 2 Ω, but becomes more obvious with a gate resistor of 5 Ω.

It is seen that the turn-on and turn-off loss increase significantly with 10 Ω and 5 Ω gate resistors respectively. Therefore, it can be concluded that 5 Ω and 2 Ω are a good choice for the turn-on and turn-off gate resistors respectively when using the LM5114, which results in a total switching loss of less than 150 μJ at 400 V, 40 A and a voltage overshoot of 45% during turn-off.

The switching losses of a 600V Si MOSFET using super-junction technology, STL24NM60N from STMicroelectronics, were also tested at 400V with R_{on} = 5 Ω and R_{off} = 2 Ω using the same circuit layout to compare with the performance of the GaN Systems HEMT. The result is shown in Fig. 3.11. It can be seen that the GaN HEMT has realized a loss reduction of around 90% for both turn-on and turn-off compared to a state-of-the-art super-junction silicon MOSFET.

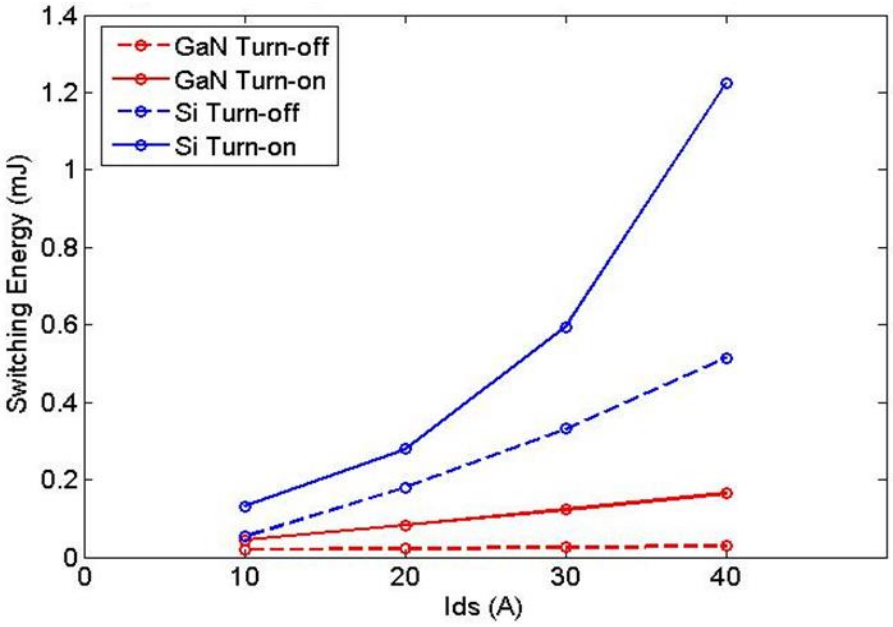


Fig. 3.11. Switching losses comparison of GaN Systems HEMT and Si STL24NM60N at 400 V with R_{on} = 5 Ω and R_{off} = 2 Ω

3.2.4 Summary of the GaN HEMTs switching performance characterization

This section presents the design and test results of a DPT circuit. The GaN HEMT, GS66516T, has been demonstrated to enable a very high switching speed of up to 138 V/ns with a maximum voltage overshoot of 67% during turn-off. The overshoot can be reduced by optimising the circuit stray inductance. The high switching speed of the GaN HEMT has led to a switching loss reduction of around 90% compared to a super-junction Si MOSFET. A gate driver with a small pull-down resistor and high current output such as the TI LM5114 has been seen to offer a good compromise between high switching speed and avoiding unwanted switching events due to the Miller effect. It was seen that with a well-designed driving circuit, the dissipation in the 2DEG channel of the GaN HEMT could be negligible during turn-off at relatively low current due to the absence of the Miller plateau.

3.3 Measurement of dynamic on-state resistance of GaN HEMTs

3.3.1 Introduction

One of the uncertainties that is limiting the uptake of GaN HEMTs is understanding the impact of dynamic on-state resistance, which is a reversible increase in the on-state resistance following a period of off-state voltage stress. The mechanism of this phenomenon is well documented and is explained in terms of injected charges getting trapped in the defects located at the material surface or deeply inside the GaN buffer or substrate, resulting in the depletion of the 2DEG layer and an increase of on-state resistance. The resistance will then gradually recover to the nominal value due to the release of trapped charges, known as detrapping.

It has been demonstrated that the trapping process can take place during two states. In the off-state, electrons supplied by the gate leakage current are injected from the gate metal towards the AlGaN barrier, GaN buffer or the passivation layer and are trapped there. In the switching state when there is high instantaneous power dissipation in the device, hot electrons are generated in the channel and can hop into a trapped state located close to the channel [66-68]. On the other hand, two mechanisms have been reported to be responsible for the detrapping process, which involve thermionic emissions and electron tunnelling [67-69]. Therefore, there are likely to be multiple time constants involved in the trapping and detrapping process due to the combined effects of these mechanisms.

3.3.2 Measurement techniques and challenges

A. Clamping circuit

The dynamic on-state resistance can be determined by measuring the on-state voltage and drain current. However, as the drain-source voltage of the device will swing from millivolts to hundreds of volts in each test cycle, a voltage clamping circuit is required to avoid saturating the amplifier of the oscilloscope, whilst allowing the maximum vertical resolution to be used to ensure accurate results.

The clamping circuits usually consist of diodes and capacitors to provide the clamping action and must have a quick response from the voltage blocking state to the stress-free state, allowing the on-state resistance measurement to take place in a short time. For example, if the GaN-based converter has a switching frequency of higher than 500 kHz, a settling time of less than 1 μs is required to provide a reliable indication of the conduction loss in the transistor. The response time and settling transient of the measurement instruments must therefore be carefully considered.

In addition, the clamping circuit must have a small physical size to fit within a compact circuit layout, since the test points need to be close to the DUT to minimise parasitic effects. In this work, a commercial voltage clipping probe, clp1500V15A1 from Springburo, with an integrated clamping circuit was used, which has a very compact design and a short settling time of 150 ns.

B. Test circuit

The double-pulse-test circuit described in 3.2.2 is one of the most commonly adopted methods for measuring dynamic on-state-resistance, and was recommended by the JEDEC Standards and Publications in January 2019 [135], which was published after this research was undertaken. However, the circuit itself has some limitations, which will be discussed in the next section.

C. Quantization error of oscilloscope

As the oscilloscope used for the test has a vertical resolution of 8 bits, there will potentially be quantization errors in both the voltage and current measurements. The adopted voltage clipping probe has a clamping level of 2.5 V. A scale of 500 mV/div has to be used to

include the whole measured waveform on the screen and to avoid saturating the oscilloscope channel amplifier. The maximum measurement error in the dynamic on-state resistance due to oscilloscope quantization error is calculated by considering the worst case errors in the voltage and current.

The maximum error of the voltage measurement can be calculated in (3-1).

$$V_{error} = \frac{(500\ mV \times 10)/2^8}{2} = 9.6\ mV \tag{3-1}$$

As a 50 mΩ CVR shown in section 3.2.2 C was used to undertake the measurement, a scale of 200 mV/div needs to be used to include the whole waveform for measuring 20 A. The maximum error of the current is calculated in (3-2).

$$i_{error} = \frac{(200\ mV \times 10)/2^8}{2} / 50\ \text{m}\Omega = 78.1\ mA \tag{3-2}$$

The GS66516T from GaN Systems with a DC resistance of 25 mΩ serves as the DUT. If the measurement is taken at 20 A, the maximum error in the calculated resistance is shown in (3-3).

$$R_{error}\% = (\frac{25\ m\Omega \times 20\ A + 9.6\ mV}{20\ A - 78.1\ mA} - 25\ m\Omega)/25\ m\Omega = 2.3\% \tag{3-3}$$

The quantization tends to have a larger influence when the measured voltage signal becomes smaller. The maximum error at 10 A is given by (3-4).

$$R_{error}\% = (\frac{25\ m\Omega \times 10\ A + 9.6\ mV}{10\ A - 78.1\ mA} - 25m\Omega)/25m\Omega = 4.7\% \tag{3-4}$$

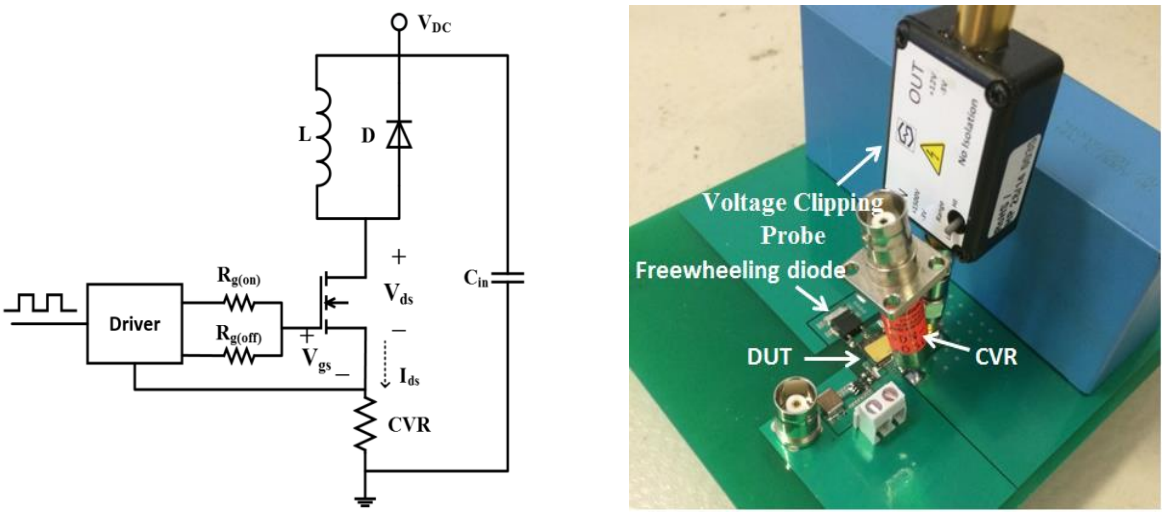
D. Current measurement

In the pulsed tests, the current is measured with a 0.05Ω SDN-414-05 coaxial current viewing resistor from T&M Research Products with a bandwidth of 2 GHz, which is however not suitable for continuous operation due to the thermal limitations. The current probe AP015 from Lecroy is used instead to undertake the current measurement for the continuous operation tests. Because of the probe jaw size, it can only be connected to measure the inductor current rather than the device current. Therefore, the capacitive current from the upper device cannot be seen in the current measurement. Also, the

bandwidth of the AP015 current probe is limited to 20 MHz, which may lead to the loss of some details in the current waveforms.

3.3.3 DPT test circuit

The measurement technique described in the JEDEC Standards was used initially, shown in Fig. 3.12. The current in the DUT rises to the measurement level at the end of the first pulse and the on-state voltage is measured during the second pulse after the short off-state. Some example test waveforms at 400 V, 20 A using the DPT circuit are shown in Fig. 3.13.



(a) (b)

Fig. 3.12 (a) Schematic and (b) practical implementation of DPT test circuit

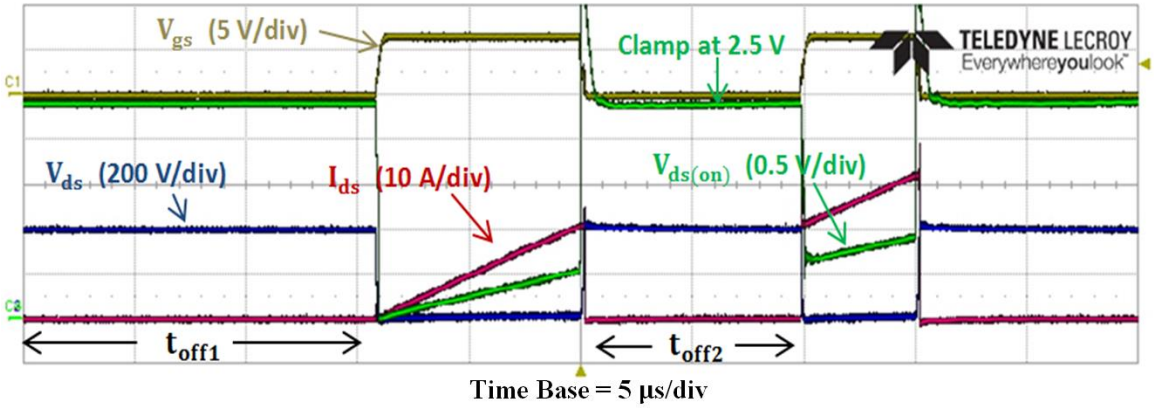


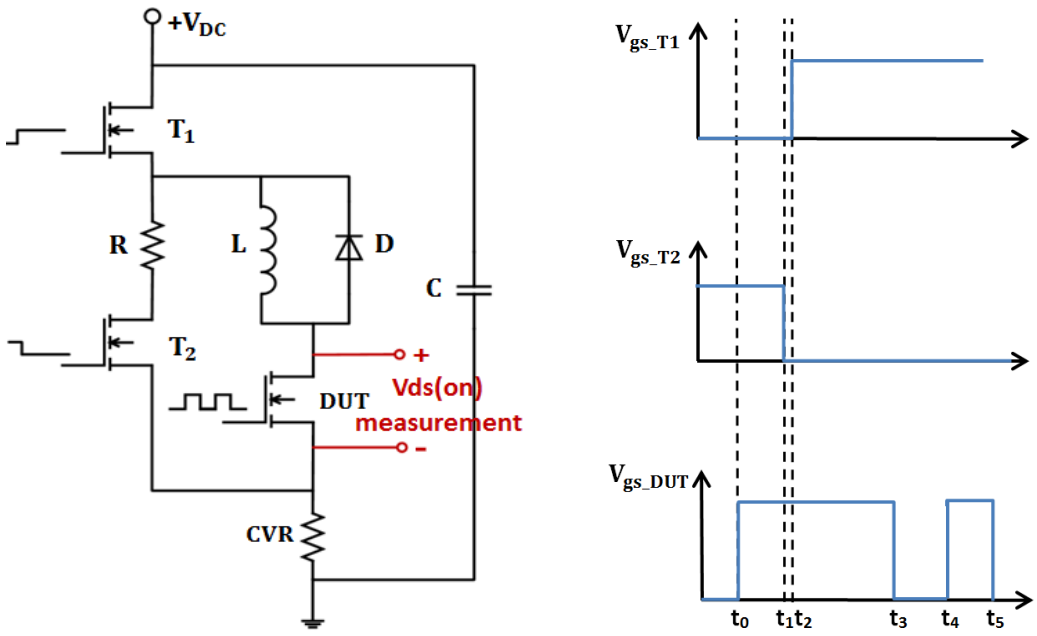
Fig. 3.13 Sampling test waveforms at 400 V, 20 A using DPT technique

The JEDEC Standard suggests that the off-state time t_{off2} is controlled as the stress time and the on-state voltage during the second pulse is monitored to evaluate the impact of the stress time t_{off2} on the dynamic on-state resistance $R_{ds(on)}$.

This method however, has a limitation, which may influence the reliability of the measurement. The DUT will be blocking a pre-stress voltage V_{DC} during t_{off1} from when the main supply voltage is applied until the two pulses are given. This second-level stress time is likely to cause a trapping effect on the DUT. An increase in the dynamic on-state resistance could then occur, which may not be reset during the few micro seconds of the first pulse. Therefore, the accuracy of the measurement using this technique may vary significantly according to the initial voltage stress.

3.3.4 Dynamic on-state resistance using modified DPT circuit

To address this issue, a modified DPT circuit was proposed to undertake the test. An additional leg consisting of two GS66516T GaN HEMTs from GaN Systems was added to control the application of the stress voltage across the DUT prior to the first pulse. The circuit schematic and control signals are shown in Fig. 3.14. The practical implementation of the test circuit is shown in Fig. 3.15.



(a) (b)

Fig. 3.14 (a) Schematic of the modified test circuit and (b) control signals of the test circuit for dynamic on-state resistance measurement

As shown in Fig. 3.14, the transistor T_1 blocks the DC link voltage during t_0~t_2 and the DUT remains unstressed. t_1~t_2 is the dead time between transistor T_1 and T_2, which is set to 20 ns. A resistor R of 100 Ω is used to guard against shoot-through after transistor T_1 is switched on at t_2. The inductor current rises in the DUT after t_2, and is commutated to the diode at t_3, then switched back to the DUT at t_4. t_3~t_4 is a controllable stress time. The test finishes at t_5 when the DUT is switched off.

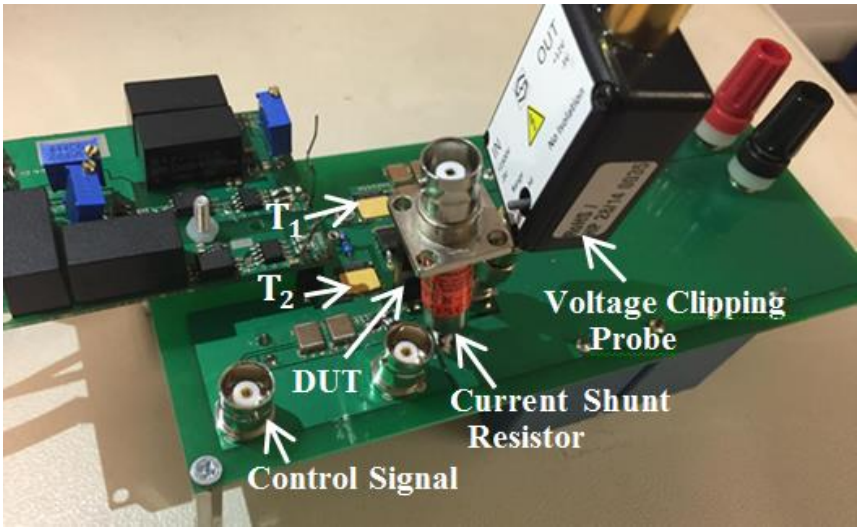


Fig. 3.15. Practical implementation of the modified test circuit

A. Dynamic on-state resistance with different stress voltages

In this test, t_0 is set 2 μs ahead of t_2 so that the DUT is switched on before transistor T_1, ensuring that no stress voltage is applied to the device before the first conduction period. Since the DUT is switched on in a stress-free condition, the dynamic on-state resistance measured during t_4~t_5 is solely due to the stress time t_3~t_4, which is fixed at 50 μs.

Three GaN devices and a super-junction Si MOSFET from different manufacturers were tested, listed in Table 3.3. Each device was tested using a stress voltage from 100 V – 400 V at a specific current level of 20 A for the GaN Systems HEMT and 8 A for the other devices. Experimental waveforms are shown in Fig. 3.16 for the GaN Systems HEMT 650 V/60 A device. The device current rises to 20 A at the end of the first pulse and the device on-state voltage $V_{ds(on)}$ is measured in the second pulse. The dynamic on-state resistance $R_{ds(on)}$ is calculated by dividing $V_{ds(on)}$ by I_{ds} after V_{gs_DUT} reaches its steady-state value, which is typically within 50 ns from the start of the turn-on transient.

Table 3.3 Summary of the devices under test

Manufacturer	GaN Systems	Panasonic	Transphorm	STMicroelectronics
Part No.	GS66516T	PGA26C09DV	TPH3206PS	STL24NM60N
Technology	p-GaN HEMT	p-GaN HEMT	GaN Cascode	Silicon
Ratings	650 V/60 A	600 V/15 A	600 V/17 A	650 V/16 A
R_{dc}	25 mΩ	71 mΩ	150 mΩ	215 mΩ

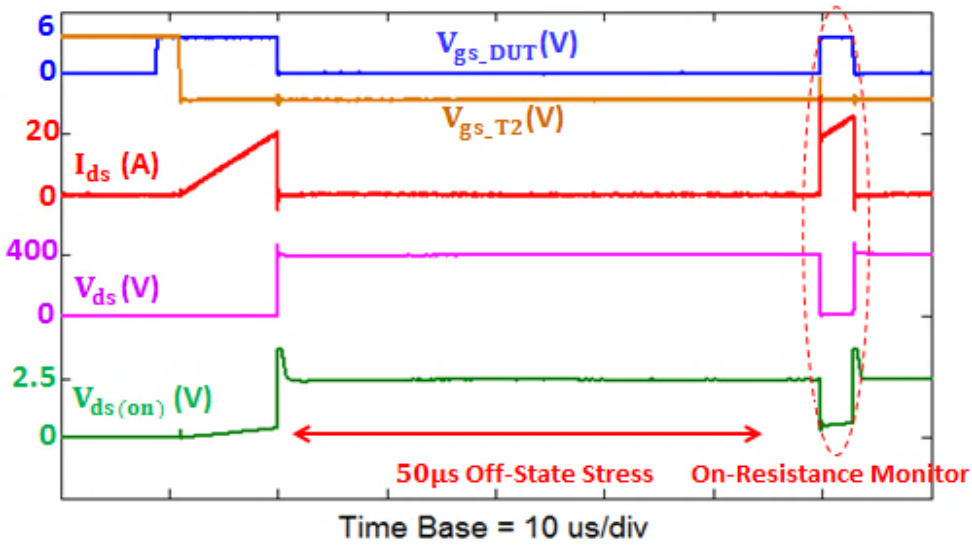


Fig. 3.16. Experimental waveforms of dynamic on-state resistance measurement with a stress voltage of 400 V for the GaN Systems HEMT 650 V/60 A

The dynamic on-state resistance during the 3 µs after turn-on at t_4 with a stress voltage of 100 V to 400 V is presented in Fig. 3.17 for the three GaN devices and also for a Si MOSFET for comparison.

The resistance values are normalized to the measured DC resistance R_{DC} at room temperature. As expected, there is no dynamic on-state resistance effect in the Si device. However, this result serves to confirm the accuracy of the resistance measurement. An increase in on-state resistance is observed for all three GaN devices and becomes more severe with higher stress voltage. Nevertheless, the variation patterns of the dynamic on-state resistance for the three devices are different. The GaN Systems HEMT in Fig. 3.17 (a) shows a peak increase of 42% at 400 V stress voltage, which drops to 21% after 3 µs of conduction, whilst the p-GaN device from Panasonic in Fig. 3.17 (b) has a much faster detrapping process with the on-state resistance recovering fully within 1 µs. This is likely to be due to different defect density distributions and trapping patterns in the two devices. The cascode GaN device from Transphorm in Fig. 3.17 (c) has a well suppressed dynamic

on-state resistance showing only a 6% increase with 400 V stress. However, the resistance value shows a small periodic variation in resistance which does not decay noticeably during the 3 µs. This difference in behavior is likely to be due to the use of a d-mode HEMT in the cascode device.

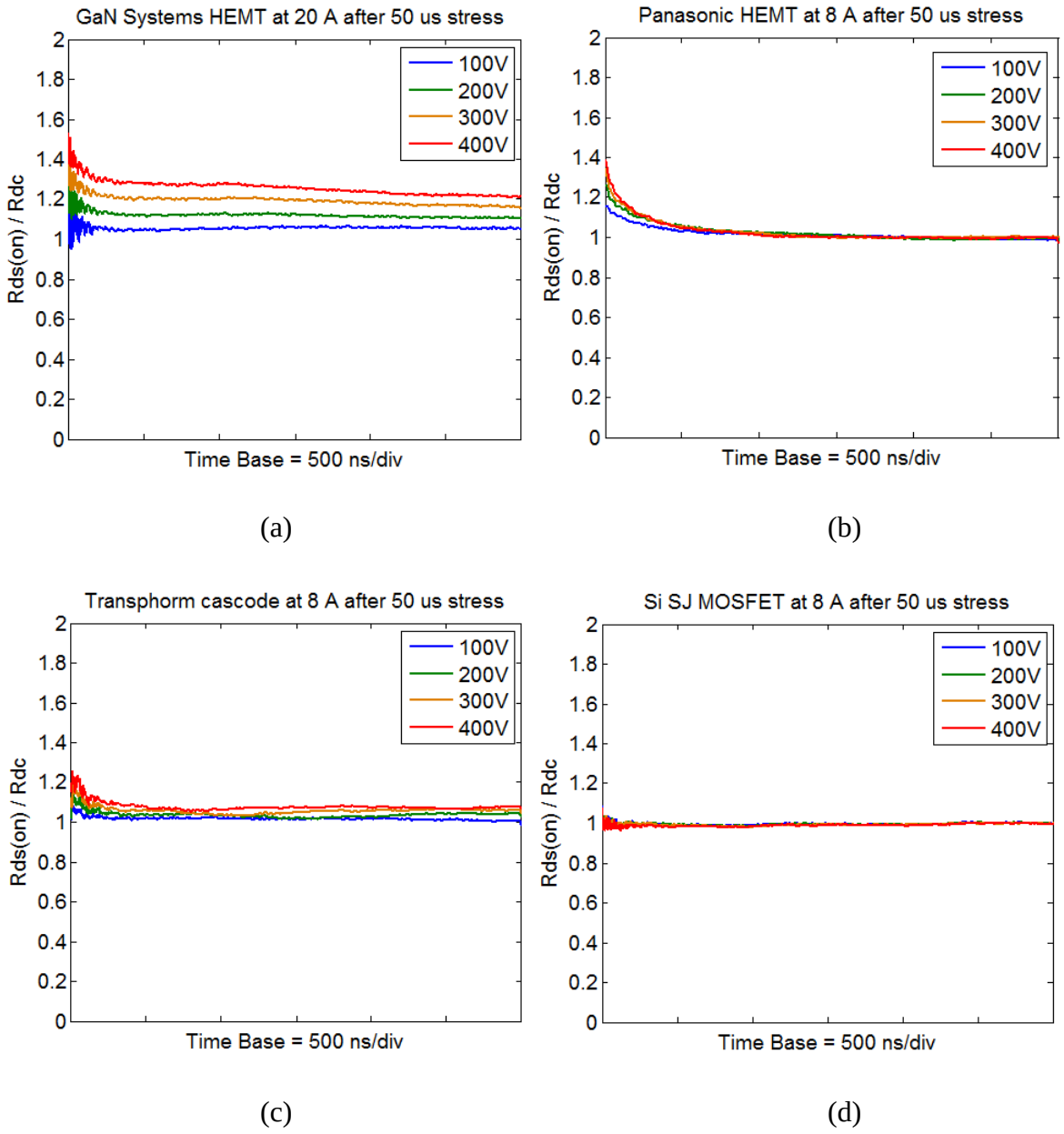


Fig. 3.17. Dynamic on-state resistance after 50 µs of stress voltage for (a) GaN Systems HEMT (b) Panasonic p-GaN HEMT (c) Transphorm cascode GaN device (d) Si MOSFET

B. Dynamic on-state resistance with different temperatures

The dependence of dynamic on-state resistance on junction temperature was examined by repeating the previous tests with the devices pre-heated to specific temperatures. A calibration curve of DC resistance against temperature was generated to infer the junction temperature of the device under test. The device junction temperature was determined by measuring the corresponding DC resistance immediately before the pulse test. The device DC resistance against temperature was measured in a separate test by measuring the on-state voltage of the device when submerged in heated oil while conducting a small current.

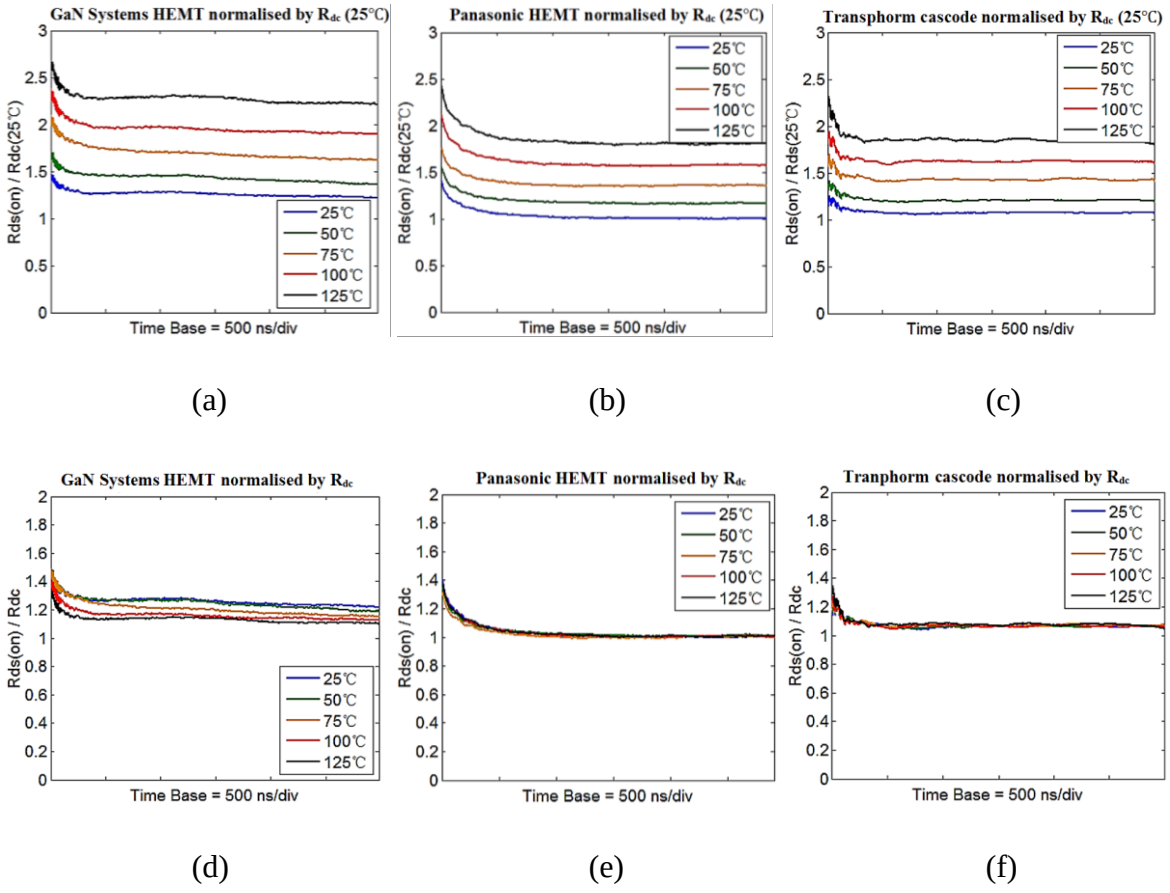


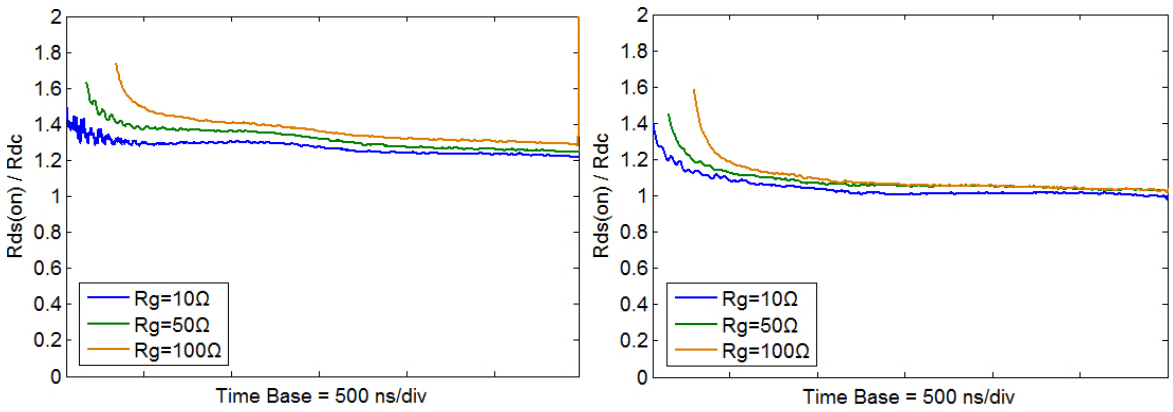
Fig. 3.18. Dynamic on-resistance at different junction temperatures normalized by DC resistance at 25 ℃ (top) and normalized by the corresponding DC resistance at each temperature (bottom) for (a, d) GaN Systems HEMT (b,e) Panasonic p-GaN HEMT (c, f) Transphorm cascode GaN device

Fig. 3.18 shows the dynamic on-state resistance at different junction temperatures normalized by the DC resistance at room temperature (top) and by the corresponding DC resistance at each temperature (bottom). It is seen in Fig. 3.18 (a, b, c) that the GaN

Systems HEMT has the most pronounced increase in the on-state resistance at elevated temperatures, which is due to the increase of both the DC resistance and the dynamic on-state resistance. An increase of 130% in the on-state resistance at 3 μs for 125℃ is observed for the GaN Systems HEMT compared to the DC resistance at room temperature, while the other two devices show an increase of around 80% at 3 μs for 125℃. It is seen in Fig. 3.18 (d) that the increase in on-state resistance due to the trapping process shows less impact as the temperature rises for the GaN Systems HEMT, since the increase in the device DC resistance due to temperature becomes dominant. In contrast, it is seen in Fig. 3.18 (e, f) that the variation pattern of dynamic on-state resistance due to the trapping and detrapping process for the other two GaN devices is relatively insensitive to temperature.

C. Impact of switching energy on dynamic on-state resistance

It has been concluded in [68, 69] that the energy generated during the switching transient can have an influence on the trapping process. To investigate the impact of the switching energy on $R_{ds(on)}$. The previous test with a stress voltage of 400 V for 50 μs was repeated under different switching conditions for the E-mode GaN HEMTs from GaN Systems and Panasonic. A larger gate resistor was used to produce higher switching loss in the devices.



(a) (b)

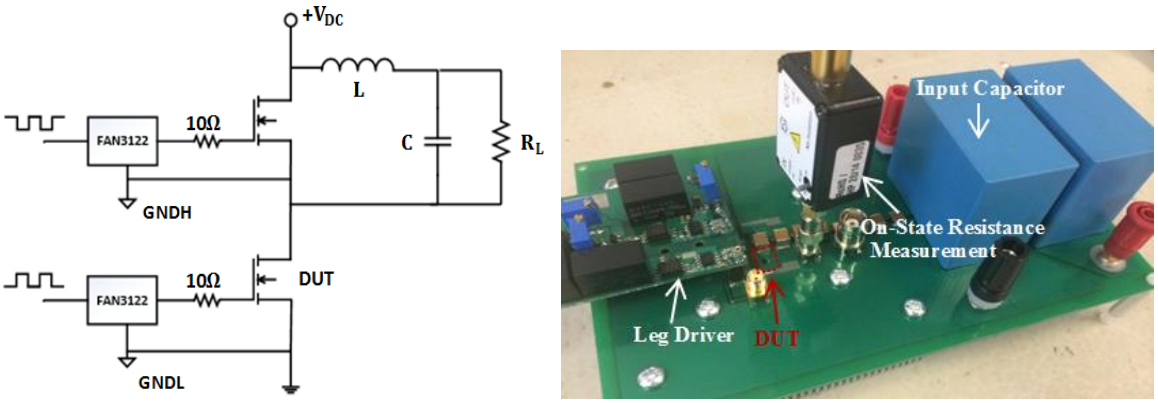
Fig. 3.19. Dynamic on-state resistance when switching with different gate resistors with a stress voltage of 400 V for 50 μs for the GaN HEMTs from (a) GaN Systems and (b) Panasonic

The measured results are shown in Fig. 3.19. The resistance was calculated after the gate-source voltage had reached steady state. It is indicated in Fig. 3.19 that the higher

switching energy due to the use of a 100 Ω gate resistor results in an increase of 9% over an interval of 3 μs in the dynamic on-state resistance for the GaN Systems HEMT and an increase of 6% over a 2.5 μs interval for the Panasonic HEMT. Whilst a gate resistor of 100 Ω results in an extremely slow switching transient of a GaN transistor, the results confirm the dependence of dynamic on-state resistance on the device switching transient.

3.3.5 Dynamic on-state resistance using continuous operation converter

Up to now, only a few publications have made contributions to understanding the behaviour of dynamic on-state resistance in terms of the switching frequency, duty ratio and switching losses during continuous operation, which is the normal pattern of operation in a converter application.



(a) (b)

Fig. 3.20. (a) Circuit schematic and (b) practical implementation of the tested step-down converter

Therefore, a step-down converter using the GaN Systems HEMT was built to evaluate the dynamic on-state resistance during continuous operation. The circuit schematic and practical circuit board are shown in Fig. 3.20. The free-wheel path was provided by a second GaN device operating as a synchronous rectifier. The test was carried out with a supply voltage of up to 300 V and a load current of 10 A. The period of continuous operation was limited to 1 ms to minimise self-heating. The circuit waveforms and the transistor on-state resistance showed a steady pattern at the end of the 1 ms test period. The dynamic on-state resistance at different switching frequencies and duty ratios was investigated.

A. Dynamic on-state resistance with different operating voltages

Fig. 3.21 shows the experimental waveforms for operation at 100 kHz, and Fig. 3.22 presents the dynamic on-state resistance in the final cycle of the 1 ms test with different supply voltages and a load current of 10 A at room temperature. The plot shows the complete transistor conduction period of 5 µs. The duty ratio was set at 0.5. It is seen that the on-state resistance is greater than the DC value and increases with the input voltage that is the transistor off-state voltage, which is consistent with the pulse test results.

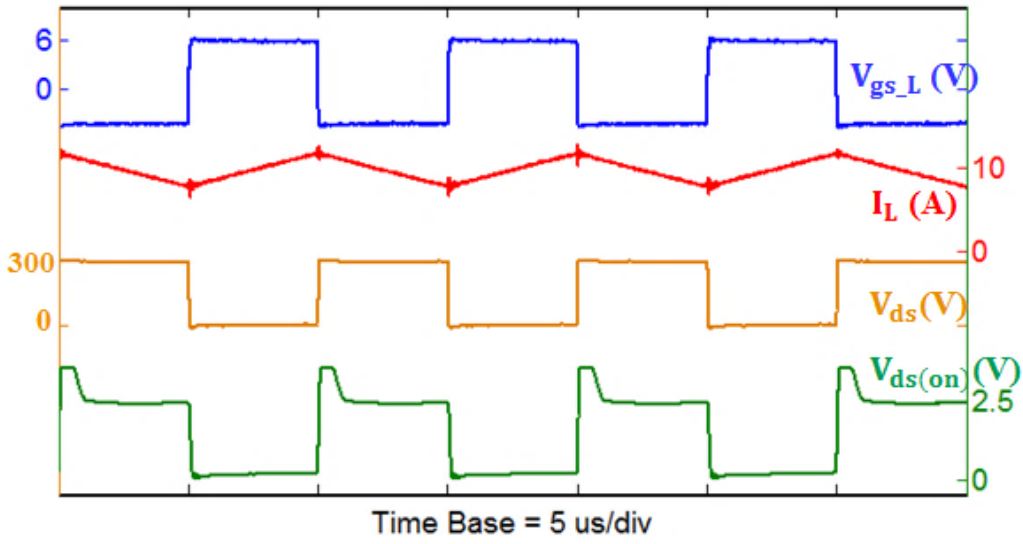


Fig. 3.21. Experimental waveforms of converter operating at 300 V with 10 A load current, 100 kHz, duty ratio of 0.5 and R_g=10 Ω

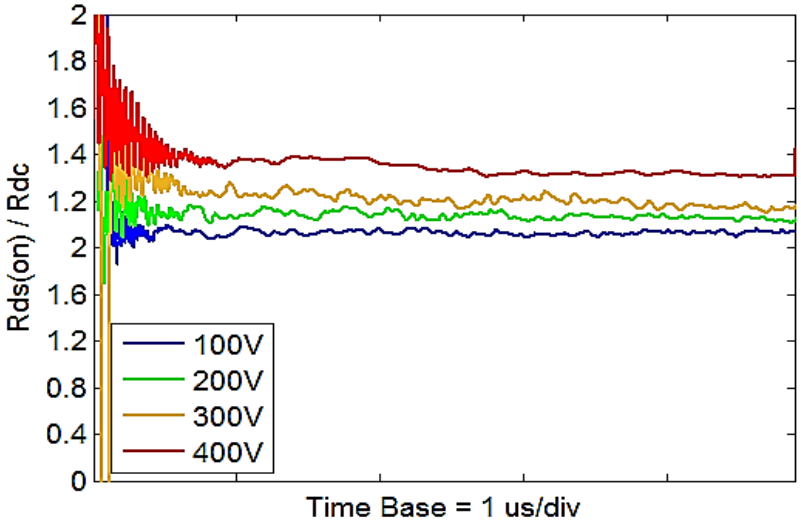


Fig. 3.22. Dynamic on-state resistance in the final cycle of the 1 ms test period with different input voltages, a load current of 10 A, duty ratio of 0.5 at 100 kHz and R_g=10 Ω

B. Dynamic on-state resistance with different switching frequencies

The transistor on-state resistance in the final cycle of the 1 ms test period when operating at 300 V with 10 A load current is shown in Fig. 3.23 for different switching frequencies and a duty ratio of 0.5. It is seen that the on-state resistance increases with the switching frequency, however the fast detrapping process remains evident during the first micro-second or two after the transistor turns on.

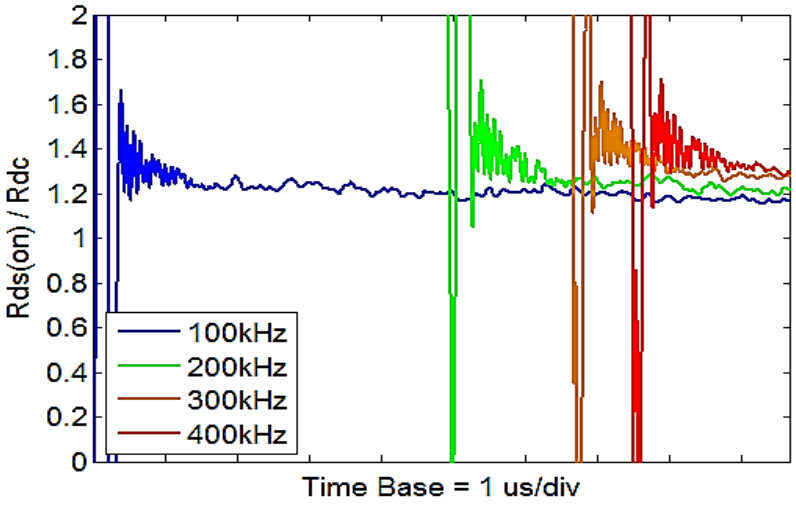
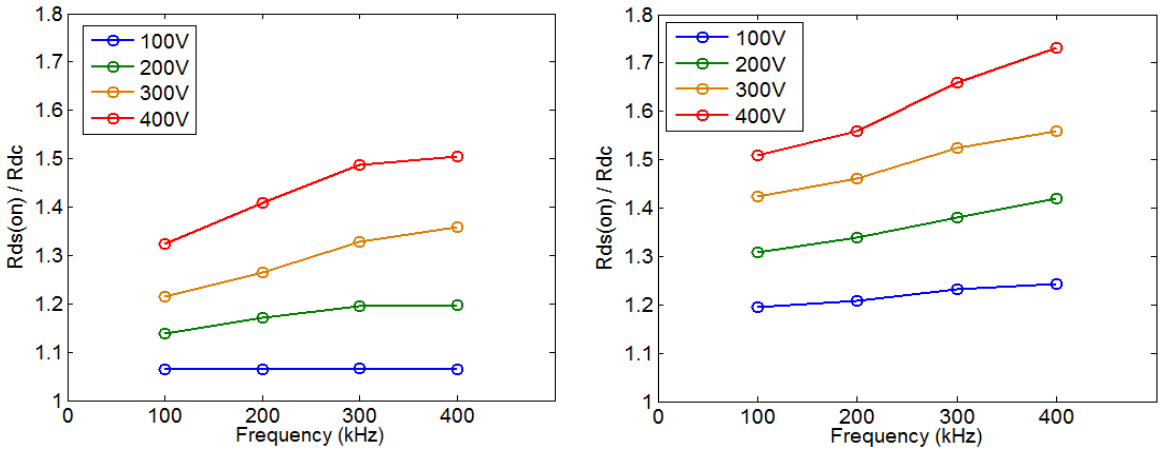


Fig. 3.23. Dynamic on-state resistance in the final cycle of the 1 ms test period at different switching frequencies with an input voltage of 300 V, load current of 10 A, duty ratio of 0.5 and R_g=10 Ω

To provide an estimate of the increase in transistor conduction loss caused by the dynamic on-state resistance, the average on-state resistance across the transistor conduction period was calculated and is plotted in Fig. 3.24 for a range of frequencies. With a low inductor ripple current, the increase in on-state loss will be approximately equal to the increase in average resistance. Fig. 3.24 (a) shows that the average on-state resistance across the transistor conduction period increases by 18.1% as the frequency is increased from 100 kHz to 400 kHz with a transistor off-state voltage of 400 V. In addition, the increase in dynamic on-state resistance with switching frequency is more apparent with higher operating voltage. Two mechanisms are responsible for this phenomenon.

One is the larger number of switching transients for high switching frequency operation which will lead to increased trapping during the switching transients and the other is the shorter detrapping time in each cycle, which together contribute to a cumulative trapping

process, resulting in the increase in on-state resistance during high switching frequency operation.



(a) (b)

Fig. 3.24. Average on-state resistance of GaN Systems HEMT in the final cycle of the test period at different switching frequencies and operating voltages with a load current of 10 A and duty ratio of 0.5 using (a) 10 Ω gate resistors and (b) 50 Ω gate resistors

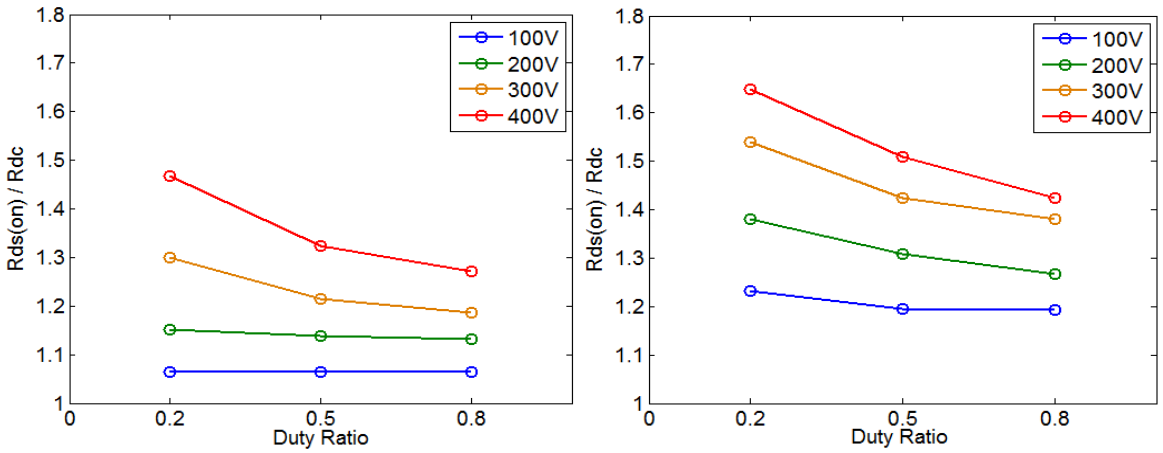
In order to demonstrate the effect of the switching transients, the test was repeated with a gate resistor of 50 Ω and the average on-state resistance is shown in Fig. 3.24 (b). It is evident that the increase in dynamic on-state resistance with switching frequency is more pronounced when using the 50 Ω gate resistors, resulting in an increase of 73.2% when operating at 400 V and 400 kHz, which demonstrates the contribution of the increased switching energy on the cumulative trapping process.

C. Dynamic on-state resistance with different duty ratios

The test was conducted for operation at 100 kHz with a load current of 10 A for different input voltages and duty ratios. The average on-state resistance measuring across the final transistor conduction period of 1 ms are presented in Fig. 3.25.

It can be seen from Fig. 3.25 (a) that the increase of dynamic on-state resistance is more apparent for small duty-ratio operation, resulting in an increase of 19.6% as the duty ratio is reduced from 0.8 to 0.2. This is thought to be due to the increased duration of the off-state stress time and the shorter time in each conduction cycle for detrapping to occur. Fig. 3.25 (b) indicates that the increase in dynamic on-state resistance with duty ratio is

accentuated with larger gate resistors, which is likely to be due to the effect of the increased energy during the switching transients.



(a) (b)

Fig. 3.25. Average on-state resistance of GaN Systems HEMT in the final cycle of the test period at different switching duty ratios and operating voltages with a load current of 10 A and switching frequency of 100 kHz using (a) 10 Ω gate resistors and (b) 50 Ω gate resistors

3.3.6 Dynamic on-state resistance using modified pulsed test circuit

Although the previous pulsed test circuit presented in 3.3.4 has been demonstrated to have a good performance on measuring the dynamic on-state resistance with different stress voltages, junction temperatures and switching energy, it is not very suitable to evaluate the impact of stress time on the dynamic on-state resistance. The stress time between the first and second pulse cannot be extended to a milli-second time scale due to the natural decay of the inductor current. The stress time before the first pulse can be controlled and further extended, but the on-state voltage measurement at the beginning of the first pulse is too small due to the low current, therefore highly subject to the quantization error of the oscilloscope, resulting in an unreliable measurement of dynamic on-state resistance.

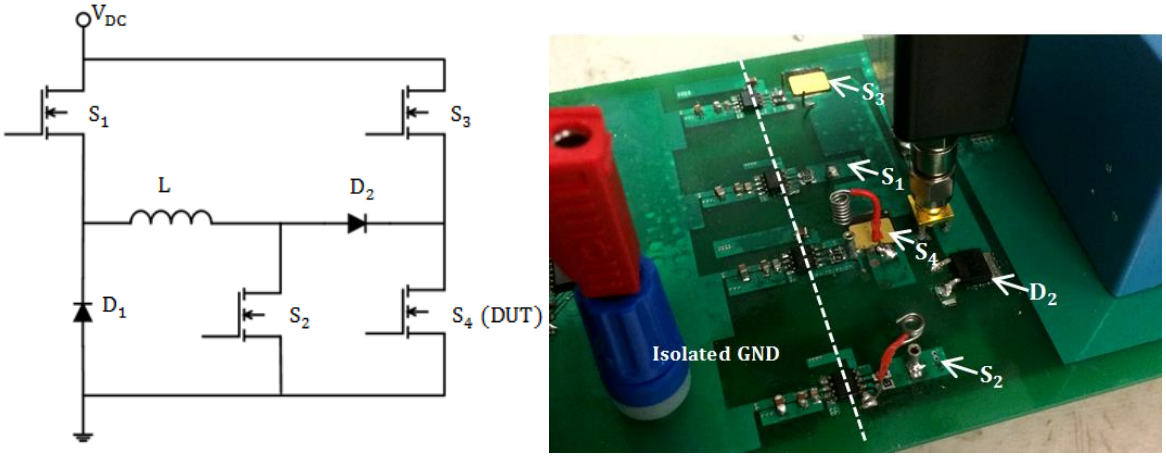
Therefore, a new circuit was proposed and designed that allows the observation of the dynamic on-state resistance in a pre-stress-free manner for both pulsed test and continuous operation over an extended time scale. The modified test circuit is capable of serving the following purposes.

(1) Measurement of dynamic on-state resistance after a precisely controlled off-state time from 10 μs up to any length.

(2) Measurement of dynamic on-state resistance for continuous operation with different voltages, currents and frequencies in a pre-stress-free manner. The purely inductive load enables the possibility of high operating current to enhance the measurement accuracy.

(3) Investigation and quantification of the impact of temperature on the DC resistance while the device is conducting a certain current for a controllable time.

The schematic and practical circuit of the modified test circuit are shown in Fig. 3.26.



(a) (b)

Fig. 3.26. (a) Schematic and (b) practical circuit of the modified test circuit

A. Dynamic on-state resistance with different stress times

Two 650 V /22 A SMD Si MOSFETs from Infineon were used for S_1 and S_2, which were responsible for building the inductor current to the required level. The device under test was again a GS66516T 650 V/60 A GaN HEMT from GaN systems. The same type of device was also used for S_3 that is in charge of controlling the duration of the stress voltage applied to the DUT. SiC Schottky Diodes, C4D10120E 1.2 kV/33 A from Cree, were used for D_1 and D_2. An isolated gate driving IC, Si8271 from Silicon Labs, was used to drive all the devices.

Example waveforms for operation at 400 V 10 A are shown in Fig. 3.27. S_1 and S_2 are turned on during t_1~t_2 and the inductor current I_L is increased to 10 A. t_0~t_2 is the stress

time controlled by S_3 and S_4 that are switched in a complementary manner with a dead time of 20 ns. A gate voltage of 0-9V is used to drive S_1 and S_2.

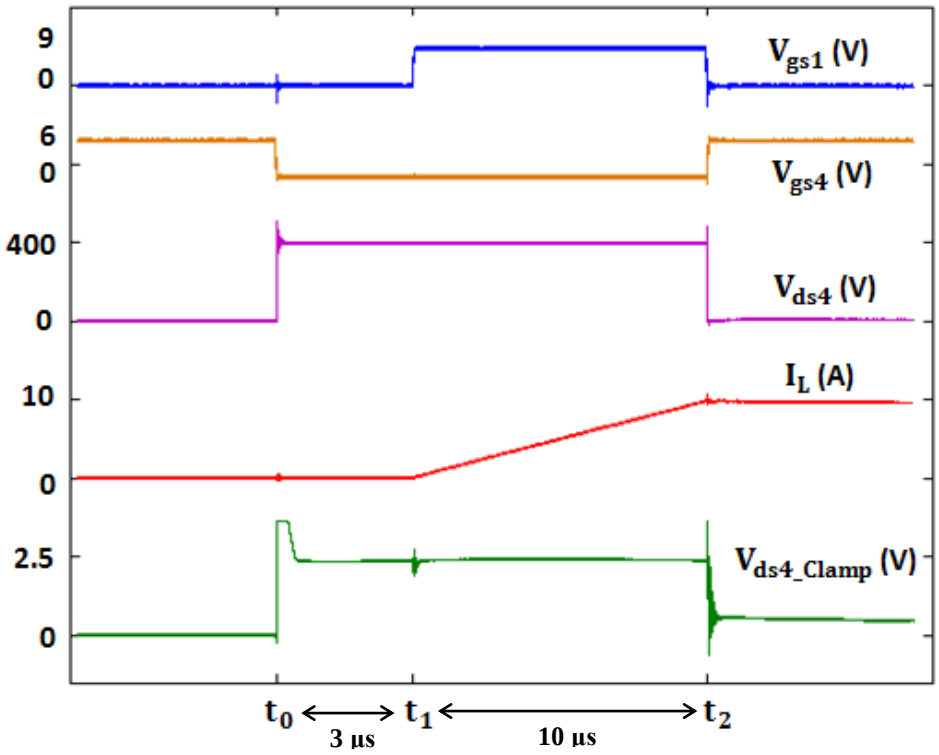


Fig. 3.27. Experimental waveforms for dynamic on-state resistance measurement at 400V 10A using the modified test circuit

The stress time t_0~t_2 was set from 100 µs to 100 ms to evaluate the impact of the stress time on dynamic on-state resistance. The dynamic on-state resistance 1 µs after turn-on at 10 A with a stress voltage of 100 V to 400 V for an extended stress time is shown in Fig. 3.28.

It can be seen from Fig. 3.28 that the increase in dynamic on-state resistance is within 5% for a stress time from 100 µs to 1 ms with a stress voltage of 400 V. However, a stress time from 1 ms to 10 ms is seen to increase the dynamic on-state resistance by around 24%. The impact of stress time in the range of 40 ms to 100 ms showed a progressively smaller increment in the dynamic on-state resistance, which may indicate that the number of trapped charges has reached a saturation level. In addition, the dynamic on-state resistance for stress voltages of more than 200 V shows a similar trend, whilst the dynamic on-state resistance with a stress voltage of 100 V is less sensitive to the stress time.

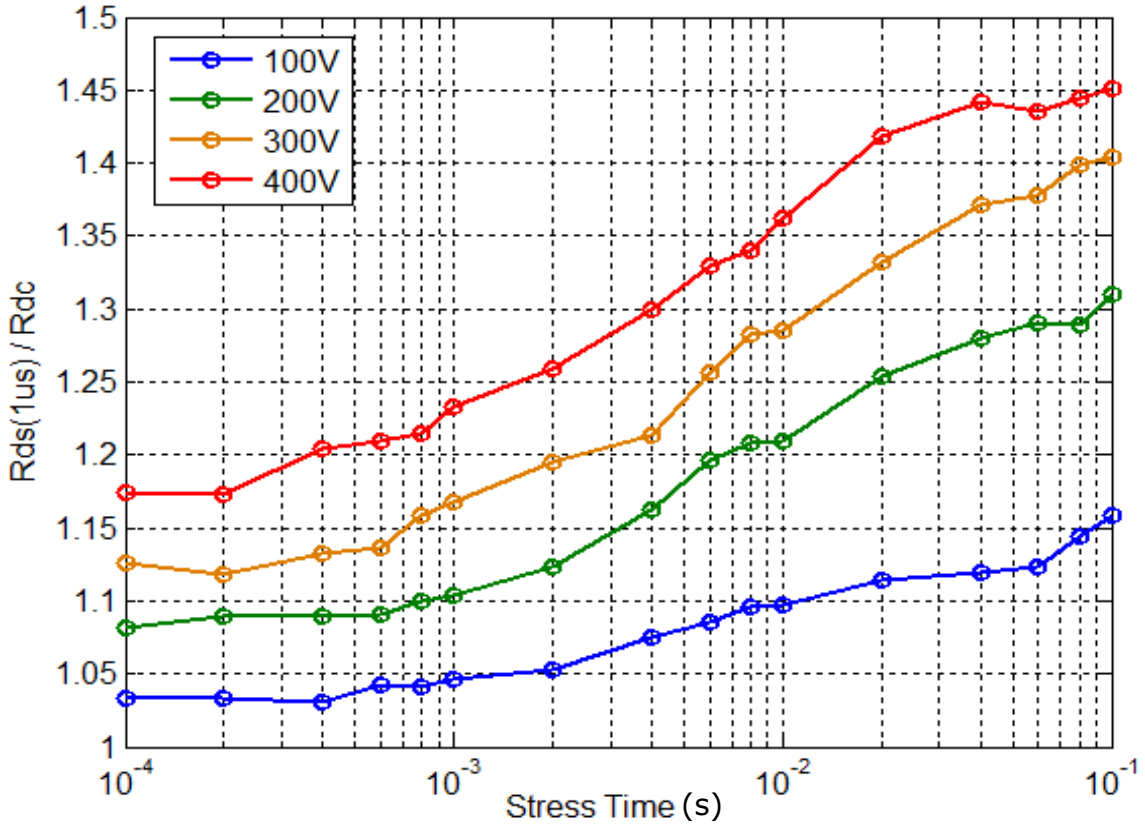


Fig. 3.28. Dynamic on-state resistance at 1 μs after turn-on at 10 A following a stress voltage of 100 V to 400 V for 100 μs~100 ms

B. Dynamic on-state resistance during continuous operation

The dynamic on-state resistance during continuous operation has been thoroughly investigated in 3.3.5. However, one of the uncertainties still remains, which is the step-down converter is not operated in a pre-stress-free condition. Although it represents the normal pattern of the operation of converter applications, the pre-stress before the 1 ms test period may cause a misleading effect on the impact of trapping, detrapping and switching energy on the dynamic on-state resistance. The modified test circuit however, is capable of examining the dynamic on-state resistance after a period of continuous switching without the initial voltage stress, so that the results can be used to compare with 3.3.5.

In this case, the gate of S_2 is pulled to ground. S_1, D_1, S_3 and S_4 form an H-bridge current source and are constantly switched for a controlled time. The inductor current is maintained at the required level by adjusting the duty ratio of S_1 and S_4. S_1 and S_3 turn off after the switching period while the DUT S_4 remains on. The resistance measurement then

takes place while the current is free-wheeling through the DUT, D_1 and D_2. The experimental waveforms for testing at 400 V 10 A and 250 kHz are shown in Fig. 3.29.

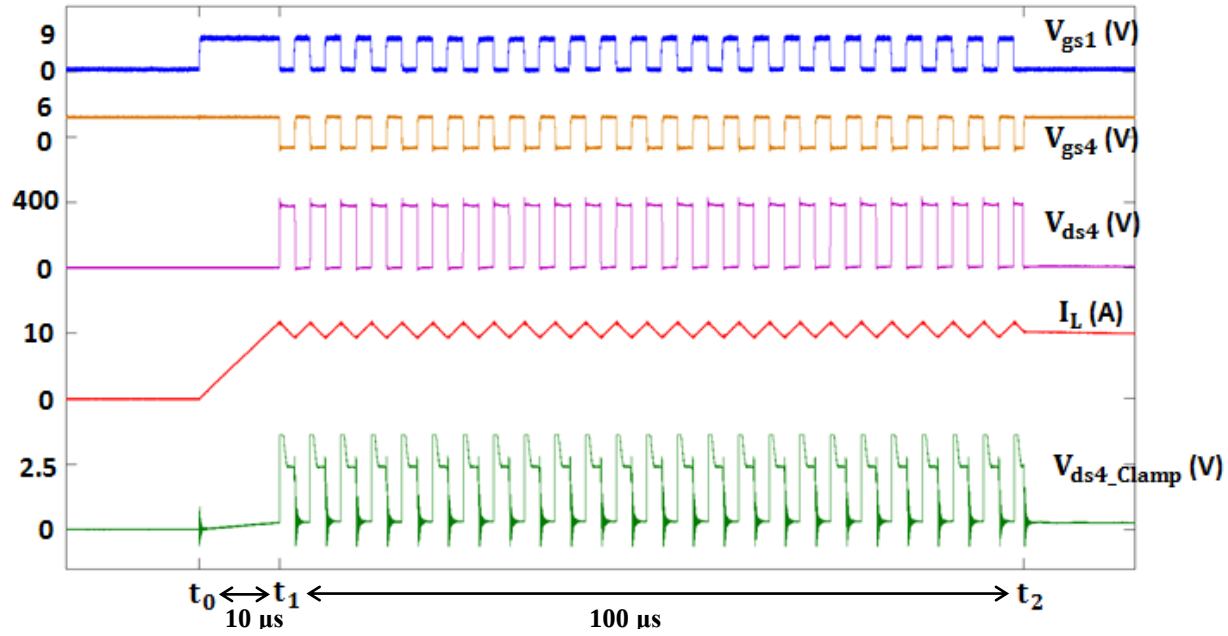


Fig. 3.29. Experimental waveforms for dynamic on-state resistance measurement at 400 V, 10 A, 250 kHz using the modified test circuit

The inductor current rises to 10 A at t_1 and the DUT is constantly switching during t_1~t_2 at the required current level. The dynamic on-state resistance 1 µs after t_2 was measured and plotted against the continuous switching period t_1~t_2, shown in Fig. 3.30.

It is evident from the comparison between Fig. 3.28 and Fig. 3.30 that the increase in dynamic on-state resistance of the DUT after continuous operation is more pronounced than after an off-state stress for a similar time, indicating the switching process has caused more severe charge trapping than a constant off-state stress. The difference becomes more substantial in the time scale of 10 ms to 100 ms. However, the device self-heating due to the conduction and switching losses is likely to have contributed to the increase in on-state resistance. Further investigation is needed to identify and quantify the impact of device self-heating on the dynamic on-state resistance during continuous operation.

It is noted that the previous results of the on-state resistance during continuous operation shown in Fig. 3.24 (a) are higher than the results shown in Fig. 3.30. For instance, the increase in dynamic on-state resistance after operating with 400 V, 10 A, at 250 kHz for 1

ms is roughly 46% in Fig. 3.24 (a) but is seen to be only 23% in Fig. 3.30. Therefore, it is likely that the pre-stress before the test period of 1 ms in the previous continuous operation test may have contributed to the increase in the on-state resistance.

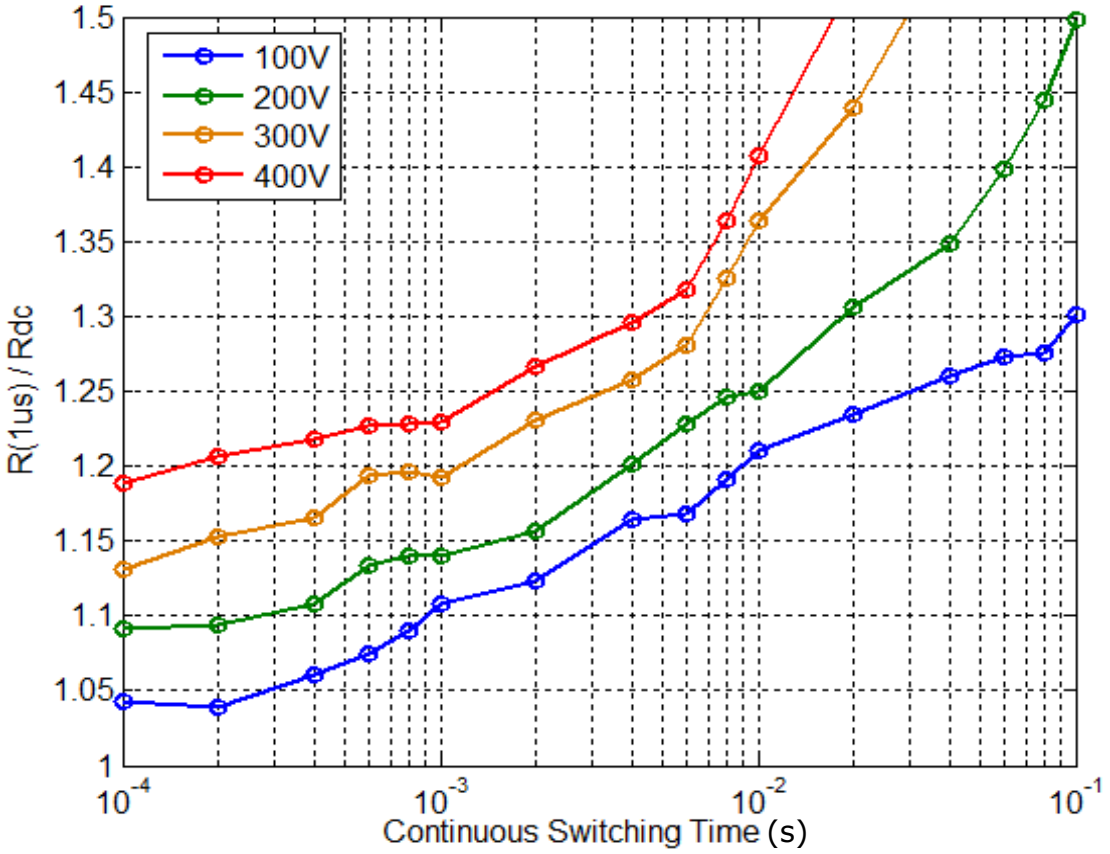


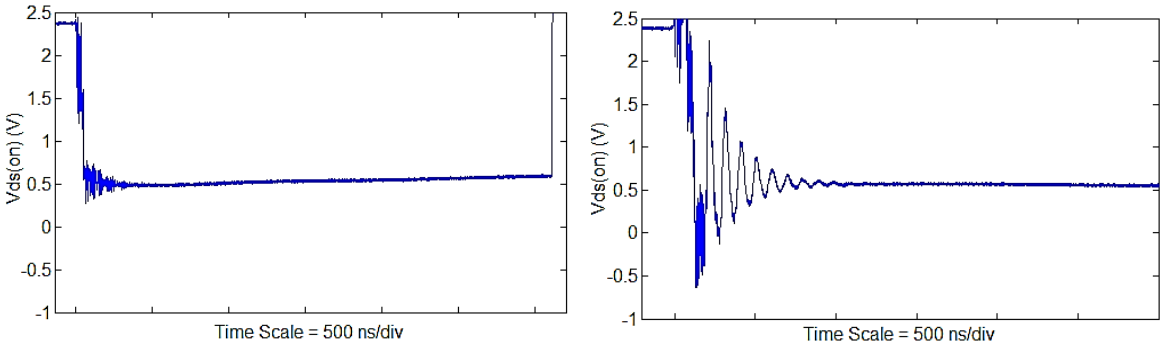
Fig. 3.30. Dynamic on-state resistance at 1 μs after continuous switching with a load current of 10 A, switching frequency of 250 kHz and duty ratio of 0.5, and operating voltage of 100 V to 400 V for 100 μs~100 ms

3.3.7 Performance comparison of the original and modified test circuits

Despite the additional capabilities of the modified test circuit, the performance during the on-state voltage measurement $V_{ds(on)}$ has been compromised compared to the original test circuit due to the parasitic components from the additional devices. Fig. 3.31 shows sample waveforms for the on-state voltage during 3 μs after the device turns on at 400 V and 20 A using the two test circuits.

It can be seen from Fig. 3.31 that severe oscillations are observed in the on-state voltage measurement during the first 1 μs using the modified pulsed test circuit due to the introduced circuit components and parasitic effects, meaning that the result for dynamic

on-state resistance in the first 1 μs is not usable. In contrast, the on-state voltage measurement with the original circuit shows a much cleaner waveform, enabling the measurement of dynamic on-state resistance almost immediately after turn-on.



(a) (b)

Fig. 3.31. Experimental waveforms for on-state voltage measurement with the voltage clipping probe using (a) original test circuit and (b) modified test circuit

3.4 Summary

This chapter describes the characterization of GaN HEMTs in terms of switching performance and dynamic on-state resistance. The switching characteristic of a GaN HEMT GS665016T 650 V/60 A from GaN Systems was evaluated using a DPT circuit. The impact of the PCB layout and gate driver was firstly identified. The vertical layout design for the gate and power loop was adopted. Three gate driving ICs were tested and the LM5114 from Texas Instruments was found to have the best performance due to the compact package, high output currents and small pull-down resistance. A turn-on speed of 9.2 A/ns and a turn-off speed of 94.7 V/ns were achieved using 5 Ω and 2 Ω gate resistors respectively. The total switching loss under such conditions was demonstrated to be less than 150 μJ at 400 V, 40 A. The channel dissipation at turn-off was seen to be negligible with a low current of 10 A and gate resistors of 1Ω and 2 Ω due to the very small input charge and the absence of the Miller plateau period.

A thorough investigation into the dynamic on-state resistance of GaN HEMTs in terms of stress voltage, stress time, junction temperature, switching frequency, switching energy has been undertaken. The limitations of the conventional test technique using the DPT circuit are identified and two test circuits were developed to provide a more reliable and accurate measurement.

An increase of 20~30% in dynamic on-state resistance was observed for the two E-mode GaN devices within 3 μs of turn-on after 50 μs of 400 V stress voltage. In contrast, the cascode GaN device from Transphorm exhibited a well suppressed dynamic on-state resistance of less than 6%. The dynamic on-state resistance has been demonstrated to be related to the energy generated during the switching transient. The use of a 100 Ω gate resistor resulted in an increase of 6~9% in the dynamic on-state resistance for the two E-mode GaN devices under the same test condition. The dynamic on-state resistance effect was seen to be largely insensitive to elevated temperature, the increased on-state resistance at higher temperature being mainly due to the change in DC resistance. The dynamic on-state resistance of the GaN HEMT from GaN Systems showed a clearly rising trend for stress times in a range of 1~40 ms, but the rate of increase became lower over a stress time scale of 40~100 ms. An increase of 45% in the dynamic on-state resistance within 1 μs of turn-on at 400V, 10 A was observed after the device blocked a stress voltage of 400 V for 100 ms.

In continuous operation, the dynamic on-state resistance effect was seen to be more severe at high frequency or low duty ratio. An increase of 50.4% in average on-state resistance of the GaN Systems HEMT was observed when operating at 400 V, 10 A, 400 kHz and 0.5 duty ratio which was aggravated by the use of a 50 Ω gate resistor, resulting in an increase of 73.2% in the average on-state resistance at the same conditions. However, the device self-heating may have contributed to the increase in the on-state resistance during continuous operation. Further work is required to rule out the effect of device self-heating from the dynamic on-state resistance.

Chapter 4

GaN-Based Interleaved Switched-Capacitor Step-Down Converter

4.1 Introduction

To investigate some of the challenges and benefits of using WBG devices in demanding power conversion applications, this chapter considers the case of a high-step-down ratio DC/DC converter, 270-28 V at around 1 kW. This is a typical requirement in many aerospace systems and similar high-step-down requirements are emerging in the automotive and vehicle sector, for example 400-48 V. High efficiency and high power density are key priorities.

Following a brief discussion of the topology selection, the operating principle of the circuit is discussed leading to a detailed analysis of the impact of parasitic capacitance and losses. The circuit operation is validated by computer simulation and a prototype is developed and tested to confirm the performance. Particular care was taken in the prototype development to achieve a compact electrical layout and effective thermal management.

4.2 Topology selection and description

Transformer-based circuits are a common solution for realizing high conversion ratios, but tend to be less attractive for size/weight-sensitive applications where voltage isolation is not essential. Several high-step-down ratio, non-isolated DC/DC converter topologies have been reviewed in Chapter 2. The key features of these topologies are shown in Table 4.1, where D is the duty-ratio. The cascaded and quadratic buck topologies can overcome the need for extremely small transistor duty-ratios, which lead to poor device utilisation. However the cascaded buck circuit requires two active switches and suffers from the efficiency penalty of processing the power twice, whilst the quadratic buck circuit imposes high voltage stress on the active device, which increases the switching losses. Switched-capacitor/inductor circuits have relatively lower device voltage stress and are reported to have higher efficiency [132]. In addition, the diode stress voltage is only half of the switch

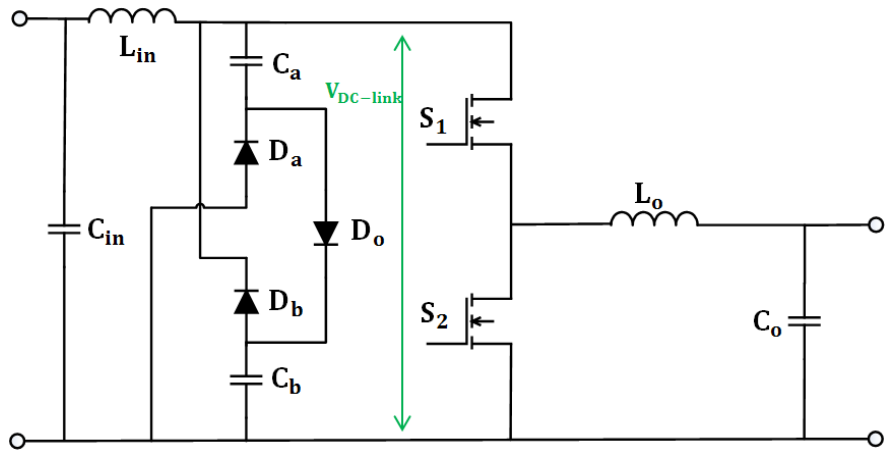
voltage, which allows lower voltage devices with smaller parasitic capacitance to be used, reducing the switching losses. The combination of a switched-capacitor and switched-inductor circuit as seen in the switched-capacitor buck converter offers a simple topology with greater step-down ratios whilst retaining straightforward duty-ratio control. Switched-capacitor based circuits also tend to be more advantageous for power dense applications since capacitors are usually more efficient and physically smaller than inductors as energy storage components.

Table 4.1 High-step-down ratio DC/DC converter topologies key features

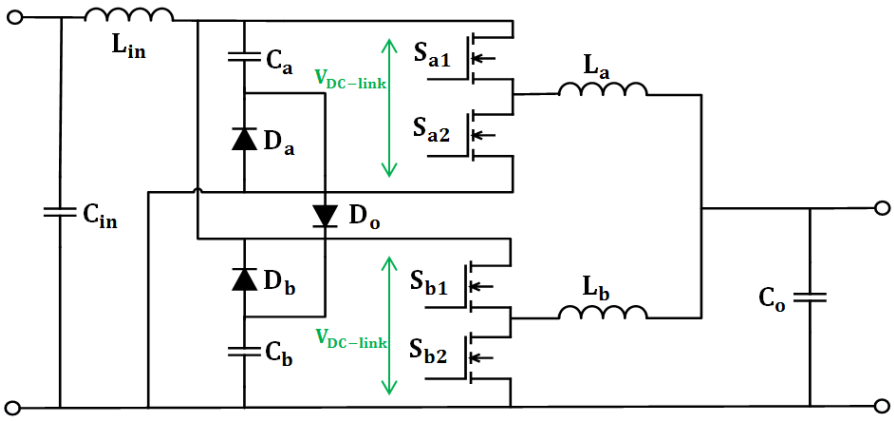
	V_o/ V_{in}	Component count		Highest device voltage stress	
		Switch	Diode	Switch	Diode
Cascaded buck	D^2	2	2	V_{in}	V_{in}
Quadratic buck	D^2	1	3	$V_{in}+ V_o/D$	$V_{in}+ V_o/D$
Switched-capacitor buck	$\frac{D}{2-D}$	1	4	$2V_o/D$	V_o/D
Switched-inductor buck	$\frac{D}{2-D}$	1	2	$2V_o/D$	V_o/D
Coupled-inductor buck	$\frac{D}{2-(2-N)D}$	1	1	$V_{in}+ V_o/N$	$\frac{1}{1+N}(V_{in}- V_o)+V_o$

Due to its potential for high efficiency and high power density, the switched-capacitor buck converter was selected for detailed study for this application. The previously published work on the circuit has only examined its performance at a lower power of less than 100 W, such as demonstrated in [131-133], and the potential suitability of the circuit for use with WBG devices has not been assessed. Also, the circuit analysis during the switching transients and the understanding of the impact of the circuit parasitic components on the converter performance are still quite limited, which all strengthens the case for a detailed examination of the topology.

Fig. 4.1 (a) shows the circuit schematic of the switched-capacitor synchronous buck converter, which consists of input inductor L_{in}, input capacitor C_{in}, switched capacitors C_a and C_b, and diodes D_a, D_b and D_0 in the front end, followed by a transistor half bridge. To enable the circuit to deliver the high output current whilst allowing reductions in the input and output filter components, an interleaved switched-capacitor synchronous buck converter is proposed in this chapter, shown in Fig. 4.1 (b).



(a)



(b)

Fig. 4.1. Circuit schematic of (a) switched-capacitor step-down converter and (b) proposed interleaved switched-capacitor step-down converter

4.3 Circuit operation principle at steady-state

The ideal waveforms of the proposed converter, Fig. 4.1 (b) at steady-state are shown in Fig. 4.2.

During 0~DT, the top device S_{a1} in leg *a* turns on, the two switched capacitors C_a and C_b are discharged in parallel by the current in the output inductor L_a minus the current in the input inductor L_{in}. The current in L_a rises linearly. Meanwhile, since the top device S_{b1} in phase b is off, the inductor current i_{Lb} freewheels through S_{b2}.

During DT~T/2, the top device S_{a1} in leg *a* turns off, the two switched capacitors C_a and C_b are charged in series by the current in the input inductor L_{in}. The output inductor L_a is discharged as its current freewheels through S_{a2}.

During T/2~T, the behaviour of the two phases is exchanged with S_{b1} turning on for a time DT whilst S_{a2} remains off.

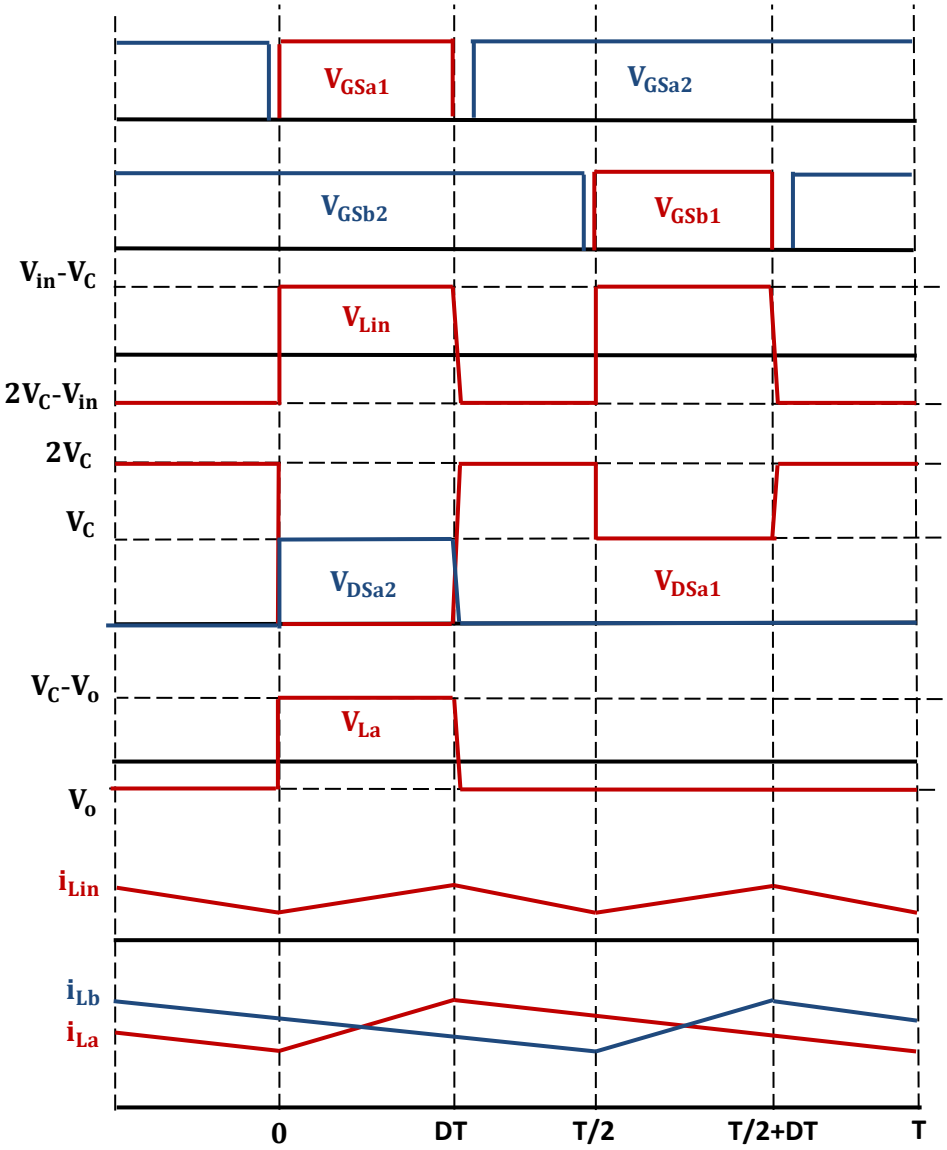


Fig. 4.2. Ideal operation waveforms of the interleaved switched-capacitor step-down converter

The volt-seconds balance of the input inductor L_{in} and the output inductor L_a can be used to obtain the conversion ratio of the converter, where the voltage across C_a and C_b are assumed to be equal and given by V_C.

$$(V_{in} - V_C)DT = (2V_C - V_{in})(T/2 - DT) \tag{4-1}$$

$$(V_C - V_o)DT = V_0(1 - D)T \tag{4-2}$$

Eliminating V_C from (4-1) and (4-2),

$$\frac{V_o}{V_{in}} = \frac{D}{2(1-D)} \tag{4-3}$$

From the operation waveforms in Fig. 4.2, it can be seen that the transistor duty-ratio must be limited to less than 0.5 to allow time for the input inductor voltage to reverse.

Fig. 4.3 compares the voltage conversion ratios of three topologies buck, switched-capacitor buck and interleaved switched-capacitor buck. It can be seen that the switched-capacitor topologies show greater step-down ratios than the conventional buck topology, whilst the interleaved operation slightly reduces the step-down ratio compared to the original SC buck converter shown in Fig. 4.1 (a).

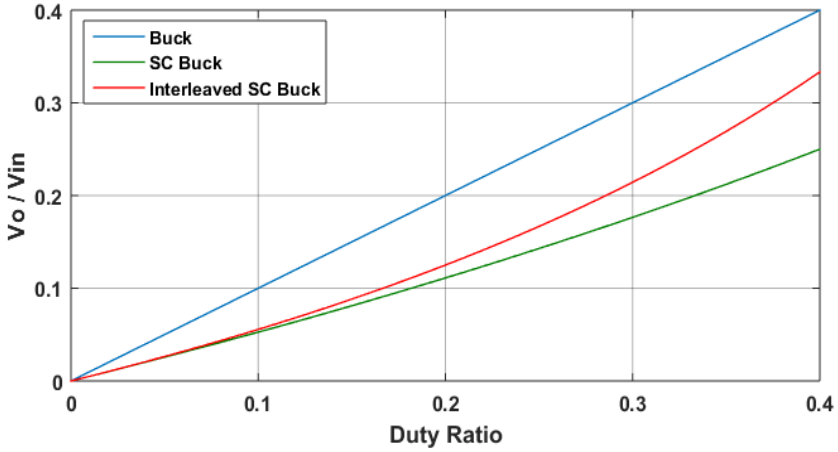


Fig. 4.3. Conversion ratio of buck, switched-capacitor buck and interleaved switched-capacitor buck topologies

4.4 Circuit analysis during switching transients

In order to evaluate the impact of the device parasitic capacitance and the advantages of using WBG devices, the circuit performance during the switching transients needs to be fully understood. Fig. 4.4 depicts the theoretical voltage and current waveforms of the top and bottom devices in leg *a* on an expanded time scale. The waveforms assume the device output capacitances are linear and that the transistor channel currents rise and fall linearly at the switching instants. V_{Lin} is the voltage across the input inductor, $V_{DC\text{-}link}$ is the input voltage across the two switching legs and V_{La} is the voltage across output inductor L_a. The current in the transistors, i_{DSa1} and i_{DSa2} are split into two components: the channel current, $i_{channel\_Sa1}$ and $i_{channel\_Sa2}$, and the current in the output capacitance, i_{oss_Sa1} and i_{oss_Sa2}.

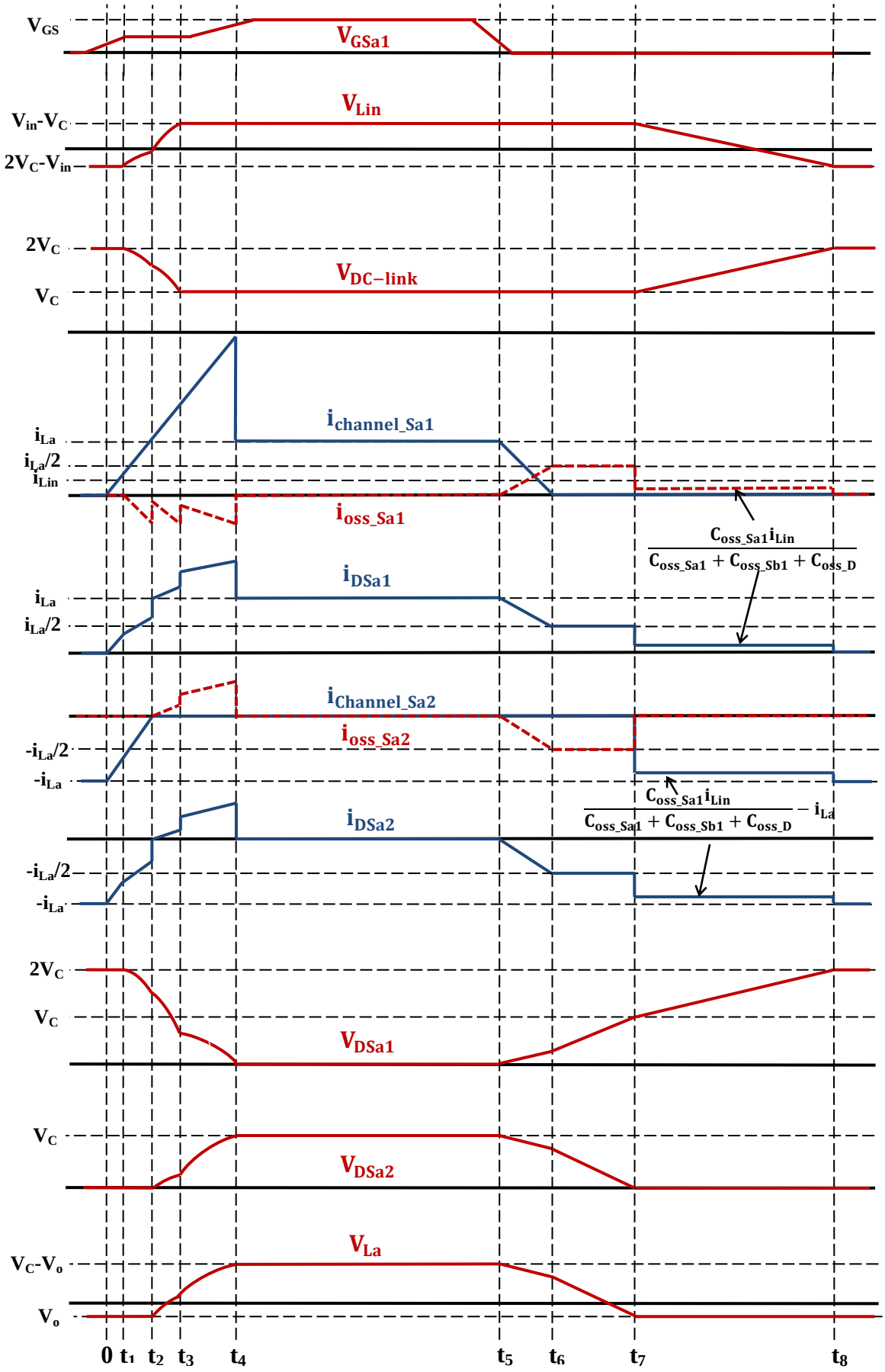


Fig. 4.4. Converter ideal operation waveforms during switching transients

4.4.1 Sub-Period 0~t_1

Initially the input inductor current flows in D_0 charging C_a and C_b whilst the output inductor currents freewheel in S_{a2} and S_{b2}. This sub-period starts when the top device in phase *a* S_{a1} is switched on, the inductor current i_{La} starts to commutate from the bottom device S_{a2} to S_{a1} whilst the inductor current in phase *b* stills freewheels through the bottom device S_{b2}. The circuit operation during this sub-period is shown in Fig. 4.5. This sub-period ends when i_{DSa1} has risen to the input inductor current level, i_{Lin}, and D_0 turns off.

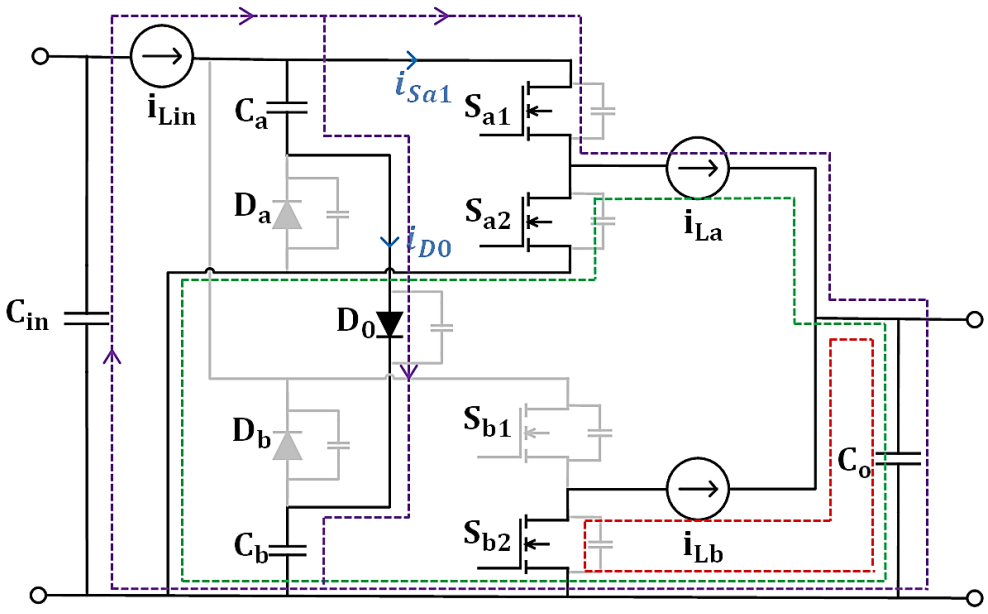


Fig. 4.5. Circuit operation during 0~t_1

4.4.2 Sub-Period t_1~t_2

During this sub-period i_{DSa1} continues to rise towards i_{La}. The difference between i_{La} and i_{Lin} flows in the output capacitances of diodes D_a, D_b and D_0 as the DC link voltage starts to fall from $2V_C$ towards V_C. The output capacitances of S_{a1} and S_{b1} also start to discharge. The circuit operation is shown in Fig. 4.6. The current and voltage relationships during this sub-period can be expressed by (4-4) and (4-5). i_{oss} represents the charging/discharging current of the device output capacitance. This stage ends when i_{Sa1} reaches i_{La} and the current in S_{a2} is reduced to zero.

$$i_{oss\_Da}(t) + i_{oss\_Db}(t) - i_{oss\_D0}(t) + i_{DSa1}(t) + i_{oss\_Sb1}(t) = i_{Lin} \tag{4-4}$$

$$\frac{dV_{Da}(t)}{dt} = \frac{dV_{Db}(t)}{dt} = -\frac{dV_{D0}(t)}{dt} = \frac{dV_{DSb1}(t)}{dt} = \frac{dV_{DSa1}(t)}{dt} = -\frac{dV_{Lin}(t)}{dt} \tag{4-5}$$

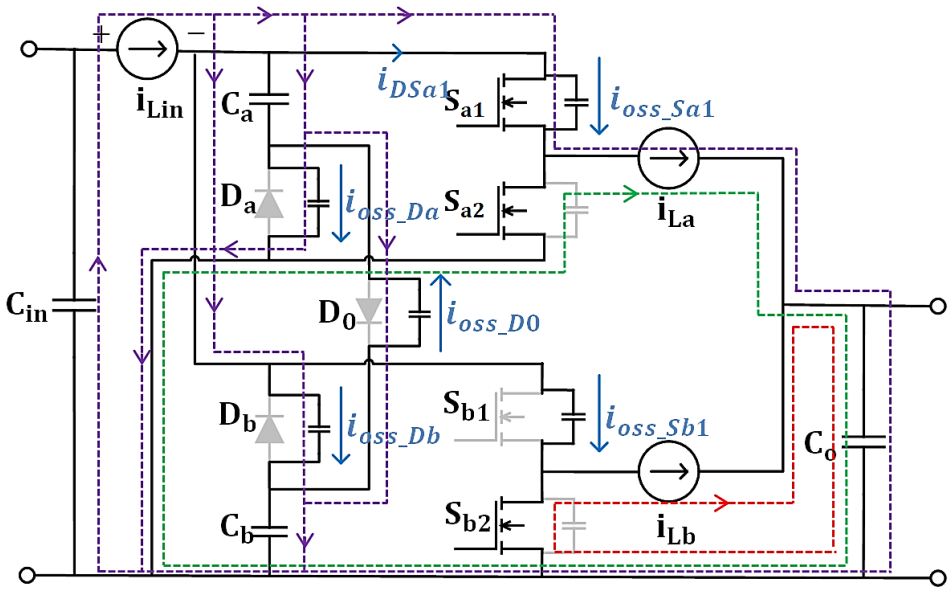


Fig. 4.6. Circuit operation during t_1~t_2

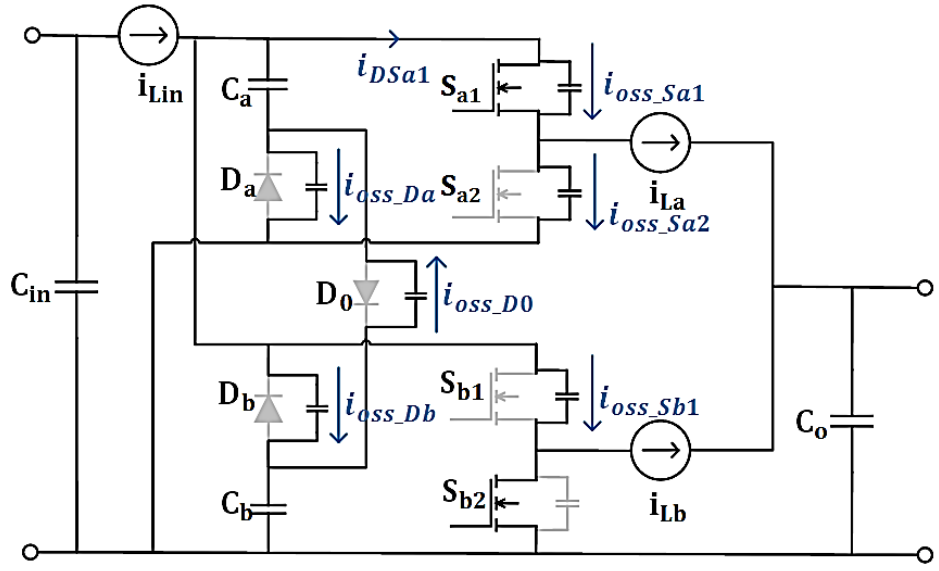


Fig. 4.7. Circuit operation during t_2~t_3

4.4.3 Sub-Period t_2~t_3

The inductor current commutation from S_{a2} to S_{a1} completes at t_2 as i_{DSa1} becomes equal to the inductor current i_{La}. The output capacitor of S_{a2} is then charged and the output capacitor of S_{a1} continues to discharge. The input inductor voltage polarity reverses during this stage. The circuit operation during this sub-period is shown in Fig. 4.7 and the voltage and current equations are given in equation (4-6) to (4-8). This stage ends when the DC link voltage reduces by half and D_a and D_b are forward biased.

$$i_{oss\_Da}(t) + i_{oss\_Db}(t) - i_{oss\_D0}(t) + i_{DSa1}(t) + i_{oss\_Sb1}(t) = i_{Lin} \quad (4\text{-}6)$$

$$i_{DSa1}(\mathrm{t}) - i_{oss\_Sa2}(\mathrm{t}) = i_{La} \quad (4\text{-}7)$$

$$\frac{dV_{Da}(\mathrm{t})}{dt} = \frac{dV_{Db}(\mathrm{t})}{dt} = -\frac{dV_{D0}(\mathrm{t})}{dt} = \frac{dV_{DSb1}(\mathrm{t})}{dt} = \frac{d[V_{DSa1}(t)+V_{DSa2}(t)]}{dt} = -\frac{dV_{Lin}(\mathrm{t})}{dt} \quad (4\text{-}8)$$

4.4.4 Sub-Period t_3~t_4

During this stage, the DC link voltage is clamped to V_C since D_a and D_b are forward biased. The output capacitors of S_{a1} and S_{a2} continue to charge and discharge until the voltage across S_{a2} rises to V_C and the voltage across S_{a1} falls to zero, by which time the charging and discharging of the parasitic capacitance is complete and the current in S_{a1} falls to be equal to i_{La}. The circuit operation during this sub-period is shown in Fig. 4.8, and the circuit equations are given in equation (4-9) and (4-10).

$$i_{DSa1}(\mathrm{t}) - i_{oss\_Sa2}(\mathrm{t}) = i_{La} \quad (4\text{-}9)$$

$$V_{DSa1}(\mathrm{t}) + V_{DSa2}(\mathrm{t}) = V_C \quad (4\text{-}10)$$

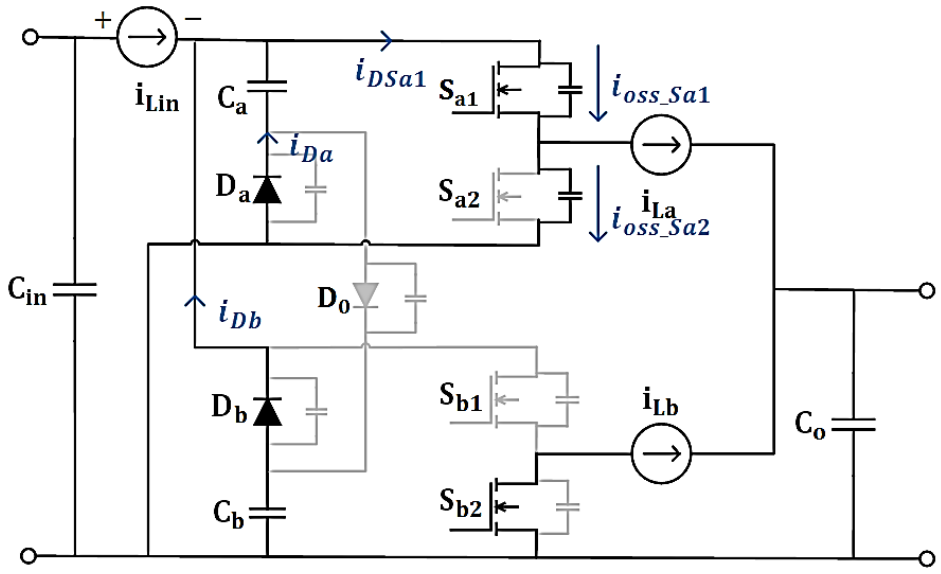


Fig. 4.8. Circuit operation during t_3~t_4

4.4.5 Sub-Period t_4~t_5

During this sub-period, S_{a1} is in the on-state and i_{La} rises linearly as shown in Fig. 4.2 and described in section 4.3. The circuit operation during this sub-period is shown in Fig. 4.9.

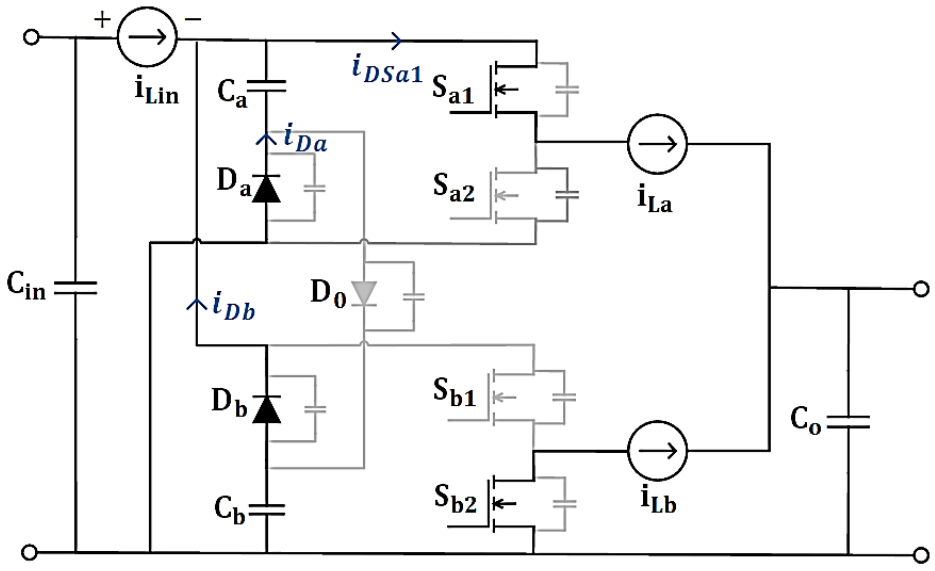


Fig. 4.9. Circuit operation during t_4~t_5

4.4.5 Sub-Period t_5~t_6

S_{a1} is signalled off at t_5 whilst S_{a2} remains in the off-state, and the channel current of S_{a1} starts to fall rapidly. The reduction in $i_{channel\_Sa1}$ diverts the output inductor current i_{La} to charge and discharge the output capacitance of S_{a1} and S_{a2}. This sub-period ends when $i_{channel\_Sa1}$ falls to zero and the S_{a1} channel turns off. The circuit operation during this sub-period is shown in Fig. 4.10. The current and voltage equations are the same as those of the turn-on sub-period t_3~t_4.

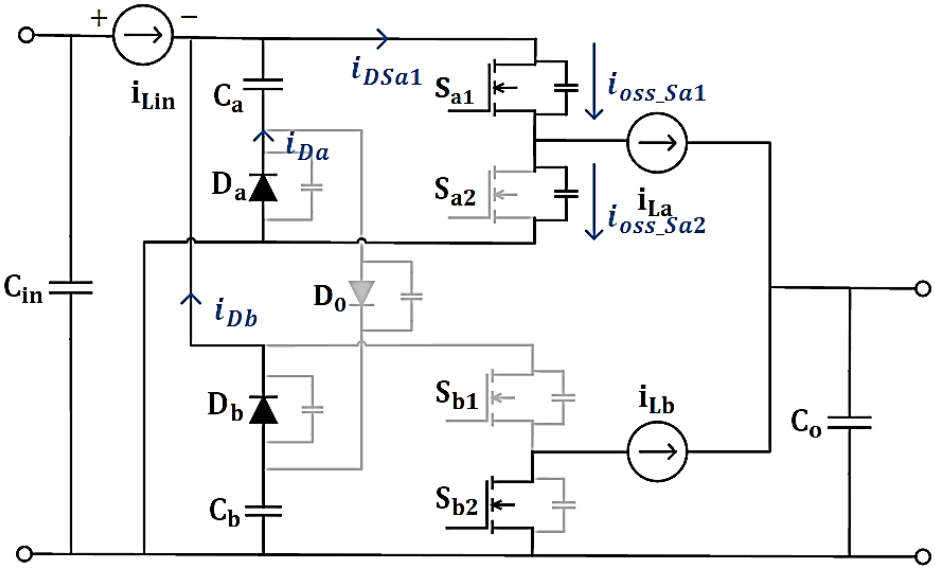


Fig. 4.10. Circuit operation during t_5~t_6

4.4.5 Sub-Period t_6~t_7

As the S_{a1} channel current falls to zero, the output capacitance of S_{a1} and S_{a2} are charged and discharged by the output inductor current i_{La}, which is assumed to be divided equally under the premise of linear and equal output capacitances for S_{a1} and S_{a2}. The circuit operation in this sub-period is shown in Fig. 4.11 and the main equations are given in equation (4-11) and (4-12). This stage ends when the output capacitance of S_{a2} is fully discharged, and V_{DSa2} falls to zero and V_{DSa1} rises to V_C.

$$i_{oss\_Sa1}(\mathrm{t}) - i_{oss\_Sa2}(\mathrm{t}) = i_{La} \tag{4-11}$$

$$V_{DSa1}(\mathrm{t}) + V_{DSa2}(\mathrm{t}) = V_C \tag{4-12}$$

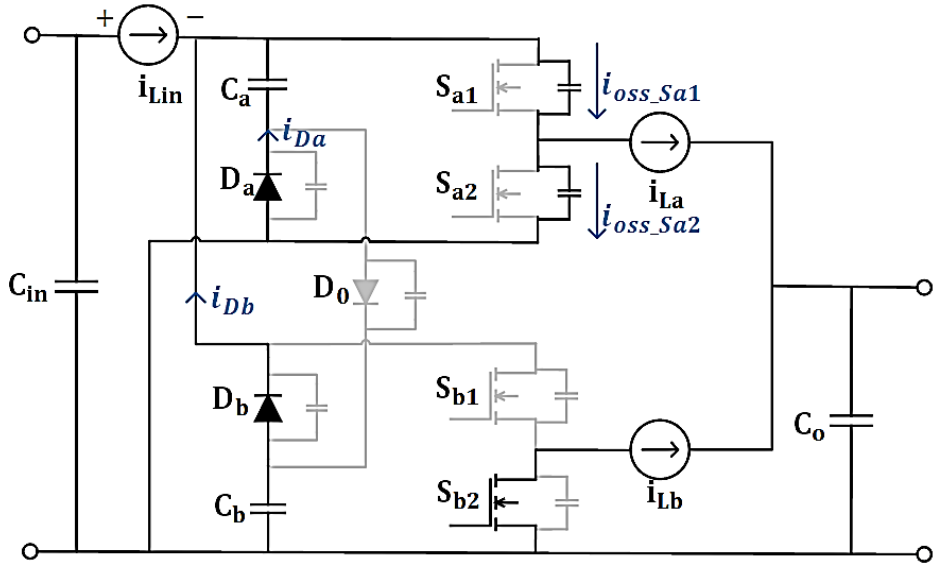


Fig. 4.11. Circuit operation during t_6~t_7

Due to the non-linearity of the device output capacitances, there will be a decreasing capacitive charging current in C_{oss_Sa1} as its voltage approaches V_C and an increasing capacitive discharging current in C_{oss_Sa2} as its voltage approaches zero during this sub-period. As the capacitive current i_{oss_Sa1} falls below the input current level i_{Lin}, diodes D_a and D_b will turn off and the input inductor current will start to charge the parasitic capacitance of D_a and D_b, causing the DC link voltage to increase, in which case the voltage relationship of S_{a1} and S_{a2} becomes as shown in (4-13) and (4-14).

$$V_{DSa1}(\mathrm{t}) + V_{DSa2}(\mathrm{t}) = V_C + V_{Da}(\mathrm{t}); \tag{4-13}$$

$$\frac{dV_{Da}(t)}{dt} = \frac{dV_{Db}(t)}{dt} = -\frac{dV_{D0}(t)}{dt} = \frac{d[V_{DSa1}(t)+V_{DSa2}(t)]}{dt} \qquad (4\text{-}14)$$

4.4.6 Sub-Period t_7~t_8

As the voltage across S_{a2} falls to zero, the output inductor current starts to freewheel through the anti-parallel diode of S_{a2}. The input inductor current i_{Lin} then charges and discharges the output capacitance of D_a, D_b and D_0. Due to the increase in the DC link voltage, the output capacitance of S_{a1} and S_{b1} are also charged. The charging current i_{oss_Sa1} causes a small reduction in i_{DSa2}, shown in (4-15). This sub-period ends when D_0 is forward biased and the DC link voltage is equal to $2V_C$. The circuit operation during this sub-period is shown in Fig. 4.12 and the main current equation is given in (4-15), where C_{oss_D} is the sum of the output capacitances of D_a, D_b and D_0. The duration of this stage depends on the input inductor current i_{Lin} and the sum of the parasitic capacitance. During sub-periods t_6~t_7 and t_7~t_8, the device output capacitances perform a turn-off snubber function for S_{a1}, restricting the rate of rise of voltage across the device and limiting the turn-off loss. Part of the stored charge will be released at the next turn on of the top device in leg *b* S_{b1}, and the remainder will be released when S_{a1} turns on.

$$i_{oss\_Sa1}(t) = i_{La} - i_{oss\_Sa2}(t) = \frac{C_{oss\_Sa1} i_{Lin}}{C_{oss\_Sa1}+C_{oss\_Sb1}+C_{oss\_D}} \qquad (4\text{-}15)$$

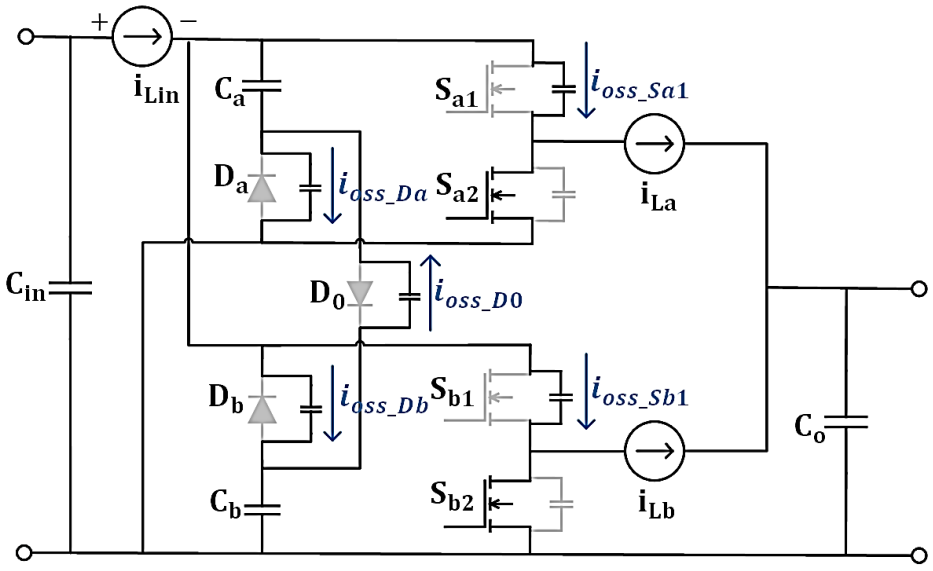


Fig. 4.12. Circuit operation during t_7~t_8

4.5 Converter parameter design and component selection

The converter was designed according to the initial specifications shown in Table 4.2, that are typical benchmarks for aerospace use or similar converter applications [136].

Table 4.2 Converter preliminary specification

Parameter	Value
Rated power	1.2 kW
Nominal input voltage	270 V
Nominal output voltage	28 V
Switching frequency	200 kHz
Input inductor currnet ripple	30%
Output inductor currnet ripple	20%
Input voltage ripple	1%
Output voltage ripple	1%
Ambient temperature	25 ℃

The input inductor current ripple is designed to be smaller than 30% of the input current. As a voltage of V_{in}-V_C is impressed across the input inductor during the on-state of the top devices, the inductance can be determined by (4-16).

$$L_{in} = \frac{(V_{in} - V_C)DT}{\Delta i_{Lin}} \tag{4-16}$$

The input capacitor C_{in} supplies the ripple current of the input inductor L_{in}, and is sized to keep the input voltage ripple lower than 1%, given by (4-16). The capacitance can be determined by (4-17).

$$\Delta V_{Cin} = \frac{1}{C_{in}} \times \frac{1}{2} \times \frac{\mathrm{T}}{4} \times \frac{\Delta i_{Lin}}{2} \tag{4-17}$$

$$C_{in} = \frac{\Delta i_{Lin}}{16 f \Delta V_{Cin}} \tag{4-18}$$

The switched capacitors supply the transistor current and are sized to have a voltage ripple of lower than 1%. During the off-state of the top devices, the switched capacitors C_a and C_b are charged in series by the input inductor current i_{Lin}. The capacitors ripple voltage is therefore given by (4-19), and the capacitance can be determined by (4-20).

$$\Delta V_C = \frac{1}{C_a} \times \left(\frac{\mathrm{T}}{2} - DT\right) \times i_{Lin-avg} = \frac{1}{C_b} \times \left(\frac{\mathrm{T}}{2} - DT\right) \times i_{Lin-avg} \tag{4-19}$$

$$C_a = C_b = \frac{(1-2D)Ti_{Lin\_avg}}{2\Delta V_C} \quad (4\text{-}20)$$

where $\Delta V_C=\Delta V_{Ca}=\Delta V_{Cb}$

The output inductor current ripple is designed to be smaller than 20% of the output current, and the inductor values can therefore be determined by (4-21).

$$L_a = L_b = \frac{V_0(1-D)T}{\Delta i_{Lo}} \quad (4\text{-}21)$$

where $\Delta i_{Lo}=\Delta i_{La}=\Delta i_{Lb}$

The output capacitor current ripple Δi_{Co} is the sum of the output inductor ripples taking account of their interleaved relationship as given by [137]. The output capacitor C_o filters the output current ripple and is sized to maintain the output voltage ripple lower than 1%. The capacitance can be determined by (4-23).

$$\Delta i_{Co} = \frac{1-2D}{1-D}\Delta i_{Lo} \quad (4\text{-}22)$$

$$C_o = \frac{\Delta i_o T}{8\Delta V_{Co}} \quad (4\text{-}23)$$

Table 4.3 summarises the design criteria of the converter main component parameters.

Table.4.3 Converter key components parameters

Parameter	Value	Design Criteria
D	0.172	$\frac{V_o}{V_{in}} = \frac{D}{2(1-D)}$
Input capacitor C_{in}	4 µF	$\Delta V_{Cin}/V_{in} \leq 1\%$; equation (4-17)
Input current i_{Lin_avg}	4.4 A	$i_{Lin\_avg} = \frac{P_{in}}{V_{in}}$
Input inductor L_{in}	75 µH	$\Delta i_{Lin}/i_{Lin-avg} \leq 30\%$; equation (4-18)
Switched capacitors C_a, C_b	8.8 µF	$\Delta V_C/V_C \leq 1\%$; equation (4-20)
Output inductor current i_{Lo_avg}	20.4 A	Assuming $\eta = 95\%$; $i_{Lo\_avg} = \frac{P_{in}\eta}{2V_o}$
Main inductors L_a, L_b	33 µH	$\Delta i_{Lo}/i_{Lo-avg} \leq 20\%$; equation (4-21)
Output capacitor C_o	6.6 µF	$\Delta V_{Co}/V_o \leq 1\%$; equation (4-23)

4.6 Prototype description

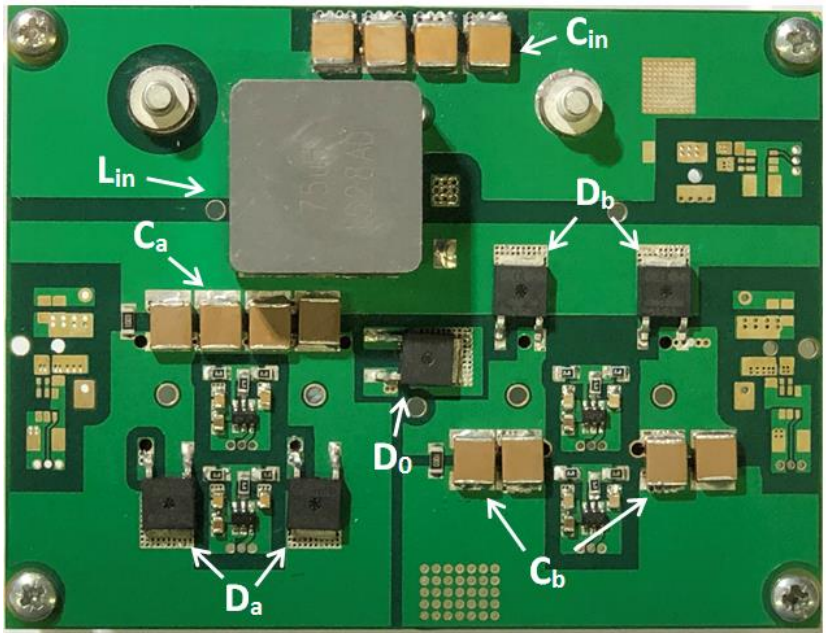
A converter prototype was constructed to demonstrate the topology and evaluate the circuit performance. The prototype comprised three circuit blocks: the digital interface circuit, the main switching circuit and the output filter circuit.

The digital interface circuit provides decoupled, isolated logic signals for the transistor drivers. The circuit was built on a two-layer PCB. A microcontroller, UCD3138064, from TI was connected to the circuit board to generate the 0-3.3 V PWM signals, which were converted to 0-5 V PWM signals through logic buffers to avoid the impact of unwanted capacitive coupling. The signal isolation was provided by opto-couplers, ACPL-P484, with high common mode rejection (CMR) performance from Broadcom. The isolated control signals were then sent to the driving ICs. An isolated power supply, ISE0506A from XP Power, was used to power the opto-couplers and driving ICs.

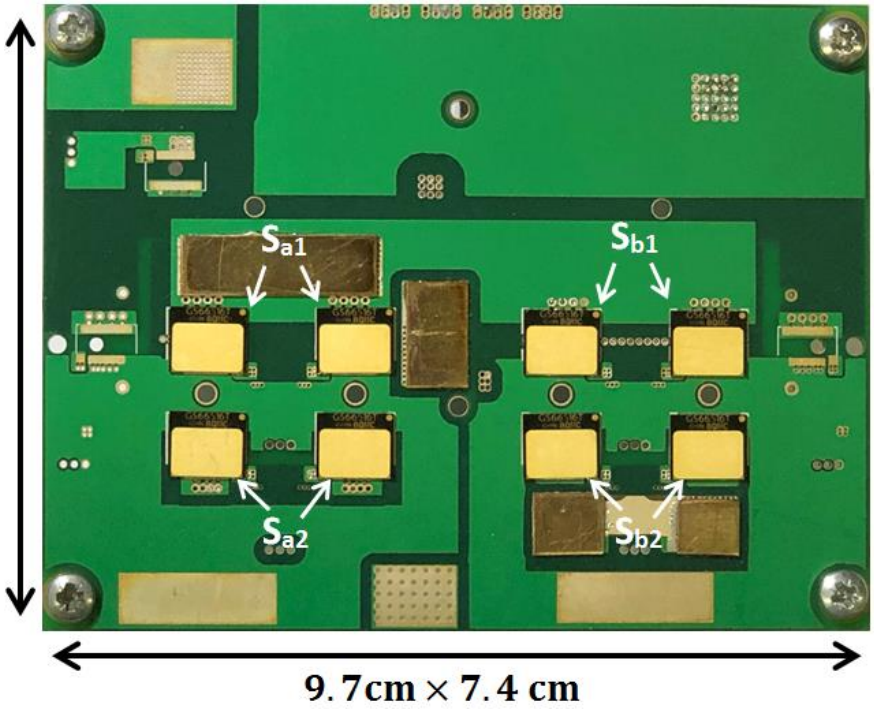
Since the switched capacitors C_a and C_b and diodes D_a, D_b and D_0 all form part of the current commutation loop for the main transistors, minimising the layout inductance of this part of the converter is a high priority. The main switching circuit was built on a four-layer PCB, consisting of the input inductor, input capacitors, main transistors, switched diodes and switched capacitors. Two adjacent layers were used to create vertical loops with minimal size for the gate drive connections and the main circuit current commutation. Surface-mount devices were adopted for the main switching circuit due to the smaller package inductance. Eight top-cooled GaN HEMTs, GS66516T, 650 V/60 A, from GaN Systems were selected to form the transistor half-bridge legs. Two devices were used in parallel for each switch. Four GaN-FET gate driving ICs, LM5114, from TI were used to drive the main transistors. Two paralleled transistors were driven by a single driver to ensure synchronous switching. Five SiC diodes, C3D10065E, 650 V/ 15 A, from CREE were used to form the main switched diodes. Two devices were used in parallel for D_a and D_b whilst D_o was formed by a single device. The device has a small package size and a low output charge. A SMD inductor, IHLP-8787MZ-5A, 75 μH/ 12 A, from VISHAY was used as the input inductor.

An insulated metal substrate (IMS) board with high thermal conductivity, T-Clad HR T30.20, was used for the output filter circuit, which consisted of two power inductors, AGP4233, 33 μH/ 22.5 A, from Coilcraft and three 2.2 μF ceramic capacitors.

Fig. 4.13 shows the top and bottom of the four-layer PCB. All the top-cooled transistors are mounted on the bottom side for better thermal performance. The converter prototype is shown in Fig. 4.14 and the three circuit blocks are indicated. Including the heatsink, the overall volume of the prototype was $20\times10\times4.3$ cm^3 (0.86 Litre).



(a)



(b)

Fig. 4.13. Main switching circuit board (a) top side (b) bottom side

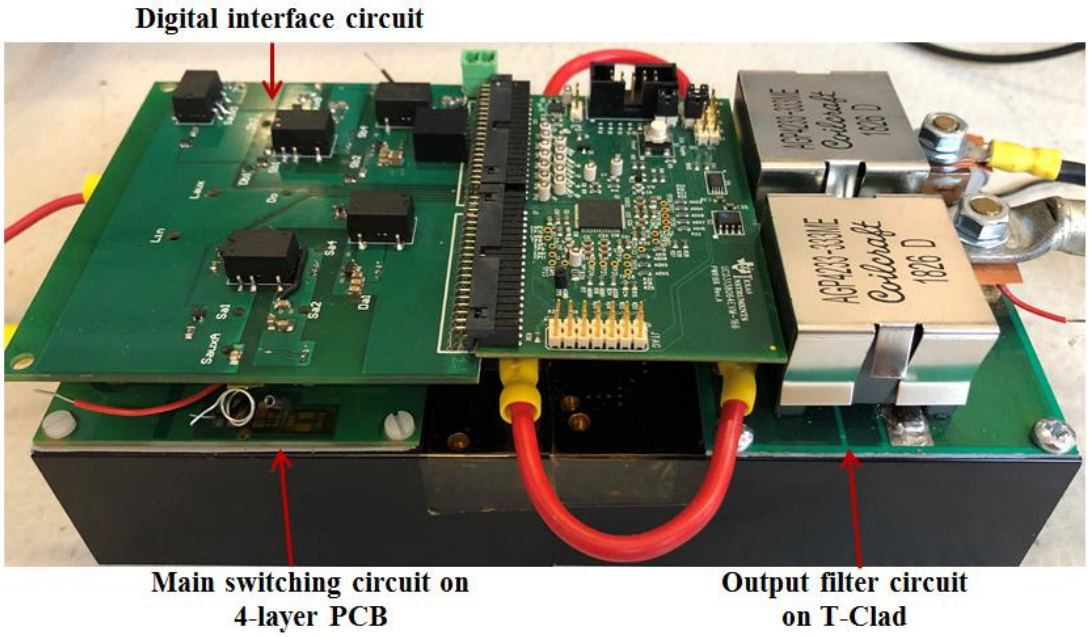


Fig. 4.14. Converter prototype

4.8 Converter thermal management

The top-cooled GaN HEMTs (GS66516T) were mounted on the bottom side of the PCB, and the heat was conducted directly to the natural convection heatsink through thermal interface material (TCIM 3.0 from MTC) with a thermal conductivity of 3 W/mK and a thickness of 0.25 mm, providing a shorter thermal path than conventional bottom-cooled devices.

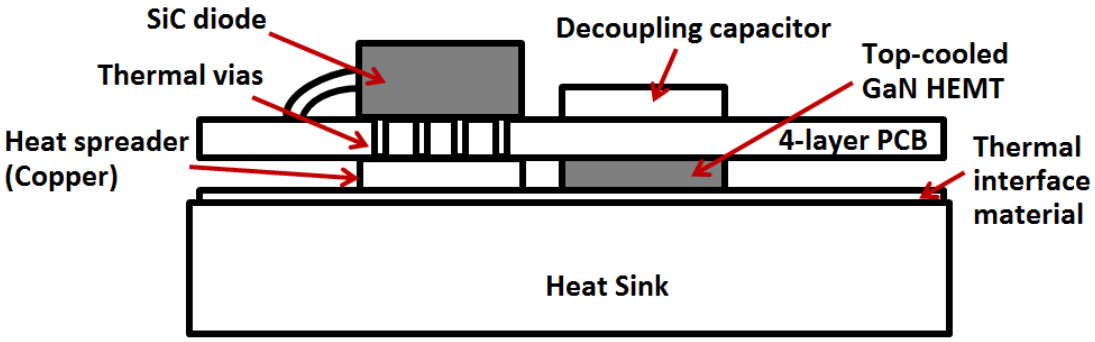


Fig. 4.15. Cross-sectional view of the converter and thermal arrangements

A cross sectional view illustrating the construction and thermal paths is shown in Fig. 4.15. The SiC diodes (C3D10065E) were mounted on the top side of the PCB. A number of thermal vias were placed under the diodes to reduce the PCB thermal resistance. Copper pieces with the same height as the GaN transistors were soldered on the bottom side of the

PCB, serving as heat spreaders and gap spacers between the PCB and thermal interface material. The inductors were naturally air cooled.

The thermal equivalent circuit for the transistors and diodes is shown in Fig. 4.16. The device junction-to-case thermal resistance is taken from the datasheet, and the various material thermal resistances were calculated using (4-24), summarised in Table 4.4.

$$R_\theta = \frac{T_M}{A_C \times K} \tag{4-24}$$

where T_M is the thickness of the material, A_C is the contact area and K is the material thermal conductivity, $R_{JC\text{-}D}$, $R_{JC\text{-}S}$, R_{TIM1} and R_{TIM2} denote the junction-to-case thermal resistances of the diodes, transistors and the thermal resistances of the thermal interface material between diodes and transistors, and heatsink.

Table 4.4 Components thermal resistance

$R_{JC\text{-}D}$	R_{PCB}	R_{Copper}	R_{TIM1}	$R_{JC\text{-}S}$	R_{TIM2}	R_{HSA}	Unit
1	5.1	0.001	0.7	0.3	1.8	1.4	℃/W

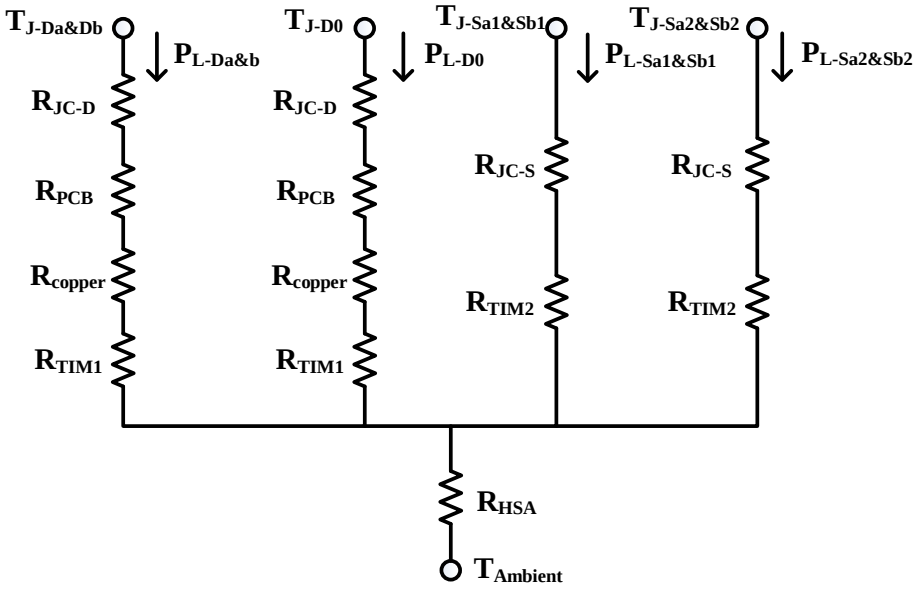


Fig. 4.16. Converter thermal equivalent circuit

4.9 Converter simulation model

The simulation model was built in LTSpice, taking advantage of the GaN HEMT and SiC diode SPICE models provided by the manufacturers, which include all the general electrical parameters as well as the voltage-dependent parasitic capacitance and package

stray inductance. The transistor SPICE model also takes into account the device thermal impedance, parameter variation due to the device self-heating and allows the observation of the junction temperature. The converter thermal model was established based on the equivalent thermal circuit shown in Fig. 4.16.

The impact of parasitic capacitance of the PCB and inductors should not be neglected for high-frequency operation. The parasitic capacitances of the PCB and the inductors were measured using an impedance analyser. The capacitance of the inductors was found from the self-resonant frequency. The results are shown in Table 4.5.

Table 4.5 Circuit parasitic capacitance

Parasitic capacitance		Value
Input inductor L_{in}		69.8 pF
Output inductor L_o		7.5 pF
PCB	Contribution to top device $S_{a1\&b1}$	29.6 pF
	Contribution to bottom device $S_{a2\&b2}$	154.8 pF
	Contribution to DC link	781.8 pF

The DC and AC winding resistances of the inductors were measured with the impedance analyser. The results are shown in Table 4.6.

Table 4.6 Inductors winding resistance

	R_{DC}	$R_{AC@200kHz}$	$R_{AC@400kHz}$
Input inductor L_{in}	29.8 mΩ	935 mΩ	1.8 Ω
Output inductor $L_{a\&b}$	2.8 mΩ	914 mΩ	1.4 Ω

The ambient temperature was set to 25℃. The simulation was run until the transistors reached thermal steady-state. The simulation output results for operation at 270-28 V, f=200 kHz, P_o=1.2 kW, D=0.17 are shown in Table 4.7.

Table 4.7 Converter simulation output results

Output power P_o	1.2 kW
Output voltage V_o	27.9 V
L_{in} current ripple Δi_{Lin}	30.7%
$L_{a\&b}$ current ripple $\Delta i_{La\&b}$	16.7%
C_{in} voltage ripple ΔV_{Cin}	<1%
$C_{a\&b}$ voltage ripple $\Delta V_{Ca\&b}$	<1%
C_o voltage ripple ΔV_{Co}	<1%

The steady-state simulation waveforms over one cycle are shown in Fig. 4.17. The expanded simulation waveforms during the switching transient of top device S_{a1} are presented in Fig. 4.18 and Fig. 4.19. The simulation results show the current in an individual transistor, which is half the total switch current since each switch comprises two transistors in parallel.

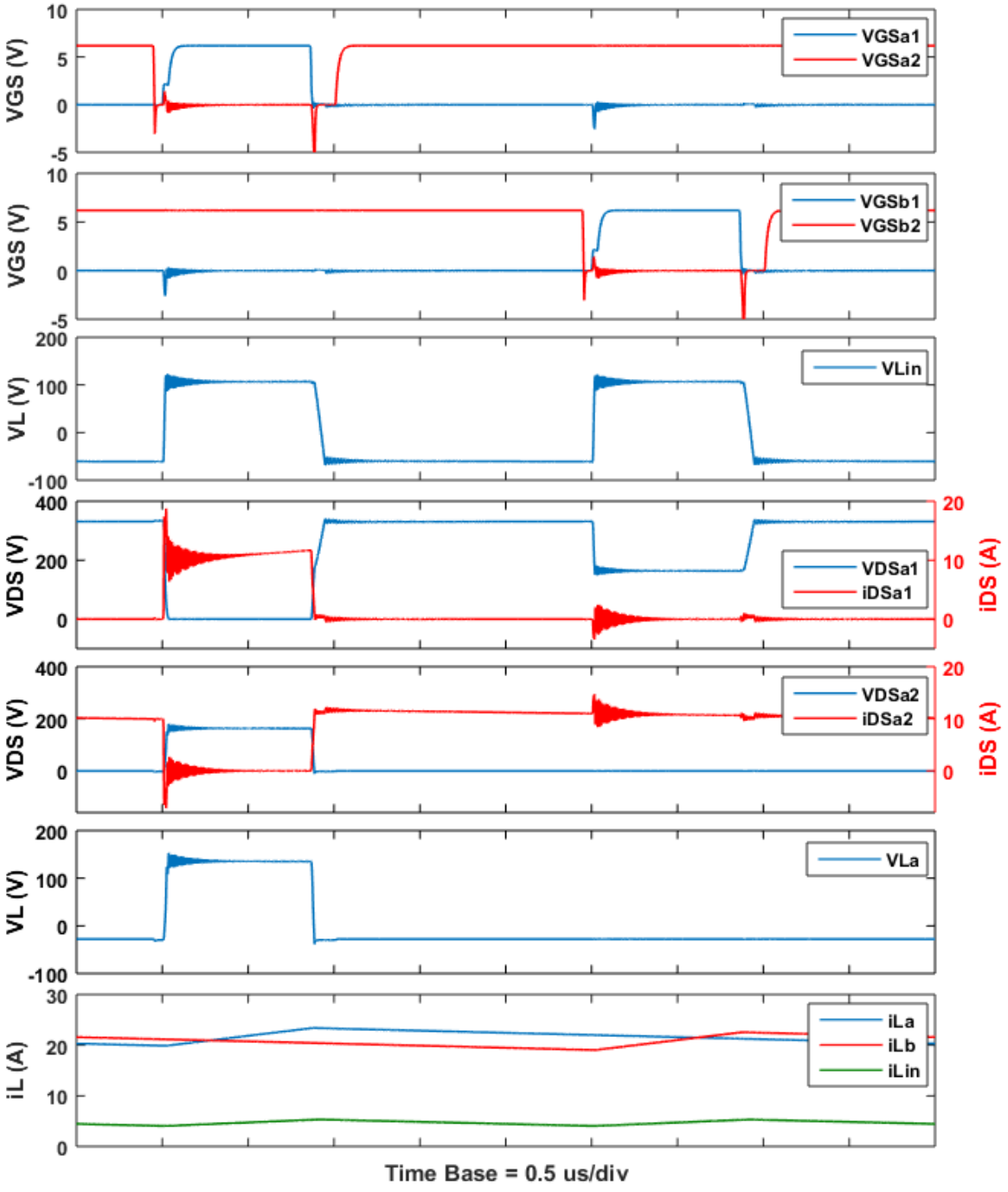


Fig. 4.17. Simulation results of the converter operating at 270-28 V, 200 kHz, 1.2 kW

It is evident that the simulation results are quite consistent with the theoretical waveforms shown in Fig. 4.2. Current and voltage oscillations can be observed in S_{a1} during the turn-on transient due to resonance between the device output capacitance and parasitic inductance. It can be seen that when the top device in leg *b* S_{b1} turns on, the output capacitance of S_{a1} is discharged, causing a voltage reduction in V_{DSa1}. The input inductor voltage changes direction at the switching instants. The input inductor current ripple is at twice the switching frequency due to the interleaving between the two legs. It can be seen that the voltage slew rate during the turn-off transient of the top devices is reduced due to the snubber effect of the parasitic capacitance, indicating that the turn-off switching loss in the transistors is significantly reduced, however the energy stored in the parasitic capacitance will be dissipated in the transistors at the turn-on instants.

Fig. 4.18 and Fig. 4.19 show the simulation waveforms during then turn-on and turn-off transients of S_{a1}, corresponding to the theoretical waveforms shown in Fig. 4.4.

It can be seen from Fig. 4.18 that the DC link voltage transition starts when the top device current reaches $i_{Lin}/2$ at t_1 ($i_{Lin}/2$ as two transistors are used in parallel) as predicted, and the input inductor voltage V_{Lin} begins to reverse as the front-end diodes are charged and discharged. The current continues to rise until i_{DSa1} reaches $i_{La}/2$ at t_2, and the output capacitor of S_{a2} starts to be charged. Due to the very fast turn-on speed of the GaN HEMT channel, sub-period $0\sim t_2$ only lasts for 2.4 ns. However, the following sub-period $t_2\sim t_4$ is extended due to the charge/discharge of the associated parasitic capacitances in the circuit, which lasts for 28.2 ns.

It can be seen from Fig. 4.19 that the dv/dt during the turn-off transient is much slower than at turn on due to the charging of the parasitic capacitances that act as snubber capacitances. It is seen that the drain currents of S_{a1} and S_{a2} change to $i_{La}/4$ at t_6, indicating that the channel current of S_{a1} has fallen to zero as shown in Fig. 4.4. As predicted, the capacitive charging/discharging currents are not constant during $t_6\sim t_7$ due to the non-linearity of the device output capacitance. The charging phases $t_5\sim t_7$ and $t_7\sim t_8$ are associated with output capacitance of the transistor leg and the front-end diodes respectively, which last for 18.5 ns and 62.1 ns. During the turn-off transient, $t_6\sim t_8$ is a lossless capacitive charging phase, and only a small loss occurs in the transistors during $t_5\sim t_6$.

The converter thermal model was built based on the thermal equivalent circuit shown in Fig. 4.16. The device junction temperatures for S_{a1} and S_{a2} at steady-state were measured to be 71℃ and 44℃ respectively. The higher temperature of S_{a1} is due to the turn-on losses associated with the discharge of the parasitic capacitance and is discussed in more detail in sections 4.4.2~4.4.4.

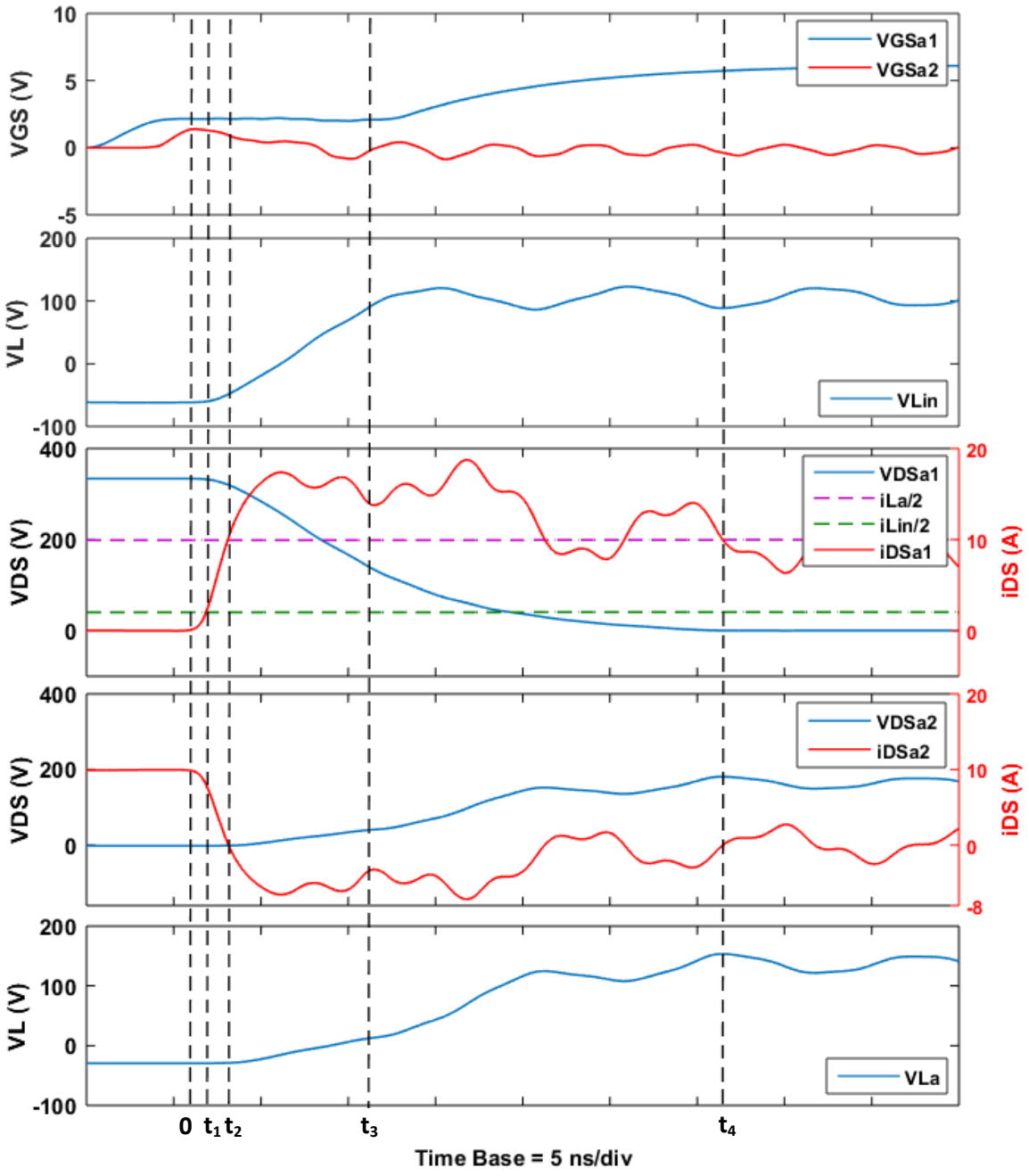


Fig. 4.18. Simulation results during the S_{a1} turn-on transient for the converter operating at 270-28 V, 200 kHz, 1.2 kW

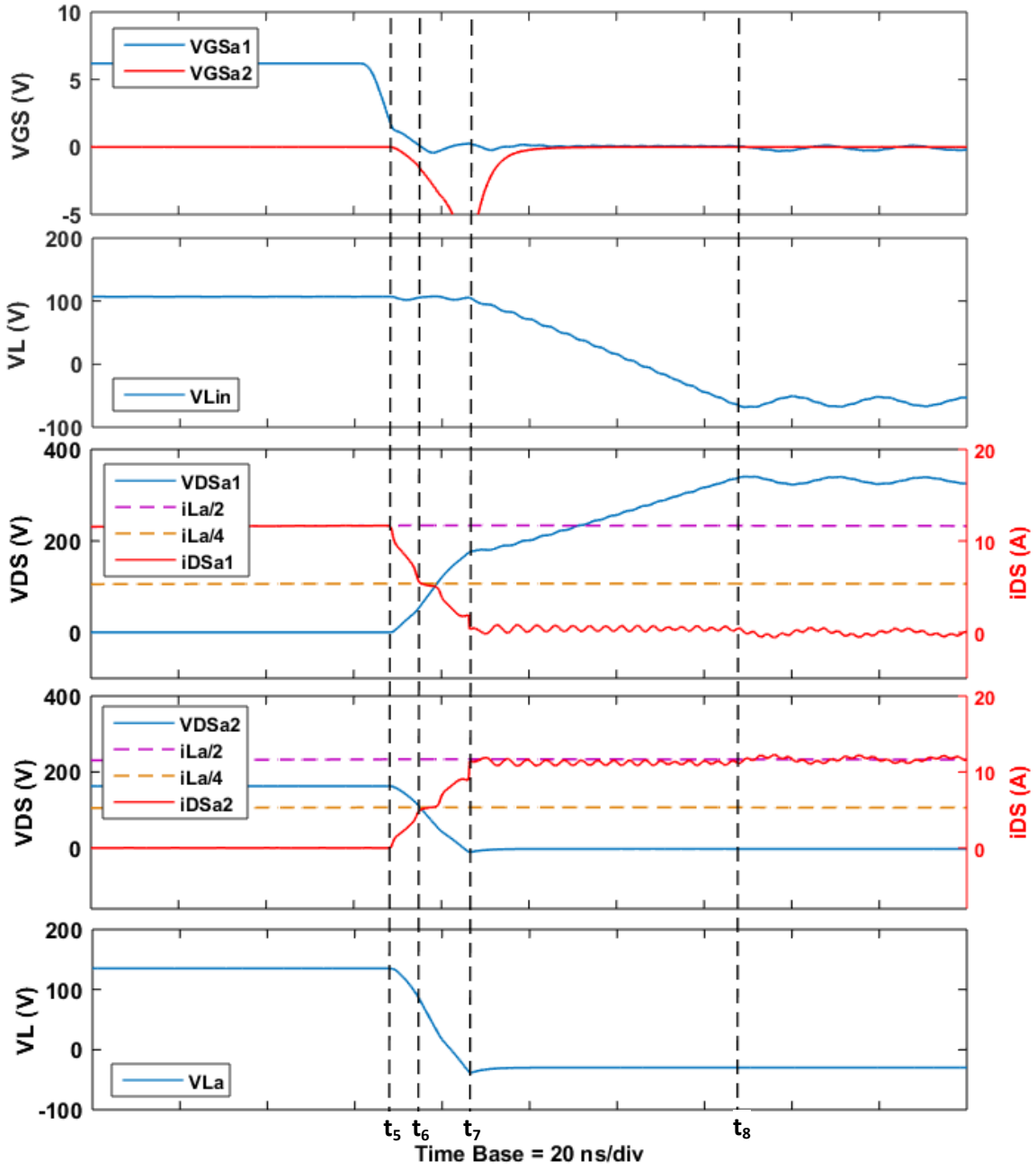
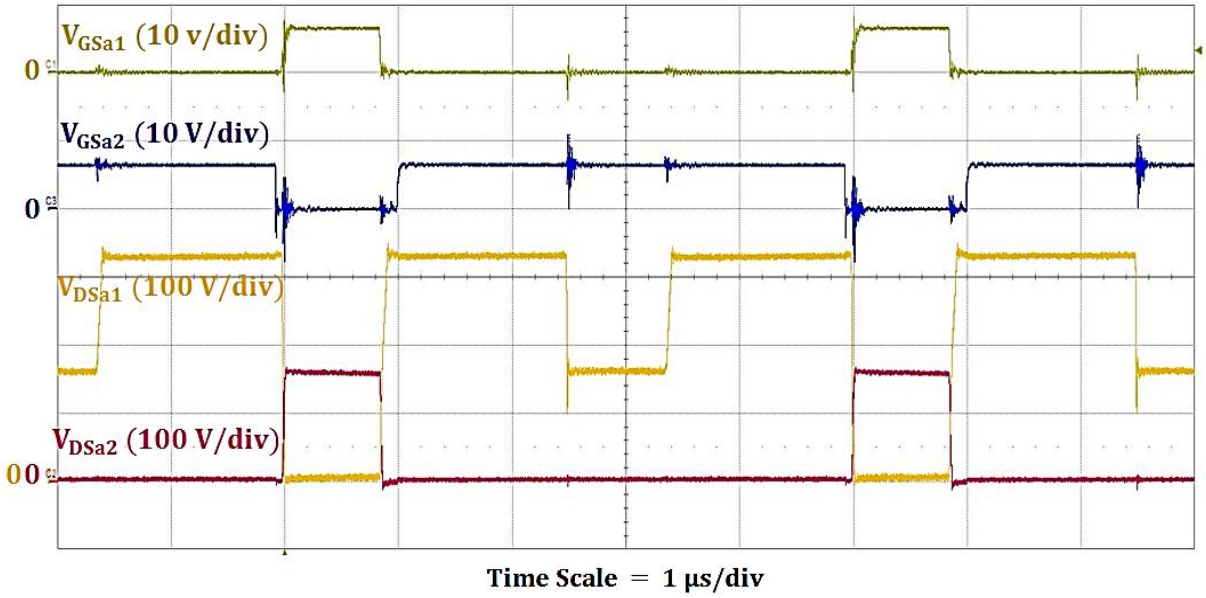


Fig. 4.19. Simulation results during the S_{a1} turn-off transient for the converter operating at 270-28 V, 200 kHz, 1.2 kW

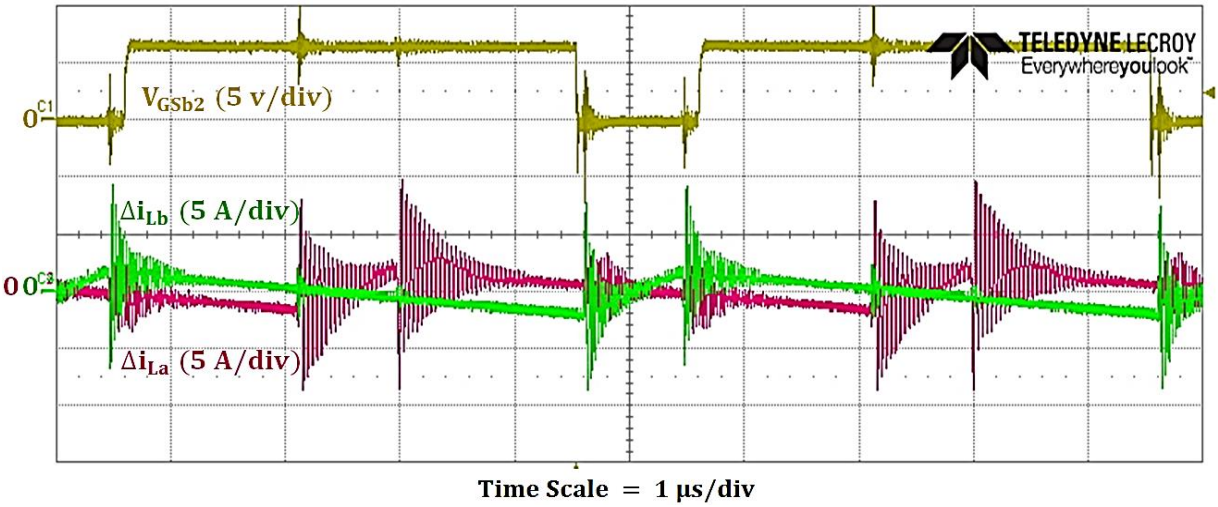
4.10 Experimental results

The prototype was tested up to 1.2 kW. The transistor duty ratio was set to 0.17. The dead time between the top and bottom devices in each leg was set to 50 ns and 150 ns to accommodate the different switching times seen in the simulation. The experimental waveforms of the gate-to-source and drain-to-source voltage for the phase *a* transistors S_{a1} and S_{a2} are presented in Fig. 4.20 (a) when operating at 270.9 V to 27.5 V, 200 kHz and

1.2 kW. The ripple current of the output inductors and the gate signal of the phase *b* bottom device S_{b2} are shown in Fig. 4.20 (b).



(a)

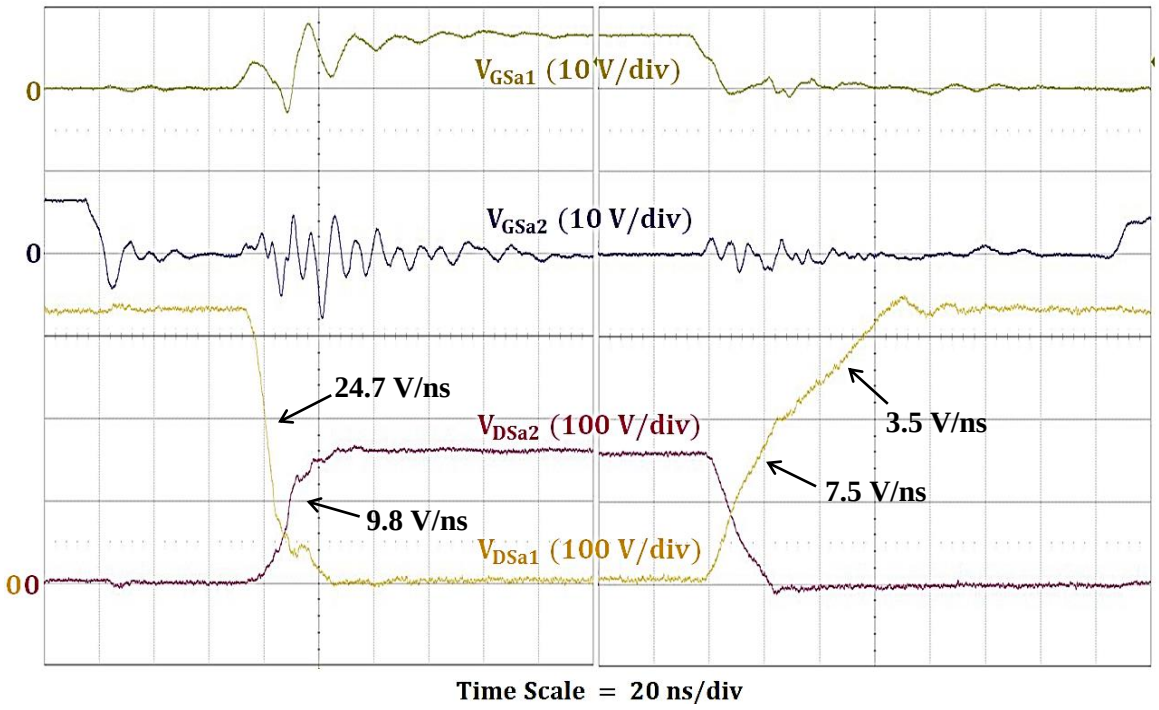


(b)

Fig. 4.20. Experimental waveforms of (a) gate and drain-to-source voltage for S_{a1} and S_{a2} and (b) ripple current of output inductors for operation at V_{in} = 270.9, V_o = 27.5 V, f = 200 kHz, i_{out} = 41.4 A, P_{in} = 1.22 kW and D = 0.17

It can be seen from Fig. 4.20 (a) that the transistor voltage waveforms are clean and consistent with the theoretical waveforms. The highest off-state voltage of S_{a1} and S_{a2} were measured to be 328.2 V and 159.6 V, which are very close to the theoretical predictions of 323.5 V and 161.8 V. The reduction in V_{DSa1} in the middle of the off-state time is due to

the operation of the other phase, which also causes ringing in the gate voltages due to the Miller effect. It can be seen from Fig. 4.20 (b) that the output inductor currents i_{La} and i_{Lb} have an interleaved pattern, meaning the output capacitor current ripple frequency has been doubled. The output inductor current ripple was measured to be 3.5 A which matches the theoretical calculation. Transients are seen in the inductor current waveforms at the switching point due to the charging/discharging of the inductor parasitic capacitance, however the subsequent high frequency oscillation was attributed at least in part to the Rogowski coil used for current measurement.



(a) (b)

Fig. 4.21. Experimental waveforms during switching transients for operation at V_{in} = 270.9, V_o = 27.5 V, f = 200 kHz, i_{out} = 41.4 A, P_{in} = 1.22 kW and D = 0.17 (a) S_{a1} turn-on; (b) S_{a1} turn-off

Fig. 4.21 shows the expanded experimental waveforms during the leg *a* switching transients. The dv/dt of V_{DSa1} during the turn-on and turn-off transients was measured to be 24.7 V/ns and 7.5 V/ns (3.5 V/ns during the second charging phase). The dv/dt levels during turn off were close to the theoretical calculations of 9.4 V/ns and 2.9 V/ns that are obtained using $i_{La}/2C_{oss\_Sa1}$ assuming $C_{oss\_Sa1}=C_{oss\_Sa2}$ for the first charging phase and $i_{Lin}/(C_{oss\_Sa1}+ C_{oss\_Sb1}+ C_{oss\_D})$ for the second charging phase. The switching speed was

limited to a certain extent since the gate driver was supplying two parallel-connected transistors. The dv/dt was also limited by the charge/discharge of the associated parasitic capacitances in the circuit. Oscillations in the gate voltage of the transistors can be observed during the turn-on transient due to the high di/dt and dv/dt, resulting in a swing of -3.3 V to +7.9 V in V_{GSa1}. However, the measurement values were thought to be exaggerated due to the probe lead inductance. The gate ringing is significantly reduced during the turn-off transient due to the lower dv/dt. The oscillations in the drain-to-source voltage are also minimised due to the well-controlled PCB parasitic inductance. The voltage overshoot in V_{DSa1} at turn off is only 5.7%.

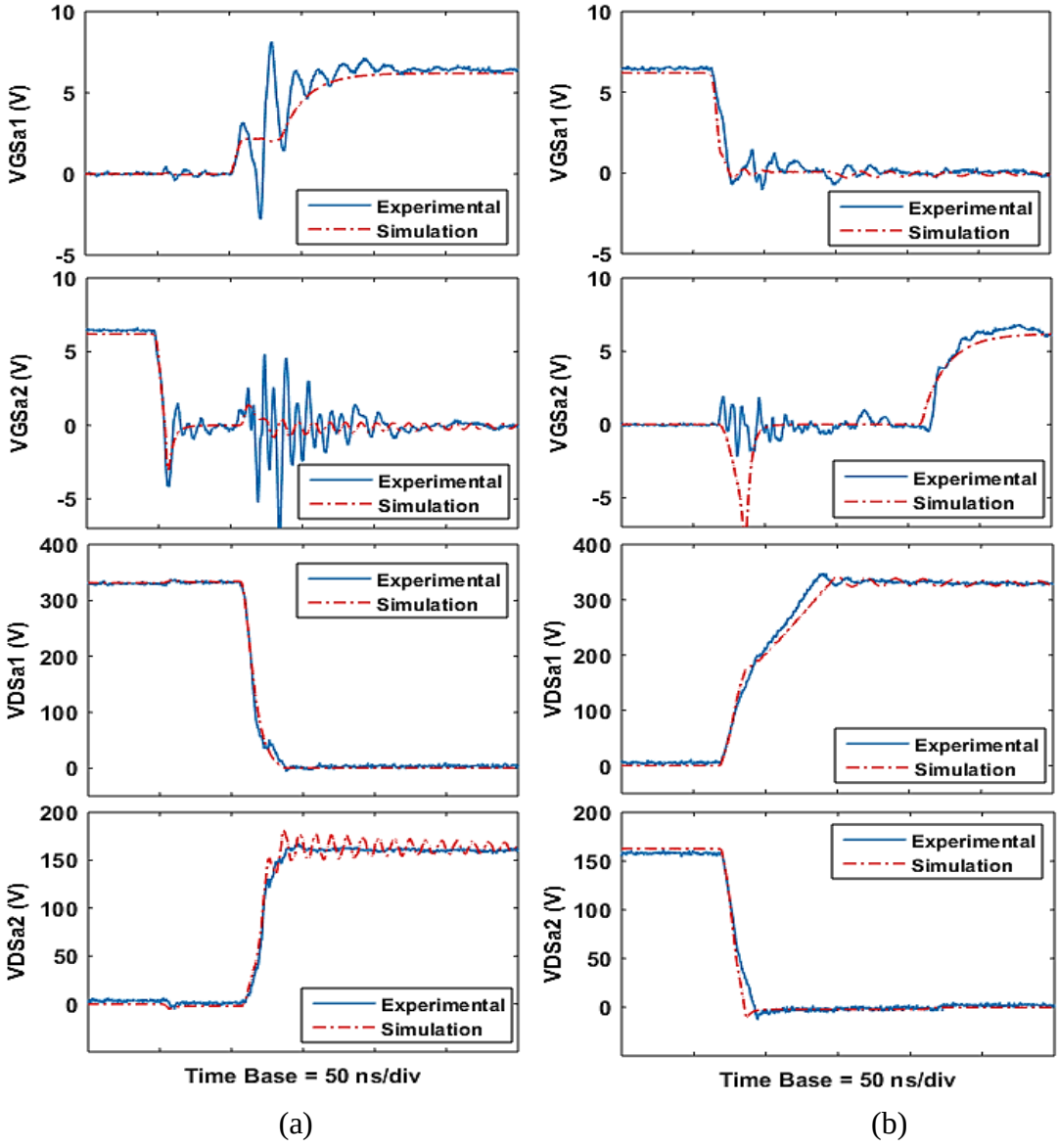
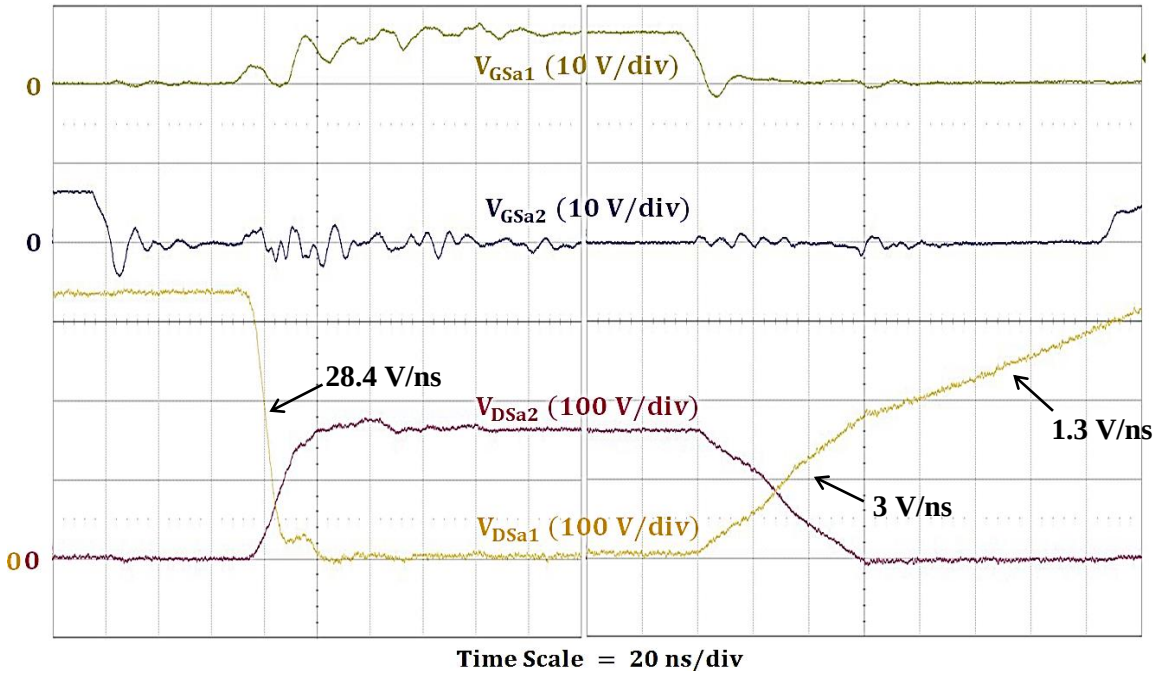


Fig. 4.22. Comparison of experimental and simulation waveforms during (a) S_{a1} turn-on and (b) S_{a1} turn-off transients for operating at 270-28 V, 200 kHz, 1.2 kW

Fig. 4.22 shows the comparison of the experimental waveforms during the switching transients with the simulation waveforms shown in Fig. 4.18 and Fig. 4.19. It can be seen that the experimental waveforms show a close match with the simulation results, confirming that the practical circuit operates as expected and the simulation model is accurate and reliable. More severe oscillations are shown in the experimental gate voltage waveforms compared to the simulation due to the additional parasitic inductance in the PCB and the test probe leads. The dv/dt of the transistor voltage in the simulation and experiment during the turn-on transients presents an excellent match, whilst a slight discrepancy can be seen during the second charging phase at turn off, which is likely to be due to the non-linear device output capacitance at lower voltage and errors in measuring the PCB parasitic capacitances.



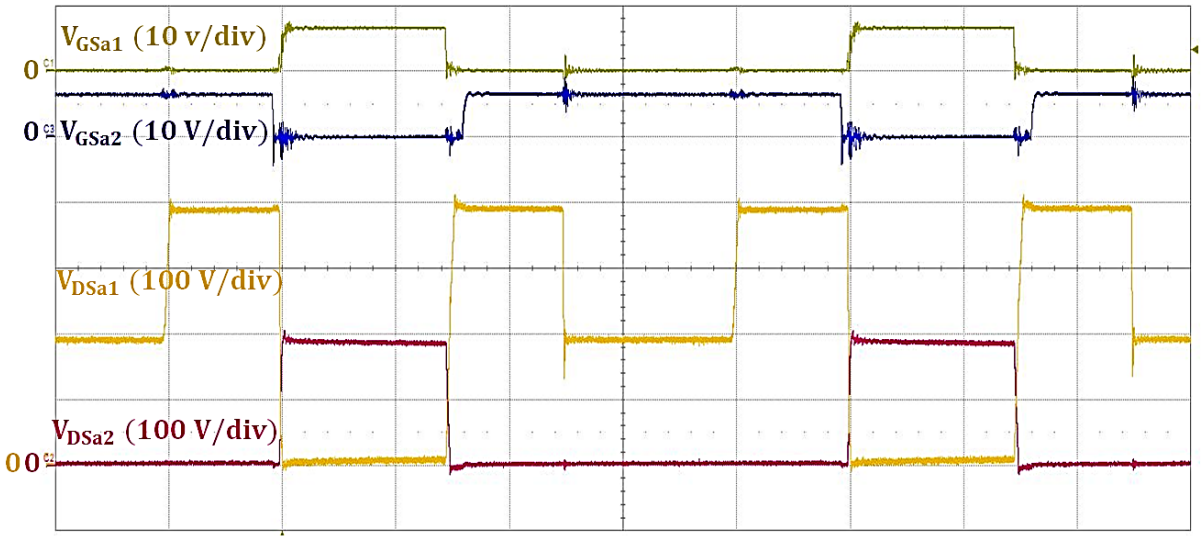
(a) (b)

Fig. 4.23. Experimental waveforms during switching transients for operation at V_{in} = 270.9, V_o = 28.5 V, f = 200 kHz, i_{out} = 11.7 A, P_{in} = 380 W and D = 0.17 (a) S_{a1} turn-on; (b) S_{a1} turn-off

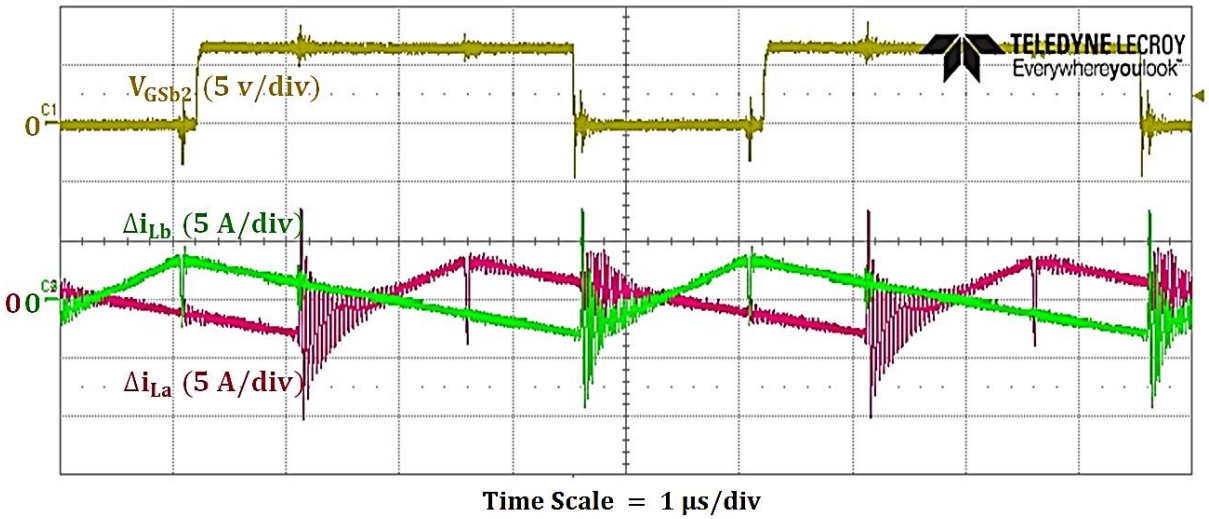
Fig. 4.23 shows the experimental waveforms during the switching transients for the converter operating at 380 W to demonstrate the circuit performance at reduced load conditions. It can be seen that the dv/dt of 28.4 V/ns during the turn on of S_{a1} is similar to the value at the rated load condition, since the device turn-on speed is not load current dependent. However, the turn-off transition is much slower with a dv/dt of 3 V/ns and

1.3 V/ns due to the smaller current available to charge the parasitic capacitance at reduced load conditions.

The prototype was then tested for a voltage conversion ratio of 270 V to 56 V by setting the duty ratio to 0.29. The experimental results are shown in Fig. 4.24 for the converter operating at 270.9 V to 56.3 V, 200 kHz and 1.2 kW. The expanded waveforms during the switching transients of S_{a1} are shown in Fig. 4.25.



(a)



(b)

Fig. 4.24. Experimental waveforms of (a) gate and drain-to-source voltage for S_{a1} and S_{a2} and (b) ripple current of output inductors for operation at V_{in} = 270.9, V_o = 56.3 V, f = 200 kHz, i_{out} = 20.5 A, P_{in} = 1.22 kW and D = 0.29

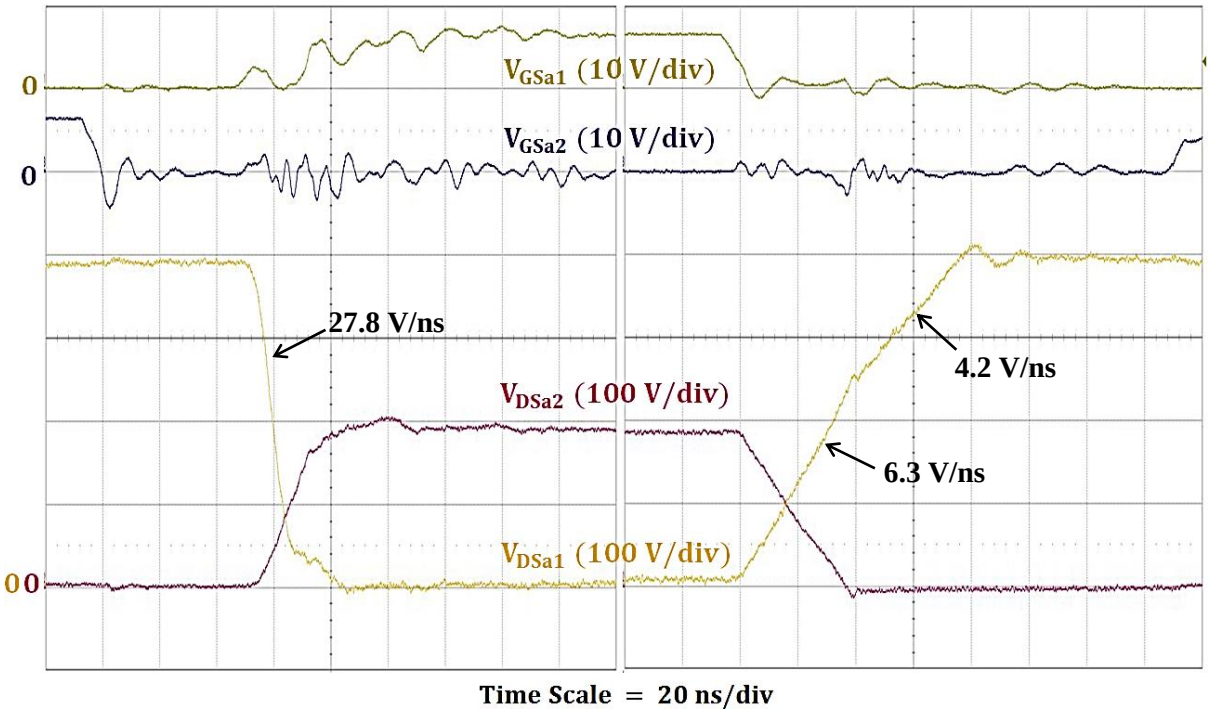


Fig. 4.25. Expanded experimental waveforms during S_{a1} switching transients for operation at V_{in} = 270.9 V, V_o = 56.3 V, f = 200 kHz, i_{out} = 20.5 A, P_{in} = 1.22 kW and D = 0.29

It can be seen from Fig. 4.24 that as the duty ratio is increased, the highest off-stage voltage across S_{a1} and S_{a2} becomes 389.6 V and 191.6 V respectively due to the increase in the switched capacitor voltage V_C. Also the output inductor current ripples have increased to 6.1 A. The dv/dt during turn-on and turn-off is similar to that for operation at 1.2 kW with a duty ratio of 0.17.

As the charging/discharging paths of the switched capacitors are not identical due to the different stray inductance and track resistance, voltage imbalance may occur between C_a and C_b. In order to examine the balance between the two switched capacitors, the voltages of C_a and C_b were recorded for operation over the load range of 300~1.2 kW, 200 kHz, D=0.17, as shown in Fig. 4.26. It can be seen that the difference between the switched capacitor voltages is within $\pm$3 V over the whole load range, which is attributed to the compact layout and the small PCB parasitic inductance. In addition, the circuit itself has some correction capabilities since the switched capacitor with higher voltage tends to release more charge than the other in each cycle, and the charges in the two switched capacitors thereby tend to equalise.

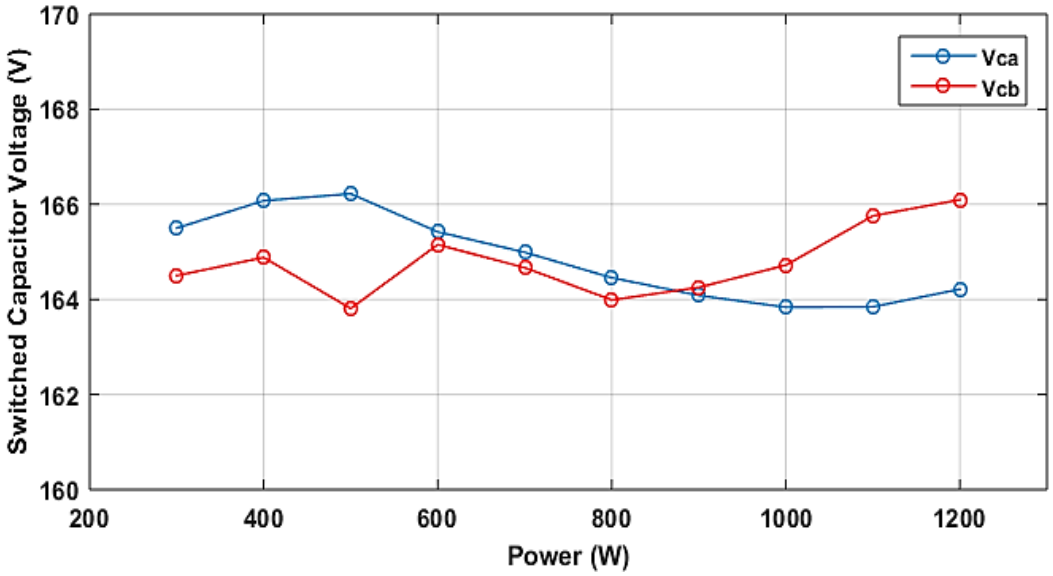


Fig. 4.26. Voltages of switched capacitor C_a and C_b against load power for operation at V_{in}=270 V, D=0.17

4.11 Converter loss breakdown

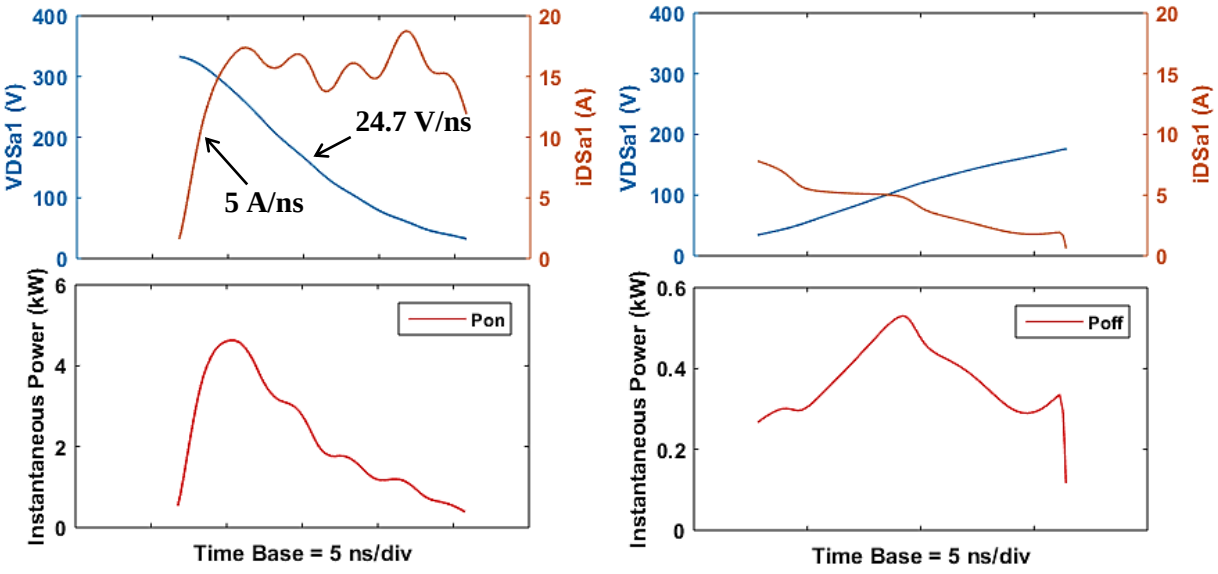
The loss breakdown of the converter when operating at 1.2 kW with a duty ratio of 0.17 was calculated based on the simulation waveforms, shown in Table 4.8. The drain current including the device channel current and output capacitor current was used for device loss calculation, which however will not cause a significant error since the capacitive current is quite small and only occurs during the switching transients. The steady-state transistor junction temperatures obtained from the thermal simulation were used. The losses in the capacitors were neglected due to the very small ESR of the ceramic capacitors.

The switching losses in the top device were estimated based on the simulation results shown in Fig. 4.27 using equation (4-25). The bottom device switches on and off in a ZVS manner and is assumed to have no switching losses.

$$P_{sw} = \int_0^{T_{sw}} V_{ds}(t)\, i_{ds}(t) dt \cdot f \qquad (4\text{-}25)$$

where T_{sw} is the switching time.

The stored energy in the S_{a1} output capacitor is released through the channel during the turn-on transient and cannot be observed in i_{DSa1}. However, this amount of energy is taken into account in the device turn-off loss when the S_{a1} output capacitor is charged.



(a) (b)

Fig. 4.27. Top device S_{a1} instantaneous power losses during (a) turn-on and (b) turn-off transients for operation at V_{in} = 270 V, V_o = 27.9 V, f = 200 kHz, i_{out} = 43 A , P_{in} = 1.24 kW and D = 0.17

The conduction and reverse conduction losses in the transistors were estimated based on (4-26) and (4-27).

$$P_{con} = {i_{ds-rms}}^2 (R_{ds(on)@TJ} + R_{ds(on)@25℃} K_{dy}) \tag{4-26}$$

where T_J is the device junction temperature; K_{dy} is the coefficient of the dynamic on-state resistance increase based on the measurement results in Fig. 3.22 and Fig. 3.23, Chapter 3.

$$P_{con-rev} = \int_0^{T_{sw-rev}} V_f(t)\, i_{ds}(t) dt \cdot f \tag{4-27}$$

where $T_{sw\text{-}rev}$ is the reverse conduction time and V_f is the voltage drop across the transistor

The diode conduction loss was estimated based on (4-28).

$$P_{con-D} = \int_0^{T_{con-D}} V_f(t)\, i_d(t) dt \cdot f \tag{4-28}$$

where $T_{con\text{-}D}$ is the diode conduction time and V_f is the forward voltage drop of the diode.

The copper loss in the inductors was estimated using the measured DC and AC resistance, given by (4-29). The core loss was obtained from the inductor loss calculation tool provided by the manufacturers.

$$P_{copper-L} = {i_{L-rms}}^2 R_{dc} + \Delta {i_{L-rms}}^2 R_{ac} \quad (4\text{-}29)$$

Table 4.8 Converter loss breakdown at 270-28 V, 200 kHz, 1.2 kW

Loss factors		Components parameters	Loss (W)	Percentage contribution
Main circuit				
Main transistor S_{a1} & S_{a2}	Switching	E_{on}=41.6 μJ; E_{off} = 5 μJ	39.2	43.8%
	Conduction	$R_{ds(on)}$ = 40 mΩ @ 71℃ =30 mΩ @ 44℃; $K_{dy\text{-}Sa1}$=1.35; $K_{dy\text{-}Sa2}$=1.16	18.4	20.6%
	Reverse conduction	V_F=1.3 V	2.0	2.2%
Switched diodes D_a and D_b		V_f = 1.2 V @ i_d = 4 A	7.1	7.9%
Switched diode D_0		V_f = 1.1 V @ i_d = 5 A	3.6	4.0%
Input inductor L_{in}	Copper	R_{DC} = 29.8 mΩ; $i_{Lin\text{-}rms}$ = 5.2 A R_{AC} = 1.8 Ω; $\Delta i_{Lin\text{-}rms}$ = 0.4 A	1.1	1.2%
	Core	volt-sec = 1.2 T·cm^2	4.8	5.4%
Output inductor L_a & L_b	Copper	R_{DC} = 2.8 mΩ; $i_{La\text{-}rms}$ = 21.7 A R_{AC} = 0.9 Ω; $\Delta i_{La\text{-}rms}$ = 1 A	4.4	4.9%
	Core	volt-sec = 1.1 T·cm^2	5.8	6.5%
PCB tracks			2.9	3.2%
Total Loss (W)			89.4 W	
Efficiency			92.6%	

It can be concluded from Table 4.8 that the transistor switching loss is dominant and contributes 43.8% to the total loss, followed by the transistor conduction losses that account for 20.6%. A soft-switching approach is thereby likely to be beneficial in reducing the losses, increasing the converter efficiency and boosting the circuit performance.

4.12 Converter efficiency

The converter efficiency was measured when the converter was operating with an input voltage of 270 V, a switching frequency of 200 kHz, and a duty ratio of 0.17 and 0.29 over the load range of 300~1.2 kW, shown in Fig. 4.28. A peak efficiency of 92.6% was recorded, representing a total loss of 88.8 W which shows a very good correspondence with the estimated loss of 89.4 W in Table 4.8. It can be seen that the converter efficiency

with D=0.29 is higher than with D=0.17 when operating above 700 W, which is mainly attributed to the reduced conduction losses with lower load current but higher output voltage. A peak efficiency of 94.2% is achieved at 1.2 kW.

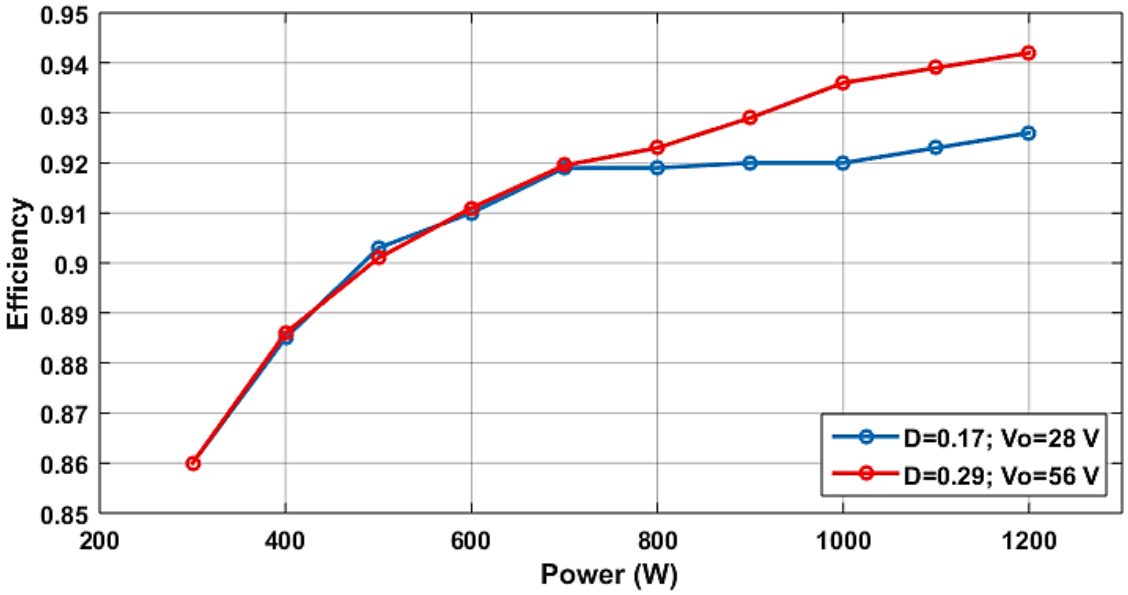


Fig. 4.28. Experimental measurement of converter efficiency for operation at V_{in}=270 V, P_o=300~1.2 kW, f=200 kHz and D=0.17 and 0.29

4.13 Comparison with Si-based circuit

To demonstrate the impact of WBG devices, an equivalent Si-based circuit was designed by replacing the SiC diodes and GaN HEMTs with similarly rated Si devices. VISHAY ultrafast recovery diodes, VS-HFA16TA60 600 V/16 A, were used to replace the SiC diodes and Si MOSFETs, STB45N60 600 V/34 A, from STMicroelectronics were used to replace the GaN HEMTs. The diodes and MOSFETs were in surface-mount D2PAK packages.

The Si-based converter losses for operation at 270-28 V, 200 kHz, 1.2 kW were calculated by means of LTSpice simulation and compared with the original converter loss breakdown shown in Table 4.8. The results are summarised in Table 4.9.

As all the stored parasitic capacitance charge is dissipated and creates energy loss in the top devices at turn on, the switching loss of the top Si MOSFETs can be estimated by (4-25). The turn-off loss was neglected due to the effect of the parasitic capacitance limiting

the dv/dt. The parasitic capacitance of the PCB is assumed to be equal to the WBG-based circuit.

$$P_{sw} = (Q_{oss\_MOSFET} + Q_{rr\_MOSFET} + Q_{rr\_Diode} + Q_{PCB})\frac{V_{ds}}{2} \cdot f \qquad (4\text{-}30)$$

where Q_{oss} and Q_{rr} are the output and reverse recovery charges of the MOSFET and diode, Q_{PCB} is the parasitic charge of the PCB

The conduction loss was estimated assuming a device junction temperature of 25℃.

Table 4.9 WBG-based and Si-based converter losses at 270-28 V, 200 kHz, 1.2 kW

Loss factors		Si-based Converter Loss (W)	WBG-based Converter Loss (W)
Main transistor S_{a1} & S_{a2}	Switching	85.3	39.2
	Conduction	42.8	20.4
Switched diodes D_a, D_b and D_0		13	10.7
Inductor L_{in}, L_a and L_b		16.1	16.1
PCB tracks		2.9	2.9
Total Loss (W)		160.3	89.4
Efficiency		86.6%	92.6%

It can be seen from Table 4.9 that the Si-based converter shows a much lower efficiency of 86.6% compared to the WBG-based converter, representing an increase of 70.9 W in the total loss. The transistor conduction and switching losses are both approximately doubled.

In order to increase the efficiency of the Si-based converter to above 90%, a switching frequency of 100 kHz or lower would be required. The magnetic components size would therefore increase by at least twice if the same inductor current ripple is maintained. An off-the-shelf part, IHV-60-24, 60 μH/24 A, could be selected as the output filter inductor. The footprint comparison of the candidate inductor (right) and the original output inductor, AGP4233, 33 μH/22.5 A, from Coilcraft (left) is shown in Fig. 4.29. The weight comparison of the two inductors is shown in Table 4.10.

Table 4.10 Output inductors weight for the WBG-based and Si-based converters

Inductor part no.	Weight (g)
AGP4233 33 μH/22.5 A × 2	270
IHV-60-24 60 μH/24 A × 2	540

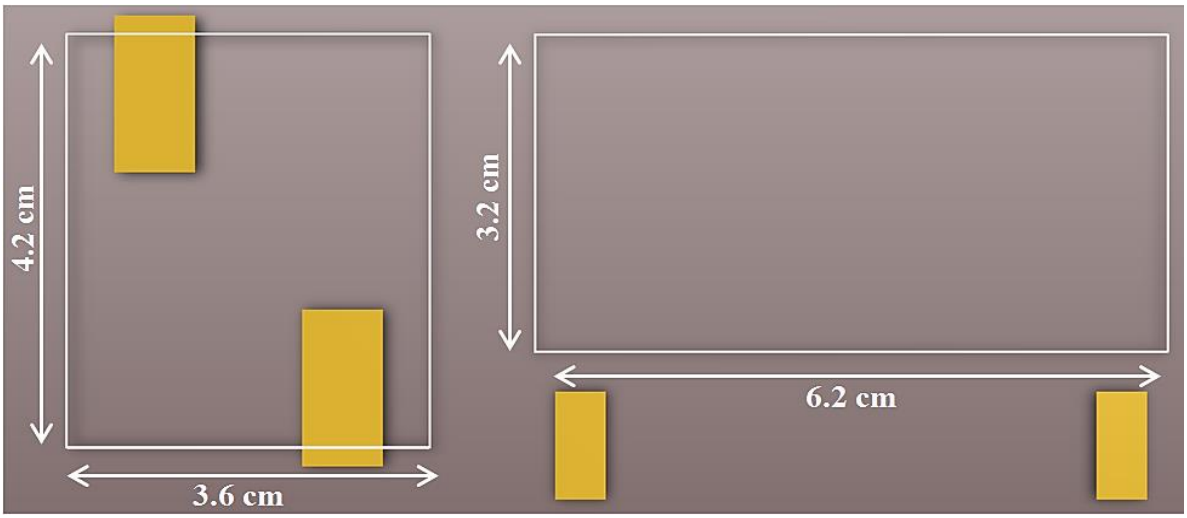


Fig. 4.29. Footprint comparison of output inductors for AGP4233 used in the original converter (left) and IHV-60-24 used in Si-based converter (right)

It can be seen that the Si-based solution with the selected output inductor is likely to increase the converter width to 13 cm or more, resulting in an increase of 30% in the total volume, and an increase in the converter weight by 270 g.

4.14 Summary

A hard-switching, interleaved, switched-capacitor, step-down converter topology was analysed and demonstrated in this Chapter. The interleaved operation doubled the current ripple frequency at the input and output, enabling reductions in the input filter inductor and the input and output capacitor sizes. Furthermore, the parallel channels allow higher load current to be delivered more easily. The circuit performance has been analysed in detail covering the idealised operation and the impact of parasitic device capacitance. The addition of an interleaved phase is seen to limit the transistor duty ratio to below 0.5, and compared with the single-phase switched capacitor buck converter, the conversion ratio is slightly higher at a specific duty-ratio. The parasitic capacitance in the circuit, which includes the diodes, transistors and input and output inductors must be charged/discharged at the switching instants. Whilst this limits the dv/dt and switching losses at transistor turn off, the top transistor turn-on losses are considerable and can limit the circuit operation at high frequencies. This problem will become more severe if larger area devices are used, which inherently have higher capacitance, for example to reduce conduction losses or to enable operation at higher powers.

The circuit operation and performance were confirmed by simulation and experimental testing of a 270-28 V, 200 kHz and 1.2 kW prototype. The prototype used SiC diodes and top-cooled GaN HEMTs, and required a creative thermal design to ensure effective cooling of the devices whilst maintaining compact electrical connections. An overall size of $20\times10\times4.3$ cm^3 (0.86 Litre) was achieved. The experimental waveforms corresponded closely with the simulation results and theoretical expectations. The two switched capacitor voltages were monitored for operation over the load range of 300 W∼1.2 kW and remained well balanced.

An efficiency of 92.6% was achieved for operation at 270-28 V, 200 kHz and 1.2 kW. The transistor switching loss accounted for 43.8% of the total loss and this was mainly due to the turn-on loss in the top transistors. To illustrate the value of WBG devices in this application, a Si-based circuit using similarly rated devices was evaluated by simulation. Compared with the original WBG-based converter, the efficiency fell from by 92.6% to 86.6% with the same switching frequency of 200 kHz. Alternatively, to maintain the similar efficiency, the switching frequency would need to be reduced to 100 kHz in which case the converter would be 30% larger.

Chapter 5

Operation of the Soft-Switching Switched-Capacitor Step-Down Converter

5.1 Introduction

To reduce the switching losses associated with the significant parasitic capacitances in the interleaved switched-capacitor buck converter, Chapter 4, a soft-switching method is proposed in this chapter. The analysis of the circuit operation is followed by detailed design and validation on a 1.2 kW, 270 V – 28 V converter. Compared with the original hard-switching circuit, the dv/dt is well-controlled and the losses in the transistors are significantly reduced.

5.2 Circuit description

The proposed soft-switching, interleaved, switched-capacitor buck converter is shown in Fig. 5.1. An auxiliary circuitry (marked in red) is introduced which consists of three switching devices S_{auxa}, S_{auxb} and S_{aux0}, a SiC diode D_{aux0} and a resonant inductor L_{aux}.

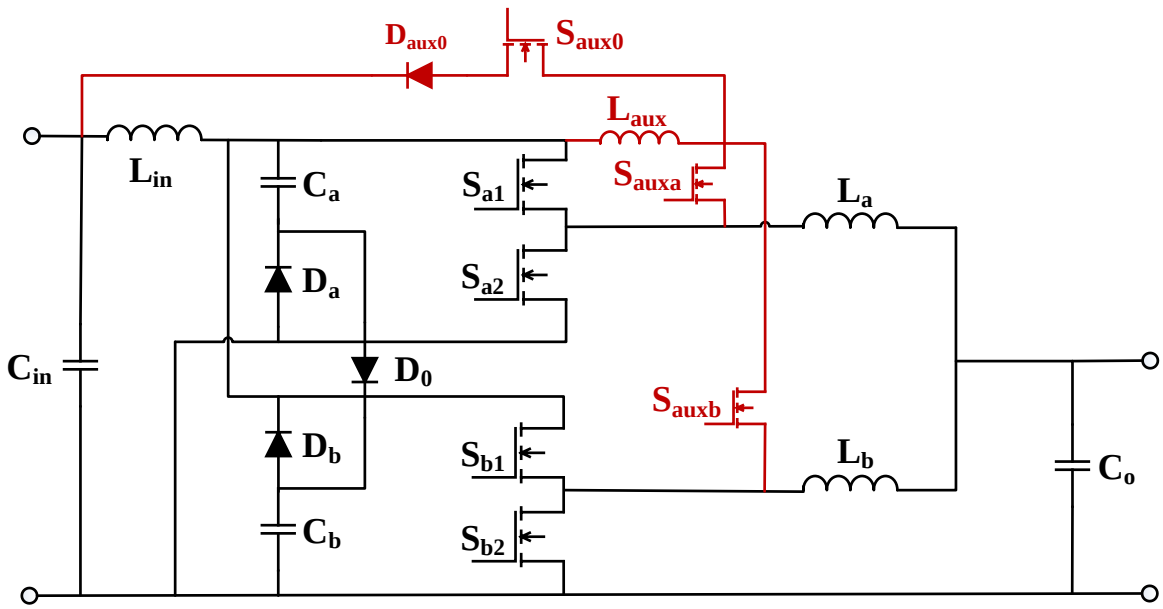


Fig. 5.1. Interleaved soft-switching switched-capacitor step-down converter

The auxiliary branches formed by the inductor L_{aux} and switches S_{auxa} and S_{auxb} are responsible for charging/discharging the output capacitance of the switching legs immediately before the turn on of each upper device, S_{a1} and S_{b1}, thereby allowing zero-voltage turn on of the devices. The branch consisting of the auxiliary switch S_{aux0} and diode D_{aux0} allows the energy in the auxiliary inductor L_{aux} to be returned to the input after zero-voltage turn on of S_{a1} and S_{b1} has taken place.

The auxiliary switches turn on prior to the turn-on of the top devices and the auxiliary inductor is charged. As a result, the freewheeling output filter inductor current commutates from the lower device, S_{a2} or S_{b2}. The auxiliary inductor current continues to rise as L_{aux} interacts resonantly with the leg output capacitance, swinging the leg voltage from zero to $2V_C$, where $V_C=V_{Ca}=V_{Cb}$.

The detailed explanation of circuit operation will be covered in the next sections. During the turn-off of S_{a1} and S_{b1}, the leg output capacitor acts as a snubber capacitor to control the dv/dt and reduce the turn-off losses. Since the auxiliary inductor current rises from zero in each commutation cycle, S_{auxa} and S_{auxb} will turn on under zero-current conditions. However, when they turn off, the auxiliary switches are responsible for diverting current and the devices will incur inductive turn off losses. In addition, a RC snubber is connected in parallel with each auxiliary switch to damp the ringing between the auxiliary inductor and the output capacitor of the auxiliary switches when the DC link voltage is stepping up and down.

5.3 Circuit operation principle at steady-state

The ideal steady-state operating waveforms of the circuit for D<0.5 are shown in Fig. 5.2. V_{GSa1} and V_{GSa2} are the gate-to-source voltages of the top and bottom devices in leg *a*, whilst V_{GSb1} and V_{GSb2} are the gate-to-source voltages of the devices in leg *b*. V_{GSauxa} and V_{GSauxb} are the gate-to-source voltages of the auxiliary switches that are responsible for soft-switching the corresponding main switches. V_{GSaux0} is the gate-to-source voltage of auxiliary switch S_{aux0} for controlling the return path of the auxiliary inductor current. V_{DSa1} and V_{DSauxa} are the drain-to-source voltage of the main switch and the auxiliary switch in leg *a*. V_{Lin} is the voltage of the input inductor L_{in}. V_{Laux} and i_{Laux} are the voltage and current of the auxiliary inductor L_{aux}. i_{La} and i_{Lb} are the output inductor currents. V_{DSauxa} is assumed to have an instantaneous voltage change during the switching transients of S_{auxa}.

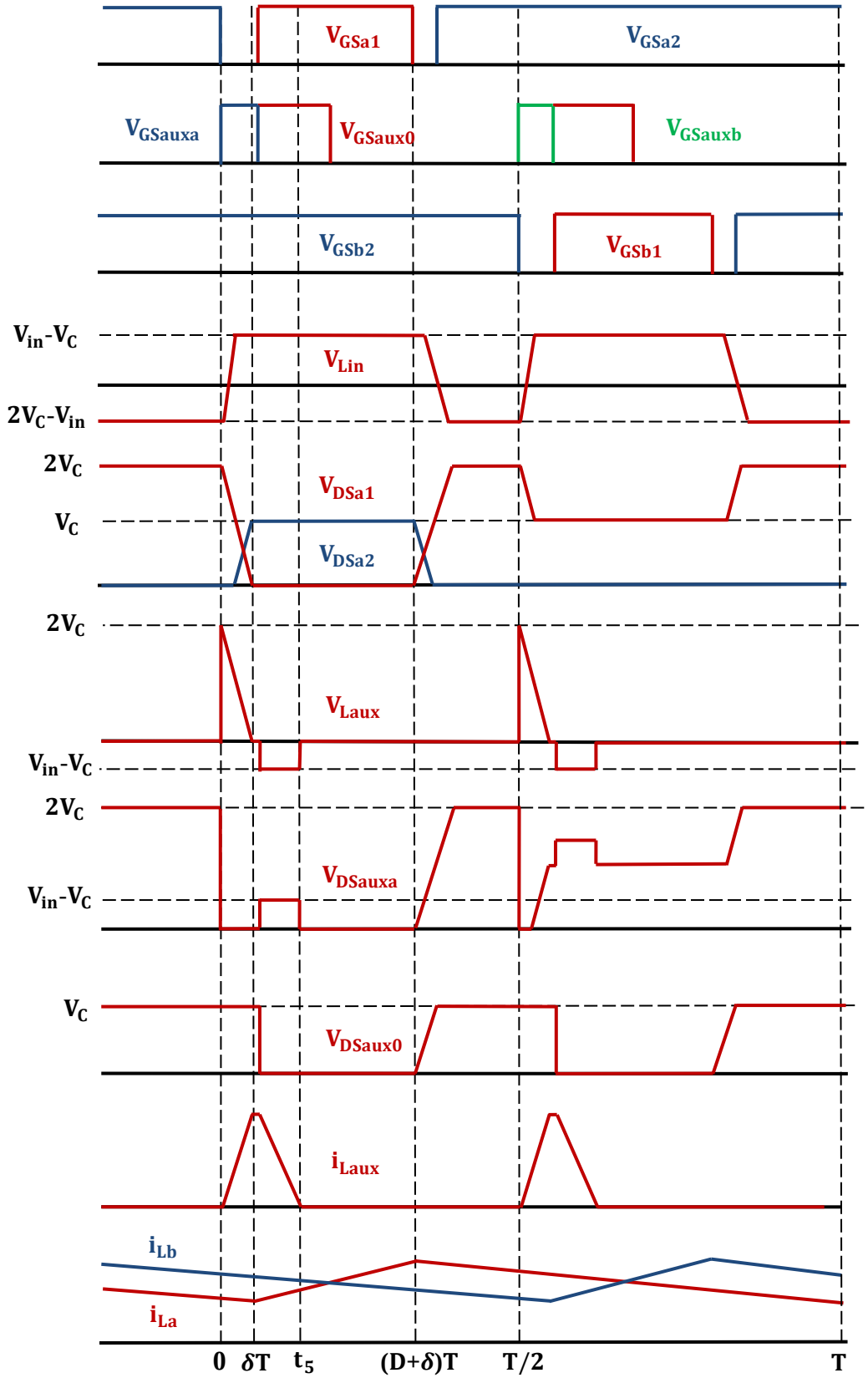


Fig. 5.2. Ideal steady-state waveforms for D<0.5

To realize soft-switching, the auxiliary switch S_{auxa} or S_{auxb} are turned on during the dead time of the top and bottom devices. S_{aux0} is switched on immediately after the auxiliary switch turns off to feed the remaining auxiliary inductor energy back to the input. The main switches S_{b1} and S_{b2} are controlled to be delayed by half the cycle behind leg *a* to ensure the interleaved operation.

Assuming D and δ are the duty ratios of the main and auxiliary switches respectively and neglecting the rise and fall times in the waveforms, the volt-seconds of the input and output inductors can be equated as (5-1) and (5-2).

$$(V_{in} - V_C)(D + \delta)T = (2V_C - V_{in})(0.5 - (D + \delta))T \tag{5-1}$$

$$(V_C - V_o)(D + \delta)T = V_0(1 - (D + \delta))T \tag{5-2}$$

The auxiliary duty ratio δ may be fixed regardless of the voltage conversion ratio, as it is only determined by the time advance of the auxiliary transistors, which is associated with the parasitic capacitance of the components in the circuit. The main duty ratio D can be determined by (5-3), obtained by eliminating V_C between (5-1) and (5-2). The auxiliary duty ratio δ will cause a small variation on the voltage conversion ratio compared with the hard-switching version, and may be compensated by adjusting the main duty ratio D.

$$D = \frac{2(1-\delta)V_o - V_{in}}{2V_o + V_{in}} \tag{5-3}$$

5.4 Circuit analysis during advance time

During the advance time where zero-voltage turn on of the top device S_{a1} in leg *a* occurs, five stages ($0 \sim t_5$) are defined for analysing the circuit behaviour. $0 \sim t_1$ is the linear charge phase of the auxiliary inductor. $t_1 \sim t_4$ is the resonant phase where the auxiliary inductor interacts with parasitic capacitances of the diodes and transistors. $t_4 \sim t_5$ is the discharge phase of the auxiliary inductor where all the energy in the inductor is returned to the input and the auxiliary inductor current is reset.

5.4.1 Circuit operation at nominal load conditions

During $t_1 \sim t_4$, two different resonance patterns can occur depending on the circuit parameters and load conditions. Fig. 5.3 shows the ideal steady-state waveforms during $0 \sim t_5$ for the operation pattern when the converter operates at nominal load conditions.

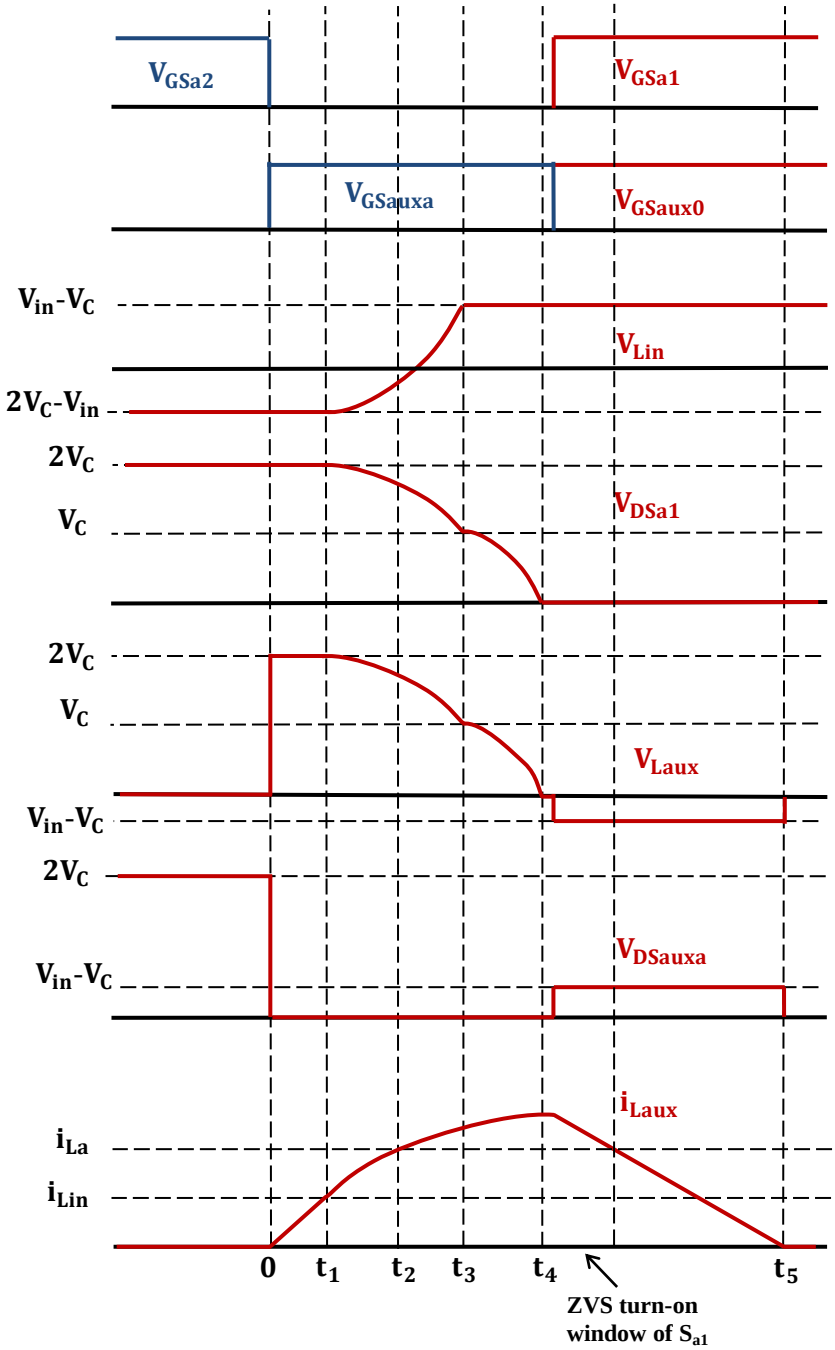


Fig. 5.3. Expanded ideal steady-state waveforms during 0~t_5 for D<0.5 at nominal load conditions

A. Sub-period 0~t_1

Initially the capacitors C_a and C_b are being charged in series by i_{Lin}, whilst the output inductor currents i_{La} and i_{Lb} are freewheeling through S_{a2} and S_{b2}, which are operating as synchronous rectifiers. The bottom device S_{a2} in leg *a* is signalled to turn off at t=0, however the freewheeling current will continue to flow in S_{a2}, but there will be an

increased reverse conduction voltage drop. Also at t=0, the auxiliary transistor S_{auxa} turns on under zero-current switching. The output capacitances of S_{auxa} and S_{auxb} will discharge rapidly into the channel of S_{auxa}. The auxiliary inductor L_{aux} is charged by $V_{Ca}+V_{Cb}=2V_C$. The current i_{sa2} in the bottom device S_{a2} starts to commutate to S_{auxa} and the current in diode D_0 starts to fall. This stage ends when the auxiliary inductor current i_{Laux} reaches i_{Lin}. The circuit operation during this sub-period is shown in Fig. 5.4.

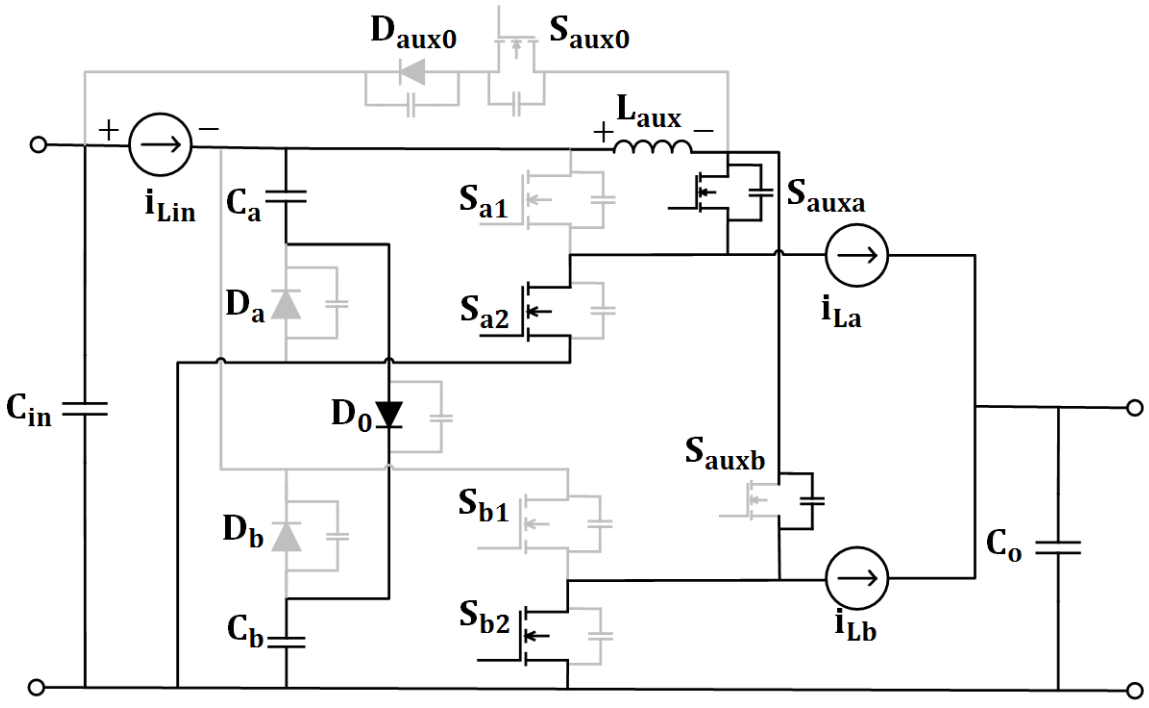


Fig. 5.4. Circuit operation during $0\sim t_1$

Assuming the auxiliary transistor S_{auxa} turns on instantaneously, the duration of this stage T_1 can be determined by (5-4).

$$T_{1=}\frac{i_{Lin}L_{aux}}{2V_C} \tag{5-4}$$

B. Sub-period $t_1\sim t_2$

This stage starts when the auxiliary inductor current i_{Laux} exceeds the input inductor current i_{Lin}, and diode D_0 turns off. As i_{Laux} continues to rise, the output capacitors of D_a and D_b are discharged and D_0 is charged. At the same time the output capacitor of S_{a1} and S_{b1} start to discharge while S_{a2} remains conducting. This stage ends when the auxiliary inductor current i_{Laux} reaches the output inductor current i_{La}. The DC link voltage transition

has not yet finished at the end of this stage, which can be seen in Fig. 5.4. The circuit operation during this sub-period is shown in Fig. 5.5.

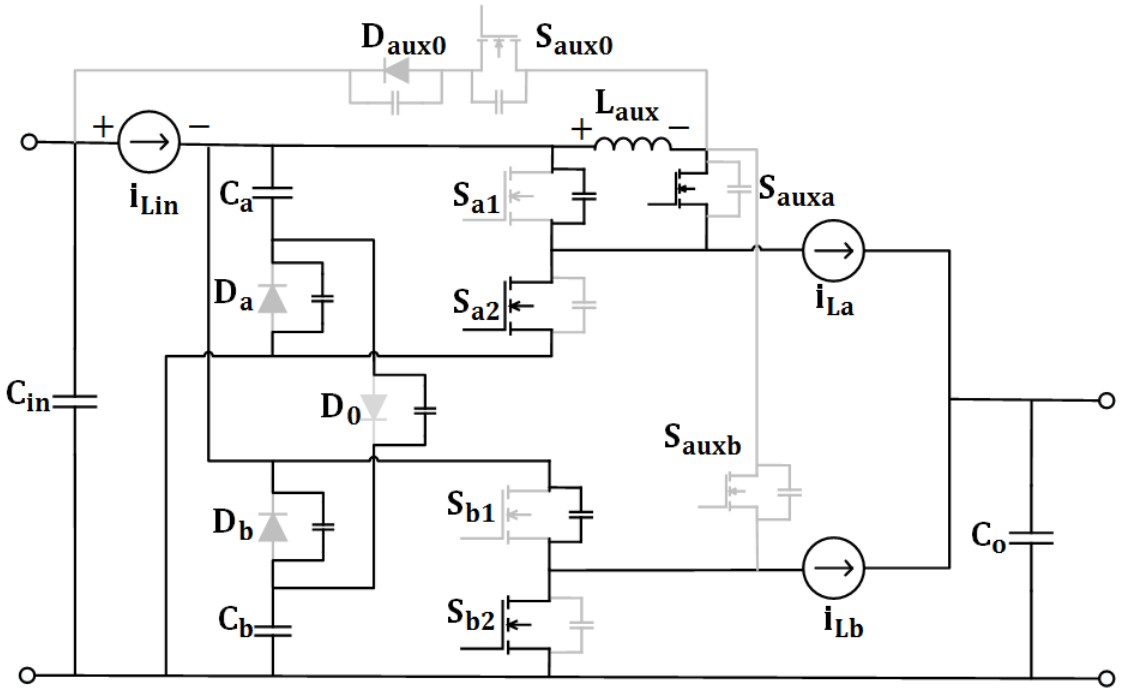


Fig. 5.5. Circuit operation during t_1~t_2

The simplified equivalent circuit including all the resonant components is drawn in Fig. 5.6. As the difference in the auxiliary inductor current i_{Laux} and the input inductor current i_{Lin} provides the charging and discharging current of diodes D_a, D_b, D_0 and the main transistors S_{a1}, S_{b1}, the current relationship in the circuit can be expressed as equation (5-5), where i_{oss} refers to the capacitive charging or discharging current of the device output capacitor. The input inductor L_{in} is considered to be a constant current source i_{Lin} and the switched capacitors C_a and C_b are considered to be constant voltage sources V_C.

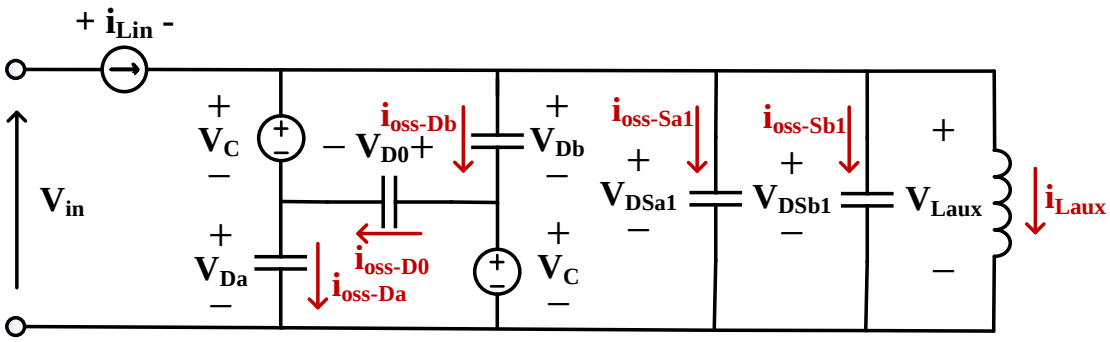


Fig. 5.6. Simplified equivalent circuit during t_1~t_2

$$i_{oss\_Da}(t) + i_{oss\_Db}(t) - i_{oss\_D0}(t) + i_{oss\_Sa1}(t) + i_{oss\_Sb1}(t) + i_{Laux}(t) = i_{Lin} \quad (5\text{-}5)$$

Since the output capacitances of the diodes and main transistors have the same charging/discharging rate, equation (5-6) can be obtained.

$$\frac{dV_{Da}(t)}{dt} = \frac{dV_{Db(t)}}{dt} = -\frac{dV_{D0}(t)}{dt} = \frac{dV_{DSb1}(t)}{dt} = \frac{dV_{DSa1(t)}}{dt} = \frac{dV_{Laux(t)}}{dt} \quad (5\text{-}6)$$

Assuming the front-end diodes, main transistors and auxiliary transistors have linear output capacitances, the device capacitive current and the inductor voltage equations are shown in (5-7).

$$i_{oss}(t) = C_{oss}\frac{dV_{oss}(t)}{dt};\ V_{Laux}(t) = L_{aux}\frac{di_{Laux}(t)}{dt} \quad (5\text{-}7)$$

Substituting (5-6) and (5-7) into (5-5),

$$L_{aux}C_{T2}\frac{d^2 i_{Laux}(t)}{dt^2} + i_{Laux}(t) = i_{Lin} \quad (5\text{-}8)$$

where $C_{T2} = C_{oss\_Da} + C_{oss\_Db} + C_{oss\_D0} + C_{oss\_Sa1} + C_{oss\_Sb1}$

The solution of differential equation (5-8) can be written as

$$i_{Laux}(t) = A\sin[\omega_{T2}(t - t_1)] + B\cos[\omega_{T2}(t - t_1)] + i_{Lin} \quad (5\text{-}9)$$

for $t_1 < t < t_2$, where A and B are constants depending on the initial conditions

Using the initial conditions of this stage

$$i_{Laux}(t_1) = i_{Lin};\ \frac{di_{Laux}(t_1)}{dt} = \frac{2V_C}{L_{aux}} \quad (5\text{-}10)$$

The auxiliary inductor current is given by (5-11),

$$i_{Laux}(t) = \frac{2V_C}{\omega_{T2}L_{aux}}\sin[\omega_{T2}(t - t_1)] + i_{Lin} \quad (5\text{-}11)$$

where $\omega_{T2} = \frac{1}{\sqrt{L_{aux}C_{T2}}}$

and the auxiliary inductor voltage is given by (5-12),

$$V_{Laux}(t) = 2V_C\cos[\omega_{T2}(t - t_1)] \quad (5\text{-}12)$$

Since this stage ends at $i_{Laux}(t_2)=i_{La}$, the duration of this stage T_2 can be determined from (5-11) as shown in (5-13).

$$T_2 = \frac{1}{\omega_{T2}} \sin^{-1}\left[\frac{\omega_{T2} L_{aux}(i_{La}-i_{Lin})}{2V_C}\right] \tag{5-13}$$

The auxiliary inductor voltage at the end of this stage can be determined from (5-12).

$$V_{Laux}(t_2) = 2V_C \cos(\omega_{T2} T_2) \tag{5-14}$$

C. Sub-period t_2~t_3

This period starts when the auxiliary inductor current i_{Laux} reaches the output inductor current i_{La}. At this time, the current commutation between the bottom device S_{a2} and the auxiliary device S_{auxa} is complete. Additional increases in i_{Laux} will flow into the output capacitance of leg *a*, increasing V_{Sa2} and reducing V_{Sa1}. The charging and discharging of the output capacitances of the leg *a* transistors will occur through a resonant interaction with L_{aux}. The difference in i_{Laux} and i_{Lin} continues to charge and discharge the parasitic capacitance of the diodes D_a, D_b and D_0 and transistors S_{a1} and S_{b1} until the DC link voltage is equal to $V_C=V_{Ca}=V_{Cb}$ and diodes D_a, D_b conduct, which marks the end of this stage. The circuit operation during this sub-period is shown in Fig. 5.7.

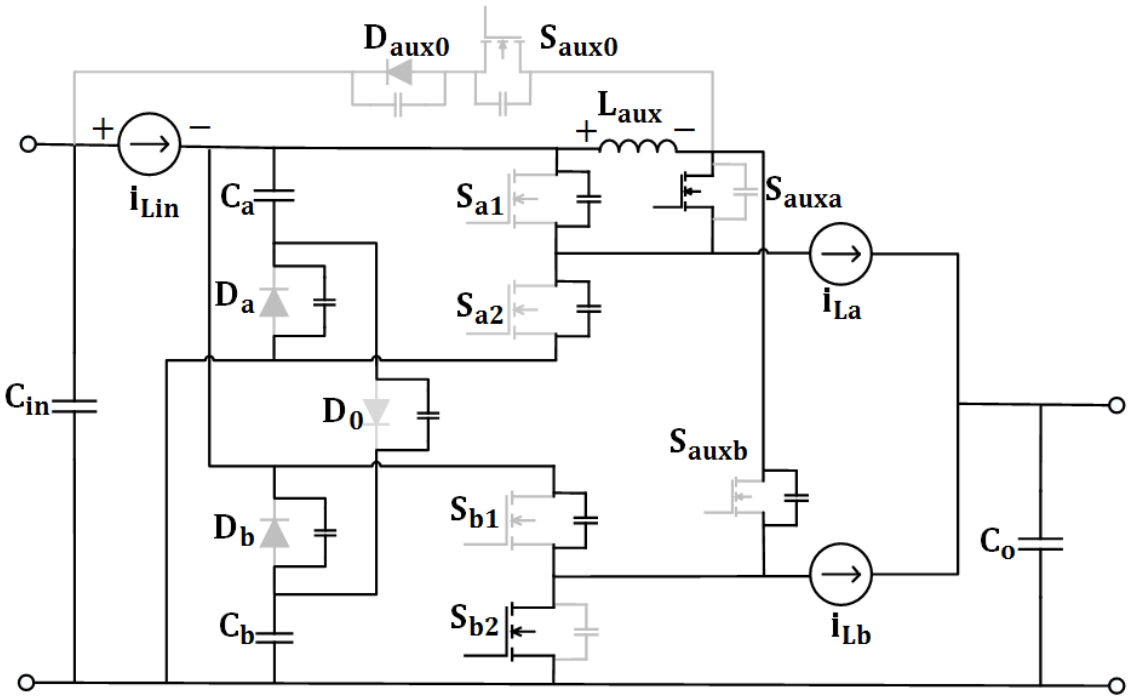


Fig. 5.7. Circuit operation during t_2~t_3

The converter equivalent circuit during this stage is shown in Fig. 5.8.

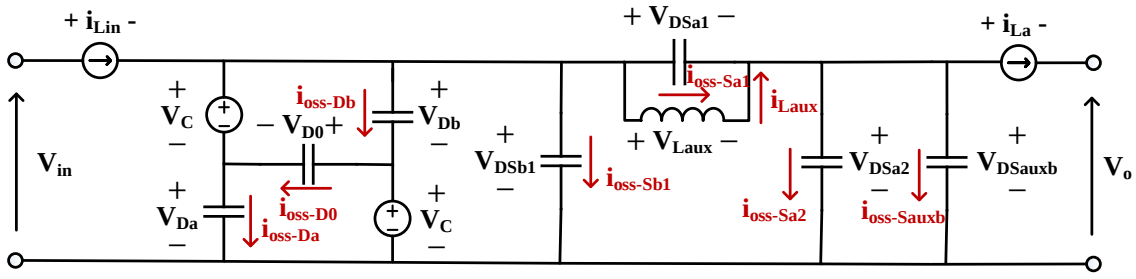


Fig. 5.8. Simplified equivalent circuit during t_2~t_3

(5-15) and (5-16) can be derived from the equivalent circuit using Kirchhoff's current and voltage laws.

$$i_{oss\_Da}(t) + i_{oss\_Db}(t) - i_{oss_{D0}}(t) + i_{oss_{Sa1}}(t) + i_{oss_{Sb1}}(t) + i_{Laux}(t) = i_{Lin};$$

$$i_{oss\_Sa1}(t) + i_{Laux}(t) = i_{oss\_Sa2}(t) + i_{oss\_Sauxb}(t) + i_{La} \tag{5-15}$$

$$\frac{dV_{Da}(t)}{dt} = \frac{dV_{Db(t)}}{dt} = -\frac{dV_{D0}(t)}{dt} = \frac{dV_{DSb1}(t)}{dt} = \frac{d[V_{DSa1(t)}+V_{DSa2(t)}]}{dt};$$

$$\frac{dV_{DSa1(t)}}{dt} = \frac{dV_{Laux(t)}}{dt}; \frac{dV_{DSa2(t)}}{dt} = \frac{dV_{DSaub(t)}}{dt} \tag{5-16}$$

Combining (5-7), (5-15), and (5-16), the circuit characteristic equation during this sub-period can be obtained, shown in (5-17).

$$L_{aux}C_{T3}\frac{d^2 i_{Laux}(t)}{dt^2} + i_{Laux}(t) = \frac{C_{oss\_Sa2}+C_{oss\_Sauxb}}{C_{oss\_D}+C_{oss\_Sa2}+C_{oss\_Sauxb}} i_{Lin} + \frac{C_{oss\_D}}{C_{oss\_D}+C_{oss\_Sa2}+C_{oss\_Sauxb}} i_{La} \tag{5-17}$$

where $C_{T3} = \frac{C_{oss\_D}(C_{oss\_Sa2}+C_{oss\_Sauxb})}{C_{oss\_D}+C_{oss\_Sa2}+C_{oss\_Sauxb}} + C_{oss\_Sa1}$; $C_{oss\_D} = C_{oss\_Da} + C_{oss\_Db} + C_{oss\_D0}$

The initial conditions of the auxiliary inductor current and voltage in this stage are given by (5-18).

$$i_{Laux}(t_2) = i_{La}; \frac{di_{Laux}(t_2)}{dt} = \frac{V_{Laux}(t_2)}{L_{aux}} \tag{5-18}$$

The general expression of the auxiliary inductor current and voltage can be obtained by solving (5-17) using the initial conditions (5-18), shown in (5-19) and (5-20).

$$i_{Laux}(t) = \frac{V_{Laux}(t_2)}{\omega_{T3} L_{aux}} \sin[\omega_{T3}(t - t_2)] + \frac{(C_{oss\_Sa2} + C_{oss\_Sauxb})(i_{La} - i_{Lin})}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} \cos[\omega_{T3}(t - t_2)] + \frac{C_{oss\_Sa2} + C_{oss\_Sauxb}}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} i_{Lin} + \frac{C_{oss\_D}}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} i_{La} \quad (5\text{-}19)$$

$$V_{Laux}(t) = V_{Laux}(t_2) \cos[\omega_{T3}(t - t_2)] - \frac{(C_{oss\_Sa2} + C_{oss\_Sauxb})(i_{La} - i_{Lin})}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} \omega_{T3} L_{aux} \sin[\omega_{T3}(t - t_2)] \quad (5\text{-}20)$$

where $\omega_{T3} = \frac{1}{\sqrt{L_{aux} C_{T3}}}$

This stage ends when diodes D_a and D_b become forward biased and the DC link voltage is clamped to V_C. Therefore, the duration of this sub-period T_3 can be determined by setting $V_{Laux}=V_C$ in (5-20), giving (5-21).

$$T_3 = \frac{1}{\omega_{T3}} [\cos^{-1}(\frac{V_C}{\sqrt{A^2 + B^2}}) - \tan^{-1}(\frac{B}{A})] \quad (5\text{-}21)$$

where $A = V_{Laux}(t_2), B = \frac{(C_{oss\_Sa2} + C_{oss\_Sauxb})(i_{La} - i_{Lin})}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} \omega_{T3} L_{aux}$

The auxiliary inductor current by the end of this stage $i_{Laux}(t_3)$ can be obtained by setting $t - t_2 = T_3$ in (5-19), shown in (5-22).

$$i_{Laux}(t_3) = \frac{V_{Laux}(t_2)}{\omega_{T3} L_{aux}} \sin(\omega_{T3} T_3) + \frac{(C_{oss\_Sa2} + C_{oss\_Sauxb})(i_{La} - i_{Lin})}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} \cos(\omega_{T3} T_3) + \frac{C_{oss\_Sa2} + C_{oss\_Sauxb}}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} i_{Lin} + \frac{C_{oss\_D}}{C_{oss\_D} + C_{oss\_Sa2} + C_{oss\_Sauxb}} i_{La} \quad (5\text{-}22)$$

D. Sub-period t_3~t_4

During this stage, the auxiliary inductor current continues to flow in the leg *a* output capacitance, discharging S_{a1} and charging S_{a2}. The stage ends when $V_{DSa1}=0$ and $V_{DSa2}=V_C$. The excess current in the auxiliary inductor then transfers to the S_{a1} anti-parallel diode, creating a zero-voltage condition for the turn on of S_{a1}. The circuit operation during this sub-period is shown in Fig. 5.9.

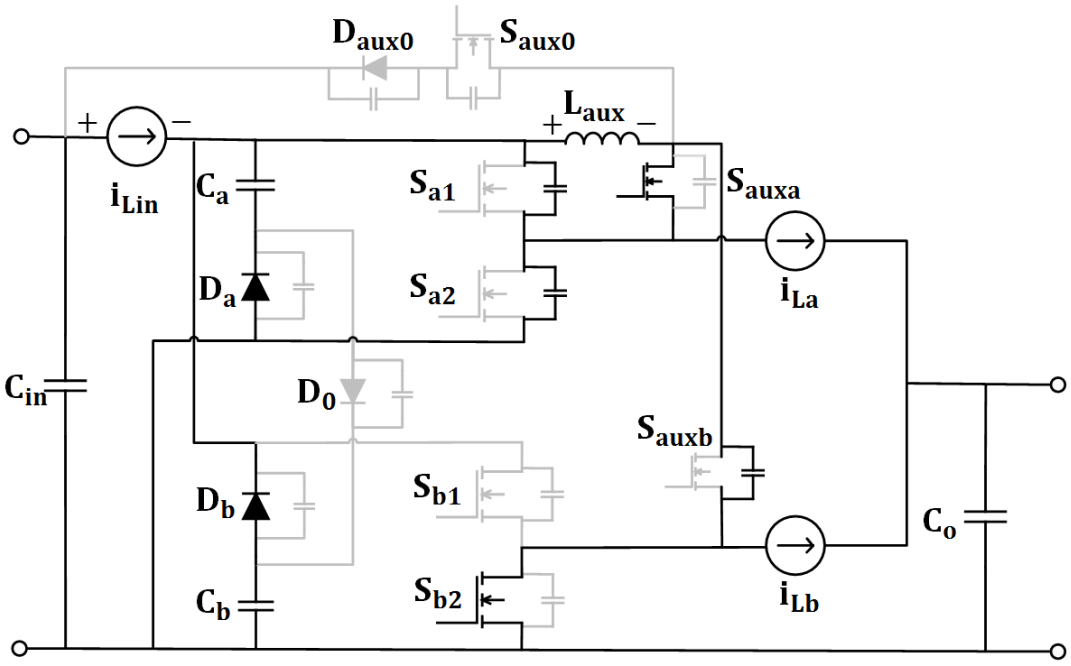


Fig. 5.9. Circuit operation during t_3~t_4

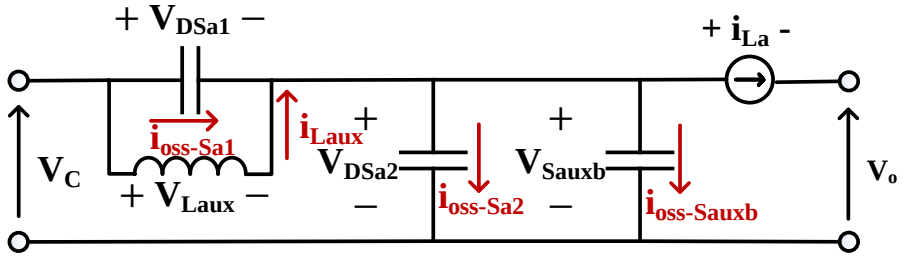


Fig. 5.10. Simplified equivalent circuit during t_3~t_4

The equivalent circuit during this stage is shown in Fig. 5.10. The current and voltage expressions are shown in (5-23) and (5-24).

$$i_{oss\_Sa1}(t) + i_{Laux}(t) = i_{oss\_Sa2}(t) + i_{oss\_Sauxb}(t) + i_{La} \tag{5-23}$$

$$\frac{dV_{DSa1}(t)}{dt} = -\frac{dV_{DSa2}(t)}{dt} = -\frac{dV_{DSauxb}(t)}{dt} = \frac{dV_{Laux}(t)}{dt} \tag{5-24}$$

The auxiliary inductor current differential equation can be obtained by combining (5-23) and (5-24) with the voltage and current equations for the inductor and capacitors, (5-7), shown in (5-25).

$$L_{aux}C_{T4}\frac{d^2 i_{Laux}(t)}{dt^2} + i_{Laux}(t) = i_{La} \tag{5-25}$$

where $C_{T4} = C_{oss\_Sa1} + C_{oss\_Sa2} + C_{oss\_Sauxb}$

The initial condition of the inductor current $i_{Laux}(t_3)$ of this stage is given by (5-22) and the initial auxiliary voltage is $V_{Laux}(t_3)=V_C$.

The auxiliary inductor current and voltage general solutions can be derived by solving the differential equation (5-23) using the initial conditions, giving (5-26).

$$i_{Laux}(t) = \frac{V_C}{\omega_{T4} L_{aux}} \sin \omega_{T4}(t - t_3) + i_{Laux}(t_3)$$

$$V_{Laux}(t) = V_C \cos \omega_{T4}(t - t_3) \tag{5-26}$$

where $\omega_{T4} = \frac{1}{\sqrt{L_{aux} C_{T4}}}$

The final condition of this stage is $V_{Laux}(t_4) = 0$. The duration of this sub-period T_4 is determined by setting $V_{Laux}(t_4) = 0$ in (5-26), giving (5-27).

$$T_4 = \frac{\pi}{2\omega_{T4}} \tag{5-27}$$

The auxiliary inductor current at the end of this stage is given by substituting (5-27) into (5-26), producing (5-28). As the auxiliary inductor current will be discharged when the next stage begins, this is the peak auxiliary inductor current over a period.

$$i_{Laux}(t_4) = \frac{V_C}{\omega_{T4} L_{aux}} + i_{Laux}(t_3) \tag{5-28}$$

E. Sub-period t_4~t_5

Transistor S_{a1} is signalled to conduct after t_4, but whilst its anti-parallel diode is in conduction, that is during the ZVS turn-on window shown in Fig. 5.3. S_{aux0} turns on and S_{auxa} turns off when S_{a1} is signalled to conduct or just after. When S_{auxa} turns off, i_{La} transfers to S_{a1} and turn-off loss will occur in S_{auxa}. The auxiliary inductor L_{aux} is discharged by the impressed voltage V_{in}-V_C and the stored energy is returned to the supply. The output capacitor of S_{auxa} will be discharged through the channel of S_{a1} by means of a resonant interaction with L_{aux} after i_{Laux} falls to zero. The circuit operation during this sub-period is shown in Fig. 5.11.

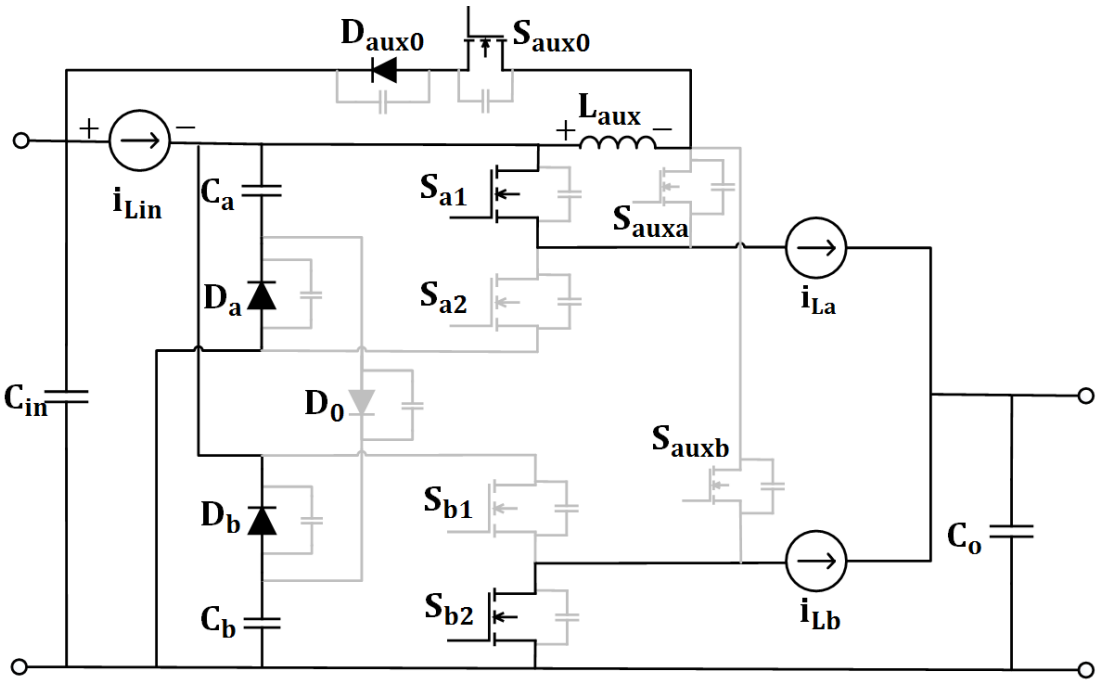


Fig. 5.11. Circuit operation during t_4~t_5

This sub-period ends when the auxiliary inductor current falls to zero. The duration T_5 is given by (5-29).

$$T_5 = \frac{L_{aux} i_{Laux}(t_4)}{V_{in} - V_C} \tag{5-29}$$

The converter then operates for the remainder of the cycle in the same way as the hard-switching circuit. The turn off of top devices S_{a1} and S_{b1} is as analyzed in 4.5.5 and 4.5.6. The leg output capacitance acts as a snubber capacitor and the transistor turn-off losses are well controlled.

5.4.2 Circuit operation at heavy load conditions

Fig. 5.12 shows the ideal steady-state waveforms during $0 \sim t_5$ when the converter is operating under heavier load conditions. This pattern can also occur at rated load conditions but with different auxiliary inductance or circuit parasitic capacitances.

In this operating pattern, the DC link voltage falls more rapidly during the interval $t_1 \sim t_2$ with diodes D_a and D_b becoming forward biased before i_{Laux} is equal to i_{La}. The individual sub-periods are as follows.

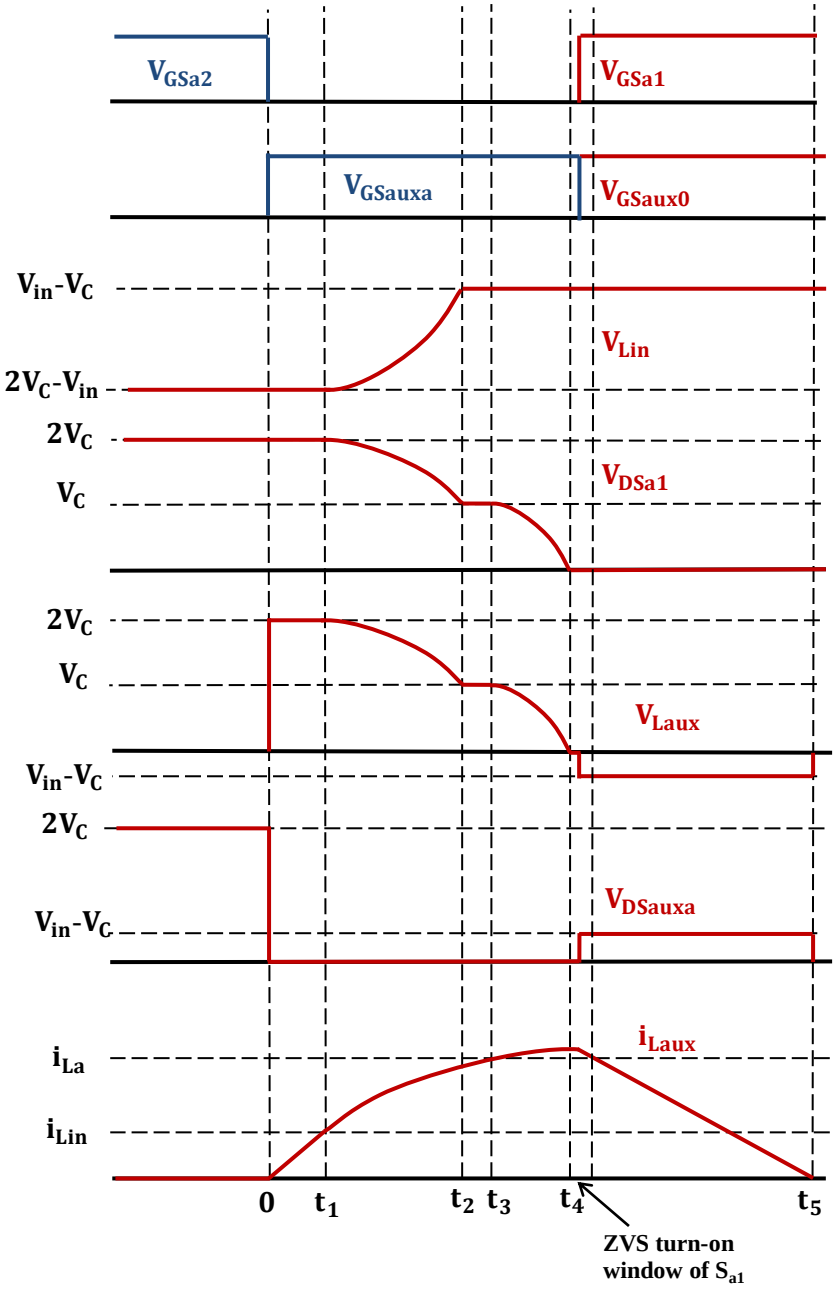


Fig. 5.12. Ideal steady-state waveforms during 0~t_5 for D<0.5 at heavy load conditions

A. Sub-period 0~t_1

The circuit behaviour during this sub-period remains the same as at rated load conditions.

B. Sub-period t_1~t_2

As before, the stage starts when the auxiliary inductor current reaches i_{Lin} but now ends when DC link voltage is equal to V_C. The initial and final conditions are shown in (5-30).

$$i_{Laux}(t_1) = i_{Lin}; \frac{di_{Laux}(t_1)}{dt} = \frac{2V_C}{L_{aux}}$$

$$V_{Laux}(t_2) = V_C \tag{5-30}$$

The general solutions for i_{Laux} and V_{Laux} will be the same as before, equation (5-11) and (5-12). The equation for V_{Laux} is repeated here for convenience.

$$V_{Laux}(t) = 2V_C \cos[\omega_{T2}(t - t_1)] \tag{5-31}$$

where $\omega_{T2} = \frac{1}{\sqrt{L_{aux}C_{T2}}}$ and $C_{T2} = C_{oss\_Da} + C_{oss\_Db} + C_{oss\_D0} + C_{oss\_Sa1} + C_{oss\_Sb1}$

The duration of this sub-period T_2 can be determined by substituting (5-30) into (5-31).

$$T_2 = \frac{1}{\omega_{T2}} \cos^{-1} \frac{V_C}{2V_C} = \frac{1}{\omega_{T2}} \cos^{-1} \frac{1}{2} \tag{5-32}$$

The auxiliary inductor current by the end of this sub-period is given by (5-32).

$$i_{Laux}(t_2) = \frac{2V_C}{\omega_{T2}L_{aux}} \sin \omega_{T2}T_2 + i_{Lin} \tag{5-32}$$

C. Sub-period t_2~t_3

This stage starts when the DC link voltage becomes equal to V_C. The auxiliary inductor is linearly charged by V_C during this stage. Since this sub-period ends when $i_{Laux}(t_3) = i_{La}$, the duration of this sub-period T_3 can be determined by (5-33).

$$T_3 = \frac{L_{aux}[i_{La} - i_{Laux}(t_2)]}{V_C} \tag{5-33}$$

D. Sub-period t_3~t_4

This stage starts with the auxiliary inductor voltage and current being V_C and i_{La} and ends when V_{DSa1} falls to zero. As the equivalent circuit during this stage is the same as in sub-period t_3~t_4 of the nominal load operation shown in Fig. 5.10, the duration of this sub-period T_4 can be determined by substituting the final condition V_{Laux}=0 into the voltage solution (5-26), giving (5-34).

$$T_4 = \frac{\pi}{2\omega_{T4}} \tag{5-34}$$

where $\omega_{T4} = \frac{1}{\sqrt{L_{aux}C_{T4}}}$ and $C_{T4} = C_{oss\_Sa1} + C_{oss\_Sa2} + C_{oss\_Sauxb}$

The peak auxiliary inductor current in this case is given by (5-35).

$$i_{Laux}(t_4) = \frac{V_C}{\omega_{T4}L_{aux}} \sin \omega_{T4}T_4 + i_{La} \tag{5-35}$$

E. Sub-period t_4~t_5

The circuit behaviour during this sub-period remains the same as in the nominal load conditions, where the duration can be determined by equation (5-29).

5.5 Auxiliary circuit design

The auxiliary circuit consists of S_{auxa}, S_{auxb}, S_{aux0}, L_{aux} and D_{aux}. Two additional RC snubbers are connected in parallel with auxiliary transistors S_{auxa} and S_{auxb}, which are omitted in the circuit plots. The main design considerations of the auxiliary circuit are discussed in this section.

5.5.1 Control timings of auxiliary circuit

The on-time of the auxiliary device S_{auxa} ($0 \sim t_4$) needs to be sufficient to ensure the parasitic capacitive charge associated with the turn on of S_{a1} is fully removed, yet needs to be as short as possible to minimise the conduction time and losses in the auxiliary circuit. The top device S_{a1} should be turned on before the turn off of S_{auxa} to ensure the path for the load inductor current, indicating that the leg dead time T_{DT} is shorter than the on-time of S_{auxa}.

Therefore, the conduction time δT of auxiliary transistor S_{auxa} is given by (5-36).

$$\delta T > T_{DT} > T_1 + T_2 + T_3 + T_4 \tag{5-36}$$

The auxiliary transistor S_{aux0} should switch on slightly earlier the turn off of S_{auxa}, and switch off after t_5 when the auxiliary inductor current is zero. However, S_{aux0} must turn off before the main transistor S_{a1} turns off at (D+δ)T to avoid the next DC link voltage transition as seen in Fig. 5.2.

The conduction time δ_2T of auxiliary transistor S_{aux0} is given by (5-37).

$$\frac{L_{aux} i_{Laux}(t_4)}{V_{in}-V_C} < \delta_2 T < DT \tag{5-37}$$

Therefore, in order to reset the current, the size of L_{aux} is subject to (5-38).

$$L_{aux} < \frac{V_{in}-V_C}{i_{Laux}(t_4)} DT \tag{5-38}$$

5.5.2 RC snubbers design

As discussed in 5.4.3, the voltage across auxiliary device S_{auxb} in phase *b* will be increased to V_C+V_{Laux} during t_2~t_4 when the leg *a* output voltage is rising. A similar transient will occur across S_{auxa} during the zero-voltage turn on of S_{b1}. In addition, when the DC link voltage swings from V_C to $2V_C$, the voltage across the auxiliary device S_{auxa} or S_{auxb} will also increase to $2V_C$. During these events, the output capacitor of the auxiliary device is charged rapidly and tends to resonate with the auxiliary inductor L_{aux}. The resulting high-frequency oscillations will introduce unnecessary losses, voltage stress in the auxiliary devices and potential EMI issues. In order to damp the parasitic oscillations, RC snubbers are connected in parallel with auxiliary devices S_{auxa} and S_{auxb}.

The snubber resistance and capacitance was determined using an empirical approach during preliminary design, and further tuned during the tests for achieving a decent balance between the snubber loss and damping effect.

5.6 Converter component selection

The design target of the soft-switching converter is the same as the hard-switching version and is shown in Table 5.1.

Table 5.1 Converter design target

Parameter	Value
Rated power	1.2 kW
Input voltage	270 V
Output voltage	28 V
Switching frequency	200 kHz
Ambient temperature	25 ℃

The circuit parameters and the component selection criteria are listed in Table 5.2 for operation at a nominal power of 1.2 kW. The impact of the auxiliary branch on the passive

components size for the main circuit is very small, therefore the same design can be used for these components as in the hard-switching converter, Chapter 4.

Table 5.2 Circuit key parameters and design criteria

Parameter	Value	Design Criteria
Main circuit		
Main transistor duty ratio D	0.162	$D = \frac{2(1-\delta)V_o - \delta V_{in}}{2V_o + V_{in}}$
Input capacitor C_{in}	4 µF	$\Delta V_{Cin}/V_{in} \leq 1\%$; $C_{in} = \frac{\Delta i_{Lin}}{16 f \Delta V_{Cin}}$
Input current i_{Lin_avg}	4.4 A	$i_{Lin\_avg} = \frac{P_{in}}{V_{in}}$
Input inductor L_{in}	75 µH	$\Delta i_{Lin}/i_{Lin-avg} \leq 30\%$; $L_{in} = \frac{(V_{in}-V_C)DT}{\Delta i_{Lin}}$
Switched capacitors C_a, C_b	8.8 µF	$\Delta V_{Co}/V_{Co} \leq 1\%$; $C_a = C_b = \frac{(1-2D)i_{Lin\_avg}}{2f\Delta V_{Co}}$
Output inductor current i_{Lo_avg}	20.4 A	Assuming $\eta = 95\%$; $i_{Lo\_avg} = \frac{P_{in}\eta}{2V_o}$
Output inductors L_a, L_b	33 µH	$\Delta i_{Lo}/i_{Lo-avg} \leq 20\%$; $L_o = \frac{V_0(1-D)T}{\Delta i_{Lo}}$
Output capacitor C_o	6.6 µF	$\Delta V_{Co}/V_o \leq 1\%$; $C_o = \frac{(1-2D)\Delta i_{Lo}}{8(1-D)f\Delta V_{Co}}$
Auxiliary circuit		
Auxiliary transistor $S_{auxa\&b}$ duty ratio δ	0.01	$T_1 + T_2 + T_3 \leq \delta T \leq T_{DT}$
Auxiliary transistor S_{aux0} duty ratio δ_2	0.05	$T_4 \leq \delta_2 T \leq DT$
Auxiliary inductor L_{aux}	0.17 µH	Optimised based on (1) ω_{T1}, ω_{T2} and ω_{T3} to ensure all the resonant stages finish within δT; (2) Z_{T1}, Z_{T2} and Z_{T3} to ensure the resonant current reaches the expected level*
Snubber capacitor C_s	0.01 nF	To ensure the snubber resistor losses are less than 2 W
Snubber resistor R_s	400 Ω	To ensure the voltage overshoot across the auxiliary device $S_{auxa\&b}$ is less than 30% and the ringing is damped in 0.5 µs

*$\omega_{T1\&2\&3}$ is the resonant frequency and $Z_{T1\&2\&3}$ is the characteristic impedance for each resonant phase

5.7 Converter prototype description

A 1.2 kW demonstrator was constructed to validate the soft-switching solution and compare the performance with the hard-switching converter circuit. The converter layout remained unchanged, comprising a digital interface board, a main switching board and an output filter board. The interface board was extended to provide the isolated control signals and power supplies for driving the auxiliary transistors. The buffer circuit was also extended.

The main switching board, a four-layer PCB accommodated the main switching devices (top-cooled GaN HEMTs, GS66516T 650 V/60 A, from GaN Systems), switched diodes (SiC diodes, C3D10065E 650 V/15 A, from CREE), three GaN HEMTs (top-cooled GaN HEMTs, GS66508T 650 V/30 A, from GaN System) as the auxiliary devices and a SiC diode (same model as the switched diode) for resetting the auxiliary inductor current. The same low-side MOSFET drivers (LM5114, 7.6 A sink/ 1.3 A source, from TI) were used for the main and auxiliary transistors. The bottom of the main PCB is shown in Fig. 5.13.

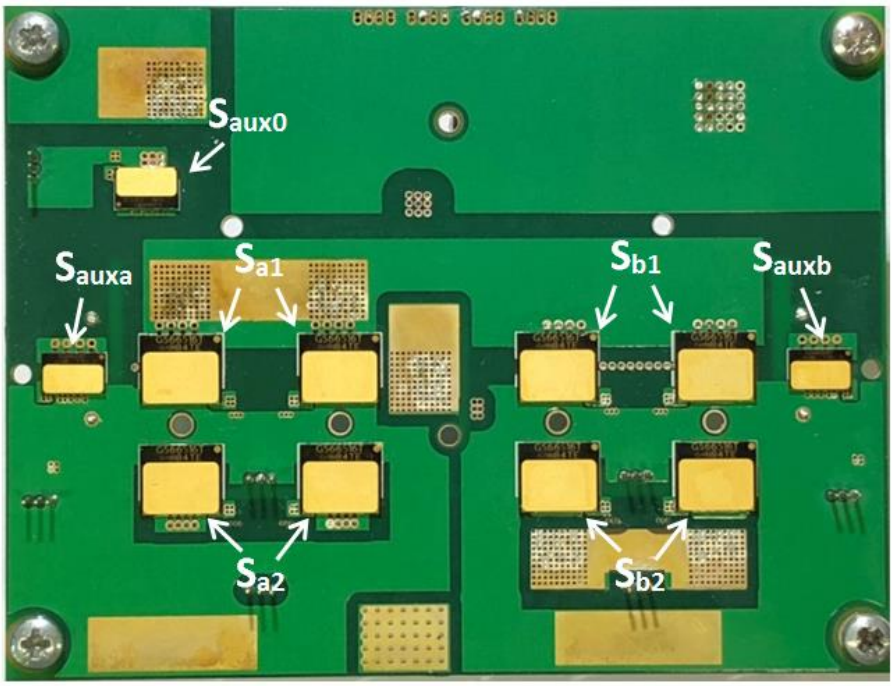
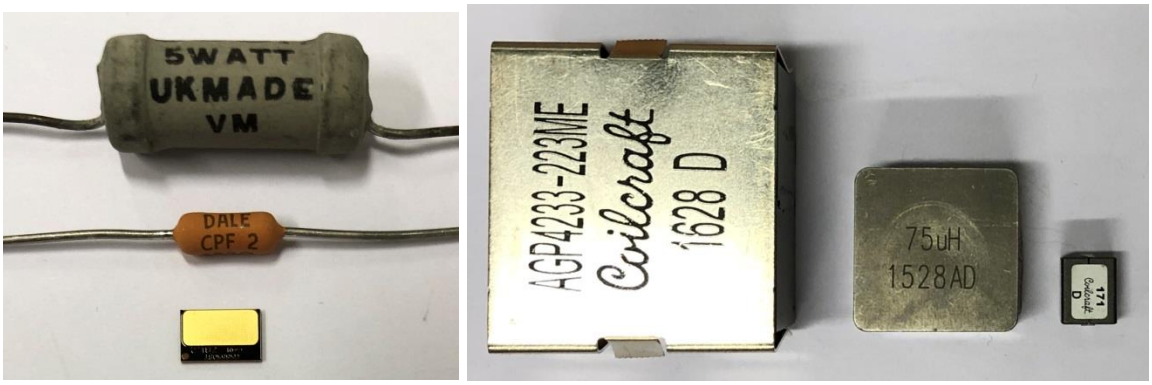


Fig. 5.13. Main circuit board on four-layer PCB (bottom side)

A metal film resistor (CPF 2 W from VISHAY) and a SMD 0603 ceramic capacitor serve as the snubber resistor and capacitor, which were mounted close to the two auxiliary switching devices S_{auxa} and S_{auxb}. Fig. 5.14 (a) shows the size comparison of a 2 W metal

film resistor, a generic 5 W metal film resistor and the target GaN HEMT that were used for the auxiliary switching device, which highlights the importance of limiting the snubber loss to manage the space and layout for the circuit board.



(a) *(b)*

Fig. 5.14. Size comparison of (a) 5 W resistor, 2 W resistor and GaN HEMT GS66508T (from top to bottom); (b) Output, input and auxiliary inductor (from left to right)

High thermal conductivity T-Clad (HR T30.20) was used for the output filter board. As before, the SMD 75 μH/ 12 A part (IHLP-8787MZ-5A) from VISHAY formed the input inductor and the 33 μH/ 22.5 A ferrite core part (AGP4233) from Coilcraft formed the output inductor. A chip inductor (SLR1075 0.17 μH/ 50 A) from Coilcraft was used as the auxiliary inductor. The three inductors are shown in Fig. 5.10 (b).

5.8 Simulation results

The converter was simulated in LTSPICE. SPICE models from the manufacturers were used for the GaN transistors, which include the device non-linear parasitic capacitance. The diode was modelled with parasitic capacitance given by the datasheet. The ideal model was used for the capacitors. The winding resistances from Table 4.6 are included in the inductor models. The simulation was run at the rated condition shown in Table 5.1. The steady-state waveforms are presented in Fig. 5.15, with Fig. 5.16 showing the zero-voltage switching transient in detail, which can be compared with the theoretical waveforms shown in Fig. 5.3 and Fig. 5.4. The drain-to-source voltage and current waveforms of the main transistors S_{a1}, S_{a2} and the auxiliary transistors S_{auxa}, S_{auxb} and S_{aux0} are shown in Fig. 5.17 to validate the soft-switching operation.

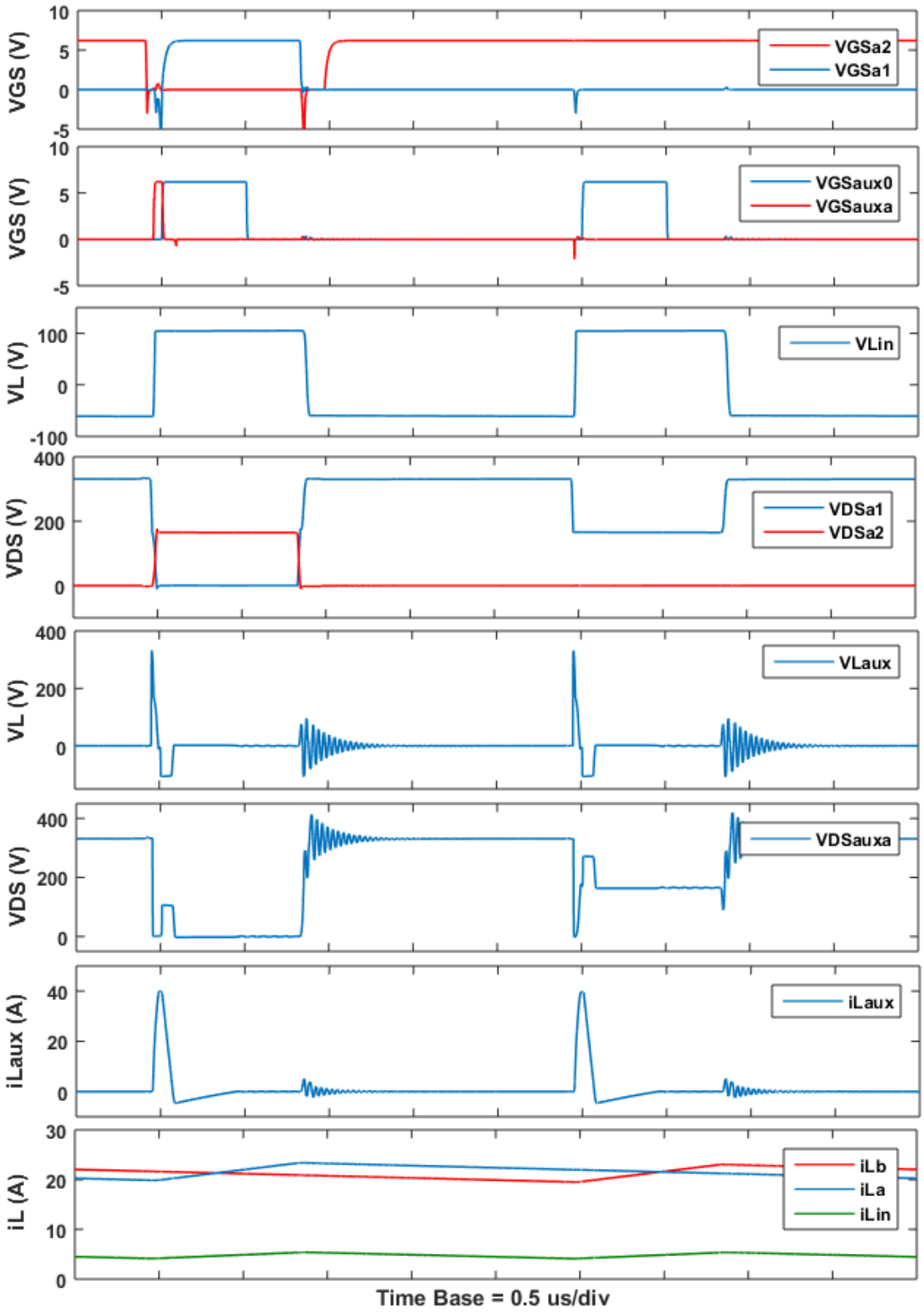


Fig. 5.15. Simulation results of the soft-switching converter operating at 270-28 V, 200 kHz, 1.2 kW

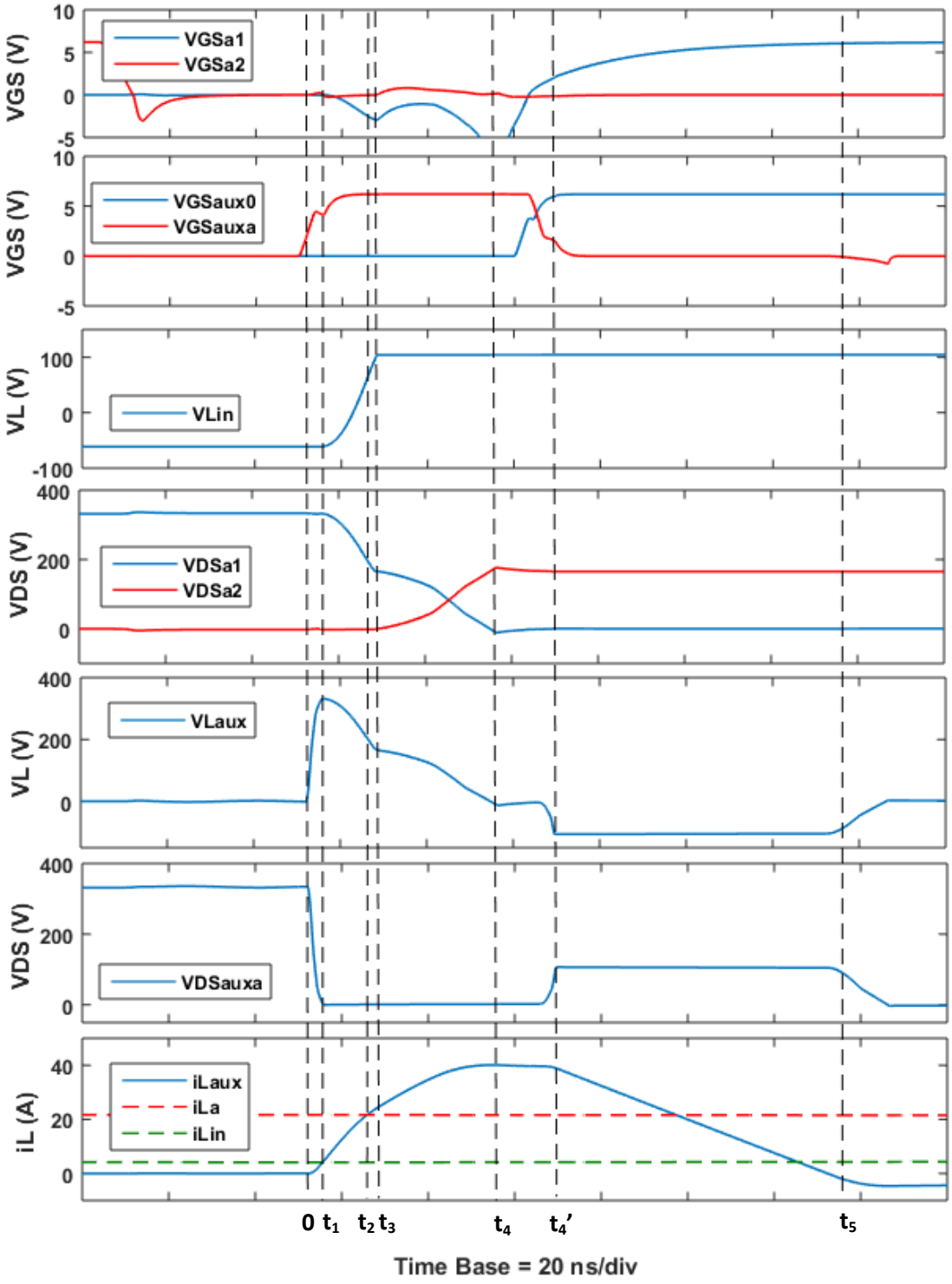


Fig. 5.16. Expanded simulation waveforms during 0~t_5 where zero-voltage turn on of S_{a1} is achieved when operating at 270-28 V, 200 kHz, 1.2 kW

It can be seen from Fig. 5.15 that the steady-state simulation waveforms are consistent with the theoretical expectations that are shown in Fig. 5.2. Only the voltage waveforms of the main and auxiliary devices in phase *a* are presented. However, the performance in the

other phase is the same, but delayed by half a cycle. It can be seen that the snubber circuit provides decent damping of the voltage oscillation across the auxiliary transistor during the transition of the DC link voltage from 0 to $2V_C$. A peak voltage overshoot of 25% is observed across the auxiliary device, and the settling time is 450 ns.

Fig. 5.16 shows the magnified simulation waveforms where zero-voltage turn on of S_{a1} occurs. It can be seen that the circuit performance of each stage exhibits the pattern as described in Fig. 5.4 with the circuit parameters based on Table 5.2. The on-time of the auxiliary device S_{auxa} was set to 50 ns i.e. $t_0 \sim t_4'$. Two resonant phases can be seen clearly. The auxiliary device S_{aux0} was turned on slightly in advance of the turn-off of S_{auxa} to ensure a path is available for the auxiliary inductor current when S_{auxa} turns off.

Two discrepancies with the ideal waveforms are seen in the simulations. Firstly, an additional free-wheeling period is observed from the simulation result which is indicated as $t_4 \sim t_4'$. At t_4, the third resonance phase ends and the auxiliary inductor voltage has dropped to zero. The auxiliary inductor freewheels in the loop formed by the auxiliary inductor L_{aux}, auxiliary device S_{auxa} and main device S_{a1} until the auxiliary device S_{auxa} is turned off. This stage will create conduction loss in the components in the freewheeling loop, therefore it should be as short as possible. The main device S_{a1} needs to be gated on during this stage to avoid the penalty of the extra voltage drop of the reverse conducting GaN HEMT. Another unexpected feature that has been observed is the reversal of the auxiliary inductor current after t_5. This is due to the reverse recovery and reverse bias capacitance of the auxiliary diode D_{aux}. Once established the reverse current circulates through S_{a1} and the body diode of S_{auxa}, resulting in a small increase in the conduction loss in the main device S_{a1}. This extra inductor current will gradually reduce to zero at a rate of $[V_{DSa1(on)}+V_{DSauxa(on\_rev)}]/L_{aux}$.

Table 5.3 compares the key variable values for each stage from the simulation results and the theoretical calculations shown in section 5.4.1. It can be seen that the values from the theoretical calculations and simulation results show a very good agreement. The minor differences are because the device output capacitance is considered as linear and the circuit efficiency in the theoretical prediction is assumed to be 95%.

Table 5.3 Analytical and simulation results of key variables at 270-28 V, 200 kHz, 1.2 kW

Parameters	Analytical	Simulation	Comments
$t_0 \sim t_1$	2.5 ns	2.6 ns	Auxiliary inductor linearly charged
$t_1 \sim t_2$	8.4 ns	8.7 ns	First resonant phase
$t_2 \sim t_3$	4.3 ns	3.9 ns	Remaining time for DC link voltage transition
$t_3 \sim t_4$	23.9 ns	26.7 ns	Second resonant phase
$t_4 \sim t_4'$	NA	12.2 ns	Current freewheeling until S_{auxa} turns off
$t_4' \sim t_5$	61.6 ns	63.8 ns	Auxiliary inductor linearly discharged
$i_{Laux}(t_1)$	3.9 A	3.8 A	Auxiliary inductor exceeds input inductor current
$V_{DSa1}(t_1)$	325.6 V	330.7 V	Initial DC link voltage $2V_C$
$i_{Laux}(t_2)$	18.6 A	19.9 A	Auxiliary inductor current exceeds i_{La}
$V_{DSa1}(t_2)$	247.2 V	236.2 V	Auxiliary inductor voltage after first resonant phase
$i_{Laux}(t_3)$	25.7 A	24.2 A	Auxiliary inductor current after DC link voltage transition
$V_{DSa1}(t_3)$	162.8 V	165.3 V	DC link voltage falls to V_C
$i_{Laux}(t_4)$	40.2 A	40.2 A	Peak current in auxiliary inductor
$V_{DSa1}(t_4)$	0 V	0 V	ZVS condition for S_{a1} realized

The loss conditions of the main and auxiliary transistors during the switching transients are summarized in Table 5.4. Fig. 5.17 shows the simulated current and voltage of the top and bottom devices S_{a1}, S_{a2}, and auxiliary devices S_{auxa}, S_{aux0} during the switching transients corresponding to the waveforms shown in Fig. 5.16.

Table 5.4 Switching conditions of main and auxiliary devices

	S_{a1}/S_{b1}	S_{a2}/S_{b2}	S_{auxa}/S_{auxb}	S_{aux0}
Turn-on	ZVS -lossless	ZVS -lossless	ZCS -low loss	ZVS -lossless
Turn-off	Soft-switching (snubber)* - low loss	ZVS -lossless	Hard-switching -lossy	ZCS -lossless

* Device output capacitance acts as snubber capacitance

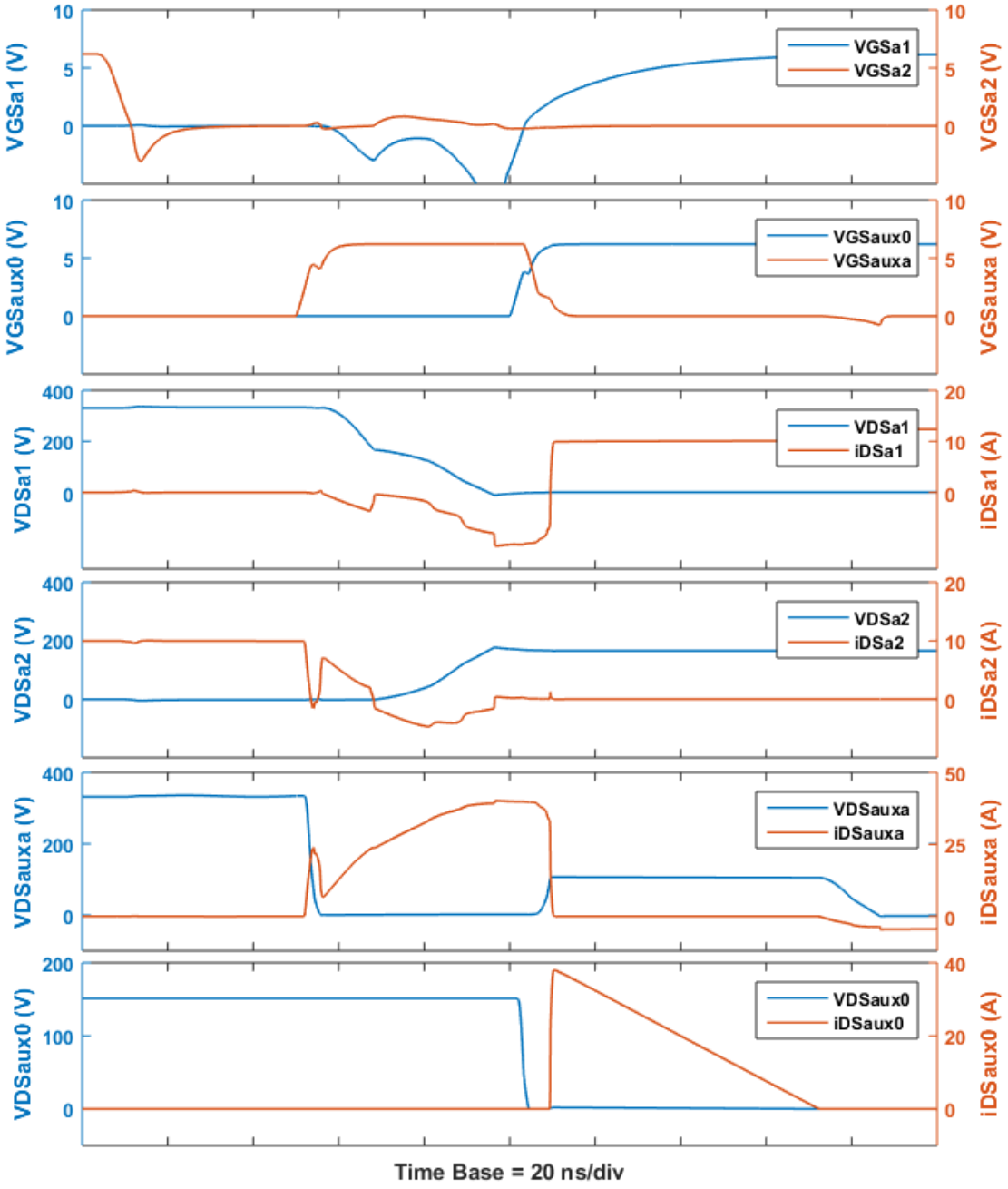


Fig. 5.17. Expanded simulation waveforms corresponding to Fig. 5.13 showing the transistor voltage and current at 270 V-28 V, 200 kHz, 1.2 kW

The discharging current in the top device S_{a1} can be observed during the two resonant phases. After the output capacitor is fully discharged and the device voltage falls to zero, S_{a1} starts reverse conduction during the freewheeling stage t_4~t_4' until it is signalled to conduct. The bottom device current i_{DSa2} initially falls in a consistent pattern with the rise in the auxiliary device current i_{DSauxa} because the freewheeling current in S_{a2} is commutating to the auxiliary device S_{auxa}. When the second resonant phase starts, i_{DSa2} is

approximately equal but opposite to the top device current i_{dsa1} since the S_{a1}, S_{a2} output capacitances are charged/discharged in a complementary manner. Therefore, no turn-off loss occurs in S_{a2}. The auxiliary device S_{auxa} turns on at zero current. However, an initial current pulse flows due to the discharge of the output capacitor, which will cause capacitive turn-on losses. The turn off of S_{auxa} is a hard switching transient. The auxiliary device S_{aux0} turns on with ZVS and turns off with ZCS as the device voltage and current rise and fall naturally accordingly to the circuit operation.

Fig. 5.18 shows the simulation waveforms for operation at 270 V-28 V, 200 kHz, 1.6 kW to demonstrate the circuit performance at heavy load as described in 5.4.2. The on-time of S_{auxa} was increased to 60 ns to ensure the ZVS transition had time to complete. Different auxiliary inductance or circuit parasitic capacitances could also trigger this pattern at lower powers. Table 5.5 shows the duration of each stage from the theoretical calculation and simulation results at this condition.

Table 5.5 Analytical and simulation results of key variables at 1.6 kW, 270 -28 V, 200 kHz

Parameters	Analytical	Simulation	Comments
$t_0 \sim t_1$	2.5 ns	2.5 ns	Auxiliary inductor linearly charged
$t_1 \sim t_2$	12.4 ns	12.2 ns	First resonant phase
$t_2 \sim t_3$	5 ns	3.4 ns	DC link voltage transition completes; Auxiliary inductor linearly charged
$t_3 \sim t_4$	23.9 ns	27.4 ns	Second resonant phase
$t_4 \sim t_4'$	NA	16.5 ns	Current freewheeling until S_{auxa} turns off
$t_4' \sim t_5$	67.9 ns	75 ns	Auxiliary inductor linearly discharged
$i_{Laux}(t_2)$	24.3 A	24.2 A	Auxiliary inductor current after DC link voltage transition completes
$V_{DSa1}(t_2)$	162.8 V	165.5 V	DC link voltage falls to V_C
$i_{Laux}(t_3)$	25.3 A	28.2 A	Auxiliary inductor current reaches i_{La}
$V_{DSa1}(t_3)$	162.8 V	165.2 V	Voltage across S_{a1} maintains at V_C
$i_{Laux}(t_4)$	42.8 A	47.4 A	Peak current in auxiliary inductor
$V_{DSa1}(t_4)$	0 V	0 V	ZVS condition for S_{a1} realized

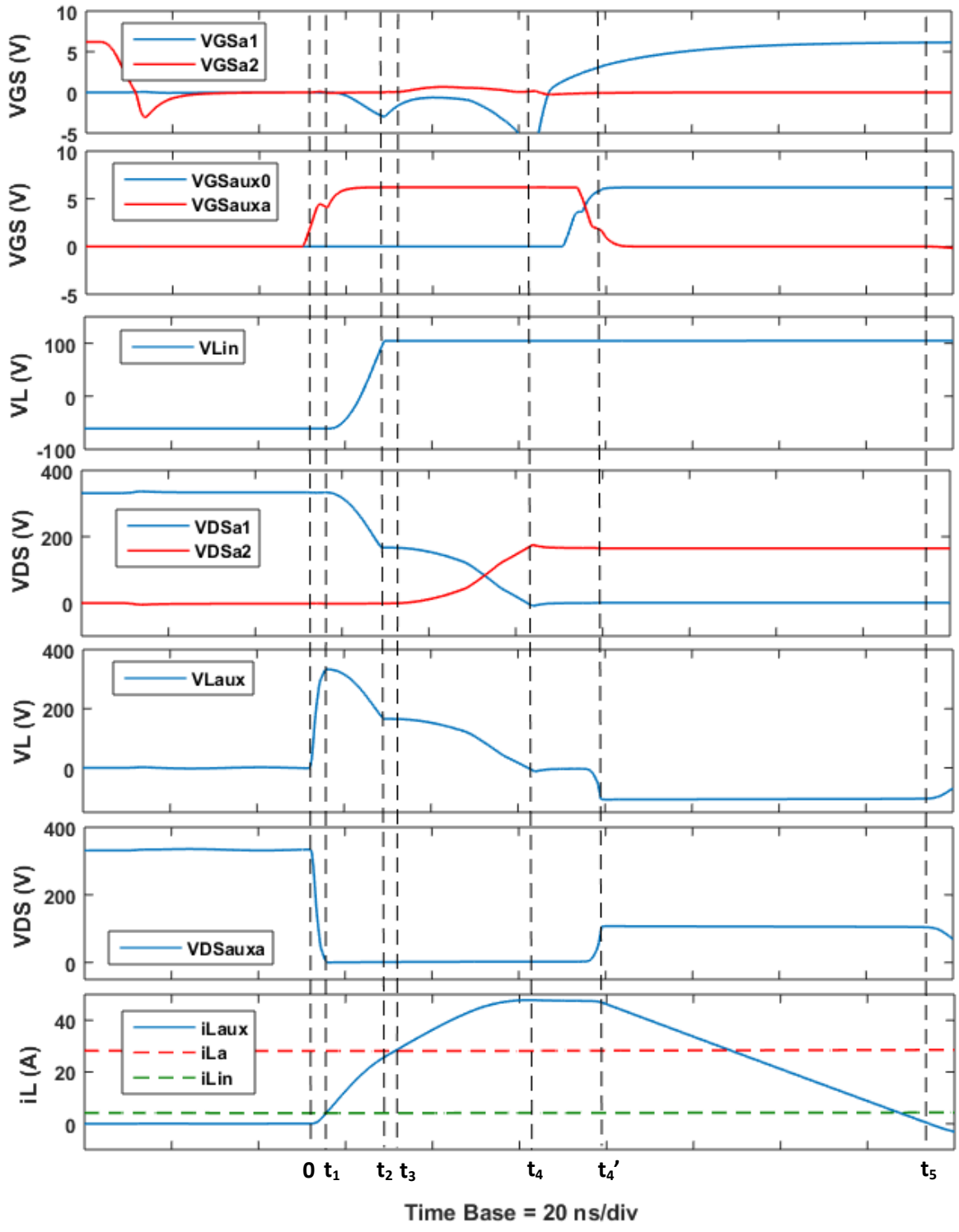


Fig. 5.18. Expanded simulation waveforms during t_0~t_5 where zero voltage turn on of S_{a1} is achieved when operating at 270-28 V, 200 kHz, 1.6 kW

5.9 Experimental results

The prototype was tested up to 1.2 kW. The gate signals of the main and auxiliary transistors are shown in Fig. 5.19, which were generated using a TI microcontroller. The main and auxiliary duty ratios were set to 0.17 and 0.01. The dead times between the top and bottom devices were set to 100 ns and 150 ns.

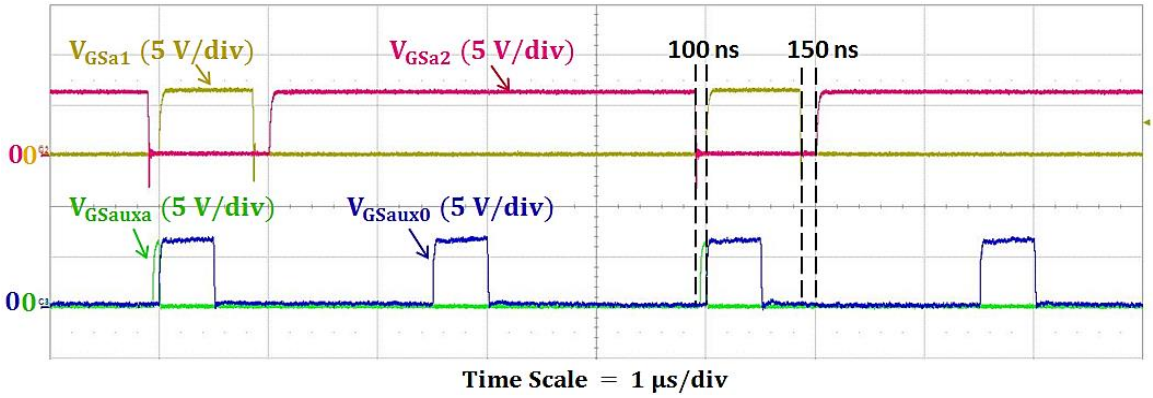
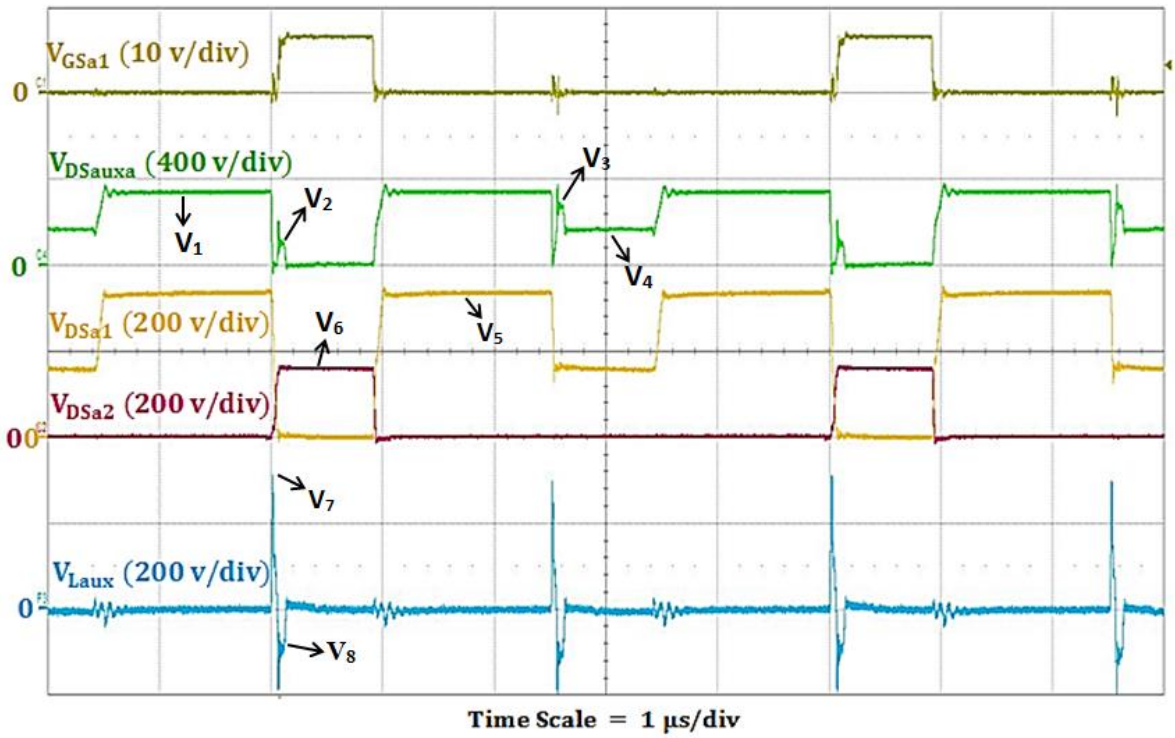


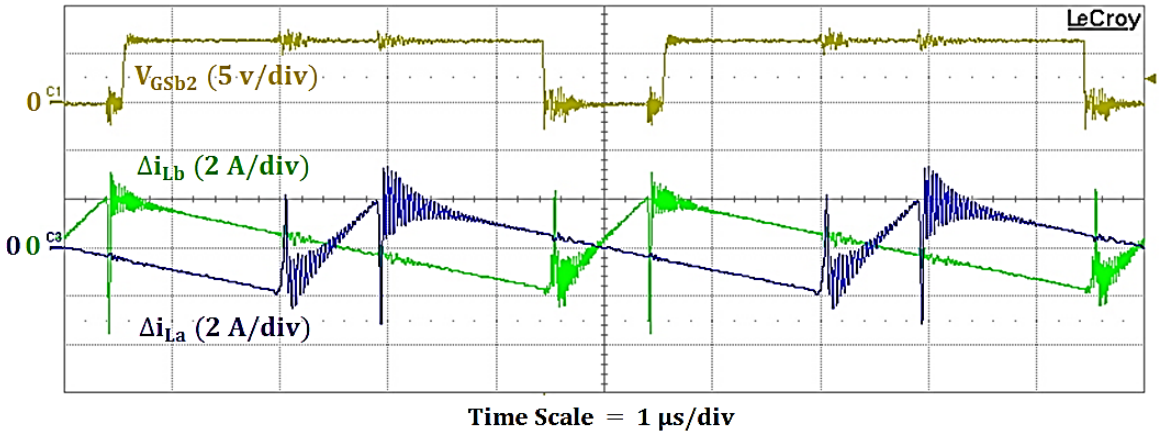
Fig. 5.19. Gate signals of main and auxiliary transistors S_{a1}, S_{a2}, S_{auxa} and S_{aux0}

The experimental waveforms of the drain-to-source voltage for the transistors in phase *a* and the auxiliary inductor voltage were recorded when operating at 270.9 V to 28.6 V, 200 kHz and 1.2 kW. The results are presented in Fig. 5.20 (a). The ripple current of the output inductors and the gate signal of the bottom device in phase *b* are shown in Fig. 5.20 (b).

It is evident that the experimental waveforms are clean and consistent with the theoretical steady-state waveforms. The voltage waveforms of the transistors in one phase are shown. However, the behaviour of the other phase is also evident in the waveforms, causing the reduction in V_{DSa1} and auxiliary transistor voltage V_{DSauxa} whilst the devices are in the off-state. The interleaved operation between phase *a* and *b* can be seen from the ripple current of the output inductors shown in Fig. 5.20 (b), which will double the ripple current frequency in the input inductor, input capacitor, switched capacitor and output capacitor, resulting in a size reduction in these passive components. Transients are seen in the inductor current waveforms at the switching point due to the charging/discharging of the inductor parasitic capacitance, however the subsequent high frequency oscillation was attributed, at least in part, to the Rogowski coil used for current measurement.



(a)



(b)

Fig. 5.20. Experimental waveforms of (a) main and auxiliary transistor voltages and (b) ripple current of output inductors for V_{in} = 270.9, V_o = 28.6 V, f = 200 kHz, i_{out} = 39.1 A, P_{in} = 1.21 kW and D = 0.17

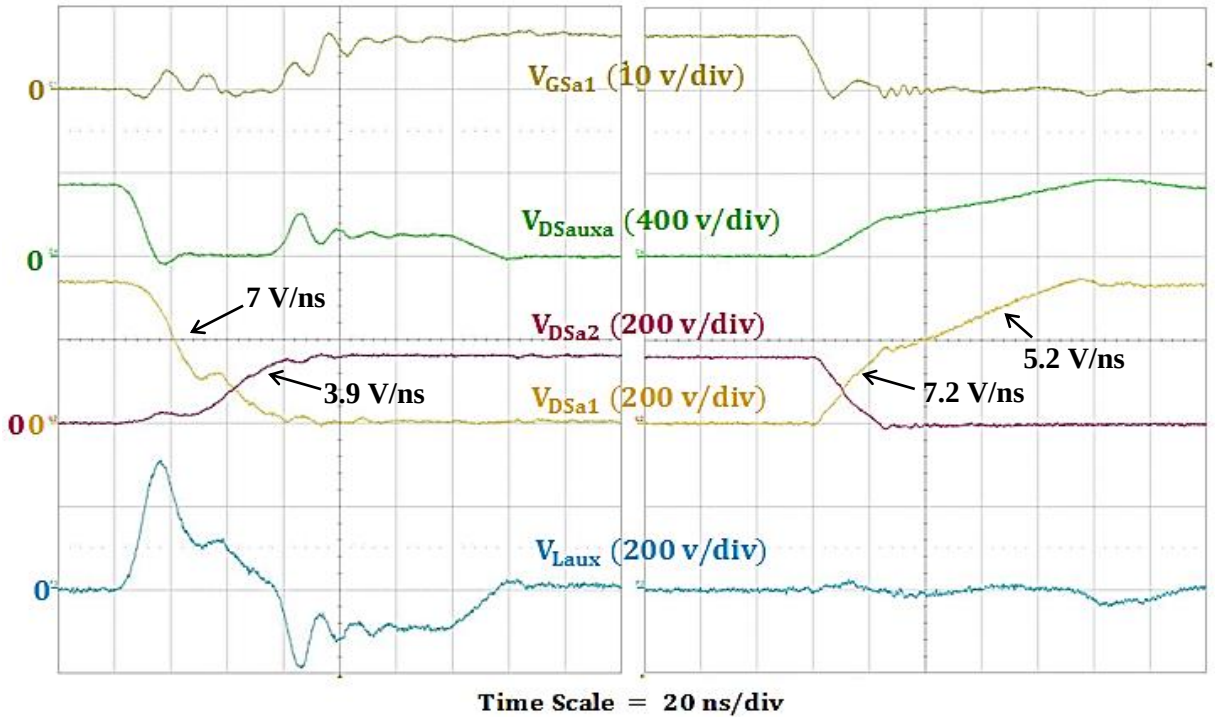
It can be seen from Fig. 5.20 (a) that there is virtually no ringing in the main transistor voltages V_{DSa1} and V_{DSa2} due to the well-controlled turn-on and turn-off conditions. However, very small voltage oscillations are observed in V_{DSauxa} at the turn-off instant due to the hard-switching transient. The voltage oscillations in V_{DSauxa} during the transition of DC link voltage that are caused by the resonance between the auxiliary inductor and the

output capacitance of the auxiliary transistor voltage, are very well controlled, proving the effectiveness of the RC snubbers. The key voltage values marked in Fig. 5.20 (a) are measured and compared with the theoretical values, shown in Table 5.6. The experimental values present an excellent match with the theoretical expectations except for V_7 where 36.7 V of difference is noticed. This is because the voltage across S_{auxa} does not fall to zero instantaneously after turn-on in the prototype, resulting in the peak in the auxiliary inductor voltage being slightly delayed to a point where the DC link voltage is already less than $2V_C$.

Table 5.6 Comparison of key voltage values between experimental and analytical results

	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8
Theory	$2V_C$	V_{in}-V_C	V_{in}	V_C	$2V_C$	V_C	$2V_C$	V_{in}-V_C
Analytical	332.6	104.6	270.9	166.3	332.6	166.3	332.6	104.6
Experimental	332.9	106.3	273.8	165.6	335.4	162.2	295.9	100.7

Fig. 5.21 shows the experimental waveforms of V_{GSa1}, V_{DSa1}, V_{DSa2} and V_{Laux} during the switching transients of the top device S_{a1}. The on-time of the auxiliary device S_{auxa} was set to be 50 ns which can be found from the V_{DSauxa} waveform. It can be seen that the output capacitor of S_{a1} has just been fully discharged before S_{auxa} turns off, indicating that ZVS is achieved within 50 ns. The short conduction time of 50 ns will limit the conduction loss in the auxiliary transistors and auxiliary inductor. S_{a1} is switched on immediately after the drain-to-source voltage falls to zero to avoid the reverse-gate-bias conduction of the GaN HEMTs. After the auxiliary switch S_{auxa} turns off, the auxiliary inductor current is diverted to the reset path consisting of S_{aux0} and D_{aux0}. The auxiliary inductor voltage V_{Laux} corresponds to the change of V_{DSauxa} since the top device S_{a1} has already turned on. During the turn-off transient of S_{a1}, two charging stages can be observed from Fig. 5.21 (b). First the output inductor current divides between the output capacitance of S_{a1} and S_{a2}, providing snubber action for the turn off of S_{a1}. V_{DSa2} falls to zero then i_{La} diverts to the freewheel path through S_{a2}. Second, diodes D_a and D_b turn off and the input inductor current charges the parasitic capacitance in the DC link until D_0 becomes forward bias and the DC link voltage equals $2V_C$.



(a) (b)

Fig. 5.21. Experimental waveforms during the switching transients of S_{a1} for V_{in} = 270.9, V_o = 28.6 V, f = 200 kHz, i_{out} = 39.1 A, P_{in} = 1.21 kW and D = 0.17 (a) S_{a1} turn-on transient; (b) S_{a1} turn-off transient

Fig. 5.22 presents the comparison of the experimental waveforms shown in Fig. 5.21 (a) and the simulation waveforms shown in Fig. 5.16 to validate the circuit performance during t_0~t_5 where ZVS of S_{a1} is achieved. It can be seen that the circuit largely operates as expected. The dv/dt of S_{auxa} during the switching transient is seen to be slower in the experimental waveforms, attributed to the additional parasitic capacitance in the prototype that was not modelled in the simulation and also the second resonant phase becomes slightly longer which might be due to the mismatch in the transistor SPICE model parameters for the device output capacitance at lower voltage.

Apart from this, two effects in the experimental waveforms are noticed which differ from the simulation results, marked in A and B in Fig. 5.22. First (A), a voltage reduction in V_{DSa1} can be observed when the DC link voltage transition finishes. This is due to the stray inductance in the front-end circuit, including the package inductance of diodes, which is not modelled in the simulation. As the voltage transition in the front-end circuit completes, the current in diodes D_a and D_b starts to rise rapidly, resulting in a voltage drop across the stray inductance. The voltage reduction in the DC link can therefore be seen in V_{DSa1}.

Second (B), the voltage of the bottom device S_{a2} is seen to be increased by a small amount right after the auxiliary transistor S_{auxa} turns on, whilst in the simulation results, the output capacitor of S_{a2} is not charged until the DC link voltage transition completes (second resonance phase starts). This is attributed to the effects of additional stray inductance and stray capacitance in the practical prototype.

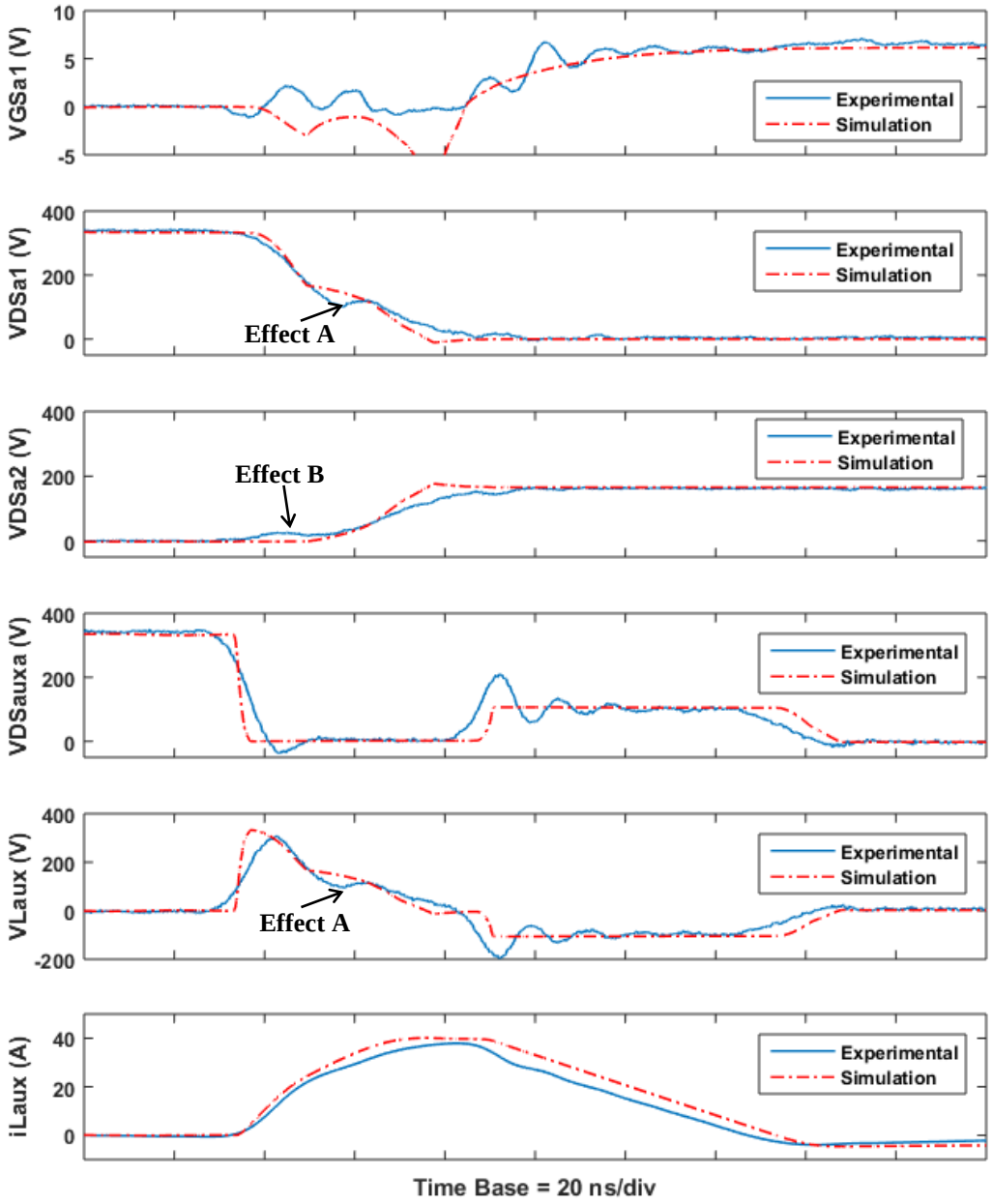
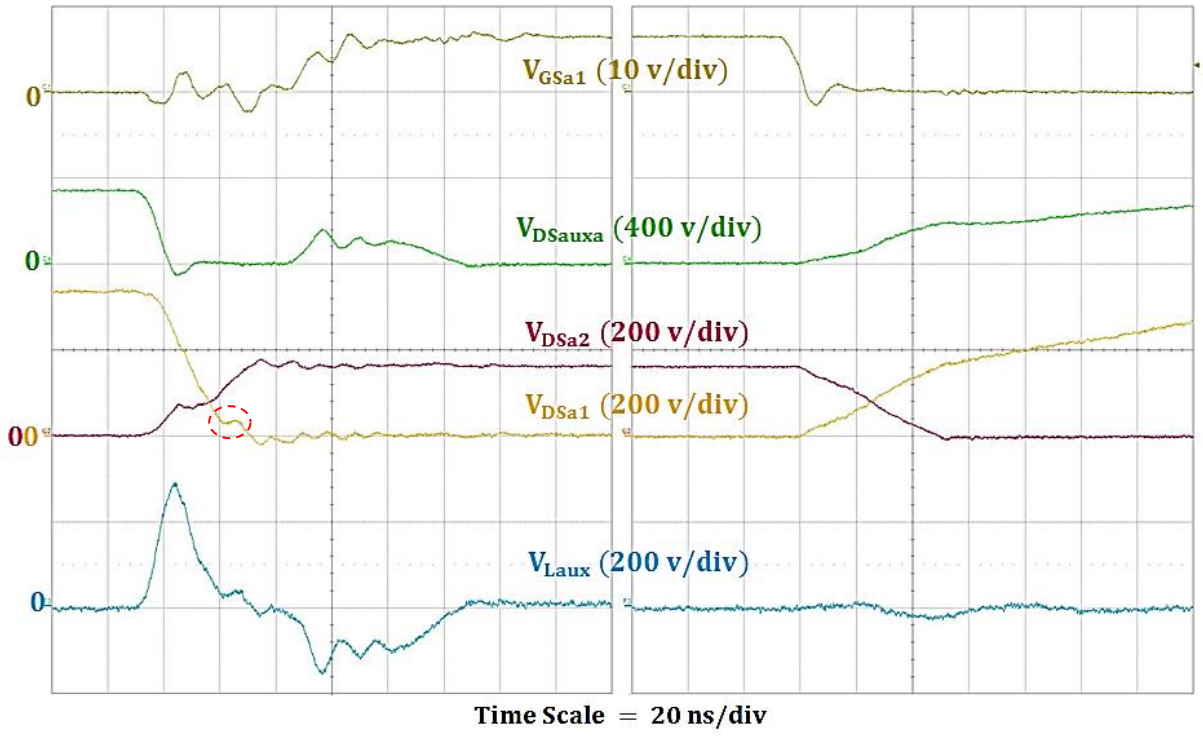


Fig. 5.22. Comparison of experimental and simulation waveforms during t_0~t_5 for 270-28 V, 200 kHz, 1.2 kW

Fig. 5.23 shows the experimental waveforms of the converter operating at 400 W to demonstrate the circuit performance at reduced load. It can be seen that the ZVS turn-on

transition for S_{a1} becomes shorter compared to the previous condition, since the output inductor current i_{La} is now much lower than the peak current in i_{Laux}, resulting in a larger charging current for the leg capacitance. In contrast, the voltage transition during the turn-off of S_{a1} becomes much longer since the current responsible for charging and discharging the parasitic capacitance is reduced.

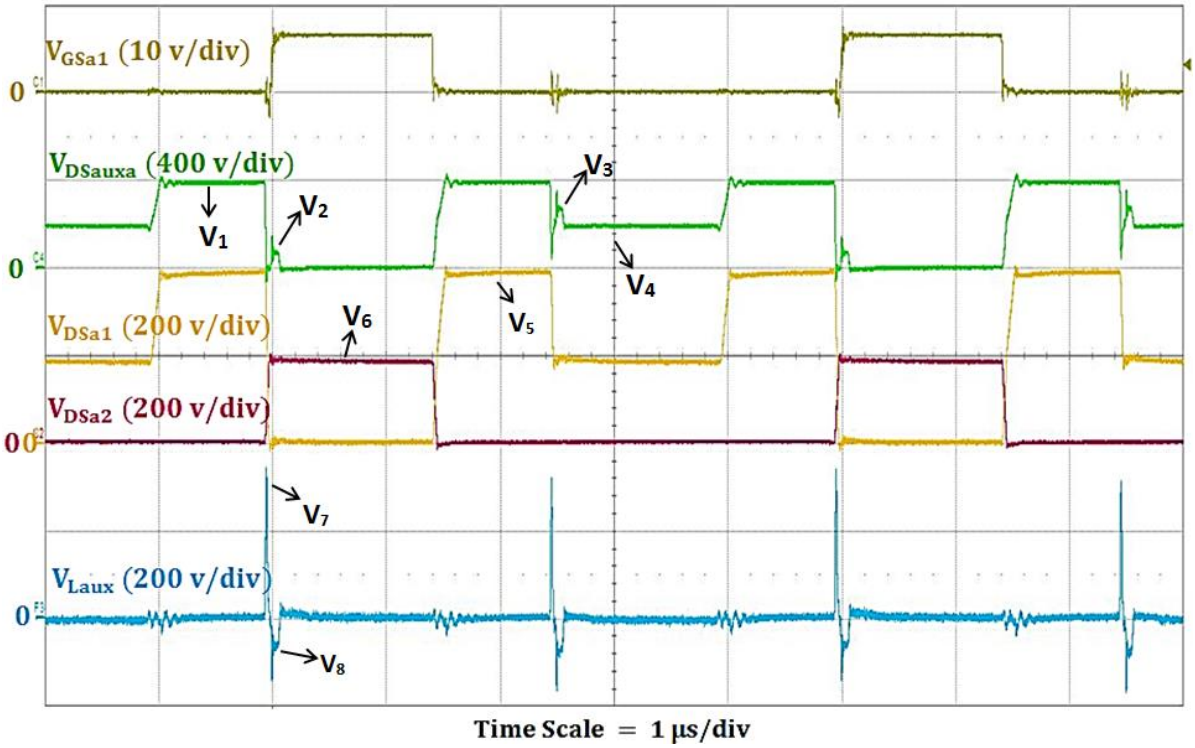
It can be found that the initial rise in the bottom device voltage V_{dsa2} due to effect B becomes more pronounced in this case. In addition, the reduction in V_{dsa1} due to effect A appears much later, almost at the end of the transient, indicating that the completion of the DC link voltage transition is delayed due to the slower discharging rate of the output capacitance of the front-end diodes during the first resonance phase.



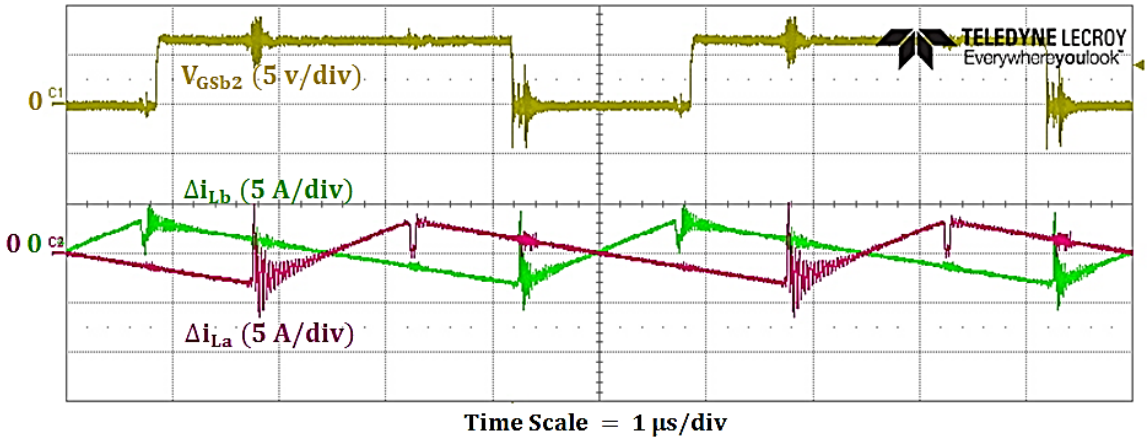
(a) (b)

Fig. 5.23. Experimental waveforms during (a) S_{a1} turn-on transient and (b) S_{a1} turn-off transient of S_{a1} for V_{in} = 270.9, V_o = 28.3 V, f = 200 kHz, i_{out} = 14.6 A, P_{in} = 461 W and D = 0.17

The converter performance was then examined when operating at a duty ratio of 0.29, which results in a voltage conversion of 270 V to 56 V. The switching frequency of 200 kHz and an auxiliary duty ratio of 0.01 remained unchanged. The experimental waveforms for P_{in} = 1.21 kW are shown in Fig. 5.24.



(a)



(b)

Fig. 5.24. Experimental waveforms of (a) main and auxiliary transistor voltage and (b) ripple current of output inductors for V_{in} = 270.9, V_o = 56.3 V, f = 200 kHz, i_{out} = 20.2 A, P_{in} = 1.21 kW and D = 0.29

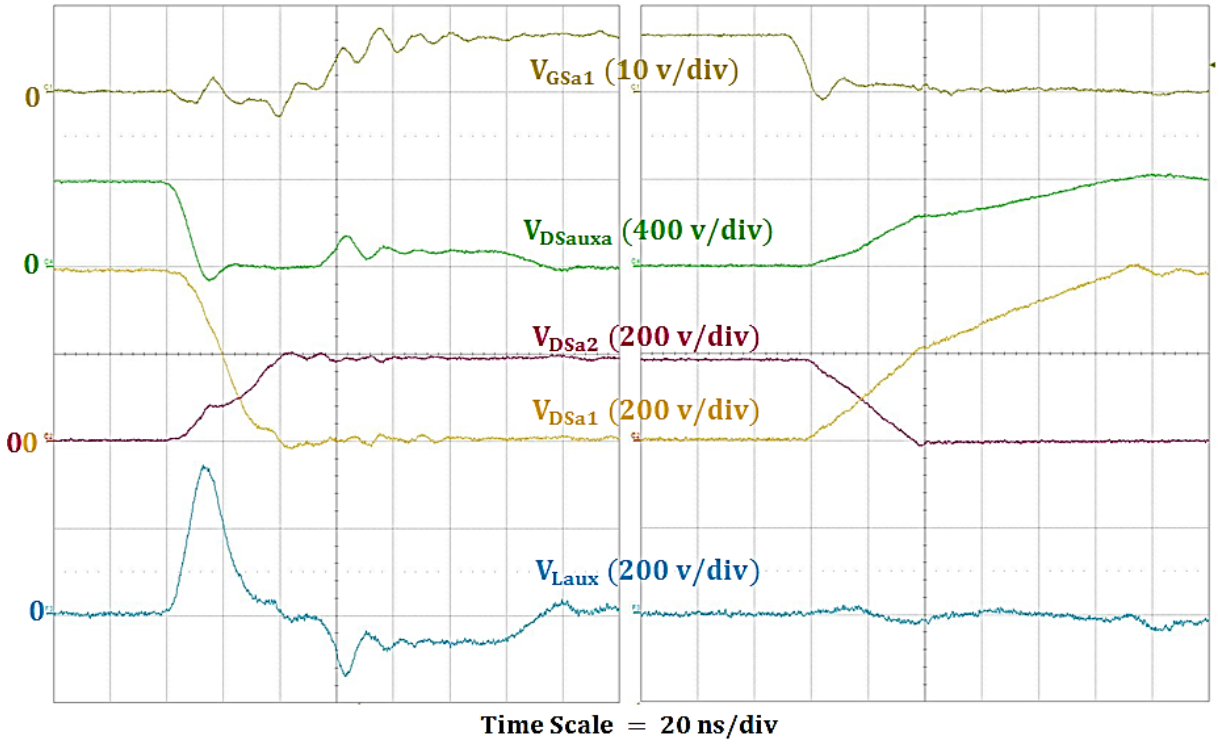
The key voltage values in the waveforms are summarised and compared again with the theoretical values in Table 5.7. It can be seen that the shape of the voltage waveforms is very similar to before, but the voltage values during each stage have changed, since the voltage of the switched capacitor V_C is now increased to 193.1 V, indicated in Table 5.7. A

peak voltage of 391 V is observed across the transistors. The output inductor current ripple is also increased due to the larger duty ratio.

Table 5.7 Comparison of key voltage values between experimental and analytical results

	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8
Theory	$2V_C$	V_{in}-V_C	V_{in}	V_C	$2V_C$	V_C	$2V_C$	V_{in}-V_C
Analytical	386.2	77.8	270.9	193.1	386.2	193.1	386.2	77.8
Experimental	382.8	76.3	270.4	195.8	391	190.6	339.1	75.5

The magnified experimental waveforms for the same switching transients are shown in Fig. 5.25. It can be seen that the circuit performance during the switching transients is very similar to that seen at the reduced load condition shown in Fig. 5.23, since in both cases the output inductor current is reduced.



(a) (b)

Fig. 5.25. Experimental waveforms during the switching transients of S_{a1} for V_{in} = 270.9, V_o = 56.3 V, f = 200 kHz, i_{out} = 20.2 A, P_{in} = 1.21 kW and D = 0.29 (a) S_{a1} turn-on transient; (b) S_{a1} turn-off transient

5.10 Converter energy management

The loss breakdown of the converter operating at 1.2 kW with a duty ratio of 0.17 was calculated based on the simulation waveforms. The results are summarized in Table 5.8. The device junction temperature was assumed to be the same as the measured case temperature. The impact of PCB and inductor parasitic capacitance was included based on the measured values in Table 4.5. The losses in the capacitors are neglected due to the very small ESR of ceramic capacitors. The PCB tracks have been designed to have minimal losses.

The switching energy in the transistors was estimated based on (5-39). The gate driving circuit of the auxiliary transistor in the simulation was modified to match the dv/dt in the experimental conditions.

$$E_{sw} = \int_0^{T_{sw}} V_{ds}(t)\, i_{ds}(t) dt \tag{5-39}$$

where T_{sw} is the switching time.

The main transistors actual turn-off energy should be the calculated value using (5-39) minus the output capacitor stored energy during $2V_C \sim V_C$ i.e. 4.1 μJ for the GS66516T since this stored energy will be recycled in a lossless manner during the next ZVS turn-on transient.

The conduction losses of the transistors and diodes were estimated using (4-26), (4-27) and (4-28), Chapter 4.

The inductor copper loss was estimated using (4-29). The core loss was obtained from the inductor loss calculation tool provided by the manufacturer, which assumes sinusoidal flux and is therefore likely to underestimate the loss arising from narrow duty-ratio pulse operation.

It can be seen that the main transistor conduction loss contributes the most to the total converter loss, followed by the auxiliary transistor switching losses. Most of the main transistor switching loss has been removed, which only accounts for 0.6% of the total loss due to the soft-switching operation. The auxiliary circuit introduces additional loss, 26.4% of the total loss, which is dominated by the switching loss of the auxiliary transistor. The

predicted loss of 68.3 W compares with a measured loss in the prototype of 91.7W, which was attributed to additional stray losses for example in the auxiliary inductor.

Table 5.8 Converter loss breakdown at 270-28 V, 200 kHz, 1.2 kW

Loss factors		Component parameters	Loss (W)	Percentage contribution
Main circuit				
Main transistor S_{a1} & S_{a2}	Switching	E_{off} = 4.5 μJ using (5-40)	0.6	0.6%
	Conduction	$R_{ds(on)}$ = 30 mΩ @ 42℃; $K_{dy\text{-}Sa1}$=1.35; $K_{dy\text{-}Sa2}$=1.16	17.4	25.5%
	Reverse conduction	V_f = 1.3 V	2.1	3.1%
Switched diodes D_a and D_b		V_f = 1.2 V @ i_D = 4 A	7.4	10.9%
Switched diode D_0		V_f = 1.1 V @ i_D = 5 A	3.7	5.4%
Input inductor L_{in}	Copper	R_{DC} = 29.8 mΩ; $i_{Lin\text{-}DC}$ = 5.2 A R_{AC} = 1.8 Ω; $\Delta i_{Lin\text{-}rms}$ = 0.4 A	1.1	1.6%
	Core	volt-sec = 1.2 T·cm^2	4.8	7%
Output inductor L_a & L_b	Copper	R_{DC} = 2.8 mΩ; $i_{La\text{-}DC}$ = 20.4 A R_{AC} = 0.9 Ω; $\Delta i_{La\text{-}rms}$ = 1 A	4.4	6.4%
	Core	volt-sec = 1.1 T·cm^2	5.8	8.5%
Total main circuit loss			47.3	69.1%
Auxiliary circuit				
Auxiliary transistor S_{auxa} & S_{auxb}	Switching	E_{on} = 6 μJ; E_{off} = 12.9 μJ	11.8	17.3%
	Conduction	$R_{ds(on)}$ = 60 mΩ @ 39℃	1.5	2.2%
Auxiliary transistor S_{aux0} conduction		$R_{ds(on)}$ = 50 mΩ	0.7	1.0%
Auxiliary diode D_{aux0}		V_f = 2 V @ i_D = 20 A	1.5	2.2%
Auxiliary inductor L_{aux}	Copper	R_{AC} = 7.6 mΩ; $\Delta i_{Laux\text{-}rms}$ = 6.8 A	0.4	0.6%
	Core	volt-sec = 67 mT·cm^2	1.1	1.6%
RC snubber		C_s = 0.01 nF	1.0	1.5%
Total auxiliary circuit loss			18.0	26.4%
PCB tracks			3.0	4.4%
Efficiency				
Total Loss (W)			68.3 W	
Efficiency			94.3%	

The thermal condition of the converter operating with a duty ratio of 0.17 at 1.2 kW was monitored using a thermal camera, shown in Fig. 5.26. The surface temperatures of the main components are summarized in Table 5.9.

Although the accuracy of the temperature measurement from the thermal camera is subject to some uncertainty due to the material emissivity, camera resolution and spot size, it still provides a good indication of the temperature rise in each component. It can be found that the temperature of the main and auxiliary transistors is very well controlled due to the soft-switching operation, all of which are lower than 50℃ at 1.2 kW, 200 kHz. However, the temperature rise of the auxiliary inductor is severe with a surface temperature of 79.6℃, which is much greater than that expected based on the loss estimation in Table 5.8. Furthermore the internal temperature is likely to exceed 100℃, which is a limitation on further increases of the converter switching frequency and power level. A customised auxiliary inductor that is specifically designed for pulsed operation and with improved thermal management would be needed for higher power and switching frequency.

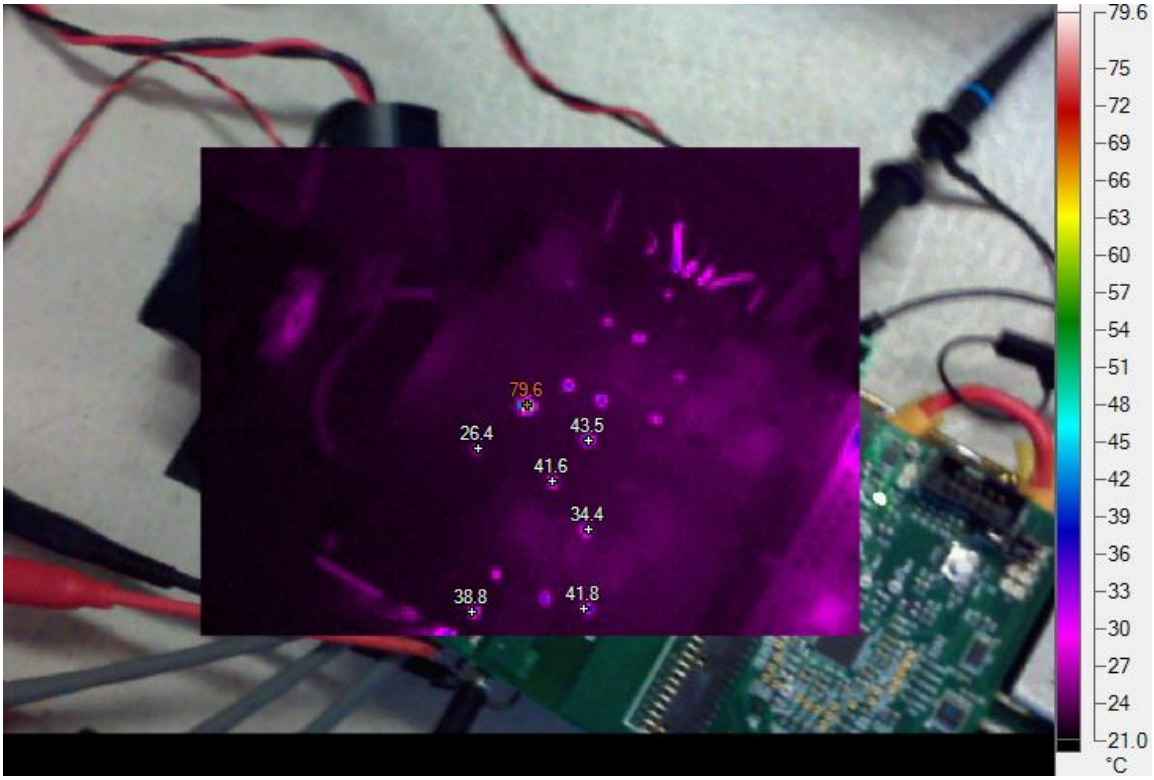


Fig. 5.26. Thermal image of the prototype for operation at V_{in} = 270.9, V_{out} = 28.6 V, f = 200 kHz, i_{out} = 39.1 A, P_{in} = 1.21 kW and D = 0.17

Table 5.9 Component case temperatures

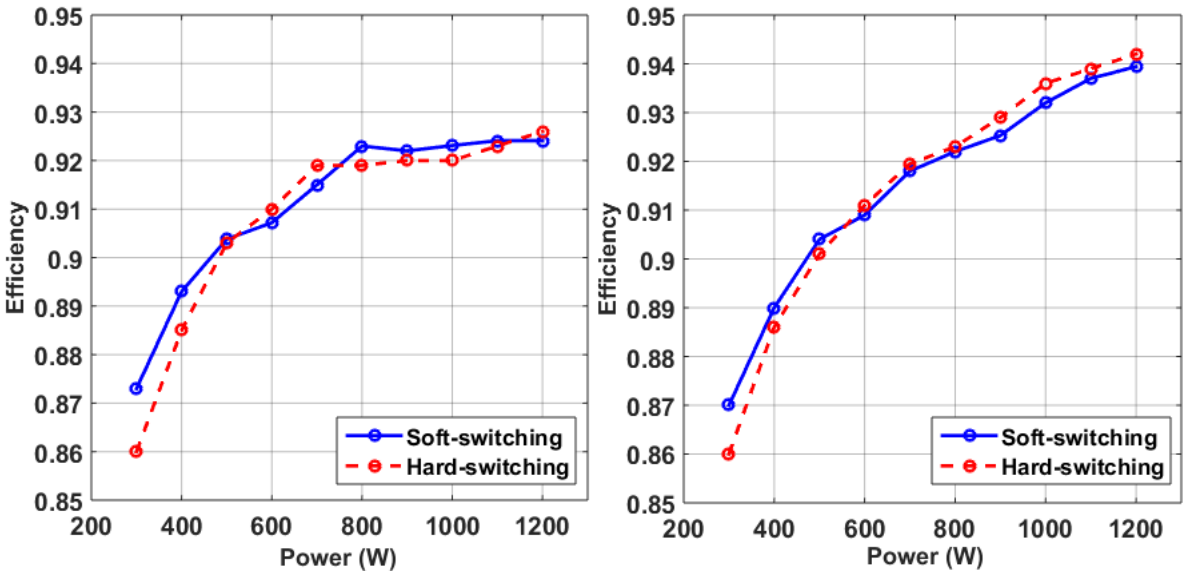
Component	Input inductor L_{in}	Auxiliary inductor L_{aux}	Top transistor S_{a1}	Bottom transistor S_{a2}	Auxiliary transistor S_{auxa}	Switched diode D_a	Switched diode D_0
T_{case} (℃)	26.4	79.6	41.6	34.6	38.8	41.8	43.5

5.11 Comparison with hard-switching converter

The comparison of estimated losses in the hard-switching and soft-switching converter operating at 270-28 V, 200 kHz, 1.2 kW is shown in Table 5.10. It can be seen that the soft-switching circuit is predicted to have a loss reduction of 21.1 W and an efficiency increase of 1.7%.

Table 5.10 Hard-switching and soft-switching converter losses at 270-28 V, 200 kHz, 1.2 kW

Loss factors		Hard-switching Loss (W)	Soft-switching Loss (W)
Main transistors	Switching	39.2	0.6
	Conduction	18.4	17.4
Switched diodes D_a, D_b and D_0		10.7	11.1
Inductor L_{in}, L_a and L_b		16.1	16.1
PCB tracks		2.9	3
Auxiliary circuit components		NA	18
Total Loss (W)		89.4	68.3
Efficiency		92.6%	94.3%



(a) (b)

Fig. 5.27. Efficiency of hard-switching and soft-switching converter for operation at P_{in} = 300~1.2 kW with a duty ratio of (a) D = 0.17 and (b) D = 0.29

However, in the experimental measurement, the two converters exhibit a similar efficiency when operating at a duty ratio of 0.17 and 0.29 from 300 W~1.2 kW, shown in Fig. 5.27. A peak efficiency of 92.4% was recorded for the soft-switching converter at 1.2 kW for D = 0.17, representing a total loss of 91.2 W. A mismatch of 19.8 W is noticed compared to the estimated value. The underestimation of auxiliary inductor loss is considered to be the main mechanism. Also, the variations of the component datasheet parameters may also affect the consistency between the prediction and the experimental results.

The converter efficiency with D = 0.29 was seen to be higher than with D = 0.17 in both cases when operating above 900 W, which is mainly attributed to lower conduction losses. A peak efficiency of 93.9% was reported at 1.2 kW for the soft-switching converter.

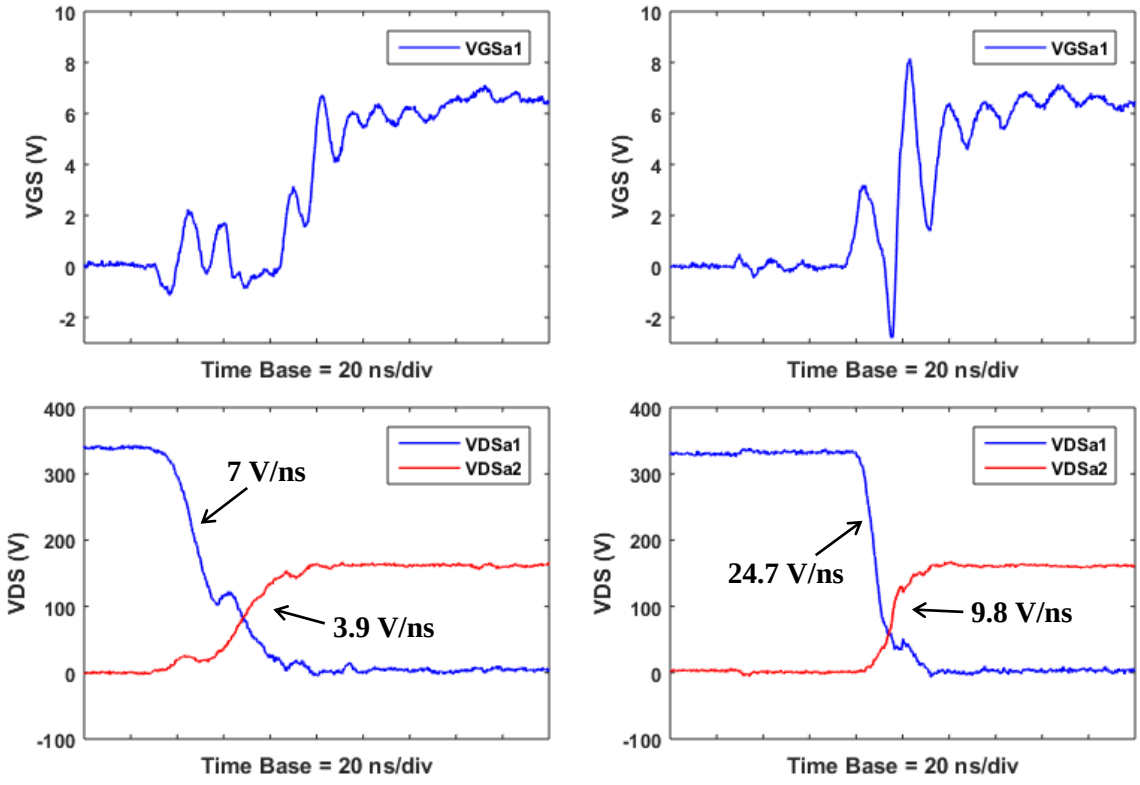


Fig. 5.28. Transistor gate and drain-to-source voltage when operating at 1.2 kW, 200 kHz, D = 0.17 for (a) soft-switching converter and (b) hard-switching converter

Due to the additional losses introduced by the auxiliary components, the soft-switching circuit does not show a distinct advantage over the hard-switching version for this design in terms of losses and efficiency. However, most of the switching losses in the transistors

have been removed, indicating the potential of further increasing the switching frequency and reducing the passive component size. In addition, it can be seen from Fig. 5.28 that the dv/dt of the transistor voltage during the switching transient has been reduced in the soft-switching converter, which suppresses the oscillations in the gate and is likely to improve the electromagnetic compatibility performance of the converter.

Moreover, the performance of the soft-switching converter may be more advantageous with different component selection. For example larger devices could be used for S_{a1}, S_{a2}, S_{b1} and S_{b2}, reducing the conduction loss, and the additional capacitance of the devices should not significantly affect the switching losses due to the soft-switching circuit. Furthermore, smaller devices with a lower capacitance could be used in the auxiliary circuit, reducing the switching losses. The increased on-state resistance of the devices is likely to have only a small penalty considering the small contribution of the auxiliary devices conduction loss, Table 5.8.

5.12 Summary

A soft-switching method was applied and demonstrated in the interleaved switched-capacitor buck converter at 300~1.2 kW 200 kHz with different duty ratios. An additional auxiliary branch consisting of three transistors, a diode and a resonant inductor was introduced to realize a lossless charging/discharging of the main device output capacitance. The operation of the soft-switching circuit was analysed in detail and examined in the simulation model based on LTSpice for nominal and heavy load conditions. Two resonant patterns were identified depending on the load conditions and circuit parameters. The simulation waveforms were compared with the experimental results for operation at 270-28 V, 200 kHz, 1.2 kW and showed a good consistency.

The overall size of the soft-switching converter remains unchanged as the size of auxiliary components is small and able to fit in a compact circuit layout. The efficiency of the soft-switching circuit was seen to be similar to the hard-switching circuit over a load range of 300~1.2 kW for a duty ratio of 0.17 and 0.29 due to the additional losses in the auxiliary circuit, which were considered to be dominated by the auxiliary inductor. An efficiency of 92.6% was recorded for operation at 200 kHz, 1.2 kW with a duty ratio of 0.17, which represents a loss of 91.2 W. The case temperatures of the main switching devices and diodes were measured to be lower than 40℃. The converter efficiency was improved to

93.9% at 200 kHz, 1.2 kW when operating with higher duty ratio such as 0.29, however the voltage stress in the transistors was also increased to around 400 V due to the higher switched capacitor voltage.

The soft-switching converter is considered to be superior to the hard-switching circuit as the losses in the main transistors were significantly reduced, allowing a potential increase in the switching frequency, and the dv/dt during the switching transient is well controlled, which results in a cleaner gate voltage in the main transistors. A better thermal management or a customized design for the auxiliary inductor is likely to improve the converter efficiency.

Chapter 6

Conclusions and Future Outlook

6.1 Introduction

In this chapter the key findings from this research are summarized and the contributions are highlighted. The future outlook and research opportunities building on the findings of this work are identified.

6.2 Key findings and research contributions

6.2.1 Switching characterization of GaN HEMTs

The switching characteristic of a GaN HEMT GS665016T 650 V/60 A from GaN Systems was evaluated using a DPT circuit. Three gate driving ICs were tested and the LM5114 from Texas Instruments was found to have the best performance due to the compact package, high output current and small pull-down resistance. A turn-on speed of 9.2 A/ns and a turn-off speed of 94.7 V/ns were achieved using 5 Ω and 2 Ω gate resistors respectively, resulting in a current overshoot of 32% during turn-on and a voltage overshoot of 45% during turn-off. The total switching loss under such conditions was demonstrated to be less than 150 μJ at 400 V, 40 A. The channel dissipation during turn-off was seen to be negligible with low currents and small gate resistors. The GaN Systems HEMT provided a switching loss reduction of around 90% compared to a similarly-rated super-junction Si MOSFET.

This part of work demonstrates the fast switching capability and the significance of driver selection and parasitic component optimization for GaN HEMTs. The ultra-low turn-off loss mechanism was identified and the switching loss reduction compared with the Si MOSFET was confirmed.

6.2.2 Dynamic on-state resistance characterization of GaN HEMTs

The dynamic on-state resistance of three GaN HEMTs from GaN Systems, Panasonic and Transphorm were measured under a variety of conditions using specially developed test

circuits. An increase of 20~30% in dynamic on-state resistance was observed for the two E-mode GaN devices within 3 μs of turn-on following an off-state stress voltage of 400 V for 50 μs. In contrast, the cascode GaN device from Transphorm exhibited a well suppressed dynamic on-state resistance of less than 6%. The dynamic on-state resistances of the three GaN devices were seen to be largely insensitive to elevated temperature but were affected by the switching energy. The dynamic on-state resistance of the GaN HEMT from GaN Systems increased with stress time, but the rate of increase became lower for stress times of 40~100 ms. During continuous operation, an increase of 50.4% in average on-state resistance of the GaN HEMT from GaN systems was observed when operating at 400 V, 10 A, 400 kHz and 0.5 duty ratio, which was aggravated by the use of a 50 Ω gate resistor, resulting in an increase of 73.2% in the average on-state resistance.

The main contributions of this work are:

- The limitations of the conventional DPT circuit for measuring dynamic on-state resistance were identified and a modified circuit was developed to undertake the tests. The effectiveness of the modified DPT circuit was confirmed and the measurement results were provided. Another modified test circuit was developed to evaluate the impact of stress time and switching energy during continuous operation on the dynamic on-state resistance in an initial-stress-free condition.

- Identification and measurement of the impact of stress voltage, stress time, junction temperature, switching energy on the dynamic on-resistance of commercial E-mode and cascode GaN HEMTs.

- Measurement of the dynamic on-resistance of the GaN Systems HEMT, GS66516T, in a continuously switching converter with different voltages, switching frequencies and switching speeds.

- A conference paper was published at IEEE APEC 2017 describing the measurement techniques and results. This was one of the first papers on the topic and many others have been published since.

6.2.3 GaN-based hard-switching interleaved switched-capacitor step-down converters

A hard-switching, interleaved, switched-capacitor, step-down converter topology realizing high-conversion-ratio was analysed in detail covering the idealised operation and the impact of parasitic device capacitance, and was demonstrated in a 270-28 V, 200 kHz and 1.2 kW prototype. The prototype used SiC diodes and top-cooled GaN HEMTs and a creative thermal design to ensure effective cooling of the devices whilst maintaining compact electrical connections. An overall size of $20\times10\times4.3$ cm^3 (0.86 Litre) and an efficiency of 92.6% for operation at 270-28 V, 200 kHz and 1.2 kW were achieved. The transistor switching loss accounted for 43.8% of the total loss and this was mainly due to the turn-on loss in the top transistors. A Si-based circuit using similarly rated devices was evaluated and compared with the original WBG-based converter, resulting in the efficiency falling from by 92.6% to 86.6% with the same switching frequency of 200 kHz. Alternatively, to maintain a similar efficiency, the switching frequency would need to be reduced to 100 kHz in which case the converter would be 30% larger.

The main contributions of this work are:

- The conventional switched-capacitor step-down converter was extended to a two-phase interleaved topology to reduce the passive components size and enable higher output current, multi-kW applications.

- The circuit operation during the switching transients was analysed and the parasitic capacitance was identified as a limiting factor, resulting in relatively high switching losses even when using wide bandgap devices.

- The interleaved, switched capacitor buck converter has been assessed practically at 1.2 kW, a much higher power than had been demonstrated previously for this type of circuit. The experimental work confirmed the switching loss predictions and provided a basis for quantifying the performance gain when using wide bandgap devices instead of silicon.

- To achieve compact and effective electrical and thermal connections, a multi-layer assembly concept was devised and demonstrated for the prototype.

6.2.4 GaN-based soft-switching interleaved switched-capacitor step-down converters

A soft-switching method was applied and demonstrated in the interleaved switched-capacitor buck converter at 300~1.2 kW 200 kHz with different duty ratios. The overall size of the soft-switching converter remained unchanged as the size of the auxiliary components was small and able to fit in a compact circuit layout. The efficiency of the soft-switching circuit was seen to be similar to the hard-switching circuit over a load range of 300~1.2 kW for a duty ratio of 0.17 and 0.29 due to the additional losses in the auxiliary circuit, which were considered to be dominated by the auxiliary inductor. An efficiency of 92.4% was recorded for operation at 200 kHz, 1.2 kW with a duty ratio of 0.17, which represented a loss of 91.2 W. The case temperatures of the main switching devices and diodes were measured to be lower than 40℃. The converter efficiency was improved to 93.9% at 200 kHz, 1.2 kW when operating with higher duty ratio such as 0.29, however the voltage stress on the transistors was also increased to around 400 V due to the higher switched capacitor voltage. The soft-switching converter was considered to be superior to the hard-switching circuit as most of the switching loss in the main transistors was removed, allowing a potential increase in the switching frequency, and the dv/dt during the switching transient was well controlled, resulting in a cleaner gate voltage in the main transistors, which is also likely to result in fewer EMI issues.

The main contributions of this work are:

- A soft-switching technique was proposed for the interleaved, switched capacitor buck converter that significantly reduces the switching losses and controls the dv/dt. Detailed circuit analysis was undertaken to provide a basis for design. The analysis was validated by simulation.

- The soft-switching converter was demonstrated and assessed practically, confirming the predicted operation and the reduction in switching losses. However, the losses in the auxiliary circuit limited the overall performance, but these losses could be reduced through optimised component selection.

6.3 Future outlook and research opportunities

6.3.1 Dynamic on-state resistance of GaN HEMT during continuous operation

Further research is needed to decouple the increase in on-state resistance due to self-heating and temperature rise from the dynamic on-state resistance of GaN HEMTs during continuous operation and to understand the cumulative trapping effect on dynamic on-resistance.

The conduction losses associated with the dynamic on-state resistance need to be understood in real converter applications at different operating conditions with an accurate loss breakdown taking into account the device DC resistance variation due to the self-heating.

6.3.2 Further tests on the hard-switching switched-capacitor step-down converter

The initial component selection for the GaN devices was relatively conservative considering the limited thermal capability of the devices and package. Only 30% of the GaN transistor current rating was eventually used. However, it has been observed that the circuit components in the hard-switching GaN-based switched-capacitor step-down converter remained at low temperatures of less than 40 ℃ for operation at 1.2 kW, 200 kHz, indicating that the converter has the potential to realize a higher power density and a better peak efficiency. Alternatively, the 650 V/30 A GaN HEMTs with a similar top-cooled package could be used to replace the 650 V/60 A devices to reduce the size of the PCB and the converter. This may also improve the overall converter efficiency since a better conduction-switching loss ratio can be achieved with the smaller device.

6.3.3 Optimisation of the soft-switching switched-capacitor step-down converter

The performance of the soft-switching switched-capacitor converter was largely limited by the auxiliary inductor. The behaviour of the auxiliary inductor needs to be fully understood especially the inductor losses associated with the pulsed operation and the high dv/dt. A customised design and a better thermal management are required to reduce the losses and control the temperature rise in the auxiliary inductor, so that a higher power density and a better efficiency can be realized for the soft-switching switched-capacitor buck converter.

6.3.4 Advanced control for interleaved switched-capacitor step-down converters

The hard-switching and soft-switching prototypes used an open-loop control implemented on a UCD3138 DSP. The output inductor currents between the two interleaved phases may become unbalanced with the increase of power level. A closed-loop control to balance the phase currents such as the peak current control may be required for the converters for operation at higher power. Furthermore, an advanced control strategy may also be required for maintaining the voltage balance between the two switched capacitors for operation at higher powers.

6.3.5 Embedded design for GaN-based switched-capacitor step-down converters

An integrated converter assembly could be produced by embedding components within the substrates to enable a low profile layout and superior electrical and thermal performance. As the switched diodes are included in the current commutation path for switched-capacitor converters, 3D embedding of the transistors and diodes would be very beneficial for reducing the power loop parasitic inductance. By integrating the driver ICs with the transistors, the gate loop stray inductance would also be significantly reduced and the switching speed of the GaN transistors could be further increased to improve the converter efficiency. In addition, a much better thermal path could be realized for the switched diodes by sintering the diode dies on a high-thermal-conductivity substrate.

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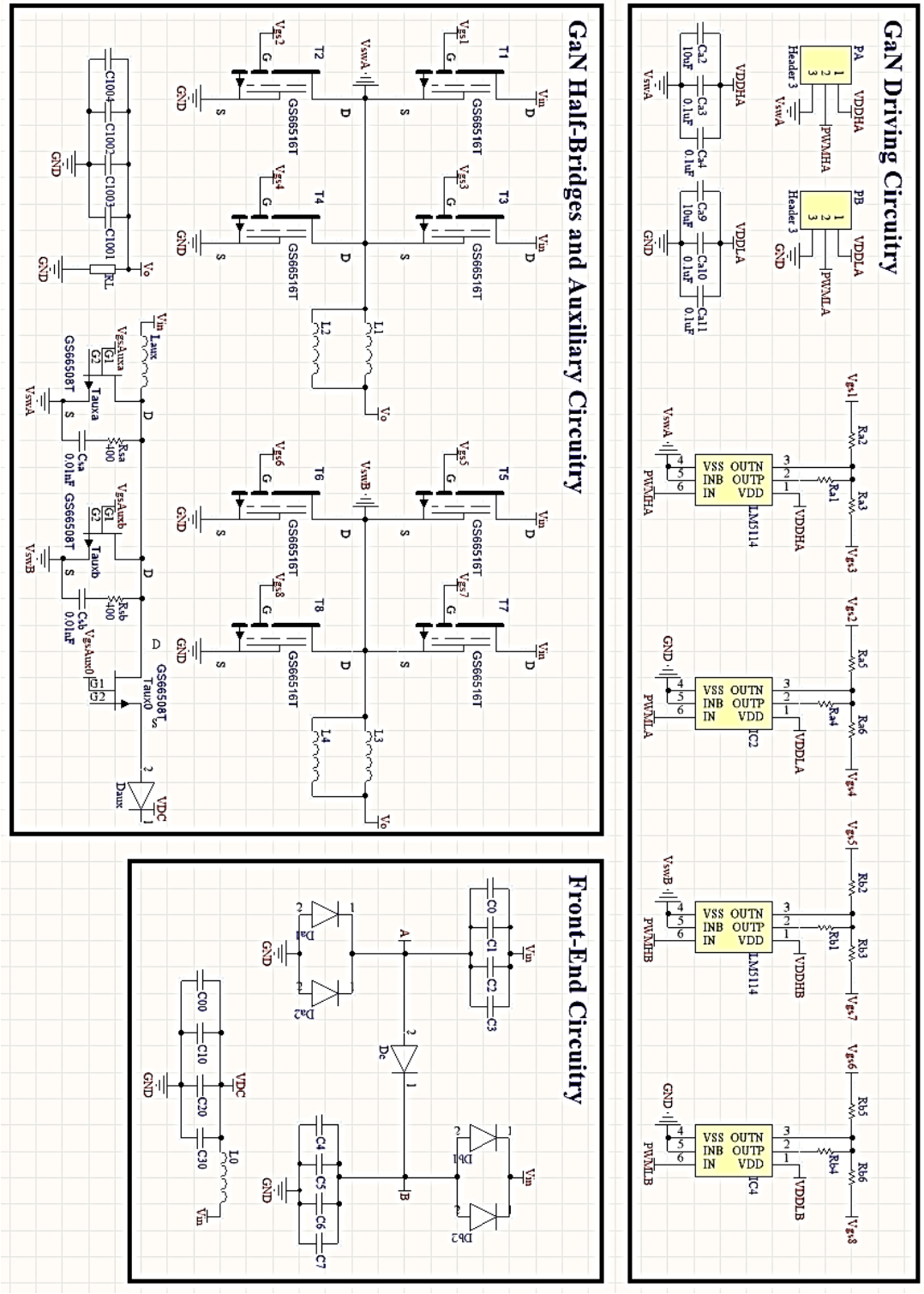
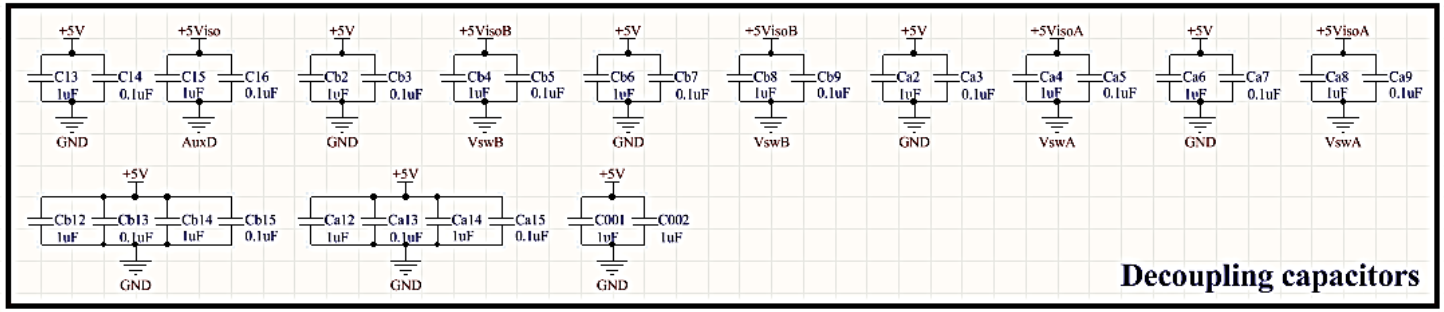
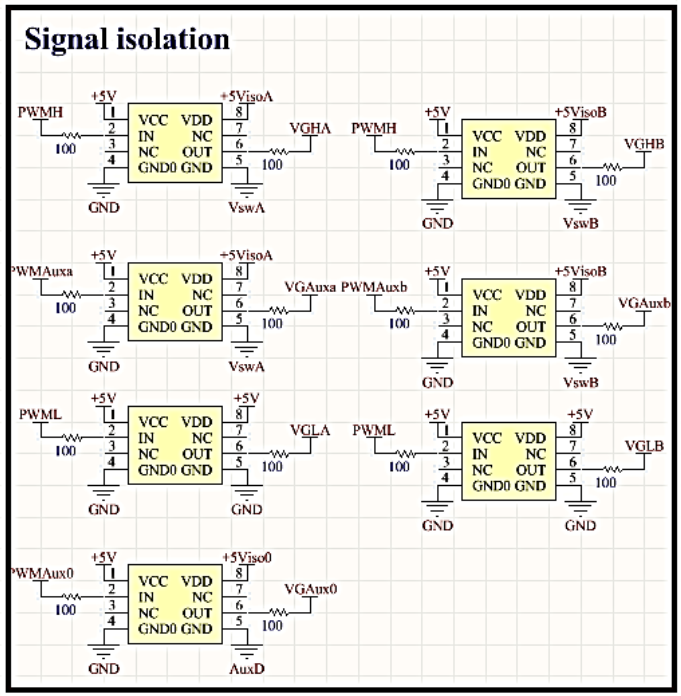
Appendix A. Soft-switching switched-capacitor step-down converter circuit schematics




+5V
+5Viso
+5VisoB
+5VisoA
C13 1uF
C14 0.1uF
C15 1uF
C16 0.1uF
Cb2 1uF
Cb3 0.1uF
Cb4 1uF
Cb5 0.1uF
Cb6 1uF
Cb7 0.1uF
Cb8 1uF
Cb9 0.1uF
Ca2 1uF
Ca3 0.1uF
Ca4 1uF
Ca5 0.1uF
Ca6 1uF
Ca7 0.1uF
Ca8 1uF
Ca9 0.1uF
Cb12 1uF
Cb13 0.1uF
Cb14 1uF
Cb15 0.1uF
Ca12 1uF
Ca13 0.1uF
Ca14 1uF
Ca15 0.1uF
C001 1uF
C002 1uF
GND
AuxD
VswB
VswA
Decoupling capacitors


Signal isolation
PWMH
PWML
PWMAuxa
PWMAuxb
PWMAux0
VGHA
VGHB
VGLA
VGLB
VGAuxa
VGAuxb
VGAux0
100
VCC VDD
IN NC
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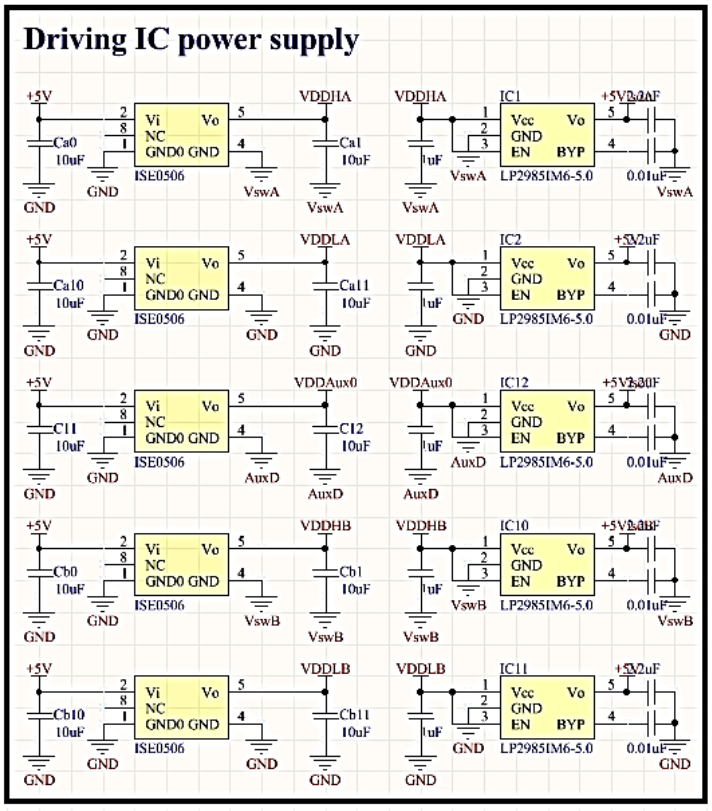
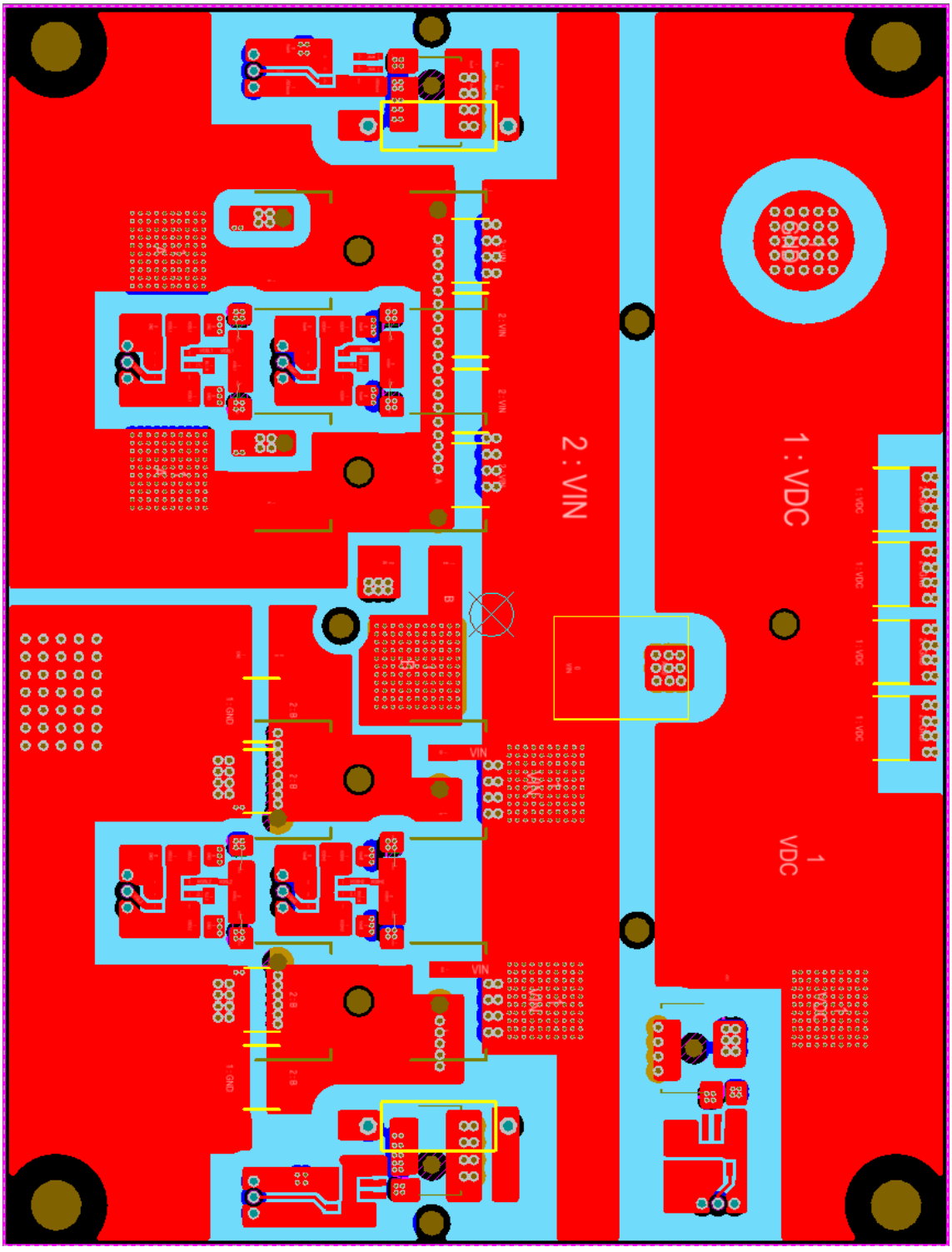
+5ViosoA
+5ViosoB
+5Viso0
GND
VswA
VswB
AuxD

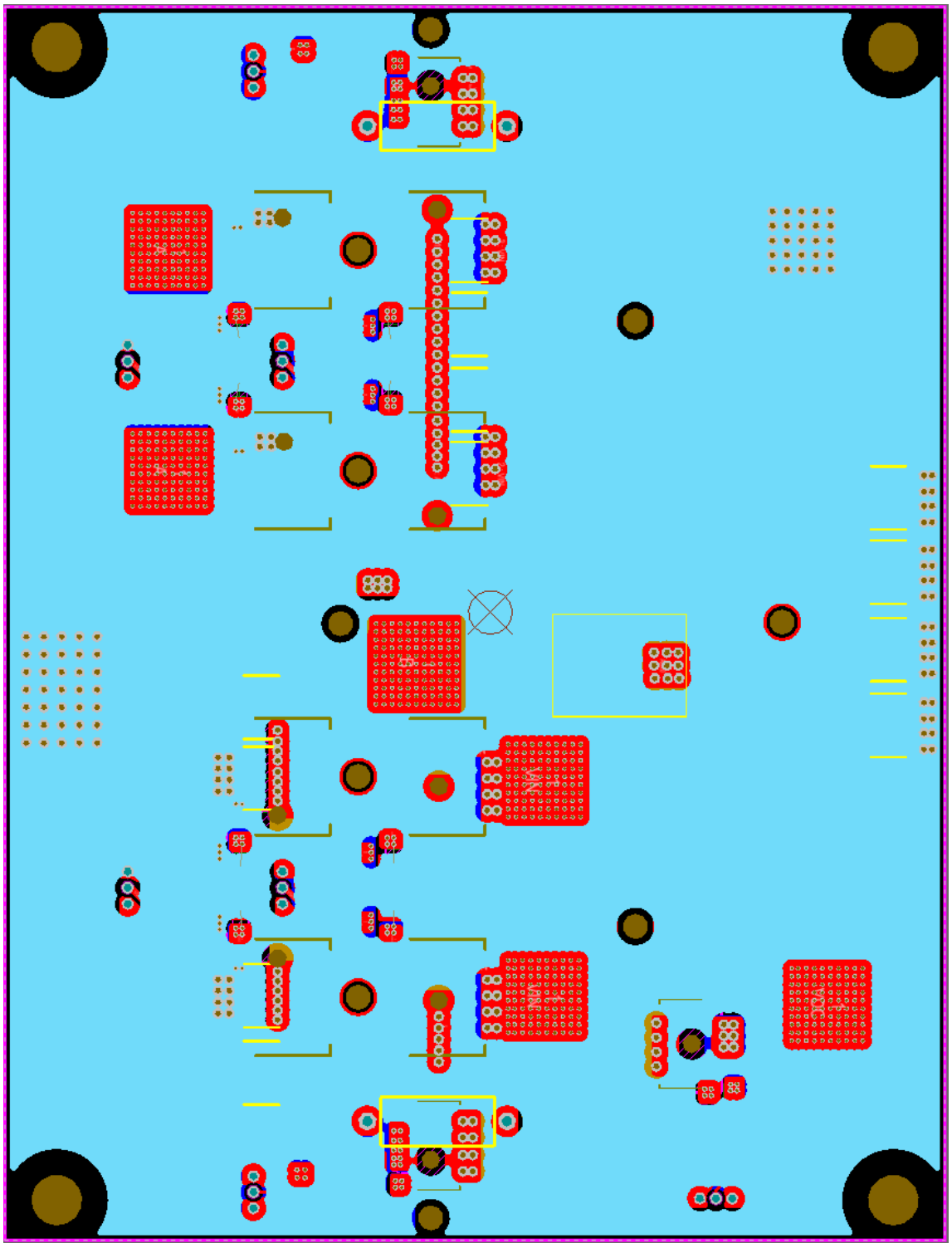

Driving IC power supply
+5V
Ca0 10uF
Ca1 10uF
Ca10 10uF
Ca11 10uF
C11 10uF
C12 10uF
Cb0 10uF
Cb1 10uF
Cb10 10uF
Cb11 10uF
Vi Vo
NC
GND0 GND
ISE0506
VDDHA
VDDLA
VDDAux0
VDDHB
VDDLB
IC1
IC2
IC12
IC10
IC11
Vcc Vo
GND
EN BYP
LP2985IM6-5.0
1uF
0.01uF
2uF
GND
VswA
VswB
AuxD

Appendix B. Soft-switching switched-capacitor step-down converter PCB layout

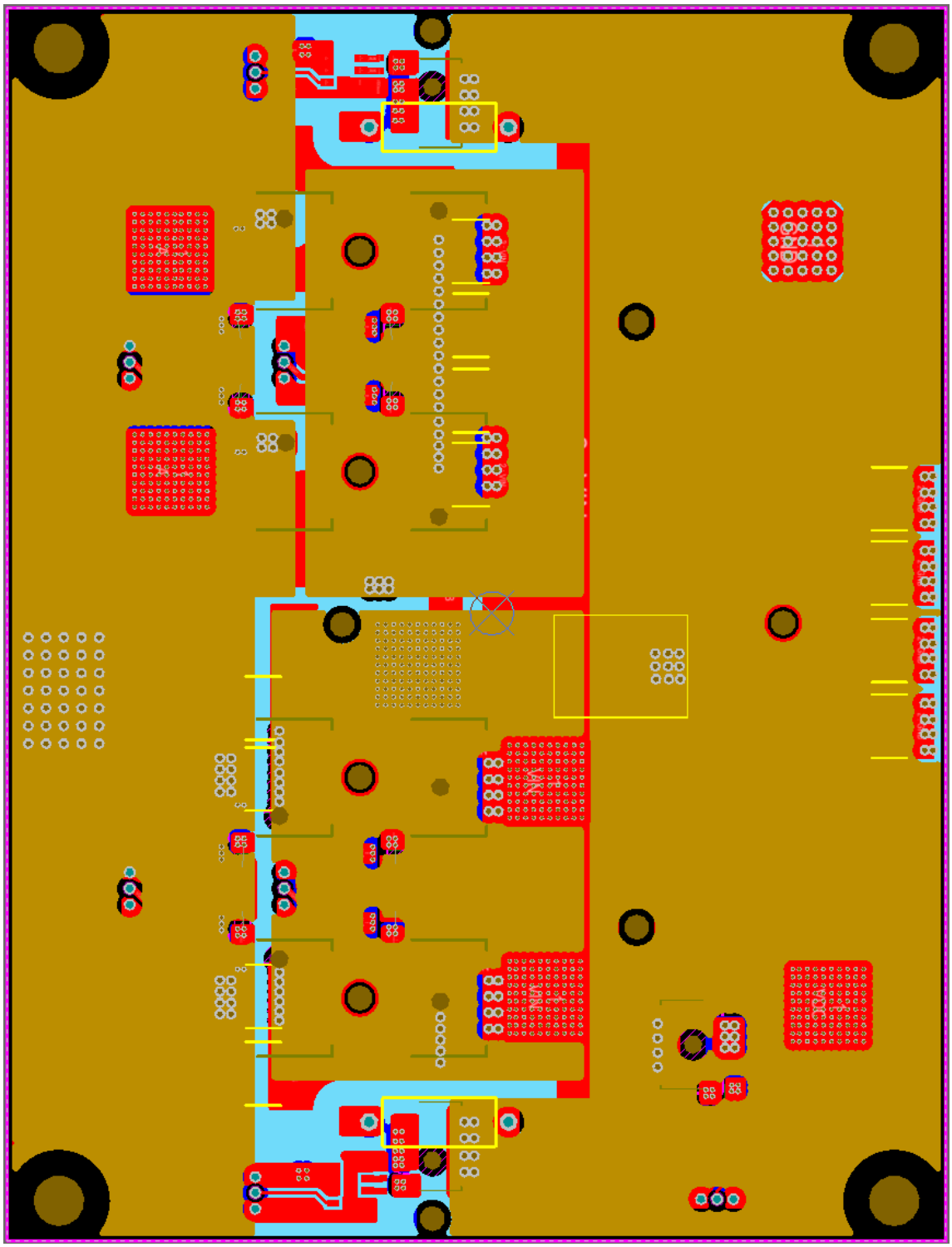
Main switching circuit top Layer



Main switching circuit mid Layer 1



Main switching circuit mid Layer 1



Main switching circuit bottom layer