2020

Bibliometric Review of NoC Router Optimization

Priti Shahane
pritis@sitpune.edu.in

Jayshree Pande
jayshree.pande@sitpune.edu.in

Bibliometric Review of NoC Router Optimization

Priti Shahane[1], Jayshree Pande [2]

[1]Assistant Professor, Department of Electronics and Telecommunications, Symbiosis Institute of Technology, Affiliated to Symbiosis International (Deemed University), Pune, India

Email: pritis@sitpune.edu.in

[1]Assistant Professor, Department of Electronics and Telecommunications, Symbiosis Institute of Technology, Affiliated to Symbiosis International (Deemed University), Pune, India

Email: jayshree.pande@sitpune.edu.in

ABSTRACT

Network on chip (NoC) has been proposed as an emerging solution for scalability and performance demands of next generation System on Chip (SoC). NoC provides a solution for the bus based interconnection issue of SoC, where large numbers of Intellectual Property modules (IP) are integrated on a single chip for better performance. The NoC has several advantages such as scalability, low latency and low power consumption, high bandwidth over dedicated wires and buses. Interconnections between multiple chip cores have a significant impact on the communication and performance of the chip design in terms of region, latency, throughput and power. In the NoC architecture, the router is a dominant component that significantly affects the performance of the NoC. NoC router architectures evolved since the year 2002 and progress in the domain pertaining to the optimization in the NoC router architectures has been discussed. The key objective of this bibliometric review is to understand the extent of the existing literature in the domain of performance efficient NoC router architectures. The bibliometric analysis is primarily based on data extracted from Scopus. It reveals that major contributions are done by researchers from USA, China followed by India in the form of conference, journals and articles publications. The major contribution is by the subject areas of Computer Science and Engineering followed by Mathematics and Material Science. The geographical analysis is done by using the GPS visualize tool. The clusters were created using Gephi.

Keywords: Network on chip, System on chip, Bus interconnection, Router, Buffers, NoC performance parameters

1. INTRODUCTION

The advancement of integration technology and technology scaling has led to the advent of the System on Chip (SoC) architecture. The SoC comprises a variety of heterogeneous Intellectual Property (IP) modules on a single chip. The benefit of the SoC is its smaller size, higher speed, low power consumption, high reliability and cost-effectiveness. There are, however, several challenges to the evolution of the SoC. The SoC architecture is confronted with the problem of interconnection between different IP modules, which restricts the scalability of the device. As the number of IP modules in SoC increases, it becomes difficult to meet performance parameters such as the bandwidth, latency and power consumption defined by bus-based interconnection. Effective communication between the various IP modules in the SoC is therefore a research challenge. (Kumar S. et al.2002, Agarwal A.et al. 2009, Benini, L., and De Micheli, G. 2002).

Traditional bus based designs are not able to handle demanding communication requirements of large SoCs. The disadvantages of traditional bus architectures include long data delay, low bandwidth due to scalability issues and high power consumption. Thus the usage of bus architecture is limited to smaller numbers of IP modules. In order to meet the communication requirements of large scale SoCs, there is a great need to find a new design alternative to overcome the interconnection problem of conventional bus based architectures. Network on chip (NoC) is a solution for such a communication bottleneck. NoC, an embedded switching network is used to interconnect different IP modules in SoC. The NoC provides solution for salability issue of SoC architecture for large design. Routers, link and network interface are the three main parts of NoC. The router is the heart of NoC as it coordinates data packet traversal based on the routing strategy. The network interface or network adaptor provides the bridge between the router and the devices attached to it. It performs two operations such as protocol conversion and data packet formation as per the switching techniques. The link provides a channel for transmission of data between the various devices of the network. In NoC architecture, the router is a dominant component that significantly impacts the performance of NoC (Bjerregaard, T., and Mahadevan, S.2006, Marculescu et al., 2007)

The architecture of the router consists of the input port, scheduler, crossbar switch, and output port. The design of the router is greatly impacted by buffer management, topology used for connecting different IP modules and the scheduling algorithm. These router architecture parameters affect the performance of router design in terms of power, area and latency. Therefore effective router design plays a pivotal role in keeping the communication backbone efficient in SoC architecture.

1.1 Generic NoC router architecture

This section presents traditional router architecture for NoC. It consists of an input port with a virtual channel (VC), a VC allocator, a routing computational unit, a crossbar and an output port. The architecture of the router for a specific NoC is unique depending on the architecture of input

ports, implemented routing algorithm and the switching method and the implemented quality of service. The general router architecture is shown in figure 1 and the functionality of the components are described in the following section (Shahane, P. M., and Pisharoty, N. 2016).

a) **Buffers/ Virtual channels:** The input and output channels consist of buffers that store messages in transit. Most of the routers support five port architecture in which data can be transmitted in 4 directions and one port is dedicated to a processing unit/core. Buffers increase the total available bandwidth in the network. Some on-chip routers use a single first-in-first-out (FIFO) buffer. But a single buffer gives rise to the head-of-line blocking (HoL) problem. HoL blocking occurs for each input node when there is a single FIFO input queue and the packet in the head of queue is stalled from being forwarded to the corresponding output node due to output port congestion. This restricts the use of the output channel. The Virtual Channel is the solution to the HoL blocking. Virtual channel flow control consists of an array of parallel buffers for each input port. In this technique, there are several buffers per physical channel and as a result, if any packet is blocked then other packets that belong to other output ports can pass the blocked data packets. Due to this, the throughput of the network improves and the average packet latency reduces by overcoming the HoL problem. But adding buffers in the virtual channel can significantly increase logic area overhead and power dissipation. Hence, there is a need for efficient use of buffers in the router design.

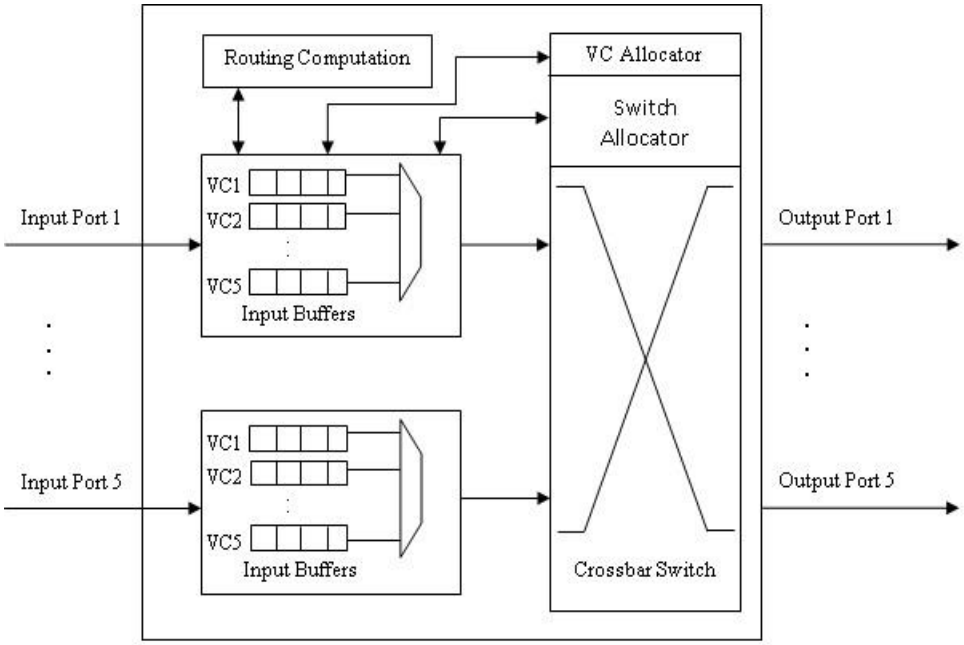

Figure 1: Generic typical NoC router architecture

b) **Routing computation:** A routing computation unit is required to compute the routing of the incoming packets. This stage determines the destination output port to which data packet has to be assigned.VC allocation is necessary since several header flits require to send packets to the same VC in the output port. There are two different implementation methods for routing computation. These methods are lookup table based routing and finite state machine based routing.

c) **Arbiter:** An arbiter is used to select a packet from a certain incoming port to be delivered to its requested output port. The arbiter plays a vital role in controlling data packet contention when various input ports require the same output port. There are several methods to implement the arbiter such as fixed priority arbiter, round robin arbiter, first come first serve arbiter and programmable priority arbiter.

d) **Crossbar:** The crossbar switch interconnects the input port data to the output port. The structure of a crossbar comprises of an array of multiplexers. The data to be sent to the output port depends on the select lines. The arbiter generates a select line depending on the request signal.

The performance of NoC is strongly dependent on the design choices of the NoC router as the router is the heart of the NoC system. The efficiency of the design of the router is measured in terms of router area, power efficiency and latency.

1.2 Evolution of NoC router architecture

A packet based data transmission concept was proposed by Willam Dally and Brain Towels in 1999 (Dally W. and Towles B. 2001). They emphasized on routing of data in packets instead of the routing of wires. The NoC is a promising approach to handle communication problems in SoC architecture by replacing buses and wires with packet routing. The concept of NoC facilitates modular design structures by providing a standard interface between the different modules. Thus NoC design methodology improves the overall performance and bandwidth of the system.

The NoC paradigm has been gaining momentum since its introduction in early 2000 due to the possibility of scaling with the network size. In 2002, Luca Bennini and De Michali introduced the NoC paradigm. A lot of research work is going on to replace off-chip interconnect with on-chip interconnect as the bus based system has failed to provide efficient communication for large networks. Therefore, Network on chip is an emerging paradigm for communication within large systems implemented on a single silicon chip. The SoC architectures utilize heterogeneous IP modules from a variety of vendors with standard interfaces, and these IP modules can communicate with the help of an on-chip network in a plug-and-play fashion.

The general router architecture as explained in the above consists of an input ports with buffers and virtual channels (VC), a VC allocator, a routing computational unit, a crossbar switch and an output port. The NoC router architecture is specified by its topology, routing algorithm and flow

control. Network topology specifies the static arrangement of routing nodes and links in an interconnection network. Exemplary topologies are Mesh, Torus, Fat tree, Spindergon, etc. The routing algorithm defines how messages between nodes traverse the network. The routing algorithm may be deterministic or adaptive. A good routing algorithm will balance the traffic load across the network and should avoid deadlock and livelock. Flow control is the allocation of communication resources for the guaranteed and reliable transmission of data packets between the nodes. (Dally W. and Towles B. 2004). The NoCs are generally evaluated with respect to their performance parameters such as throughput, latency, area, energy consumption and operating frequency (Banerjee et al., 2009).

Most of the router designs use buffers to store data packets or flits before transmitting them within the network (Taylor et al., 2004; Hoskote et al., 2007; Cai et al., 2015). Buffers are needed to control the flow of messages traversing in the network. It also reduces network contention and decrease latency. In the case of a contention situation, one of the data packets will proceed to the destination and the other data packet will be stored in the buffer to be transmitted later (Moscibroda et al., 2009). Dally et al. (2004) suggested the use of virtual channels rather than a single first-in-first-out (FIFO) input buffer to avoid the head of line (HoL) problem. HoL blocking limits the output channel utilization. To overcome this, it is suggested to use separate virtual channels as the number of output ports at the input which also increases the throughput of the network.

Although VC buffers increase performance in terms of improved bandwidth efficiency, they consume considerable power and on-chip area (Borkar et al.,2007; Jafri et al., 2010). Buffers in the router consume static power when buffers are empty. It also consumes dynamic power during reading/write operation. Second, buffers consume more chip network area and also increase design complexity due to buffer allocation and de-allocation of flits.

Gratz et al. (2006) implemented the TRIPS prototype router with wormhole routing for a 4x10, 2D mesh network with four virtual channels. The input buffers of routers occupied 75% of the total on-chip network area. Also, the NoC router consumes a substantial amount of power in MIT RAW chip ~ 40% (Taylor et al., 2004), and in the Intel 80-core Terascale chip ~30% (Hoskote et al., 2007). Additionally, F. Martini et al. (2007) proved that the frequency of the NoC router can be increased by reducing buffer size. They introduced one flit latches instead of buffers in the router. It was observed that switching frequency increased from 1GHz up to more than 2GHz due to reduction in the data path delay of the control logic of buffers. It helped to reduce critical path delay and increase the operating frequency of the router.

To improve the area, energy efficiency and operating frequency of the NoC router, there is a need for bufferless routers (Gratz et al., 2006). The best examples of bufferless routers are Bufferless Router(BLESS)and Cheap Interconnect Partially Permuting Router (CHPPER) (Fallin et al.,2011). Yu Cai et al. (2015) have shown that bufferless routing saves up to 30% of power consumption and results in a 38% reduction in the area of Mesh or Torus topology compared to

buffer architecture. CHIPPER NoC implementation reveals that, relative to buffered routing, it decreases the average network power by 54 % and the area by 36.2 % for 8X8 mesh topology (Fallin et al., 2015). The main concept for bufferless routing is to eliminate input buffers and use data packet deflection to overcome contention in the network. With low network traffic, the bufferless router provides efficient performance by minimizing area and power consumption. However, at high network usage, there is a possibility of high contention which deflects data packets due to unavailability of the destination port. This unwanted hopping increases dynamic energy consumption as well as network latency. The solution for bufferless deflection routing at high network load is provided by Minimally buffered deflection routing (MinBD) (Fallin et al., 2012). MinBD NoC router design efficiently combines both buffered and bufferless paradigms. MinBD router uses deflection routing with minimal buffering. It also requires less area due to a smaller buffer area which can be used only in case of contention. Thus a MinBD router becomes a good choice for the input block of the router.

NOC's buffered and bufferless structure and their design methodologies are studied in detail by the author Sujata et al., 2020. This paper discussed commonly used architectures with design challenges for optimization of NoC parameters. Also, in this paper modified routing called dynamically buffered and bufferless reconfigurable NoC (DB2R-NoC's) are implemented and validate for multimedia data on FPGA processors.

The scheduler is another aspect of router design. The scheduler plays an imperative role in the communication of data packets in the NoC. In the router, the scheduling algorithm decides the data packet transfer from input devices to output devices. The scheduler allows access to the crossbar switch depending on the priority of the node based on the scheduling algorithm, which ensures fair service to all the input devices. The key function of any scheduler is to resolve the contention free requests for the same destination (Rantala et al., 2006). Since the speed of transfer of data packets in the router depends on the scheduler, the efficient design of the scheduler is of vital importance.

A lot of research work has been done on fast scheduling algorithms for crossbar switches (McKeown et al.,1999; Belhajali et al.,2013; Saravanakumar et al.,2012;Ruma et al., 2013). Various schedulers are fixed priority, Round Robin Arbiter(RRA) and Iterative Serial Line in Protocol (iSLIP) scheduler. The problem of starvation is very critical in the fixed priority scheduler, as only one input port has the highest priority, while all other ports have a low priority access to the output port. It offers an unfair arbitration technique due to the predetermined priority of ports. Low priority nodes can face high latency problems. RRA allows each requester to be assigned the highest priority in turn. The priority of each requester is rotated in a cyclic order. It is based on the principle that a request that has just been submitted by any node should have the lowest priority in the next round of arbitration. This provides an accurate estimate of the worst-case waiting period for ports to be requested. The maximum waiting time for any requester is equal to the number of requesters minus one. RRA has a high level of fairness as each input

port has an equal chance of accessing the output port and the issue of starvation can be overcome.

The other important factor that impacts the interconnection mechanisms of NoC in terms of cost and performance is the implementation medium for NoC. Application Specific Integrated Circuits (ASICs) are gradually being replaced by Field Programmable Gate Arrays (FPGA) in many contemporary applications due to high cost and longer design cycles. Modern FPGAs are also growing with the increase in chip density. It provides support for various software and/or hardware blocks embedded within them, such as memory blocks, DSP slices, a large number of I/O ports and even soft and hard processors. These hardware blocks, along with customizable logic blocks, make FPGA the perfect platform for NoC designs. Although ASICs have better performance characteristics in terms of speed, area and power, FPGAs replace ASIC mainly because of their flexibility and quick time to market. Also, the wire delay of ASIC is more than the gate delay of FPGA. Therefore implementation of SoC design by exploiting the advantages of NoC in FPGAs is becoming an active area of research where the challenge is to implement a design within the limits of available FPGA resources. Therefore, the design of an FPGA based generic light-weight router becomes imperative where the area can be traded-off for performance to meet applications requirements (Gemal et al., 2016, Brugge M. and Khalid M.2014.,Salaheldin et al.2015,Papamichael et al.2012,Gindin et al.2007). Various FPGA platforms such as Virtex, Spartan and Altera families are available for implementation of NoC. FPGAs serve as an excellent platform for rapid prototyping for SoC. Therefore performance efficient design of NoC router on FPGA is becoming an emerging research area.

2. PRELIMINARY COLLECTION OF DATA

The preliminary data was collected from Scopus. The University library portals provide access to the databases like Web of Science and Scopus, Clarivate, Science Direct and many more. The preliminary collection was done on the 9th of November 2020 from the Scopus database as it is the most popular and largest databases among the available peer reviewed databases. The keywords used are provided in the next section.

2.1 Keywords used

The top twenty keywords related to the study are listed in table no.1. The most important keywords used were “NoC Router Optimization” for carrying out the search. Other related keywords and the number of publications are listed in table 1.

Table 1: Keywords and number of publications

Keywords	Number of Publications
Routers	221
Network-on-chip	146
Servers	107
VLSI Circuits	107
Optimization	83
Network On Chip	70
Network Architecture	68
Distributed Computer Systems	51
Integrated Circuit Design	51
Microprocessor Chips	51
Computer Architecture	42
Programmable Logic Controllers	40
Mapping	38
Topology	34
Energy Utilization	33
Network-on-chip(NoC)	33
System-on-chip	33
Design	32
Energy Efficiency	28
NoC Design	28

Source: http://www.scopus.com (accessed on 9th November 2020)

The study is restricted to English language. The search reveals that there are 249 English publications based on this topic.

Table :. Trends in publishing language

Publication Language	Number of Publications
English	249
Chinese	3

Source: http://www.scopus.com (accessed on 9th November 2020)

Table 3: Type of publication

Type	Number of Publications	Percentage from 252
Conference Proceeding	115	45.63%
Journal	109	43.25%
Book Series	26	10.31%
Book	2	0.007%

Source: http://www.scopus.com (accessed on 9th November 2020)

Researchers working in this domain have published 45.63% papers in conference proceedings, 43.25% in journals, 10.31% in book series and 0.007% books as depicted in table 3.

2.2 Preliminary data highlights

In this study 252 publications were extracted using keywords. The preliminary investigation is based on the Scopus database only. Different types of documents like conference proceedings, journal papers, books series and books spanned from the period ranging from 2002 to 2020 for the domain of NOC router. Per year publication count is given in table 4 for the last ten years and the publication per year analysis is depicted in figure 2.

Table 4: Number of publications per year

Year	Number of publications
2020	7
2019	24
2018	18
2017	32
2016	20
2015	20
2014	21
2013	23
2012	25
2011	35
2010	27

Source: http://www.scopus.com (accessed on 9th November 2020)

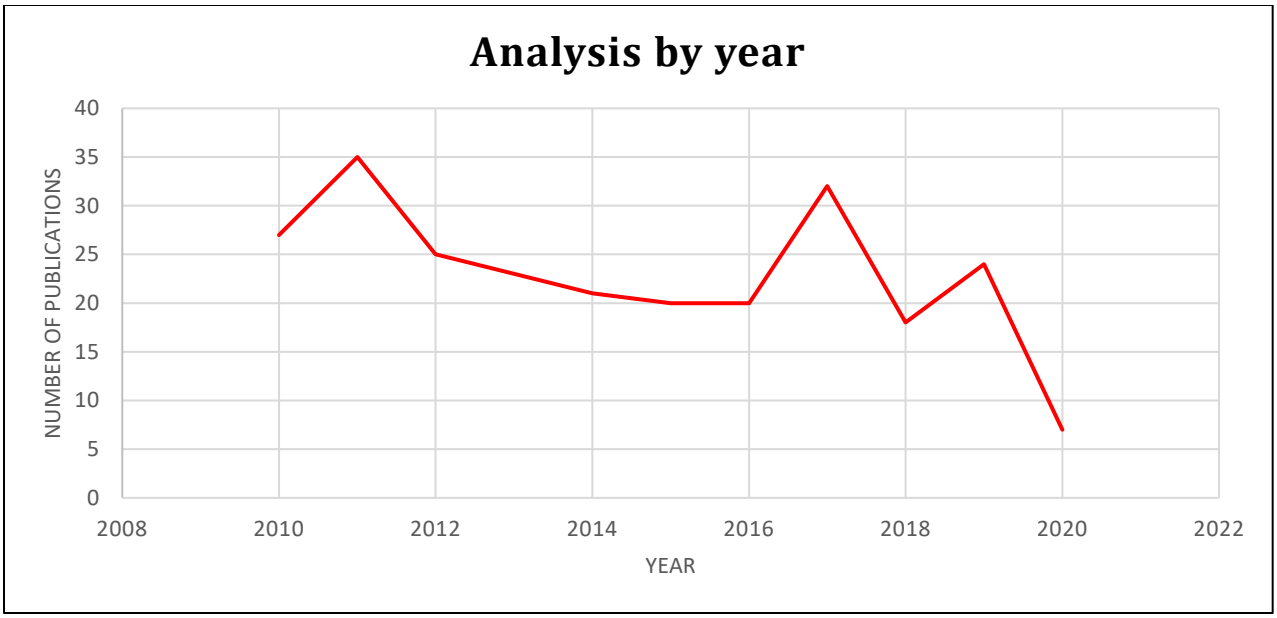

Figure 2: Publication trend per year

Source: http://www.scopus.com (accessed on 9th November 2020)

2.3 Investigations on data

The bibliometric survey shows the type of literature available in this research area making use of the geographical distribution and how the different authors from several geographical locations have contributed by publishing and their affiliation statistics.

3. BIBLIOMETRIC ANALYSIS

Two different ways were used to do the bibliometric analysis

- Geographical location analysis
- Statistical analysis using affiliations, document type, author statistics and analysis of the citations for the documents.

3.1 Analysis by geographical location

The analysis based on geographical locations for the research work done in the area of NOC router optimization is shown in figure 3. This figure has been drawn using GPS visualizer tool from gpsvisualizer.com. Maximum numbers of publications are from the countries like USA, China and India followed by Brazil, Germany, Iran and Sweden.

Figure 3: Geographical locations for study of NoC router optimization

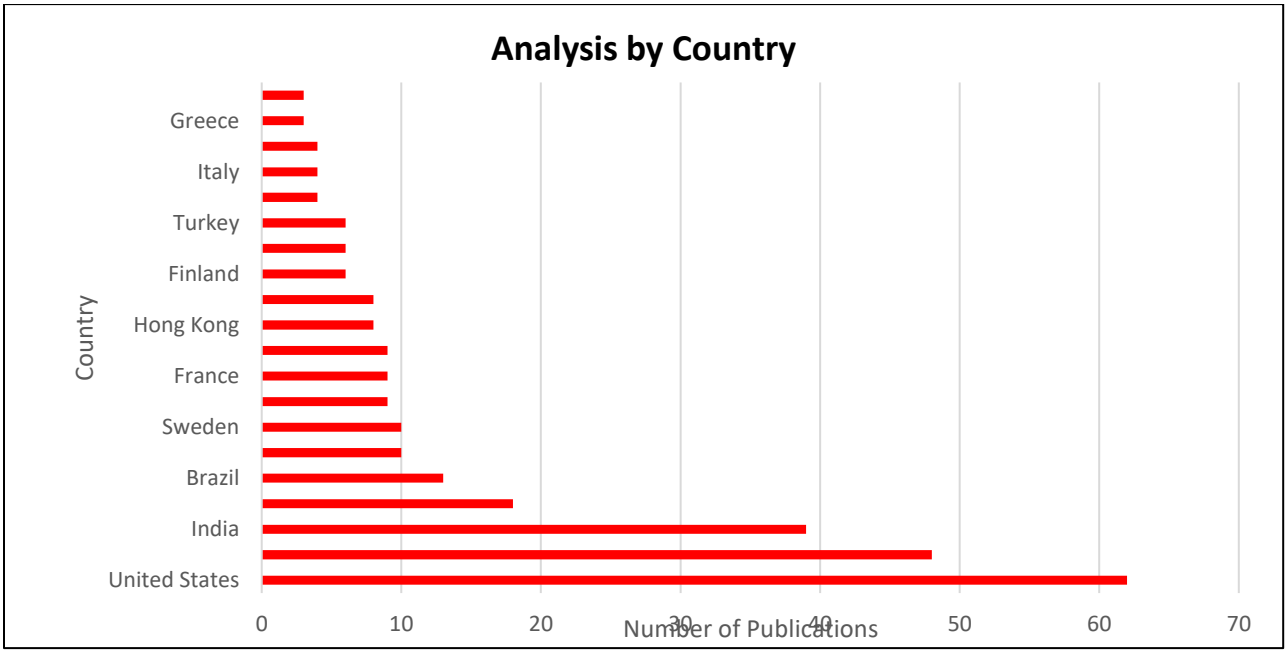

Figure 4: Analysis by country

Source: http://www.scopus.com (accessed on 9th November 2020)

3.2 Analysis based upon subject area

The analysis based on the subject area is depicted in figure 5. It is observed from the analysis that most of the research work done is from the area of Computer Science, Engineering followed by Mathematics. The number of publications from the areas of Energy, Material science and Earth and Planetary Science are comparatively less in the field of NoC router architecture.

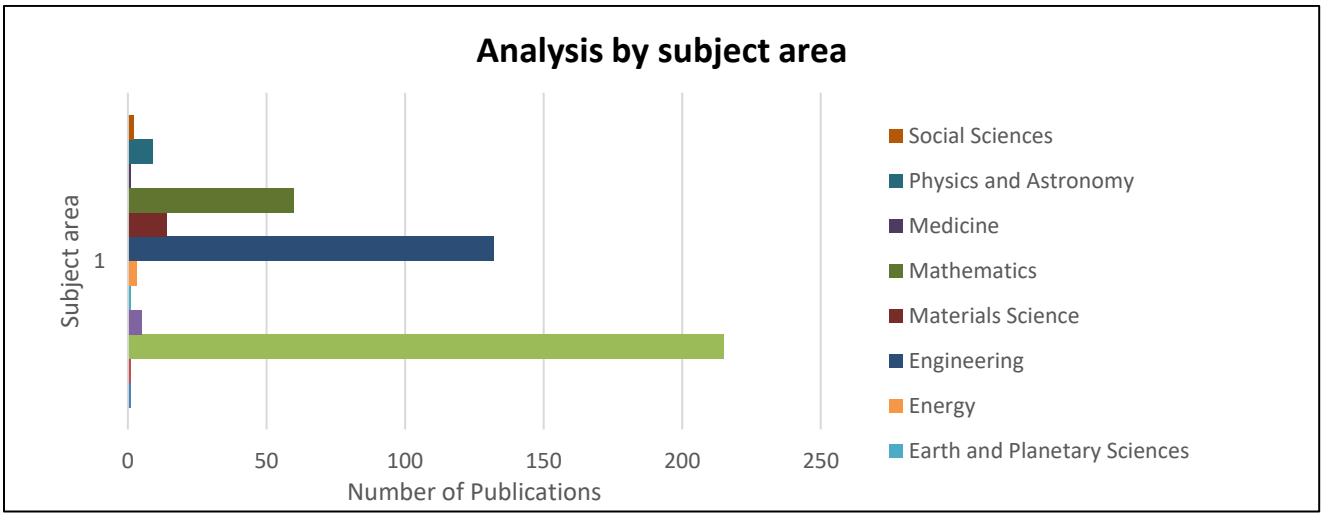

Figure 5: Analysis by subject area

Source: http://www.scopus.com (accessed on 9th November 2020)

3.3 Analysis based upon affiliations

Several Universities all over the world have significantly contributed in the research work in the domain of NoC router architecture optimization as shown in figure 6. This research area is dominated by Universities of USA and India. Top twenty affiliations are shown in figure 6.

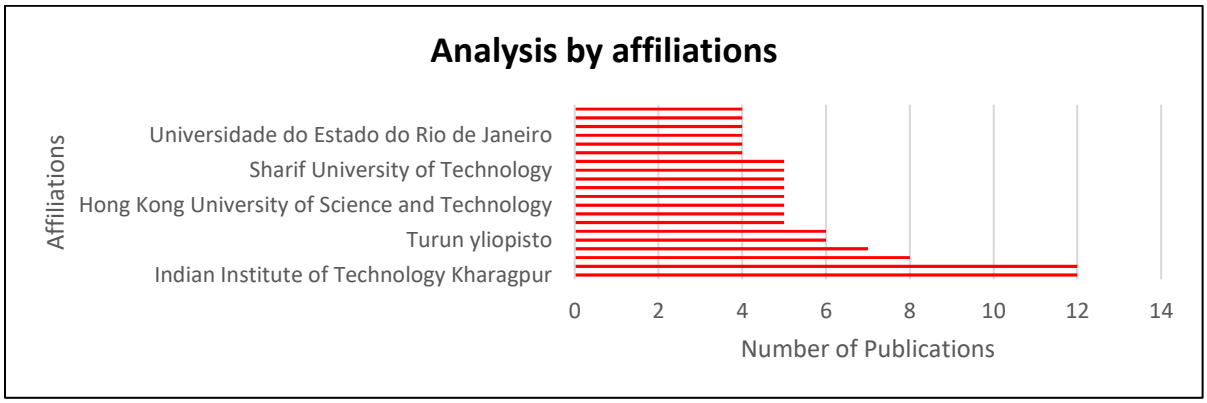

Figure 6: Analysis by affiliations

Source: http://www.scopus.com (accessed on 9th November 2020)

3.4 Analysis based on the authors and number of publications

Key researchers in the area of NoC Router and Optimization are shown in figure 7. Top ten authors contributing in this area are shown.

Figure 7: Key researchers in the area of NoC router optimization

Source: http://www.scopus.com (accessed on 9th November 2020)

3.5 Analysis based upon document type

Analysis based on document type is shown in figure 8. From the figure it is clear that from the publications 46% are conference proceedings, 43% are journal papers, and 10% are book series and remaining 1 % are books.

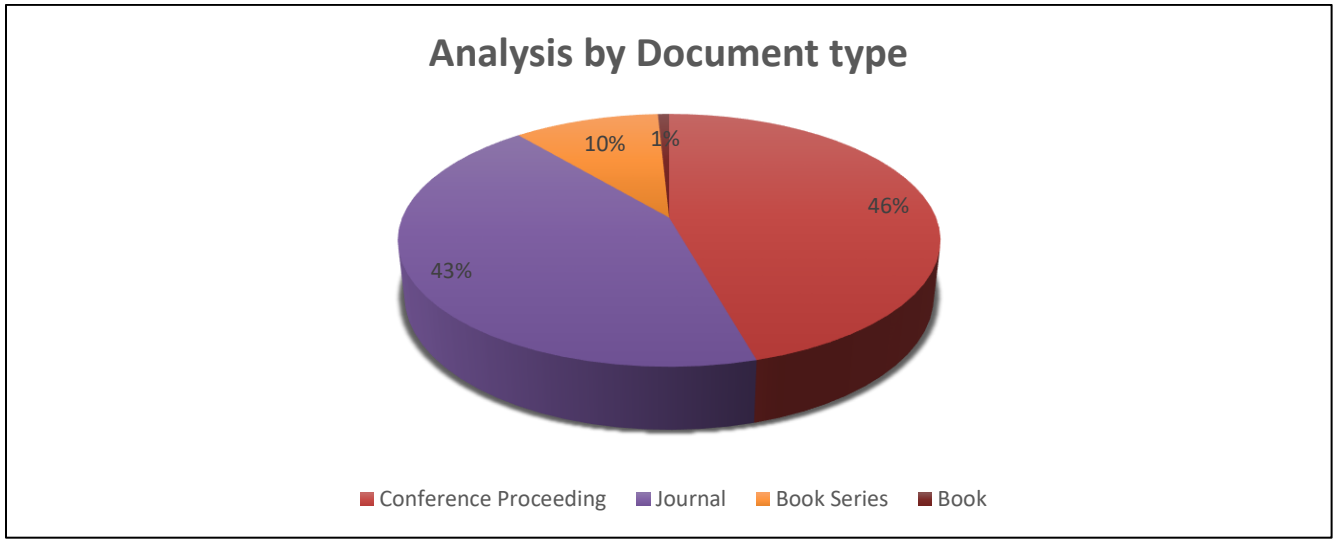

Figure 8: Analysis based on document type

Source: http://www.scopus.com (accessed on 9th November 2020)

3.6 Analysis using clusters

In this study to depict the relation between various statistical parameters clusters are used. The tool Gephi is used for this purpose which is an open source platform for making clusters. Affiliation, Keywords, Authors, source type are represented by edges and nodes in the clusters and their interrelation is depicted in figure 9, figure 10 and figure 11. The cluster shown in figure 9 shows the relation between affiliation, language and publication type. The layout employed for creating this cluster is Frutherman Reingold in the Gephi open source software. There are 61 nodes and 60 edges in this cluster. Figure 10 depicts the cluster between subject area and year. There are 42 nodes and 34 edges. Cluster shown in figure 11 is drawn using the lay out Yifan Hu. It shows the relation between keyword and source title. There are 73 node and 75 edges in this cluster.

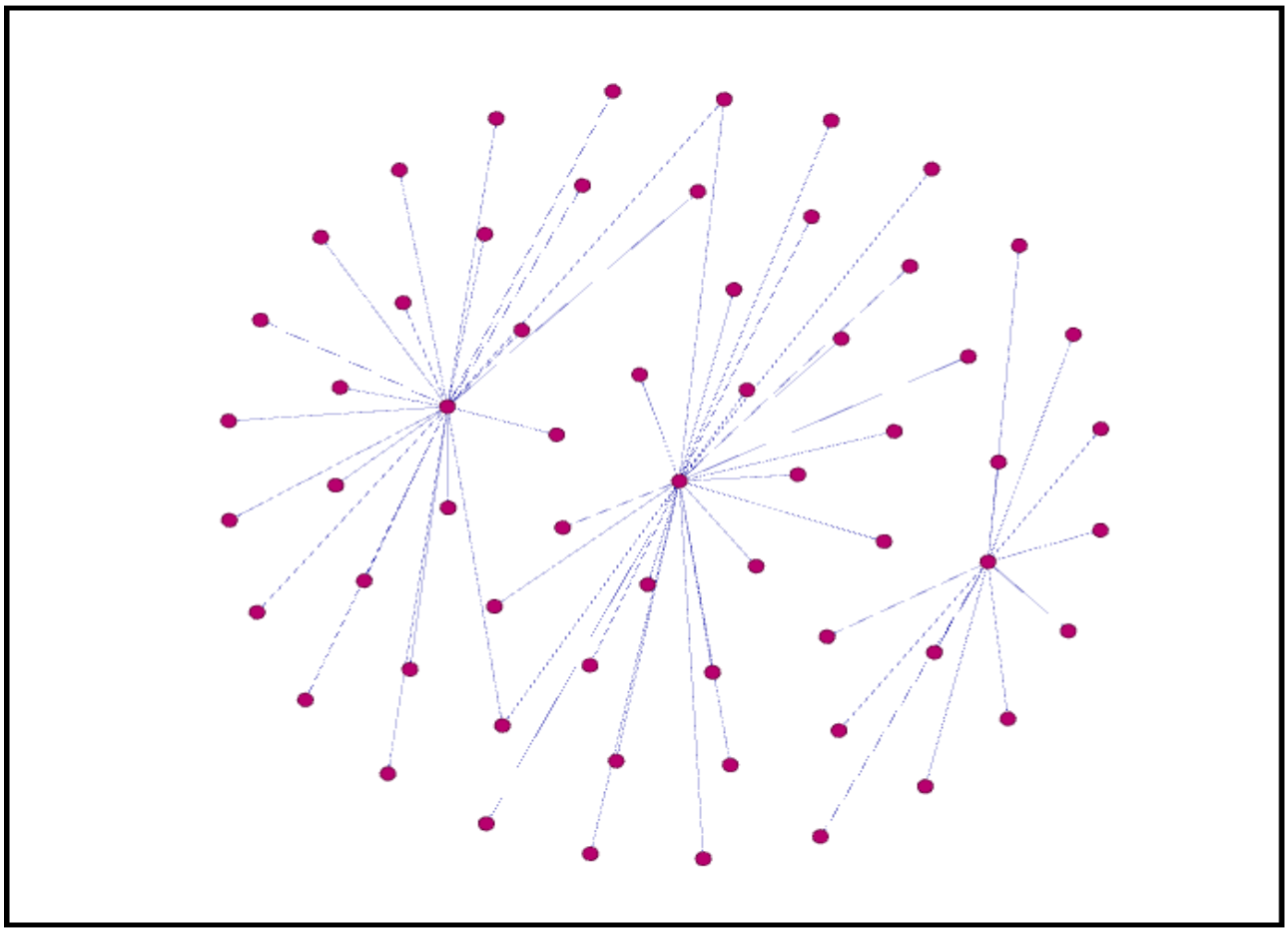

Figure 9: Cluster for relation between affiliation, language and publication type

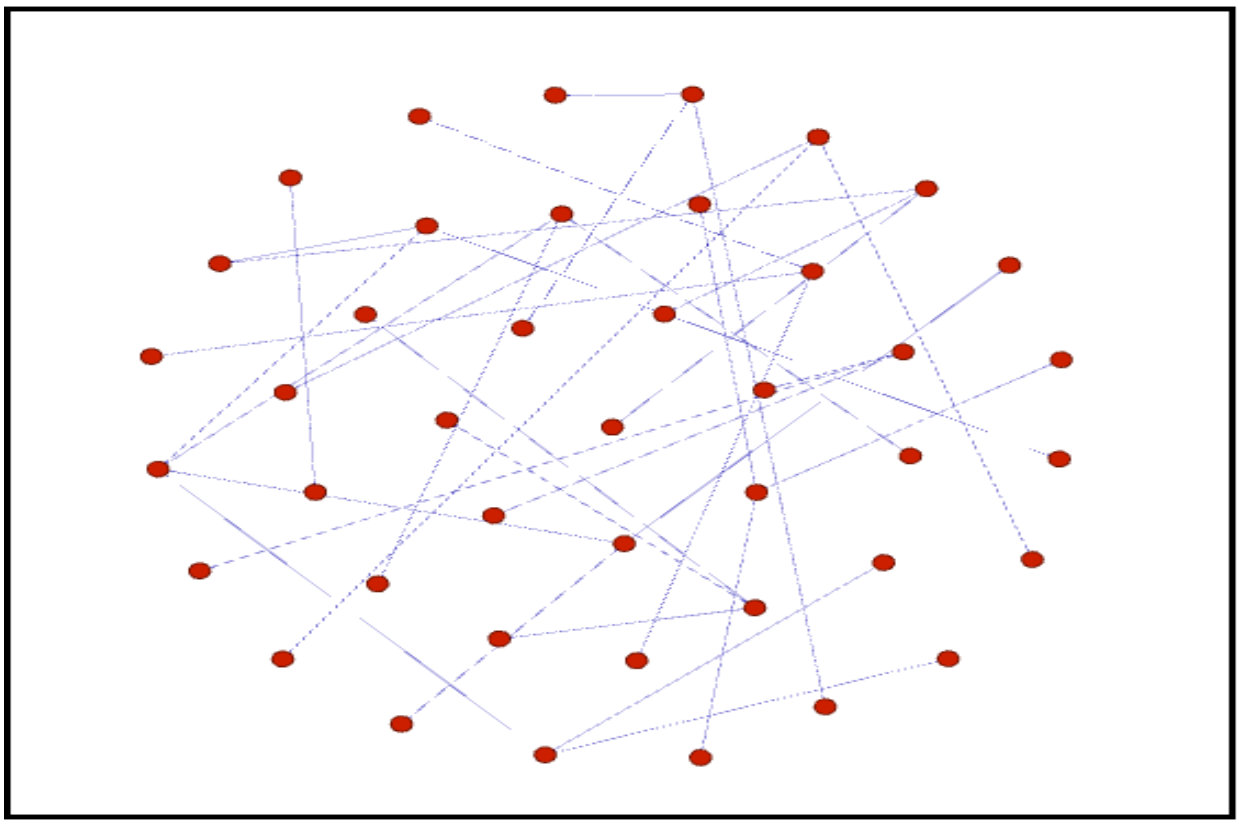

Figure 10: Cluster for relation between subject area and year

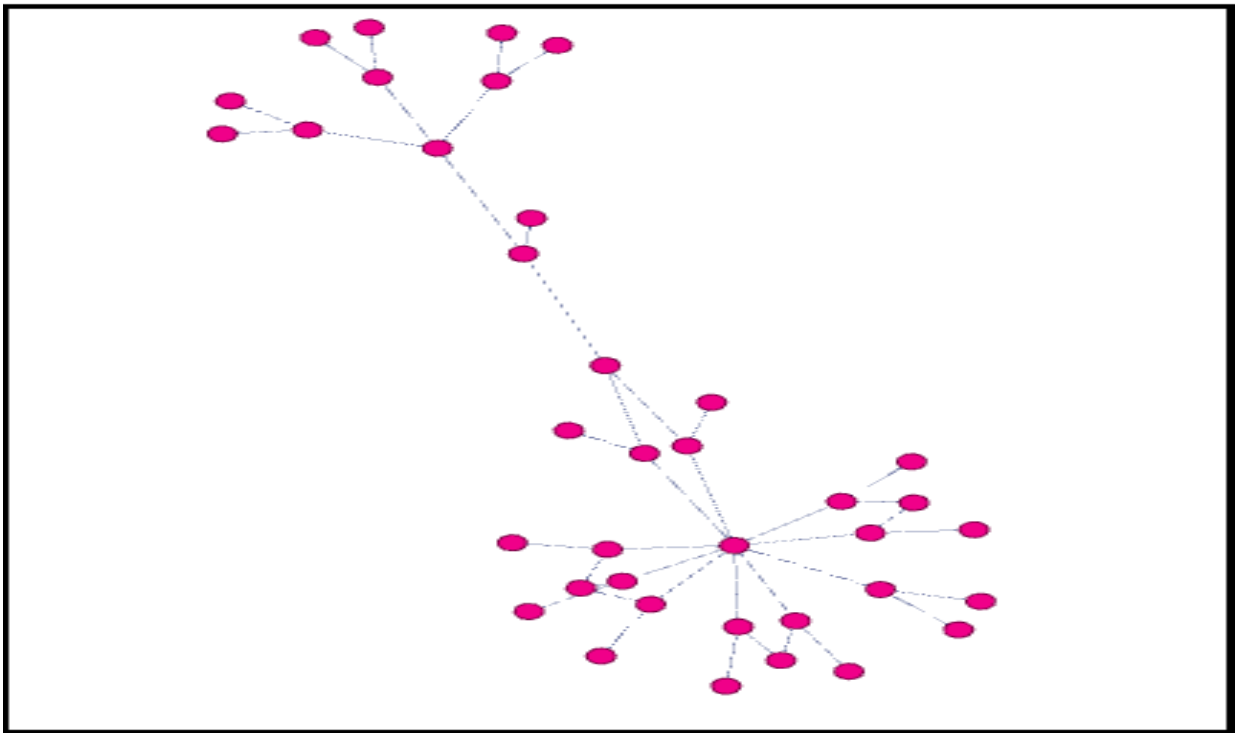

Figure 11: Cluster for relation between keyword and source title

3.7 Citation Analysis

The citations of each author (top twenty considered here) in the domain of NoC router optimization are given below in table 5.

Table 5: Authors with maximum of citations in the domain of NoC router optimization

Authors	<2016	2016	2017	2018	2019	2020	subtotal	>2020	total
Bakhoda A., Kim J., Aamodt T.M.	44	7	15	14	20	11	67	0	111
Mishra A.K., Vijaykrishnan N., Das C.R.	49	6	11	14	9	1	41	1	91
Ogras U.Y., Bogdan P., Marculescu R.	41	10	8	7	9	8	42	1	84
Modarressi M., Tavakkol A., Sarbazi-Azad H.	41	11	8	6	7	7	39	0	80
Ye Y., Xu J., Huang B., Wu X., Zhang W., Wang X., Nikdast M., Wang Z., Liu W., Wang Z.	21	12	13	11	12	6	54	0	75
Park S., Krishna T., Chen C.-H., Daya B., Chandrakasan A., Peh L.-S.	28	11	17	7	6	2	43	0	71
Mak T., Cheung P.Y.K., Lam K.-P., Luk W.	34	11	7	4	6	1	29	0	63
Ye Y., Xu J., Wu X., Zhang W., Liu W., Nikdast M.	25	9	10	6	4	2	31	0	56
Bokhari H., Javaid H., Shafique M., Henkel J., Parameswaran S.	9	10	18	7	3	2	40	0	49
Das S., Doppa J.R., Kim D.H., Pande P.P., Chakrabarty K.	0	3	11	5	10	7	36	0	36
Lee J., Nicopoulos C., Park S.J., Swaminathan M., Kim J.	6	2	10	9	3	4	28	0	34
Xu T.C., Liljeberg P., Tenhunen H.	22	5	0	0	3	0	8	0	30
Kim H., Ghoshal P., Grot B., Gratz P.V., Jimenez D.A.	15	1	2	5	4	1	13	0	28
Chen G., Anders M.A., Kaul H., Satpathy S.K., Mathew S.K., Hsu S.K., Agarwal A., Krishnamurthy R.K., Borkar S., De V.	6	12	5	3	0	1	21	0	27
Hu W., Lu Z., Jantsch A., Liu H.	18	2	1	4	2	0	9	0	27
Fu X., Li T., Fortes J.A.B.	19	2	3	1	2	0	8	0	27
Zhan J., Stoimenov N., Ouyang J., Thieley L., Narayanan V., Xie Y.	8	6	5	2	4	1	18	0	26
Tosun S., Ar Y., Ozdemir S.	5	3	8	4	3	2	20	1	26

Source: http://www.scopus.com (accessed on 9th November 2020)

4. LIMITATIONS OF THIS STUDY

Different combinations of keywords were used to explore the Scopus database for the purpose of bibliometric review. A few important journals and articles which were not available in Scopus database could not be incorporated in this study.

5. CONCLUSION

NoC has been recommended as an emerging alternative for scalability and performance needs of next generation System on chips (SoCs). NoC provides a solution for communication infrastructure for SoC. The router is a foremost component which significantly impacts the performance of NoC architecture. Therefore performance efficient NoC router design is paramount important. The bibliometric review of NoC router architectures and optimization is purely based on the data extracted from Scopus. The review highlights that maximum contribution in this area in terms of research publications is from the areas of Computer Science and Engineering It is revealed from this bibliometric analysis that major publications are from conferences, journals and articles from US publications, followed by Chinese and publications from the India. Based on the bibliometric review done in these study researchers who are the key research contributors in this area of research can evolve design methodology to optimize NoC router performance.

REFERENCES

1 Kumar, S., Jantsch, A., Soininen, J. P., Forsell, M., Millberg, M., Oberg, and Hemani, A. (2002). A network on chip architecture and design methodology. *Proceedings VLSI IEEE Computer Society Annual Symposium*, pp. 117-124.

2 Agarwal, A., Iskander, C., and Shankar, R. (2009). Survey of network on chip (noc) architectures and contributions. *Journal of Engineering, Computing and Architecture*, 3(1), pp. 21-27.

3 Benini, L., and De Micheli, G. (2002). Networks on chips: A new SoC paradigm. *Computer-IEEE Computer Society*, 35, pp. 70-78.

4 Bjerregaard, T., and Mahadevan, S. (2006). A survey of research and practices of network-on-chip. *ACM Computing Surveys (CSUR), 38(1)*, pp. 1-51.

5 Marculescu, R., Ogras, U. Y., Peh, L. S., Jerger, N. E., and Hoskote, Y. (2009). Outstanding research problems in NoC design: system, microarchitecture, and circuit perspectives. *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, 28(1)*, pp. 3-21.

6 Shahane, P. M., and Pisharoty, N. (2016). Implementation of input block of minimally buffered deflection NoC router. *International Journal of Engineering and Technology, 8*, pp. 1796-1800.

7 Dally, W. J., and Towles, B. (2001, June). Route packets, not wires: on-chip inteconnection networks. *Proceedings of the 38th annual Design Automation Conference, ACM*, pp. 684-689

8 Dally, W. J., and Towles, B. P. (2004). Principles and practices of interconnection networks. *The Morgan Kaufmann Series in Computer Architecture and Design, Elsevier.*

9 Banerjee, A., Wolkotte, P. T., Mullins, R. D., Moore, S. W., and Smit, G. J. (2009). An energy and performance exploration of network-on-chip architectures. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *17*(3), pp.319-329.

10 Taylor, M. B., Kim, J., Miller, J., Wentzlaff, D., Ghodrat, F., Greenwald, B., Hoffman, H. and Ma, A. (2002). The raw microprocessor: A computational fabric for software circuits and general-purpose programs. *IEEE micro, 22(2)*, pp.25-35.

11 Hoskote, Y., Vangal, S., Singh, A., Borkar, N., and Borkar, S. (2007). A 5-GHz mesh interconnect for a teraflops processor. *IEEE Micro, 5*, pp.51-61.

12 Cai, Y., Mai, K., and Mutlu, O. (2015). Comparative evaluation of FPGA and ASIC implementations of bufferless and buffered routing algorithms for on-chip networks. *Proceedings of Sixteenth International Symposium on Quality Electronic Design*, pp. 475-484

13 Moscibroda, T., and Mutlu, O. (2009). A case for bufferless routing in on-chip networks. *ACM SIGARCH Computer Architecture News, 37(3)*, pp. 196-207.

14 Borkar, S. (2007). Thousand core chips: a technology perspective. *Proceedings of the 44th Annual Design Automation Conference*, pp. 746-749.

15 Jafri, S. A. R., Hong, Y. J., Thottethodi, M., and Vijaykumar, T. N. (2010). Adaptive flow control for robust performance and energy. *Proceedings of the 43rd Annual IEEE/ACM International Symposium on Microarchitecture,* pp. 433-444.

16 Gratz, P., Kim, C., McDonald, R., Keckler, S. W., and Burger, D. (2006). Implementation and evaluation of on-chip network architectures. *Proceeding of International Conference on Computer Design, ICCD*, pp. 477-484.

17 Taylor, M. B., Kim, J., Miller, J., Wentzlaff, D., Ghodrat, F., Greenwald, B., Hoffman, H. and Ma, A. (2002). The raw microprocessor: A computational fabric for software

circuits and general-purpose programs. *IEEE micro*, *22(2)*, pp.25-35.

18 Hoskote, Y., Vangal, S., Singh, A., Borkar, N., and Borkar, S. (2007). A 5-GHz mesh interconnect for a teraflops processor. *IEEE Micro*, *5*, pp.51-61.

19 Martini, F., Bertozzi, D., and Benini, L.(2007). Assessing the impact of flow control and switching techniques on switch performance for low latency NoC design. *Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip.*

20 Cai, Y., Mai, K., and Mutlu, O. (2015). Comparative evaluation of FPGA and ASIC implementations of bufferless and buffered routing algorithms for on-chip networks. *Proceedings of Sixteenth International Symposium on Quality Electronic Design*, pp. 475-484

21 Fallin, C., Craik, C., and Mutlu, O. (2011). CHIPPER: A low-complexity bufferless deflection router. *High Performance Computer Architecture (HPCA), IEEE 17th International Symposium*, pp. 144-155.

22 Fallin, C., Nazario, G., Yu, X., Chang, K., Ausavarungnirun, R., and Mutlu, O. (2012). MinBD: Minimally-buffered deflection routing for energy-efficient interconnect. *Proceedings Networks on Chip (NoCS), Sixth IEEE/ACM International Symposium*, pp. 1-10.

23 Fallin, C., Nazario, G., Yu, X., Chang, K., Ausavarungnirun, R., and Mutlu, O. (2014). Bufferless and Minimally-Buffered Deflection Routing. *Routing Algorithms in Networks-on-Chip, Springer*, pp. 241-275.

24 Sujata S.B. and Sandi A. N. (2020). NOC'S: Buffered and Bufferless Structure and their design methodologies for High throughput and Low latency. *International Journal of Advanced Trends in Computer Science and Engineering*, *9(3)*,pp. 4117-4127.

25 Rantala, V., Lehtonen, T., Plosila, J.(2006). Network on chip routing algorithms. *Journal of Systems Architecture, TUCS Technical Report no* 779, pp. 5-7.

26 McKeown, N. (1999). The iSLIP scheduling algorithm for input-queued switches. *IEEE/ACM Transactions on Networking (TON), 7(2),* pp.188-201.

27 Belhajali, D., Mbarek, I. B., Hasnaoui, S., and Jelassi, K. (2013). A SoC interconnection scheduling-design and implementation of a scheduler based on credited-iSLIP algorithm. *Advances in Optoelectronic Materials*, *1(2)*, pp. 18-24.

28 Saravanakumar, U., Rajasekar, K., and Rangarajan, R. (2013). Implementation of scheduling algorithms for on chip communications. *International Journal of Computer Applications*, *62(14)*, pp. 35-38.

29 Brugge, M., and Khalid, M. A. (2014). A Parameterizable NoC Router for FPGAs. *Journal of Computers*, 9(3), pp. 519-528.

30 Gindin, R., Cidon, I., and Keidar, I. (2007). NoC-based FPGA: architecture and routing. *Proceedings of the First International Symposium on Networks-on-Chip*, IEEE Computer Society , pp. 253-264.

31 Salaheldin, A., Abdallah, K., Gamal, N., and Mostafa, H. (2015). *Review of NoC-based FPGAs architectures*. *Proceedings of International Conference on Energy Aware Computing Systems and Applications (ICEAC),* pp 1-4.

32 Papamichael, M. K., and Hoe, J. C. (2012). CONNECT: re-examining conventional wisdom for designing nocs in the context of FPGAs. *Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays,* pp. 37-46.