Carrier-based Closed-loop DC-link Voltage Balancing Algorithm for Four Level NPC Converters based on Redundant Level Modulation

Jun Wang, *Member, IEEE,* Xibo Yuan, *Senior Member, IEEE,* Bosen Jin

***Abstract*—Four-level neutral-point-clamped (NPC) multilevel converter topologies have been proposed and actively studied for low/medium voltage applications. As an inherent issue with these topologies, the voltage balancing of dc-link capacitors is challenging, especially when it operates as a single-end inverter/rectifier with high power factors and high modulation indexes. This paper proposes a closed-loop voltage balancing algorithm that is effective and simple to implement with regular level-shifter carriers for a four-level NPC converter, e.g. a π-type converter. This approach is based on the Redundant Level Modulation (RLM), which utilizes one additional voltage level in one switching cycle to gain extra controllability of the capacitor voltages without distorting/undermining the fundamental-frequency output voltage. An algorithm based on analytical expressions and logical operations is developed to achieve a dynamic closed-loop voltage balancing with RLM. The proposed method is effective over the full span of linear modulation indexes (*M* = 0 ~ 1.15) and power factors. The proposed algorithm is validated and evaluated in both simulations and experiments.**

***Index Terms*—neutral point clamped, redundant level modulation, four level, carrier based, voltage balancing.**

I. Introduction

NEUTRAL-POINT-CLAMPED (NPC) multilevel converters have been actively studied and implemented as alternative topologies for low/medium voltage, high-power applications in the past decades. Compared to a conventional two-level converter, the benefits of multilevel topologies include lower d*v*/d*t*, lower output harmonics and lower switching losses. In recent years, the family of NPC multilevel topologies has been expanding. As a derivative of the three-level NPC converters, the four-level NPC topologies, such as a π-type converter, have been proposed and actively researched [1]–[6]. Fig. 1 shows a generalized representation of a four-level NPC structure.

The main challenge in a four-level NPC converter with Pulse Width Modulation (PWM) is to maintain the middle capacitor voltage, especially under unity power factors (*PF*) and high modulation indexes (*M*) [4]–[6]. To operate normally, the three dc-link capacitors voltages must be maintained at 1/3 of the whole dc-link voltage.

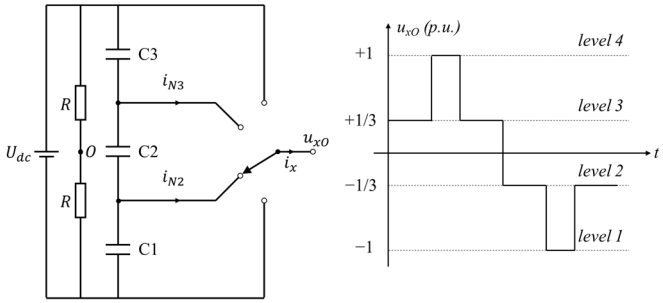


Fig. 1. A generalized four-level NPC structure with one phase leg

To explain this challenge, Fig. 2 illustrates the charge/discharge status of the middle capacitor C2 with the ordinary modulation at unify *PF*, where a fundamental cycle is sliced up to *I-VIII* switching cycles. As illustrated, typically the sum of the red discharge areas is significantly larger than the blue charge areas in this case. Especially in sections *II, III, VI* and *VII*, the ordinary modulation leads to only the discharge of C2 at around the peak load current. Subsequently, the converter operating at unity PF results in the constant discharge of C2 over fundamental cycles. In this case, the voltage of C2 will collapse to zero and the converter will lose the ability of outputting four voltage levels.

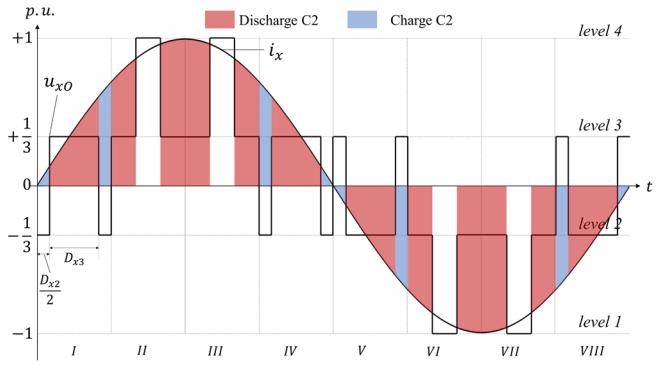


Fig. 2. Charge/discharge status of C2 with ordinary modulation ($cos\ \varphi = 1$).

To achieve the voltage balancing of a four-level NPC converter, numerous research efforts have been made in the literatures. As the conventional approach, Zero-sequence Signal Injection (ZSI) is one degree of freedom in a multi-phase four-level converter [4]–[6]. This approach is in principle equivalent to the nearest three vector (NTV) with redundant space vector selection presented in [1], which alters the three-phase reference voltages without affecting the line-to-line output voltages. As analyzed in [1], when the four-level topology is in a single-end configuration with passive front ends, this conventional approach loses the controllability in the case of a high *PF* and a high *M*. Although this conventional approach can be more

This work was supported in part by the EPSRC UK National Centre for Power Electronics under Grant EP/R004137/1. Corresponding author: Xibo Yuan.

Jun Wang and Xibo Yuan are with the Department of Electrical and Electronic Engineering, University of Bristol, Bristol, BS8 1UB, U.K. (e-mail: jun.wang@bristol.ac.uk; xibo.yuan@bristol.ac.uk).

Bosen Jin was with the Department of Electrical and Electronic Engineering, University of Bristol, Bristol, BS8 1UB, U.K. He is now with Agilent Technologies Ltd., UK. (e-mail: bosen.jin@agilent.com)

effective in a back-to-back configuration, in which the control challenge is moderated as a result of the two active ends, it still cannot maintain the effectiveness over the full span of *M* and *PF* [6]. In this work, modulation index *M* is defined as the peak phase voltage divided by half of the dc-link voltage, for which the linear modulation range is between 0 ~ 1.15 (with third-order harmonic injection).

As a newly identified degree of freedom, utilizing redundant output voltage levels within one switching cycle has been exploited in recent studies for the voltage balancing of various topologies, such as [7]–[9] in a three-level NPC converter; [10]–[13] in a four-level and n-level NPC converter based on overlapped carriers; [14]–[20] in four-level and n-level NPC converters based on virtual space vectors and perturbation of duty ratios; [21] in a five-level flying-capacitor converter. However, the approach in [14]–[20] involves complex compensator parameters and virtual vector modulators that are challenging to establish from scratch and to be transferred between setups. As the carrier-based solutions, [10]–[13] are based on special overlapped carriers. However, the approach in [10], [13] is essentially an open-loop control that maintains equal charge/discharge of the capacitors within each switching cycle. If there is an initial unbalance of the capacitor voltages, this method cannot pull back the unbalance due to its open-loop nature. Although [11], [12] adds a fine adjustment of duty ratios to form a closed-loop control, it requires a mandatory PI controller to obtain the required control efforts, which involves extra tuning process. As the voltage balancing is mandatory for four-level NPC converters without additional balancing circuits, a simple-to-implement control scheme is desired, which can greatly simplify the controller prototyping process.

As the contribution, this paper proposes a carrier-based closed-loop voltage balancing algorithm for a four-level NPC converter that is simple to implement and effective over full operating conditions. The proposed approach features the following merits:

- Closed-loop control of capacitor voltages on switching cycle basis
- No mandatory PI/PID controllers required. The algorithm solves the precise control efforts dynamically through analytical expressions and measured signals
- No reduction in converter output voltage/capacity at any operating point
- Simple implementation with ordinary level-shifted carriers
- Effective over the full span of converter operating points

The proposed approach was firstly brought up in the conference paper [22] and further improved by combining it with conventional ZSI approach to form a hybrid scheme in this paper. The rest of the paper is organized as follows. Section II introduces the principles of the proposed voltage balancing scheme. Section III further improves the scheme with a hybrid approach. Section IV shows the performance evaluations in simulations and a comparison with similar existing approaches. Section V shows the experimental validations.

II. C2 BALANCING WITH REDUNDANT LEVEL MODULATION

To solve the critical problem in the four-level NPC topologies, i.e. balancing the middle capacitor voltage, this paper proposes an approach that utilizes the redundant output voltage levels to gain the controllability of C2 voltage, which is named as the Redundant Level Modulation (RLM) in this work.

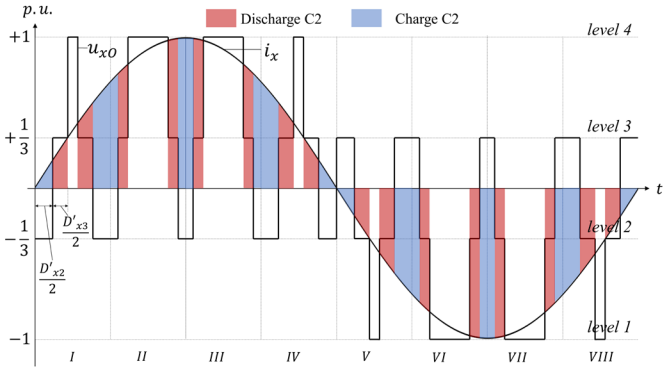


Fig. 3. Charge/discharge status of C2 with RLM ($cos\ \varphi = 1$).

A. Principles of Redundant Level Modulation (RLM)

In a four-level converter, the charge/discharge status of the middle capacitor can be altered by introducing an additional phase output voltage level (the redundant level) in one switching cycle. Fig. 3 illustrates the top-level principle of RLM. Taking switching cycle *II* as an example, the additional *level 2* is added while the ordinary modulation only utilizes *level 4* and *level 3*. The existence of the *level 2* in this cycle brings blue charge durations for C2 that does not exist in Fig. 2 with ordinary modulation. The volt-time product of this switching cycle stays the same while part of *level 3* is replaced with a proper combination of *level 2* and *level 4*. The use of *level 2* in this cycle is redundant for synthesising the output voltage, but it can be utilized to gain extra controllability of C2 voltage. This is a similar concept as the virtual zero-level modulation (VZM) in [8], where part of the zero level in a three-level converter can be replaced by adjacent two voltage levels. Similarly, each switching cycle in Fig. 3 has exactly the same volt-second product as in Fig. 2, hence this approach is harmless to the average output voltage of each switching cycle. This approach can be understood as altering the high-frequency behavior of the phase output voltage while the fundamental-frequency output voltage is unaffected. By utilizing this degree of freedom, the duration of the red and blue areas can be manipulated to control the voltage of C2. The deviation of the C2 voltage is defined as

$$\Delta U_{C2} = U_{C2-ref} - U_{C2} \tag{1}$$

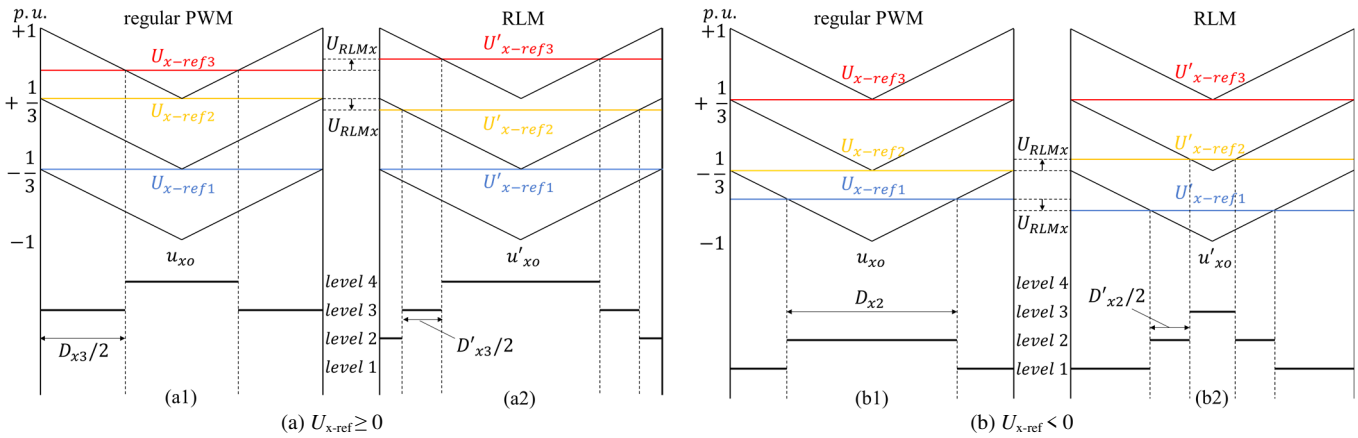
The reference value of the middle capacitor voltage $U_{\text{C2-ref}}$ is normally the 1/3 of the total DC-link voltage, but it can also be given as an individual demand.

To pull the unbalance ΔU_{C2} to zero within one switching cycle, the difference of the neutral point (NP) currents needs to satisfy the following equation as derived in [3]

$$\Delta U_{C2} = \frac{1}{3} \cdot (\bar{i}_{N2-ref} - \bar{i}_{N3-ref})/(C \cdot f_{sw}) \tag{2}$$

where $i_{\text{N2-ref}}$ and $i_{\text{N3-ref}}$ are the reference NP currents to counter the voltage unbalance with the reference direction defined in Fig. 1. Subsequently, to balance U_{C2} in one switching cycle, K_{ref} is defined as the control objective as

$$K_{ref} = \bar{i}_{N2-ref} - \bar{i}_{N3-ref} = 3 \cdot \Delta U_{C2} \cdot C \cdot f_{sw} \tag{3}$$



(a) $U_{x\text{-ref}} \geq 0$ (b) $U_{x\text{-ref}} < 0$

Fig. 4. Illustration of the level-shifted carriers and split modulating waves in one switching cycle.

In each switching cycle, the average neutral point currents are contributed by three-phase load currents as

$$\bar{i}_{N2} = I_a D_{a2} + I_b D_{b2} + I_c D_{c2} \tag{4}$$

$$\bar{i}_{N3} = I_a D_{a3} + I_b D_{b3} + I_c D_{c3} \tag{5}$$

where I_x is the phase load current; D_{x2} and D_{x3} are the duty ratios of the output voltage *level 2* or *level 3*. Therefore, the control of the neutral point currents can be achieved by manipulating the D_{x3} and D_{x2} of all phases ($x = a, b, c$). Note the manipulation of D_{x3} and D_{x2} is independent for each individual phase through the RLM. For one individual phase, a simplified reference command can be implemented as following, considering equations (1)-(5)

$$I_x(D_{x2-ref} - D_{x3-ref}) = K_{ref}/3 \tag{6}$$

where the control objective K_{ref} is equally distributed to three phases as $K_{ref}/3$. To achieve the control objective, there are two cases to proceed depending on the polarity of the modulating wave as shown in Fig. 3. When the reference phase voltage $U_{x\text{-ref}}$ (x=*a,b,c*) is positive, *level 4, level 3* and *level 2* are utilized and the control focus is the middle level's duty ratio D'_{x3}. When $U_{x\text{-ref}}$ is negative, *level 3, level 2* and *level 1* are utilized, and the control focus becomes D'_{x2}. The following example is given when the reference voltage $U_{x\text{-ref}}$ is positive. Firstly, the following equation must be satisfied for the three duty ratios

$$D_{x4-ref} + D_{x3-ref} + D_{x2-ref} = 1 \tag{7}$$

To satisfy the reference output voltage, the following equation must stand

$$D_{x4-ref} + D_{x3-ref}/3 - D_{x2-ref}/3 = U_{x-ref} \tag{8}$$

Equations (6)-(8) contains three variable that are solvable. For the middle level, the closed-form solution of $D_{x3\text{-ref}}$ is

$$D_{x3-ref} = -(4K_{ref} - 9I_x + 9I_x U_x)/(18I_x) \tag{9}$$

However, the control command $K_{ref}/3$ can be unfeasible depending on the imbalance. In principle, this command always attempts to pull back the imbalance within one switching cycle no matter how large the imbalance is. Therefore, the solved duty ratios must be trimmed by an upper/lower limiter. Comparing Fig. 2 and Fig. 3, it can be seen that, when $U_{x\text{-ref}}$>0, the degree of freedom is to shrink D_{x3} and introduce additional D_{x4} and D_{x2} to maintain the same volt-second product. In this case, the trim is performed on the D_{x3}. There are two constraints that limit the modified duty ratio D'_{x3}. Constraint (10) ensures the modified D'_{x3} to be equal to/smaller than the original value D_{x3}. By setting up this rule along with (8), it is ensured that the maximum modulation index is not undermined.

$$D'_{x3} \leq D_{x3} \tag{10}$$

Constraint (11) defines a minimum "dwell time" T_{DT} [8], [21] to avoid skipping voltage levels so that the multilevel operation is ensured with reduced *dv/dt*

$$D'_{x3} \cdot T_{sw} \geq T_{DT} \tag{11}$$

If the reference value $D_{x3\text{-ref}}$ is beyond these two boundaries, it will be limited to produce a reasonable D'_{x3}.

From equation (1) to (11), an optimal D'_{x3} is found to achieve the tracking of the control objective $K_{ref}/3$, which will lead to the RLM operation and subsequently the precise control of the middle capacitor voltage U_{C2}. All the calculations are made under per unit values to retrieve correct values of duty ratios.

Note the above calculations are in the case of a positive $U_{x\text{-ref}}$. When $U_{x\text{-ref}}$ is negative, *level 3, level 2* and *level 1* are used instead as shown in Fig. 3, with the duty ratio of the middle level (*level 2* in this case) solved as

$$D_{x2-ref} = (4K_{ref} + 9I_x + 9I_x U_x)/(18I_x) \tag{12}$$

To track the total control objective K_{ref}, the above duty ratio calculations are conducted for all three phases individually.

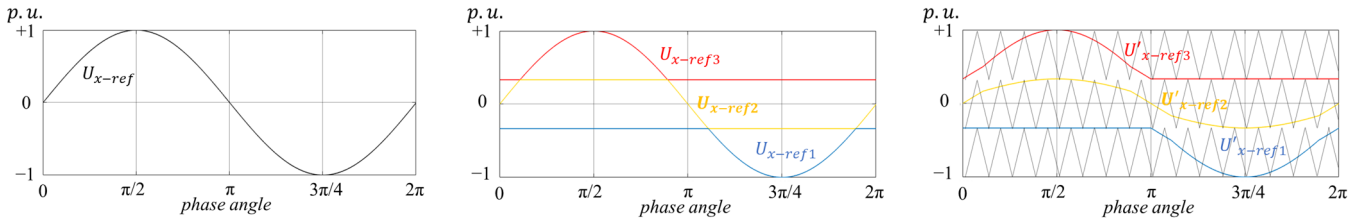
B. Implementation of RLM with level-shifted carriers

The proposed RLM approach can be implemented through various modulation techniques. In multilevel converters, the most commonly used modulation scheme is the level-shifted carrier PWM for simple implementation, such as in [6], [8]. Based on the level-shifted carriers, the RLM operation can be achieved by split and modify the modulating waves as in [8], [9], although this approach was only implemented for three-level NPC converters in these previous studies.

In this approach, the original sinusoidal modulating wave $U_{x\text{-ref}}$ is split to three signals $U_{x\text{-ref3}}$, $U_{x\text{-ref2}}$ and $U_{x\text{-ref1}}$ that correspond to the three level-shifted carriers through the piecewise function in Table I. The level-shifted carrier pattern can be realized as one carrier with offsets to virtually generate three carriers in the hardware programming.

TABLE I. SPLIT FUNCTION OF THE MODULATING WAVE

	$U_{x\text{-ref}} \geq 1/3$	$1/3 > U_{x\text{-ref}} \geq -1/3$	$U_{x\text{-ref}} < -1/3$
$U_{x\text{-ref3}}$ =	$U_{x\text{-ref}}$	1/3	1/3
$U_{x\text{-ref2}}$ =	1/3	$U_{x\text{-ref}}$	−1/3
$U_{x\text{-ref1}}$ =	−1/3	−1/3	$U_{x\text{-ref}}$



(a) original sinusoidal wave (b) split waves (c) altered split waves with level-shifted carriers

Fig. 5. Implementation of the RLM balancing scheme with split modulation wave method (M = 1, Kref = 0).

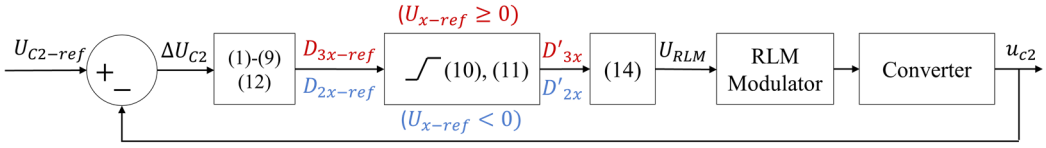


Fig. 6. Closed-loop control of U_{C2} through RLM.

Fig. 4 shows a zoomed-in switching cycle to demonstrate how the RLM operation is realized by altering the split modulating waves. The degree of freedom in this approach is the width of the middle level (D'_{x3} or D'_{x2}) that can be varied between the original duty ratios and zero (if the dwell time can reach zero) as expressed in (10)-(11), without changing the cycle's volt-second product. Because the switching frequency f_{sw} is typically much higher than the fundamental frequency f_0, the reference voltages can be considered constant in this view. To realize the redundant level and the calculated duty ratios D'_{x3} or D'_{x2}, an offset voltage U_{RLM} is injected through (13) to "space away" two adjacent modulating waves. Then the phase output voltage u_o is changed from Fig. 4 (a1)(b1) to Fig. 4(a2)(b2) while the average output voltage stays the same.

$$\begin{cases} U'_{x-ref3} = U_{x-ref3} + U_{RLMx} \\ U'_{x-ref2} = U_{x-ref2} - U_{RLMx}, (U_{x-ref} \geq 0) \\ U'_{x-ref1} = U_{x-ref1} \end{cases}$$
$$\begin{cases} U'_{x-ref3} = U_{x-ref3} \\ U'_{x-ref2} = U_{x-ref2} + U_{RLMx}, (U_{x-ref} < 0) \\ U'_{x-ref1} = U_{x-ref1} - U_{RLMx} \end{cases} \quad (13)$$

Derived from the geometrical relationships in Fig. 4, the offset voltage $U_{RLMx} \geq 0$ for phase x can be calculated from the original duty ratios (D_{x3} or D_{x2}) and the target duty ratios (D'_{x3} or D'_{x2}) as

$$U_{RLMx} = \begin{cases} (D_{x3} - D'_{x3})/3, & (U_{x-ref} \geq 0) \\ (D_{x2} - D'_{x2})/3, & (U_{x-ref} < 0) \end{cases} \quad (14)$$

Fig. 5 shows a zoomed-out view of a fundamental cycle of the original modulating wave, the split modulating waves and the altered modulating waves. To extend the maximum linear M from 1 to 1.15, a third-order harmonic can be injected in Fig. 5 (a) first before splitting it to Fig. 5 (b) as applied in [8].

Therefore, a closed-loop control of U_{C2} is formed as shown in Fig. 6, which is based on analytical expressions (1)-(14) with no integral/derivative operations. The precise target duty ratios and U_{RLM} is found from the measured unbalance of U_{C2}.

C. Features of the proposed RLM approach

The proposed approach can be easily implemented in a Digital Signal Processor (DSP) based control system. As introduced, level-shifted-carrier-based modulators are very common in multilevel converters. The proposed approach does not require any changes on the modulator block because it only manipulates the modulating waves. A detailed block diagram of the control scheme can be found in [22]. Moreover, the proposed algorithm involves only analytical expressions and logical operations without requiring any mandatory PI/PID controllers, which is similar to the algorithm in [7] for three-level converters. The proposed algorithm can be considered as dynamically finding/applying a gain depending on the instantaneous load current to eliminate the capacitor voltage error in the closed-loop control in Fig. 6, together with the integral element from the plant (capacitor). This feature simplifies the implementation and the tuning process of control parameters. Additionally, the proposed approach offers a precise control towards the control objective. Instead of a fixed dwell time (see [21]), the D'_{x3} and D'_{x2} in this approach is adjusted dynamically in each switching cycle depending on the imbalance of U_{C2}. Although an optional PI controller can be added in the loop to adjust/improve the control performance, the proposed approach fundamentally does not require additional PI controllers to realize the voltage balancing.

Meanwhile, there are negative side effects of this approach while it balances the capacitor voltages. As shown in Fig. 4, introducing the redundant voltage level leads to additional switching transitions in one switching cycle, i.e. four times instead of two, and subsequently increased switching losses. But, the increase of switching loss can be moderated by applying a lower switching frequency or applying wide-bandgap (WBG) power devices with ultra-low switching losses. Note the switching losses of the four-level NPC topology are already relatively low, because the semiconductors only switch at a portion of the dc-link voltage, rather than a full dc-link voltage in a standard two-level converter. The additional switching transitions can also lead to higher high-frequency harmonics, although these high-frequency harmonics can be relatively easy to filter. Additionally, the multilevel topology inherently requires lower switching frequency to achieve the same harmonic limits against standard two-level converters.

These negative side-effects are not unique in the proposed approach and they exist in all the existing methods in [10]–[20], because fundamentally they all utilize the additional voltage levels. Given the voltage balancing scheme is typically mandatory for the four-level NPC topology, the increased switching transitions can be considered as an inevitable drawback for the topology. Note that the proposed approach is slightly different to [14]–[20], in which the two outer levels,

level 4 and *level 1*, can be both used in one switching cycle, which can lead to four voltage levels appearing in one switching cycle. In contrast, the proposed approach adds only one adjacent voltage level (as shown in Fig. 4), i.e. only three levels at most in one switching cycle of the phase output voltage.

III. Further Optimization on the Balancing Scheme

The RLM scheme presented in Section II already enables the middle capacitor voltage to be well controlled in a single-end four-level NPC topology. It still has the following aspects that can be improved

1) Outer capacitors C3 and C1 are not controlled. Although the outer capacitors can be self-balanced over a fundamental cycle [10], [22] when C2 is balanced, a low-frequency ripple can show in U_{C3} and U_{C1} .
2) The RLM scheme in Section II leads to additional switching transitions in all the three phase legs, which leads to doubled switching transitions compared to regular Sinusoidal PWM (SPWM). Therefore, this configuration is referred as 3-ph (three-phase) RLM in this section. As implemented in three-level converters in [7], [8], it may be possible to activate RLM in only one phase to sufficiently achieve voltage balancing while avoiding the increase of switching transitions in the rest two phase legs.

To improve the above aspects, the conventional zero-sequence signal injection (ZSI) can be mixed with the RLM approach to form a hybrid voltage balancing scheme, which can further extend the controllability and improve the performance. This concept of hybrid ZSI and RLM has been proposed and implemented in three-level converters [8]. The principle of ZSI is to inject a zero-sequence signal U_{ZSI} into the reference voltages of all three phases as

$$U'_{x-ref} = U_{x-ref} + U_{ZSI} \quad (x = a, b, c) \tag{15}$$

The added zero-sequence component is canceled out in the line-to-line voltages hence it is harmless to the fundamental-frequency output voltage. By applying appropriate ZSI, the charge/discharge status of the capacitors can be manipulated to serve the purpose of voltage balancing. The common approach of selecting an optimal ZSI signal is to perform optimal-searching iterations in each switching cycles, which has been successfully implemented in three-level NPC converters [8], [23]. The optimal U_{ZSI} is selected out from the constrained range as follows to avoid over-modulation

$$-1 - \min(U_{x-ref}) \le U_{ZSI} \le 1 - \max(U_{x-ref}) \tag{16}$$

A. ZSI for C1/C3 and 3-ph RLM for C2

This work further applies ZSI in a four-level NPC converter to balance the top and bottom dc-link capacitors. To balance U_{C3} and U_{C1}, the sum of the neutral point currents needs to satisfy the following equation as derived in [10]

$$\Delta U_{C3} - \Delta U_{C1} = (\bar{i}_{N2-ref} + \bar{i}_{N3-ref})/(C \cdot f_{sw}) \tag{17}$$

By injecting the ZSI component, the altered duty ratios lead to the manipulated neutral point currents as

$$\bar{i}_{N2-ZSI} = I_a D_{a2-ZSI} + I_b D_{b2-ZSI} + I_c D_{c2-ZSI} \tag{18}$$

$$\bar{i}_{N3-ZSI} = I_a D_{a3-ZSI} + I_b D_{b3-ZSI} + I_c D_{c3-ZSI} \tag{19}$$

By performing an iterative operation with a sufficiently small step size, a zero-sequence signal is selected to control the sum of the NP currents to track the reference in (17). Therefore, the control objective becomes finding the U_{ZSI} that yields the smallest difference S between the altered sum and the reference sum of NP currents, which is expressed as

$$S = \left|(\bar{i}_{N3-ZSI} + \bar{i}_{N3-ZSI}) - (\bar{i}_{N2-ref} + \bar{i}_{N3-ref})\right| \tag{20}$$

Combining the presented ZSI scheme and the RLM scheme, a two-stage hybrid voltage balancing algorithm is proposed in this work to balance the voltages of all three dc-link capacitors with its top-level concept illustrated as Scheme 2 in Fig. 7.

Note the RLM step must be placed after the ZSI step, because ZSI can only be injected before the split of modulating waves. This voltage balancing scheme enables the closed-loop control of all three dc-link capacitors in the four-level topology. The performance of this scheme will be evaluated in Section IV.

B. ZSI for C1, C2 and C3 and 1-ph RLM

As introduced in the beginning of Section III, the second possible aspect to improve the balancing scheme is to activate RLM in only one phase out of three phases, which can be referred as 1-ph RLM. Compared to 3-ph RLM, 1-ph RLM has reduced controllability in exchange for less switching transitions. In the case of a four-level NPC, 1-ph RLM cannot balance the C2 voltage on its own at a high modulation index due to its reduced controllability as concluded from extensive simulation attempts. But, 1-ph RLM will work if the control challenge of balancing C2 is beforehand eased by the ZSI step.

Therefore, a further optimized voltage balancing scheme is proposed as follows. Based on the two-stage hybrid Scheme 2 in Fig. 7, instead of attempting to control only C3 and C1, the ZSI stage can be programmed to balance all three capacitors, as implemented in [6]. After the ZSI stage, the C3 and C1 are balanced and the moderated control objective of balancing C2 is handed over to the 1-ph RLM stage. To balance all three capacitors, the control objective of the ZSI stage can be set to minimize the voltage deviation of all three capacitors at the same time, for which the objective function J is expressed as follow as implemented in [6]

$$J = -\Delta U_{C3} i_{C3-ZSI} - \Delta U_{C2} i_{C2-ZSI} - \Delta U_{C1} i_{C1-ZSI} \tag{21}$$

where the three capacitor currents can be found from the NP currents as

$$\begin{cases} i_{C3-ZSI} = \frac{2}{3}\bar{i}_{N3-ZSI} - \frac{1}{3}\bar{i}_{N2-ZSI} \\ i_{C2-ZSI} = -\frac{1}{3}\bar{i}_{N3-ZSI} + \frac{1}{3}\bar{i}_{N2-ZSI} \\ i_{C1-ZSI} = -\frac{1}{3}\bar{i}_{N3-ZSI} - \frac{2}{3}\bar{i}_{N2-ZSI} \end{cases} \tag{22}$$

To apply 1-ph RLM, the dominant phase y [8] needs to be selected out from the three phases $x = a, b, c$. In this work, the selection criterion is to find the phase that originally contributes the most opposing component against the control objective K_{ref}. The original difference of the two unaltered NP currents is as

$$K_{ori} = \bar{i}_{N2} - \bar{i}_{N3} = I_a(D_{a2} - D_{a3}) + I_b(D_{b2} - D_{b3}) + I_c(D_{c2} - D_{c3}) \tag{23}$$

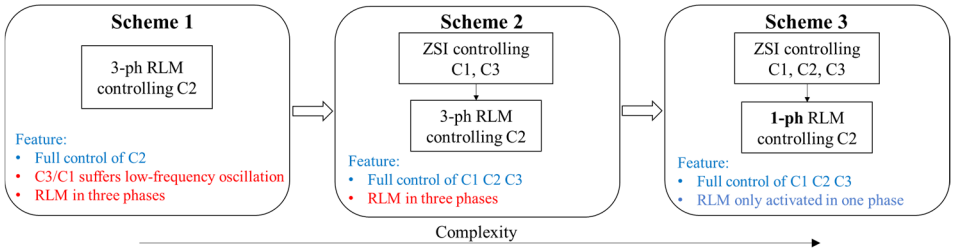


Fig. 7. Optimization process of the proposed voltage balancing schemes for a four-level NPC converter

TABLE II. Comparison of key concepts of carrier-based voltage balancing schemes for four-level NPCs

	Closed-loop control	Mandatory PI controller	RLM for C2	ZSI for C2	ZSI for C1/C3	Effective over full operating conditions
[6]	Yes	No	No	Yes	Yes	No
[10], [13]	No	No	Yes, 3-ph RLM	No	No	**Yes**
[11]	Yes	Yes	Yes, 3-ph RLM	No	Yes	**Yes**
[12]	Yes	Yes	Yes, 3-ph RLM, only at $M > 0.5$	Yes, only at $M < 0.5$	Yes	**Yes**
Scheme 1	**Yes**	**No**	Yes, 3-ph RLM	No	No	**Yes**
Scheme 2	**Yes**	**No**	Yes, 3-ph RLM	No	**Yes**	**Yes**
Scheme 3	**Yes**	**No**	**Yes, 1-ph RLM**	**Yes**	**Yes**	**Yes**

For example, when $K_{ori} < K_{ref}$, if $I_a(D_{a2}- D_{a3})$ is the smallest term in (23), phase a is the dominant phase. When $K_{ori} > K_{ref}$, if $I_b(D_{b2}- D_{b3})$ is the largest term in (23), phase b is the dominant phase. After the dominant phase y is selected, the RLM is then applied to mitigate its contribution in (23) following the closed loop in Fig. 6 to track the control objective K_{ref}. In this case, the dominant phase y bears the full control objective K_{ref}, instead of $K_{ref}/3$ in (6). Therefore, in the 1-ph RLM, the calculation in (9) and (12) should be changed as

$$D_{y3-ref} = -(4K_{ref} - 3I_y + 3I_yU_y)/(6I_y) \quad (24)$$

$$D_{y2-ref} = (4K_{ref} + 3I_y + 3I_yU_y)/(6I_y) \quad (25)$$

The top-level process of the proposed ZSI+1-ph RLM scheme is illustrated as Scheme 3 in Fig. 7. This optimized scheme can still achieve the voltage balancing of all three capacitors. Meanwhile, the usage of RLM is reduced from three phases to one phase at any moment, thus the additional switching losses is reduced. The performance of this scheme will also be evaluated in Section IV.

C. Summary and comparison with existing approaches

Fig. 7 visualizes the development process of the concepts in the improved schemes. The basic RLM Scheme 1 already solves the fundamental controllability issue of C2, which enables the four-level NPC topology to operate normally in a single-end configuration. Based on Scheme 1, this section further optimizes the approach by introducing ZSI to form a two-stage hybrid scheme. By effectively mixing the two degrees of freedom, ZSI and RLM, the controllability and performances are further improved in the hybrid schemes.

To demonstrate the uniqueness of the proposed schemes, a comparison with the existing approaches is conducted in this section. Table II shows a comparison of the existing approaches regarding the key concepts and features. As a reference, the conventional approach [6] applies the ZSI, which is a closed-loop control without PI controllers. However, [6] loses the controllability at a high M and high PF.

As the carrier-based solutions utilizing the redundant voltage level, [10]–[13] can be seen as the main competitor to the proposed scheme. Firstly, the approach in [10][13] are open-loop controls that are fundamentally realized by achieving zero neutral point currents in each switching cycle. However, in practical, a closed-loop control is required to pull back the capacitor voltage deviation caused by non-ideal operations [13]. Developed from [10][13], [11][12] realized a closed-loop control with a mandatory PI controller to convert the imbalance of voltage into the fine adjustments (≤10%) of the duty ratios, which requires time-consuming tuning process that is typically based on trial and error. In contrast, the proposed RLM is solved from analytical expressions to dynamically find the precise control efforts and duty ratios on switching cycle basis.

Regarding the RLM operation, [10]–[13] all utilize one extra redundant voltage level in all three phases (3-ph RLM), which can lead to up to doubled total switching losses. In contrast, the proposed Scheme 3 only activates RLM in one phase at one time, which significantly reduces the additional switching transitions required. This point will be quantifiably analyzed in Section I.B. Moreover, the proposed approach only alters the modulating waves, instead of requiring special carriers and modulators, e.g. the carrier-overlapped PWM [10].

IV. PERFORMANCE EVALUATION BY SIMULATION

The performance of the proposed voltage balancing schemes is evaluated through simulation models in this section. The parameters of the simulated system are listed in Table III.

TABLE III PARAMETERS OF SIMULATED SYSTEM

PARAMETERS	Value
DC-link voltage U_{dc}	600 V
Nominal capacitor voltage	200 V
dc-link capacitance $C3=C2=C1$	2 mF
Fundamental frequency f_0	50 Hz
Carrier frequency f_{sw}	5 kHz
Minimum dwell time T_{DT}	4 μs
Load current	15 Arms at $M = 1.15$

A. Controllability

Firstly, the steady-state simulation waveforms of the proposed RLM are presented in Fig. 8, which shows that the proposed RLM can well balance the C2 voltage in both a low modulation index (0.5) and a full modulation index (1.15).

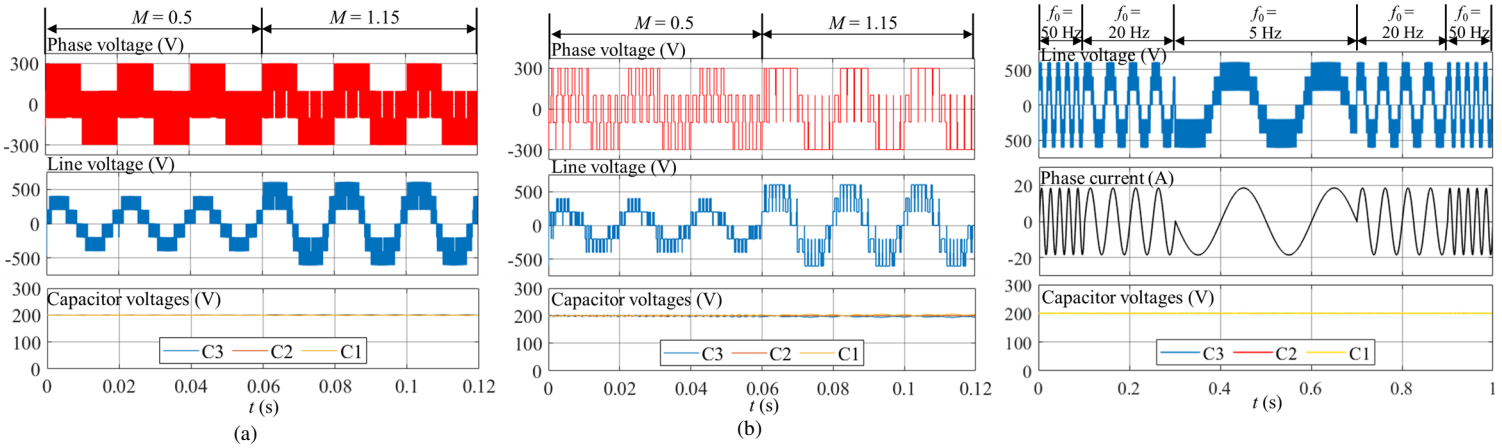


Fig. 8 Simulation waveforms with RLM (Scheme 1) at different carrier frequencies f_0 = 50 Hz, $cos\ \varphi$ = 1 (a) f_{sw} = 5 kHz (a) f_{sw} = 500 Hz

Fig. 9 Simulation waveforms with Scheme 2 at various fundamental frequencies f_{sw} = 5 kHz, $cos\ \varphi$ = 1, M = 1

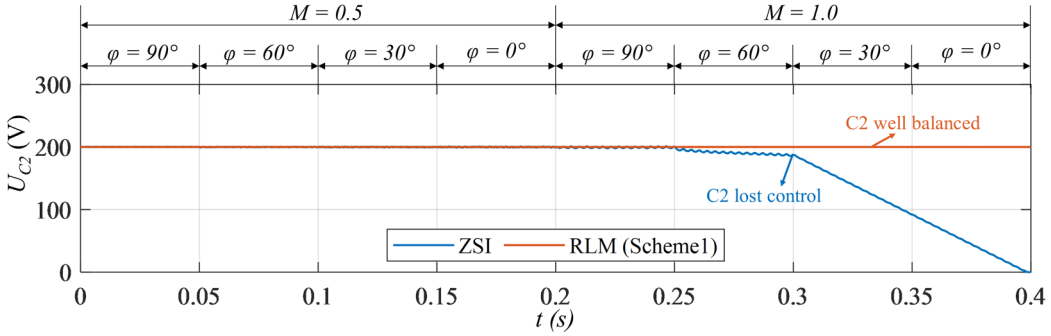


Fig. 10 Comparison of voltage balancing capability of conventional ZSI and proposed RLM against various modulation indexes and power factor angle φ

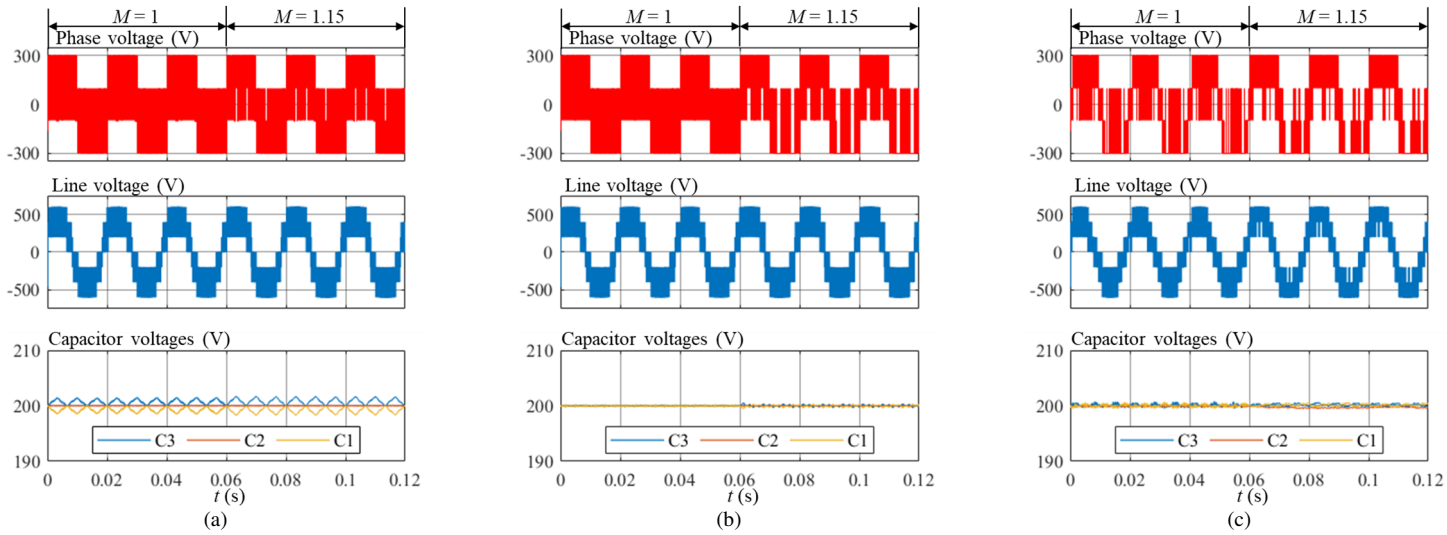


Fig. 11. Simulation waveforms with modulation index M stepped from 1 to 1.15 with $cos\ \varphi$ = 1 (a) Scheme 1 (b) Scheme 2 (c) Scheme 3

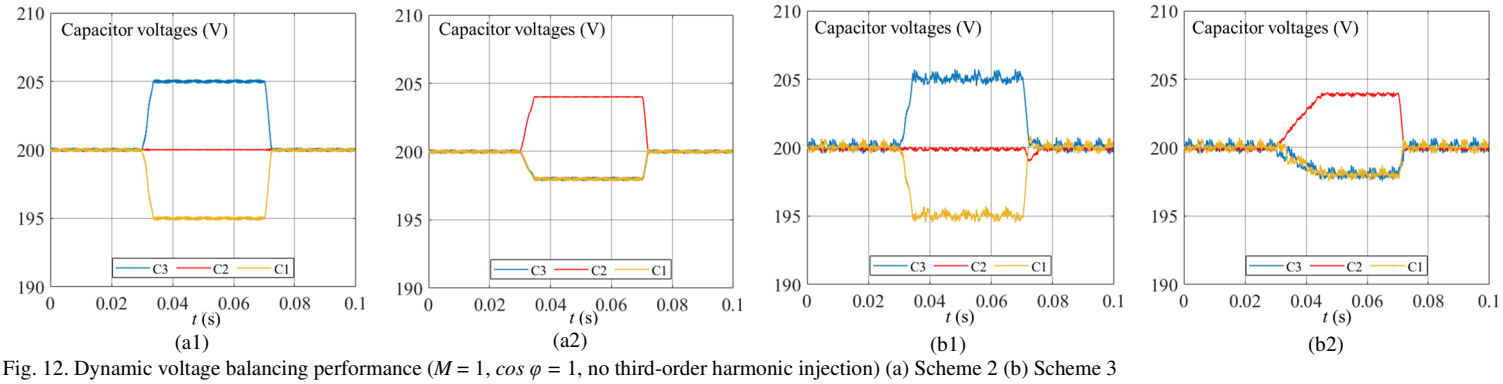


Fig. 12. Dynamic voltage balancing performance (M = 1, $cos\ \varphi$ = 1, no third-order harmonic injection) (a) Scheme 2 (b) Scheme 3

To verify the proposed scheme at a low switching frequency, f_{sw} is lowered to only ten times of the f_0 in Fig. 8(b), and it can be clearly seen that the phase output voltage shows the RLM pattern as intended in Fig. 3 with C2 voltage well controlled.

Fig. 9 shows the dynamic performance of the proposed scheme when the output frequency f_0 varies (e.g. in a variable frequency drive). At a high M and a high PF, the control algorithm is still effective when f_0 is lowered to 5 Hz.

To verify the effectiveness of the proposed approach over various power factor angles, Fig. 10 shows the capacitor C2 voltage waveforms under proposed RLM scheme in various cases with a comparison to the conventional ZSI approach. As Fig. 10 shows, the conventional ZSI approach can still balance the C2 voltage at the whole PF range with a low M, while it loses the controllability at a high PF with a high M. This finding is consistent with the theoretical analysis presented in [1]. In contrast, the proposed RLM scheme is verified to fulfill the control objective throughout the whole span of modulation indexes and power factors.

To verify the further optimized Scheme 2 and 3, Fig. 11 shows the simulation waveforms with the M stepped from 1 to 1.15. It can be seen that all three schemes can successfully balance the middle capacitor voltage, which enables this single-end four-level topology to function normally. As shown in Fig. 11(a), Scheme 1 leads to a low-frequency oscillation of the outer capacitor (C1 and C3) voltages due to lack of a closed-loop control, although they are balanced naturally over fundamental cycles. All three capacitors are well balanced in Scheme 2 and 3 as shown in Fig. 11(b)(c). It is visible that the overlap periods in the phase voltage waveform is less in Fig. 11(c) due to the intermittent use of RLM by design. Fig. 12 shows the dynamic voltage balancing performance comparing Scheme 2 and 3 with stepped references are given for three capacitor voltages. It can be seen that both schemes offer the decoupled closed-loop control for three capacitor voltages at the full modulation index. It is noticeable that Fig. 12(b) shows a slower and less smooth dynamic performance compared to Fig. 12(a), because in Scheme 3 only one phase utilizes RLM while the ZSI step attempting to cope with two control objectives at the same time. Compared to Scheme 2, Scheme 3 trades off partial controllability for less switching transitions.

To summarize, the simulation results confirm the validity of all the proposed voltage balancing schemes over the full span of converter operating conditions, as demonstrated in Fig.8-11.

B. Count of switching transitions

In principle, activating RLM in three phases will increase the total switching transitions by 100%, which is the case for Scheme 1 and 2. If only one phase is in activation of RLM, the increase of switching transitions can be lowered to 33%. Therefore, this section compares the count of switching transitions across the proposed schemes, which are captured in simulations and plotted in Fig. 13 with reference to ideal SPWM case across various carrier frequencies. The results confirm that the ZSI + 3-ph RLM leads to doubled switching transitions, while the ZSI + 1-ph RLM only leads to a 33% increase. As shown in Table II, the existing methods in [10]–[13] all features the 3-ph RLM, which results in up to 100% increased switching transitions with reference to the ordinary SPWM. In contrast, the proposed Scheme 1 only activates RLM in one phase at a time, which lowers the increase to 33%.

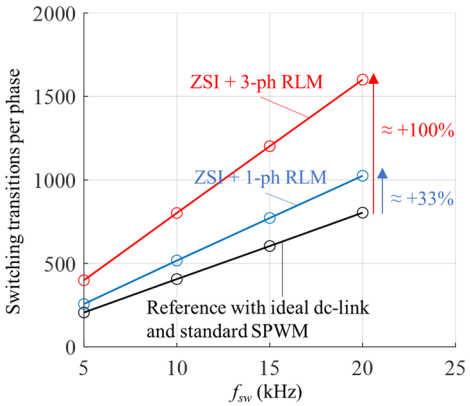


Fig. 13. Count of switching transitions over a fundamental cycle in a four-level π-type NPC inverter (M = 0.95).

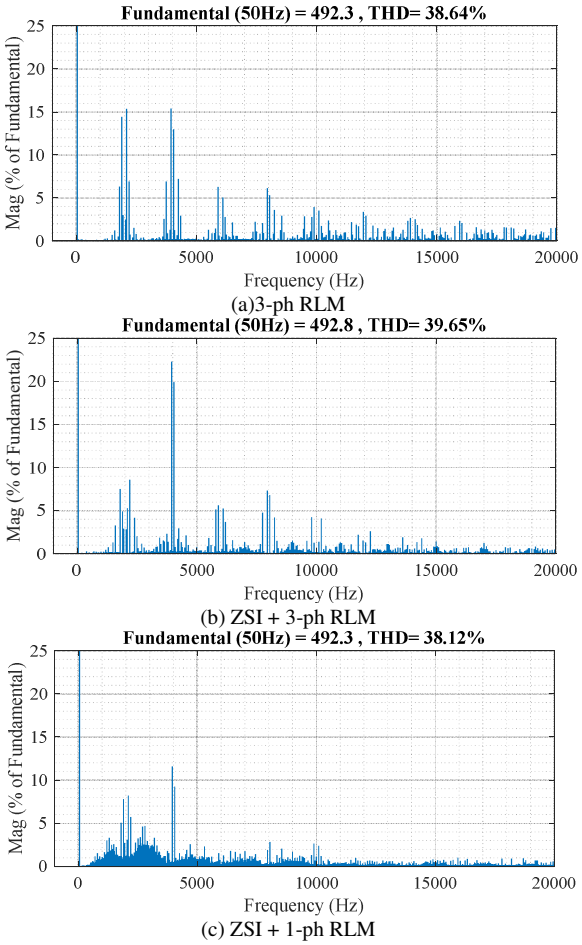


Fig. 14. FFT of converter output line-to-line voltage (M = 0.95).

C. Harmonics

FFT analysis is conducted to evaluate the harmonic performance of the proposed schemes. The results on the converter output line-to-line voltage are plotted in Fig. 14, with the carrier frequency lowered to 2 kHz for the ease of illustration with the Total Harmonic Distortion (THD) calculated up to 20 kHz.

The THD performance of the compared three schemes are very close, with the lowest value found in Scheme 3 in the studied case. In Scheme 1, the harmonic contents show 0.2% at

100 Hz (2nd), 0.17% at 200 Hz (4th) and 0.19% at 250 Hz (5th) due to the low-frequency oscillation in outer capacitor voltages. In Scheme 2 and 3, there are no significant low-order harmonics while the main harmonics are around the multiples of the switching frequency, which can be easily filtered out. Compared to Scheme 2, Scheme 3 features lower THD and lower harmonic amplitudes at multiples of the switching-frequency while it causes a spread over the spectrum and introduces lower-frequency harmonics (e.g. extends to half of the *f*sw). This effect is caused by the non-periodic behavior of Scheme 3 since each phase only operates with RLM intermittently over one fundamental cycle. In contrast, Scheme 2 operates all three phases constantly with the redundant levels.

To summarize, the three proposed schemes offer slightly different harmonic performances while they all successfully balance the middle capacitor voltage for the normal function of the topology. Scheme 1 features low-frequency harmonics due to the oscillation of the outer dc capacitor voltages which may require larger dc-link capacitors to attenuate. Scheme 2 features concentrated high-frequency harmonics around the multiples of carrier frequency. Scheme 3 features lower harmonic amplitudes at the multiples of carrier frequency, while it introduces lower-frequency harmonics. From the ac-side filter design point of view, the harmonics in Scheme 2 is relatively the easiest to be filtered out by high-frequency filters.

D. Summary

This section verified and quantifiably evaluated the performances of the proposed schemes. All the three proposed schemes can successfully balance the C2 voltage to enable the four-level topology to operate normally at all operating conditions. Among the three proposed schemes, Scheme 1 is the basic solution to control C2 in this topology, which is the easiest option to be reproduced in the controller prototyping. If the aim includes eliminating the low-frequency oscillation of U_{C3} and U_{C1}, both Scheme 2 and Scheme 3 can be applied, so that smaller dc-link capacitors can be used. Scheme 2 features smoother dynamic performance while it leads to concentrated high-frequency harmonics and higher switching losses compared to Scheme 3. If the switching loss is the main concern, Scheme 3 offers reduced switching transitions compared to Scheme 2, while it involves more control complexity and a spread of converter output harmonics.

V. Experimental Verification

A test rig is built to validate the proposed balancing schemes, with a picture of it presented in Fig. 15. The specifications of the test rig are shown in Table IV. The employed topology is a four-level π-type NPC that has been proposed in [3] with only six switches per phase leg.

TABLE IV SPECIFICATIONS OF THE TEST RIG

Topology	Three-phase four-level π-type NPC inverter
Fundamental frequency f_0	50 Hz
Switching frequency f_{sw}	5 kHz
dc-link voltage U_{dc}	120 V
dc-link capacitances	C3=C2=C1 = 1000 μF
R	22 Ω per phase
L	6.34 mH per phase

The control algorithm is implemented in a DSP, TMS320F28335. Operating at a power factor close to unity, the converter outputs a phase voltage U_a and load current I_a, which are captured and shown in Fig. 16 and Fig. 17. It can be seen that the capacitor voltage U_{c2} is well maintained at 40 V in two cases with full modulation index (M = 1 or 1.15) instead of getting

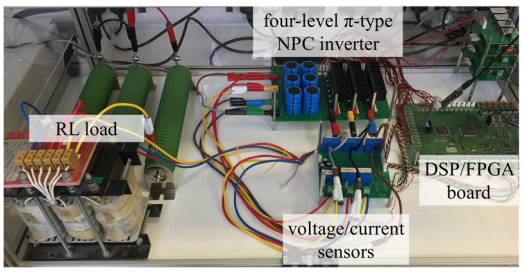


Fig. 15. Picture of the test rig.

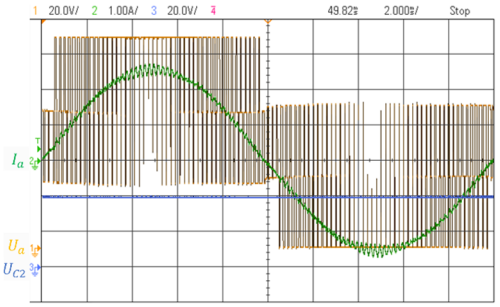


Fig. 16. Experimental waveforms with M = 1.

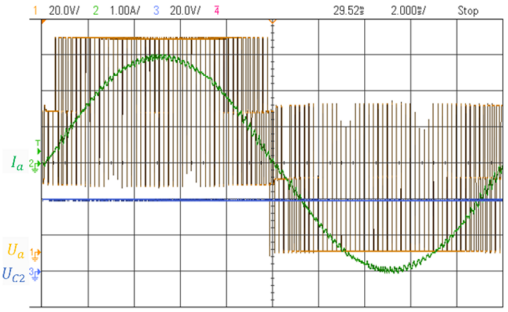


Fig. 17. Experimental waveforms with M = 1.15.

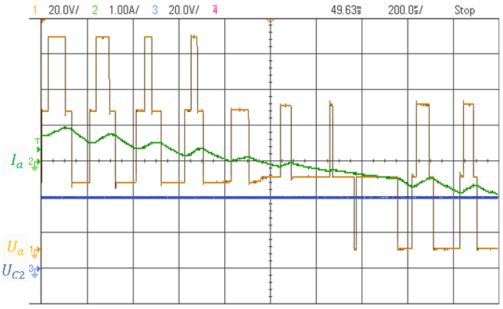


Fig. 18. Experimental waveforms (zoomed-in).

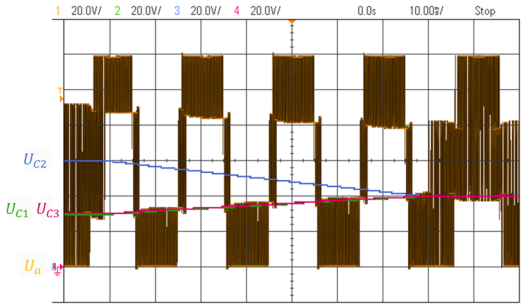


Fig. 19. Transitional capacitor voltages with a control command of U_{C2} stepped from 60V to 40V (M = 1).

fully discharged, while the converter outputs normal four-level voltages and sinusoidal currents with no visible low-order distortions. The effectiveness of the proposed schemes is also confirmed experimentally for the modulation index between 0 ~ 1 with a step of 0.1.

Fig. 18 shows a zoomed-in view of the converter behavior under the proposed voltage balancing scheme. It shows that the converter outputs three voltage levels in some of the switching cycles as intended by RLM, instead of two voltage levels.

Fig. 19 shows the closed-loop response of the system when a step command is given to U_{c2} to change from 60 V to 40 V. The U_{c2} well follows the command and stabilizes at 40 V after several fundamental cycles, with the outer two capacitors balanced also at 40 V. In summary, the experiments show that the proposed control algorithm works well at the worst case (M = 1 or 1.15 and a high power factor) without undermining the converter output voltage/capacity.

VI. Conclusion

This paper proposes a closed-loop voltage balancing algorithm for a four-level NPC converter, which is effective in a single-end configuration and full operating conditions. The proposed approach bases on Redundant Level Modulation (RLM) that introduces one additional voltage level in a switching cycle for the purpose of voltage balancing. An algorithm is proposed based on mathematical expressions and logical operations to dynamically solve the precise duty ratios from the measured unbalance of capacitors without involving mandatory PI/PID controllers. The algorithm is implemented through split modulating waves and regular level-shifted carriers that can be easily realized in DSPs. The closed-loop nature of the approach enables the balancing of any initial imbalance. The proposed schemes overcome the limitations in the conventional zero-sequence signal injection approaches.

The main drawback of the RLM approach is the additional switching transitions and associated increase of switching losses, which is the cost of the extra controllability. The proposed scheme is further improved by combining it with the zero-sequence signal injection approach, which features extended controllability and reduced switching transitions. The choice between the presented three balancing scheme variations depends on the design priorities concerning simplicity, device power loss and harmonic spectrums.

Simulations and experiments have confirmed that the proposed approach works well at the worst case, which is the full modulation index (M = *1 or 1.15*) and unity power factor. The proposed control algorithm enables the four-level NPC topology to be used as a single-end inverter with passive front ends at the full span of operating conditions.

References

[1] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 190–196, Feb. 2005.

[2] Kui Wang, Zedong Zheng, Lie Xu, and Yongdong Li, "A four-level hybrid-clamped converter with natural capacitor voltage balancing ability," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1152–1162, Mar. 2014.

[3] X. Yuan, "A four-level π-type converter for low-voltage applications," in *IEEE Proc. European Conference on Power Electronics and Applications*, 2015.

[4] B. Jin and X. Yuan, "Neutral points voltage balancing control of a four-level π-type converter," in *IEEE Proc. Energy Conversion Congress and Exposition*, 2016.

[5] B. Jin and X. Yuan, "Control of a four-level active neutral point clamped converter with neutral point voltage balance," in *IEEE Proc. International Conf. Power Electronics and Motion Control (ECCE Asia)*, 2016.

[6] B. Jin and X. Yuan, "Topology, efficiency analysis and control of a four-level π-type converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1044–1059, Jun. 2019.

[7] I. Lopez, S. Ceballos, and J. Pou, "Modulation strategy for multiphase neutral-point-clamped converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 928–941, 2016.

[8] J. Wang, X. Yuan, K. J. Dagan, and A. Bloor, "Optimal neutral point voltage balancing algorithm for three-phase three-level converters with hybrid zero-sequence signal injection and virtual zero-level modulation," *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 3865–3878, Apr. 2020.

[9] J. Pou *et al.*, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2288–2294, 2007.

[10] K. Wang, Z. Zheng, and Y. Li, "A novel carrier-overlapped PWM method for four-level neutral-point clamped converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 7–11, Jan. 2019.

[11] K. Wang, Z. Zheng, and Y. Li, "Topology and control of a four-Level ANPC inverter," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2342–2352, Mar. 2020.

[12] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A composite voltage balancing method for four-level NPC inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Dec. 2020.

[13] K. Wang, Z. Zheng, L. Xu, and Y. Li, "A generalized carrier-overlapped PWM method for neutral-point clamped multilevel converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9095–9106, Sep. 2020.

[14] S. Busquets-Monge, J. Bordonau, and J. Rocabert, "A virtual-vector pulsewidth modulation for the four-level diode-clamped DC–AC converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1964–1972, Jul. 2008.

[15] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1751–1758, 2008.

[16] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth modulations for the comprehensive capacitor voltage balance of n-level two-leg diode-clamped converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 8, pp. 1951–1959, 2009.

[17] S. Busquets-Monge, R. Maheshwari, and S. Munk-Nielsen, "Overmodulation of n-level three-leg DC-AC diode-clamped converters with comprehensive capacitor voltage balance," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1872–1883, 2013.

[18] S. Busquets-Monge, R. Grino, J. Nicolas-Apruzzese, and J. Bordonau, "Decoupled dc-Link capacitor voltage control of dc–ac multilevel multileg converters," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 3, pp. 1344–1349, 2016.

[19] S. Busquets-Monge, R. Maheshwari, J. Nicolas-Apruzzese, E. Lupon, S. Munk-Nielsen, and J. Bordonau, "Enhanced dc-Link capacitor voltage balancing control of dc-ac multilevel multileg converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2663–2672, 2015.

[20] S. Busquets-Monge, A. Filba-Martinez, S. Alepuz, and A. Calle-Prado, "A modulation strategy to operate multilevel multiphase diode-clamped and active-clamped dc-ac converters at low frequency modulation indices with dc-link capacitor voltage balance," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7521–7533, 2017.

[21] H. Tian and Y. W. Li, "Carrier-based stair edge PWM (SEPWM) for capacitor balancing in multilevel converters with floating capacitors," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3440–3452, 2018.

[22] J. Wang, X. Yuan, B. Jin, and I. Laird, "Closed-loop DC-link voltage balancing algorithm for a four-level π-type converter," in *Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2019.

[23] X. Yuan, Y. Li, and C. Wang, "Objective optimisation for multilevel neutral-point-clamped converters with zero-sequence signal control," *IET Power Electronics*, vol. 3, no. 5, pp. 755–763, 2010.

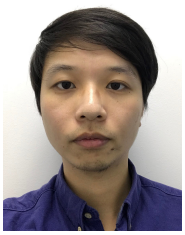
Jun Wang (S'17-M'19) received the B.S. degree from Sichuan University, Chengdu, China, the MSc degree from the University of Nottingham, UK, in 2014, and the Ph.D. degree from University of Bristol, UK, in 2019, all in electrical engineering.

He has been a Research Associate since 2019 with the Electrical Energy Management Group (EEMG) at the University of Bristol. His research interests include PWM power converters, multilevel dc/ac converter topologies, power loss modelling of power devices and magnetic components, design optimization and application of wide-bandgap devices.

Xibo Yuan (S'09-M'11-SM'15) received the B.S. degree from China University of Mining and Technology, Xuzhou, China, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2005 and 2010, respectively, both in electrical engineering.

He has been a Professor since 2017 in the Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, UK, where he became a Lecturer, Senior Lecturer and Reader in 2011, 2015 and 2016, respectively. He also holds the Royal Academy of Engineering/Safran Chair in Advanced Aircraft Power Generation Systems. He is an executive committee member of the UK National Centre for Power Electronics and the IET Power Electronics, Machines and Drives (PEMD) network.

His research interests include power electronics and motor drives, wind power generation, multilevel converters, application of wide-bandgap devices, electric vehicles and more electric aircraft technologies. Professor Yuan is an Associate Editor of IEEE Transactions on Industry Applications and IEEE Journal of Emerging and Selected Topics in Power Electronics. He a Fellow of IET and received The Isao Takahashi Power Electronics Award in 2018.



Bosen Jin received the B.S. degree from Northumbria University, Newcastle, UK, the MSc degree from University College London, London, UK, and the Ph.D degree from University of Bristol, UK, in 2012, 2013 and 2019, respectively, all in electrical engineering.

He is currently an R&D hardware engineer with Agilent Technologies Ltd., UK. His research interests include the multilevel converter topologies and controls, power loss modelling and analysis.