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Review

Evaluation of Quadrature Signal Generation Methods with Reduced Computational Resources for Grid Synchronization of Single-Phase Power Converters through Phase-Locked Loops

Paula Lamo [1,*], Alberto Pigazo [2] and Francisco J. Azcondo [3]

[1] Escuela Superior de Ingeniería y Tecnología, Universidad Internacional de La Rioja, 26006 Logroño, La Rioja, Spain
[2] Escuela Técnica Superior de Náutica, Universidad de Cantabria, 39005 Santander, Cantabria, Spain; pigazoa@unican.es
[3] Escuela Técnica Superior de Ingenieros Industriales y de Telecomunicación, Universidad de Cantabria, 39005 Santander, Cantabria, Spain; azcondof@unican.es
* Correspondence: paula.lamo@unir.net; Tel.: +34-941-21-02-11

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Abstract: Low-cost single-phase grid connected converters require synchronization with the grid voltage to obtain a better response and protection under diverse conditions, such as frequency perturbations and distortion. Phase-locked loops (PLLs) have been used in this scenario. This paper describes a set of quadrature signal generators for single-phase PLLs; compares the performances by means of simulation tests considering diverse operation conditions of the electrical grid; proposes strategies to reduce the computational burden, considering fixed-point digital implementations; and provides both descriptive and quantitative comparisons of the required mathematical operations and memory units for implementation of the analyzed single-phase PLLs.

Keywords: synchronization; phase-locked loop; PLL; computational burden; digital implementation; single-phase; low-cost; low-voltage

1. Introduction

In recent years, there has been a considerable increase in the presence of power converters in the electrical grid due to the diversification of sources, storage systems and loads as well as the fulfilment of the applicable standards [1]. Electrical grids are losing inertia [2], thus, the term grid-following converter used for stiff grids gives way to the term grid-forming converter for low inertia grids in which the control becomes more challenging to ensure the proper power quality indexes. Front-end power converters and smart transformers [3] are used to supply many electrical loads. Some relevant examples are the charging points for electric vehicles [4] and the power supply for railway transportation [5]. The raising of renewable generation such as photovoltaic [6] and wind [1] along with energy storage plants [7] also benefits from the power converter interfaces. The energy distribution systems also leverage their capabilities.

Even though the use of self-synchronized converters in certain applications, which eliminates the need for a dedicated synchronizer, results in a simpler and more robust controller [8], in most applications, the active synchronization enables complementary functions that go beyond the basic current control functions, e.g., providing a measure of grid frequency/voltage for anti-island methods [9,10]. This is where synchronization strategies, especially phase-locked loops (PLLs), can play a key role in improving the phase and, therefore, the current reference generation.

The synchronization circuit tracks the grid phase corresponding to the positive sequence fundamental of the voltage at the connection point and should maintain this synchronization during disturbances.

Modern active rectifiers connected to low-voltage (LV) grids avoid the diode rectification stage to increase the overall efficiency. Currently, it is necessary to take into account not only the power factor [11] but also the effect on the LV grid and neighboring loads, with the use of voltage/frequency regulation functions [12], ride-through capabilities [13], etc.

In this work, after the introduction, a classification of PLLs according to the generation technique of the phase reference is presented in Section 2. In Section 3, examination of the state of the art of PLLs with quadrature signal generation (QSG) used in single-phase power electronic converters is carried out. An in-depth study of the building blocks identifying the pros and cons of each of them is presented. Additionally, the strategies are evaluated in simulation using the Monte Carlo method, and its computational burden is compared at both descriptive and implementation levels considering a digital device with fixed-point arithmetic. Finally, the conclusions of the work are presented.

2. Principle of Operation and Types of PLLs

The PLL operates in closed-loop, generating an output signal around the center frequency in-phase with an input signal [14,15]. Once the PLL is locked, the circuit also tracks the grid frequency.

The basic structure of a PLL consists of three functional blocks [15], as seen in Figure 1: a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO) [16]. The phase detector compares the phase of the PLL with that of the grid, providing an error signal, ε, whose direct current (DC) component corresponds to the phase error. The filter attenuates other frequency components present in that error signal, which is carried out usually through a first-order low-pass filter. The LF output, $\Delta\omega'$, provides an estimation of the frequency deviation of the PLL from its nominal oscillation frequency, ω_0, which allows the VCO to generate a periodic signal of frequency $\omega' = \omega_0 + \Delta\omega'$, typically a sinusoidal one in grid-connected power converters. When the PLL is locked, it is in-phase with the grid voltage ($\theta' \approx \theta$) and provides a frequency estimation, ω', approximately matching that of the grid ($\omega' \approx \omega$).

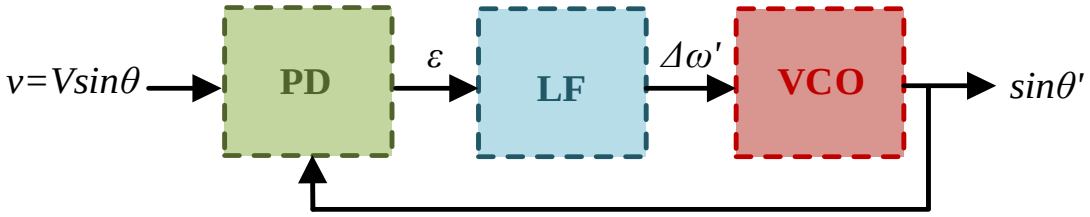


Figure 1. Basic structure of a phase-locked loop (PLL).

The definitions of the LF and VCO transfer functions, LF (z) and VCO (z), depend on the design goals of the PLL and the application in which it is used.

The response time, overshooting and the steady-state error of the PLL depend on the characteristics of the selected functional blocks as well as the effect of noise, disturbances and events in the electrical grid [17] that modify the waveform of the grid voltage.

Although a zero-order LF is the simplest approach, it is unable to follow phase ramps or frequency variations [17]. First-order LFs achieve monitoring of the grid phase during slow-frequency variation events, thus, they are very widespread in synchronization of grid-connected converters [1]. On the other hand, higher-order LFs are capable of tracking grid frequency variations, and they are especially interesting to attenuate harmonics. This is the case of [18–20], where a second-order LF is used to withstand large variations in voltage and frequency. Similarly, adaptive filters have also been embedded within the PLL structure to filter out the harmonic distortion. An example of this type of implementation is shown in [20], where the design of an adaptive comb filter with an even-order

harmonic filtering capacity is proposed. While in [21], the implementation of several adaptive notch filters is proposed. These techniques slightly affect the dynamic response of the PLL and significantly increase the associated computational burden.

The VCO generates the periodic signal used by the phase detector. In analog PLLs, this block is a dedicated circuit controlled by the output voltage of the LF [3], but in the digital versions used in current power electronic converters, the controlled oscillator is realized with look-up tables (LUTs), the coordinate rotation digital computer (CORDIC) or the digitally controlled oscillator (DCO). The LUTs, as in [22], occupy large memory resources either implemented in a field-programmable gate array (FPGA) or in digital signal processors (DSP). The use of CORDIC algorithms [23] adds complexity and slows down the execution of PLL circuits. This solution increases the precision obtained compared with the LUTs in return for increasing the computational burden of the system. In [24], the use of CORDIC algorithms is proposed to implement different mathematical functions in addition to the sine and cosine of the phase estimated by the PLL. While [25] uses a scheme that combines CORDIC and the LUT which, due to the symmetric characteristic of the sine and cosine function, only the information of a quarter of a period is included. Moreover, in [26,27], DCOs are implemented in a fixed-point DSP. As an example, in Figure 2, the structure of the proposed DCO is presented.

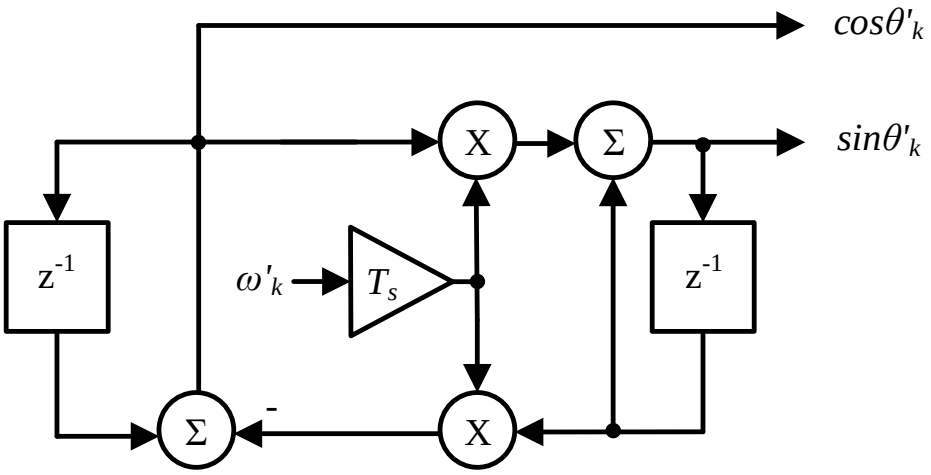


Figure 2. Implementation of the digitally controlled oscillator (DCO) proposed in [27].

Considering the operation principle of the phase detector (PD), PLLs are classified into three categories [1]: enhanced PLLs (EPLLs), power-based PLLs (pPLLs) and PLLs with quadrature signal generation (QSG PLLs). The EPLL [28] is based on an adaptive LF, which reconstructs the input signal by estimating the amplitude and phase angle provided by the VCO of the PLL [29]. The EPLL has the handicap of introducing a $\pi/2$ phase shift [30]. The PDs of the pPLLs using the pq theory [31] are designed for three-phase systems. However, it is possible to implement them in single phase PLLs with active filters [32–34]. The output signal of these PDs in pPLLs has a term around 2ω, which is difficult to filter with the LF, causing oscillations in the phase error signal. Additionally, certain controllers in converters connected to the grid require information on the voltage amplitude and, in pPLLs, this is not directly available. The effect of the 2ω term at the PD output on the behavior of the first-order LF can be reduced by adopting a PD that cancels that oscillatory term and shifts the PD ripple to a higher frequency. Such is the case of PLLs based on the Park transformation. This block is widely adopted due to its balance between simplicity and performance when the electrical grid corresponds to a balanced three-phase system in a sinusoidal operating regime. Since the Park transformation requires three-phase signals or their representation in the complex stationary reference frame through the Clarke transformation, in the case of single-phase power converters, a QSG is used to generate the β_k signal from the grid voltage signal (it is considered as α_k, and the homopolar component is set to zero). There are different ways to build the QSG. The most commonly used are described below.

Table 1 compares the computational burden and the dynamics of the functional blocks analyzed in this section.

Table 1. Summary of building blocks of the PLLs.

Functional Blocks	Type	Computational Burden	Dynamics
PD	EPLL [29,30]	Medium	Performance issues due to the $\pi/2$ phase shift
	pPLL [31,32]	Medium	Oscillations of the phase error signal
	QSG PLL	Depend on the selected strategy (see next section)	
LF	Zero order [17]	Low	Performance issues under phase ramps and frequency variations
	First order [1]	Low	Good under slow variations in the grid frequency
	High order [19,20]	Medium–High	Good
	Adaptive [21,22]	High	Good
VCO	LUTs [22]	High	Good
	CORDIC [24,25]	High	Good
	DCO [26]	Low	Good

3. PLLs Based on Park Transformation

The QSG in Figure 3 uses the samples of the grid voltage, v, to define the component in-phase, α, and in-quadrature, β, of the grid voltage phasor in a stationary complex reference frame. By introducing normalization, the amplitude dependency in tuning the proportional–integral (PI) controller is overcome. Then, α and β, through the Park transformation, are converted into a rotating reference frame, dq, which is synchronized with the grid, forcing the phase of the PLL, θ', to track that of the grid. This is ensured by the PI controller, whose input is the error signal $\epsilon = -q$. Under steady-state and pure sinusoidal conditions, the q component becomes approximately zero, with a certain ripple, when synchronization is achieved. The output of the PI controller provides an estimation of the frequency deviation, $\Delta\omega'$, from the central PLL frequency, $\omega_0 = 2\pi f_0$, giving rise to the estimation of the grid frequency ω'. In steady state, the result approximates the actual grid frequency, ω. The estimated phase of the grid voltage, θ', which is also used to calculate the functions and required in the Park transform, is obtained by integrating ω'. In some proposals, the estimated grid frequency, ω', is used to adjust the frequency response of the QSG by means of its feedback.

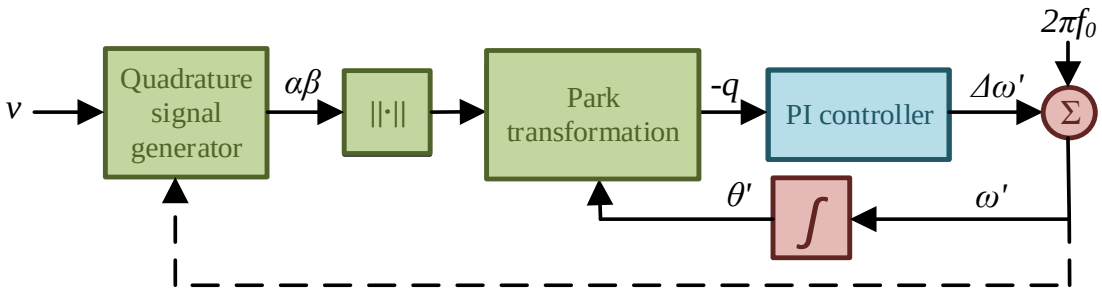


Figure 3. General structure of a single-phase synchronous reference frame (SRF) PLL.

3.1. Transport Delay PLL

The transport delay (TD) is one of the most common and probably the simplest method of QSG (Figure 4). It consists of generating the quadrature signal by means of a delay $D = round\left(\frac{T}{4T_s}\right)$ samples applied to the grid voltage, where T is the period of the fundamental grid voltage, thus, it manages to generate a periodic quadrature component by means of a memory buffer of constant length [1,35].

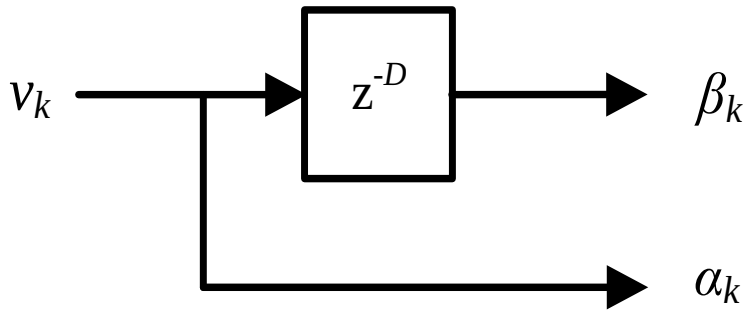


Figure 4. Discrete time representation of the QSG of the transport delay (TD) PLL.

This QSG works properly if the voltage is a pure sinusoidal signal with constant frequency equal to the nominal of the grid, f_0. Frequency variations produce a not-orthogonal quadrature signal and causes a phase error, and they reach the PD and lead to an error in the quantities detected in steady state [1].

The phase error can be partially compensated by a variable memory buffer [20]. However, this correction is not complete because the variable buffer does not consider the fractional variation of the frequency. In [36], it is recommended to consider both the integer, $D = round\left(\frac{\pi}{2\omega' T_s}\right)$, and fractional, $\frac{T}{4T_s} - D$, parts of the delay, using the Lagrange polynomial of M order to approximate the fractional lag. The precision of this approximation depends on the order of the interpolation polynomial and the sampling frequency. When the sample rate is high, the use of a low-order interpolation polynomial is enough. However, in the case of low sampling frequencies, the use of a high-order interpolation algorithm is necessary to obtain the same level of precision, which considerably increases the computational burden of the system.

An alternative approach to that proposed is the nonfrequency-dependent TD-PLL (NTD) [37], where the QSG structure of TD is maintained, but the effect of grid frequency variations is compensated through a delay of $T/4$, which replaces one of the trigonometric functions in the Park transform. This modification increases memory requirements but reduces overall complexity by employing only one trigonometric function and corrects for offset errors in the TD PLL.

In [38], an adaptive TD PLL is proposed. The orthogonal version of the single-phase signal under frequency deviations can be generated as

$$\beta(t) = \frac{V_g(t - T/4) + V_g(t)\sin(\Delta\omega'_k T/4)}{\cos(\Delta\omega'_k T/4)}. \quad (1)$$

With this strategy, the orthogonal signal can be generated even in environments with frequency variations with a fixed length delay.

A different strategy is given in [39], where compensation is applied to the PLL output, by adding/subtracting a compensation phase, $\theta_{comp}^{'(\omega'_k)}$, which depends on the integral action of the PI controller, $\Delta\omega'_k$.

$$\theta_{comp}^{'(\omega'_k)} = -\frac{T}{8}\Delta\omega'_k \quad (2)$$

3.2. PLL Based on Inverse Park Transformation

Voltage or current representations in the stationary reference frame, i.e., $\alpha\beta$ coordinates, can be transformed to a rotating frame of reference, dq, through the Park transformation [1]. The inverse transformation is given by

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos(\gamma) & -\sin(\gamma) \\ \sin(\gamma) & \cos(\gamma) \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{3}$$

where γ is the angle of rotation of the axes dq referred to axes $\alpha\beta$.

In PLLs based on the inverse Park transformation (IPT PLL) [40], the orthogonal signal is generated by applying (3) to the output of the PD once filtered out [41,42]. Guidelines for the design and details of the IPT PLL analysis are presented in [37,43,44].

In [44,45], the PLL based on the multiharmonic decoupling cell (MHDC PLL) is proposed, where the QSG used is a combination of the TD and the IPT. With this configuration, the MHDC maintains the strength of a quadrature IPT system to attenuate the high-order harmonics at the input of the PLL, but it also inherits the delay effect of the PLL *T/4*, which makes it sensitive to frequency variations.

3.3. PLL Based on Synthesis Circuit

Synthesis circuit PLL (SC PLL) [46] is known as one of the simplest SRF PLLs [47]. This strategy constructs an orthogonal signal using the estimated amplitude and phase angle.

When it is necessary to extract the phase and amplitude of one or more harmonic components, or when the presence of harmonics at the input of the PLL degrades its performance, its structure can be extended to take into account the presence of harmonics [46]. In this sense, it must be considered that each additional harmonic requires an additional SC PLL, thus increasing the computational burden of the QSG.

3.4. PLL Based on Hilbert Transform

The Hilbert transform (HT) [1] is a mathematical tool that has two main characteristics. First, the phase angle of the spectral components of the input signal is shifted by ±90° as a function of its frequency, and second, it only affects the phase of the signal and has no effect on its amplitude.

The Hilbert transform of a generic signal $x(t)$ is defined as [40]:

$$X(t) = \frac{P}{\pi} \int_{-\infty}^{\infty} \frac{x(\tau)}{t-\tau} d\tau \tag{4}$$

where P indicates that the integral is a Cauchy principal value.

This technique allows the generation of an analytical signal from a real signal with unity gain, except for the DC component. The ideal Hilbert transform violates the property of causality and is therefore not feasible [41]. Because its frequency response stretches across the entire spectrum, digital realization requires an approximation. Three main approaches can be found in the literature [48,49]: complex filters, which require complex and computationally expensive hardware multipliers; the combination of two filters that form 90°, which are commonly implemented as delayed band-pass infinite impulse response (IIR) filters variables, which deteriorate PLL performance; and finite impulse response (FIR) filters, which require the real part to be delayed to adjust the relative phases of in-phase and quadrature signals. The latter approach is the preferred method for PLLs in grid-connected converters [40,41,50]. The type III and IV FIR filters can be applied as for the generation of the quadrature signal [51], but the necessary multiplications in type III are half those in type IV [49].

3.5. PLL Based on Signal Delay Compensation

Two delay buffers applied to the input voltage can be chained together (Figure 5), forming a configuration called delay signal compensation (DSC) [52] and obtaining the quadrature signal

at the output of the first delay block [37,53]. Its harmonic blocking capabilities can be enhanced by adding new DSC operators before the PD and compensating for the PLL output by adding a frequency-dependent phase. Therefore, the resources required for digital implementation increase.

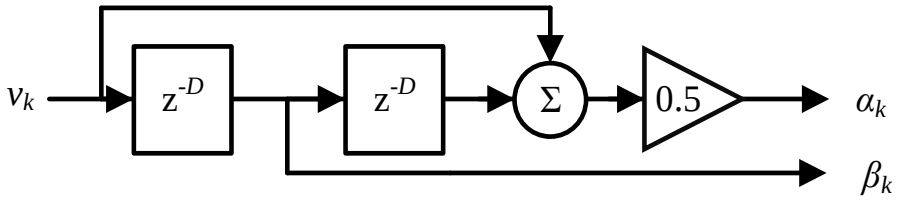


Figure 5. QSG with two delay buffers.

3.6. Derivative PLL

The PLL with generation of the quadrature signal based on a derivative block (D PLL) [54] has been widely used in the continuous domain [55]. Its digital implementation (Figure 6) produces a very precise result [56], although it requires a numerical approximation to the derived function, following one of the methods shown in Table 2, to reduce the effect of noise.

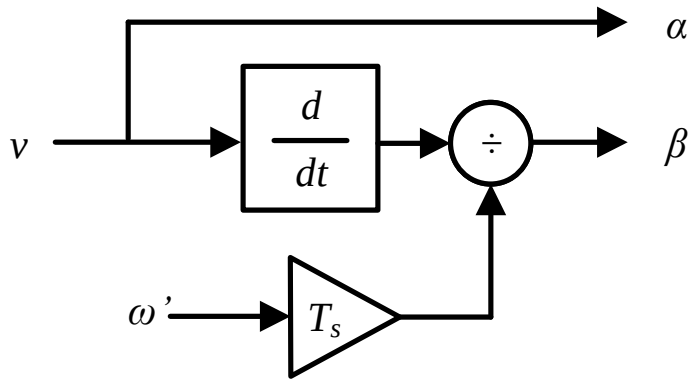


Figure 6. QSG of the derivative PLL.

Table 2. Approaches to the derived function.

Approach	α	$\beta=\frac{x'(t)}{\omega'}$
D-backward	$x(t)$	$\frac{1}{\omega'}\frac{x(t)-x(t-T_s)}{T_s}$
D-central difference	$x(t-T_s)$	$\frac{1}{\omega'}\frac{x(t+T_s)-x(t-T_s)}{2T_s}$
D-Richardson extrapolation	$x(t-2T_s)$	$\frac{1}{\omega'}\frac{-x(t+2T_s)+8x(t+T_s)-8x(t-T_s)+x(t-2T_s)}{12T_s}$

In order to reduce the noise that amplifies the calculation of the derived function, it is necessary to increase the number of samples, which, in addition, introduces a phase shift in the quadrature component. This effect can be compensated for by introducing delays in the in-phase component, while the resulting lag of the QSG must be compensated after the VCO.

3.7. PLL Based on Recursive Discrete Fourier Transform

In this technique, shown in Figure 7, the QSG uses the recursive discrete Fourier transform (RDFT) PLL [22,57]:

$$G_{RDFT}(z) = \frac{\left(1-z^{-D}\right)z^{-1}e^{\frac{j2\pi}{D}}}{1-e^{\frac{j2\pi}{D}}z^{-1}} \quad (5)$$

where D is the number of samples considered in each period of the grid, and by assigning $D = round\left(\frac{2\pi}{\omega' T_s}\right)$, the fundamental voltage is tracked and the harmonics rejected due to the zero-pole assignment across the unit circle.

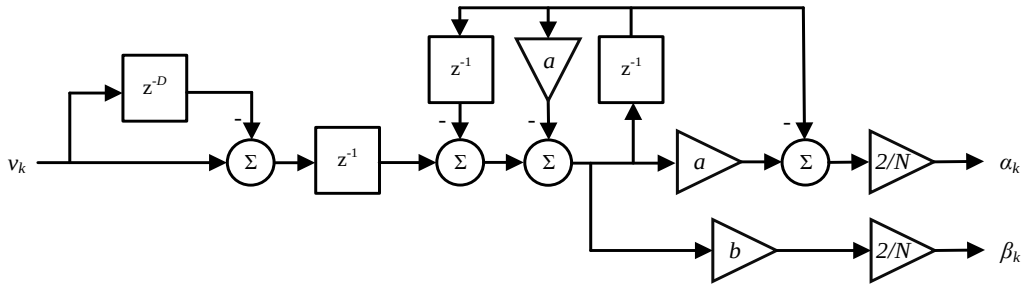


Figure 7. Quadrature signal generator with recursive discrete Fourier transform (RDFT) where $a = \cos(2\pi/N)$ and $b = \sin(2\pi/N)$.

The main drawback associated with this technique is the accumulated error produced by rounding, which can lead to instabilities [58]. This drawback can be mitigated by including a damping factor in the transfer function (5):

$$G_{RDFT}(z) = \frac{\left(1 - r^D z^{-D}\right) r z^{-1} e^{\frac{j2\pi}{D}}}{1 - r e^{\frac{j2\pi}{D}} z^{-1}} \tag{6}$$

where $r < 1$ is the damping factor. From the point of view of computational burden, this approach involves many operations and largely depends on the processor or digital circuit used [58]. A fixed sampling frequency, under grid frequency variations, results in errors and oscillations in the PLL phase and a poor attenuation of harmonics in the input signal. Several solutions are possible, and the simplest is to adjust the sampling frequency according to the fundamental frequency variations so that N remains constant. However, the use of a variable sample rate may not be feasible in the application where the PLL is used. In [59], it is proposed to improve the response of the algorithm to frequency variations by redesigning it with the use of a variable sampling frequency.

3.8. PLL Based on Kalman Filtering

The real-time application of linear Kalman filters (KF) [60] estimates the state variables ($\mathbf{x}_k$) of a linear system by weighting the information from the system measurement equation (in the vector $\mathbf{s}_k$) and the previous states of the system and its inputs ($\mathbf{x}_k$, $\mathbf{u}_k$) through the filter gains, known as Kalman gains, which are also updated at each sampling interval as a function of the evolution of the estimation error. The equations of state and measure of the system are written as

$$\begin{cases} \mathbf{x}_{k+1} = \mathbf{A}_k \mathbf{x}_k + \mathbf{B}_k \mathbf{u}_k + \Gamma \xi_k \\ \mathbf{s}_k = \mathbf{C}_k \mathbf{x}_k + \mathbf{D}_k \mathbf{u}_k + \eta_k \end{cases} \tag{7}$$

where ξ and η are noncorrelated noise sequences with normal probability distributions, $\mathbf{A}_k$ and $\mathbf{C}_k$ are the state and measurement transition matrices, respectively, and $\mathbf{u}_k$ is a deterministic input sequence, which, in the case of application to the QSG of PLLs, can be avoided [61]. The recursive version of the Kalman filter reduces the computational load of the method, and if the model of the signals corresponds to a stochastic linear system and invariant in time, the structure of the recursive filter loop is further simplified, resulting in the so called limiting Kalman filter (LKF).

In [62], the approach used is a LKF that models the fundamental grid frequency. The recursive filter for LKF performs the estimation of the state variables and their update based on the error from the comparison of the measurement and the state estimated. A greater number of states, due to a more complex signal model, results in the use of a greater number of registers and multiplications. On the other hand, with the defined signal model, in the LKF, the values of the Kalman gains can be precalculated

and stored in memory registers for use in the modified recursive loop. Therefore, the computational burden reduction in the system is significant.

3.9. PLL Based on Second-Order Generalized Integrator

The PLL based on the second-order generalized integrator (SOGI PLL) [29,35] uses an adaptive filter to improve the generation of the quadrature signal. First, the SOGI structure generates the quadrature signal of the fundamental of the grid voltage by using an integrator and, second, its structure eliminates unwanted frequency components, harmonics, from the output signals α_k and β_k. The block diagram of this QSG is shown in Figure 8, where the use of ω'_k allows the QSG to follow the fundamental of the grid voltage.

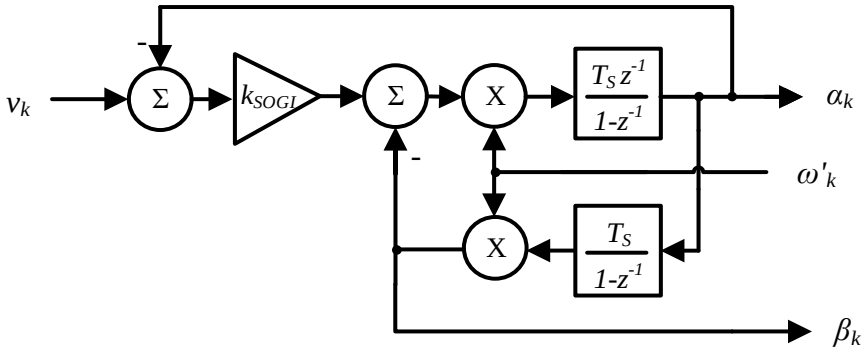


Figure 8. Block diagram of the QSG second-order generalized integrator (SOGI).

There are many variants that can be found of this QSG in the literature. In [63–65], the SOGI PLL is included within an active filter structure for the generation of the quadrature signal in single-phase SRF PLLs. In [65], it is shown that the IPT and the SOGI are equivalent under certain conditions. From an implementation point of view, the SOGI proposed in [65–67] has a minimum resource demand applying a constant $\omega'_k = \omega_0$. However, in this case, the structure is very sensitive to the frequency oscillations of the PLL due to the PD and LF used. In order to overcome these limitations, the SOGI can be combined with an FLL providing the resonant frequency and avoiding the PLL stage [1].

One drawback of this strategy is that it does not block a DC component, which give rise to errors in the output signals if they are present in the input signal. SOGI–QSG structures have been proposed in the literature that, by adding one or more zeros at the origin [67–74], prevent this effect. Attempts have also been made to improve the harmonic filtering capacity of the PLL from a closed loop feedback system [69], especially in floating arithmetic applications, with the design of a pre-filter [73] and with a structure of multiple generalized second-order integrators and an FLL [75] that reduces the computation time and obtains an algorithm with low computational burden.

3.10. PLL Based on First-Order All-Pass Filters

The first-order all-pass filter (APF) PLLs are easy to implement to create the fictitious orthogonal signal [39,76–78].

The first-order filter used in this method has the transfer function:

$$APF(z) = \frac{c - z^{-1}}{1 + cz^{-1}} \tag{8}$$

where $c = \frac{1-tan(\omega'_k T_s/2)}{1+tan(\omega'_k T_s/2)}$.

The use of APFs (Figure 9) to create the quadrature signal is not limited to first-order filters. In fact, higher-order APFs can also be used as in [39], where a second-order APF is proposed, although this implies an increase in computational burden.

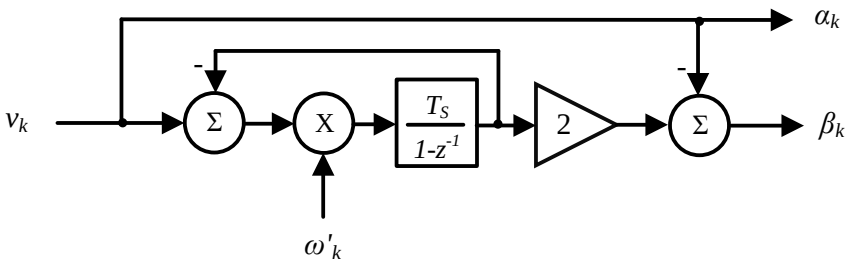


Figure 9. Diagram of the first-order APF PLL.

In APFs, it is not necessary to adapt to frequency [78]. However, a compensator is often necessary at the output of the PLL to correct the phase error. In this sense, three possible topologies to generate the quadrature signal using a nonadaptive APF are discussed in [78].

3.11. PLL Based on Two-Sample

This strategy generates the quadrature signal from a buffer of two samples (2S) by applying finite differences around the operating point that can be dynamically adjusted as a function of the grid frequency ω'_k, estimated by the PLL [79]. As a result, the quadrature signal at each instant k is generated with three consecutive samples of the grid voltage. Few memory resources are required. The 2S-QSG is obtained from

$$\beta_k = (\alpha_{k-2} - \alpha_k)\frac{1}{sin\left(\frac{4\pi}{N_k}\right)} + \alpha_k tan\left(\frac{2\pi}{N_k}\right) \tag{9}$$

where N_k can be obtained either dynamically or taken as a fixed value.

The implementation of the 2S-QSG requires low computational burden. Furthermore, a simplification of its algorithm has been proposed, starting from the first term of the Taylor series of trigonometric functions and assuming a high sampling frequency [79], as well as the elimination of the division operation and the use of digital oscillators such as VCO [27]. A handicap of this strategy is its low immunity to noise and harmonic distortion of the voltage, which has been solved in [80], including an adaptive filter in its structure.

3.12. Evaluation

Fixed-point implementations of the QSGs versions analyzed in this section, not including complex functions such as trigonometric ones, are included in the structure of a PLL and evaluated by means of a Monte Carlo (MC) tests using MATLAB/Simulink®. These strategies are SOGI [65], DSC [37], 2S [79], *T/4* [1], LKF [62], IPT [40], APF [39] and D-backward. The same PD, LF (K_p = 15.33 and K_i = 117.56) and VCO are used in all the cases, according to Figure 10. The sampling period, T_s, is 160 µs.

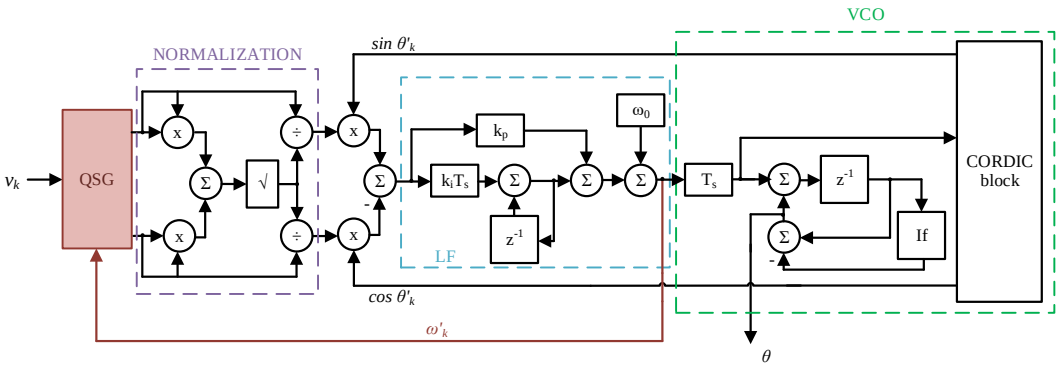
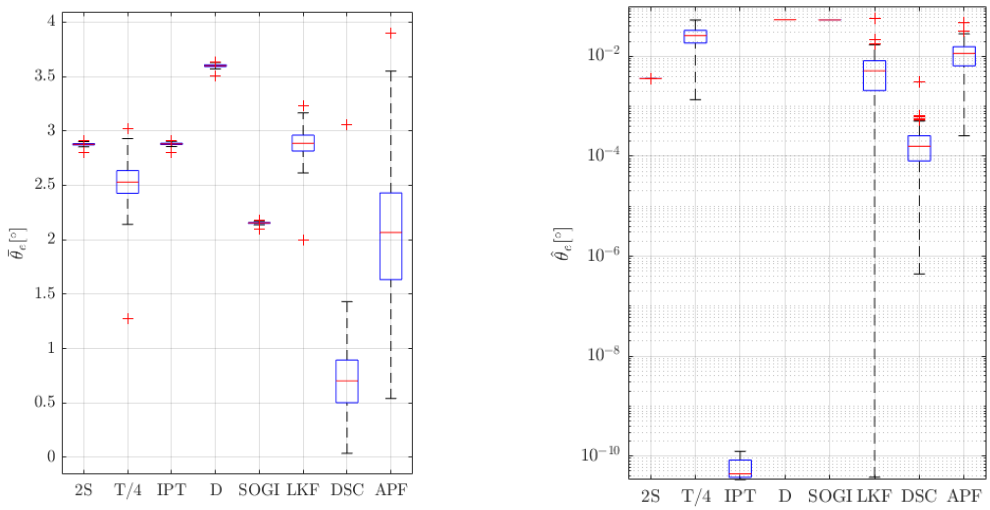


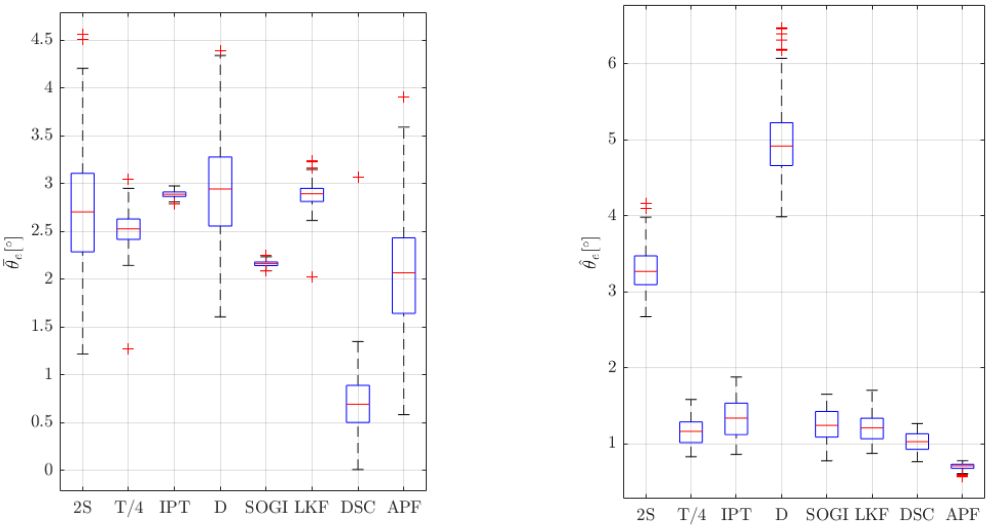
Figure 10. Structure of the PLL used in the tests.

The MC tests consider ideal (Figure 11 and Figures 13–15) and harmonically distorted grid voltages (Figure 12) within the limits stablished in EN 50160 [81] and other effects due to the measure chain, such as noise (band-limited white noise whose noise power is 5 ppm) and DC component (2%). A total of 250 simulation conditions are generated through Latin hypercube sampling (LHS), which reduces the representative number of MC tests. Voltage harmonic combinations, with orders from 2nd to 50th and amplitudes within the individual and collective limits in EN 50160 ($V_{THD} \leq 8\%$), are considered. Results are presented according to a uniform probability density function (PDF). The nominal grid frequency changes in the test following a normal PDF, in the range from 47 up to 52 Hz.



(**a**) (**b**)

Figure 11. Results of Monte Carlo (MC) tests in steady state. Grid voltage and the nominal grid frequency are combined through Latin hypercube sampling (LHS). (**a**) Mean phase error and (**b**) Ripple of the phase error.



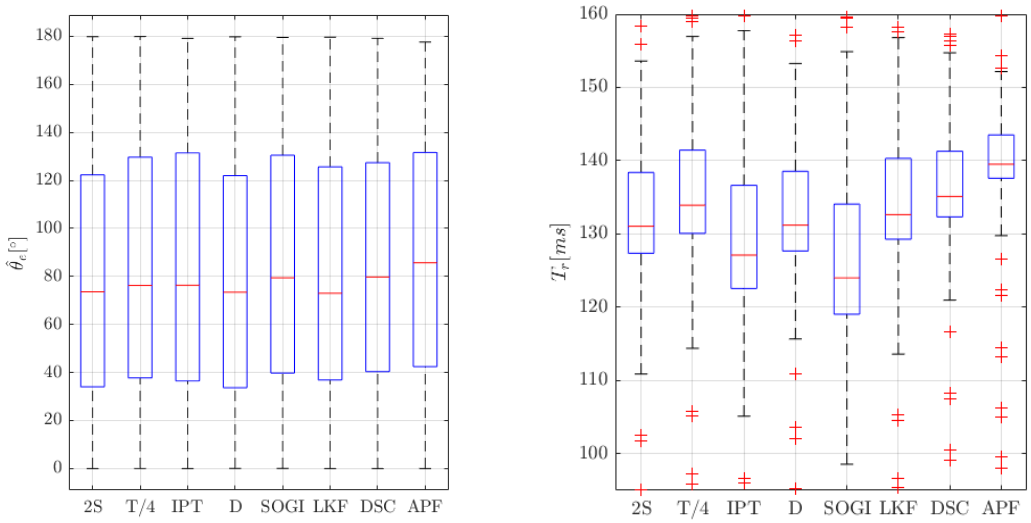
(**a**) (**b**)

Figure 12. Results of MC tests in steady state. Harmonic distortion of the grid voltage and the nominal grid frequency are combined through LHS. (**a**) Mean phase error and (**b**) Ripple of the phase error.

The resulting PDFs for the measured mean phase error ($\overline{\theta_e}$) in steady state are shown in Figure 11a. The PDFs obtained in this test for the D PLL are higher with a median equal to 3.6°. The best results are obtained with the DCS PLL with 0.7° median. The measured phase error ripple ($\hat{\theta}_e$) under the same steady state test is shown in Figure 11b, where the ripples with the D and SOGI are equivalent and with medians equal to 0.55°. Meanwhile, the IPTs present the lower results with lower errors by eight orders of magnitude. However, the strategy that performs the best during steady state, considering Figure 11, is the DSC PLL.

The resulting PDFs for the $\overline{\theta_e}$ in steady state under harmonic distortion is shown in Figure 12a. The PDF for the D PLL obtained in this test is again the highest, with a median 3.9° and an 8° variance. The best results are obtained with the DCS PLL with which the median is 0.7° and variance 0.4°. The measured $\hat{\theta}_e$ under the same test is shown in Figure 12b, where the ripple with the D PLL is the worst with a median of 5.9°. Meanwhile, the APF presents the lower results with a median of 0.6°. The response time of θ_e is measured from the step beginning to the time instant where θ_e reaches a 3% of the peak θ_e. The strategies that achieve the best response times considering both figures are DSC and APF.

The response to frequency jumps has been evaluated combining the steady-state MC conditions with different starting phases and magnitudes, in the range of 0–360° and −5–5 Hz, and assuming uniform PDFs; the results are shown in Figure 12. The lower median of the overshoot PDFs (Figure 13a) is obtained by LKF (75°), while the medians of the APF and SOGI are higher with 85° and 80°, respectively. The PDFs of the response times are shown in Figure 13b, where high-performance differences are observed. In terms of response time, the best performer is the SOGI, achieving 124 ms as median. The worst performer is the APF again (median and variance equal 140 and 7 ms, respectively).

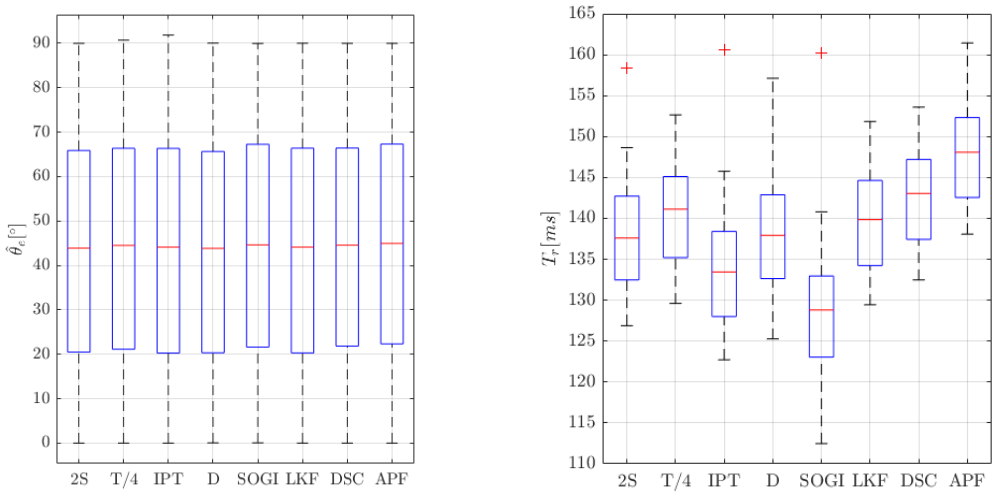


(**a**) (**b**)

Figure 13. Results of MC tests with frequency jumps. Starting phase angle and jump magnitude are varied through LHS. (**a**) Overshoot of the phase errors and (**b**) response times.

Figure 14 shows the obtained results in the case of phase jumps. The magnitude of the jumps is uniformly distributed in the range of −90–+90°, and the starting point is applied at different phase instants in the range of 0–360°. Again, LHS is used to combine these conditions with those of the steady-state test. The PDFs of the measured overshoots and response times in the phase errors after the transient are shown in Figure 14a,b, respectively. Among all the other evaluated QSGs, the best balance of overshoot and response time is due to the SOGI (median of overshoot and response time are

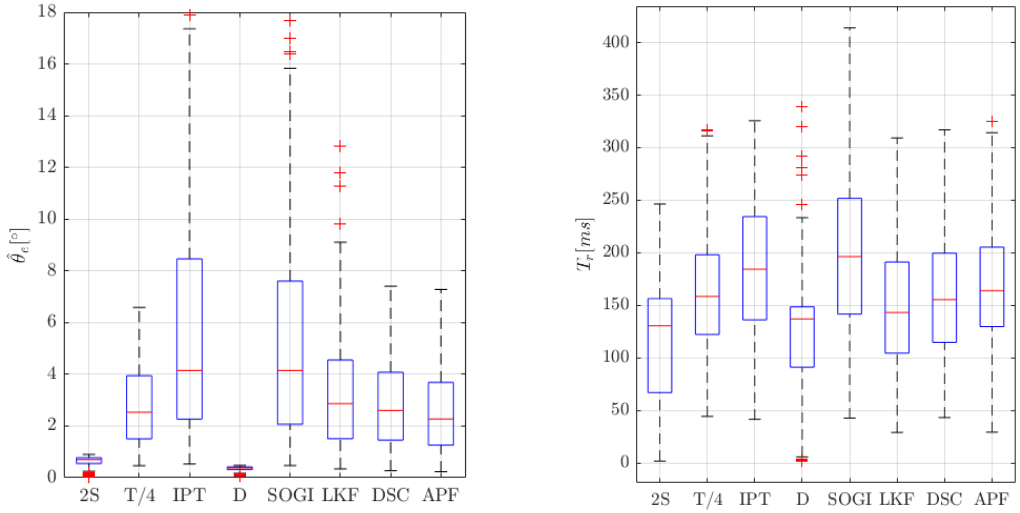
45° and 128 ms, respectively), and the worst is APF (median of overshoot and response time are 46° and 147 ms, respectively).



(**a**) (**b**)

Figure 14. Results of MC tests with phase jumps. Starting phase angle and jump magnitude are varied through LHS. (**a**) Overshoot of the peak phase error and (**b**) response times.

The performance of the 2S PLLs in case of voltage dips was also analyzed. Steady-state test conditions were combined through LHS with different voltage dip depths, in the range of 20–90%, durations in the range of 10–200 ms and initial phases of 0–360°. The dynamics of the PLLs are evaluated in the falling down transient. The overshoot of the phase error is shown in Figure 15a, where the performance of the SOGI and IPT present the higher results with medians of 4.3°. Besides, the PDFs of the measured response times are shown in Figure 15b, and the largest median corresponds to SOGI (119 ms). However, the best performance under voltage dips in general terms is obtained by the D PLL.



(**a**) (**b**)

Figure 15. Results of MC tests with voltage dips. Starting phase angle, dip depth and duration are varied through LHS. (**a**) Overshoot of the peak phase error and (**b**) response times.

For comparison purposes, Table 3 summarizes the number of operations and memory units required for the digital implementation of the equivalent blocks of QSG in single-phase PLLs, described in Sections 2 and 3. Initially, the originally proposed structures (such as SOGI [65], *T/4* [1], DSC [37] or D-Backward) are simple. However, the successive proposals presented in the literature to improve its behavior under grid disturbances increase its computational burden and the complexity of the circuit (for example, in the case of multiSOGI structure (MSOGI) [75], *T/4* [39], DSC + filter [53] or D-Richardson). On the other hand, the memory registers depend on the sampling frequency used in the circuit (such as the proposals based on *T/4*) or the number of blocks implemented to eliminate harmonics from the grid voltage (like 2S + filter [80] or the MSOGI [75]). This is why the designer must balance the need to comply with the computational burden and timing requirements in its system and the behavior of the strategy under grid disturbances that is required.

Table 3. Number of operations and memory units required for the digital implementation.

QSG	+/−	×/÷	*T*	*M*
SOGI [65]	4	3	0	2
MSOGI [75]	1 + 6*F*	4*F*	0	2*F*
DSC [37]	1	1	0	2 × round(*N*/4)
DSC + filter [53]	10	23	6	16 × round(*N*)
2S [79]	2	3	0	2
2S + filter [80]	3 + 3*F*	3 + 4*F*	0	2 + 3*F*
T/4 [1]	0	0	0	round(*N*/4)
Recent *T/4* [39]	1	1	0	round(*N*/4)
KF [60]	407	349	6	0
LKF [62]	8	13	0	0
IPT [40]	6	7	0	6
MHDC [44,45]	9	12	2	9
SC [46]	2	3	1	1
HT [1]	5	3	0	10
APF [39,76]	2	2	0	2
D-backward	1	1	0	1
D-central difference	1	1	0	5
D-Richardson extrapolation	3	2	0	14
RDFT [22]	4	5	0	*N* + 3
pq theory [31]	3	4	1	1
Enhanced [28]	2	5	2	1

×/÷ = gains, multiplications and divisions, ***T*** = trigonometric functions, ***M*** = data memory units, *F* = number of harmonic orders considered and $N = 2\pi/(\omega'_k Ts)$.

The synthesis of PLLs in an FPGA can be carried out through different methods. Designers have specific rapid prototyping programs available, such as SysGen of Xilinx, or high-level codes, e.g., C language, which implement the circuit using nonoptimized preconfigured blocks. Other methods, intended to reduce the computational resources used in the FPGA from the point of view of the number of hardware resources required and/or the area occupied by the circuit, are available, such as the use of pre-configured Xilinx blocks (intellectual property, IP) or the design of reconfigurable modules based on an adder/subtractor.

IPs can be configured depending on the elements that compose them, specifying whether their implementation is carried out through DSP or LUTs. The choice of the synthesis procedure depends on the needs of the designer and the free resources in the FPGA to embed the algorithm. This type of circuit uses a control block that defines the finite state machine (FSM) of the proposed PLL and the IP blocks that it calls in parallel depending on the needs of the algorithm in each state or clock cycle. In contrast, in those cases where the requirements of the control of the power converter assume that the sample rate of the synchronization circuit outputs is much lower than the clock frequency of the digital device used in the control, it is possible to design a circuit that further reduces the hardware resources required in the FPGA with respect to the previous proposal, increasing the execution time

of the algorithm. Here, the Booth-type reconfigurable modules based on an adder/subtractor block reduce both the area occupied and the number of hardware resources.

Following the rapid prototyping technique with SysGen, Table 4 shows a comparison with the resources consumed by each PLL analyzed in relation to the computational burden obtained by the five of the simplest strategies in Table 3. In order to facilitate its understanding, the resources of each strategy are compared in percentage terms with the resources obtained in the implementation of the *T/4* PLL, as this is the PLL based on the Park transform, which is easier to implement and widely consolidated in the literature. Table 4 shows that, although the five strategies show similar resource consumption, the 2S and the DSC PLL are the two strategies that require less resources after the *T/4* PLL. The structure of Figure 10 is a traditional and nonoptimized implementation of PLLs, so the use of different QSGs does not significantly affect the computational burden of the circuit. To appreciate a greater difference, it is necessary to use more optimized implementations such as that presented in Figure 16. This last PLL implementation scheme presents three optimizations that significantly reduce the computational burden using an oscillator, which replaces trigonometric functions, and eliminating the division operation and the normalization block, assuming high switching frequency [79].

Table 4. Summary of resources consumed by different PLLs in the field-programmable gate array (FPGA) using SysGen.

	T/4	2S		DSC		Hilbert		SOGI	
	Units	**Units**	**%**	**Units**	**%**	**Units**	**%**	**Units**	**%**
Registers	3472	3486	100.40	3521	101.41	3754	108.12	3552	102.30
LUTs	4927	5449	110.59	5015	101.79	5812	117.96	5393	109.46
Occupied sections	1697	1861	109.66	1686	99.35	1999	117.80	1876	110.55
LUT flip-flop pairs	5144	5682	110.46	5244	101.94	6175	120.04	5644	109.72
RAMB36E1 /FIFO36E1s	0	0	100.00	0	100.00	0	100.00	0	100.00
RAMB18E1 /FIFO18E1s	3	2	66.67	4	133.33	2	66.67	2	66.67
BUFG/BUGCTROLs	1	1	100.00	1	100.00	1	100.00	1	100.00
DSP48E1s	64	72	112.50	64	100.00	64	100.00	72	112.50

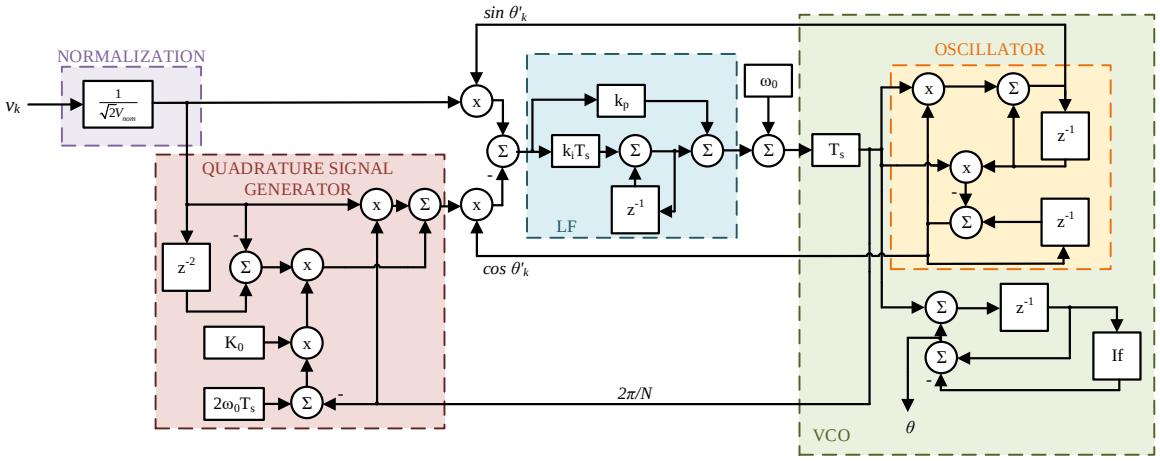


Figure 16. Structure of the optimized 2S-PLL [79] used in the Table 5.

On the other hand, as an example of the application of the different implementation techniques, Table 5 compares the hardware resources consumed by the optimized 2S PLL [79] and the cycles necessary to develop the circuit, according to Figure 16. The proposed strategy (using SysGen) assumes a 93.2% reduction in the slice register and 75.1%, 74.0% and 78.4% of LUTs, occupied sections and LUT flip-flop pairs, respectively. In contrast, the reduction of DSPs is 61.1% compared to the circuit of Figure 10. Moreover, if the implementation techniques are compared, Table 5 shows that rapid

prototyping presents nonoptimized algorithms that abuse the use of DSPs compared to the use of specific hardware techniques.

Table 5. Summary of the 2S PLL computational burden using different techniques of implementation.

	Design Using Specific Hardware			Rapid Prototyping	
	Based on IPs		Based on Reconfigurable Arithmetic Module	SysGen	C Language
	Based on DSPs	Based on LUTs			
Registers	299	300	357	237	525
LUTs	465	1100	669	1355	451
Occupied sections	242	406	257	482	170
LUT flip-flop pairs	598	1213	736	1231	595
RAMB36E1 /FIFO36E1s	0	0	0	0	0
RAMB18E1 /FIFO18E1s	0	0	0	1	0
BUFG/BUGCTROLs	2	2	1	1	1
DSP48E1s	3	0	0	28	16
Necessary clock cycles	17	17	157	-	17

4. Conclusions

To achieve a good current reference for grid connected converters, even in weak grids, the design of the functional blocks in the PLL must take a compromise solution between the quality of the dynamic and steady-state response and the computational burden. Steady-state results show that the consistency of the D-backward and 2S PLLs deteriorates the most due to the harmonic distortion, from variance 3.58° to 3.61° and 2.87° to 2.89°, respectively. All the QSGs perform worst in terms of phase ripple by increasing the harmonic distortion, from the 5.37×10^{2}°–5.38×10^{2}° range to 3.58×10^{3}°–3.6×10^{3}° respectively. In frequency and phase jumps tests, the PLLs resulting in shorter response times are SOGI, IPT, 2S and D PLLs, with similar consistency (e.g., the variance) across the MC tests. Voltage dips tests show that 2S and D PLLs are the best performers, both in terms of maximum phase error (with medium of 0.7° and 0.38° in the range of 0.55°–0.77° and 0.32°–0.42°, respectively) and response times (with medium of 131 and 138 ms in the range of 65–158 ms and 92–148 ms, respectively). The number of operations and memory units required by each analyzed PLL shows that the QSGs resulting in less resources are SOGI, 2S and D ones. It is also shown that by adapting this QSGs to filter out harmonics, the computational burden increases (see Table 3). A selection of these QSGs has been also implemented by means of an automatic tool, e.g., SysGen, in a field programmable gate array (see Table 5), showing that the 2S PLL uses a similar amount of registers than the *T/4* PLL (+0.4%) while other QSGs require +1.41% (DSC PLL) or more +8.12% (Hilbert PLL). In terms of LUTs and occupied sections, the DSC PLL performs the best with this automated generation tool. In order to evaluate the performance of these automated tools for rapid prototyping, the 2S PLL has been also implemented by means of specific hardware, and it is demonstrated (see Table 4) that the number of LUTs, occupied sections and flip flops required can be reduced significatively. Hence, from the analysis carried out, the most suitable QSG for a specific application where a cost-effective solution is required, should consider the both the PLL performance under diverse operation conditions and the associated computational burden.

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Abbreviations

APF PLL	PLL based on first-order all-pass filters
CORDIC	Coordinate Rotation Digital Computer
D	Derivative
DC	Direct current
DCO	Digitally Controlled Oscillator
DSO	Distribution system operators
DSC	Delay Signal Compensation
DSP	Digital signal processor
D PLL	PLL based on derivative
EPLL	Enhanced Phase-Locked Loop
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FSM	Finite state machine
HT	Hilbert transform
IIR	Infinite Impulse Response
IP	Intellectual Property
IPT PLL	Phase-Locked Loop based on the inverse of Park transformation
KF	Kalman filter
LF	Loop filter
LHS	Latin Hypercube Sampling
LKF	Limiting Kalman filter
LUT	Look Up Tables
LV	Low-voltage
MC	Monte Carlo
MHDC PLL	Phase-locked loop based on multiharmonic decoupling cell
MSOGI	Multisecond-order generalized integrator
NTD	Nonfrequency-dependent TD
PD	Phase detector
PDF	Probability density function
PI	Proportional–integral
PLL	Phase-locked loop
pPLL	Power-based phase-locked loop
SC PLL	Synthesis circuit phase-locked loop
SOGI PLL	PLL based on the second-order generalized integrator
QSG	Quadrature signal generation
QSG PLL	PLLs based on the quadrature signal generation
RDFT PLL	PLL based on recursive discrete Fourier transform
SRF PLL	Synchronous reference frame phase-locked loop
TD PLL	Transport delay phase-locked loop
VCO	Voltage controlled oscillator
2S-QSG	Quadrature signal generation based on two samples

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