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The upgraded front-end electronics of the CMS electromagnetic calorimeter for the HL-LHC

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Summary. — The Compact Muon Solenoid detector was originally designed to operate for about ten years, for LHC instantaneous luminosity up to $1{\cdot}10^{34}$ cm^{-2} s^{-1} and integrated luminosity of 500 fb^{-1}. The High Luminosity LHC will increase the instantaneous luminosity by about a factor of 5 from current levels and CMS will accumulate an integrated luminosity of 3000 fb^{-1} by about 2035. With such high luminosity the electromagnetic calorimeter of CMS will have to cope with a challenging increase in the number of interactions per bunch crossing and in radiation levels. The front-end readout electronics will be completely redesigned, with the goals of providing precision timing, low noise, sampling rate 4 times higher than the current one and added flexibility in the trigger system.

1. – Introduction

The primary driver of the ECAL upgrade is the trigger requirement for an increase of the trigger latency from about 6.4 μs in the legacy system to a maximum of 12.5 μs, and a Level-1 trigger rate of up to 750 kHz compared to the current 150 kHz. These are both mandatory at HL-LHC in order to maintain the physics performance of CMS while exploiting the higher luminosity [1].

Moreover the HL-LHC conditions are a significant challenge to both detector and electronics and performance because the increase in the accumulated radiation dose and fluence levels will imply significant loss in crystal light transmission and photo-detector performance. To provide the desired energy resolution over the full range of the signal events, the front-end readout electronics will be completely redesigned.

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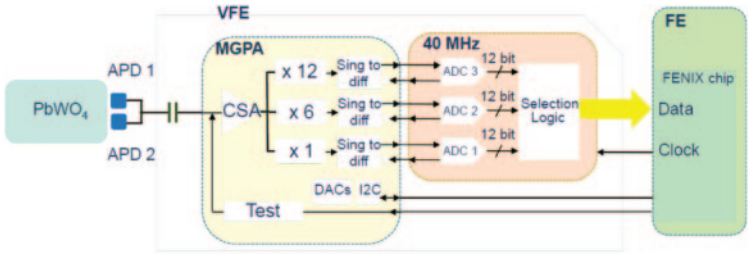

Fig. 1. – ECAL current on-detector readout chain.

2. – The CMS ECAL readout architecture

In the legacy readout architecture each lead-tungstate crystal is coupled to two APDs connected in parallel to form one analog channel. The APDs are read out by the Very Front-End (VFE) card. Each VFE card has five readout channels consisting of a multi-gain pre-amplifier (MGPA) and a quad-ADC. The MGPA provides three outputs with different gain values ($\times 1$, $\times 6$, $\times 12$). The three outputs are sampled and converted by a multi-channel, 12-bit, 40 MS/s ADCs. The ADC outputs from the five VFE cards are sent to a Front-End (FE) card. The FE card forms the trigger primitive for the 5×5 crystal array and contains a digital latency buffer and the primary event buffer. A schematic of the present ECAL on-detector electronics is shown in fig. 1.

The legacy readout system will not be able to satisfy the requirements of the ECAL upgrade. A higher bandwidth preamplifier and a faster sampling rate are needed to cope with the increased pile-up and to improve the spike rejection.

3. – ASIC developments

Two custom ASIC developments are ongoing in order to cope with the new requirements in terms of input bandwidth, conversion rates, transmission rates and radiation tolerance [2]. The two new ASICs will be hosted by a new VFE board with the same form factor and cooling system as the legacy system. A schematic of the upgraded ECAL on-detector electronics is shown in fig. 2.

3˙1. *CATIA preamplifier*. – The CATIA (CAlotimeter TransImpedance Amplifier) is a fully analog ASIC designed in a commercial CMOS 130 nm technology. The input stage drives two output amplifiers with gains $\times 1$ and $\times 10$. The output stages provide differential outputs with a differential voltage swing of 1.2 V.

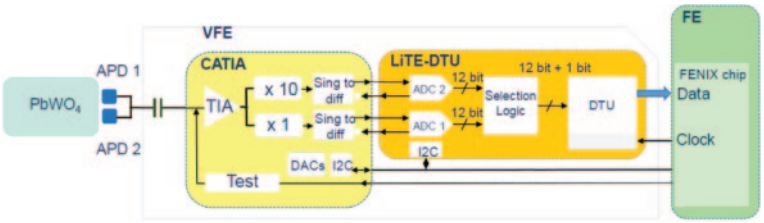

Fig. 2. – Upgraded ECAL on-detector readout chain.

A first prototype has been produced and successfully tested connected to the detector in a dedicated beam test. A second prototype and the final CATIA submissions are foreseen for the middle of 2018 and 2020, respectively.

3˙2. *LiTe-DTU*. – In the electronic readout chain, the CATIA ASIC will be followed by a Data Transmission Unit, named LiTE-DTU. This unit will receive the two analog signals from the preamplifier outputs and will convert them into a digital representation. The LiTE-DTU is a data conversion, compression and transmission ASIC. It will be implemented in CMOS 65 nm technology and is based on a 12-bit, 160 MS/s radiation-tolerant ADC IP block.

The ADC is the most critical component of the LiTE-DTU, it will be designed by an external company and the design will be based on successive approximation architecture. It has to satisfy the resolution and sampling rate requirements and, moreover, it has to sustain a maximum total ionizing dose of 10 kGy and implement a single-event upset protection [3].

3˙2.1. Data selection and compression. The converted data from the two ADCs will be fed into two small FIFOs, which are used to implement the sample selection algorithm with look-ahead capability in order to prevent the mixing of samples from different gains in the same detector signal.

The LiTE-DTU is designed to be directly connected to the lpGBT and Versatile Link+radiation-tolerant transceiver and optical module. The lpGBT modularity does not match well with the LiTE-DTU one, however it is possible to take advantage of the statistical distribution of the output values to perform a lossless compression based on the Huffman encoding. Indeed, the probability to have events with more than 6 significant (non-zero) bits is below $2.4 \cdot 10^{-4}$.

The data are organized in 32-bit packets. Each packet can accommodate up to five 6-bits consecutive samples or up to two 13-bits samples. A frame delimiter packet is inserted every 51 packets, it includes the number of samples in the frame, the frame id and a CRC of the data in the frame. An idle packet with a clock-like pattern is inserted when no data is available in order to avoid a loss of synchronization on the lpGBT side.

4. – Summary

The CMS ECAL upgrade foresees a redesign of the front-end electronics in order to cope with the new, more demanding requirements. Therefore, both the VFE and the FE cards and ASICs will be redesigned. The VFE card will be based on two new ASICs, the input preamplifier CATIA and the data conversion, compression and transmission logic LiTE-DTU. The first prototype of the CATIA ASIC has already been produced and tested, while the second version is currently been designed.

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