A Compact Polar/Cartesian Hybrid Phase Shifter for S-Band Phased Arrays

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***Abstract*— A phase shifter with polar output has been implemented with techniques commonly used for quadrature phase shifters. The hybrid approach employs dual-path programmable gain amplifiers and polyphase filters as cascaded quadrature phase shifter stages. Each stage is implemented using active components as well as differential RC filters which consume less area than the typical LC low-pass/high-pass approach. 5-bit phase resolution has been implemented. A 4-bit linear PGA follows the phase shifter chain for antenna tapering.**

The RFIC employing LNA and balancing devices has been been designed in a 0.25 μm SiGe BiCMOS technology which guarantees a low cost solution for medium scale integration such as in phased arrays. According to simulation results, a very homogeneous distribution of phase/gain states can be expected over a wide bandwidth. Achieved gain and noise figure in the band of interest (2.9 GHz ... 3.1 GHz) exhibit 25.9 dB and 11.6 dB, respectively, with a power consumption of 114 mW.

Digital controlled polar phase shifters being implemented as integrated circuits commonly apply circuit board techniques where fixed phase shifts or true time delays are switched, [1]. While this strategy promises high bandwidth and low insertion loss, device costs are high as each stage is composed of bulky inductors or transmission lines which are even not integrable in the lower GHz range.

A hybrid approach has been developed to overcome this issue. The polar approach contains phase switching while the magnitude is kept constant. Instead, a sum of orthogonal switchable vectors is used in each phase shifter stage. This technique is usually referenced to as cartesian or vector-sum phase shifting.

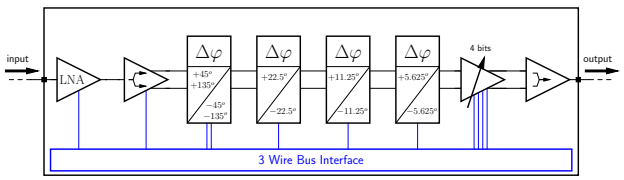


Fig. 1. System overview of the proposed phase shifter concept.

Fig. 1 gives an overview of the proposed system. A low noise amplifier as the first element reduces the system noise figure. The balun converts the single-ended input signal into a differential signal suitable for processing in the differential phase shifter core. The core consists of 4 phase shifter stages and a 4-bit PGA for antenna tapering. The first stage rotates the input signal in 90^o steps (providing two bits of resolution) as both vectors are switchable. All successive stages shift one bit by switching of one vector. An active balun matched to 50 Ω transforms the differential output signal back to a microstrip-compatible single-ended signal. The individual phase shifter stages have been implemented by dual-path PGAs with RF-domain DACs followed by buffered polyphase filters (PPFs). These DACs are a discretized version of the Gilbert analog multiplier cell. The output signals of both PGA paths are summed in quadrature in the PPF. A second order PPF is implemented for suiting the complete application bandwidth (2.9 GHz ... 3.1 GHz) with low vector amplitude error.

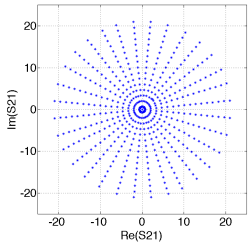
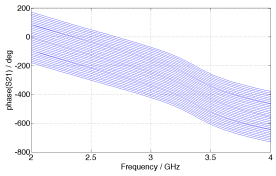
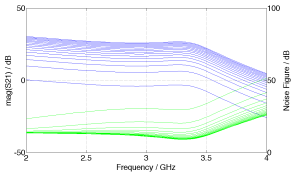


Fig. 2. Phase/gain map at f_c =3 GHz.

Fig. 2 shows the so-called phase/gain map at f_c =3 GHz. All attainable phase and gain states are properly distributed over constant-gain circles with a maximum deterministic phase error of $\Delta\varphi = 0.45^o$.



(a) S_{21} phase.



(b) S_{21} magnitude and NF.

Resultant transmission phases are plotted in Fig. 3(a). Offsets between states are almost constant over 1 GHz of bandwidth, resulting in a sharp antenna main beam even far below or above the application bandwidth. The fine resolution of the PGA for antenna tapering is depicted in Fig. 3(b).

References

[1] R. Garver, "Broad-Band Diode Phase Shifters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 20, no. 5, pp. 314–323, 1972.