Physical Investigations of novel Materials and Structures for Nano-MOSFETs

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Chapter 1

Introduction

The enormous success of CMOS technology over the last 30 years has been based on the device scaling concept. In its simplest form of constant field scaling proposed by Dennard (1) device dimensions are scaled by a constant factor $\kappa(> 1)$, while the body doping is increased and the applied voltages are reduced, to cause the depletion regions in the device to scale as much as the physical dimensions. The most important result of constant-field scaling is that once the device dimensions and the power-supply voltage are scaled down by κ, the circuit speeds up by the same factor. Moreover, the power dissipation per circuit, proportional to VI, is reduced by κ^2.

Scaling allowed an ever increasing density of transistors with higher speed and reduced power consumption and resulted in a great number of added functionality in all kinds of electronic products.

With todays devices featuring channel length of a few tenths of nanometers, the question has to be asked: What are the performance limits of MOS field effect transistors ? To improve the performance of MOSFETs it is no longer sufficient to simply scale the dimensions of the transistor. Material properties set natural boundaries. Performance increase has relied in part on the steady increase of channel carrier velocity due to gate-length scaling. However, the intrinsic carrier transport properties have remained constant, i.e. that of the relaxed silicon lattice (2). Additional innovations have to be introduced to increase the carrier mobility in the channel, for example by applying strain. Until the last years the dielectric constant of the gate insulator has not participated in scaling, either. For SiO_2-based dielectrics gate tunneling is a major concern at about 1 nm gate dielectric thickness (3). In Fig. 1.1 the main challenges faced in ultimately scaled devices and some possible solutions are indicated. They can be divided in the following categories:

(i) gate stack engineering: including high-k dielectrics and metal gate reduced gate leakage currents and increased gate capacitance;

(ii) source/drain engineering: optimal design of doping profiles and metal source/drain contacts for low series resistance;

(iii) channel engineering: high mobility channel materials for transport enhancement and high on-current;

(iv) suppression of short channel effects: multi-gate architectures for optimal control of the channel potential by the gate;

(v) variability: in nanoscale devices random dopant fluctuations, gate oxide and semiconductor thickness variability and the properties of individual interfaces are having very important effects on the device properties that were unimportant in larger devices.

To meet this demands material properties like bandstrucutre, dielectric constant and interface properties have to properly designed. Therefore, as device dimensions reach sizes in the range of a few nanometers, transistors, that have already been intensively investigated for three decades, face many new challenges that make them again attractive for basic physics research. The basic elements of a CMOS circuit is the inverter shown in Fig. 1.1. From it two important device performance metrics can be derived: (i) the gate-delay time τ that determines the maximum clock frequency of the circuit and (ii) the power consumption P. Considering the gate-delay time and the power consumption enables to understand which device parameters and material properties are effective for further MOSFET performance enhancement and to gain insight into the trade-offs between them (4). The gate-delay time is given by (5):

$$\tau = \frac{CV_{\mathrm{dd}}}{I_{\mathrm{on}}} \tag{1.1}$$

where C is the capacitance of the transistor to be charged or discharged, V_{dd} is the power supply voltage and I_{on} the current from coming another transistor. The I_{on}-current in saturation is given by (6):

$$I_{\mathrm{on}} = \mu_{\mathrm{eff}} C_{\mathrm{ox}} \frac{W}{L} \frac{(V_{\mathrm{g}} - V_{\mathrm{th}})^2}{2m} \tag{1.2}$$

where $m = 1 + C_{\mathrm{dm}}/C_{\mathrm{ox}}$ is the body factor, C_{dm} is the bulk depletion capacitance, C_{ox} is the gate capacitance per area, μ_{eff} is the effective mobility, L the channel length, V_{g} the gate voltage and V_{th} the threshold voltage. Including also series resistances $R_{\mathrm{S/D}}$ the gate delay time can be written as:

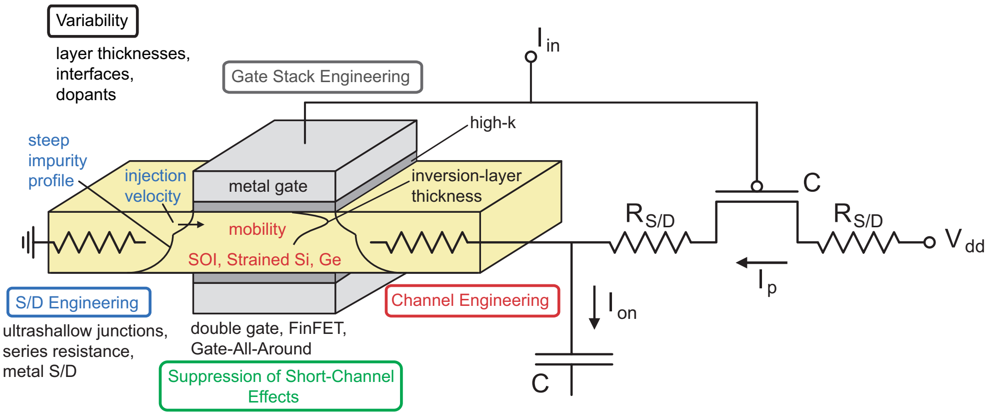
Variability
layer thicknesses,
interfaces,
dopants
Gate Stack Engineering
I in
high-k
steep
impurity
profile
injection
velocity
metal gate
inversion-layer
thickness
C
R S/D
R S/D
V dd
mobility
SOI, Strained Si, Ge
I p
S/D Engineering
ultrashallow junctions,
series resistance,
metal S/D
double gate, FinFET,
Gate-All-Around
Channel Engineering
I on
Suppression of Short-Channel
Effects
C

Figure 1.1: Schematic diagram of a double-gate MOSFET in a CMOS inverter circuit. The main challenges that are faced in device engineering for ultimately scaled devices are indicated with possible solutions.

$$\tau = \frac{2mL^2V_{\mathrm{dd}}}{\mu_{\mathrm{eff}}\left(V_{\mathrm{g}} - V_{\mathrm{th}} - I_{\mathrm{on}}R_{\mathrm{S/D}}\right)^2} \tag{1.3}$$

Increasing the transistor width, and thereby the current, has no impact on the switching speed, if two similar MOSFETs are connected in a circuit. The geometrical device parameters that have an impact on switching speed are the channel length that enters quadratically, and is therefore most effective for speed enhancement, and the gate oxide thickness that enters through the body factor m. The material properties that influence the switching speed are the carrier mobility μ, the source/drain resistances $R_{\mathrm{S/D}}$ and the dielectric constant of the gate-oxide and the semiconductor. Therefore, to increase the switching speed of MOSFET devices the channel length has to be reduced, the carrier mobility in the semiconductor material should be large, source/drain resistances should be small, the gate-oxide thin and its dielectric constant large.

As device dimensions decrease, the close proximity between the source and drain reduces the ability of the gate electrode to control the potential distribution and the current flow in the channel (7). Source/Drain influence on the channel can be reduced by increasing the channel doping concentration. In very small devices the doping becomes too high ($10^{19}\,\mathrm{cm}^{-3}$) for proper device operation. A much better electrostatic integrity is obtained in multi-gate devices due to a smaller natural length λ. It is the relevant length scale for potential variations in the channel caused by source/drain contacts and is a function of the semiconductor thickness t_{s} and the gate oxide thickness t_{ox} . The best electrostatic integrity is obtained in gate-all-around devices where λ is given by (8):

$$\lambda_{circ} = \sqrt{\epsilon_{\mathrm{s}} t_{\mathrm{s}}^2 ln \left(1 + \frac{2\epsilon_{\mathrm{ox}}}{t_{\mathrm{s}}}\right) / 8\epsilon_{\mathrm{ox}}} \tag{1.4}$$

A basic understanding of the trade-offs between different device parameters can be obtained from the power consumption of a MOSFET. Since static power dissipation is very low in CMOS circuits, the main power consumption comes from switching. The average power dissipation depends on how often a transistor switches, controlled in a CMOS circuit by a clock generator of frequency f. The power consumption can be approxiamted by (9):

$$P \approx f C_{\mathrm{load}} V_{\mathrm{dd}} + I_{\mathrm{on}} \cdot 10^{-V_{\mathrm{th}}/S} \cdot V_{\mathrm{dd}} + I_{\mathrm{leak}} \cdot V_{\mathrm{dd}} \tag{1.5}$$

where f, C_{load}, V_{dd}, I_{on}, V_{th}, S and I_{leack} are the clock frequency, the load capacitance, the power-supply voltage, the on-current, the sub-threshold slope and the total leackage current.

From Eqn. 1.5 it is obvious that low-power MOSFETs require a low supply voltage V_{dd}, a higher threshold voltage V_{th}, a small S and low leakage currents, and therefore, immunity to short channel effects. However, these requirements are in conflict with those of a high I_{on} (10). A lower V_{dd} and higher V_{th} lead to a significant reduction in I_{on}. Higher substrate doping densities, necessary to suppress short-channel effects in bulk planar MOSFETs and for a small subthreshold slope, decrease I_{on} due to a lower mobility. Furthermore, higher channel doping causes increased leackage currents due increased junction-tunneling and gate-induced drain leackage. If thicker gate oxides are employed to reduce gate-tunneling, S is increased and I_{on} decreased.

In this thesis several aspects to overcome some of the fundamental challenges addressed above have been investigated:

- **Chapter 1: Metal Source/Drain Contacts**
  Schottky-barrier (SB) MOSFETs with NiSi source/drain contacts were investigated. To lower the effective Schottky Barrier height (SBH) and thereby improving the subthreshold slope and the $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio, silicidation induced dopant segregation is very promising. In the first part of the chapter, the scalability of SB-MOSFETs with arsenic dopant segregation is analyzed for the first time by a thorough investigation of the effect of silicidation induced dopant segregation on dopant profiles. In the second part of the chapter, the impact of SBH-variability on the performance of SB-MOSFETs with and without dopant segregation is

investigated. A new experimental method has been developed, that allows the determination of the SBH variability from transistor characteristics. With this method the SBH variability in SB-MOSFETs has been measured and effect of dopant segregation on the variability of the SBH in MOSFETs has been quantified for the first time.

- **Chapter 2: Strained Silicon - A High Mobility Channel Material**
  Thin strained Silicon layers (sSi) with a thickness of 8 nm were formed by strain transfer between a SiGe buffer and a Si cap layer. The main advantage of the strain transfer method are that only one epitaxial growth step is required to make an ultrathin strained layer and standard silicon cleaning can be applied for expitaxial overgrowth. Thicker sSi-layers with excellent morphology and low defect densities were obtained by sSi or SiGe overgrowth
  A new method for the fabrication of asymmetrical strained Si/SiGe heterostructures by He^+-ion implantation and annealing was developed. Asymmetric strain relaxation of Si/SiGe lines transforms biaxial stress into strongly asymmetric stress for very narrow lines. Asymmetric strain relaxation is explained by the limitation of the path length of threading dislocations by the line boundaries, leading to an asymmetric misfit dislocation network. These lines are attractive for the fabrication of strained nanowire heterostructure MOSFETs with improved electron and hole mobilites.
  In order to investigate the impact of biaxial tensile strain on the electrical device properties, Hallbar MOSFETs on SOI and biaxial tensile strained SSOI have been fabricated. Performance improvements in terms off on-current and transconductance enhancement and mobility gain in devices on SSOI have been experimentally demonstrated, that are in very good agreement with the works of other groups in recent years.
  Low temperature magnetotransport measurements were performed to determine the effective mass of electrons in the lowest subband in biaxial tensile strained SSOI from the temperature dependence of the Shubnikov-de Haas amplitudes in the longitudinal resistance. With the first direct measurement of the electron effective mass in biaxial tensile strained SSOI, it was possible to confirm theoretical bandstructure calculations that predicted no mass change for a biaxial stress of 1.2 GPa.

- **Chapter 3: Multigate Devices - Silicon Nanowires**
  A process for the fabrication of Nanowire-MOSFETs in a top-down approach has been developed. Long channel NW-MOSFETs on SOI and biaxially tensile strained SSOI were successfully fabricated.
  Current flow on different crystal planes in multi-gate NW devices opens a new opportunity for device engineering due to the anisotropy of silicon. On SOI NW devices the possibility to match on-currents of n- and p-type Nanowire FETs by proper choice of channel direction was demonstrated.
  Size dependent strain relaxation of strained nanoscale structures has been employed to fabricate uniaxial tensile strained NW-MOSFETs. These show substantial higher on-currents and transconductances as well as higher electron mobilities compared to identical unstrained NW-MOSFETs.

Chapter 2

Metal Source/Drain Contacts

2.1 Introduction

Recently there has been a renewed interest in Schottky barrier (SB)-MOSFETs as an alternative to conventional MOSFETs with doped source and drain contacts in ultimately scaled devices which require highly conductive contacts with abrupt doping profiles (11). SB-MOSFETs meet this requirements because the metallic source/drain areas offer abrupt junctions and low extrinsic parasitics (12).

In this introduction the different operation principles of conventional and SB-MOSFETs are briefly discussed that have been analyzed in great detail by Knoch and coworkers (13; 14; 15; 16). The different operating principles of a conventional and a SB-MOSFET are illustrated in Fig. 2.1(a). In a conventional MOSFET with doped source/drain contacts the electrical behavior is determined by the potential maximum in the channel Φ_f^0 that mediates the injection of carriers from the source into the channel (17). When the gate moves the conduction band downward, a larger fraction of the exponential tail of the source Fermi function can contribute to the current, giving rise to the exponential increase of current in the device off-state.

On the other hand, the electrical characteristics of SB-MOSFET are dominated by the Schottky-barrier that builds up at the metallic source/drain-channel interface. To illustrate the current control mechanism Fig. 2.1(b) shows on the right side a schematics of the conduction and valence band profiles of a SB-MOSFET for three different gate voltages and on the left a typical experimental transfer characteristic of a SB-MOSFET with NiSi source/drain contacts. The characteristic has the typical ambipolar behavior with a large subthreshold slope $S_1 = 250\,\mathrm{mV/dec}$ in the branch corresponding to electron injection by tunneling through the drain SB. Two different

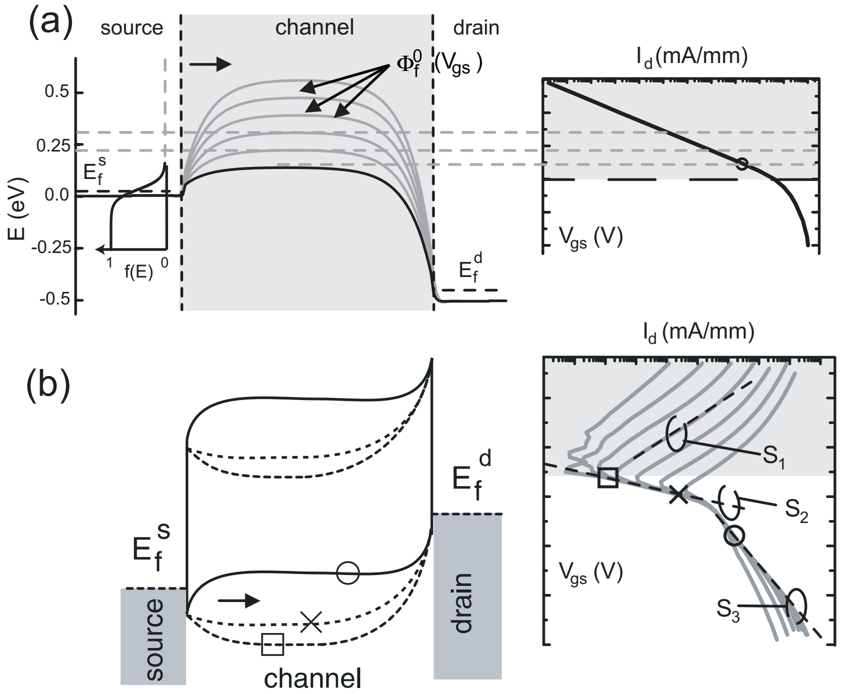

Figure 2.1: (a) Conduction band profile in transport direction for a conventional long channel MOSFET. The gate voltage moves the conduction band downwards, so that a larger fraction of the exponential tail of the source Fermi distribution can contribute to the current. This gives rise to the exponential increase of the current in the devices of state, as illustrated to the left of the band profile. (b) Conduction and valence band along the current transport direction in a Schottky-barrier MOSFET. To the left typical ambipolar transfer characteristic of a SB-MOSFET is shown. Three gate voltages are indicated that correspond to the respective band rofiles. (18; 13).

subthreshold slopes S_2 and S_3 can be identified in the hole branch indicating that the Fermi level is pinned more closely to the hole band. Between the gate voltages belonging to the symbols □ and ×, electron injection from the drain is suppressed and the injection of holes is mediated by thermal emission, as in a conventional MOSFET, leading to a small subthreshold slope S_2. When the valence band is pushed above Φ_{SB} for more negative gate voltages, the injection of holes is determined by the change of the tunneling probability through the SB with gate voltage. As a result, SB-MOSFETs exhibit in this V_g-region inverse subthreshold slopes S_3 larger than 60 mV/dec and lower on-currents compared to conventional MOSFETs (15).

2.2 Scaling Issues of n-type Dopant Segregation SB-MOSFETs

Metallic source/drain contacts in SB-MOSFETs ensure lower parasitic resistances compared to conventional doped contacts. However, due to the Schottky-barrier (Φ_B) at the metallic source/drain contacts, the performance of SB-MOSFETs still falls behind that of conventional FETs. Therefore much work was devoted to lower the Schottky barrier height by using silicides with lower Φ_B (19; 20) or dopant segregation (21; 22) and to improve the carrier injection into the channel by using thin gate oxides and thin-body silicon-on-insulator (SOI) (15; 23).

Traditionally an ohmic contact between a semiconductor and a metal is formed by highly doping the semiconductor (24). However, for a fully depleted SOI MOSFET channel doping causes merely a shift in threshold voltage and reduced carrier mobility. Figure 2.2(b) shows the threshold voltage shift due to channel doping in a fully depleted SOI device. The carrier injection into the channel is uneffected and therefore subthreshold swing and transconductance are not improved. In order to improve the carrier injection without shifting the threshold voltage a non-uniform doping profile with a high dopant concentration only at the metal/semiconductor interface is needed. This can be achieved through silicidation induced dopant segregation (25). The segregation layer causes a strong band bending at the contact channel interface effectively thinning the SB (Fig. 2.2(a)). However, for application in advanced CMOS it is essential that devices based on dopant segregation are scalable to ultra-short channel lengths. Hence, the segregation layers are required to be thin and to have very steep dopant profiles into Si at the contact/channel interface. As the channel length is decreased source and drain contacts come closer together and the dopant tails of the segregation layers overlap. There is a minimum channel length L_{min} at which the overlap of the dopant tails of the segregation layers starts to constitute a significant channel doping that gradually leads to a loss of improved carrier injection. The value of L_{min} is determined by the extend of the segregation layer l_{seg} and the slope of the dopant tail into Si. This is illustrated in Fig. 2.2(c) and (d).

In this chapter Arsenic dopant segregation is investigated systematically with emphases on process compatibility with MOSFET downscaling requirements for the 22 nm node. To this end attention is focused on the dependence of the slope of the dopant profile into Si and the dopant concentration at the NiSi/Si-interface on implantation energy, NiSi thickness and the annealing process employed for the formation of the silicide layer. Interface rough-

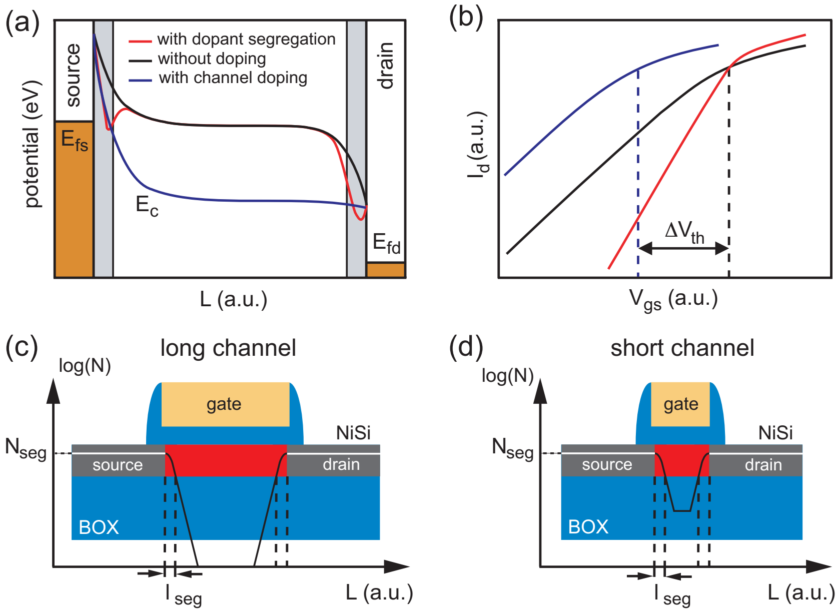
(a)
potential (eV)
source
drain
with dopant segregation
without doping
with channel doping
E_fs
E_c
E_fd
L (a.u.)
(b)
I_d (a.u.)
ΔV_th
V_gs (a.u.)
(c)
long channel
log(N)
gate
NiSi
N_seg
source
drain
BOX
l seg
L (a.u.)
(d)
short channel
log(N)
gate
NiSi
N_seg
source
drain
BOX
l seg
L (a.u.)

Figure 2.2: (a) Conduction band profile of a SB-MOSFET without doping, with channel doping and with doping segregation. (b) Transfer characteristics corresponding to devices with the conduction band profiles shown in (a). (c) In a long channel SB-MOSFET with dopant segregation the dopant distributions from source and drain contacts are well separated. (d) In a short channel SB-MOSFET with dopant segregtion the source/drain dopant distribution tails overlap creating a constant doping density in the channel.

ness data from TEM and XRR measurements on silicided samples is used to highlight the deteriorative effect on the performance due to increased variability of ultimately scaled SB-MOSFETs. Finally, experimental results on As dopant profiles at the silicon silicide interface are used to investigate the scaling limits of SB-MOSFETs with dopant segregation with simulations.

2.2.1 Sample Preparation

For the investigation of Arsenic dopant segregation in nickel silicide layers three sets of samples were fabricated: i) (100) Si samples were implanted with As to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ at energies from 1 to 10 keV. After cleaning of the samples and removing the native oxide with (1%) HF-solution Ni layers of different thicknesses were deposited by E-beam evaporation. Subsequently the samples were annealed at 450 °C for 20 sec in forming gas to form nickel monosilicide (NiSi). Unreacted Ni was removed with H_2SO_4:H_2O_2 (4:1); ii) (100) Si samples that were implanted with As at an energy of 5 keV and doses between $5{\times}10^{13}\,\mathrm{cm}^{-2}$ and $1 \times 10^{15}\,\mathrm{cm}^{-2}$. After implantation 30 nm NiSi layers were formed using the same steps and process parameters as for

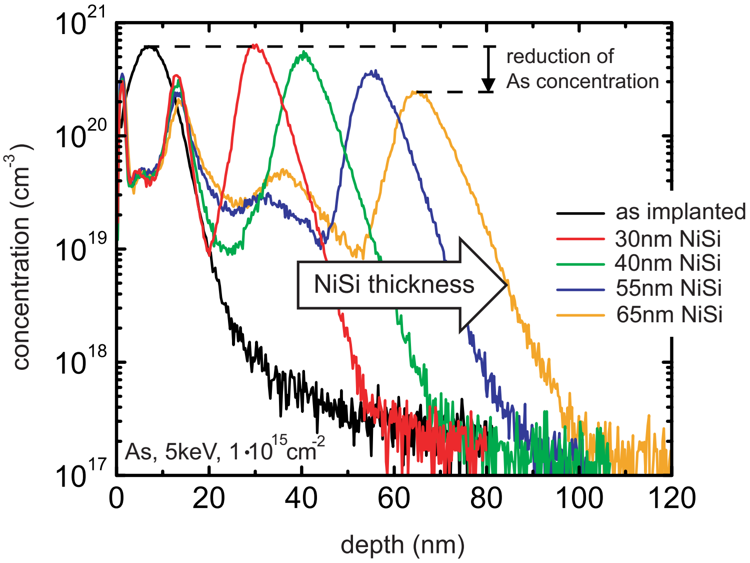

Figure 2.3: SIMS spectra of Si samples implanted with As, 5 keV, 1×10^{15} cm^{-2}. The spectrum of the as-implanted sample and silicided samples with different NiSi thicknesses are shown. The dopant peak shifts with the NiSi/Si interface during silicidation. With the increase of NiSi thickness the peak concentration and the slope of the dopant distribution tail into Si decrease.

the samples (i); iii) Si samples were implantated with As at energies 1 keV and 2 keV to a dose of 1×10^{15} cm^{-2}. NiSi layer were formed with a two-step annealing process: After Ni deposition Ni_2Si was first formed by annealing the samples at a temperature of 280 °C for 60 sec. The unreacted Ni was removed and a second annealing step at 500 °C was performed to form nickel monosilicide. The dopant profiles of as-implanted and silicided samples were measured with time-of-flight secondary ion mass spectroscopy (SIMS) using a 1 keV Cs-ion beam. To determine the dopant concentration in the samples two calibration standards have been used: a Si sample and a NiSi sample with a known As concentration. Roughness at the NiSi/Si interface has been determined with XRR measurements.

2.2.2 Experimental Results

In this paragraph the dependence of the slope and concentration of the As dopant distribution at the NiSi/Si interface on implantation energy, implantation dose and NiSi thickness are discussed. In addition it is demonstrated that with a modified silicidation process shallow NiSi/Si junctions with dopant segregation and slopes of the dopant profile very close to that of as-implanted one can be fabricated. For simplicity reasons in the following

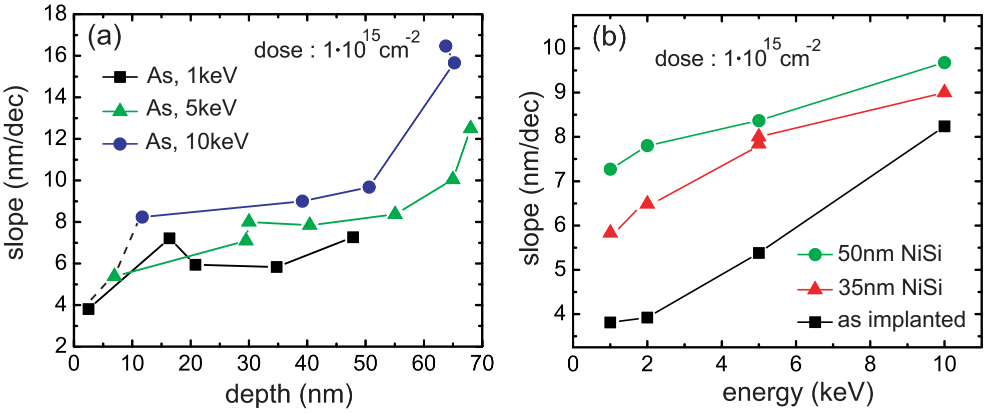

Figure 2.4: (a) Plot of the slope of the As dopant distribution tail vs. NiSi thickness. With increasing NiSi thickness the slope of the dopant distribution tail decreases. A steeper initial dopant profile for a lower implantation energy results in a steeper profile after silicidation. The dotted line connects the points corresponding to the as-implanted profiles. (b) Plot of the slope of the As dopant distribution tail into Si as a function of implantation energy. The values of as-implanted samples and of samples that were silicided after implantation are shown.

the term "dopant slope" is used when referring to the slope of the As dopant profile at the NiSi/Si interface into the Si substrate side.

Dependence of the Dopant Slope on Implantation Energy and NiSi Thickness

Figure 2.3 shows the SIMS spectrum of a bulk Si sample implanted with As, 5 keV, $1 \times 10^{15}\,\mathrm{cm}^{-2}$ and that of four identically implanted samples with different NiSi thicknesses ranging from 30 nm to 65 nm. The peak of the dopant profile shifts from the as-implanted position during silicidation with the movement of the NiSi/Si-interface as a consequence of silicidation induced dopant segregation. The peak concentration decreases with increasing NiSi thickness from $6 \times 10^{20}\,\mathrm{cm}^{-3}$ in the as-implanted case down to $2.3 \times 10^{20}\,\mathrm{cm}^{-3}$ for a NiSi thickness of 65 nm. Simultaneously the dopant slope increases from 6.8 nm/dec to 10 nm/dec. These results are presented in fig. 2.4 (a) where the slope of the As is plotted against the NiSi layer thickness for three different implantation energies. For all three implantation energies the slope increases with increasing NiSi thickness, indication of dopant redistribution during segregation. The smaller slope of the as-implanted dopant profile for smaller implantation energy translates into a smaller slope of the dopant distribution into Si at the NiSi/Si-interface for smaller NiSi thicknesses. In fig. 2.4 (b) the slope of the dopant distribution is plotted vs. the implantation energy

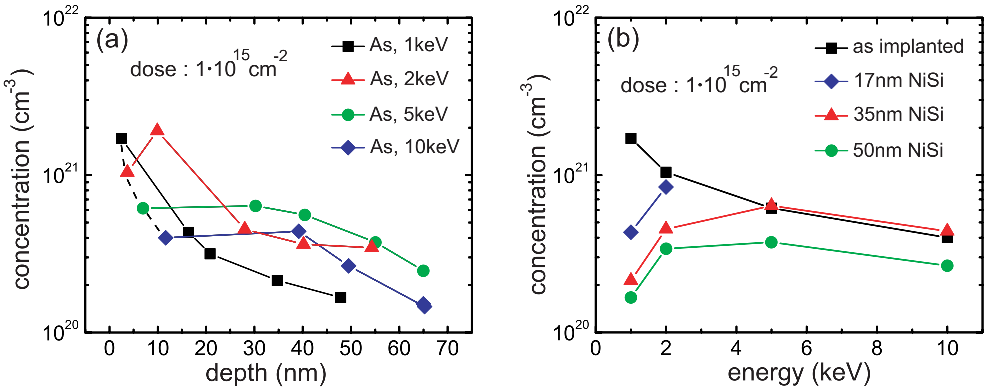

Figure 2.5: (a) Plot of the As concentration at the NiSi/Si interface vs. the NiSi thickness for different implantation energies. The dotted line connects the points corresponding to the as-implanted samples. (b) Plot of the As concentration at the NiSi/Si interface as function of NiSi thickness for different implantation energies.

for the as-implanted samples and two different NiSi thicknesses. For the as-implanted samples the slope of the dopant profile increases with increasing implantation energy. While the increase in slope from 1 keV to 2 keV in only about 0.1 nm/dec there is a rapid linear increase of the slope with further increase of implantation energy that reaches 8.2 nm/dec for 10 keV. Similar behavior is observed after silicidation of the implanted samples. There is only a small difference in slope for implantation energies of 1 keV and 2 keV, followed by a steeper linear increase in slope with augmenting implantation energy. By comparing the degradation of the slopes of the as-implanted dopant profiles through silicidation induced dopant segregation for low (1 keV) and high (10 keV) implantation energy, it is found that the increase in slope for a steep initial profile is larger than for an intially broader dopant profile. Also, a larger NiSi thickness results in a larger slope of the dopant distribution. The larger increase in slope with increasing implantation energy of the as-implanted samples compared to the increase in slope due to silicidation induced dopant segreation can be explained by the different mechanisms responsible for dopant redistribution. While for the as-implanted samples increased scattering of the implanted dopants with the matrix atoms with increasing energy is responsible for the augmenting slope of the dopant profile, for the silicided samples the increase is caused by dopant redistribution between the forming NiSi and the Si due to the different solute solubilities of arsenic dopants. The degradation of the slope of the dopant profile due to segregation is smaller than that due to an increase in implantation energy. It is therefore advantageous in terms of dopant slope to start with a low energy implantation even if a significantly thicker NiSi layer than the concentration peak of the as-implanted dopant profile is to be formed.

Dependence of the Dopant Concentration at the NiSi/Si Interface on Implantation Energy and NiSi Thickness

In this subsection the dependence of As dopant concentration at the NiSi/Si-interface on NiSi thickness and implantation energy are discussed. Figure 2.5(a) shows a plot of the dopant concentration at the NiSi/Si-interface as a function of the NiSi thickness for four different implantation energies. The dotted line connects the peak concentrations of the as-implanted samples. With increasing implantation energy from 1 keV to 10 keV the dopant concentration drops from $2 \times 10^{21}\,\mathrm{cm}^{-3}$, the solid solubility limit of arsenic in silicon, to $3 \times 10^{20}\,\mathrm{cm}^{-3}$. For 2 keV implantation energy the dopant concentration first increases during the formation of a thin NiSi layer, than decreases and afterwards stays constant with increasing NiSi thickness over a certain NiSi thickness range. Similarly, for 5 keV and 10 keV, the dopant concentration remains constant for a certain range of NiSi thickness. For all three energies the concentration at the interface drops from the value measured on as-implanted samples for a NiSi thickness of about $3-4$ times the depth of the dopant peak in the as-implanted samples. The shape of the curve corresponding to 1 keV compared to the other three energies can be explained by the fact that the thinnest NiSi layer for this energy is with 17 nm approximately 8 times thicker than the depth of the concentration peak of the as-implanted dopant profile.

Figure 2.5(b) shows the dopant concentration at the NiSi/Si interface as a function of implantation energy for samples with three different NiSi thicknesses. The dopant concentration in the as-implanted cases are plotted for comparison. For the as-implanted samples the peak dopant concentration decreases with increasing implantation energy. In the case of the silicided samples, the dopant concentration at the NiSi/Si interface first increases for all investigated NiSi thicknesses, reaches a maximum value specific for the NiSi thickness and then decreases at the same rate as the concentration in the as-implanted samples. For each implantation energy there is an optimum NiSi thickness (and visa versa for each NiSi thickness an optimum range of implantation energies) for which the dopant concentration at the NiSi/Si-interface reaches the as implanted concentration peak value. For example, for a 35 nm NiSi layer implantation energy in between $5-10$ keV can be choosen. The concentration at the NiSi/Si-interface of the 50 nm NiSi layer lies for all investigated values of implantation energies below that of the as implanted samples. This can be interpreted as follows: For an implantation energy of 10 keV the concentration peak of $3 \times 10^{20}\,\mathrm{cm}^{-3}$ lies at about

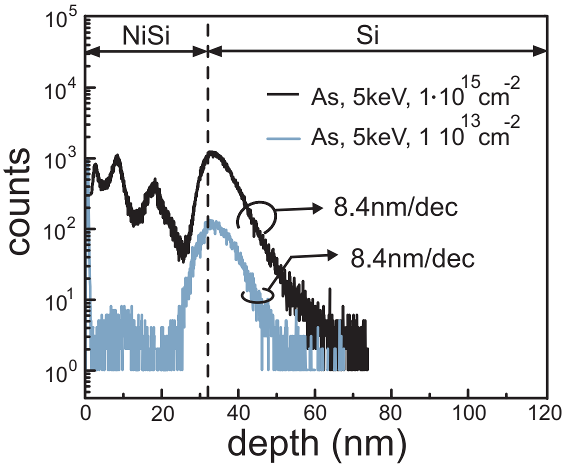

Figure 2.6: SIMS profiles of As implanted samples at an energy of 5 keV to a dose of $5 \times 10^{13}\,\mathrm{cm}^{-2}$ (grey) and $1 \times 10^{15}\,\mathrm{cm}^{-2}$ (black), respectively. On both samples a 30 nm NiSi layer was formed after implantation. A similar slope of the dopant profile at the NiSi/Si-interface is obtained in both cases.

11.7 nm below the sample surface. According to the before stated rule of thumb that the optimum NiSi thickness for maximum dopant concentration at the NiSi/Si-interface should be 3-4×the depth of the concentration peak in the as implanted samples, the layer is already too thick for this implantation energy. Comparing with fig. 2.5(a) we find that for a NiSi thickness of around 40 nm an As concentration equal to that in as implanted samples can be obtained at the NiSi/Si-interface.

Dependence of the Dopant Slope on Dopant Concentration

In this subsection the influence of dopant concentration at the NiSi/Si-interface on the dopant slope is discussed. Figure 2.6 shows two SIMS profiles of samples implanted with arsenic at 5 keV to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ and $5 \times 10^{13}\,\mathrm{cm}^{-2}$, respectively. After implantation both samples were silicided to a NiSi thickness of 30 nm. Both samples show the same dopant profile slope of 8.4 nm/dec. The difference in implantation dose translates to a difference in dopant concentration at the NiSi/Si-interface after segregation. It has been shown that a high concentration of dopants at the NiSi/Si interface is important for an effcient lowering of the SBH (22). Therefore it is advantageous for device performance to choose a large implantation dose.

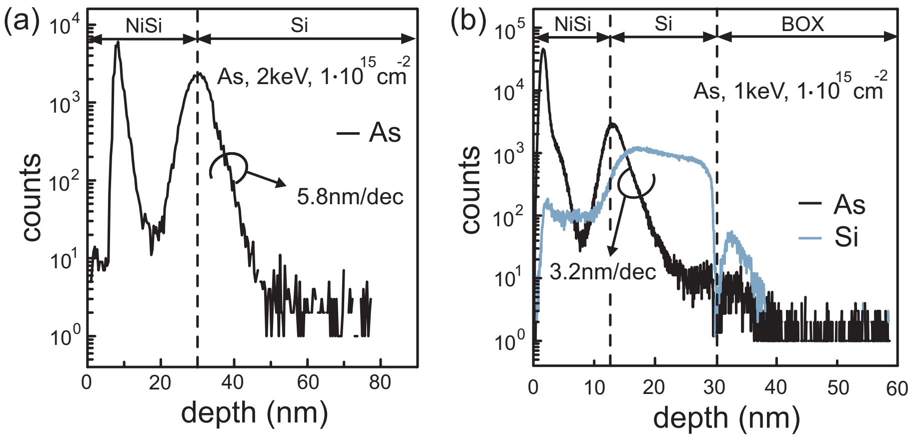

Figure 2.7: SIMS profile of As dopant distribution at the NiSi/Si interface formed by a two-step annealing process. (a) SIMS profile of a Si sample implanted As 2 keV $1 \times 10^{15}\,\mathrm{cm}^{-3}$ with a 30 nm NiSi layer. (b) SIMS profile measured on a 30 nm SOI sample implanted with As 1 keV $1 \times 10^{15}\,\mathrm{cm}^{-3}$ with a 13 nm NiSi layer. The slope of the dopant distribution tail into Si at the NiSi/Si interface into Si amounts to 5.8 nm/dec and 3.2 nm/dec, respectively.

Two-Step Silicidation

In this subsection the impact of the annealing process on the dopant slope is discussed. By modifying the annealing sequence it is possible to obtain a steeper dopant profile at the NiSi/Si-interface than in a one step process. Figure 2.7 (a) shows the SIMS profile of a 30 nm NiSi layer formed on bulk Si by a two-step silicidation process. The sample was implanted with As at an energy of 2 keV to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-3}$. Subsequently, Ni was deposited by e-beam evaporation and the sample was annealed at 280 °C for 60 sec. This results in the formation of the high resistivity Ni_2Si-phase (26). After the removal of the unreacted Ni the sample was annealed at a temperature of 500 °C in order to form the nickel monosilicide phase. An As dopant slope of 5.8 nm/dec was determined from the SIMS spectrum. For the same implantation conditions and NiSi thickness formed by a one-step silicidation process a higher dopant slope of 6.6 nm/dec was measured. A similar improvement of dopant slope due to a two-step annealing process was obtained for silicon on insulator (SOI) material. Figure 2.7(b) shows the SIMS spectrum of a 13 nm NiSi layer formed on a 30 nm SOI sample with the two-step silicidation process. The slope of the As dopant profile is in this case 3.2 nm/dec in comparison with 5 nm/dec for the one-step annealing process. In Fig. 2.8 three differently processed samples implanted with As at an energy of 15 keV to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ and 85 nm NiSi are compared. One sample was processed after ion implantation with a one-step silicidation process. A second sample was processed with the two-step silicidation process described above. As in the case of low implantation energy and lower NiSi thickness the slope of the dopant profile improves from 27 nm/dec for the one-step to 17 nm/dec for the two-step process. On the third sample in a first step Ni_2Si was formed by annealing at 280 °C. Subsequently implantation was carried out into the Ni_2Si layer. Finally nickel monosilicide was formed in a second annealing step at 500 °C. The slope of the dopant profile for this process flow is 22 nm/dec. While there is an improvement in dopant slope compared to one-step annealing, the dopant concentration at the NiSi/Si-interface is reduced by nearly an order of magnitude compared to the two other process flows. This is very disadvantageous since a high dopant concentration at the NiSi/Si-interface is imperative for an efficient lowering of the SBH. It is therefore concluded that the two-step annealing process for NiSi formation after ion implantation can be employed to further improve the slope of the As dopant profile after process optimization through implantation energy, dose and NiSi thickness, as described above.

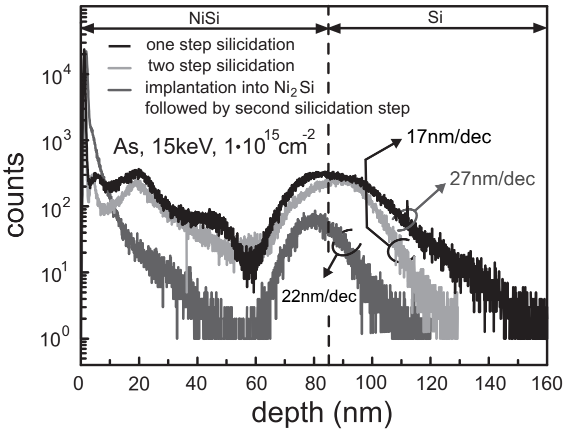

Figure 2.8: Comparison of the SIMS profiles of As dopant distribution at the NiSi/Si interface for three annealing processes. Implantation conditions are in all cases: As, 15 keV, 1×10^{15} cm^{-2}. (a) One-step silicidation (black-line), (b) two-step silicidation (light-grey) and (c) implantation into Ni_2Si followed by a second annealing to form NiSi (grey).

2.2.3 Simulation of Scaled SB-MOSFETs with Dopant Segregation

In this paragraph the results on the As dopant profile at the NiSi/Si-interface after silicidation induced dopant segregation are used to investigate the scaling limits of n-type SB-MOSFETs with dopant segregation with simulations.

As has been pointed out in the introduction the limiting factors for the scalability to smaller channel length of SB-MOSFETs with dopant segregation are the extention to the dopant segregation layer l_{seg} and the slope of the dopant profile. The discussions in the previous subsections delt with the vertical dopant profiles at the NiSi/Si interface but for device contacts lateral dopant segregation at the source/drain-contact interfaces is of interest (compare Fig. 2.12).

The Vertical and Lateral Slope of the Dopant Profile after Implantation

To investigate the slope of the dopant profile in the lateral direction towards the channel ion implantation into a SOI layer was simulated using a two-dimensional Monte-Carlo model (27). After forming the gate stack, source/drain contacts were implanted with arsenic to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$. From the simulated dopant profiles the slopes in the lateral and vertical direction were extracted. The inset of Fig. 2.9 shows part of the simulated structure. In the contact area red corresponds to a dopant concentration of $10^{21}\,\mathrm{cm}^{-3}$ and blue to a concentration of $10^{16}\,\mathrm{cm}^{-3}$. As the gate shields the channel during ion implantation the dopant distribution only reaches to a small extend into the channel as a result of ion straggling during implantation. The plot of Fig. 2.9 shows the slope of the dopant profile vs. implantation energy. Two important conclusions are drawn from Fig. 2.9: first, the dopant slopes in the vertical direction extracted from the simulations perfectly agree with the values measured by SIMS. Secondly, the slope of the dopant profile in the lateral direction is for all implantation energies smaller than that in the vertical direction. The larger the implantation energy the larger becomes the difference between the slopes in the lateral and vertical direction. For an implantation energy of 1 keV to 2 keV the slope of the As dopant distribution in the lateral direction is in the range of $1{-}2\,\mathrm{nm/dec}$.

In the previous paragraph it was found that there is an optimum NiSi layer thickness for each implantation energy in order to obtain maximum dopant concentration at the NiSi/Si-interface after silicidation induced dopant segregation and a fast drop of dopant concentration into Si. Furthermore it was shown that the degradation of the steepness of the as implanted dopant profile due to silicidation induced dopant segregation can be minimized using a two step annealing process for the formation of NiSi. For an As implantation of 1 keV and a NiSi layer thickness of about 10 nm fabricated by a two-step annealing process the slope of the dopant distribution after silicidation induced dopant segregation can therefore be assumed to be in the range of $1{-}2\,\mathrm{nm/dec}$. Values in this range for the slope of the dopant distribution in the lateral direction were used in the device simulation of short channel n-type SB-MOSFETs with dopant segregation as presented in the following subsection.

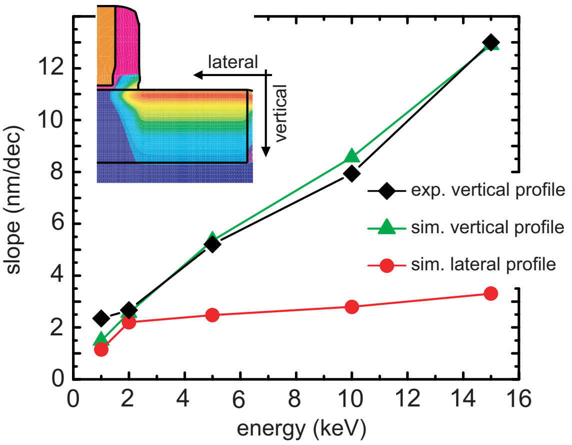

Figure 2.9: Plot of the slope of the dopant distribution profile in the vertical and lateral dircetion plotted against implantation energy. The slopes extracted from SIMS profiles agree well with the values obtained for the vertical profiles from simulations. The slope of the dopant profile in the lateral direction is for all energies smaller than the vertical one.

Device Simulation Results

In order to study the effect of different slopes of the dopant profile on the electrical characteristics of SB-MOSFETs with dopant segregation simulations of nanoscale devices have been performed. The Schrödinger equation has been solved self-consistently with the one-dimensional Poisson equation using the non equilibrium Greens function formalism (28; 29). To compute the Greens function a one-dimensional finite difference scheme with lattice constant a and nearest-neighbor hoping was employed. Only ultrathin body SB-MOSFETs with a silicon thickness of $t_{\mathrm{si}} = 5\,\mathrm{nm}$ and a very thin gate oxide of $t_{\mathrm{ox}} = 1\,\mathrm{nm}$ were simulated, as are mandatory for ultimately scaled SB-MOSFETs (15). TheSB-height in the simulations was set to $\Phi_{\mathrm{SB}} = 0.64\,\mathrm{eV}$ as is appropriate for NiSi. The results for two values of the slope of the dopant profile at theNiSi/Si-interface of 4.6 nm/dec and 1 nm/dec are shown in Fig. 2.10(a) and (b). In the case of a dopant slope of 4.6 nm/dec large shifts in the threshold voltage for channel smaller than $L = 20\,\mathrm{nm}$ were obtained. In the case of a smaller dopant slope of 1 nm/dec a device with $L = 10\,\mathrm{nm}$ showed an acceptable threshold voltage shift and good carrier injection. The experimental results showed that dopant slopes of about 1 nm/dec can be obtained with the technique of nickel silicidation induced dopant segregation. Therefore, SB-MOSFETs with dopant segregation show good scalability down to channel length of about $L = 10\,\text{nm}$.

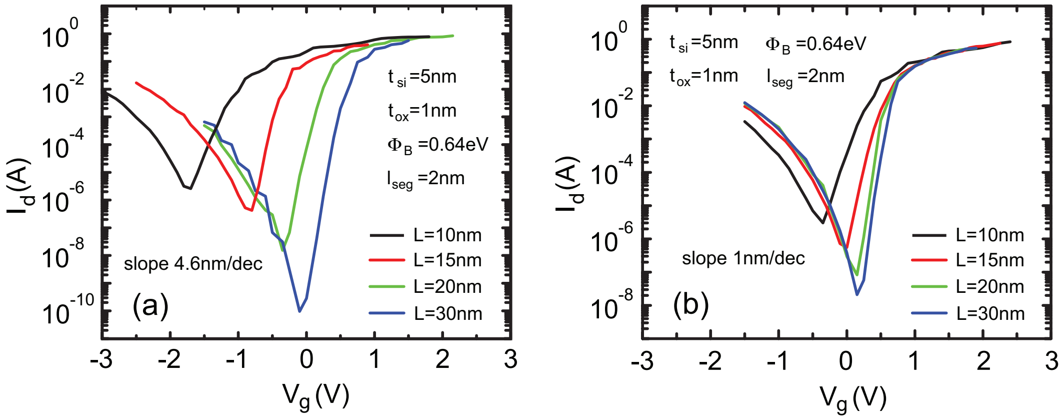

Figure 2.10: Simulated transfer characteristics of n-type SB-MOSFETs with dopant segregation for four different channel length and two different slopes of the dopant profile at the NiSi/Si-interface. (a) For a slope of the dopant profile of 4.6 nm/dec large shifts in the threshold voltages for channel length below $L = 20\,\text{nm}$ are observed. (b) In the case of a dopant slope of 1 nm/dec even a device with $L = 10\,\text{nm}$ channel length show good carrier injection and an acceptable threshold voltage shift.

2.2.4 Discussion on the Effects of NiSi/Si-Interface Roughness

The roughness of the NiSi/Si-interface was investigated with XRR (x-ray reflectivity) measurements. The measurements show that there is a substantial roughness at the interface between NiSi and Si. Fig. 2.11(a) shows a XRR measurement of a 44.7 nm NiSi layer formed with a one step annealing process. The extracted rms roughness is 2.1 nm. The inset shows a transmission electron microscopy (TEM) image of another NiSi layer clearly showing the interface roughness. This roughness has an effect on the data obtained by SIMS measurements discussed above. As the area probed by SIMS on the sample is several tenth of micrometers square large, much larger than the correlation length of the interface roughness (see TEM image in Fig. 2.11(a)), the measurement averages the actual dopant profile over the area measured by SIMS. The slopes of the As dopant profile at the NiSi/Si interface determined by SIMS are, therefore, larger than the actual value. Apart from effecting the slopes of the dopant profiles at the NiSi/Si-interface extracted from SIMS measurement, the roughness also has a significant impact on device performance in scaled SOI SB-MOSFETs. Fig. 2.11(b) shows a sketch of a SB-MOSFET of channel length L and width W. In a long channel device in which the channel length L is much larger than the peak to valley ratio of the NiSi/Si interface roughness at the source/drain contacts $\Delta\sigma_r$, the roughness has neglectable impact on device behavior. But if $\Delta\sigma_r$ becomes comparable to the channel length L, the roughness of the NiSi/Si-interface causes substantial fluctuations in channel length, leading to a large variation of device performance such as threshold voltage fluctuation, increased subthreshold slope and variations in on-current. A promising way to reduce the NiSi/Si-interface roughness is to add Pt during Ni metal deposition (30; 31). Another method to avoid channel length variations within a SB-MOSFET as a result of NiSi/Si-interface roughness is to reduce the channel width W below the correlation length of the interface roughness σ_c by fabrication of nanowire devices. This method has the additional advantage of a significantly smaller screening length for the potential distribution at the metallic source/drain channel interface due to the increased number of gates, thereby effectively thinning the SB and reducing the inherent SBH-variability as will be dicussed in detail in the following chapter.

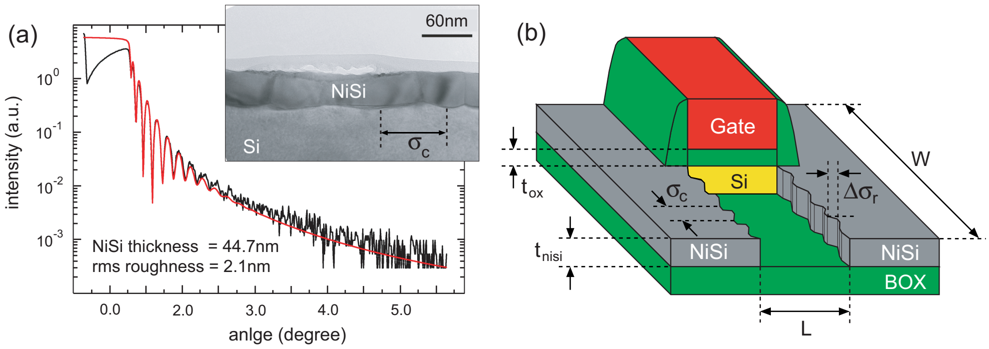

Figure 2.11: (a) The figure shows a XRR measurement of a NiSi film. The thickness of the NiSi layer was determined to be 44.7 nm. The NiSi/Si rms interface roughness was found to be 2.1 nm. The inset shows a TEM image of a NiSi layer in which the NiSi/Si-interface roughness is visible. The effect of interface roughness on SIMS spectra is to broaden the distribution and to deteriorate the slope. (b) Sketch of a SOI SB-MOSFET with NiSi source/drain contacts, channel length L and width W. Part of the Si channel has been cut out to make the NiSi roughness better visible. If the peak to valley ratio of the interface roughness $\Delta\sigma_r$ is comparable to the channel length L, roughness leads to channel length fluctuations over the width of the device causing deteriorated device performance.

2.3 Impact of Variability on the Performance of SOI SB-MOSFETs

2.3.1 Introduction

Due to the injection via tunneling, SB-MOSFETs are particularly vulnerable to variability: it is well-known that the SB at a silicide-silicon interface exhibits an inherent variation along the interface (illustrated in Fig. 2.14 (a)) of a single contact leading to an average effective SB height for this particular contact (32; 33; 34). Consequently, device-to-device variations of the electrical behavior can be expected, making investigations regarding the variability of SB-MOSFETs very important. As will be discussed below, variability leads to two effects depending on the actual height of the SB: i) a shift in threshold voltage V_{th} and ii) a variation of the on-current. For SB around 0.1 eV and below the threshold voltage shift vanishes but the devices still exhibit a variability in the on-state current.

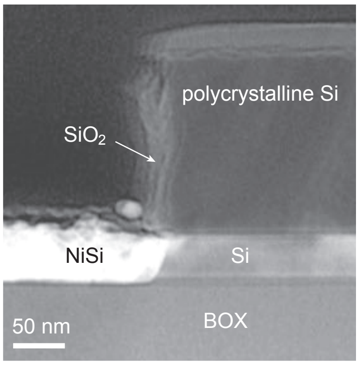

Figure 2.12: Cross section TEM image of a readily processed SB-MOSFET on 50nm SOI. The silicide-silicon interface is right at the gate edge which ensures a good gate control over the Schottky barrier.

In this chapter, the variation of V_{th} in devices with different geometric parameters is used to determine and distinguish between the main effects leading to variability. A new method is employed which is different from the traditionally used current vs. voltage and temperature (I-V-T) (35; 36) or capacitance-voltage (C-V) (37) methods. Exploiting the ambipolar operation of SB-MOSFETs there exists always a branch of the transfer characteristics belonging to a SB which is significantly larger than $k_{\mathrm{B}}T$. For instance, in a device with low SB for electron injection, Φ_{Bn}, the hole branch is chosen to extract the SB Φ_{Bh} and, in particular, its variation $\delta\Phi_{\mathrm{Bh}}$ from which Φ_{Bn} and

$\delta\Phi_{\mathrm{Bn}}$ (originally of interest) can be deduced. The reasons for this procedure are two-fold: first, the off-state of a SB-MOSFET with a SB larger than $k_{\mathrm{B}}T$ is dominated by the change of the carrier injection through the SB. Hence the off-state is independent of processing fluctuations and parasitic resistances enabling a reliable extraction of V_{th} and its variations (14). Second, an analytical model for the dependence of V_{th} on the actual SB height and the SOI and gate oxide thicknesses can be used to determine the barrier height and its variation (38). Furthermore, the same method is used to extract the inherent variability of the effective SB height in devices with dopant segregation. The analysis suggests that dopant segregation leads to a significant increase of the SB variation. Using simulations it is shown that due to this variability rather large device-to-device fluctuations of the on-state current can be expected.

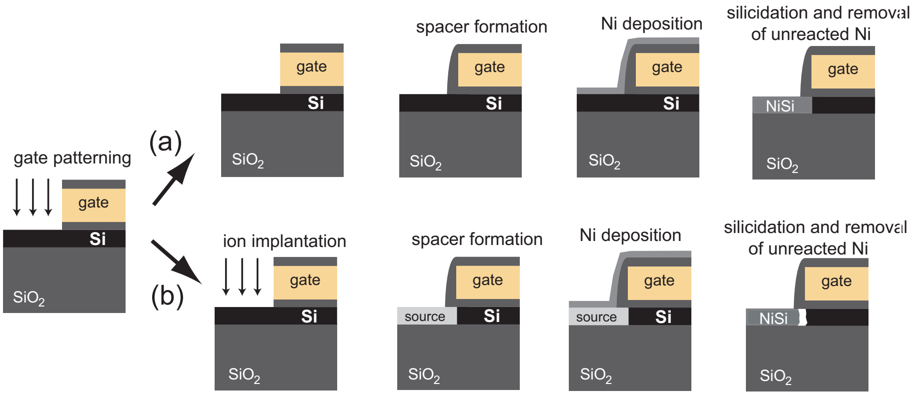

Figure 2.13: Illustration of the fabrication process of SB-MOSFETs without dopant segregation (upper part (a)) and with dopant segregation (lower part (b)).

2.3.2 Device Fabrication

SB-MOSFETs with fully nickel silicided source/drain electrodes were fabricated on (100) p-type doped SOI wafers ($N_A = 1 \times 10^{15}\,\mathrm{cm}^{-3}$) with an initial silicon thickness of $\sim$100 nm. In order to investigate the impact of t_{ox} and t_{si} on the device performance three sets of devices with $L_{\mathrm{G}} = 2\,\mu\mathrm{m}$ and $W = 40\,\mu\mathrm{m}$ were fabricated: 1) devices with $t_{\mathrm{si}} = 50\,\mathrm{nm}$ and oxide thickness of $t_{\mathrm{ox}} = 3.5\,\mathrm{nm}$; 2) devices with $t_{\mathrm{ox}} = 3.5\,\mathrm{nm}$ and $t_{\mathrm{si}} = 7.5 - 10.5\,\mathrm{nm}$; 3) devices with $t_{\mathrm{ox}} = 3.5\,\mathrm{nm}$ and $t_{\mathrm{si}} = 50\,\mathrm{nm}$ with dopant segregation. The SOI was first thinned to the desired thickness by a cycle of dry/wet thermal oxidation, followed by diluted HF stripping and etching in a modified standard cleaning solution (1 : 8 : 64 = NH_4OH : H_2O_2 : H_2O at 65 °C for 10 minutes). After a standard mesa isolation gate oxides were grown by a low temperature wet thermal oxidation process (39). 200 nm n-type poly-Si and 50 nm SiO_2 were deposited immediately after the gate oxidation in a LPCVD tool. Optical lithography and reactive ion etching (RIE) were used to define the gate. For the devices with dopant segregation ion implantation with boron (2 keV, $5 \times 10^{15}\,\mathrm{cm}^{-2}$) was done before sidewall spacers are formed. Subsequently, nickel was deposited by e-beam evaporation and the source/drain areas were fully silicided. Unreacted nickel was removed by Piranha (H_2SO_4 : H_2O_2 = 2 : 1). A TEM image of a typical device is shown in Fig. 2.12 and Fig. 2.13 illustrates the steps of the fabrication process for devices with and without dopant segregation.

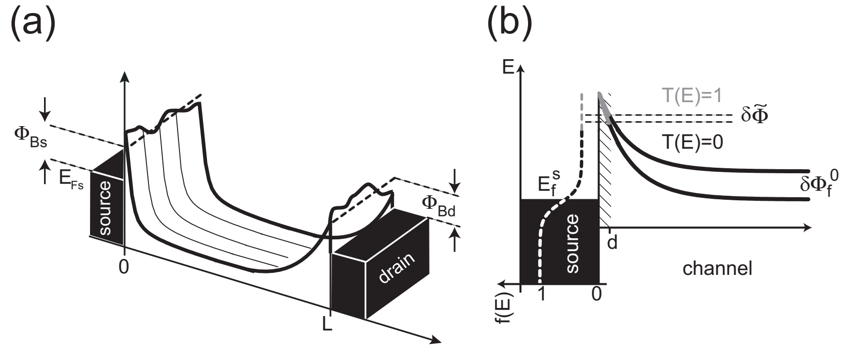

Figure 2.14: (a) Schematics of the potential distribution in a SB-MOSFET. Along the silicide-silicon contact a variation of the SB height exist leading to a different average effective SB height at source and drain. (b) shows the SB at the source contact. A tunneling distance d is introduced giving rise to an effective SB for thermal emission.

2.3.3 Measurement Method

Figure 2.14 (a) shows a schematics of the conduction band profile in a SB-MOSFET at $V_{\mathrm{ds}} = 0\,\mathrm{V}$. Along the contact-channel interfaces the variability of the SB height gives rise to average barrier heights Φ_{Bs} and Φ_{Bd} with $\delta\Phi_{\mathrm{B}} = \Phi_{\mathrm{Bs}} - \Phi_{\mathrm{Bd}} \neq 0$. In turn this results in variations of the electrical behavior from device-to-device.

In order to analyze the measurements presented below the experimental data are compared with an analytical model for the off-state of an SOI SB-MOSFET. A central ingredient of the approach is the reduction of the electrostatics of a fully-depleted SOI SB-MOSFET to a one-dimensional Poisson equation that captures the essential aspects of scaling of the gate oxide thickness t_{ox} and SOI thickness t_{si} as well as the appearance of short channel effects in laterally scaled devices. This one-dimensional Poisson equation for the surface potential $\Phi_{\mathrm{f}}(x)$ is given by (40)

$$\frac{d^2\Phi_{\mathrm{f}}(x)}{dx^2} - \frac{\Phi_{\mathrm{f}}(x) - \Phi_{\mathrm{g}} + \Phi_{\mathrm{bi}}}{\lambda^2} = \frac{\rho_{\mathrm{tot}}(x)}{\varepsilon_{\mathrm{si}}} \tag{2.1}$$

where Φ_{g} and Φ_{bi} are the gate potential and the built-in potential, respectively. The screening length $\lambda = \sqrt{\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}} t_{\mathrm{ox}} t_{\mathrm{si}}}$ is the relevant length scale on which potential variations are being screened (40). Equation (2.1) leads to an exponential screening of potential variations on the length scale λ, meaning that in particular the potential distribution at the metallic source/drain channel interfaces exhibits an exponential dependence on λ. In turn, the tunneling probability through the SB strongly depends on the gate oxide and SOI body thicknesses as has been recently shown experimentally as well as with simulations (15; 23). This exponential dependence allows replacing the actual potential profile of the SB with an effective barrier for thermal emission alone. To do so, a tunneling distance d is introduced below which the tunneling probability through the SB is set to 1 and above which no tunneling occurs (as illustrated in Fig. 2.14 (b)) (14); in silicon SB-MOSFETs d was found to be on the order of 3.7 nm (14). If the SB height of the injecting contact is significantly larger than $k_{\mathrm{B}}T$ then an analytical expression for V_{th} of an SOI SB-MOSFET can be calculated which is given by (14):

$$V_{\mathrm{th}} = \frac{k_{\mathrm{B}}T}{q} \ln\left(\frac{I_0}{C}\right)\left(\frac{1}{2} + \frac{\lambda}{d}\right) + \frac{\Phi_{\mathrm{B}}}{q}\left(\frac{\lambda}{d} - \frac{1}{2}\right) + \frac{\Phi_{\mathrm{bi}}}{q}. \tag{2.2}$$

where $C = M_{\mathrm{s}} \times \frac{2e}{h^2}\sqrt{2\pi m_{\mathrm{l}}^{\star}}\,(k_{\mathrm{B}}T)^{3/2}$ and M_{s} accounts for higher subbands as in Ref. (41). Furthermore, I_0 is a constant current level at which V_{th} is extracted and Φ_{bi} is the built-in potential; all other symbols have their usual meaning.

Now, concentrating on the branch of the ambipolar transfer characteristics that belongs to the SB significantly larger than $k_{\mathrm{B}}T$ Eqn. (2.2) can be used to relate a variation of V_{th} to the two main contributions of variability, namely Φ_{B} and t_{si}:

$$\delta V_{\mathrm{th}} = \underbrace{\frac{k_{\mathrm{B}}T}{q} \ln\left(\frac{I_0}{C}\right)\lambda\frac{\delta t_{\mathrm{si}}}{t_{\mathrm{si}}}\frac{1}{2d} + \frac{\Phi_{\mathrm{B}}}{q}\lambda\frac{\delta t_{\mathrm{si}}}{t_{\mathrm{si}}}\frac{1}{2d}}_{\text{due to }\delta t_{\mathrm{si}}} \tag{2.3}$$

$$+ \underbrace{\frac{\delta\Phi_{\mathrm{B}}}{q}\left(\frac{\lambda}{d} - \frac{1}{2}\right)}_{\text{due to }\delta\Phi_{\mathrm{B}}}.$$

The following insights can be obtained from Eqn. (2.3): i) obviously the larger the SOI thickness variation δt_{si} the larger δV_{th}; the same is true for the inherent SB height variation $\delta\Phi_{\mathrm{B}}$. ii) More important is that for constant δt_{si} the V_{th}-variation increases proportional to $\lambda/t_{\mathrm{si}} \propto 1/\sqrt{t_{\mathrm{si}}}$. iii) An effective way to reduce δV_{th} is decreasing $t_{\mathrm{ox}}/\varepsilon_{\mathrm{ox}}$ and lowering Φ_{B}. In addition, Eqn. (2.3) shows that for thin t_{ox} and thick t_{si} the first two terms of Eqn. (2.3) can be neglected leading to $\delta V_{\mathrm{th}} \propto \delta\Phi_{\mathrm{B}}$. Thus, knowing the gate oxide and SOI thicknesses as well as d allows to extract $\delta\Phi_{\mathrm{B}}$ from measuring the variation of V_{th}. Moreover, for thin t_{si} where the first two terms have to be taken into account a measurement of the SOI thickness variation (using, e.g., ellipsometry) allows obtaining $\delta\Phi_{\mathrm{B}}$ in the case of thin SOI, too. The different contributions to variability in an SOI SB-MOSFET can thus be distinguished.[1]

To measure the device-to-device variations and in particular the variation of the SB height the following procedure was used: a large number of devices was fabricated and each device was measured twice with source and drain, i.e. the injecting contact, being interchanged. The V_{th} values for a large number of devices were plotted in a histogram and fitted by a Gaussian distribution. With the knowledge of d (extracted by fitting the measured S values of various devices from each group of investigated devices to $S \approx \frac{k_{\mathrm{B}}T}{q}\ln 10\left(\frac{1}{2}+\frac{\lambda}{d}\right)$ (14)), the standard deviation $\delta\Phi_{\mathrm{B}}$ and the mean SB height can then be calculated from Eqn. (2.3) and (2.2). [2]

2.3.4 Results

Thick SOI, Thin Gate Oxide

As stated above it is possible to extract the inherent SB inhomogeneity $\delta\Phi_{\mathrm{B}}$ from devices with thick SOI and thin gate oxide since in this case $\delta V_{\mathrm{th}} \propto \delta\Phi_{\mathrm{B}}$. In Fig. 2.15 (a) the transfer characteristics of a SB-MOSFET with $t_{\mathrm{si}} \approx 50\,\mathrm{nm}$ and $t_{\mathrm{ox}} = 3.5\,\mathrm{nm}$ for $V_{\mathrm{ds}} = +1\,\mathrm{V}$ (black curve) and $V_{\mathrm{ds}} = -1\,\mathrm{V}$ (gray curve) are plotted. The gray curve had to be shifted by $+1\,\mathrm{V}$ to lie on top of the black curve for $V_{\mathrm{ds}} = -1\,\mathrm{V}$ because of the ambipolar behavior of SB-MOSFETs. The subthreshold slope of the electron branch is $S = 210\,\mathrm{mV/dec}$ before and after source/drain exchange. δV_{th} is determined at a constant current level of 10^{-8} A. The inset shows the distribution of V_{th} values for 120 devices with a mean V_{th} value of 0.67 V and a standard deviation of $\delta V_{\text{th}} = 0.026\,\text{V}$. Using Eqn. (2.3) $\delta\Phi_{\text{B}}$ is determined to be 0.01 eV and Eqn. (2.2) gives for $\Phi_{\text{B}} = 0.68\,\text{eV}$, slightly higher than the reported value of 0.64 eV (26).

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[1] In the analysis a constant oxide thickness is assumed. A variation of the oxide thickness would give two additional terms similar to the ones for t_{si}. For the investigated devices the measured homogeneity of the gate oxide is good enough to ensure that the contribution from oxide thickness variability is negligible compared to the term due to the Schottky barrier height variability.

[2] It has been discussed in a previous publication (42) that there is only a weak dependence of the tunneling distance d on the SOI and gate oxide thickness.

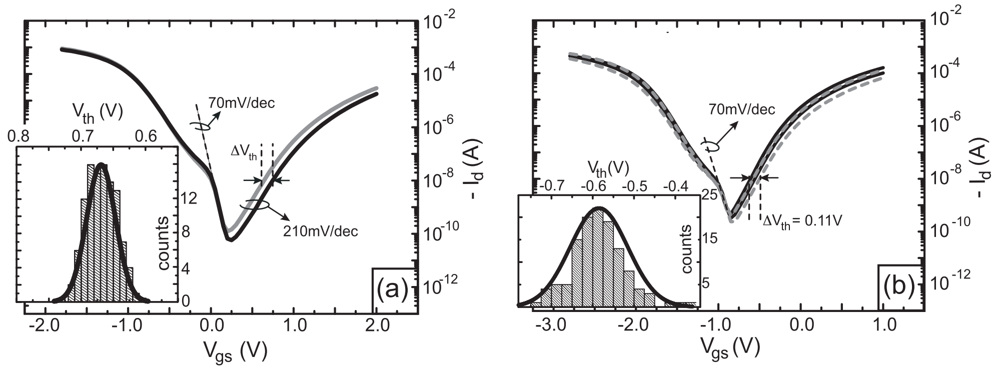

Figure 2.15: (a) Transfer characteristics of a SB-MOSFET with $t_{\text{ox}} = 3.5\,\text{nm}$ and $t_{\text{si}} \approx 50\,\text{nm}$ with source/drain exchange. For the electron branch an inverse subthreshold slope of $S = 210\,\text{mV/dec}$ is found. The inset shows the V_{th}-distribution of ∼120 devices with a mean value of $V_{\text{th}} = 0.67\,\text{V}$ and a standard deviation of $\delta V_{\text{th}} = 0.026\,\text{V}$. (b) Transfer characteristics of two different SB-MOSFET with $t_{\text{ox}} = 3.5\,\text{nm}$ and $t_{\text{si}} = 7.5 - 10.5\,\text{nm}$ with source/drain exchange. For the electron branch inverse subthreshold slope of $S = 175\,\text{mV/dec}$ and $179\,\text{mV/dec}$ are found. The variability in the present case stems from $\delta\Phi_{\text{B}}$ and δt_{si}. The inset shows the V_{th}-distribution of ∼140 devices with a standard deviation of $\delta V_{\text{th}} = 0.08\,\text{V}$.

Thin SOI, Thin Gate Oxide

The analysis is more complicated for devices with thin gate oxides and thin SOI. In this case the terms due to δt_{si} in Eqn. (2.3) cannot be neglected. Figure 2.15 (b) shows the transfer characteristics for two devices with thin $t_{\text{si}}(\simeq 7.5 - 10.5\,\text{nm})$ and thin $t_{\text{ox}}(= 3.5\,\text{nm})$ before and after source/drain exchange to illustrate the two factors contributing to δV_{th}. The V_{th}-shift at the electron branch for the solid black curves is 0.05 V and for the dashed gray curves 0.08 V. Within one device t_{si} can be assumed to be constant, so that these shifts are due to the inherent SB height variation alone. But the maximum V_{th}-shift between the two devices of 0.11 V (as indicated in Fig. 2.15 (b)) is due to δt_{si} and $\delta\Phi_{\text{B}}$. In order to distinguish between the two contributions the V_{th}-distribution for ≈ 140 devices is plotted. Fitting a Gaussian distribution function to the histogram, a mean V_{th} of $-0.58\,\text{V}$ and a standard deviation of $\delta V_{\text{th}} = 0.08\,\text{V}$ are obtained. The mean value of t_{si} and the standard deviation δt_{si} are known from an ellipsometer mapping of the samples prior to processing. Thus, $\delta\Phi_\mathrm{B}$ can be calculated with a Gaussian error propagation from Eqn. (2.3). As it turns out the main contribution to δV_th stems from the variation of the SB which is $\delta\Phi_\mathrm{B} = 0.03\,\mathrm{eV}$, much larger than the value found in case of thick SOI. A possible reason for this strong increase of variation might be the growth of the silicide in thin SOI films. The thinner the SOI the faster the nickel diffusion leading to a microstructure depending on t_si. If this is the case then it would be crucial in SOI SB-MOSFETs to avoid any variation in t_si since this variation does not manifest itself in the electrical behavior but is amplified by the silicide growth leading to a much larger variability through the formation of the Schottky barrier. Investigations addressing this issue are topics for further research.

Dopant Segregation

In order to improve the carrier injection into the channel of a SB-MOSFET the Schottky barriers at the metal-semiconductor interfaces has to be made highly transmissive. A possibility to achieve this is to introduce a thin highly doped layer at the contact interface. This causes a strong band bending thereby increasing the tunneling probability of carriers through the barrier. Such a non-uniform doping profile can be obtained with the technique of dopant segregation during silicidation. Figure 2.16 (a) displays a sketch of the conduction and valence band profile for a SB-MOSFET with boron dopant segregation showing a strongly thinned Schottky barrier. In turn this yields a significantly reduced effective Schottky barrier height for hole injection.

In Fig. 2.16 (b) transfer characteristics of a device with $t_\mathrm{si} = 50\,\mathrm{nm}$ and $t_\mathrm{ox} = 3.5\,\mathrm{nm}$ and dopant segregation are shown. During silicidation the implanted boron segregates to the silicon-silicide interface forming a thin, highly doped layer. Due to the better carrier injection the thermionic emission region in the hole branch of the characteristics is greatly extended (see main panel of Fig. 2.16 (b)). Therefore, the electron branch was taken in order to extract the V_th-distribution which is shown in the inset of Fig. 2.16 (b). Since the contribution of δt_si to δV_th is negligible, $\delta\Phi_\mathrm{B}$ can be calculated from Eqn. (2.3) to be $0.02\,\mathrm{eV}$. This is twice as much as for the devices without dopant segregation of the same geometry. The reason for this is the discreteness of the dopants leading to local changes of the potential distribution of the Schottky barrier and hence to an increased variability.

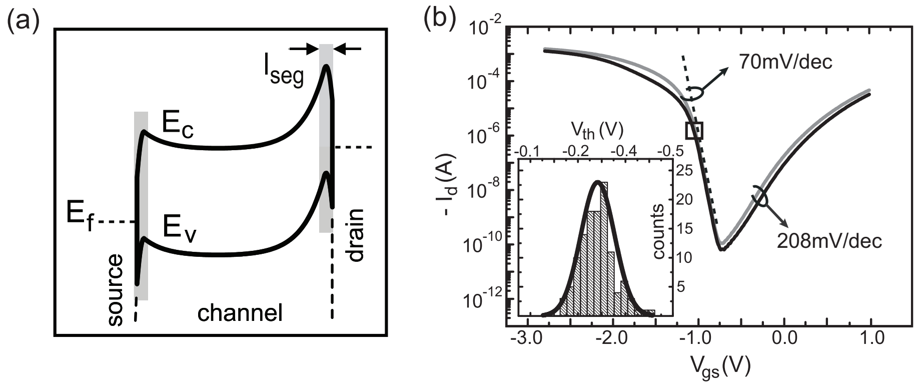

Figure 2.16: (a) Effect of dopant segregation on the band structure: a highly doped interface layer is formed that leads to a reduction of the effective SB height. (b) Transfer characteristics of a SB-MOSFETs with dopant segregation and source/drain exchange. The inset shows again the V_{th}-distribution for ~120 devices.

Simulations

In the preceding sections it was found that it is mainly the variation of the Schottky barrier that leads to a fluctuation of V_{th}. However, one might argue that if the SB is only low enough the variation of the threshold voltage will vanish. While this is indeed the case the important point to keep in mind is that the V_{th}-variation was only a means to extract the variability of the SB height without the influence of, e.g., parasitic resistances and the variability due to device processing. Even for very low Schottky barriers where no V_{th}-shift is expected, the variation $\delta\Phi_{\mathrm{B}}$ will significantly impact the on-state of the device. In order to study this effect simulations of SOI SB-MOSFETs have been performed, based on a self-consistent solution of the Schrödinger equation using the non-equilibrium Green's function formalism and the one-dimensional, modified Poisson equation (2.1). To numerically compute the Green's functions Datta's approach (29) has been used. A one-dimensional finite difference scheme with lattice constant a and nearest neighbor hopping and a quadratic dispersion relation in the conduction and valence band are used. Flietner's dispersion relation (43) has been employed in order to describe the complex band structure in the band gap. Furthermore it is assumed that the first subband contributes most to the current and hence the expressions for charge and current are averaged over the direction of W only (see Ref. (28) for details). Higher subbands are accounted for by a numerical factor as in Ref. (41).

Figure 2.17 (a) shows simulated transfer characteristics of a SB-MOSFET with an SOI thickness of $t_{\mathrm{si}} = 7\,\mathrm{nm}$, a channel length of $L = 90\,\mathrm{nm}$ and a gate oxide thickness of $t_{\mathrm{ox}} = 2\,\mathrm{nm}$ for Schottky barrier heights of $\Phi_{\mathrm{B}} = 0.3\,\mathrm{eV}$ and $0.32\,\mathrm{eV}$ (dashed curves) as well as of $\Phi_{\mathrm{B}} = 0.02\,\mathrm{eV}$ and $0.02\,\mathrm{eV}$ (solid curves).[3] In the case of the low barriers the V_{th}-shift tends to zero but the variability of Φ_{B} manifests itself in a variation of the on-state current (Note the qualitative similarity between the simulated transfer characteristic and the experimental curve in Fig. 2.8.). In contrast, in the case of a larger barrier, a fluctuation in Φ_{B} leads to a V_{th}-variation *and* a variation in the on-state current. As was already discussed above, scaling down t_{ox} is a means to decrease the impact of a variability of the Schottky barrier height (cf. Eqn. (2.3)). The reason for this is that scaling down t_{ox} decreases λ - the relevant length scale for potential variation in the channel - and therefore lowers the relative importance of the Schottky barrier on the electrical characteristics of an SB-MOSFET.

Figure 2.17 (b) shows simulated on-state currents and the relative change in on-current $\Delta I_{\mathrm{d}}/I_{\mathrm{d}}^{\mathrm{SB=0.04eV}} = \left(I_{\mathrm{d}}^{\mathrm{SB=0.02eV}} - I_{\mathrm{d}}^{\mathrm{SB=0.04eV}}\right)/I_{\mathrm{d}}^{\mathrm{SB=0.04eV}}$ due to a variation of the Schottky barrier height for a single-gate SB-MOSFET with channel length $L = 90\,\mathrm{nm}$, SOI thickness $t_{\mathrm{si}} = 7\,\mathrm{nm}$ and $\Phi_{\mathrm{B}} = 0.04\,\mathrm{eV}$ ($0.02\,\mathrm{eV}$) as a function of the gate oxide thickness; the parameters in the simulation were chosen in order to avoid the appearance of short channel effects in the range of simulated gate oxide thicknesses. Even for a Schottky barrier as low as $0.04\,\mathrm{eV}$, a reduction of the gate oxide thickness from $t_{\mathrm{ox}} = 4\,\mathrm{nm}$ to $t_{\mathrm{ox}} = 1\,\mathrm{nm}$ substantially improves the on-state current by a factor of four (15) while the variability in on-current is reduced from 28% to 15%. This underlines the importance of using thin gate oxides in SB-MOSFETs to reduce variability and improve the on-state current at the same time. Apart from reducing the oxide and the silicon thickness a further increase of on-state current and decrease of variability is obtained in a multigate device layout (40) and by using high-k gate dielectrics. As will be discussed in the next section, the reduced contact size of a multigate device layout is beneficial for avoiding the inherent variability of the Schottky barrier height, however, at the expense of requiring perfect control over the size variations/variability of the channel thickness/diameter (cf. Eqn. (2.3)).

2.3.5 Discussion

Several groups have investigated SB variability and inhomogeneities of macroscopic Schottky contacts for different metals in contact with silicon. In (45)

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[3] The width of the simulated devices is $1\,\mu\mathrm{m}$ in difference to the experimental devices that have a width of $40\,\mu\mathrm{m}$. Since an average SBH is used in the simulations the width has no effect on the simulation results. The effect of variability is investigated by running several simulations with slightly different average SBH values.

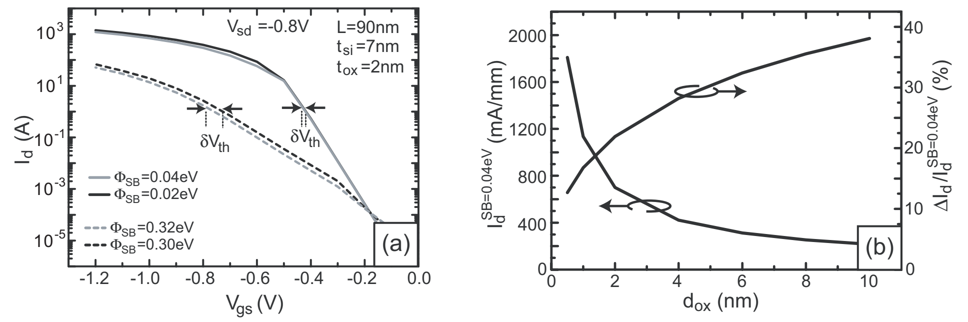


Figure 2.17: (a) Simulated transfer characteristics for $t_{\text{ox}} = 2\,\text{nm}$ and $t_{\text{si}} = 7\,\text{nm}$ for two different mean SB heights. (b) $t_{\text{si}} = 7\,\text{nm}$, $t_{\text{ox}} = 2\,\text{nm}$, $L = 90\,\text{nm}$, $\Phi_B = 0.04\,\text{eV}$, dependence of on-current on t_{ox} and relative change in on-current (44).

the authors obtained a standard deviation of the SBH of identically prepared titanium silicon SB-diodes of 0.013 eV from a fit of a gaussian to the distribution of SBH obtained from I-V measurements. Ru and coworkers (46) reported a standard deviation of the SBH for NiSi-Si diodes annealed at 500 °C of 0.085 eV from I-V measurements. The larger value compared to our results for the SBH variability can be explained by the different annealing temperatures used (32). In (33) the variability in PtSi-Si Schottky contacts was investigated. From C-V and I-V measurements on identically prepared diodes a standard deviation of the SBH of 0.01 eV and 0.02 eV was obtained, respectively. The authors also used ballistic electron emission microscopy (BEEM) to determine the inhomogeneities in the SBH on the scale of a few nanometers. The standard deviation of the SBH measured with BEEM was also 0.01 eV. Typical variations in the SBH were 1×10^{-3} eV/nm and a decay length for fluctuations in SBH was measured to be 18 nm. These results confirm the variability of the SBH in macroscopic Schottky contacts and between such contacts. The variability of the SBH in a single contact can be suppressed by decreasing its size below the characteristic length of the potential distribution at the metal/semiconductor interface as has been pointed out in (47; 48; 34). A way to reduce the inhomogeneity of the SBH in Schottky contacts would therefore be to employ nanowire devices. Even though nano-scale Schottky contacts can be expected to have less variability of the SBH along the contact interface, this does not eliminate the variability between different contacts. Therefore it is also in this case important to use thin oxides and to precisely control the silicon thickness (e.g. the diameter of the NW) in multigate devices (cf. Eqn. (2.3)).

2.4 Summary

- **Scaling issues of n-type dopant segregation SB-MOSFETs**
  Nickel silicidation induced dopant segregation has been thoroughly investigated, in order to determine the scaling limits of n-type SB-MOSFETs with arsenic dopant segregation.

  It was found that the slope of the dopant distribution into Si at the NiSi/Si-interface increases with increasing NiSi-thickness and increasing implantation energy.

  Studying the dopant concentration at the NiSi/Si-interface as a function of NiSi thickness and implantation energy it was found, that for each implantation energy, there is an optimal NiSi thickness, and visa versa, for which the dopant concentration at the interface stays at the as-implanted level. This NiSi thickness is about 3-4 times the depth of the concentration peak in the as-implanted samples. No influence of the dopant concentration on the slope of the dopant profile after dopant segregation has been observed.

  Employing a two-step silicidation process an excellent slope of the dopant profile after segregation of 3.2 nm/dec for a 13 nm NiSi layer has been obtained.

  On the basis of the experimental data simulations have been performed to investigate the scaling limits of n-type SB-FETs with arsenic dopant segregation. The importance of the slope of the lateral doping profile at the NiSi/Si contact interface has been pointed out and it was shown that this profile can be as steep as 1-2 nm/dec. Self-consistent Schrödinger-Poisson simulations of ultrathin-body SB-FETs showed that dopant segregation devices are scalable down to channel length of $L = 10\,\text{nm}$.

- **Impact of Variability on the Performance of SOI Schottky Barrier MOSFETs**
  The variability in SOI SB-MOSFETs has been investigated. By measuring the threshold voltage shifts by exchanging the source/drain contacts in a large number of devices it was possible to determine the device-to-device fluctuations of the electrical behavior of SOI SB - MOSFETs. It is found that the main contribution stems from the variability of the actual SB height. However, a variation of the SOI thickness in thin-body SOI seems to translate into a large variation of the electrical characteristics through an additional variability of the SB height. Moreover, dopant segregation during silicidation leads to

strongly decreased effective SB heights but on the other hand increases the variability of the SB. Scaling down the gate oxide thickness and in particular using multigate architectures allows reducing the variability. Simulations of SB-MOSFETs have confirmed that for larger SBHs fluctuations in Φ_B lead to a shift in threshold voltage as well as to a a variation in on current whereas for small SBHs the variation in V_th tends to zero but the variabilty still manifest itself in the on-current. Reducing the oxide thickness of the simulated devices led to a decrease in variability and a large improvement of the on-current at the same time.

Chapter 3

Strained Silicon - a High Mobility Channel Material

3.1 Introduction

In order to increase the performance of aggressively scaled devices, strain is used to increase the carrier mobility. As has already been discussed above, the performance enhancement of FET devices has relied in part on the steady increase of channel carrier velocity due to gate-length scaling. However, the intrinsic transport properties have remained constant, i.e. that of the relaxed silicon lattice. Strain is employed to modify the subband structure of Si with the aim of increasing carrier mobility. This is achieved by reducing the conduction mass either by band warping or splitting of degeneracies and increasing the population of subbands with a small mass in transport direction, as well as reducing intervalley scattering. To understand the effects of strain on transport in MOSFET channels three aspects of the strain altered subband structure are important:

1. the out-of-plane mass in confinement direction that determines the magnitude of the energy level shift due to an applied gate voltage;
2. the conductivity effective mass along the transport direction that affects mobility; and
3. the in-plane constant energy contour which determines the 2D DOS for the subband.

The on-current per channel width of a MOSFET can be written as

$$I_{\mathrm{on}} \approx q n_{\mathrm{s}}^{\mathrm{source}} \cdot v_{\mathrm{s}} \tag{3.1}$$

where $n_\mathrm{s}^\mathrm{source}$ is the charge density and v_s the carrier velocity near the source (49). In order to obtain a large on-current an ideal two dimensional (planar) device should therefore have a carrier density as large as possible and a high carrier velocity. In a long channel device where transport is dominated by diffusion, the carrier velocity is given by the product of the low field mobility $\mu_\mathrm{s} = q\tau/m_\mathrm{x}$ and the electric field near the source E_s ($v_\mathrm{s} = \mu_\mathrm{s}E_\mathrm{s}$). An improvement of the low field carrier mobility by reduction of the transport mass, m_x, and scattering directly improves I_on. In the limit of an ultra-short channel device with ballistic transport the velocity in eqn. 3.1 is the injection velocity v_inj. If the carrier density n_s is low, the Boltzmann distribution can be used and the injection velocity takes the form (41; 50):

$$v_\mathrm{inj} \approx \sqrt{\frac{12}{\pi^2}} \cdot v_\mathrm{th} \propto m_\mathrm{x}^{-1/2} \tag{3.2}$$

where v_th is the thermal velocity and m_x is the mass in transport direction. For large carrier densities the Fermi-Dirac distribution has to be employed and the injection velocity is under these conditions given by (51; 52):

$$v_\mathrm{inj} = \frac{4}{3\pi} v_\mathrm{F} = \frac{4}{3\pi}\sqrt{\frac{4n_\mathrm{s}}{m_\mathrm{x}D_\mathrm{2d}}} \tag{3.3}$$

where $D_\mathrm{2d} = 2g_\mathrm{v}\frac{\sqrt{m_\mathrm{x}m_\mathrm{y}}}{\pi\hbar^2}$ is the two dimensional density of states of the subband with the valley degeneracy g_v and m_y is the mass along the channel width. Even for a ballistic device a reduction of the mass in transport direction, m_x, improves the injection velocity v_inj, in both, the low- and high carrier density region and, therefore, the on-current.

Subband engineering through strain also effects the charge carrier density by changing the gate capacitance since $n_\mathrm{s} = C_\mathrm{g}(V_\mathrm{g} - V_\mathrm{th})$. The gate capacitance C_g is the series combination of the oxide capacitance C_ox and the inversion layer capacitance C_inv (53):

$$C_\mathrm{g} = C_\mathrm{ox}\frac{1}{1+\frac{C_\mathrm{ox}}{C_\mathrm{inv}}} = C_\mathrm{ox}\frac{1}{1+\frac{\epsilon_\mathrm{ox}}{t_\mathrm{ox}C_\mathrm{inv}}} \tag{3.4}$$

where ϵ_ox is the dielectric constant of the gate oxide. The inversion layer capacitance C_inv degrades the gate capacitance from its maximum value C_ox and therefore reduces the on-current. A large inversion layer capacitance is therefore important for a large gate capacitance that means a high carrier density. As stated in eqn. 3.4 the influence of C_inv on the gate capacitance depends on the gate oxide thickness t_ox and becomes important for thin gate oxides below about 2 nm as being used in state-of-the-art MOSFETs. The inversion layer capacitance itself is composed of two contributions (54; 55):

$$\frac{1}{C_{\mathrm{inv}}} = \frac{1}{C_{\mathrm{inv}}^{\mathrm{DOS}}} + \frac{1}{C_{\mathrm{inv}}^{\mathrm{thickness}}} \tag{3.5}$$

one due to the density of states and the other due to the finite inversion layer thickness. These are given by:

$$C_{\mathrm{inv}}^{\mathrm{DOS}} \propto D_{\mathrm{2d}} \propto m_{\mathrm{x}}^{1/2} m_{\mathrm{y}}^{1/2} \tag{3.6}$$

$$C_{\mathrm{inv}}^{\mathrm{thickness}} \approx \frac{\epsilon_{\mathrm{si}}}{t_{\mathrm{inv}}} \propto m_{\mathrm{z}}^{1/3} \cdot n_{\mathrm{s}}^{1/3} \tag{3.7}$$

While the density of states component is determined by the in-plane masses m_{x} and m_{y}, the out of plane mass m_{z} influences the component of the finite inverison layer thickness. To obtain a large carrier density for given values of V_{g} and t_{ox} the inversion layer capacitance should be large and therefore large values of the in-plane masses m_{x}, m_{y} and the out-of-plane mass m_{z} are favorable (56; 10). But as stated above a large mass m_{x} in transport direction degrades the carrier velocity. To maximize the on-current by strain engineering a trade-off between a large carrier velocity determined by the mass in transport direction m_{x} and a large carrier density determined by m_{x}, m_{y} and m_{z} has to be found.

3.1.1 Strain Effects on Si Bandstructure

In this section the effect of certain types of strain on the conduction and valence band of Si are discussed. Since the (001)-surface is nearly exclusively used for device fabrication discussion is limited to this surface. Many properties of the bandstrucutre of solids can be deduced from the symmetry properties of the crystal lattice (57). Symmetry degeneracies of energy levels result from the commutation of the crystal Hamiltonian with the symmetry operators. The six-fold degeneracy of the conduction band minima of Si that lie along the Δ-directions at about $k_{\mathrm{min}} = 0.85 \cdot (2\pi/a_{\mathrm{si}})$ are a consequence of crystal symmetry. Also a result of symmetry is that the valence band maxima of all group IV and III-V semiconductors with the heavy and light hole bands degenerate lie at the Γ-point. Strain effects the band structure by altering the symmetry properties of the crystal lattice thereby lifting symmetry determined degeneracies of energy levels and causing band warping (58).

Any type of strain ϵ_{ij} can be decomposed into the sum of a hydrostatic strain tensor $\epsilon_{\mathrm{M}}\delta_{ij}$ related to the dilation or volume change and a traceless strain deviator tensor $\epsilon_{ij}^{'}$ related to the distortion (59):

$$\epsilon_{ij} = \epsilon_{ij}^{'} + \epsilon_{\mathrm{M}}\delta_{ij} \tag{3.8}$$

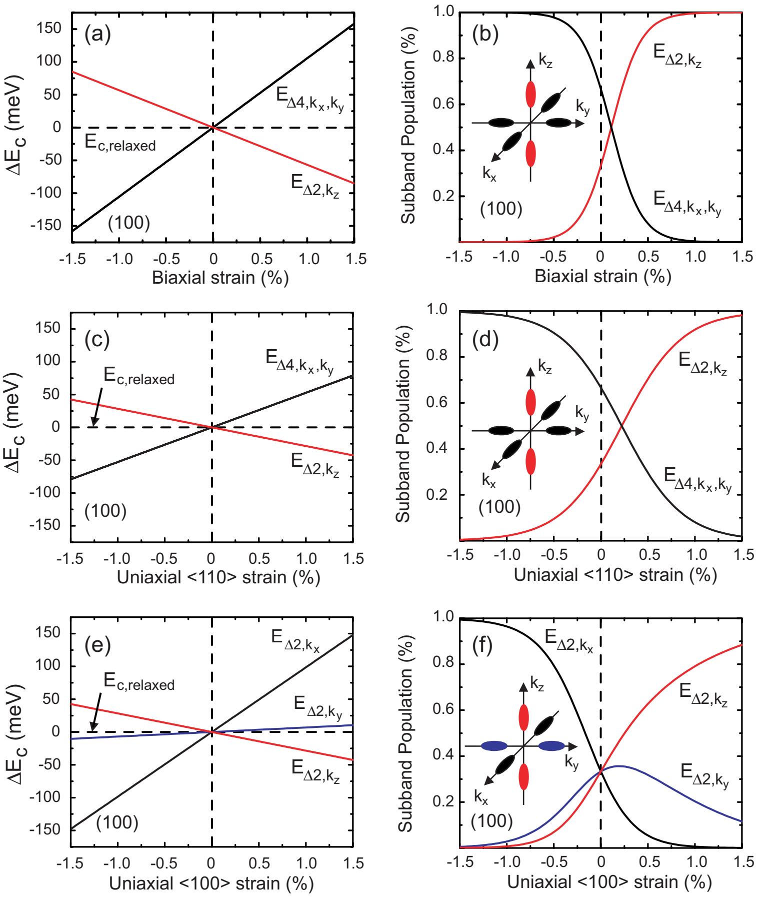


Figure 3.1: Left column: Strain induced splitting and energy shifts of the minima of the conduction band valleys calculated by deformation potential theory for biaxial, uniaxial strain along $< 110 >$ and uniaxial strain along $< 100 >$. Right column: The corresponding strain induced repopulation of the split conduction band valleys.

where $\epsilon_{\mathrm{M}} = (1/3)\mathrm{trace}(\epsilon)$. For Si a hydrostatic strain does not change the symmetry of the crystal but shifts the energy levels without effecting degeneracies. It is therefore ineffective for mobility enhancement but can cause threshold voltage shifts due to an altered band gap. The shear component $\epsilon_{ij}^{'}$ of the strain tensor is responsible for mobility increasement (60). It reduces the symmetry of the crystal thereby removing degeneracies of energy levels and warps the bands. In the following the effect of three types of strain on the conduction band of Si are first discussed, followed by an outline of the effect of strain on the valence band of Si.

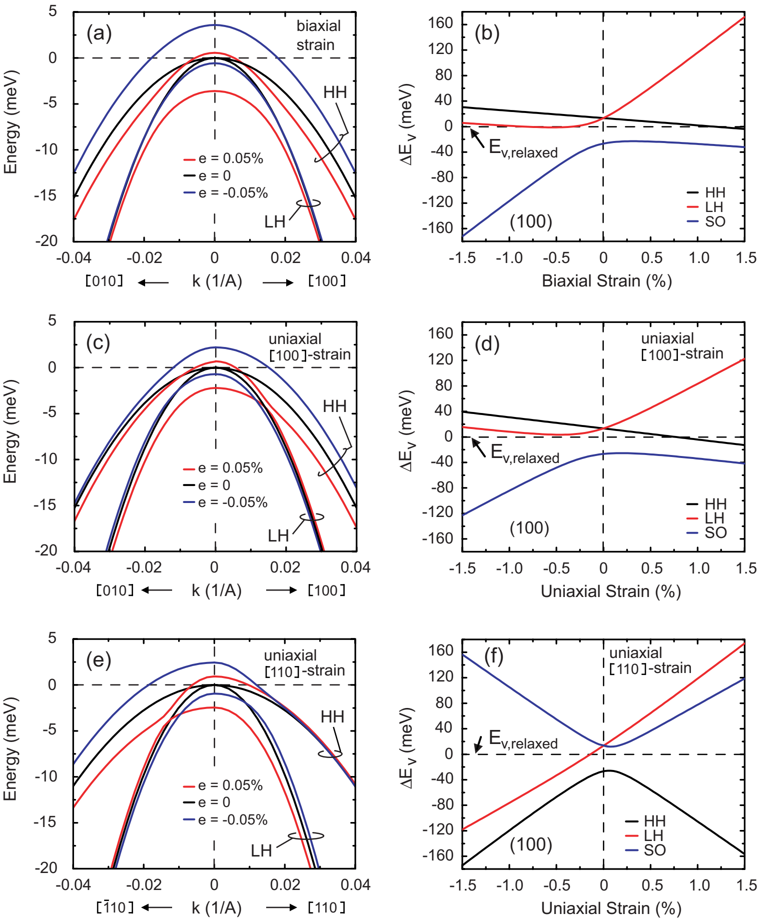


Figure 3.2: Right column: Valence bands for biaxial, uniaxial [100]- and uniaxial [110]-strain calculated using the Bir-Pikus strain Hamiltonian. Right column: The corresponding energy shifts as calculated by deformation potential theory.

Si Conduction Band

The effect of different types of strain on the symmetry properties of the Si crystal can be illustrated by its effect on a cube since a cube has the same symmetry group as the Si crystal unit cell.

The shear component of in-plane biaxial strain removes the equivalence of the in-plane x-y-directions and the out-of-plane z-direction by elongating one and shortening the other (Eqn. 3.9). Under in-plane biaxial tensile strain for example the z-axis is shortened while the x-y-direction are equally elongated. While the z-axis is still a fourfold rotational axis the x- and y-axis are now reduced to twofold rotational axis. The symmetry group is now that of a tetragonal unit cell (60). The conduction band minima along the z-axis therefore split from the minima along the x- and y-axis that are still degenerated. Fig. 3.1(a) and (b) show the strain induced conduction band splitting and energy shifts calculated using deformation potential theory (61) and the population of the subbands calculated using the simplifying assumption of Boltzmann statistics for in-plane biaxial tensile and compressive strain.

$$\epsilon'_{\mathrm{biax}} = \frac{1}{3} \cdot \begin{pmatrix} \epsilon_{\mathrm{xx}} - \epsilon_{\mathrm{zz}} & 0 & 0 \\ 0 & \epsilon_{\mathrm{xx}} - \epsilon_{\mathrm{zz}} & 0 \\ 0 & 0 & -2(\epsilon_{\mathrm{xx}} - \epsilon_{\mathrm{zz}}) \end{pmatrix} \tag{3.9}$$

The effect of uniaxial strain along any of the x-,y-,z-axis on crystal symmetry is slightly different from the in-plane biaxial strain case. This becomes obivous by comparing the strain deviator tensors for in-plane biaxial and for example uniaxial strain along the x-axis (Eqn. 3.10). In the uniaxial case the relative length changes along the y- and z-direction are different from each other. The symmetry is in this case of orthorhombic type. The sixfold degenerate conduction band minima therefore splits into three twofold degenerate sets of valleys. The conduction band splitting and energy shifts as well as the valley populations are shown in fig. 3.1(e) and (f).

$$\epsilon'_{\mathrm{uniax,[100]}} = \frac{1}{3} \cdot \begin{pmatrix} 2\epsilon_{\mathrm{xx}} - \epsilon_{\mathrm{zz}} & 0 & 0 \\ 0 & -(\epsilon_{\mathrm{xx}} - \epsilon_{\mathrm{zz}}) & 0 \\ 0 & 0 & -(\epsilon_{\mathrm{xx}} - 2\epsilon_{\mathrm{zz}}) \end{pmatrix} \tag{3.10}$$

The symmetry of the Si crystal is further reduced by applying an uniaxial strain along the $\langle 110 \rangle$-direction. The strain deviator tensor is in this case:

$$\epsilon'_{\mathrm{uniax,[110]}} = \frac{1}{3} \cdot \begin{pmatrix} \frac{\epsilon_{\mathrm{xx}}}{2} - \epsilon_{\mathrm{zz}} & \frac{\epsilon_{\mathrm{xx}}}{2} & 0 \\ \frac{\epsilon_{\mathrm{xx}}}{2} & \frac{\epsilon_{\mathrm{xx}}}{2} - \epsilon_{\mathrm{zz}} & 0 \\ 0 & 0 & -2(\frac{\epsilon_{\mathrm{xx}}}{2} - \epsilon_{\mathrm{zz}}) \end{pmatrix} \tag{3.11}$$

where ϵ_{xx} is the strain applied along the $\langle 110 \rangle$-direction. In this case the unit cell in x-y-plane is of rhombic shape. Compared to the unstrained case the z-axis is reduced to a twofold rotational axis and the two in-plane $\langle 110 \rangle$-directions are not equivalent to each other anymore. The Si conduction band splits into the twofold degenerate valleys along the z-axis and the fourfold degenerate valleys in the x-y-plane (fig. 3.1(c) and (d)). It has been further shown by Uchida (62) that uniaxial tensile strain along the $\langle 110 \rangle$-direction warps the energy surface of the k_{z}-valleys leading to a lighter effective electron mass in the direction of strain.

For all three types of strains discussed above only the tensile type is effective for electron mobility enhancement (63; 64). The strain induced splitting of the six conduction band minima results, for tensile strain, in a lowering and preferential occupation of the Δ_2 valleys on the k_z-axis. These valleys have the lighter effective electron mass m_t in transport direction.

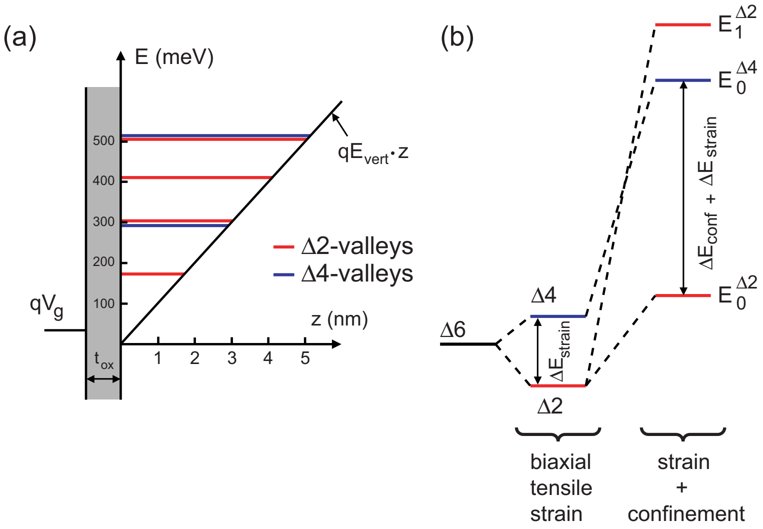


Figure 3.3: (a) Confinement induced splitting of the six-fold degenerate conduction band minima into two energy ladders corresponding to the Δ4- and Δ2-valleys in the triangular potential well approximation. (b) In the case of biaxial tensile strain, confinement and strain induced subband splitting are additive and thus increase the separation between the lowest energy levels of the two energy ladders.

Si Valence Band

The effect of strain on the valence bands of Si is far more complicated due to the valence band complexity. While the main effect of strain on the conduction band is lifting of degeneracy and shifting of subband edges, strain causes significant warping of the valence bands and mixing of HH and LH bands (64). Responsible for warping of the valence bands is again the shear component of the strain tensor whereas the hydrostatic component causes subband edge shifts. A few simple insights into the effects of strain on the valence bands can be obtained from symmetry considerations using the principle that the band structure with respect to a band extremum in the Brillouin zone has the same symmetry as this point (60). In Si the valence band maximum is at the Γ-point. The in-plane constant energy contours at the valence band maximum under biaxial strain therefore must have the symmetry of a square. A consequence of this symmetry is that the band curvatures along the k_x- and k_y-directions and therefore the effective masses

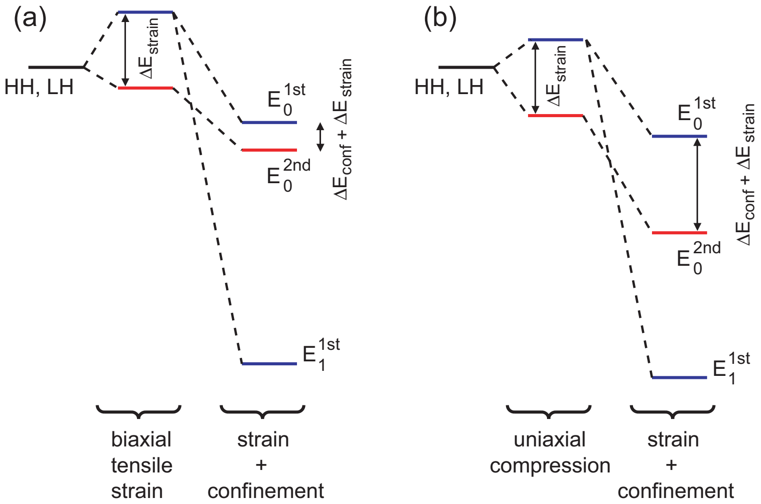

(a)
HH, LH
ΔE_{strain}
E_0^{1st}
E_0^{2nd}
$\Delta E_{conf} + \Delta E_{strain}$
E_1^{1st}
biaxial tensile strain
strain + confinement
(b)
HH, LH
ΔE_{strain}
E_0^{1st}
E_0^{2nd}
$\Delta E_{conf} + \Delta E_{strain}$
E_1^{1st}
uniaxial compression
strain + confinement

Figure 3.4: Schematics of the strain and confinement induced valley splitting and energy shifts of the valence band maximum due to (a) biaxial tensile strain and (b) uniaxial compressive strain. In the case of biaxial tensile strain confinement decreases the strain induced splitting of lowest subbands while it increases the separation in the case of uniaxial compressive strain.

in these directions are identical. Detailed bandstructure calculations show that in-plane constant energy contours at the top of the valence band under biaxial strain are ciruclar/square shaped (64). Under applied uniaxial [100]- and [110]-strain the in-plane symmetry of the Γ-point is reduced to that of a rectangle and a rhombus, respectively. The effective masses along the principles axes of the constant energy contours are not identical in this case. Calculation for the case of uniaxial compressive [100]-strain showed that the in-plane constant energy contours near the valence band maximum have an ellipsoidal shape with the short axis of the ellipsoid in the direction of strain. Holes in a p-type MOSFET with its channel aligned parallel to the strain direction would therefore benefit from a reduced conductivity mass.

Strain and Confinement

The carriers in a MOSFET are confined in potential well created by the vertical electric gate field E_{vert} at the gate oxide/silicon interface. Due to the anisotropy of the carrier masses in silicon confinement causes a splitting of the degeneracy of the conduction band minima as well as of the degenerate HH and LH band maxima and shifts the valley energies. This is illustrated in Fig. 3.3(a) for the conduction band valleys of Si. Confinement splits the six-fold generate conduction band minima into two sets of valleys: i) the in-plane Δ4-valleys with a confinement mass of $m_z = m_t$ and ii) the out-of-plane Δ2-valleys with a confinement mass of $m_z = m_l$ (65). For an effective vertical electric field of 1 MeV/cm and using the triangular potential well approximation the splitting between the lowest Δ4- and Δ2-valleys is $\approx$ 120 meV. Confinement induced energy shifts can be additive or subtractive to the strain induced valley energy shifts depending on the mass of the valleys in confinement direction (66).

Biaxial tensile strain lowers the energy of the Δ2-valleys with longitudinal electron mass m_l in confinement direction and increases the energy of the Δ4-valleys with the transverse electron mass in m_t in confinement direction. Due to the smaller mass in confinement direction the energy of the Δ4-valleys is stronger increased by confinement than the energy values of the Δ2-valleys. The separation in energy between the lowest subbands due to strain is therefore increased by confinement (Fig. 3.3(b)).

On the other hand the energy shifts caused by strain and confinement of the degenerate valence band maximum by biaxial tensile strain are subtractive (66). Biaxial tensile strain increases the energy of the LH-band and lowers the energy of the HH-band. For a stress of 1 GPa the splitting is 56 meV. Since the effective mass of the LH-band in confinement direction is smaller then that of the HH-band the energy splitting of the two lowest subbands is reduced by confinement. For a vertical electric field of $E_{\text{vert}} = 1$ MeV/cm the energy difference between the two lowest subbands is reduced to 15 meV (Fig. 3.4(a)). The advantage that the majority of carriers is in a valley with a low effective hole mass in transport direction is therefore lost at high vertical electric fields. Under uniaxial compressive strain, on the other hand, the valence bands warp strongly such that strain and confinement energy shifts are additive as shown schematically in Fig. 3.4(b).

3.2 Thin Virtual Substrat Technology for the Fabrication of SSOI

In this section the formation of strained Si during the relaxation of thin SiGe layers is presented. The strain-transfer mechanism is discussed and Si layers and SiGe/Si heterostructures grown on thin strain relaxed SiGe virutal substrates are analyzed in terms of strain, morphology and dislocation density. Epitaxial SiGe layers were deposited on (001) - Si wafers in a horizontal cold wall reactor by reduced pressure chemical vapor deposition (RPCVD). Optimized deposition conditions for epitaxial growth on 200 mm blanket wafer surfaces permit wafer scale control of the Ge content within 1%, with excellent layer thickness uniformity ($\sigma \approx 2\%$). Low temperature epitaxial growth enables deposition of strained SiGe layers with thicknesses far above the critical thickness. The epitaxial layers are defect free, with C and O contamination levels below the detection limits of secondary ion mass spectroscopy (SIMS). Finally, it is demonstrated how the strain-transfer mechanism can be employed to fabricate uniaxially tensile strained Si by applying it to a patterened Si/SiGe heterostructure.

3.2.1 Introduction

Tensile strain in silicon can be realized by growing a pseudomorphic silicon layer on a substrate with a larger lattice constant. The most frequently used method to manufacture such virtual substrates has been described by Fitzgerald et al. (67) and consists in growing a strain-relaxed SiGe epitaxial layer on a Si wafer. A state-of-the-art epitaxy process includes first a graded SiGe layer with an adequate Ge profile, followed by a strain-relaxed SiGe layer with a constant Ge concentration. The grading of the Ge profile in the buffer layer and the growth and annealing temperatures are critical parameters, controlling the relaxation process by generation and confinement of threading dislocations (TDs). Under appropriate growth conditions the degree of relaxation can exceed $R = 90\%$. Depending on the epitaxy conditions, dislocation densities can be as high as $10^9\,\mathrm{cm}^{-2}$ or as low as $10^4\,\mathrm{cm}^{-2}$ (68). The growth of a thin silicon layer on a strain-relaxed SiGe layer with a Ge concentration of 20at.% substrate leads to 1 GPa biaxial tensile strain in the silicon which improves electron mobility by nearly 100%. The typical thickness for strained silicon grown on $\mathrm{Si}_{0.8}\mathrm{Ge}_{0.2}$ relaxed layer is approximately 20 nm. However, this complex process produces virtual substrates several micrometers thick. Devices fabricated on such substrates show self-heating due to the poor thermal conductivity of SiGe (69). In addition, their growth is time consuming and costly. Various methods to realize thin relaxed SiGe buffers are presently under investigation (70; 71; 72). In previous works it was shown that H^+ - or He^+ - ion implantations and subsequent annealing of pseudomorphic $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layers on Si(100) can be successfully used to relax the SiGe layers (70; 71). The microstructures formed in the implanted bulk Si differs after H^+ - or He^+ - ion implantation and depends on the implantation dose. Low implantation doses produce platelet-like structures used in the relaxation process while high doses create microcracks which are successfully used for wafer splitting (73). For strain relaxation He^+ - ion implantation is regarded as more appropriate in terms of relaxation efficiency and final dislocation density, particularly for SiGe layers with Ge contents below 30at.%. Threading dislocations and especially dislocation pile-ups may seriously degrade the electrical performance of strained silicon devices. Therefore, minimizing their density is one of the challenges of strained Si technology.

3.2.2 The Strain Transfer-Mechanism

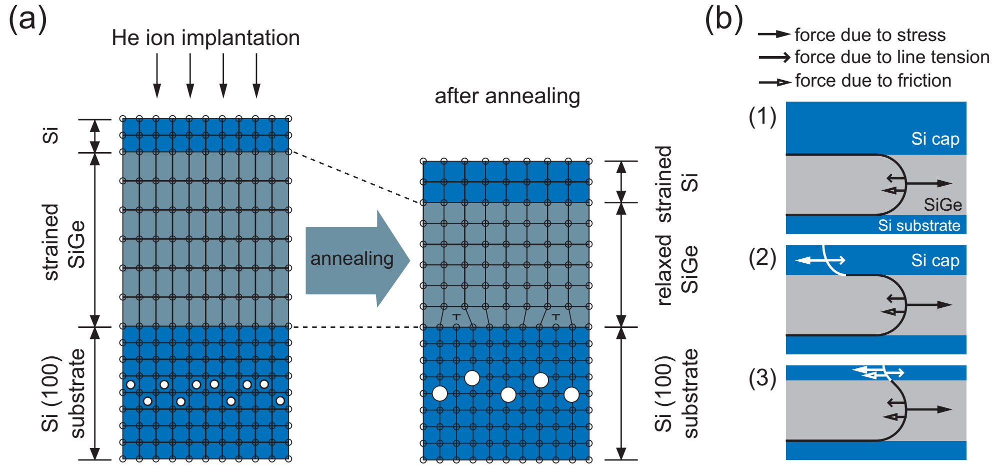

(a)
He ion implantation
Si
strained SiGe
Si (100) substrate
annealing
after annealing
strained Si
relaxed SiGe
Si (100) substrate
(b)
force due to stress
force due to line tension
force due to friction
(1)
Si cap
SiGe
Si substrate
(2)
Si cap
(3)

Figure 3.5: (a) Schematics of the strained silicon on SiGe fabrication process by He ion implantation and annealing using strain transfer during strain relaxation of the SiGe layer. (b) Sketch of the motion of TDs in a SiGe buffer and a Si top layer. Thick full, thin full and open arrows indicate forces due to stress, line tension and friction, respectively (71).

The strain transfer model is discussed first. The model is an extension of the SiGe strain relaxation model (71), describing the experimental results in terms of the formation of dislocation loops at the Si-substrate/SiGe interface, the extension of loop segments towards the SiGe/Si interface and the Si surface and the spreading of the TDs through both layers. He filled cavities, formed by He^+ - ion implantation and annealing underneath the SiGe/Si substrate interface, are responsible for the formation of dislocation loops which glide towards the interface (Fig. 3.5) (71). Under compressive plane stress in the SiGe layer, one segment of such a loop is held at the SiGe/Si-substrate interface, where it forms a misfit dislocation (MD) segment, while the other one is driven through the SiGe layer towards the SiGe/Si top interface. Once a dislocation loop has reached the surface of the Si top layer, the two TD arms connecting the MD segments in the SiGe/Si-substrate interface with the surface will spread to both sides depending on the specific conditions as the relaxation degree R_{SiGe} and silicon cap thickness t_{Si}. Three types of forces influence the motion of a TD: forces due to stress, line tension and friction (Fig. 3.5 (b)). In the SiGe layer, TD motion is driven by the compressive stress in the layer counteracted by line tension and frictional forces. In the top Si layer, the curvature of the TD, being tracked by its segment in the SiGe layer, changes its sign such that the driving force for its motion becomes line tension, counteracted by forces due to friction and the generated tensile stress. For small t_{Si} the segment of the TD within the top Si layer is able to follow that in the SiGe layer during the whole deformation process because of the large line tension force associated with its curvature, allowing complete plastic strain transfer or 100% "strain transfer efficiency". In an intermediate range of t_{Si} values, the segment of a TD within the Si top layer follows the SiGe TD segment only at the beginning of the deformation process but remains behind when the line tension force (then maximum) is compensated by the force due to the build up tensile stress. This transition occurs at a critical strain $\epsilon_{\mathrm{Si,crit}}$ determined by the critical thickness relation according to Matthews and Blakeslee theory (74; 75), independent of the further relaxation of the SiGe layer. When the tensile stress force on TD segments in the Si top layer becomes equal to the line tension force before the relaxation process in the SiGe layer has ended, the still advancing TD segments in the SiGe layer produce MD segments at both interfaces bounding the SiGe layer.

For this process a critical thickness for full strain transfer of about 8nm for a 75% relaxed $\mathrm{Si}_{0.74}\mathrm{Ge}_{0.26}$ buffer layer was found (72). Such a sSi layer transferred to an oxidized wafer is thick enough for the realization of ultrathin SOI−MOSFETs. The process is fully compatible with CMOS technology (76). Thicker sSi layers can be obtained by using the 8 nm sSi layer as seed for further epitaxial overgrowth as presented in the following (Fig. 3.6).

Efficient strain transfer to a Si cap layer by relaxation of SiGe in a Si/SiGe heterostructure employing the process described above was confirmed by strain measurements. Raman spectroscopy using a laser wavelength of 415 nm was used to analyze the strain present in the Si and SiGe epilayers (77). Since the extinction depth is quite small, the use of such a short excitation wavelength enables measurements of the Raman signal from thin epitaxial layers without interference effects from the underlying silicon substrates. The compositional dependence of the optical phonon frequencies in $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layers has been subject of several studies (78; 73; 79). In this work the expressions given in (79) were used to calculate the optical phonon frequencies for relaxed $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layers. The degree of relaxation of the SiGe layer was calculated as the ratio of the frequency shift after the relaxation process, ω_{r}, regarding the full strain state, $\omega_{0\%}$, and the total expected frequency shift for fully relaxed layer, $\omega_{100\%}$:

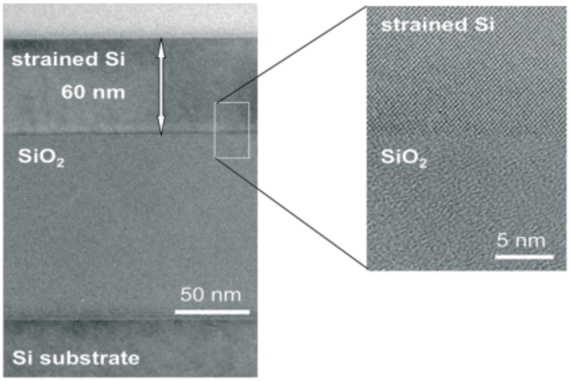


Figure 3.6: TEM image of a 60 nm strained silicon layer directly on oxide fabricated by the strain transfer process and subsequent epitaxial overgrowth of the strained silicon layer.

$$R\,(\%) = 100 \times \frac{\omega_{0\%} - \omega_{\mathrm{r}}}{\omega_{0\%} - \omega_{100\%}} \tag{3.12}$$

.

Elastic strain in the Si layer and simultaneous strain relaxation of the SiGe layer are shown in Fig. 3.7 for an as-grown and 68% relaxed $\mathrm{Si}_{0.71}\mathrm{Ge}_{0.29}$ layer. The heterostructure consists of 145 nm $\mathrm{Si}_{0.71}\mathrm{Ge}_{0.29}$ and a 5 nm Si top layer. The shift of the SiGe peaks indicates the strain relaxation of the SiGe layer. The presence of the unstrained Si peak at 520 cm^{-1} in the Raman analysis revealed the cubic structure of the Si film in the as-grown state. The Raman peak shift of the Si−Si mode in the Si layer, as a consequence of the SiGe layer relaxation, is a confirmation of the elastic strain accumulated in the film and the shift direction indicates the tensile type of strain. The amount of strain incorporated in the Si film was calculated from the wavenumber shift using the expressions given in (80).

3.2.3 Strained Silicon Overgrowth

Current industrial state of the art SOI devices are partially depleted and therefore require SOI layer with thicknesses $\geq$ 60 nm. To make use of the strained silicon layers produced by strain-transfer in these processes, the thickness of the SSOI layer has to be increased by overgrowth. Strained silicon layers with thicknesses up to 8 nm on 150 nm $\mathrm{Si}_{0.74}\mathrm{Ge}_{0.26}$ were produced by the strain-transfer mechanism as described in subsection 3.2. Due to the Si terminated surface standard CMOS cleaning procedures can be applied before overgrowth. The as-grown heterostructures, as stated above, were

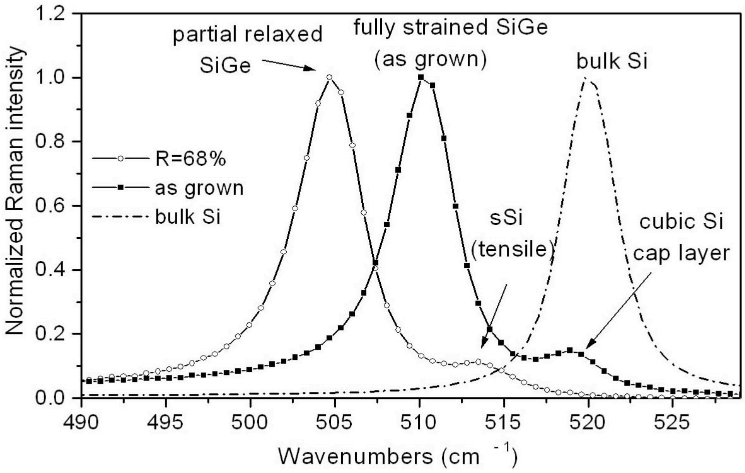
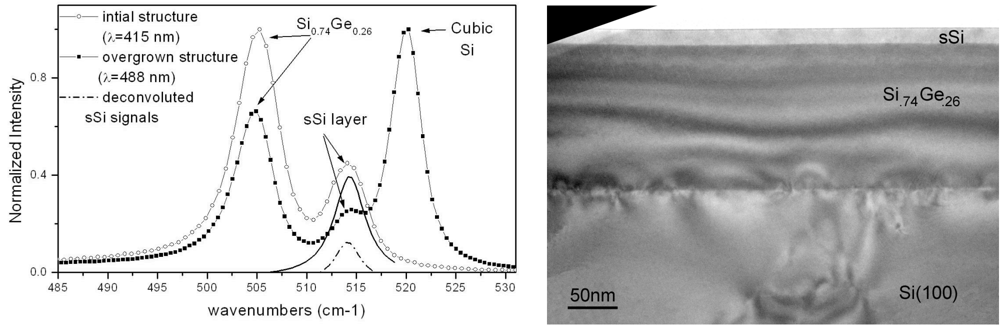


Figure 3.7: Raman spectra of Si-Si modes from SiGe and sSi epitaxial films of a Si/$Si_{0.71}Ge_{0.29}$/Si heterostructure after growth and strain relaxation. The bulk Si spectrum is shown for reference (77).

implanted with $7 \times 10^{15}$$He^{+}$ cm^{-2} at an energy of 40 keV. As a protection for the top Si layer during implantation a 100 nm plasma enhanced chemical vapor deposition (PECVD) SiO_2 film was used. In the following, two differently processed wafers, distinguished by the annealing process initiating strain transfer mechanism, the will be compared.

The first wafer was annealed in a RTP system at 850 °C for 10 min in N_2 atomsphere. After the SiGe relaxation the strain in the Si cap layer and the relaxation of the SiGe buffer were measured by Raman spectroscopy to be $\epsilon_{\text{Si}} = 0.8\%$ and $R_{\text{SiGe}} = 70\%$, respectively, corresponding to 100% strain transfer between the SiGe buffer layer and the Si cap. After etching the SiO_2 layer and appropriate pre-epitaxial wet cleaning the wafer was re-loaded into the CVD chamber. Following a moderate H_2 pre-bake at 715 °C silicon was deposited at a temperature of 715 °C. In order to achieve a better separation of the Raman signals two different wavelengths were used to measure the strain in the initial and the overgrown structure.

The Raman measurements of the resulting structure confirm that the tensile strain in the Si cap layer is fully maintained as can be seen by comparing the Raman signal of the sSi layer in the initial and overgrown structure (Fig. 3.8a). The cross-section TEM micrograph of Fig. 3.8b shows the obtained heterostructure with a sSi thickness of 18.5 nm. No interface can be seen between the sSi seed layer and the epitaxial re-grown layer. The AFM rms surface roughness of the final structure is with 0.8 nm nearly identical to



(a) (b)

Figure 3.8: (a) Raman spectra of Si-Si modes from SiGe and sSi epitaxial films from a sSi/$Si_{0.77}Ge_{0.23}$/Si (100) heterostructure before and after sSi regrowth. (b) Bright field electron micrograph showing the 18.5 nm sSi layer on top of the partially relaxed $Si_{0.74}Ge_{0.26}$ layer. The sSi layer is free of dislocations. The interface between the SiGe and the Si substrate contains misfit dislocations (77).

the value before the epitaxial step of 0.5 nm (Fig. 3.9).

The second wafer was loaded into the CVD tool after ion implantation and SiO_2 wet etching. The subsequent anneal was performed in the CVD reactor at 850 °C 10 min in H_2. Subsequently 10 nm of Si were grown epitaxially at 715 °C. Raman spectra of this sample show a high degree of relaxation of about 90% of the SiGe buffer. Similar observations of high relaxation degrees have been made after epi-chamber anneals of SiGe layers. However, the uncapped SiGe layers featured a large rms roughness of 16 nm, while the epi−chamber annealed 8 nm Si capped SiGe layer showed a rms roughness of 1.3 nm. The directly measured strain in the sSi cap layer, $\epsilon_{Si} = 0.9\%$, is lower than the tensile strain expected from a $R_{\mathrm{SiGe}} = 90\%$ relaxed SiGe layer. This indicates that the initial 8.5 nm Si cap is larger than the critical thickness for a full strain transfer.

3.2.4 Surface Roughness and Defect Analysis

With decreasing body thickness in fully depleted MOSFETs carrier scattering at the body/oxide interfaces becomes very important. In the limit that the SOI film thickness is as thin as the inversion layer of a bulk MOSFET, the sub-band energy is determined by the SOI physical thickness. Therefore, SOI thickness fluctuations due to roughness of the surface or interface cause significant spatial fluctuation of the potential for inversion layer carriers and

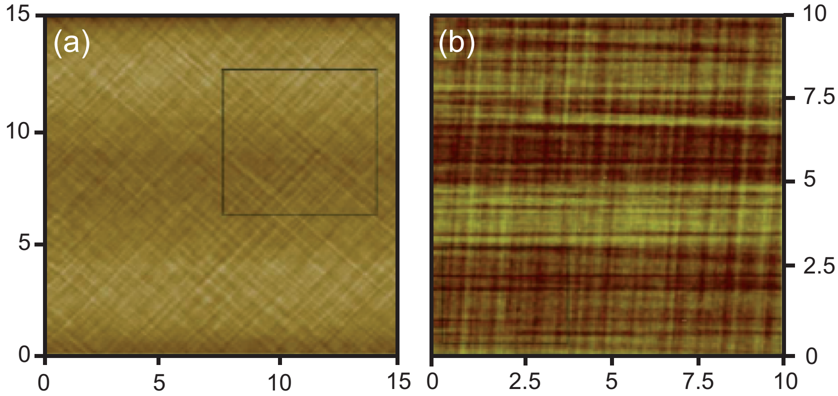


Figure 3.9: AFM images of 8 nm sSi on top of the partially relaxed $Si_{0.74}Ge_{0.26}$ layer, (a) before overgrowth and (b) after 10 nm sSi overgrowth. Before overgrowth the sSi layer had a rms roughness of 0.5 nm and after overgrowth of 0.8 nm (77).

degrade the mobility. Using atomic force microscopy a rms surface roughness of $0.3 - 0.5$ nm of the sSi layer was measured on an area of $15 \times 15\,\mu m^2$. By plan-view transmission electron microscopy (PVTEM) the TD density of thin relaxed SiGe buffers with Ge concentrations up to 26at.% and degrees of strain relaxation of $65 - 75\%$ was determined to be $\approx 3 \times 10^6\,cm^{-2}$. For thicker strained Si layers (> 15 nm) and low defect density (below $10^6\,cm^{-2}$) chemical defect etching and optical microscopy are preferred to reveal the etch pit density (EPD) under differential interference contrast. Dilute Secco etch ($K_3Cr_2O_7 : HF : H_2O$) has been proven to be very effective in defect delineation, due to its high defect selectivity in Si layers (81). The sSi was etched to a thickness of a few nanometres over the underlying SiGe layer. Fig. 3.10 shows an example of defect delineation by defect etch analysis. The different types of defects are indicated in the Figure (SF, TD, pile-ups).

3.2.5 Process Optimization for Threading Dislocation Reduction

An important issue for the use of strained silicon layers grown on relaxed SiGe buffer layers is the reduction of the TD density and the pile-up density. In particular, pile-up dislocations have a detrimental effect on the electrical performance of strained silicon MOSFETs especially if they are connecting the source/drain regions. During its movement a TD can enter into the interaction range of another TD of opposite Burgers vector and the TDs can annihilate each other. A TD remains blocked in the SiGe layer if the force

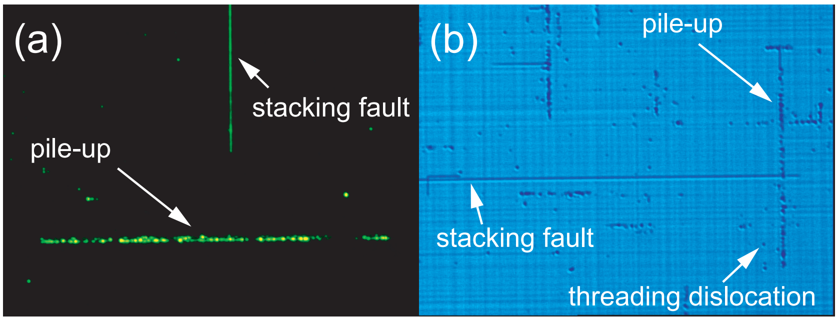


Figure 3.10: Dark field image (a) and Normarsky interference contrast image (b) of a nm strained Si layer. In both images planar and point defects are clearly visible.

due to stress equals the line tension. A high relaxation degree implies a large number of TDs and a relaxed layer is of high quality if only a low dislocation density remains in the layer after relaxation. The process optimization by adjusting the He implantation process parameters was previouly reported (82) and is not presented here. For the thin relaxed SiGe layer used in this work the typical threading dislocation density is $3 \times 10^6\,\mathrm{cm}^{-2}$ and the typical pile-up density $25\,\mathrm{cm}^{-1}$. During epitaxial overgrowth of a $\mathrm{Si_yGe_{1-y}}$ layer on a $\mathrm{Si_xGe_{1-x}}$ substrate any TD from the substrate will penetrate the new epitaxial layer, thereby enlarging its length and curvature, finally ending up at the layer surface. For $y < x$ the sign of the TD curvature will change, too. The result is a larger interaction volume signifying a higher probability for the TD to find a partner for annihilation.

In the following the epitaxial overgrowth of a strain adjusted SiGe layer is presented with emphasis on the reduction of the TD density. The investigated heterostructures consist of 6 nm Si/(180 nm) $\mathrm{Si_{0.77}Ge_{0.23}}$/Si(100). The degree of relaxation of the SiGe buffer is $R_{\mathrm{SiGe-buf}} = 70\%$ which corresponds to a induced strain in the cap layer of $\epsilon_{Si} = 0.66\%$. The Ge content ($c_{\mathrm{Ge-ov}}$) of the second SiGe layer is adjusted according to

$$c_{\mathrm{Ge-ov}} = R_{\mathrm{SiGe-buf}} \cdot c_{\mathrm{Ge-buf}} \tag{3.13}$$

where $R_{\mathrm{SiGe-buf}}$ denotes the degree of relaxation of the SiGe buffer and $c_{\mathrm{Ge-buf}}$ the Ge content in the buffer. As a consequence the overgrown SiGe layer is fully relaxed. After a 715 °C $\mathrm{H_2}$ pre-epibake the temperature was lowered to 690 °C for the growth of the SiGe layer and then raised to 705 °C for the deposition of 20 nm tensely sSi.

Fig. 3.11 shows a bright field XTEM image of this sample. No misfit dislocations can be observed at the sSi/SiGe interfaces indicating a perfect

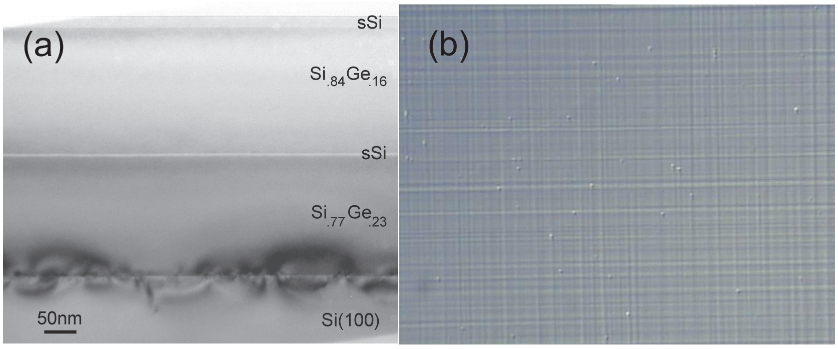


Figure 3.11: (a) Bright field electron micrograph showing a 20 nm sSi/200 nm fully relaxed $Si_{0.84}Ge_{0.16}$ layer grown on a 6.3 nm sSi/partially relaxed $Si_{0.77}Ge_{0.23}$ template. No defects are seen at the sSi/SiGe interfaces indicating pseudomorphic growth. (b) Optical micrograph using differential interference contrast showing etch pits and cross-hatch in the upper sSi layer of a sSi/fully relaxed $Si_{0.84}Ge_{0.16}$/sSi/partially relaxed $Si_{0.77}Ge_{0.23}$ heterostructure. The image area is $80 \times 60\,\mu m^2$. The threading dislocation density is $1 \times 10^6\,cm^{-2}$ (77).

pseudomorphic heterostructure. This conclusion is supported by the strain measurements showing a degree of relaxation of 100% for the epitaxial re-grown SiGe layer and a tensile strain in the sSi cap layer of 0.66% as in the sSi seed layer. The surface roughness is only slightly increased from 0.5 nm to 0.8 nm, as measured by AFM.

Chemical defect etching and optical differential interference contrast microscope analysis of the surface of the 20 nm sSi/200 nm $Si_{0.84}Ge_{0.16}$ layer stack (Fig. 3.11(b)) show a defect density of $1 \times 10^6\,cm^{-2}$ (77). Taking into account that the TDs density of the buffer is $3 \times 10^6\,cm^{-2}$, the epitaxial re-growth of the relaxed SiGe layer suppresses one out of three TDs to propagate through the overgrown structure.

3.3 Asymmetric Strain Relaxation in Si/SiGe Heterostructures

In this section a method for the fabrication of compressively uniaxially strained silicon is presented. The strained Si is obtained by strain transfer during asymmetrical relaxation of a patterned, compressively strained SiGe layer. For the relaxation of the SiGe layer the He^+−ion implantation and annealing, as presented above, are employed. For 0.8 μm wide lines the strain relaxation in the SiGe reaches 95% perpendicular to the line but only 34% along the line. This is explained in the strain transfer model by the different path length of TDs along and perpendicular to the lines leading to an asymmetric MD network.

3.3.1 Theoretical Considerations

It has recently been shown that in thin Si layers on SiGe / Si heterostructures, high biaxial tensile stresses can be generated by strain transfer from the relaxing SiGe layer to the Si layer (72). The strain induced in the Si layer upon relaxation of the SiGe layer was described by

$$\epsilon_{\mathrm{Si}} = \eta R \cdot f_{\mathrm{Ge,Si}} \tag{3.14}$$

.

Here $f_{\mathrm{Ge,Si}} = 4.2\%$ is the lattice mismatch between Ge and Si, R is the degree of relaxation of the $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ epilayer, and η is the "strain transfer efficiency" which was shown to reach 100% for Si layer thicknesses below about 8nm. A key step in this strain transfer process is strain relaxation in the SiGe epilayers. It has been shown that this relaxation can be efficiently achieved by He^+ ion implantation and subsequent thermal annealing (72; 71). In a model of this process (71), it has been assumed that the narrow defect band formed upon ion implantation underneath the SiGe / Si-substrate interface provides a high density of dislocation loops during annealing, part of which glide to the interface and evolve from there into dislocation arms consisting of segments of misfit dislocations (MDs) in the interface and threading dislocations (TDs) through the strained SiGe layer. The stress driven propagation of the TD segments through the SiGe layer along the [110] and [−110] directions is associated with an extension of the corresponding MD segments involving an increasing strain relaxation. Interaction and mutual annihilation of TD segments result in a reduction of the TD density to an acceptably low level (77). In the final state, a long MD consists of the trails of many TDs.

Accordingly, the final MD density and the corresponding level of strain relaxation are determined by the density of the loops contributing as dislocation sources and the average path length of the TDs before they annihilate or stop. Since the probabilities for both the generation of loops with different but crystallographically equivalent Burgers vectors and the average path lengths of the resulting dislocations extending in the two in-plane $\langle 110 \rangle$ directions are equal, the relaxation of the SiGe layer is symmetric isotropic, i.e., the SiGe crystal structure remains tetragonal during relaxation. The model suggests that this symmetry can be broken by patterning the SiGe layer into micrometer narrow [110] lines for which the average path length

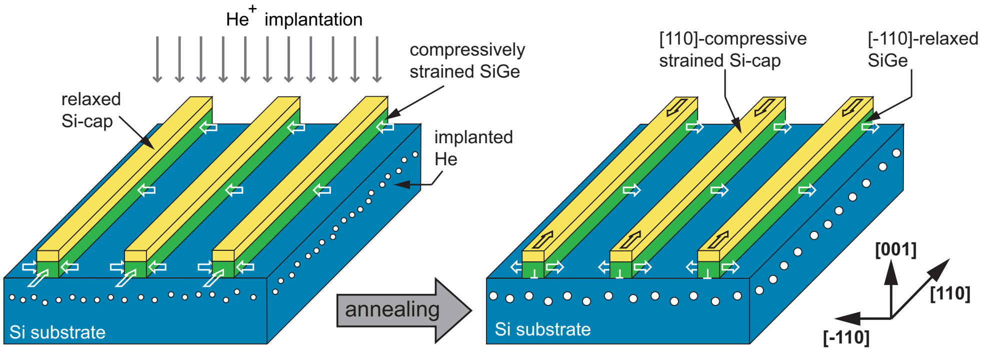


Figure 3.12: Schematics of the sample illustrating the process and the strains.

of TDs moving in the [−110] direction would be shortened by the two stripe boundaries, resulting in a reduction of the MD density in this direction and a corresponding reduction of the degree of relaxation in the [110] direction. This idea is illustrated in Fig. 3.12 and Fig. 3.13.

3.3.2 Sample Preparation

Epitaxial Si / $Si_{0.77}Ge_{0.23}$ (6 nm/180 nm) heterostructures were grown on Si (001) by chemical vapor deposition in an ASM Epsilon® production tool by Roger Loo at IMEC. The samples were implanted with $7 \times 10^{15}\,cm^{-2}$ He ions at an energy of 45 keV. Prior to patterning the samples were pre-annealed at a temperature of 450 °C for 1 min. This annealing assures the formation of He-platelets and dislocation loops required for relaxation without initiating relaxation of the SiGe layer (83). Lines along the [110] crystal direction with widths varying between 0.8 and 10 μm were patterned using standard optical lithography. Subsequently, the Si-cap layer and the SiGe were RIE etched (Fig. 3.12). Finally, the structures were annealed at a temperature of 850 °C for 10 min in N_2 atmosphere to relax the strain of the SiGe.

3.3.3 Strain Measurement by Ion Channeling

He ion channeling was employed to measure strains along and perpendicular to the lines. Other methods for the measurement of strains are not well suited for this type of structure. Raman spectroscopy measures only the average of the strains along and perpendicular to the lines and x-ray diffraction has been shown to underestimate the strain contributions of low MD densities, underestimating by this the asymmetry (84). Ion channeling angular yield scans of the Ge backscattering signal have been performed with

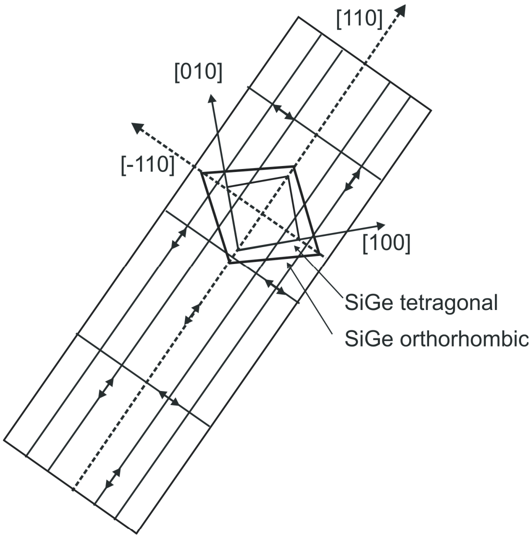


Figure 3.13: Illustration of a misfit network after asymmetric strain relaxation in a SiGe stripe on (100)Si. The limitation of the paths of TDs in the $[-110]$ direction by the stripe boundary results in a reduced MD density in this compared to the [110] direction and a correspondingly reduced degree of relaxation in the [110] direction. By this, the square basis of an orthorhombic unit cell of the SiGe crystal is distorted to a rhombic basis of an othorhombic unit cell in the $[110]\,,[-110]\,,[001]$ coordinate system.

a high-precision goniometer using 1.4 MeV He^+ ions at a scattering angle of $170\,^\circ$. They provide absolute angles between various crystal directions and by this the lattice strains (70). For cubic lattices as unstrained Si or fully relaxed SiGe, the angle between [001] and [111], for instance, has a value of $54.736\,^\circ$. Compressive tetragonal strains in SiGe/Si lead to smaller angles ($54.736\,^\circ - \Delta\theta$) with $\Delta\theta < \Delta\theta_{\mathrm{ps}}$ where $\Delta\theta_{\mathrm{ps}}$ denotes the maximum angular shift realized by the unrelaxed symmetrically stressed, pseudomorphic SiGe layer. For symmetric isotropic biaxial relaxation, the degree of relaxation may be defined as $R = 1-(\Delta\theta/\Delta\theta_{\mathrm{ps}})$. We may directly extend this definition to asymmetrically relaxing [110] lines if we assume the strain tensor to have the (110) and (-110) mirror symmetries of the lines as expected for two sets of MDs along [110] and $[1-10]$, respectively. Then two different relaxation degrees, $R_{\|}$ and $R_{\perp}$, may be defined by the two different changes, $\Delta\theta_{1,2}$ of the angles shifts between [001] and [111], and [001] and $[-111]$, respectively: $R_{\|,\perp} = 1-(\Delta\theta_{1,2}/\Delta\theta_{\mathrm{ps}})$. Accordingly, for asymmetrically relaxing [110] lines, we performed angular scans along the (-110) plane through the [001] and the inclined [111] directions along the patterned stripe, see (Fig. 3.13) and along the (110) plane through the [001] and $[-111]$ directions across the patterned stripe.

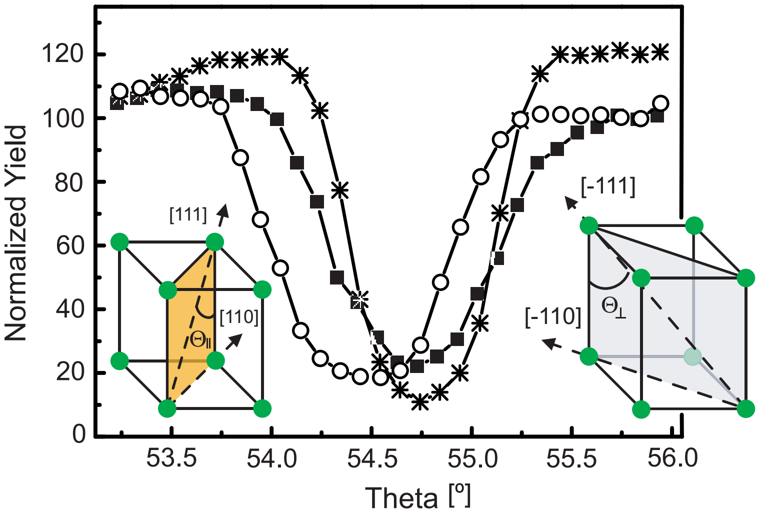


Figure 3.14: Channeling angular yield scans of the Ge backscattering signal from 0.8 μm lines measured across (empty circles) and along the line (full squares), respectively. The corresponding scan of a cubic Si crystal with its midpoint at 54.74 ° is shown as reference (star symbols). The insets show the crystallographic directions of the two nonequivalent diagonals with the angles $\theta_{\|}$ and $\theta_{\perp}$ along the stripe and perpendicular to the lines, respectively.

Figure 3.14 shows channeling angular yield scans of the Ge backscattering signal from a sample with a stripe width of 0.8 μm, both across and along the stripe. A corresponding scan for a cubic Si crystal is shown for reference. The midpoint of each scan represents the absolute angle between the [001] sample normal and the [−111] or the [111] directions, respectively (nonequivalent diagonals). The shift of the midpoint position provides direct evidence for the change of the tetragonal lattice to an orthorhombic lattice structure in the [110], [−110], [001] coordinate system. The relaxation degrees of the SiGe lines along, $R_{\|}$, and perpendicular, $R_{\perp}$, to the lines are summarized in Table I. Obviously, the strain relaxation depends strongly on the width of the lines. The very narrow lines of 0.8 μm in width show nearly full relaxation $\mathrm{R}_{\perp} = 95\%$ perpendicular to the stripe direction but only small relaxation of $\mathrm{R}_{\|} = 34\%$ along the lines. The ratio of the two relaxation degrees, $R_{\perp}/R_{\|}$, has a value of approximately 2.8.

For comparison data for symmetrically relaxed blanket SiGe layers obtained previously (72) has been included in table 3.1. According to the physical picture described above, this asymmetry in strain relaxation is due to the different path lengths of the TDs propagating along the two in-plane [110] directions. If the TD path in the [−110] direction is limited by the stripe

SiGe lines			Virtual Si top layers					
Linewidth (μm)	Relaxation degree (%)		Strain /stress (%)/(GPa)		Rel. res. change (%)			
					n-Si		p-Si	
	$R_\parallel$	$R_\perp$	$\epsilon_\parallel/\sigma_\parallel$	$\epsilon_\perp/\sigma_\perp$	$\Delta_\parallel$	$\Delta_\perp$	$\Delta_\parallel$	$\Delta_\perp$
$\rightarrow \infty$	70	70	0.68/1.22	0.68/1.22	-59	-59	6.7	6.7
3.2	41	75	0.40/0.75	0.72/1.27	-46	-53	-31	43
2.8	35	77	0.34/0.65	0.74/1.30	-43	-52	-39	50
1.4	45	95	0.43/0.83	0.92/1.60	-54	-63	-46	60
0.8	34	95	0.33/0.65	0.92/1.60	-48	-61	-59	71

Table 3.1: Relaxation degress, $R_{\parallel,\perp}$, along and perpendicular to the SiGe lines of different widths, together with strains $\epsilon_{\parallel,\perp}$ and stresses $\sigma_{\parallel,\perp}$ as well as resistivity changes $\Delta_{\parallel,\perp}$, expected to occur in thin Si cap on the SiGe lines. $\Delta_{\parallel,\perp}$ values were calculated on the basis of piezoelectric modell on Si (85).

boundary, the density of MDs in this direction is reduced as illustrated by the thin line pattern in Fig. 3.13. This observation is confirmed by plan view transmission electron microscopy PV-TEM in Fig. 3.15 where the MD density in the direction parallel is a factor of 2.4 lager than perpendicular to the lines, reflecting the ratio of the corresponding relaxation degress.

Figure 3.15 shows a PV-TEM micrograph of a 4 μm wide stripe, where the misfit dislocation density perpendicular to the direction of the stripe is about a factor of 2.4 larger than parallel to the stripe which reflects the ratio of the corresponding relaxation degrees. The asymmetry decreases with increasing stripe width and vanishes when the stripe width becomes larger than the mean TD path length in the blanket layer. The measurements indicate that this path length is of the order of a few micrometers.

3.3.4 Strain, Stress and Resistivity

The asymmetric strain and stress impacts the electronic properties of the Si and leads to an anisotropic conductivity. So far, no measurements of carrier mobilities in such asymmetrically stressed thin cap layers are available. Therefore piezoelectric coefficients measured on Si (85) for tensile stresses up to about 10 MPa are extrapolated to the two orders of magnitude higher stresses expected from measurements made in this experiment and are used to estimate the relative resistivity change expected in the lines. Assuming for thin Si cap lines (< 8 nm) perfect strain transfer efficiency, the asymmetric strains along and perpendicular to the lines, $\epsilon_{\parallel,\perp}$, are calculated by using

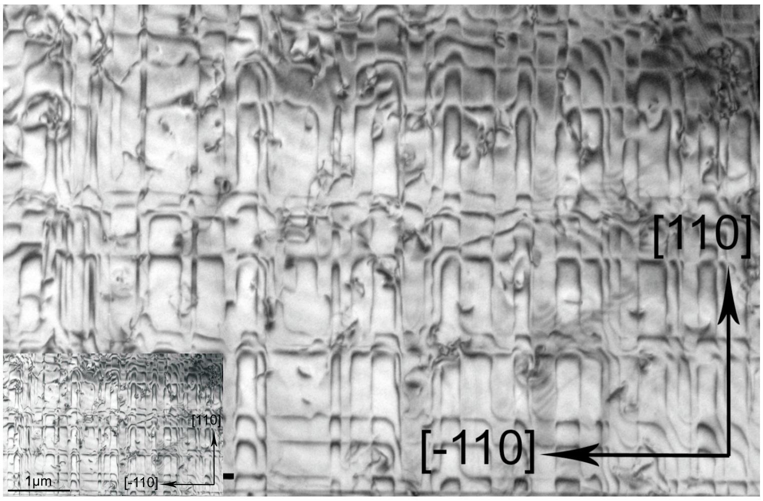


Figure 3.15: Plan view TEM micrograph of an asymmetric MD array in a 4μm wide stripe, where the misfit dislocation density perpendicular to the direction of the lines is about a factor of 2.4 larger than that parallel to the lines.

$\eta = 1$ and $R = R_{\|,\perp}$, in (Eq. 3.14). For the lines, the asymmetric biaxial stresses $\sigma_{\|,\perp}$ are related to the asymmetrical strains by

$$\sigma_{\|,\perp} = \left[\frac{(C_{11} + 2C_{12})\,/C_{11} - C_{12})}{C_{11}}\right] \frac{\left(\epsilon_{\|} - \epsilon_{\perp}\right)}{2} \pm C_{44}\left(\epsilon_{\|} - \epsilon_{\perp}\right) \qquad (3.15)$$

where C_{11} and C_{12} denote elastic constants of Si. According to Table I, for the narrow lines, values as high as $\epsilon_{\perp} \approx 1\%$ corresponding to $\sigma_{\perp} \approx 1.6\,\text{GPa}$ are reached. The anisotropic relative resistivity changes in the [110] and [−110] directions, $\Delta_{\|,\perp}$, are given by:

$$\Delta_{\|,\perp} = (\Pi_{11} + \Pi_{12} \pm \Pi_{44})\,\frac{\sigma_{\|}}{2} + (\Pi_{11} + \Pi_{12} \mp \Pi_{44})\,\frac{\sigma_{\perp}}{2} \qquad (3.16)$$

where $\Pi_{\mathrm{i,j}}$ are the piezoresistivity coefficients. The high values of $\Delta_{\|,\perp}$, given in table 3.1 (even though beyond the limits of linear piezoelectricity) indicate significant changes in the carrier mobilities. The stress induced reduction of the relative resistivity change in n-Si is comparable for line and layer structures, whereas it is substantially larger in p-Si for narrow lines than for layers. For comparison, the values for Si layers with symmetrical biaxaial strain obtained previously (72) have been included in table 3.1. The resistivity changes according to piezoresistivity for n-and p-type Si are plotted in Fig. 3.16. A relaxation asymmetry of 1 represents biaxial tensile strain and an asymmetry of 0 corresponds to pure uniaxial tensile stress. While for

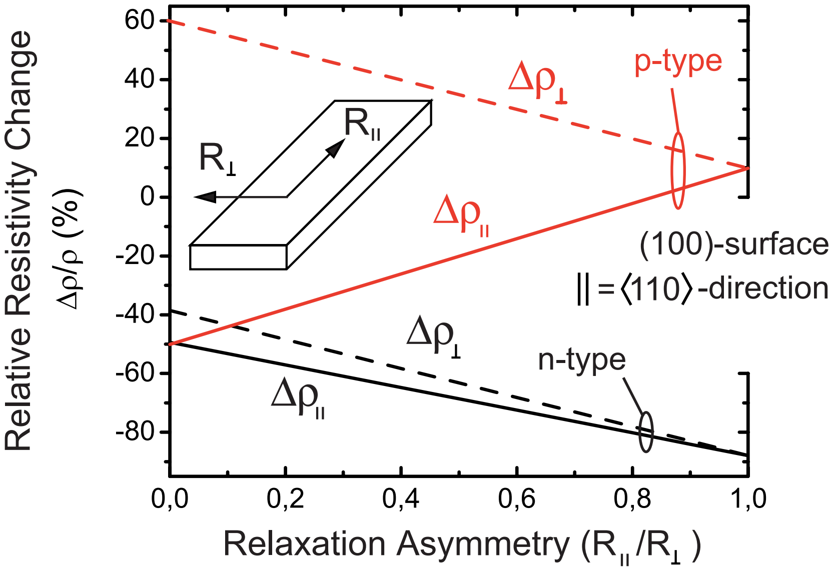


Figure 3.16: The relative change in resistivity of n- and p-type (100) Si according to piezoresistance theory is plotted as a function of the relaxation asymmetry of a rectangular structure. While biaxial tensile strain is only effective in reducing the resistivity of n-type Si, uniaxial tensile strain along ⟨110⟩ reduces the resistivity of n- and p-type Si at the same time (86).

current along ⟨110⟩ the relative change in resistivity for n-type Si is largest for biaxial strain, there is still a 50% relative resistivity change for uniaxial tensile strain along ⟨110⟩. Additionally there is an equal decrease in relative resistivity of p-type Si not present for biaxial strained Si.

3.4 Electrical Characterization

3.4.1 Fabrication of Hall-bar MOSFETs

Hall-bar MOSFETs were fabricated on (100) p-type doped SOI and SSOI ($N_A = 1 \times 10^{15}\,\mathrm{cm}^{-3}$) with an initial silicon thickness of 60 nm. The channel length of the devices is L = 670 μm and the width W = 140 μm as is the distance between the voltage contacts. The device fabrication process consists of the following steps:

1. *Mesa definition:*
   The mesa is defined by optical lithography and RIE etching. An Ar/SF$_6$-plasma is used to etch the silicon down to the BOX. (Fig. 3.17(a))

2. *Gate stack deposition:*

After mesa isolation and RCA cleaning, a 6nm gate oxide was grown using RTP dry oxidation at 800 °C for 25 min. Two hundred nanometer n-type poly-Si and 80 nm SiO_2 were then deposited by LPCVD. The n-poly silicon was activated by RTP annealing at 950 °C for 60 sec.

3. *Gate stack definition:*
   The 80 nm SiO_2 on top of the poly-Si layer was patterned by optical lithography, followed by RIE. The poly-Si was etched by ICP-RIE using a HBr plasma (Fig. 3.17(b)).

4. *Contact implantation:*
   Source/drain and voltage contacts were implanted after gate patterning: n-type devices with As at 5 keV to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ and p-type devices with B at 2 keV with a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$ (Fig. 3.17(b)).

5. *Passivation and dopant acitvation:*
   After implantation a 80 nm SiO_2 passivation layer is deposited by LPCVD to protect the devices from ambient influences. Subsequently the implanted dopants have been activated by RTP annealing at 1000 °C for 10 sec.

6. *Contact metallization:*
   Optical lithography and RIE were employed to define and open the S/D, gate and contact windows. A standard lift-off procedure was used for metallization of the contacts. Negative optical lithography was used to open windows on the contacts for metal deposition. The native oxide on top of the contacts was removed by HF (1%) etching directly before metal deposition. 200 nm Al were deposited by E-beam evaporation. Finally, the photoresist was removed with acetone and propanol (Fig. 3.17(d)).

3.4.2 Room Temperature Measurements

In this section the electrical characteristics of p- and n-type Hall-bar MOSFETs fabricated on (100) SOI and biaxial tensile strained (100) SSOI corresponding to a Ge-content of $x_{\mathrm{Ge}} = 20\%$ and to a stress of $\sigma = 1.2\,\mathrm{GPa}$, both aligned along the $< 110 >$ - direction, are discussed.

Fig. 3.18 shows the transfer characteristics on a linear and logarithmic scale of two p-type Hall-bar FETs on (a) 60 nm SOI and (b) 60 nm SSOI. Both devices have a good $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio of $\approx 10^7$ but somewhat larger subthreshold slopes of 93 nm/dec for SOI and 105 mV/dec for SSOI since the

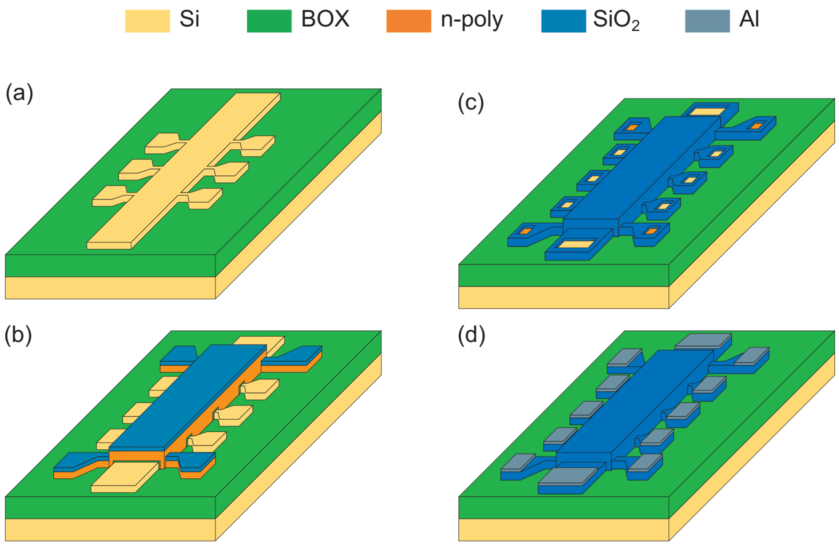


Figure 3.17: Process for the fabrication of Hall-bar MOSFETs. The devices have a gate length of $L = 670\,\mu\text{m}$, width of $W = 140\,\mu\text{m}$ and a distance between the voltage-probes of $L_\text{H} = 140\,\mu\text{m}$.

devices were not annealed in forming-gas (H_2:N_2/10:90) after metallization. In Fig. 3.19(a) the output characteristics of a SOI and a SSOI p-type Hall-bar FET are compared. At the same gate overdrive the SSOI device features a factor ×1.2 larger current compared to the SOI-FET. The statistical I_on/I_off-plot of about 80 SOI and 80 SSOI devices in the inset of Fig. 3.19(b) confirms the observed on-current enhancement by a factor of ×1.2 for p-type SSOI-FETs over SOI devices. A similar enhancement by a factor of ×1.2 is measured for the transconductance maximum of SSOI p-type Hall-bar FETs compared devices on SOI (Fig. 3.19(b)). This enhancement is in good agreement with the results reported by Takagi et al. (87). In Fig. 3.20 histograms of the transconductance maxima at $V_\text{ds} = -0.5\,\text{V}$ for p-type Hall-bar FETs on SOI (c) and SSOI (d) are shown. P-type Hall-bar FETs on SOI have an average maximum transconductance of $3.54\,\mu\text{S}$ while parallel processed SSOI devices feature an average maximum transconductance of $4.33\,\mu\text{S}$. The threshold voltage of the SSOI devices is shifted due to the strain induced band gap-narrowing, affinity increase and change in the valence band density of states on average by about $\Delta V_\text{th,p-type} = -80\,\text{mV}$ (Fig. 3.20(a) and (b)) in agreement with calculations of Zhang and Fossum (88). The large negative threshold voltage values for the p-type devices are due to the n^+-poly gate.

The transfer characteristics of n-type Hall-bar FETs on 60 nm SOI and 60 nm SSOI are shown in Fig. 3.21(a) and (b), respectively. Similar to the p-type Hall-bar FETs the devices have a good I_on/I_off-ratio. Comparing the on-currents and transconductances of n-type SOI and SSOI Hall-bar FETs, the SSOI devices show a ×1.6 larger on-current and a factor ×1.8 enhanced transconductance (Fig. 3.21(c) and (d)). In Fig. 3.22 the transfer characteristics are compared and the inset shows a statistical $I_{\mathrm{on}}/I_{\mathrm{off}}$-distribution of about 80 SOI and 80 SSOI n-type Hall-bar FETs confirming the on-current enhancement in SSOI n-type devices by a factor of ×1.7 over SOI devices in agreement with results from Takagi (87). Histograms of the maximum transconductance are shown in Fig. 3.23 for n-type Hall-bars on (c) SOI and (d) SSOI. The average transconductance enhancement due to biaxial tensile strain is ×1.7. The average threshold voltage shift due to strain in n-type FETs of $\Delta V_{\mathrm{th,n-type}} = 190\,\mathrm{mV}$ is substantially larger compared to p-type devices (Fig. 3.23). Transconductance enhancement and threshold voltage shift agree well with the theoretical values reported by Zhang and Fossum using their threshold voltage model for strained MOSFETs (89). If this shift is compensated by increased channel doping for off-state control, part of the strain induced mobility gain will be lost due to increased impurity ion scattering.

The effective electron mobility can be determined from the current characteristics of a MOSFET device at low drain bias (6):

$$\mu_{\mathrm{eff}} = \frac{L}{W} \cdot \frac{I_{\mathrm{d}}}{Q_{\mathrm{inv}}\left(V_{\mathrm{g}}\right) V_{\mathrm{ds}}} \tag{3.17}$$

where L and W are the channel length and width, Q_{inv} is the inversion charge density, I_{d} the drain current and V_{ds} the drain to source voltage. To accurately determine the inversion charge density Q_{inv} as a function of gate voltage, a split C-V measurement was performed, to determine the gate-to-channel capacitance in the Hall-bar MOSFETs. Figure 3.24(a) shows the CV-curve after correction for overlap capacitances and the drain current as a function of gate voltage that have been employed to determine the mobility. In Fig. 3.24(b) the effective electron mobility is plotted versus the vertical effective field that has been calculated as (90):

$$E_{\mathrm{vert}} = \frac{Q_{\mathrm{inv}}}{2\epsilon_{\mathrm{Si}}} \tag{3.18}$$

where ϵ_{Si} is the dielectric constant of Silicon. The depletion charge is neglected, since the the devices are fully depleted with a very small doping density. In biaxial tensile strained SSOI with a stress of 1.2 GPa electron mobility is enhanced by a factor of ×1.7 in comparison to a SOI control sample. This enhancement and a maximum mobility in SSOI of $1250\,\mathrm{cm}^2/\mathrm{Vs}$ at low vertical electric field is in excellent agreement with results in recent literature (91; 92).

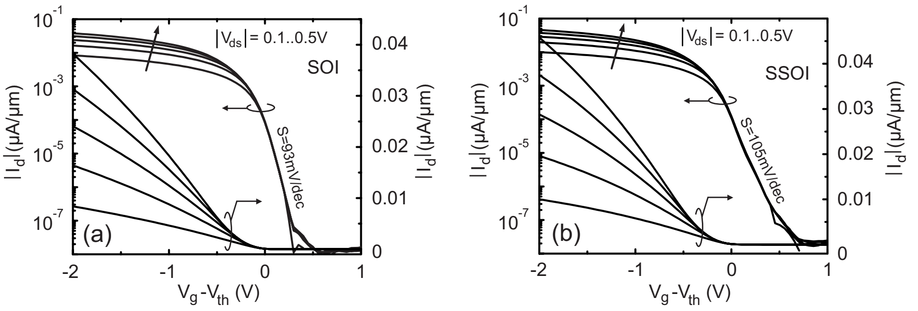


Figure 3.18: Transfer characteristics on a logarithmic and linear scale of p-type Hall-bar MOSFETs on (a) 60 nm SOI and (b) 60 nm SSOI. The devices have a channel width $W = 140\,\mu$m, channel length $L = 670\,\mu$m and gate oxide thickness $t_{\mathrm{ox}} = 8$ nm

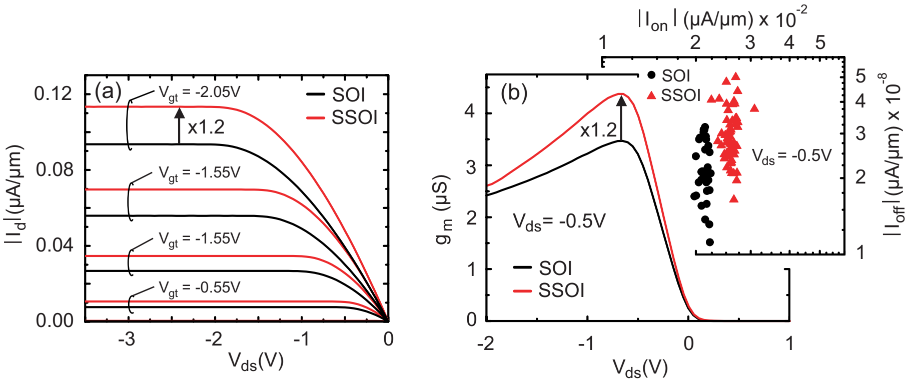


Figure 3.19: (a) Output characteristics of p-type Hall-bar MOSFETs on 60 nm SOI and 60 nm biaxial tensile strained SSOI. (b) Transconductances of the Hall-bar MOSFETs. The inset shows a statistical $I_{\mathrm{on}}/I_{\mathrm{off}}$-plot of the fabricated devices. The SSOI devices show a factor ×1.2 larger on-current and transconductance compared to parallel processed SOI devices.

3.4.3 Low Temperature Measurements

In this section low-temperature magnetoresistance measurements on the n-type Hall-bar MOSFETs discussed in the previous sections are presented. Hall-bar MOSFETs on 60 nm biaxial tensile strained SSOI and 60 nm SOI are investigated. The main objective was to confirm that biaxial tensile strain of around 1.2 GPa does not warp the in-plane conduction band as predicted by band structure calculations.

Cryostat

In this section we discuss the experimental setup used for the measurements presented in this chapter. Figure 3.25(a) shows a schematics of the ^{3}He cryostat used for the measurements. The device under test was glued with

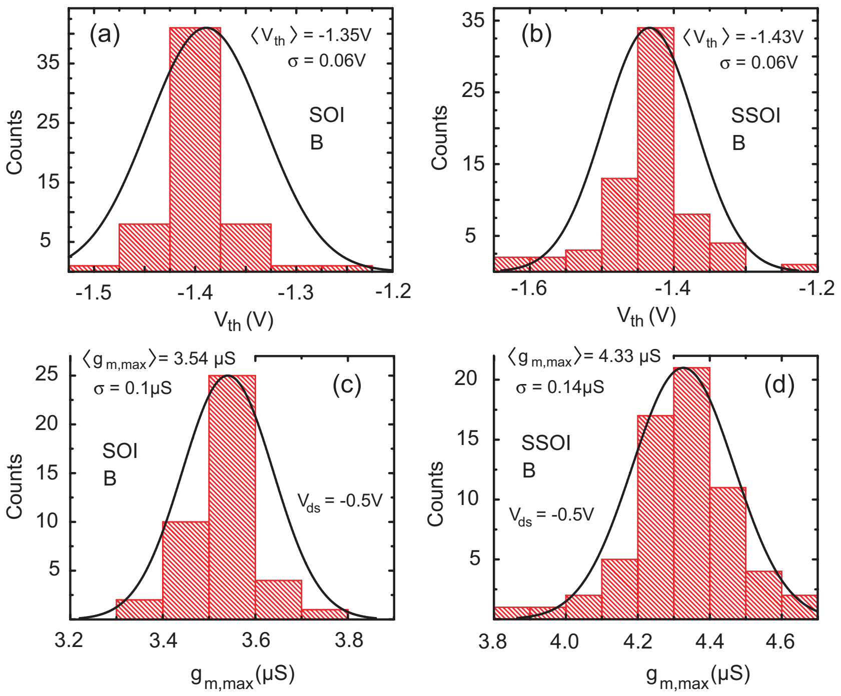


Figure 3.20: Statistical distribution of threshold voltages V_{th} in (a) and (b), maximum transconductance $g_{\mathrm{m,max}}$ at $V_{\mathrm{ds}} = -0.5\,\mathrm{V}$ in (c) and (d) of p-type Hall-bar MOSFETs on 60 nm SOI and 60 nm biaxial tensile strained SSOI.

conductive silver into a chip carrier and the contacts were bonded with an aluminum wire to the contact pads of the chip carrier. The chip carrier was fixed in the sample holder that was lowered into the cryostat. An outer vacuum chamber (OVC) isolates the ^{4}He bath from the surrounding. Inside the ^{4}He bath is an inner vacuum chamber (IVC) that further isolates the probe volume. To obtain temperatures down to 300 mK the sample volume contains a closed ^{3}He loop. At temperatures of 3−7 K ^{3}He is bonded to charcoal particles in the adsorption pump. When the adsorption pump is heated to about 38 K the ^{3}He is removed from the charcoal particles and released into the sample chamber. The 1 K-pot contains liquid ^{4}He of which the temperature is reduced to 1 K by constantly removing the highest energy molecules by pumping. Gaseous ^{3}He condensates at the cold walls of the 1 K-pot and drops into the sample chamber below. When all the ^{3}He is liquified the sample temperature is about 1.2 K. To reduce the sample temperature further the adsorption pump is cooled down to 10 K. At this temperature gaseous ^{3}He is bonded by the charcoal particles and the pressure in the sample chamber is reduced. Evaporation of ^{3}He cools the remaining liquid ^{3}He down to 300 mK.

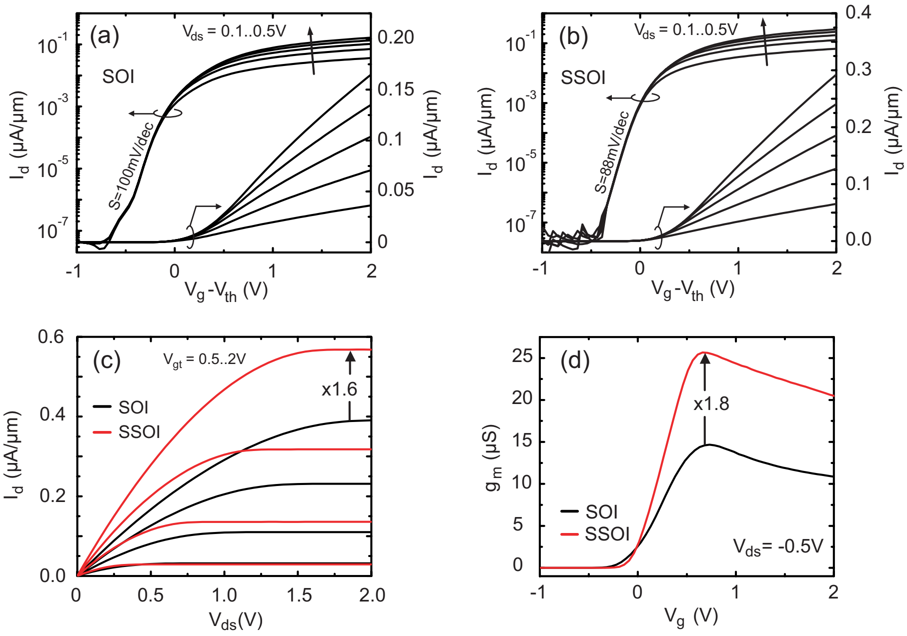


Figure 3.21: Transfer characteristics of n-type Hall-bar MOSFETs on (a) 60 nm SOI and (b) 60 nm SSOI. (c) Parallel processed Hall-bar FETs on 60 nm biaxially strained SSOI feature a factor ×1.6 larger saturation current compared to unstrained SOI devices. (d) The transconductance of SSOI Hall-bar FETs is enhanced by a factor of ×1.8 over unstrained SOI control devices.

Electrical Setup

Sample resistance is measured with a lock-in technique. The measurement of small electrical signals is difficult due to the influence of several parasitics like the 1/f-noise of a preamplifier, the 50 Hz frequency of the net supply voltage etc. A lock-in amplifier measures the absolute value of a signal in a very narrow frequency range, filtering all signal components outside this frequency range. For this a reference signal of the same frequency as the signal to be measured has to be supplied to the lock-in amplifier. For resistance measurement the setup shown in Figure 3.25(b) was used. An ac-voltage from an oscillator is taken as reference for the voltage-controlled current-source. The current produced by the source is proportional to the input voltage. To prevent any ground-loops, the inner measurement circuit is battery driven and electrically separated from the lock-in amplifier by an optical isolation amplifier. The produced current is flowing through the device. The resistance in the channel is measured at two contacts contacting the inversion layer under the gate. The voltage is amplified by a differential amplifier that is connected to an isolation amplifier that decouples the measurement signal from the ground of the lock-in amplifier. The output of the isolation ampli-

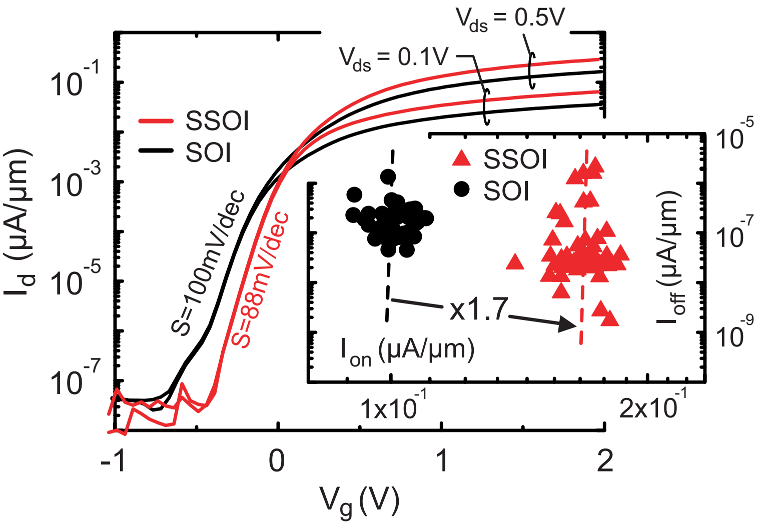


Figure 3.22: Comparison of the transfer characteristics of n-type Hall-bar MOSFETs on 60 nm SOI and 60 nm biaxial tensile strained SSOI. The inset shows a statistical $I_{\mathrm{on}}/I_{\mathrm{off}}$-plot off about 80 SOI and 80 SSOI Hall-bar-FETs. The on-current was measured for each device at a gate-overdrive of 1.2 V and the off-current at 1 V below V_{th}.

fier is connected to the input of the lock-in amplifier. The lock-in amplifier measures the voltage drop at the sample multiplied by the amplification of the differential amplifier.

3.4.4 Results

If a magnetic fields is applied perpendicular to a two dimensional electron gas, the energy eigenvalues split into Landau levels. Therefore, the electrical resistance depends on the magnetic field, due to the variable density of states at the Fermi level. Assuming a homogeneous broadening of the Landau levels, the modulation of the electrical resistance is given by (93; 94):

$$\frac{\Delta\rho_0}{\rho_0} = 4\sum_{n=1}^{\infty} \exp\left(-\frac{-\pi n}{\omega_{\mathrm{c}}\tau_{\mathrm{q}}}\right) \frac{n\xi}{\sinh(n\xi)} \cos\left(\frac{2\pi n E_{\mathrm{F}}}{\hbar\omega_{\mathrm{c}}} - n\pi\right) \tag{3.19}$$

where $\xi = 2\pi^2 k_{\mathrm{B}}T/\hbar\omega_{\mathrm{c}}$, $\omega_{\mathrm{c}} = eB/m_{\mathrm{eff}}$ is the cyclotron frequency, τ_{q} is the quantum relaxation time and E_{F} is the Fermi energy.

Eqn. 3.19 is a Fourier series expansion of a homogeneously broadened density of states convolved with the first derivative of the Fermi distribution function. The first factor in the sum describes homogeneous broadening due to a state lifetime τ_{q}. The second term describes a dampening of the

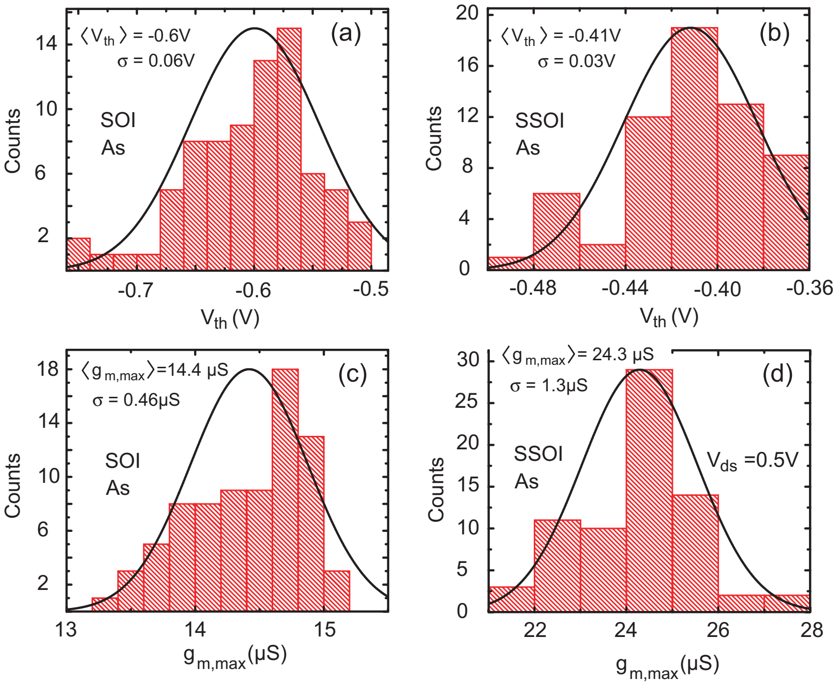


Figure 3.23: Statistical distribution of threshold voltages V_{th} in (a) and (b), and maximum transconductance $g_{\mathrm{m,max}}$ at $V_{\mathrm{ds}} = -0.5\,\mathrm{V}$ in (c) and (d) of n-type Hall-bar MOSFETs on 60 nm SOI and 60 nm biaxial tensile strained SSOI. n-tpye SSOI devices show an average threshold voltage shift of $\Delta V_{\mathrm{th}} = 190\,\mathrm{mV}$ due to strain induced bandgap narrowing, affinity increase and altered valence band density of states.

modulation due to the finite width of the Fermi function. The periodicity of the last term does not depend on $\hbar\omega_{\mathrm{c}}$, even though it appears in the formula, but reflects the degeneracy of the Landau levels. If $2\pi k_{\mathrm{B}}T > \hbar\omega_{\mathrm{c}}$, only the $n = 1$ term in the sum in Eqn. 3.19 need to be considered (95; 96). Thus, if the amplitude of the resistance modulation $\Delta\rho/\rho_0$ is measured at several temperatures, the effective mass can determined.

Shubnikov-de Haas (SdH) oscillations in the longitudinal resistance R_{xx}, measured on a n-type Hall-bar MOSFET on (100) biaxial tensile strained SSOI with a thickness of 60 nm, are shown in Fig. 3.26. The measurement was performed at a gate voltage of $V_{\mathrm{g}} = 1.6\,\mathrm{V}$ in the temperature range from $T = 0.4 - 4\,\mathrm{K}$. The frequency of the oscillations in the longitudinal resistance as a function of the inverse magnetic field are related to the electron concentration by (29):

$$n_{\mathrm{s}} = g_{\mathrm{s}} g_{\mathrm{v}} \cdot \frac{e}{h\Delta(1/B)} \tag{3.20}$$

where g_{s} and g_{v} are the spin- and valley-degeneracy, h is Planck's constant,

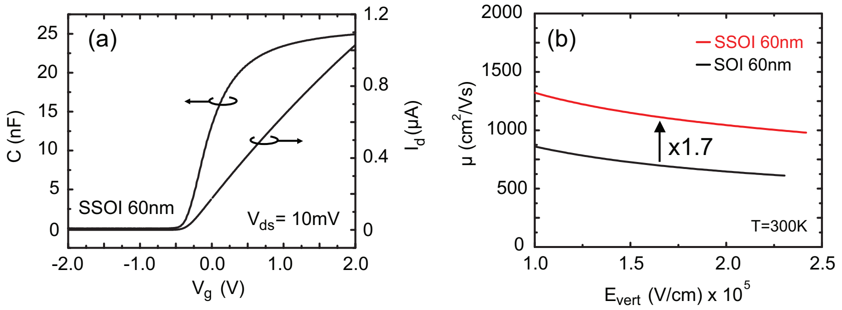


Figure 3.24: (a) Low field effective electron mobility in SOI and SSOI measured with the split-CV technique versus vertical electric field. The effective electron mobility in biaxial tensile strained SSOI is enhanced by a factor of ×1.7 compared to SOI. (b) Capacitance-voltage and drain current gate voltage measurements from which the mobility has been extracted.

e the elementary charge and B the magnetic field.

Therefore, in case of a single conducting subband the Fast Fourier transform (FFT) of the resistance as a function of inverse magnetic field contains only one frequency. In the inset of Fig. 3.26 the FFT of the SdH oscillations measured at $T = 0.4\,\mathrm{K}$ are shown, confirming that in the measurements only the lowest, twofold degenerate, Δ_2-subband is occupied. Changing the gate voltage of the Hall-bar MOSFETs the two-dimensional electron concentration in the inversion layer can be varied. Fig. 3.27(a) displays the FFT of the SdH-oscillations measured at $T = 0.5\,\mathrm{K}$ for gate voltages of $V_\mathrm{g} = 0.4\,\mathrm{V}$, $1.1\,\mathrm{V}$ and $1.6\,\mathrm{V}$ corresponding to electron concentrations of $n_\mathrm{s} = 0.95 \times 10^{12}\,\mathrm{cm}^{-2}$, $n_\mathrm{s} = 2.06 \times 10^{12}\,\mathrm{cm}^{-2}$ and $n_\mathrm{s} = 2.88 \times 10^{12}\,\mathrm{cm}^{-2}$. With increasing gate voltage the frequency of the SdH-oscillations shifts to higher values in accordance with Eqn. 3.20. Since no higher harmonics appear in the SdH oscillations, the carrier concentration can be determined from the inverse magnetic field values corresponding to peaks in the data of Fig. 3.26. In Fig. 3.27(b) the peak positions in reciprocal magnetic field of the SdH-oscillations are plotted against the peak number for three different gate voltages, corresponding to three different electron concentrations. Employing Eqn. 3.20 the electron concentration was determined from the slope of the linear fit to the peak positions in reciprocal magnetic field. The obtained electron concentrations are in very good agreement with the above values determined from the maximum frequency of the FFT of the SdH-oscillations ranging from $0.95 \times 10^{12}\,\mathrm{cm}^{-2}$ for $V_\mathrm{g} = 0.4\,\mathrm{V}$ to $2.88 \times 10^{12}\,\mathrm{cm}^{-2}$ for $V_\mathrm{g} = 1.6\,\mathrm{V}$.

The effective mass can be extracted from the temperature dependence of the SdH oscillation amplitudes A at a fixed magnetic field. After substracting the nonoscillatory background the natural logarithm of the oscillation am-

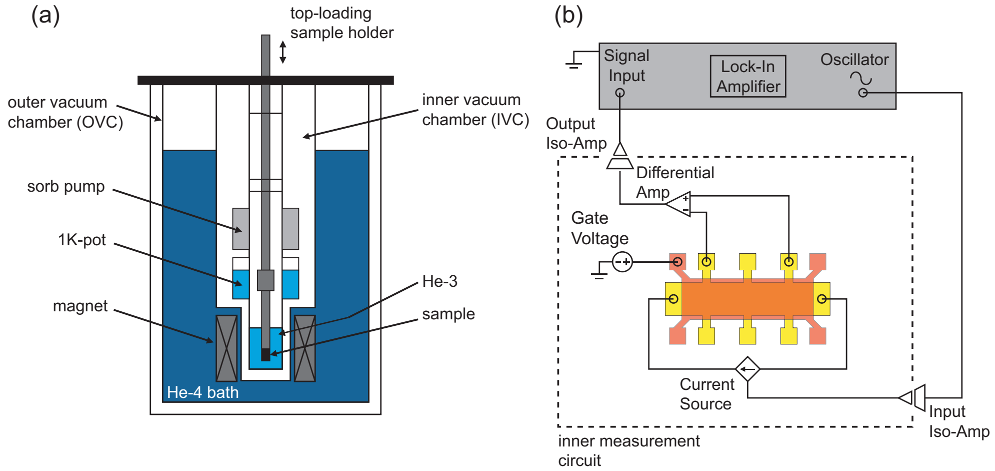

(a)
top-loading
sample holder
outer vacuum
chamber (OVC)
inner vacuum
chamber (IVC)
sorb pump
1K-pot
He-3
magnet
sample
He-4 bath
(b)
Signal
Input
Lock-In
Amplifier
Oscillator
Output
Iso-Amp
Differential
Amp
Gate
Voltage
Current
Source
Input
Iso-Amp
inner measurement
circuit

Figure 3.25: (a) Schematics of the ^{3}He cryostat used for the measurements presented in this chapter. (b) Schematics of the electrical measurement setup used to determine the channel resistance.

plitude A divided by temperature T is plotted as a function of temperature (Fig. 3.28(a)). The data was fitted with a non-linear least square technique (97) with two parameters: (i) the effective electron mass m_{eff}; and (ii) a constant C to the following equation (98):

$$\ln\left(\frac{A}{T}\right) = C - \ln\left[\sinh\left(\frac{2\pi^2 k_{\mathrm{B}} T m_{\mathrm{eff}}}{e\hbar B}\right)\right] \tag{3.21}$$

where k_{B} is the Botzmann constant, $\hbar$ is Plancks constant, e the elementary charge and B the magnetic field. In Fig. 3.28(a) the fits for three magnetic field values at a gate voltage of $V_{\mathrm{g}} = 1.6\,\mathrm{V}$ are shown. The extracted effective electron mass of $m_{\mathrm{eff}} = (0.20 \pm 0.01) \cdot m_0$ is in excellent agreement with the transverse electron mass of conduction band electrons in silicon and measured values of the effective electron mass reported by other authors (94; 96; 99; 95). This demonstrates for the first time experimentally that biaxial tensile stress of about 1.2 GPa does not warp the conduction band constant energy surfaces in accordance with band structure calculations (64; 58; 100). The electron mobility enhancement observed in MOSFETs on biaxial tensile strained SSOI is, therefore, caused by occupation of the Δ_2-valleys with low electron effective mass m_{t} in transport direction and by reduced scattering due to a lower k-space volume. In Fig. 3.28(b) the effective electron mass in biaxial tensile strained Si is plotted against electron concentration. At low carrier concentration of $n_{\mathrm{s}} \approx 1 \times 10^{12}\,\mathrm{cm}^2$ an enhancement of the effective mass is measured. The measured value of $m_{\mathrm{eff}} = 0.24 m_0$ is larger than reported by Smith and Stiles (101) but in good agreement with more recent

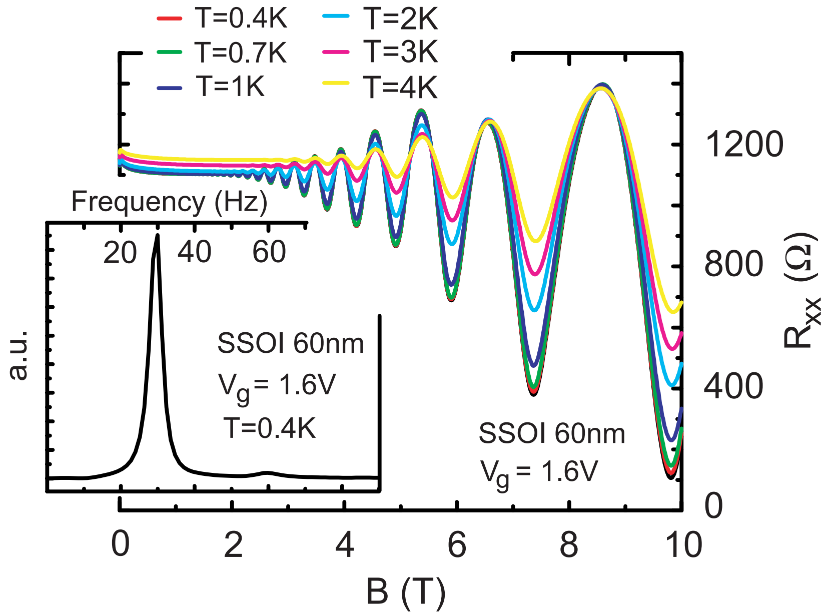


Figure 3.26: Shubnikov-de Haas oscillations of the longitudinal resistance R_{xx} measured with a Hall-bar MOSFET fabricated on 60 nm biaxial tensile strained SSOI with a thickness of 60 nm. The tensile strain in the SSOI is 1.2 GPa as determined by He$^+$-ion channeling. The measurement was performed at a gate voltage of $V_{\mathrm{g}} = 1.6\,\mathrm{V}$ in the temperature range of $T = 0.4 - 4\,\mathrm{K}$. The FFT of the oscillations at $T = 0.4\,\mathrm{K}$ feature a single peak, confirming that only the lowest energy subband is populated (inset).

results reported by Pan (99) and Dragosavac (96).

Fig. 3.29(a) shows the conductance when the magnetic field was held constant at $B = 3\,\mathrm{T}$ while the gate voltage was varied. In contrast to the usual SdH experiment, which measures changes in conductance as the Landau levels move through the Fermi surface, here the Fermi surface is moved through the Landau levels. Because the period of the conductance oscillations is constant, the measurement indicates in this case, that each Landau level contains the same number of states as given by:

$$N_{\mathrm{L}} = g_{\mathrm{s}} g_{\mathrm{v}} \frac{eB}{h} \tag{3.22}$$

.

The period of the oscillations is the change in V_{g} which results in a change in electron concentration n_{s} equal to the number of electrons needed to fill a Landau level. Therefore, the maxima in the conductance occur when the gate voltage satisfies:

$$V_{\mathrm{g}} = i \left(\frac{g_{\mathrm{s}} g_{\mathrm{v}} e^2}{h} \right) B + V_{\mathrm{th}} \tag{3.23}$$

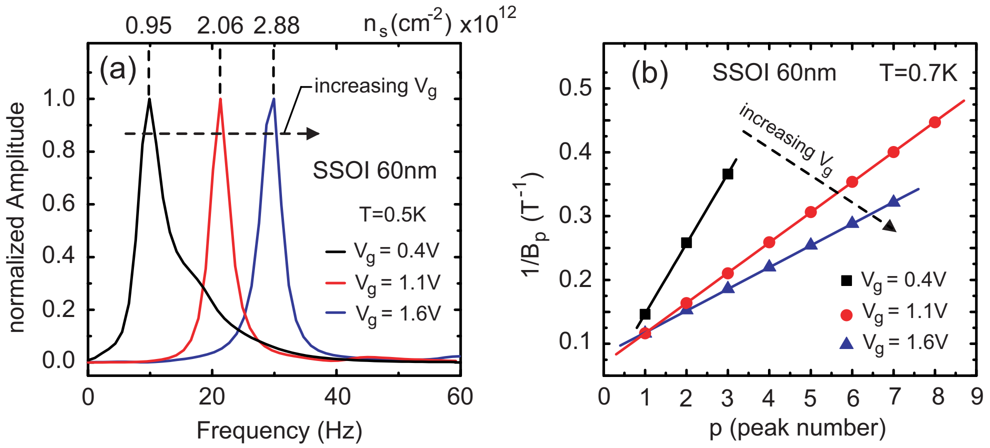


Figure 3.27: (a) FFT of the SdH-oscillations at $T = 0.5\,\mathrm{K}$ for three gate voltages measured on a Hall-bar MOSFET fabricated on 60 nm biaxial tensile strained SSOI. With increasing gate voltage the peak in the FFT shifts to higher frequencies, conrresponding to a higher electron density in the lowest subband. (b) Peak positions in reciprocal magnetic field of the SdH-osicallations for three gate voltages at $T = 0.7\,\mathrm{K}$. From the slope of the linear fit the carrier concentration can be determined.

where i is an integer and V_{th} the threshold voltage. Fig. 3.29(b) shows a plot of the number of the conductance maxima against the gate voltages at which they occur. From the slope of the linear fit the change in carrier concentration with gate voltage was found to be $d(n_{\mathrm{s}})/dV_{\mathrm{g}} = 1.69 \times 10^7\mathrm{V}^{-1}\,\mathrm{cm}^{-2}$. The intercept with the voltage axis gives the threshold voltage as $V_{\mathrm{th}} = -0.6\,\mathrm{V}$. Knowing the carrier density as a function of gate voltage the product of valley and spin degeneracy $g_{\mathrm{v}}g_{\mathrm{s}}$ can be determined from the period of the conductance oscillation. It was found to be 4.2 in satisfactory agreement with the expected value of 4 for the Δ_2-subband of the Si conduction band and spin degeneracy. The capacitance of the Hall-bar MOSFET was determined to be $C_{\mathrm{ox}} = 2.6 \times 10^{-7}\,\mathrm{Fcm}^{-2}$ in good agreement with the value determined by C-V measurements shown in Fig. 3.24(a).

For comparison n-type Hall-bar MOSFETs fabricated on 60nm unstrained SOI were measured. The SdH-osicllations at a gate voltage of $V_{\mathrm{g}} = 0.7\,\mathrm{V}$ in the temperature range of $T = 0.5 - 6\,\mathrm{K}$ are shown in Fig. 3.30. Only the lowest subband is occupied in the measurements as confirmed by FFT of the SdH oscillations (inset of Fig. 3.31(a)). The carrier concentration was extracted to be $n_{\mathrm{s}} = 1.23 \times 10^{12}\,\mathrm{cm}^{-2}$ from the peak positions in reciprocal magnetic field as described above (Fig. 3.31). From the temperature dependence of the oscillation amplitude at a fixed magnetic field the efffective electron mass was deduced employing the same fitting procedure as for the SSOI samples. Fig. 3.31(b) shows the fits for three values of the magnetic field. Within ex-

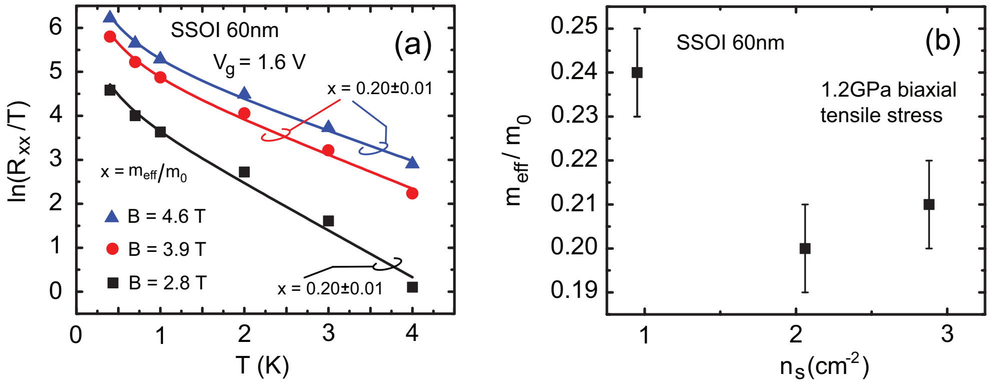


Figure 3.28: The effective electron mass can be determined from the temperature dependence of the SdH-amplitudes. (a) Fitting the effective mass at a gate voltage of $V_g = 1.6\,V$ for three magnetic field values. (b) shows the dependence of the effective electron mass on electron concentration.

perimental error no difference between the effective electron mass in biaxial tensile strained SSOI and SOI could be measured. This confirms

3.5 Summary

- **Thin Virtual Substrat Technology for the Fabrication of SSOI** sSi layers with a thickness of 8 nm were formed by strain transfer between a SiGe buffer and a Si cap layer. This thin sSi layer is sufficient for the fabrication of ultra thin body SOI MOSFETs. The main advantages of the strain transfer method are that only one epitaxial growth step is required to make an ultrathin strained layer and standard silicon clean can be applied for optional epitaxial overgrowth. Thicker sSi layers were obtained by sSi or SiGe/sSi overgrowth. A tensile strain of 0.8% was measured by Raman spectroscopy for an 18.5 nm sSi layer grown directly on such a heterostructure. The TD density was reduced to $1 \times 10^6\,\mathrm{cm}^{-2}$ by epitaxial overgrowth of a strain adjusted SiGe layer on top of the relaxed buffer. Excellent surface morphology with an rms surface roughness of 0.8 nm of the He relaxed and overgrown structures was found which allows direct wafer bonding without surface chemical mechanical polishing.

- **Asymmetric Strain Relaxation in Si/SiGe Heterostructures** Strain relaxation of patterned SiGe lines after He^+ ion implantation and annealing has been investigated. Asymmetric relaxation of the SiGe lines transforms biaxial stress into strongly asymmetric stress for

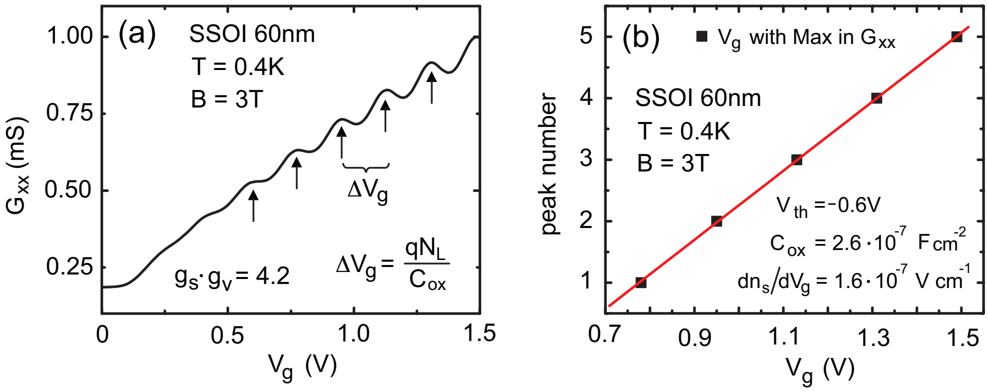


Figure 3.29: (a) Conductance as a function of gate voltage at a temperature of $T = 0.4\,\mathrm{K}$ and a magnetic field of $B = 3\,\mathrm{T}$ measured with a Hall-bar MOSFET on 60 nm biaxial tensile strained SSOI. Contrary to the SdH-oscilations displayed in Fig. 3.26, which measure changes in the resistance as the Landau levels move through the Fermi surface, here the Fermi surface moves through the Landau levels. The product of spin and valley degeneracy was deduced to be $g_\mathrm{s} \cdot g_\mathrm{v} \approx 4.2$ from the period of the oscillations. (b) Gate voltages with peak values of the conductance plotted versus gate voltage. Threshold voltage, gate capcitance and $dn_\mathrm{s}/dV_\mathrm{g}$ can be deduced from the linear fit.

very narrow lines which should yield to significant improvements of the electron and hole mobilities (table 3.1). The effect is explained by the limitation of the path lengths of the threading dislocations by the stripe boundary leading to an asymmetric misfit dislocation network. These lines are attractive for the fabrication of strained nanowire heterostructure MOSFETs with improved electron and hole mobilites.

- **Electrical Measurements on SOI and SSOI Hall-bar MOSFETs**

  The relevant physical properties of biaxial tensile strained SSOI for its application in field-effect devices have been extensively studied.

  N- and p-type Hall-bar MOSFETs were fabricated on SOI and SSOI. On-current and transconductance improvements due to strain of a factor ×1.2 for p-type and ×1.7 for n-type SSOI devices were experimentally demonstrated. An effective electron mobility enhancement by a factor of ×1.7 over a range wide range of vertical electrical field values and a peak mobility value of $1250\,\mathrm{cm}^2/\mathrm{Vs}$ at low vertical field are in perfect agreement with recent results by other groups.

  The effect of biaxial tensile strain on the electron affinity has been experimentally determined by measuring the threshold voltage shifts in SSOI devices compared to unstrained FETs. The observed threshold voltage shifts compare very well to recent theoretical models that

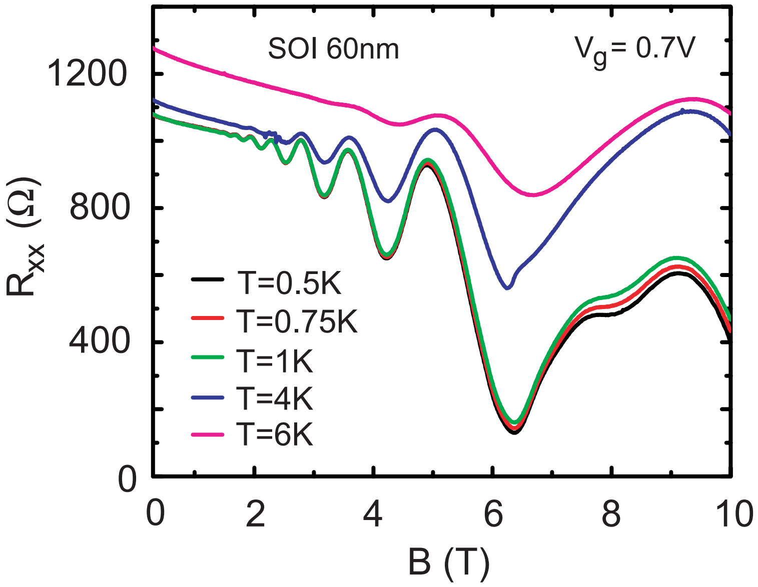


Figure 3.30: Shubnikov-de Haas oscillations measured on a 60 nm SOI Hall-bar MOSFET at a gate voltage of $V_\mathrm{g} = 0.7\,\mathrm{V}$ in the temperature range from $T = 0.5 - 6\,\mathrm{K}$.

incorporate strain altered electron affinity changes.

For the first time, the effective electron mass as a function of electron concentration in biaxial tensile strained SSOI has been experimentally determined from the temperatures dependence of Shubnikov-de Haas oscillations in the longitudinal resistance. No change in mass compared to unstrained SOI samples were observed. This proves that biaxial tensile stress of about 1.2 GPa does not warp the in-plane conduction band constant energy surfaces in accordance with band structure calculations. The electron mobility enhancement observed in MOSFETs on biaxial tensile strained SSOI is, therefore, caused by occupation of the Δ_2-valleys with low electron effective mass m_t in transport direction and by reduced scattering due to a lower k-space volume.

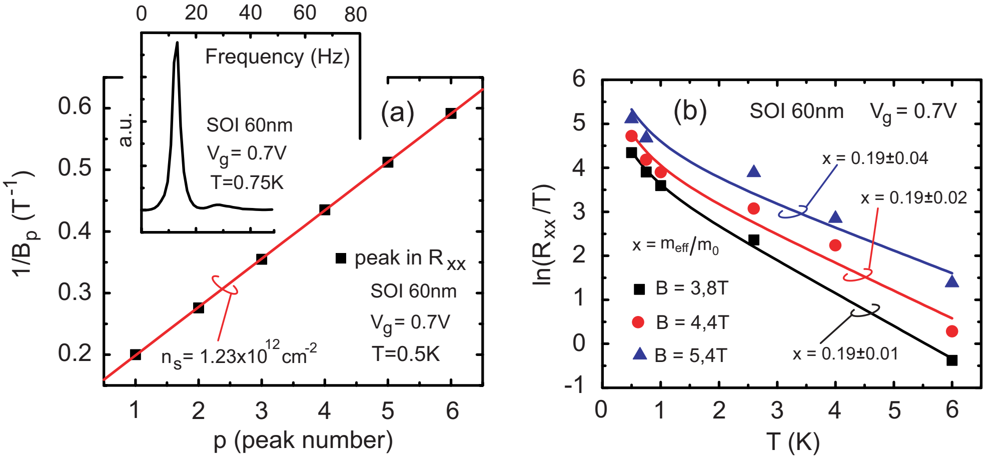


Figure 3.31: (a) Peak positions in reciprocal magnetic field of SdH oscillations of Fig. 3.30 for a temperature of $T = 0.5\,\mathrm{K}$. The data was fitted to determine the carrier concentration. The inset shows the FFT of the SdH oscillations at $T = 0.75\,\mathrm{K}$ confirming that only the lowest subband is occupied. (b) Fits to determine the effective mass of electrons in the lowest subband of the SOI Hall-bar MOSFET for three magnetic field values.

Chapter 4

Multigate Devices - Si Nanowire

4.1 Introduction

Improving the performance of MOSFETs by downscaling of the conventional silicon MOSFETs has become extremely difficult and technologically challenging: To avoid the appearance of short channel effects multi-gate architectures such as FinFETs and in particular gate-all-around (GAA) nanowire (NW) FETs have to be employed in ultimately scaled devices (11). Recently such GAA NW-FETs with excellent performance have been demonstrated (102). At the same time a lot of effort is devoted to high-mobility channel materials that enable performance improvements without scaling. In particular strained silicon is currently accepted as the key solution for CMOS performance improvements being integrated in leading edge fabrication processes (103). It is therefore appealing to combine a GAA NW-FET architecture with a high-mobility material in order to achieve the best performance possible. Biaxially strained SOI (SSOI) is particularly suited for this purpose since nanowire devices can be fabricated with accurate control of device position and crystalline direction in a top-down approach. However, it is known that small islands of SSOI tend to relax depending on the structures length to width ratio leading to uniaxially strained silicon (104).

In this chapter a fabrication process of Silicon NWs on SOI and biaxially strained SOI substrates is described and electrical characteristics of fabricated devices are discussed. Electron Beam Lithography (E-beam) is used to define the initial NW that is further thinned by oxidation and etching. Using biaxially strained silicon as starting material pattern dependent strain relaxation is used to fabricate uniaxial tensile strained NWs. Furthermore,

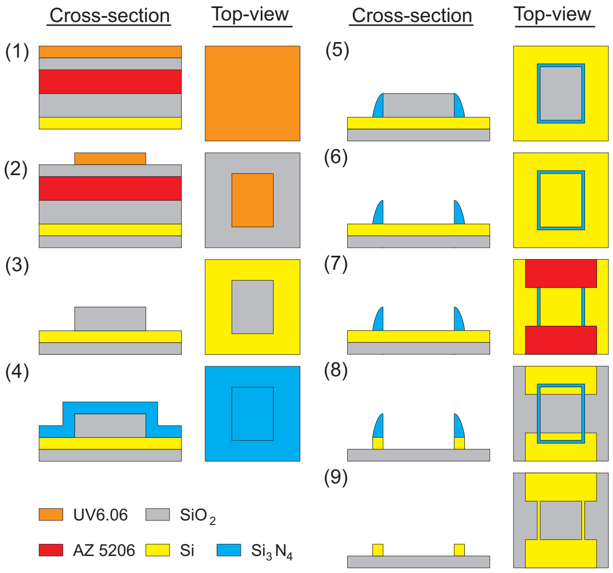


Figure 4.1: Process flow for the fabrication of Si NWs using sidewall spacer technology.

mobility enhancement and on-current gain in Si NW-FETs fabricated on SOI and biaxially SSOI are investigated. Comparing SOI and SSOI a 2.3 times larger mobility and similiar on-current improvement is observed in long channel SSOI NW-FETs. In addition, NW-FETs with triangular cross-section and channel length of $L = 200 - 800\,\text{nm}$ are presented.

4.2 Sidewall Spacer Technology

Sidewall spacer technology (SST) uses standard optical lithography and RIE to form spacers that further serve as hard mask in a subsequent patterning step to achieve feature sizes smaller then the diffraction limit for the wavelength of light used in the lithography step. The technique has the advantage that feature sizes of several tens of nanometers can be achieved without the need for expensive state of the art lithography tools (105). Also the throughput is higher compared to electron beam lithography. The technique relies on the availability of several materials that can be etched selectively to one another. It further demands a good thickness and step coverage control of the various films involved and requires directional dry-etching to create vertical sidewalls. Disadvantageous are the very stringent demands on process control and the significantly larger number of process steps involved to fabricate short channel transistors with SST compared to E-beam lithography. Figure 4.1 illustrates the process steps necessary to create the mesa struc-

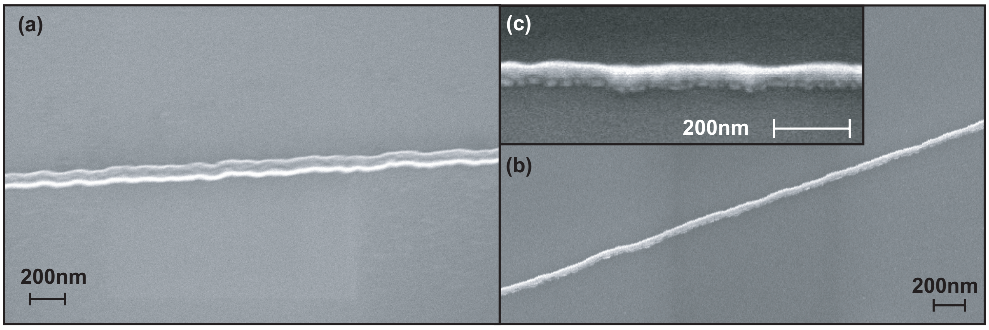


Figure 4.2: SEM images of Si NWs fabricated by the SST method. (a) Top view of a Si NW on BOX with homogenous width. (b) titled view of a long Si NW with good homogeneity over a long distance. (c) Titled view of a Si NW showing the line edge roughness resulting from RIE etching.

ture of a nanowire MOSFET on SOI using SST. The materials used in this example can be replaced by other materials that can be etched selectively to one another.

The process started with the deposition of 100 nm SiO_2 by LPCVD on a cleaned (100) SOI substrate. Then the sample was coated with AZ5206 photoresist and backed for 15 min at 150 °C, followed by the deposition of 50 nm SiO_x by E-beam evaporation. In the last step UV6.06 photoresist was spun onto the sample and backed for 1 min at 130 °C. A rectangular structure was patterned by optical lithography into the UV6.06 layer and transferred by RIE using a $JCHF_3$ plasma into the 50 nm SiO_x layer. Subsequently the AZ5206 and the 100 nm SiO_2 layer were etched with an O_2 and a $JCHF_3$ plasma, respectively. During these etching steps the AZ5206 and the top 50 nm SiO_x layer were removed. On top of the remaining SiO_2 structure 80 nm Si_3N_4 was deposited by LPCVD. The thickness of the Si_3N_4 layer and the SiO_2 structure define the width of the resulting Si NWs. Si_3N_4 spacer are then created by etching the nitride layer in a $JCHF_3$ plasma. After removing of the SiO_2 with HF two rectangular structures that overlap with the Si_3N_4 spacers are patterened in a second optical lithography step. These rectangels define the source and drain areas of the transistor. The SOI layer is then etched with an Ar/SF_6 plasma. After removing the photoresist with aceton and propanol, the Si_3N_4 spacers are etched selectively to the SOI and the BOX with hot phosphoric acid.

Figure 4.2 shows SEM images of Si NWs fabricated with the SST process described above. In Fig. 4.2(a) an $\approx$ 60 nm wide silicon line on BOX is shown. The line has a homogenous width but features substantial wiggling. The homogenous width of the line suggests that the spacers formed by etching

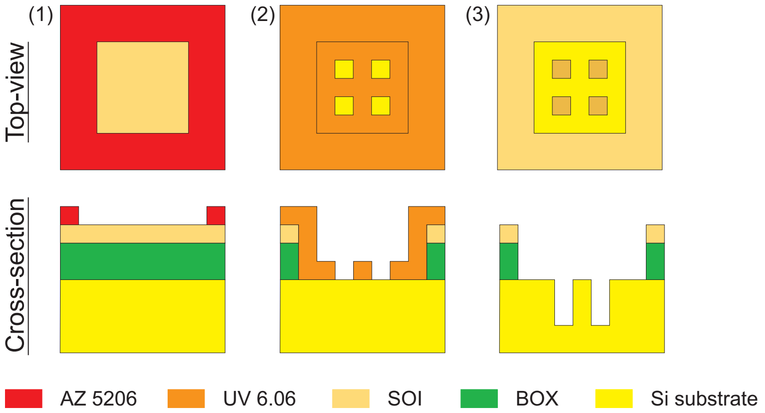


Figure 4.3: Process for the fabrication of markers for electron beam lithography.

the Si_3N_4 layer are uniform in width. The wiggling of the line most probably results from wiggling of the edges of the SiO_2 structure formed by optical lithography at which sides the spacers are formed. The sidewalls of the line feature significant roughness as a result of the RIE etching (Fig. 4.2 (c)).

4.3 Fabrication of NW-MOSFETs

Ebeam Lithography Markers

The fabrication of Si-NW transistors includes several oxidation steps. Therefore is is not possible to use the conventional metallic E-beam lithography markers. An alternative marker type was developed that uses holes etched into the silicon substrate. The definition of these markers requires two optical lithography and RIE steps and is outlined in Fig. 4.3. In the first step $150 \times 150\,\mu m^2$ windows are defined by negative optical lithography in the photoresist and etched down to the Si substrate. In a second step four $15 \times 15\,\mu m^2$ squares are defined inside the first square and then transferred into the silicon substrate using a fast etching SF_6-plasma. Experience has shown that 600 nm deep holes work as high contrast markers in the following E-beam lithography steps even after deposition of polysilicon and SiO_2 layers.

Two Layer Resist System

Different negative resists were tested for E-beam lithography. The best results in terms of the obtained minimal structure size and uncomplicated processing were obtained with hydrogen silsesquioxane (HSQ). The disadvantage of HSQ is that it can only be removed by HF after E-beam exposure or after backing above a critical temperature (≈ 300 °C). When the HSQ resist is removed with HF from structures defined on SOI these structure will be partly underetched. Underetching can lead to shortcuts between the source/drain areas and the gate of the transistor. To circumvent this problem of underetching while maintaining the good resolution of HSQ, a two layer resist system was used. The samples were first coated with the optical photoresist AZ5206. The resist was then backed for 15 min at 150 °C. Afterwards HSQ was spun on top of the backed AZ resist and the samples were heated again for 2 min at 150 °C and 2 min at 220 °C. Since the two resists can be etched selectively, underetching is avoided. The structures were written by E-beam lithography into the HSQ. An oxygen plasma was used to transfer the structures into the AZ resist, that served as etch mask for the transfer of the structures into the SOI layer.

Nanowire Transistor Fabrication Process

1. *Definition of the NW and the source-drain pads:*
   After cleaning with aceton and propanol, the samples were coated with the HSQ/AZ two layer resist system described above. The NW and the source and drain contact areas were then written by E-beam lithography, the contact areas with a single pass exposure and the wires using multiple-pass exposure.

2. *Mesa definition:*
   The structures were transferred into the SOI layer by RIE etching first with a O_2 and afterwards with a Ar/SF_6-plasma.

3. *Thinning and smoothing of the NWs:*
   After a standard RCA cleaning procedure a 5-8 nm SiO_2 was grown on the samples in a rapid thermal oxidation furnace. The oxidation smoothens roughness at the NW surface caused by RIE etching and decreases the NW diameter. Several cycles of oxidation and HF etching are used to thin the NW down to the desired diameter.

4. *Gate stack deposition:*
   After the growth of a RTO gate oxide, 200 nm n-type polysilicon and 80 nm SiO_2 were deposited by LPCVD. The n-polysilicon are activated by RTA at 950 °C for 1 min in N_2 atmosphere.

5. *Gate stack definition:*
   For the definition of the gate stack the two layer resist system was

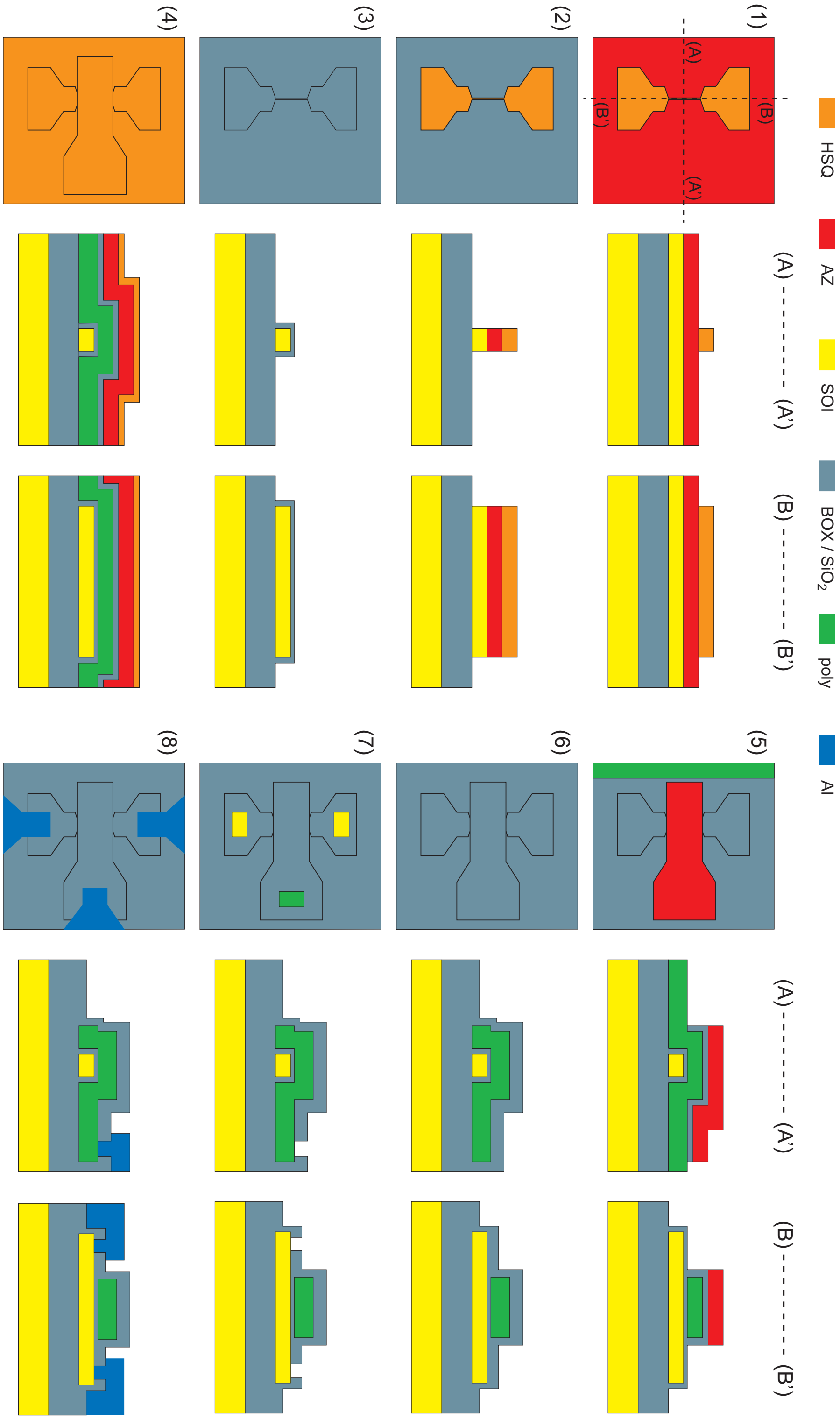

(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(A)
(A')
(B)
(B')
(A) - - - - - - - - (A')
(B) - - - - - - - - (B')
HSQ
AZ
SOI
BOX / SiO$_2$
poly
Al

Figure 4.4: Process flow for the fabrication of Si NW transistors.

employed again and the gate defined by E-beam lithography. After etching of the AZ-resist with an O_2-plasma, the n-poly-Si was etched by ICP with a highly selective HBr-plasma.

6. *Source/drain contact implantation:*
   The source/drain areas of n-type devices were implanted with As at an energy of 8 keV to a dose of $5 \times 10^{14}\,\mathrm{cm}^{-2}$ and in the case of p-type devices with B at an energy of 4 keV to a dose of $1 \times 10^{15}\,\mathrm{cm}^{-2}$. After implantation a 80 nm LPCVD SiO_2 were deposited. As and B dopants were activated by RTA at 950 °C for 30 sec and at 1000 °C for 10 sec in N_2 atmosphere, respectively.

7. *Contact windows:*
   Optical lithography and RIE with a $JCHF_3$-plasma were employed to open contact windows at the gate and source/drain of the devices. The contact surfaces were cleaned with a short O_2-plasma step.

8. *Metallization of the contacts:*
   The final fabrication step was the metallization of the gate, source and drain contacts by lift-off process. Optical lithography was used to define the metallization areas. The native oxide on top of the silicon is removed by wet etching with 1% HF. Directly after HF-etching 200 nm aluminum wa deposited by E-beam evaporation. Finally, the photoresist was removed by immersing the samples in aceton and popanol leaving behind the contact metallization.

4.4 Electrical Characterization

In this section experimental results on Si NW-MOSFETs are presented. The devices were fabricated in a top-down approach on unstrained and biaxially strained SOI substrates exhibiting good I-V characteristics with $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratios of 10^7 and off-currents as low as 10^{-13} A. Subthreshold slopes of about 70 mV/dec for SOI n- and p-FETs and 65 mV/dec for strained SOI n-FETs were obtained. The on-current and transconductance of Si NW-FETs fabricated on strained SOI substrates are 2.5 and 2.1 times larger, respectively, due to the uniaxial tensile strain along the wires. Moreover, current transport on surfaces with different crystal orientation in NWs is employed to match on-currents of SOI n- and p-FETs. Finally, the dependence of mobility enhancement on channel length in uniaxially strained devices fabricated by the lateral strain relaxation technique is discussed based on experimental data from shorter channel length n-type devices.

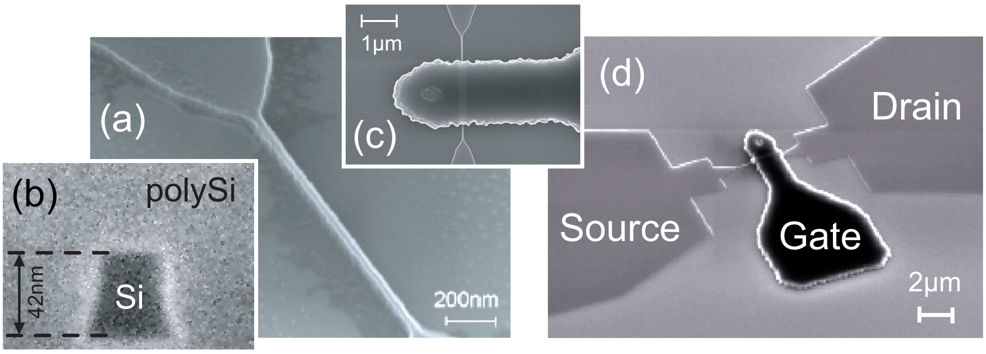


Figure 4.5: SEM images of fabricated NW-FETs on SOI and SSOI. (a) Si NW after RIE; (b) Cross-section SEM image of a trapezoidal NW after gate oxidation and polySi gate deposition; (c) Top-view of the polySi gate covering the NW; (d) Overview of the device with large source/drain areas connected by a NW that is covered by the polySi gate.

SOI and SSOI (001) wafers with top Si thickness of 50 nm and buried oxide thickness of 140 nm were used as starting material. Both SOI and SSOI substrates were p-doped with a concentration of $1 \times 10^{15}\,\mathrm{cm}^{-3}$. The SSOI was manufactured as discussed in chapter 2.

In this work biaxial tensile strained SSOI with a strain of $\epsilon_{\mathrm{biax}} = 0.65\%$, corresponding to a stress of 1 GPa, as measured by He^+-ion channeling angular scans and Raman Spectroscopy was used. Si-NWs on both SOI and SSOI were defined along the $< 110 >$-direction using E-beam lithography and RIE. To reduce sidewall roughness of the NWs, the samples were subjected to a sacrificial oxidation followed by diluted HF stripping of the oxide. The final NWs have a trapezoidal cross-section of $\approx 42 \times 42\,\mathrm{nm}^2$ (width x height) and a length of $L = 1.5\,\mu\mathrm{m}$ and $L = 3\,\mu\mathrm{m}$, as shown in the SEM image in Fig. 4.5(a) and (b). The gate oxide with a thickness of $t_{\mathrm{ox}} = 5\,\mathrm{nm}$ was subsequently formed by dry oxidation at a temperature of 850°C, followed by deposition of 200 nm n-type poly-Si and 80 nm SiO_2 in a low-pressure chemical vapor deposition (LPCVD) tool. E-beam lithography and RIE were then employed to define the gate. The Si NW is gated from three sides: on top and on both sides of the NW, as indicated in the inset of Fig. 4.5(b) and (c). The source/drain areas were formed by implantation of B (4 keV, $1 \times 10^{15}\,\mathrm{cm}^{-2}$) for p-type devices and As (16 keV, $5 \times 10^{14}\,\mathrm{cm}^{-2}$) for n-type devices. After deposition of a protective 80 nm SiO_2 layer by LPCVD, dopant activation was performed at a temperature of 1000 °C for 10 sec. Metallization contact windows were opened and aluminum was deposited by E-beam evaporation and lift-off. Finally, post-metal annealing was performed at 400 °C for 10 min in forming gas ($\mathrm{H}_2 : \mathrm{N}_2/10 : 90$). Figure 4.5(d) shows a SEM picture of a

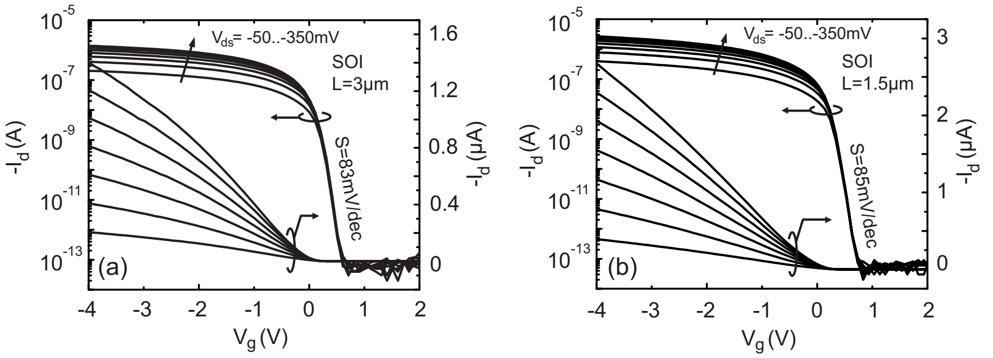


Figure 4.6: Transfer characteristics on a linear and logarithmic scale of NW p-FETs fabricated on SOI with a channel length of (a) $L = 3\,\mu$m and (b) $L = 1.5\,\mu$m. The NW channel has a trapezoidal cross-section of $\approx 42\,\mathrm{nm}^2$ and the gate oxide thickness is 5 nm.

typical device used in this work with large source and drain areas connected by the Si NW covered by the poly-Si gate with a length of $1.5\,\mu$m.

4.4.1 Long Channel SOI NW-FETs

The transfer characteristics on a linear and logarithmic scale of two p-type and two n-type devices with $L = 3\,\mu$m and $L = 1.5\,\mu$m are shown in Fig. 4.6 and Fig. 4.8, respectively. All devices have high $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratios of 10^7 and very low off-currents of 10^{-13} A. The subthreshold slopes are about $S \approx 80\,\mathrm{mV/dec}$. In Fig. 4.7(a) the transconductances and in Fig. 4.7(b) the output characteristics of two pFETs with $L = 1.5\,\mu$m and $L = 3\,\mu$m are compared. Both devices have high source/drain parasitic resistances and therefore do not saturate ideally. Transconductance scales approximately according to MOSFET theory by $g_{\mathrm{m}} \propto 1/L$ being a factor two larger in the $L = 1.5\,\mu$m channel device while the saturation current at similar overdrive of $|V_{\mathrm{g}} - V_{\mathrm{th}}| = 1.8$ V is enhanced by a factor of ×1.5 when the channel length is reduced from $L = 3\,\mu$m to $L = 1.5\,\mu$m (Fig. 4.7(b)). Figure 4.8 and Fig. 4.9 show the transfer and output characteristics of two n-type SOI NW-FETs with gate length $L = 3\,\mu$m and $L = 1.5\,\mu$m, respectively. Due to the better activation of As-dopants source/drain resistances are lower compared to the p-type devices and the output characteristics saturate perfectly.

In multi-gate devices current flows on planes with different surface orientations which have different mobilities due to the anisotropy of Si. It is therefore possible to optimize I_{on} of n- and p-type devices by choice of channel direction and height-to-width ratio of the channel (106). Hole mobility is largest on the (110)-plane with transport in the $< 110 >$-direction while electron mobility is much lower on (110)-compared to its largest value on the

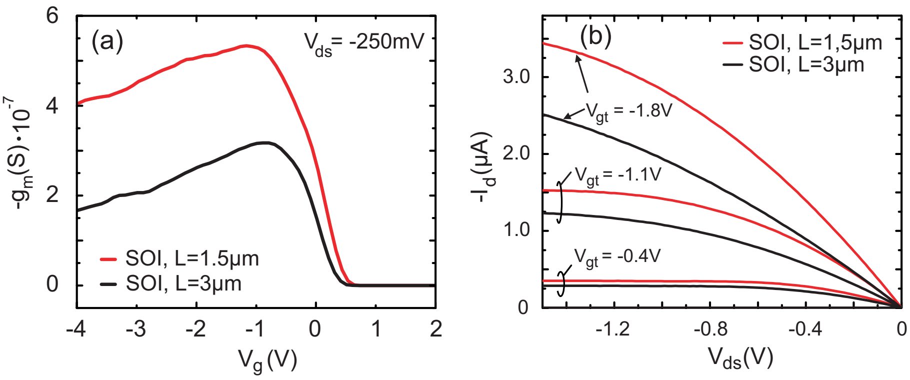


Figure 4.7: Transconductance (a) and output characteristics (b) of two NW p-FETs with channel $L = 1.5\,\mu$m and $L = 3\,\mu$m. On-current and transconductance scale approximately $\propto 1/L$ according to theory.

(001)-surface (63). However, even if electron mobility is low on the (110)-surface with current along a $< 110 >$-direction, this orientation is preferred for offering the best compromise between n- and p-type NW-FET performance. Therefore, in this study, channels were aligned along the $< 110 >$-direction, the vertical sidewalls of the devices becoming (110)-planes while the top surface is a (001)-plane (Fig. 4.10(a)). In this case the performance of n- and p-type NW devices with identical geometry should be more symmetric if the source/drain resistances are comparable. The on-current ratio between n- and p-type devices can be estimated for the fabricated devices where 2/3 of the inverted surface area is of (110)- and 1/3 of (100)-type to be $I_{\mathrm{d,n}}/I_{\mathrm{d,p}} \approx 1.2$ using the simple approximation

$$I_{\mathrm{d}} \propto \frac{W_{\mathrm{eff}}}{L} \cdot \left(\frac{2H}{W_{\mathrm{eff}}} \cdot \mu^{(110)}_{e/h,<110>} + \frac{W}{W_{\mathrm{eff}}} \cdot \mu^{(100)}_{e/h,<110>} \right) \tag{4.1}$$

for $n_{\mathrm{inv}} = 1 \times 10^{13}\,\mathrm{cm}^{-2}$ on the basis of the mobility values reported in (63), where H and W are the channel height and width, respectively, $W_{\mathrm{eff}} = W + 2H$ is the effective channel width.

However, for the devices under test the current of the n-type devices at $V_{\mathrm{g}} = V_{\mathrm{d}} = 1.2\,\mathrm{V}$ is still $\times 1.6$ times larger than that of p-type devices of equal geometry (Fig. 4.10(b)). This value is smaller compared to values commonly found for standard planar devices but not as small as theoretically expected. This discrepancy can be explained as follows: i) the fabricated p-type devices had a larger source/drain resistance compared to the n-FETs as extracted from the output characteristic at low V_{ds} and high V_{g}; ii) the trapezoidal cross-section of the NWs indicate a deviation of the vertical sidewalls from the (110)-surface reducing the effective channel width with higher hole mobility.

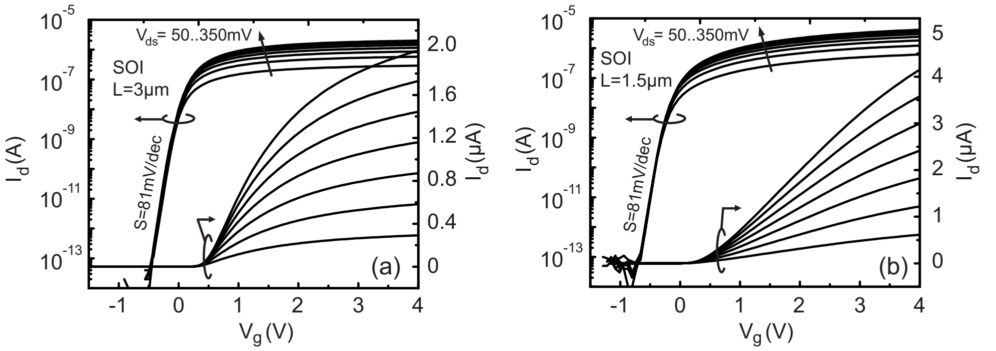


Figure 4.8: Transfer characteristics on logarithmic and linear scale of two NW n-FETs fabricated on SOI with channel $L = 1.5\,\mu$m and $L = 3\,\mu$m. Due to the good electrostatic the devices have a very low off-current and a high $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio.

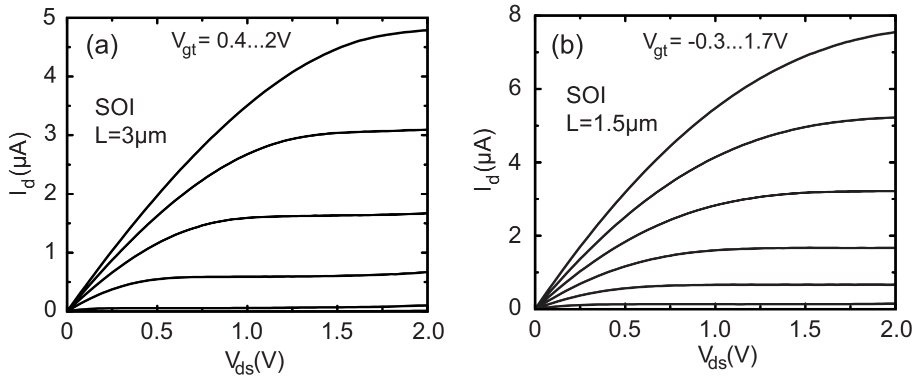


Figure 4.9: Output characteristics of the two SOI NW n-FETs shown in Fig. 4.8 with channel length (a) $L = 3\,\mu$m and (b) $L = 1.5\,\mu$m. The NW channel has a square cross-section of $\approx 40\,\mathrm{nm}^2$ and the gate oxide thickness is $5\,\mathrm{nm}$.

4.4.2 Long Channel SSOI NW-FETs

The lower electron mobility on (110)-surfaces in the $< 110 >$-direction can be improved through strain engineering. In order to investigate the impact of strain on device performance long channel n-type NW-FETs on (100)-SSOI substrates were fabricated. The SSOI had a thickness of 50nm and the BOX of 140nm. The fabrication process and device geometry are equal to the SOI NW-FETs presented in the previous paragraph.

Effect of Uniaxial Tensile Strain on the Subband Structure

Uniaxial tensile strain has been shown to alter the subband structure in the inversion layer (107). On (110) and (100)-surfaces tensile uniaxial strain along $< 110 >$ lowers the energy of the $\Delta 2$- valleys relative to the $\Delta 4$-

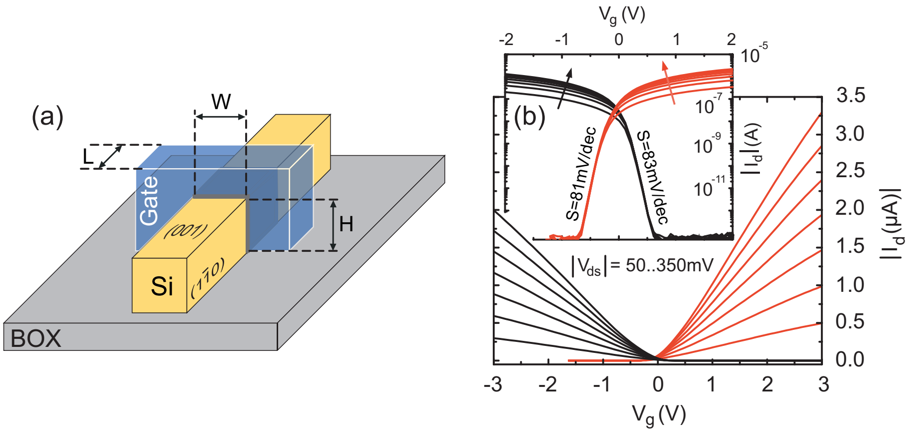


Figure 4.10: (a) Sketch of the fabricated NW devices. The trapezoidal channel has a length L, width W and height H. For devices on (100) SOI current flows on the (001)−top surface and the two $(\bar{1}10)$−planes. (b) Transfer characteristics of n- and p-type NW-FETs fabricated on 50 nm SOI. Both devices have a channel length of $L = 1.5\,\mu\text{m}$ and a gate oxide thickness of $t_{\text{ox}} = 5\,\text{nm}$.

valleys thereby increasing their occupation. On the (110)-surface the Δ2-valleys have the transverse electron mass m_t in $< 110 >$-direction and the longitudinal electron mass m_l along the $< 001 >$-direction ensuring a high mobility and a high density of states for the sub-band. Regarding the (100)-surface uniaxial tensile strain along $< 110 >$ achieves nearly equal electron mobility enhancement as biaxial strain (63). The preferentially occupied Δ2-valleys have the lower effective electron mass m_t in transport direction and conduction band warping caused by uniaxial tensile strain along $< 110 >$ additionally reduces m_t below it value in bulk Si (62).

Strain Relaxation

In order to experimentally verify the impact of uniaxial strain on device performance long channel n-type NW-FETs on SSOI were fabricated. Unpatterned biaxial SSOI layers are robust to relaxation even when the critical thickness of strained Si is exceeded. However, small isolated structures of strained Si become susceptible to strain relaxation (Fig. 4.12(a) and (b)) (104). The relaxation sensitively depends on the island dimensions and the process conditions (108). A 2D finite element simulation was performed to investigate the dependence of lateral strain relaxation on the NW geometry (109). For the simulations the elastic constants of bulk silicon have been used. Biaxial tensile strain has been modeled by applying the same force per unit length on all four sides of the rectangular structure. To obtain the strain state in the relaxed structure, the straining force was removed from

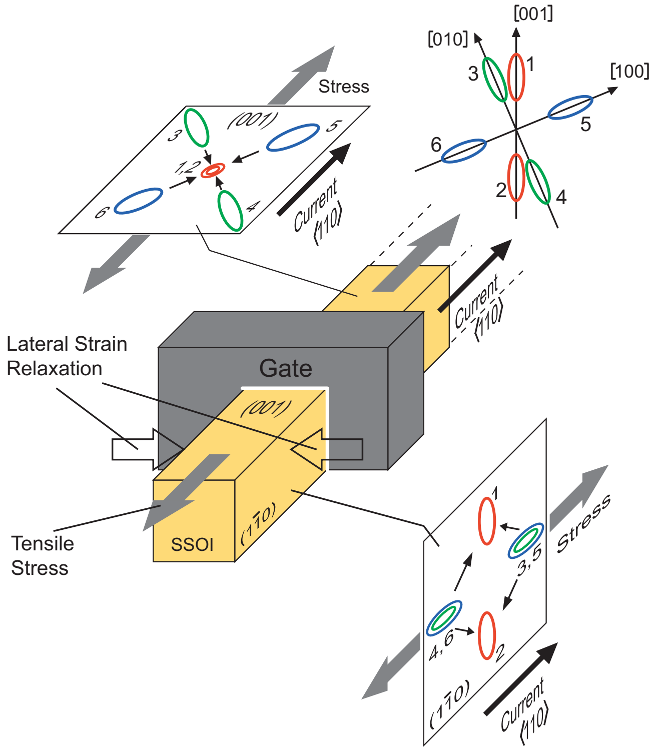


Figure 4.11: Sketch of the fabricated uniaxially strained devices. After lateral strain relaxation, the channel remains strained along the [110]-direction which is also the direction of current flow. The orientation of the six conduction band ellipsoids towards the channel and the projection of the ellipsoids on the (001) and $(1\bar{1}0)$ channel surfaces are shown. Uniaxial tensile strain along [110] energetically favors the occupation of valleys with a low conductivity mass m_t in transport direction on (100) and $(1\bar{1}0)$ surfaces. Additionally, on the (100) surface band non-parabolicity due to strain decreases m_t.

the long sides of the rectangles and boundary conditions were chosen to let these sides move freely while the tensile forces on the short sides of the rectangles were kept constant since the NW is connected at this side to the large source/drain contacts (110). As can be seen in Fig. 4.12(c) the tensile strain in the y-direction along the NW is maintained to a high degree, keeping most of the initial biaxial tensile strain while the lateral strain relaxation proceeds quickly with increasing length to width ratio.

Long channel SSOI devices

Figure 4.13(a) and (b) show the transfer and output characteristic of a SSOI n-FET with $L = 1.5\,\mu$m. The device exhibits, similar to the SOI devices, excellent gate control with a high $I_\mathrm{on}/I_\mathrm{off}$-ratio of 10^7 and a very low I_off-current. The subthreshold slope of $S = 65\,$mV/dec is close to the ideal value

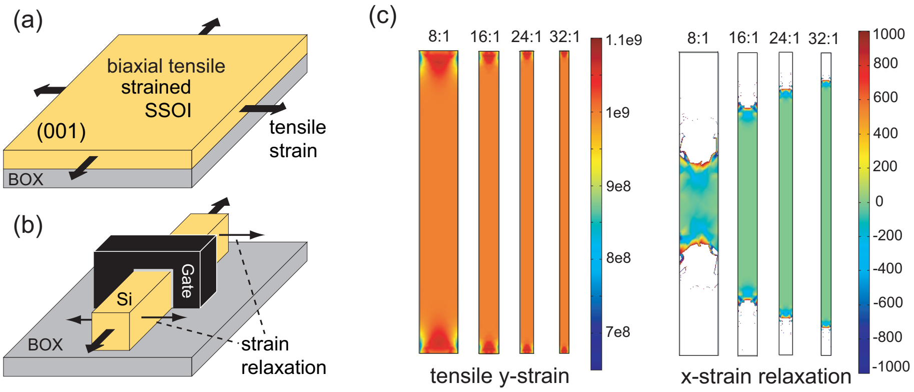


Figure 4.12: (a) 50nm SSOI with 1 GPa biaxial tensile stress is used as starting material. (b) Uniaxial tensile strain is obtained by lateral strain relaxation of patterned structures. (c) 2D finite element simulation of the strain in rectangles of different aspect ratio. Lateral strain relaxation increases with increasing aspect ratio L/W of the structure while the tensile strain along the structure is maintained at a high level.

at room temperature indicating a low defect density at interface between gate oxide and SSOI. The output characteristics of in 4.13(b) features nice saturation. Under the same implantation and activation conditions SSOI devices have smaller source/drain resistances compared to SOI devices of equal geometry, indicating a higher activation of As dopants in SSOI than in SOI.

Comparison between SOI and SSOI NW-nFETs

In the following paragraph uniaxially tensile strained and unstrained long channel NW-nFETs are compared. Fig. 4.14(a) shows the transfer characteristics of a strained and an unstrained NW-nFET. These NWs have the same cross-sections and a length of $L = 3\,\mu$m. Comparing parallel processed SOI and SSOI devices showed that the average subthreshold slope of the SSOI devices was better than that of the SOI devices. This is attributed to an improved SiO_2/Si-interface due to strain. While for devices fabricated on both materials very low I_{off}-currents and high $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratios were measured, the I_{on}-current was strongly enhanced in SSOI devices. In Fig. 4.14(b) a statistical $I_{\mathrm{d,sat}}/I_{\mathrm{off}}$-distribution is shown. The saturation current for each device was taken at an overdrive of $V_{\mathrm{g}} - V_{\mathrm{th}} = 1.2\,$V. Due to uniaxial tensile strain the I_{on}-current is enhanced on the average by a factor of 2.5, while strain does not deteriorate the low I_{off}-current. The inset of Fig. 4.14(b) shows the transconductance of the two NW-FETs with a gate length of $L = 3\,\mu$m. Under the same bias conditions the transconductance of the strained device is ×2.1 larger than for the unstrained device, in good agreement with the

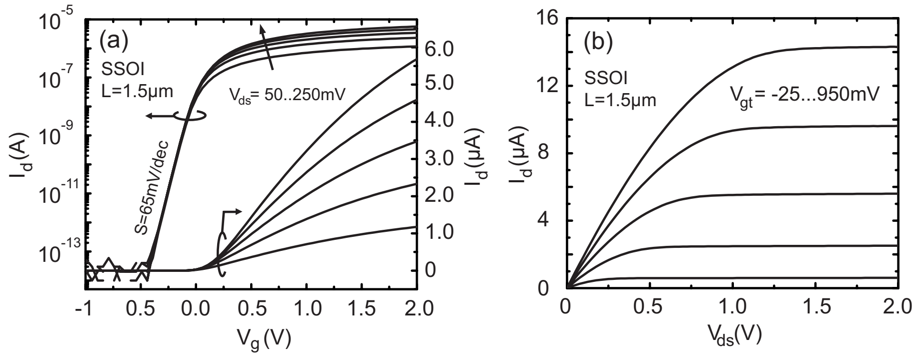


Figure 4.13: Transfer (a) and output characteristics (b) of of a NW n-FET with $L = 1.5\,\mu$m fabricated on SSOI with a biaxial tensile stress of 1 GPa. Due to lateral strain relaxation the NW is uniaxially tensile strained. The channel has a trapezoidal cross-section of $\approx 42 \times 42\,\mathrm{nm}^2$ and a gate oxide of $t_{\mathrm{ox}} = 5\,\mathrm{nm}$. The transfer characteristic has a close to ideal subthreshold slope and the output characteristic shows good saturation.

results of Fig. 4.13.

The influence of strain on electron mobility was investigated with the $I_{\mathrm{d}}/\sqrt{g_{\mathrm{m}}}$-method. The inset of Fig. 4.14(a) shows a plot of $I_{\mathrm{d}}/\sqrt{g_{\mathrm{m}}}$ against V_{g} for a strained and unstrained device measured at a source/drain voltage of $V_{\mathrm{ds}} = 50\,\mathrm{mV}$. The slope $\sqrt{A}$ of the linear part of the curves is related to the carrier mobility by $A = \mu C_{\mathrm{ox}} \frac{W}{L} V_{\mathrm{ds}}$. To extract the carrier mobility from this formula it is necessary to know the gate capacitance C_{ox}. Analytical approximations for the capacitance of multigate devices easily result in values deviating significantly from the actual capacitance and therefore in wrong values for the carrier mobility (111). For devices with equal channel cross-section the mobility enhancement factor x can be extracted from the ratio of the slopes of the $I_{\mathrm{d}}/\sqrt{g_{\mathrm{m}}}$-curves without knowing the capacitance:

$$x = \frac{\mu_{\mathrm{SSOI}}}{\mu_{\mathrm{SOI}}} = \frac{A_{\mathrm{SSOI}}}{A_{\mathrm{SOI}}} \cdot \frac{L_{SSOI}}{L_{SOI}} \tag{4.2}$$

where L_{SSOI} and L_{SOI} are the channel length of the SSOI and SOI device, respectively. For the compared devices the mobility enhancement due to uniaxial tensile strain is found to be $x = 2.3$. This mobility enhancement is consistent with the results reported for similar devices in Ref.(112) and for long channel devices under biaxial tensile strain in Refs. (63) and (91).

4.4.3 SSOI NW-FETs with Triangular Cross-section

NW-FETs with triangular cross-section and gate length of $L = 200, 400, 600, 800\,\mathrm{nm}$ were fabricated on 50 nm biaxial tensile strained SSOI. The channels were aligned along the $< 110 >$-direction. Therefore, current flows on crystal

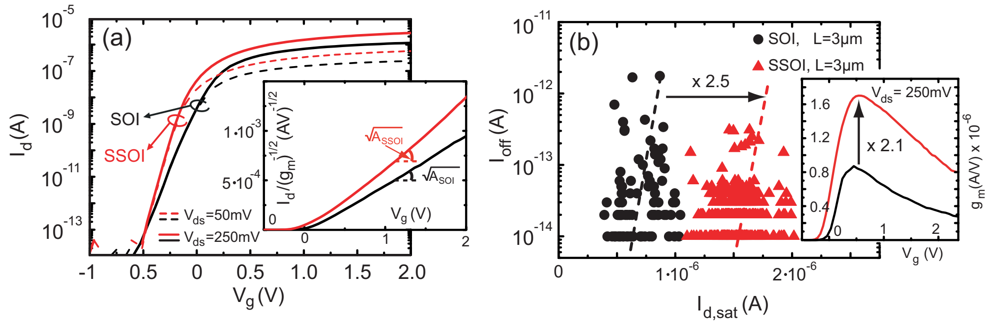


Figure 4.14: (a) Transfer characteristics two NW-FETs, one fabricated on SOI and the other on SSOI. The channel length of both devices is $L = 3\,\mu$m and the gate oxide thickness $t_{\text{ox}} = 5\,$nm. The subthreshold slope of both devices is between $S = 70 - 80\,$mV/dec. Due to uniaxial tensile strain the device fabricated on SSOI has a larger on-current. The inset shows the $I_{\text{d}}/\sqrt{g_{\text{m}}}$-plot for the devices. The slope of the linear region is related to the carrier mobility. An electron mobility enhancement by 2.3 is found for SSOI devices. (b) $I_{\text{d,sat}}/I_{\text{off}}$-plot for SOI and SSOI NW-devices with $L = 3\,\mu$m. Uniaxial tensile strain in SSOI devices results in a ×2.5 improved $I_{\text{d,sat}}$, while no degradation of I_{off} is seen.

planes close to the (111)-planes. The inset of Fig. 4.16(a) shows a top view scanning electron microscopy (SEM) image of a NW with $L = 200\,$nm channel length. A TEM image of the channel cross-section of the same device is shown in the inset of Fig. 4.16(b). Height and width at the interface with the BOX the channel are $H = W \approx 40\,$nm and the gate oxide thickness $t_{\text{ox}} = 5\,$nm. The transfer characteristics feature a close to ideal subthreshold slope of $S = 62\,$mV/dec, a high $I_{\text{on}}/I_{\text{off}}$ ratio of 10^7 at $V_{\text{ds}} = 0.25\,$V, neglectable DIBL and a very low off-current, a result of the excellent electrostatic gate control of the channel in multigate devices (Fig. 4.16(a)).
Comparing the NW-FET with $L = 200\,$nm with a parallel processed device with $L = 800\,$nm the expected increase in I_{on}-current with decreasing channel length was not observed. This is caused by differences in the channel cross-section for the devices with different channel length. After RIE of the NW it was found that shorter NWs were also narrower, resulting in a smaller effective channel width.
A direct comparison of these devices with the NW-FETs presented in the previous section is difficult, too, since the channel cross-sections are different. In the triangular NW-FETs current flows on crystal planes close to (111)-surfaces. These have smaller electron mobility than the (100)-surfaces that form the channel in the trapezoidal NW-FETs.

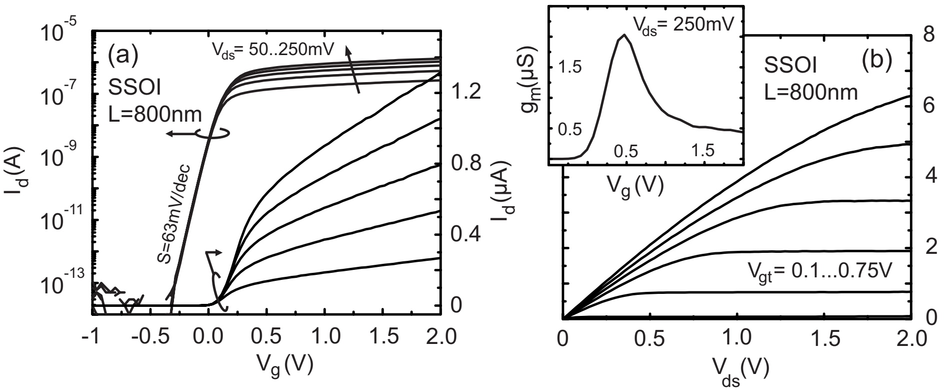


Figure 4.15: (a) Transfer characteristics of a triangular NW-FET with a channel length of $L = 800$nm on a linear and logarithmic scale. (b) Output characteristic of the NW-FET that shows the effect of series resistance. The inset shows the transconductance curve.

4.5 Suspended Nanowires

The highest impunity to short channel effects is obtained when the gate completely surrounds the channel. Therefore in this section first results towards the fabrication of GAA devices are presented. Suspended single NWs and arrays of NWs were fabricated slightly modifying the process described above. After RIE etching of the NWs they were underetched with diluted HF(1%). Fig. 4.17(a) shows a top view SEM image of a parallelepipedic untereched NW fabricated from 30 nm SOI. The transformation into cylindric wires and their diameter reduction was obtained by annealing in dry O_2 atmosphere at a temperature of 800 °C for 2 h. In order to obtain circular wires after oxidation, the NWs must have square cross-section after RIE etching. Due to the good control of the oxidation process, a precise definition of the Si-NW diameter down to a dimension below 15 nm is possible (Fig. 4.17(c)) (113; 114). Therefore, it is not necessary to force the physical lithographical limits in order to obtain thin, high quality nanowires. Moreover, an improvement of the surface quality following the oxidation/etching process was obtained as can be also seen by comparing Fig. 4.17(a) and (b). A mechanically stable array of NWs containing wires with a diameter of 30 nm and a length of 700 nm is presented in Fig. 4.17(c). The wire withstand oxidations at temperatures sufficiently high for growing a thin, high quality gate oxide and hence can be used as building blocks for GAA-MOSFETs. In a first attempt to realize such a device 190 nm SiO_2 were deposited in a LPCDV tool at about 700 °C. Figure 4.18(a)−(c) show cross-section SEM images of NWs with different height-to-width ratios embedded in SiO_2. The deposition of material around the suspended Si-NW is conformal but shows some voids. These voids result

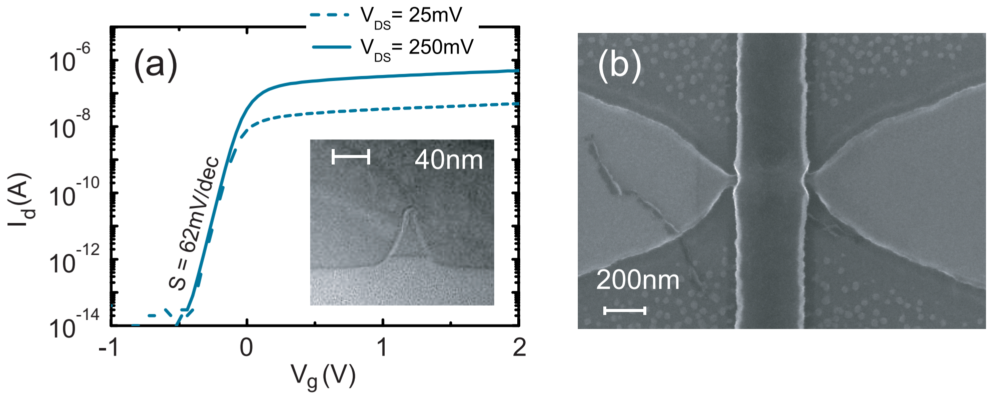


Figure 4.16: (a) Transfer characteristic of a triangular NW-FET with $L = 200\,\mathrm{nm}$ channel length and gate oxide thickness $t_{\mathrm{ox}} = 5\,\mathrm{nm}$. Due to the good gate electrostatic the device has a close to ideal subthreshold slope, high $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, low I_{off} and neglectable DIBL. The inset shows a cross-section SEM image of the device. (b) Top view SEM image of the NW-FET with a channel length of $L = 200\,\mathrm{nm}$.

from material deposition occuring at two surfaces simultaneously: (i) at the surface of the suspended wire and (ii) at the surface of the etch pit. As the gap between wire and substrate closes during deposition voids form. Using a similar LPCVD process using n-doped polysilicon it is possible to deposit a gate around the wire. Whether the voids have an influence on device properties or can be avoided through process optimization has to be the subject of further studies.

4.6 Summary

- **Fabrication Process for Si NW-FETs**
  A process for fabricating Si NW-FETs in a top-down approach has been developed. NW-MOSFETs with trapezoidal and triangular cross-section have been successfully fabricated that show excellent electrical properties.

- **Optimizing Multigate Devices through Choice of Channel Direction and Cross-section** Simultaneous current flow in multigate devices on crystal planes with different orientations opens new possibilities for device optimization due to the anisotropy of Silicon. By choosing channel orientations and cross-sections properly, n- and p-type devices can be greatly improved individually. On the other hand, this technique can also be used to match the performance of n- and p-type devices of equal dimensions, as has been shown in this work.

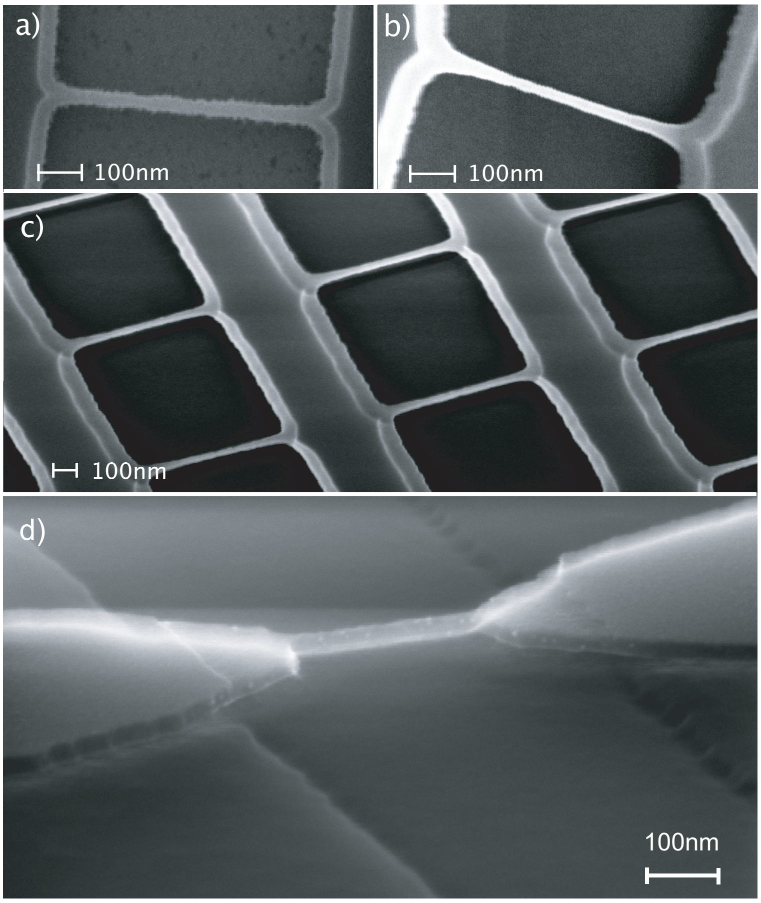


Figure 4.17: SEM images of suspended NWs. (a) 50 nm parallelepipidic suspended NW after RIE and underetching; (b) 30 nm cylindrical NW after oxidation and etching; (c) 30 nm NW array; (d) Selectively underteched < 15 nm NW.

- **Uniaxial Tensile Strained NW n-FETs Fabricated by Lateral Strain Relaxation**
  Size-dependent strain relaxation of nanoscale structures has been employed to fabricate uniaxial tensile strained NW-FETs. The dependence of strain relaxation on the aspect-ratio of the strained structure has been investigate with FEM simulations. Due to the excellent electrostatics in multigate devices, the transistors have very low I_{off}-currents and very high $I_{\text{on}}/I_{\text{off}}$-ratios. Uniaxial tensile strained NW-FETs show an enhanced mobility by a factor of ×2.3, as well as, improved on-currents and transconductances by a factor of ×2.5 and ×2.1, respectively, compared to unstrained devices.

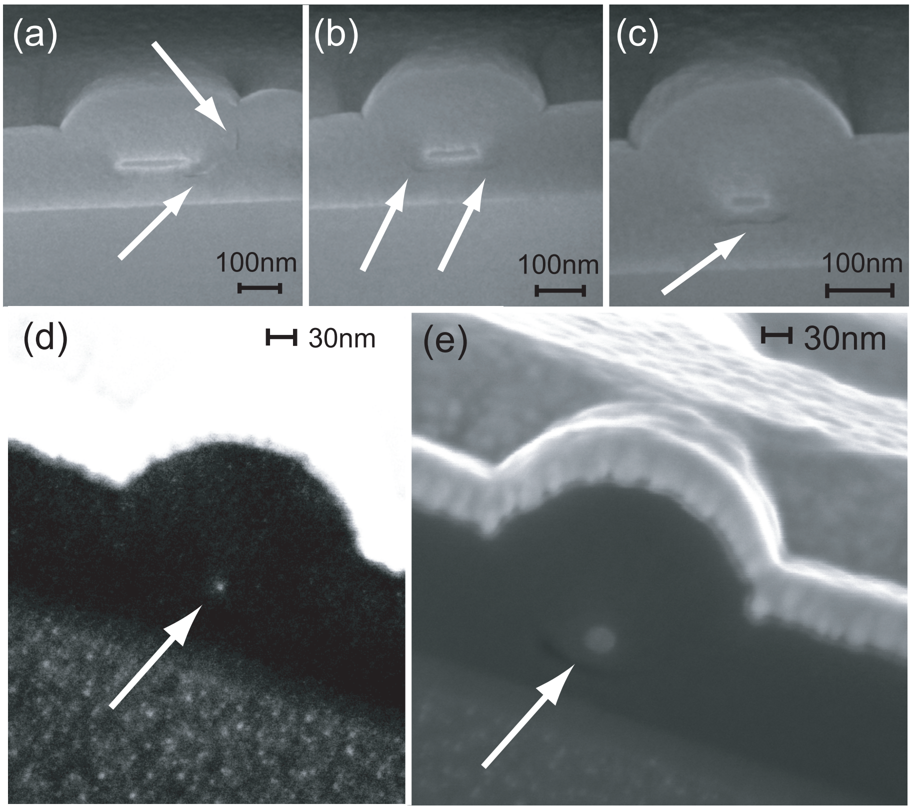


Figure 4.18: (a)−(c) Cross-section SEM images of NWs of different height-to-width ratio buried in SiO_2. The arrows indicate were voids formed during deposition of SiO_2. SEM images (d) and (e) show buried circular NWs with a diameter of (d) < 15 nm, (e) 30 nm.

- **Suspended Nanowires**
  Suspended circular NWs down to diameters < 15 nm have been successfully fabricated. It has been shown that suspended NWs withstand high enough oxidation temperatures for the growth of high quality gate-oxides. Furthermore, the change of cross-section of suspended NWs by oxidation has been investigated and a significantly smoother surface of NWs after oxidation were observed. The conformal deposition of material in a LPCVD reactor around the Si-NW has been shown. With this fabrication method gate-all-around NW-MOSFETs can be fabricated.

Chapter 5

Summary

In this thesis four important physical and material aspects faced by MOSFET devices as dimensions move to the length scale of 10 nm have been investigated:

i) metal source/drain contacts with dopant segregation for reduced contact resistance and improved carrier injection;

ii) variability of the Schottky-barrier height in MOSFET contacts;

iii) strained silicon as a high mobility channel material;

iv) silicon nanowire MOSFETs in order to suppress short channel effects by a multi-gate architecture.

Ultimately scaled devices require highly conductive contacts with abrupt junctions. However, due to Fermi-level pinning at the metal-semicondcutor interface, the performance of SB-MOSFETs still falls behind that of conventional FETs. Nickel-silicidation induced dopant segregation is highly effective in improving carrier injection through Schottky-barriers, resulting in higher $I_{\text{on}}/I_{\text{off}}$ -ratios and better subthreshold swings. Arsenic dopant segregation has been studied in detail as a function of NiSi thickness, implantation energy and dose, as well as process conditions for the formation of NiSi. It was experimentally shown that dopant concentrations as high as the solid solubility limit of arsenic in Si and lateral dopant slopes of $1-2$ nm/dec at the NiSi/Si-contact interface can be obtained. Device-simulations of ultimately scaled ultrathin-body SOI MOSFETs with dopant segregation demonstrated that devices with dopant segregation can be scaled down to channel lengths of $L = 10$ nm.

Variability has important effects on the electrical properties of nanoscale devices. The variability of the Schottky-barrier height (SBH) in SB-MOSFETs without and with dopant segregation has therefore been investigated. A new experimental method has been developed, to measure the variability of the SBH in SB-MOSFETs and to quantify the impact of various sources leading to variability in the electrical characteristics. Employing this method, the inherent variability of the SBH has been identified as the main source of variability and an increase in SBH variability due to dopant segregation by 0.01 eV was measured. With simulations of ultimately scaled devices, the importance of SBH variability for the on-current of devices, even for very low SBHs of 0.03 eV, was demonstrated.

High mobility channel materials are required, as the steady increase of carrier velocity with gate-length scaling reaches its limits. The intrinsic transport properties of Si can be substantially improved by strain. Several aspects of the fabrication of biaxial tensile strained SSOI substrates by strain transfer between a thin SiGe buffer and a Si cap layer have been investigated. Optimizing the growth process conditions by epitaxial overgrowth of a strain adjusted SiGe layer on top of the relaxed buffer, the threading dislocation density in strained Si was reduced to $1 \times 10^{6}\,\mathrm{cm}^{-2}$.

A new method for the fabrication of thin SiGe/Si-heterostructure lines featuring highly asymmetric strain was developed. Asymmetric strain relaxation relies on the limitation of the path length of threading dislocations by the stripe boundaries in thin SiGe/Si lines, leading to an asymmetrical dislocation network. Substantially decreased resistivities for electrons and holes in these lines, calculated with piezoelectricity theory, show that they are promising for strained heterostructure devices.

The electrical properties of biaxial tensile strained (001) SSOI with a stress of 1.2 GPa have been studied using Hall-bar MOSFETs. N- and p-type SSOI devices showed improved on-currents and transconductances by factors of ×1.7 and ×1.2, respectively, over unstrained parallel processed devices. The mobility in n-type FETS on SSOI, measured by split C-V, showed a peak value of $1250\,\mathrm{cm}^2/\mathrm{Vs}$ at low vertical electric field and an enhancement by a factor of ×1.7 in comparison to unstrained Si.

The impact of biaxial strain on electron affinity was determined by measuring threshold voltage shifts between strained and unstrained devices of $\Delta V_{\mathrm{th,n}} = 190\,\mathrm{mV}$ in the case of n-type and $\Delta V_{\mathrm{th,p}} = -80\,\mathrm{mV}$ in the case of p-type FETs.

The effective electron mass as a function of carrier density in biaxial tensile strained SSOI was determined from Shubnikov-de Haas oscillations in the longitudinal resistance in the temperature range of $T = 0.4 - 10\,\mathrm{K}$ and for magnetic fields values of $B = 0 - 10\,\mathrm{T}$. No change in the in-plane effective electron mass compared to unstrained SOI was observed while the dependence of the electron mass showed a similar increase from $m_{\mathrm{eff}} = 0.2m_0$

to $m_{\text{eff}} = 0.24m_0$ at low carrier densities in SSOI as for unstrained silicon. This proves that biaxial tensile stress of 1.2 GPa does not warp the in-plane constant energy surfaces of the Si conduction band, in accordance with band structure calculations. The mobility increase in biaxial tensile strained SSOI is, therefore, caused by the occupation of the Δ_2-valleys with low effective electron mass m_{t} in transport direction and reduced scattering due to a smaller k-space volume.

To avoid short channel effects in ultimately scaled FETs multi-gate geometries have to used. A fully CMOS compatible fabrication process for Si nanowire transistors has been developed and devices with trapezoidal cross-sections of about $40 \times 40\,\text{nm}^2$, featuring excellent electrical characteristics, were fabricated. Subthreshold slopes of $S = 65\,\text{mV/dec}$, large $I_{\text{on}}/I_{\text{off}}$-ratios of 10^7 and extremely low I_{off} -currents of $10^{-13}\,\text{A}$ were obtained.

Current flow on different crystal planes in multi-gate devices has been used to take advantage of the anisotropy of conductivity in Si in order to match the on-currents of n- and p-type MOSFETs with the same dimensions.

Improved electron mobility due to strain and excellent electrostatics due to a multi-gate architecture were combined in a uniaxial tensile strained NW-FET. Size-dependent lateral strain relaxation of nanostructures was used to transform biaxial tensile strain into uniaxial tensile strain along the NW. Uniaxial tensile strained NW n-FETs show a factor ×2.3 enhanced mobility and improvements in on-current and transconductance by a factor of ×2.5 and ×2.1, respectively.

Finally, circular suspended NWs with diameters down to $< 15\,\text{nm}$ were fabricated and the possiblity to integrate them into gate-all-around devices has been demonstrated.

Appendix A

Abbreviations

AFM	**a**tomic **f**orce **m**icroscopy
BEEM	**b**allistic **e**lectron **e**mission **m**icroscopy
BOX	**b**uried **ox**ide
C-V	**c**apacitive-**v**oltage
CMOS	**c**omplementary **m**etal **o**xide **s**emiconductor
CVD	**c**hemical **v**apor **d**eposition
E-beam	**e**lectron-beam
EPD	**e**tch **p**it **d**ensity
FET	**f**ield **e**ffect **t**ransistor
FFT	**F**ast **F**ourier **T**ransform
GAA	**g**ate **a**ll **a**round
HF	**h**ydro**fl**ouric acid
HH	**h**eavy **h**ole
HSQ	**h**ydrogen **s**iles**q**uioxane
I-V	**c**urrent-**v**oltage
ICP	**i**nductively **c**oupled **p**lasma
IVC	**i**nner **v**acuum **c**hamber

LH.................**l**ight **h**ole

LPCVD.........**l**ow **p**reassure **c**hemical **v**apor **d**eposition

MD.................**m**isfit **d**islocation

MOSFET......**m**etal **o**xide **s**emiconductor **f**ield **e**ffect **t**ransistor

NiSi................**Ni**ckel **si**licide

NW................**n**ano**w**ire

OVC..............**o**uter **v**acuum **c**hamber

PECVD........**p**lasma **e**nhanced **c**hemical **v**apor deposition

PtSi...............**p**la**t**inum **si**licide

PVTEM.......**p**lan **v**iew **t**ransmission **e**lectron **m**icroscopy

RBS..............**R**utherford **b**ackscattering **s**pectroscopy

RIE...............**r**eactive **i**on **e**tching

rms...............**r**oute **m**ean **s**quare

RPCVD.......**r**educed **p**resure **c**hemical **v**apor **d**eposition

RTA..............**r**apid **t**hermal **a**nnealing

RTO..............**r**apid **t**hermal **o**xidation

RTP..............**r**apid **t**hermal **p**rocessing

SB.................**S**chottky **b**arrier

SBH..............**S**chottky **b**arrier **h**eight

SCE...............**S**hort **c**hannel **e**ffects

SdH...............**S**hubnikov-**d**e **H**aas

SEM..............**s**canning **e**lectron **m**icroscopy

SF.................**s**tacking **f**ault

SIMS............**s**econdary **i**on **m**ass **s**pectroscopy

SO.................**s**pin **o**rbit

SOI...............**s**ilicon **o**n **i**nsulator

SSOI..............**s**trained **s**ilicon **o**n **i**nsulator

SST................**s**idewall **s**pacer **t**echnology

TEM..............**t**ransmission **e**lectron **m**icroscopy

TD.................**t**hreading **d**islocation

XRR..............**x**-**r**ay **r**eflectivity

XTEM..........**b**right **f**ield **t**ransmission **e**lectron **m**icroscopy

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