The Impact of Technology Scaling on Integrated Analogue CMOS RF Front-Ends for Wireless Applications

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines Doktors
der Ingenieurwissenschaften genehmigte Dissertation

vorgelegt von

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Tag der mündlichen Prüfung: 19.09.2008

Seamos realistas, exijamos lo impossible.[1]

Beware the narrow corridors of the mind![2]

Just because you're paranoid doesn't mean they aren't after you.[3]

[1] Commandante Ernesto Guevara de la Serna
[2] Sirtech 1990 in Wizardry IV
[3] Curt Cobain

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1. Introduction

In the past 50 years there has not been any event or phenomenon that affected nearly as many people as the cultural changes related to public mobile wireless communication all around the globe. During the last decade we have witnessed the emergence of a massive market for public mobile communications (cf. Fig. 1.1). Back in 1992 less than 1% of people globally have been in possesion of a mobile phone. By the end of 2005 2.2 billion people - about one third of the earth population - communicated with mobile phones [30], [46]. Nokia as the world market leader for cell phones expects that by 2008 there will be more than 3 billion mobile subscribers [30]. The authors of [56] speak of 3.5 billion subscribers in 2010. These expectations even surpass earlier market analyses of 2.5 billion mobile subscribers for 2009 [4].

At the end of the nineties the market has been dominated by consumers in the western world entering the age of mobile communications by buying their first GSM cellular phone. When the licenses for UMTS were auctioned in Germany in Spring 2000 the optimism was that big that mobile service providers paid close to 50 billion Euros to obtain them. But the ambitious expectation did not meet the economic reality. The customers did not embrace the new features of the new third generation of mobile communications (3G) as eagerly as they had welcomed those of the second generation (2G) [24].

In October 2006 about 2.5 billion cell phones were in use world-wide. In December 2005 47 million UMTS users were reported world-wide. Almost 50% of these users were located in Japan (cf. Fig. 1.2) [24]. Even though the number of UMTS-ready phones is small compared to the number of GSM/GPRS-phones the expectations for the future are great. It is expected that in

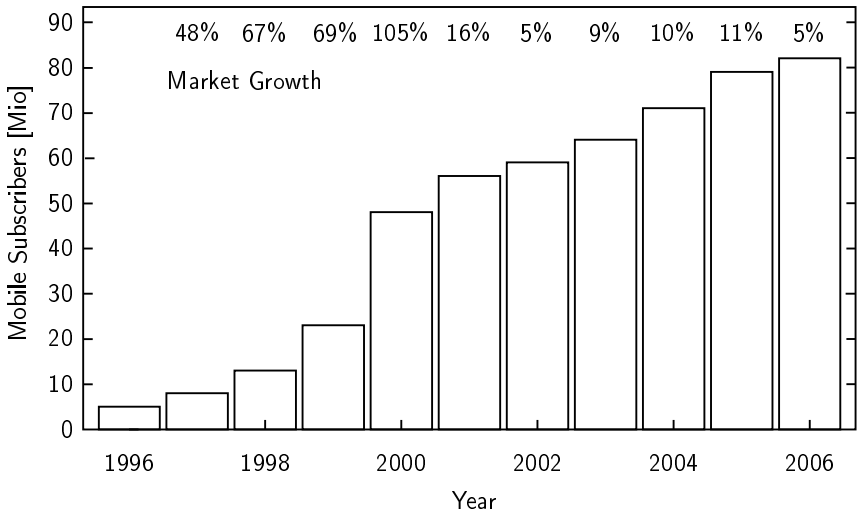


Figure 1.1.: Reported numbers of mobile communication subscribers in Germany in the last decade according to an analysis published in 2006. The total population in Germany is about 82 Million people [5].

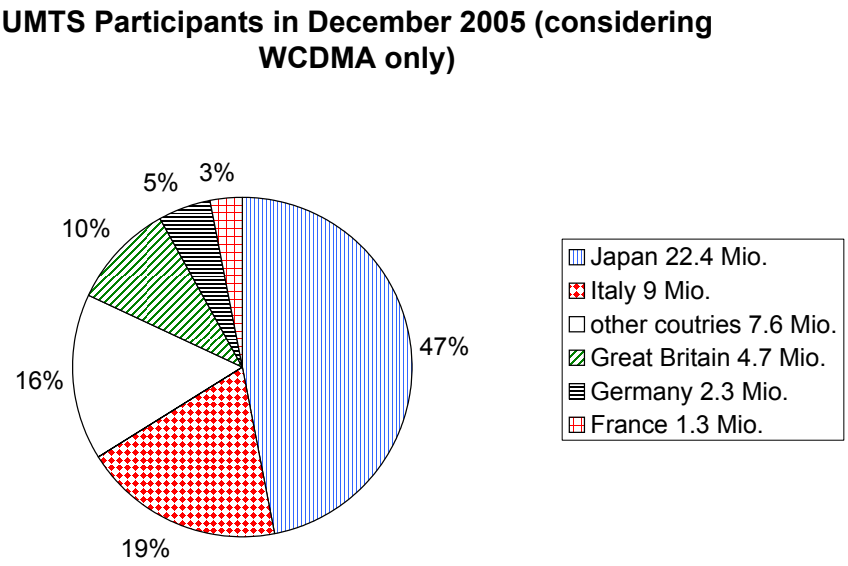


Figure 1.2.: Reported numbers of UMTS participants world-wide in 2005 according to an analysis published in February 2006. The total number reported is about 47.3 million participants [6].

Western Europe 60 % of the mobile phones in use will be UMTS-phones by 2010 [24]. This notion is supported by the trend of western consumers to exchange their mobile phones for fancier ones at least every 18 months [32], [54].

In 2005 the total number of mobile handsets that have been sold is roughly about 800 million units [30], [9]. This is an increase of about 30 % compared to the world-wide sales volume achieved in 2004. While 164 million units have been sold in Western Europe, 204 million units have been sold in Asia/Pacific Region [54]. Nokia even claims that about 980 million cell phones were sold globally in 2006 [42]. Analyses of the market situation agree that emerging markets and developing countries are the engines for the growth of the market [42], [9], [54] and [4]. 80 % of the new mobile subscribers predicted for 2006 have been expected to come from emerging markets [30]. China, India and countries in South America like Brasil or even in Africa are considered the booming markets of the near future. For 2009 sales volumes up to one billion new cell phones are within expectations [53]. It is worth noting that in developing countries the infrastructure for hard-wired communication will be neglected in favour of a mobile communication infrastructure [30].

In the short term or even mid term the market will certainly be dominated by 2G or 2.5G voice-only-phones and affordable entry level phones instead of feature phones in these emerging markets [56]. Hardware for mobile communication via the GSM/GPRS standard will stay the integral part of mobile handsets sold in the years to come (cf. Fig. 1.3). As pointed out before even in developed countries cell phones will continue to offer GSM/GPRS coverage for reasons of customer acceptance and downward compatibility.

Due to the intense competition on the market for entry level phones the key to profitable business are low-cost solutions.

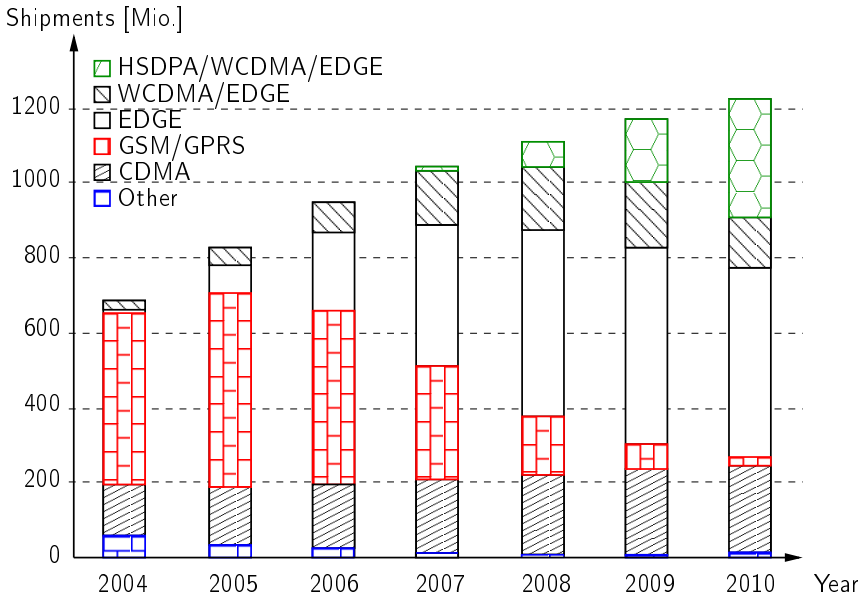


Figure 1.3.: Mobile phone shipments by air interface reported and predicted by the authors of [56].

1.1. Motivation

When we look 15 years back to the past and note the great advancements in mobile communication we have to ask how it has been possible that all of this came true in such a short period of time. The answer is that these achievements in the mobile communication sector are directly linked to the progress made in the integration of radio frequency (RF) circuits, both for economic as well as technical reasons.
On the economic side the down-scaling of integrated CMOS circuitry laid the basis for affordable mass production of integrated chips for the mass market. The semiconductor of choice for the integration of CMOS technology is silicon. The enormous success of silicon is largely credited to its inherent characteristic of building its own passivation: Silicon dioxide (SiO_2). III-V semiconductors are still reserved to niche markets.
On the technical side integrated circuit design raised the boundaries of frequency limitations. With the scaling to the sub-micron region the most prominent characteristic of a CMOS process technology beside its minimum feature size l the transit frequency f_T is severely enlarged. On a PCB with discrete components and devices the parasitic effects, parasitic capacitances and parasitic inductances e.g. of the pins and connectors prevent applications from exceeding the range of a few Gigahertz. Besides, because of their compactness integrated circuits are less sensitive to electrical and magnetic disturbances from the surrounding environment.
Upcoming technology generations typically have to pass through a three-step evolution: The first field of utilisation is in memory applications. In a second step the process generation is taken-up for the implementation of micro-processors. The adoption for analogue RF circuit design is last in line. What the first two steps have in common is that they both target digital applications. With their roots in the digital domain, process technologies tend to be optimised for digital applications. In detail this means that the substrate is rather lossy with a high conductance in order to help the fast travelling of signals across the lines [41] and to prevent latch-up effects.

The analogue designer prefers a high ohmic substrate for e.g. lossless coils with a high quality factor Q.
With an ever increasing packing density of digital transistors it is more and more important to reduce losses and electrical power consumption in order to prevent the thermal breakdown of the circuit. Driven by the desire to reduce losses related to leakage current of switched-off transistors digital integration favours high threshold voltages V_{TH} of the transistors. The classic analogue design on the contrary needs a high overdrive voltage $V_{OV} = V_{GS} - V_{TH}$ to uphold device linearity and operation in the saturation region. Safe operation in the saturation region at a given supply voltage is easier to guarantee with low threshold voltages. Furthermore, a lower supply voltage is necessary to prevent the oxide breakdown of the thin film gate oxide of the transistors. This also tampers with the device linearity analogue designers so desperately aim at. Many of the conventional building blocks of analogue circuit design like cascode stages or improved current mirror topologies rely on sufficient voltage headroom for stacking multiple transistors. This headroom is taken away with the down-scaling of modern process technologies and the associated lower supply voltages.
While digital signals are considered robust to a certain ohmic resistance along the signal path and the amount of current flowing is rather limited, analogue signals are much more sensitive or carry a decent amount of current. As a consequence analogue designs will use an increased width of the signal lines to compensate for thinner metal layers. But along with the width of the signal lines the parasitic coupling increases.

However heavy the burden of the digital heritage is on the analogue circuit performance, for cost effectiveness reasons standard CMOS process technologies dominate the integrated mass production today and will surely dominate the market in the next decade. Analogue enhancement options like extra or thicker metal layers usually are available but extra costs are charged for them.

Aside from the purely process technology related challenges of modern RF CMOS design, the competition on the chip market imposes further challenges on the circuit design.
The general trend in RF architectures is to move the digital signal processing as close to the antenna as possible, replacing analogue signal processing. The reason for this conceptional change is that digital blocks scale with the minimum feature size of the process technology while analogue blocks do not. With the consumed chip area dominating the manufacturing costs in mass production these costs are minimised. While gaining the additional benefit of increased flexibility in signal processing in the digital domain, the performance requirements for the remaining analogue blocks increase.
The degradation of analogue circuit performance due to intensified coupling from the digital signals is a secondary effect of integrating digital signal processing on the same die with analogue circuitry [2]. This is the main drawback of so called System on Chips (SoC). Nevertheless, SoC designs recently have become a popular research topic [52], [36] as they are attractive from the economic point of view. Further steps in order to cut the costs, in order to reduce the Bill of Material (BOM) are to integrate or avoid external matching components or even to integrate power amplifiers in CMOS process technologies [20].
When it comes to mobile device engineering as it is in the focus of this work the power consumption of a chip is also an important benchmark for the chip evaluation. Battery powered devices are expected to provide a reasonable operating and stand-by time before they need to be recharged. The demand for low-power systems further restricts the analogue circuit design.

For the years to come mastering the manifold obstacles of integrated analogue circuit design will present a challenging task for developing engineers in the field as well as research laboratories. This short introduction points out economical considerations, physical device limitations and electrical perturbations that influence modern chip design challenges to name but a few. It is the broad portfolio of obstructions that makes integrated analogue circuit design such an interesting and demanding research topic.

1.2. Formulation of the Task

A GSM receiver front-end, especially the LNAs, is to be implemented in a contemporary standard 65 nm CMOS technology. The developed receiver front-end has to be suitable for integration in an SoC transceiver low-cost solution.The receiver front-end to be generated is based on a GSM receiver front-end already available in a 130 nm standard CMOS technology. The receiver front-end serves as an example for the evolution analogue circuit topologies have to undergo with respect to the manifold effects associated with the down-scaling CMOS process technologies in order to uphold functionality, performance and reliability.
This work will investigate a GSM receiver front-end and evaluate its perspective to be used for upcoming CMOS process technologies. The approach to adopt or simply downscale proven state-of-the-art circuit topologies is attractive in the short term. The re-use of conventional concepts bears the advantage of avoiding the economical risks associated with new, innovative concepts. Nevertheless these conventional concepts for circuits or whole communication systems might turn out to be inoperative and infeasible in the nano-scale region.
In a time where the economic situation leaves competitors on the chip market ever shorter time to market, making the decision either to adopt old designs to the new basic conditions of shrinks in CMOS technology or to replace conventional designs and concepts altogether becomes a most vital strategic decision.

1.3. Structure of this Work

The outline of this work is as follows:

- Chapter 2 introduces performance metrics useful for wireless receiver front-ends in order to quantify the performance of employed analogue circuits blocks. In addition the advantages and disadvantages of font-end block implementations found in contemporary literature are presented.

- Chapter 3 analyses the test scenarios defined by the official 3GPP GSM specification and derives the appropriate block specifications for a GSM receiver front-end. Furthermore, it is explained why a direct-conversion receiver architecture is considered the appropriate choice for an integrated low-cost implementation of a GSM receiver. Moreover a system link budget for the receiver front-end is set-up.

- Chapter 4 illustrates the implementations of basic devices in standard CMOS technologies with special focus on field effect transistors as the most prominent devices of CMOS technologies. Here device equations for the classical long-channel model as well as device equations for the short-channel model are discussed. Besides, the analogue performance of transistor unit cells in a 130 nm CMOS technology is compared in detail to the performance of transistor unit cells in a 65 nm process technology.

- Chapter 5 elaborates on the LNAs implemented in the 65 nm CMOS technology. The performance of the LNAs is evaluated by pre-layout, post-layout and statistical simulation results. Later on the performance of the complete receiver front-end, including quadrature mixer and baseband filter stages, is evaluated by simulation and compared to the measurement results of an actual demonstrator testchip.

- Chapter 6 first lists the physical limitations of conventional CMOS device shrinks and presents promising approaches with a potential to overcome these limitations. Secondly the economical potential of future CMOS technology shrinks is investigated.

- Chapter 7 concludes this thesis with a brief summary of the work that has been done.

2. Characteristics of Analogue Circuits and Receiver Front-End Building Blocks

Before we can discuss the advantages or disadvantages of different circuit topologies in detail we need to agree on a set of characteristics in order to quantify performance and/or compare different circuits. Following the summary of relevant criteria for the circuits presented in this work this section elaborates on state of the art circuits as they are found in literature. The chapter is concluded by a review of configuration and calibration techniques that ease the challenges of integrated analogue circuit implementations designed for low-cost mass production.

2.1. Gain

The gain of a circuit block is the increase of signal level at the output (V_{OUT}, P_{OUT}) compared to the input (V_{IN}, P_{IN}). We can define the gain in the voltage domain (voltage gain g_V) or in the power domain (power gain g_P)

$$g_V = \frac{V_{OUT}}{V_{IN}} \text{ or } g_P = \frac{P_{OUT}}{P_{IN}}. \tag{2.1}$$

For convenience during calculations it can be useful to transfer gain from the linear into the logarithmic domain

$$G_V = 20\log(g_V) \text{ or } G_P = 10\log(g_P). \tag{2.2}$$

The voltage gain g_V and power gain g_P can be related by

$$g_P = g_V^2 \frac{Z_{IN}}{Z_{LOAD}}. \tag{2.3}$$

The impedances Z_{IN} and Z_{LOAD} denote reference impedances. The input impedance Z_{IN} and the load impedance Z_{LOAD} must be known in order to calculate the power gain. As these quantities are hard to obtain or define for integrated circuits like the cascaded blocks of a receive chain, it is common practice to work with voltage gains for integrated circuits.
The gain of a mixer circuit is a special case. The gain of a mixer is referred to as conversion gain $g_{V,CONV}$ respectively $G_{V,CONV}$ because input and (wanted) output signal do not occur at the same frequency as it is the purpose of a mixer block to shift frequency spectra. As the input impedance and the output impedance of a mixer are not well defined in an integrated receiver it is common practice to characterise a mixer by giving its voltage gain and not its power gain.
For other particular circuits it can make sense to define a current gain as the ratio of the output to input current or to define a transimpedance as the ratio of the output voltage to input current.

2.2. Noise

2.2.1. Noise Factor and Noise Figure

The noise factor F is a measure for the noise contribution of a circuit block. Consequently the noise factor is defined as the degradation of the signal to noise ratio (SNR) from input to output of a circuit.

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \tag{2.4}$$

The noise figure NF is the logarithmic measure of the linear noise factor F.

$$NF = 10\log(F) \tag{2.5}$$

For physical reasons the SNR_{IN} is always superior to the SNR_{OUT} in (2.4) and thus F is always larger than unity, respectively NF is always larger than 0 dB.
Another popular definition of F is

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}}. \tag{2.6}$$

It can be shown that (2.4) and (2.6) are equivalent definitions [47].
Similar to the gain definition of a mixer circuit, the noise figure of a mixer circuit is a special case. A mixer circuit for a low-IF receiver is characterised by the single sideband (SSB) noise figure:

$$SSB - NF = 10\log(\frac{S_{RF}/N_{RF+IM}}{(S/N)_{IF}}) \tag{2.7}$$

with

S_{RF}	Signal power at the RF
N_{RF+IM}	Noise power contributions from the RF and the image (IM) frequency
$(S/N)_{IF}$	Signal to noise ratio at the intermediate frequency (IF).

A mixer circuit for a direct-conversion receiver is characterised by the double sideband (DSB) noise figure:

$$DSB - NF = 10\log(\frac{S_{RF+IM}/N_{RF+IM}}{(S/N)_{IF}}) \tag{2.8}$$

with

S_{RF+IM}	Signal power contribution at the RF and the IM frequency.

The difference between both definitions is which signal and noise contributions are taken into account. If the IF is non-zero (e.g. in a low-IF receiver) not only the wanted RF component but also a spectral contribution (noise) from the image band (IM) is down-converted to IF (cf. Section 3.3.1). If IF is zero (e.g. in a direct-conversion receiver) the image band is identical to the wanted band. Assuming that the transfer characteristic of a mixer in a low-IF receiver is symmetrical around the frequency of the LO signal, the noise contribution from the IM band to the IF signal is the same as from the wanted band to the IF signal, the $SSB - NF$ is 3 dB larger than the $DSB - NF$. Another consequence of both definitions is that the minimum $DSB - NF$

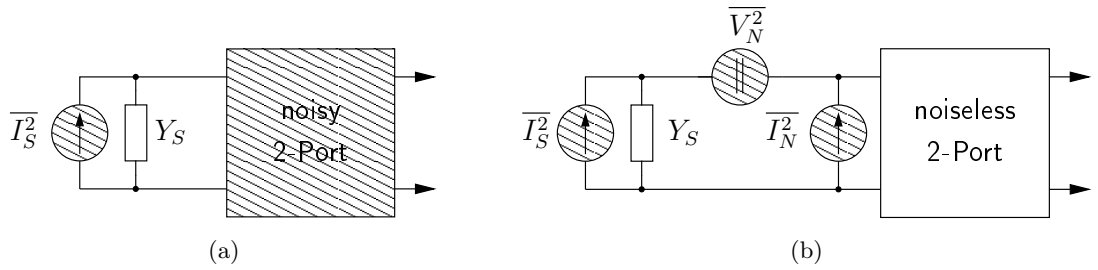


Figure 2.1.: a) Noisy two-port with a noisy signal source. b) Noiseless two-port with equivalent noise sources at the input and a noisy signal source.

for a noiseless mixer circuit is $DSB - NF_{MIN} = 0\,\text{dB}$ whereas the minimum $SSB - NF$ is $SSB - NF_{MIN} = 3\,\text{dB}$.

2.2.2. Noise Factor of Cascaded Stages

In Section 3.4.1 we want to calculate the noise factor not only for a single circuit block but for a complete analogue receiver front-end. The total noise factor F_{tot} of m cascaded stages is approximated by Friis Formula [17]:

$$F_{tot} = 1 + (F_1 - 1) + \frac{F_2 - 1}{g_{P1}} + \ldots + \frac{F_m - 1}{g_{P1} \cdots g_{P(m-1)}}, \tag{2.9}$$

with

F_i	Noise factor of stage i
g_{Pi}	Available power gain of stage i

The first block in the chain dominates the overall noise factor as its contribution is not scaled down by the gain of the previous stages.

2.2.3. Classic Two-Port Noise Theory

In two-port noise theory we replace a noisy two-port (Fig. 2.1(a)) with a noiseless one and equivalent input or output noise sources (Fig. 2.1(b)). In order to represent the (potentially frequency dependent) noise behaviour of a linear two-port correctly, we need to find two independent equivalent input noise sources. In order to determine the quantitative values for the equivalent noise voltage source $\overline{V_N^2}$ and the equivalent noise current source $\overline{I_N^2}$ we exploit the underlying idea that the noise generated e.g. at the output of the two-port must be identical no matter whether we look at the noisy two-port or the noiseless two-port with the equivalent noise sources at the input. This has to be especially true for a short circuit or open clamps at the input port. The advantage of these extreme test cases is that they render either the equivalent voltage source (open clamps) or the equivalent current source (short circuit) useless and allow for easy computation.
Following the definition of F in (2.6) we find that

$$F = \frac{\overline{I_S^2} + \overline{|I_N + Y_S V_N|^2}}{\overline{I_S^2}} \tag{2.10}$$

with

Y_S Input conductance of the input signal source.

In (2.10) the underlying assumption is that the noise powers of the signal source and the circuit block of interest are uncorrelated. Equation (2.10) does not require that the noise sources in the circuit are uncorrelated. In general V_N and I_N are correlated. That is why we split I_N into a part I_C correlated with V_N and a part I_U that is uncorrelated with V_N:

$$I_N = I_C + I_U. \tag{2.11}$$

I_C can be put into relation to V_N by the use of a proportionality constant Y_C

$$I_C = Y_C V_N, \tag{2.12}$$

where $Y_C = G_C + jB_C$ is a fictional admittance purely used for computation that lacks its counterpart in the actual circuit block. Inserting (2.11) and (2.12) in (2.10) we obtain

$$F = 1 + \frac{\overline{I_U^2} + |Y_C + Y_S|^2 \overline{V_N^2}}{I_S^2} \tag{2.13}$$

for the total noise factor of a noiseless two-port with equivalent input noise sources (cf. Fig. 2.1).

2.3. Input Matching

There are basically two kinds of input matching for electrical circuits: 'Power Matching' and 'Noise Matching'. It will be shown in this section that in general both types of matching are not identical. In consequence a circuit block e.g. an LNA that is power-matched to an input source does not necessarily exhibit its best possible noise behaviour.

2.3.1. Power Matching

As the name suggests power matching is optimised for a maximum power transfer from an input source into an electrical circuit. For a given complex source impedance $Z_S = R_S + jX_S$ an input impedance

$$Z_{IN} = R_S - jX_S = Z_S^* \tag{2.14}$$

satisfies the requirements for a maximum power transfer into a circuit. Even with the power matching criteria perfectly satisfied, the load circuit can only draw one fourth of the power dissipated by a source with a non-zero source impedance. At the input connector of a wireless receiver it is vital to absorb as much of the incoming signal power as possible. The available signal power at the antenna connector can be as low as e.g. $P_{IN} = -99\,\mathrm{dBm}$ for GSM.
Power matching is common practice in measurement laboratories. For RF applications $R_S = 50\,\Omega$ and $X_S = 0$ is the most common standard value.
The input return loss S_{11} is a quantitative measure for the level of input power matching to a given source impedance. The S_{11} of a circuit describes the ratio of the reflected to the incident power wave. The exact definition of S_{11} requires that the circuit of interest is to be terminated with a perfect power matched load. When simulating an LNA that is loaded with the mostly

capacitive input impedance of a mixer circuit the output matching constraint is violated. However, it is common practice to use S_{11} as a quantitative measure for the degree of input power matching. If the backward isolation of the LNA circuit is sufficient the inaccuracy in doing so is considered to be negligible. For details on scattering parameters and their derivation refer to advanced RF literature like [18].

2.3.2. Noise Matching

Noise matching is optimised for minimum noise performance of a circuit. In contrast to power matching which requires a certain input impedance from a circuit block, noise matching determines the source impedance of a signal source for optimum noise performance.
In (2.13) we can replace the three independent noise sources by resistances (2.15) or conductances (2.16), (2.17) of equivalent thermal noise sources [35]:

$$R_N \equiv \frac{\overline{V_N^2}}{4kT\Delta f} \tag{2.15}$$

$$G_U \equiv \frac{\overline{I_U^2}}{4kT\Delta f} \tag{2.16}$$

$$G_S \equiv \frac{\overline{I_S^2}}{4kT\Delta f}. \tag{2.17}$$

Doing so, (2.13) turns into

$$F = 1 + \frac{G_U + |Y_S + Y_C|^2 R_N}{G_S} \tag{2.18}$$

$$= 1 + \frac{G_U + \left[(G_S + G_C)^2 + (B_S + B_C)^2\right] R_N}{G_S}. \tag{2.19}$$

While R_N and G_U are fictional quantities, G_S is the real part of the signal source impedance $Y_S = G_S + jB_S$. Now it is possible to derive the noise factor with respect to the signal source admittance Y_S and set it to zero:

$$\frac{\partial F}{\partial Y_S} = 0 \quad \Rightarrow \quad G_{OPT} = \sqrt{\frac{G_U}{R_N} + G_C^2} \text{ and } B_{OPT} = -B_C \tag{2.20}$$

$$\text{respectively} \qquad G_{OPT} = \sqrt{\frac{\overline{I_N^2}}{\overline{V_N^2}} + G_C^2} \text{ and } B_{OPT} = -B_C. \tag{2.21}$$

The resulting minimum noise factor F_{MIN} is

$$F_{MIN} = 1 + 2R_N(\sqrt{\frac{G_U}{R_N} + G_C^2} + G_C). \tag{2.22}$$

Furthermore, it is possible to express the noise factor F of a circuit as

$$F = F_{MIN} + \frac{R_N}{G_S}\left[(G_S - G_{OPT})^2 + (B_S - B_{OPT})^2\right]. \tag{2.23}$$

Equation (2.23) describes non-concentric circles of constant noise factors for the complex signal source impedance $Y_S = G_S + jB_S$.
The classical derivation of noise matching presented above does not take any power considerations into account. Especially at the antenna of a wireless receiver it is desirable to transfer as much of the often low signal power into the receiver as possible. Therefore power matching is most often applied to the LNA as the first circuit block of a receive chain. Although noise matching is not common practice the classical derivation helps understanding how to achieve acceptable noise performance. From (2.23) we see that a large R_N makes the noise performance more sensitive to the input matching [35].

2.4. Linearity

The basic idea for calculation of non-linear effects is that the behaviour of a circuit block can be approximated by a non-linear transfer function (for a certain limited input range):

$$y(t) = a_1 \cdot x(t) + a_2 \cdot x^2(t) + a_3 \cdot x^3(t) + ... \tag{2.24}$$

with

$y(t)$	Output signal
$x(t)$	Input signal
a_1	> 0
a_2	> 0
a_3	< 0.

If the circuit is considered ideally balanced, even order components are set to zero e.g. $a_2 = 0$ for convenience.
When the input signal is a single-tone $x(t) = A \cdot \cos(\omega_0 t)$, the generated output signal $y(t)$ consists of different frequency components:

$$\begin{array}{llll} dc & y(t) = & & \frac{1}{2}a_2A^2 \\ \omega_0 & & + & (a_1A + \frac{3}{4}a_3A^3)\cos(\omega_0 t) \\ 2\omega_0 & & + & \frac{1}{2}a_2A^2\cos(2\omega_0 t) \\ 3\omega_0 & & + & \frac{1}{4}a_3A^3\cos(3\omega_0 t) \\ ... & & + & ... \quad . \end{array} \tag{2.25}$$

Besides the emerging spectral components, it is worth noting that the linear amplification of the output fundamental is no longer a_1 but $(a_1 + 3/4a_3A^2)$. This means that the third order non-linearity reduces the voltage gain of the fundamental sine wave. The phenomenon is well known in literature and commonly characterised by the 1 dB compression point ($CP1$) [47]. The $CP1$ is defined as the power (or voltage) level for which the amplification of the fundamental frequency is attenuated by 1 dB compared to its ideal linear amplification a_1. From (2.25) it can be shown that for

$$A_{1dB} = \sqrt{0.145\,|a_1/a_3|} \tag{2.26}$$

the input referred 1 dB compression point ($CP1i$) is reached.
In the following we assume an input signal consisting of two fundamental tones $\omega = \omega_1$ and

$\omega = \omega_2$ with different amplitudes A_1 and A_2:

$$x(t) = A_1 \cdot \cos(\omega_1 t) + A_2 \cdot \cos(\omega_2 t) \tag{2.27}$$

The output signal $y(t)$ results in

$$\begin{array}{rrcl}
dc & y(t) & = & \frac{a_2}{2}(A_1^2 + A_2^2) \\
\omega_1 & & + & (a_1 + a_3(\frac{3}{4}A_1^2 + \frac{3}{2}A_2^2))A_1 \cos(\omega_1 t) \\
\omega_2 & & + & (a_1 + a_3(\frac{3}{4}A_2^2 + \frac{3}{2}A_1^2))A_2 \cos(\omega_2 t) \\
2\omega_1 & & + & \frac{a_2}{2}A_1^2 \cos(2\omega_1 t) \\
2\omega_2 & & + & \frac{a_2}{2}A_2^2 \cos(2\omega_2 t) \\
\omega_1 + \omega_2 & & + & a_2 A_1 A_2 \cos((\omega_1 + \omega_2)t) \\
\omega_1 - \omega_2 & & + & a_2 A_1 A_2 \cos((\omega_1 - \omega_2)t) \\
3\omega_1 & & + & \frac{a_3}{4}A_1^3 \cos(3\omega_1 t) \\
3\omega_2 & & + & \frac{a_3}{4}A_2^3 \cos(3\omega_2 t) \\
2\omega_1 + \omega_2 & & + & \frac{3}{4}a_3 A_1^2 A_2 \cos((2\omega_1 + \omega_2)t) \\
\omega_1 + 2\omega_2 & & + & \frac{3}{4}a_3 A_1 A_2^2 \cos((\omega_1 + 2\omega_2)t) \\
2\omega_1 - \omega_2 & & + & \frac{3}{4}a_3 A_1^2 A_2 \cos((2\omega_1 - \omega_2)t) \\
2\omega_2 - \omega_1 & & + & \frac{3}{4}a_3 A_1 A_2^2 \cos((2\omega_2 - \omega_1)t) \\
 & & + & \ldots \quad .
\end{array} \tag{2.28}$$

First let us assume that the input signals significantly differ in amplitude i.e. $A_2 \gg A_1$. From (2.28) we see that the gain for the fundamental tone ω_2 will be reduced (desensitization) or may even drop to zero (blocking) [47].
If we assume that the second tone in (2.27) is modulated in amplitude by a sinusoid with $\omega = \omega_M$ e.g. $A_2(1 + m\cos(\omega_M t))$, where $m < 1$ is the modulation index and $A_2 \gg A_1$, (2.28) changes into

$$y(t) = \left[a_1 + \frac{2}{3}a_3 A_2^2 (1 + \frac{m^2}{2} + \frac{m^2}{2}\cos(2\omega_M t) + 2m\cos(\omega_M t))\right] A_1 \cos(\omega_1 t) + ... \tag{2.29}$$

The gain for the signal at $\omega = \omega_1$ now contains amplitude modulation with $\omega = \omega_M$ and $\omega = 2\omega_M$. This phenomenon is called cross modulation [47].
Another interesting scenario is the presence of spectral components at $\omega = 2\omega_1 - \omega_2$ or $\omega = 2\omega_2 - \omega_1$ in the output signal $y(t)$ in (2.28) (cf. Fig. 2.2). Assume two strong interferers with amplitudes A_1 and A_2 with a frequency spacing $\Delta\omega = \omega_2 - \omega_1$ so that the third order intermodulation product occurring at $\omega = 2\omega_2 - \omega_1$ falls into a wanted frequency channel. If the wanted signal is too weak the intermodulation product may dominate the spectra of the channel. Due to its position on the frequency axis the intermodulation product cannot be filtered out.

Literature commonly describes the effects of third order intermodulation in terms of the third order intercept point IP_3 (cf. Fig. 2.3). From (2.28) we see that the spectral power of the third order products grows with the power of three while the fundamental components grow linearly. If we plot the output power P_{OUT} for the fundamental component and the third order component vs. the input power P_{IN} of the fundamental input tone of a non-linear circuit block in logarithmic scaling the slope of the fundamental output tone is one while the slope for the third order component is three for small input powers far from the power levels where the circuit

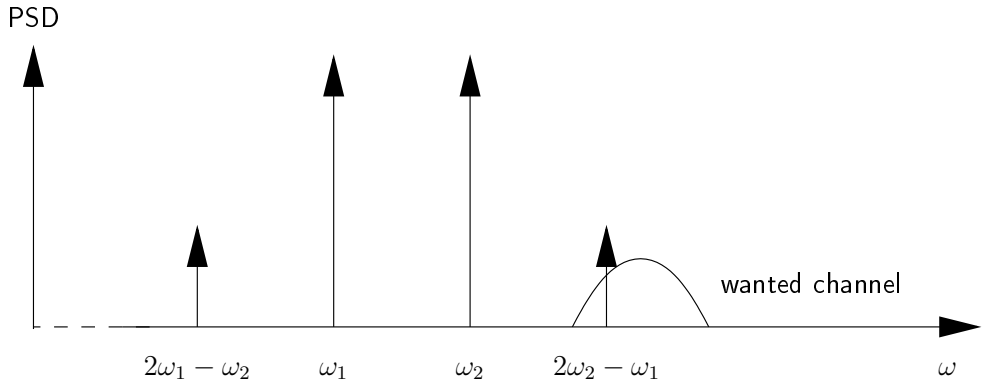


Figure 2.2.: Two interferers at $\omega = \omega_1$ and $\omega = \omega_2$ are located close to the wanted channel. The third order intermodulation product at $\omega = 2\omega_2 - \omega_1$ falls into the wanted channel [47].

is already in compression. Both curves can be extrapolated by straight lines. The IP_3 is defined as the intersection of both lines.

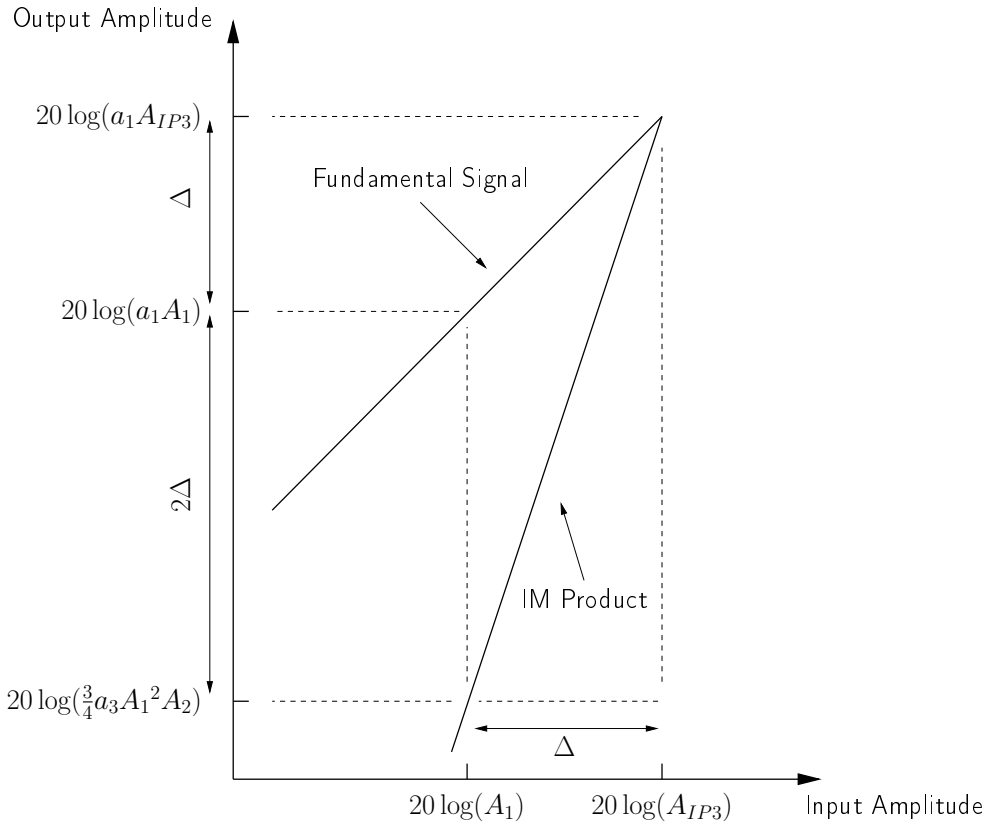


Figure 2.3.: Graphical interpretation of the IP_3 in double logarithmic scaling. The intermodulation product is growing with the power of three while the fundamental signal is growing linearly [47].

From (2.28) we denote

$$A_{IP3} = \sqrt{\left|\frac{4a_1}{3a_3}\right|} \text{ if } A_1 = A_2 = A \text{ [47].} \tag{2.30}$$

For circuit simulations and hands-on measurements it is important not only that at the interpolation point the power level of the third order components has to be negligible compared to that of the fundamental but also that it is above the noise floor of the circuit.
Putting (2.30) and (2.26) in relation we find

$$\frac{A_{IP3}}{A_{1dB}} = \sqrt{\frac{4}{3 \cdot 0.145}} \approx 9.6\,\text{dB [47].} \tag{2.31}$$

Keep in mind that the IP_3 is determined from a two-tone test, while $CP1$ is a obtained in a single-tone test.
For a series of n cascaded stages $i = 1..n$ with a linear voltage gain g_{Vi} and A_{IP3i} of each individual block

$$A_{IP3TOT} \approx \sqrt{1/(A_{IP31}^{-2} + g_{V1}^2 A_{IP32}^{-2} + g_{V1}^2 g_{V2}^2 A_{IP33}^{-2} + ...)} \tag{2.32}$$

gives the overall IIP_3 [47]. Note that the last in the chain stages dominate the overall IP_3 as their contribution to the overall IP_3 is scaled by the gain of the previous stages.

It is possible to determine not only the IP_3 but to calculate a more general IP_n. The train of thoughts is similar to that used for the IP_3. The nth-order intermodulation product is growing with the power of n. The author of [21] reports

$$IIP_n = \frac{1}{n-1}(nP_{INT} - (IM_n - G_P)) = P_{INT} + \frac{P_{SIG} - (IM_n - G_P)}{n-1}, \tag{2.33}$$

with

IM_n	power level of the n-th order intermodulation product
P_{INT}	power level of the interferer at the block input
G_P	power gain of the circuit block

for the n-th order input referred intermodulation point.
Besides the IP_3 the second order intercept point IP_2 is of special interest for the design of an integrated wireless receiver (cf. Section 3.2.3). With (2.33) we can easily formulate

$$IIP2 = 2P_{INT} - (IM_2 - G_P). \tag{2.34}$$

While it came in handy to set $a_2 = 0$ for calculating odd order effects, we need to set $a_2 \neq 0$ in (2.24) in order to derive the IP_2.

2.5. Power Consumption

When we speak about the power consumption of a circuit we are usually interested in the *dc* power consumption and not in an instantaneous or *ac* value.

$$P_{DC} = V_{DC} \cdot I_{DC} \tag{2.35}$$

Especially for mobile applications with a limited battery life-time the power consumption is of concern.

After this brief introduction to characteristics and performance metrics of analogue circuitry we will now review circuit topologies for the circuit blocks of a receive chain in the following sections.

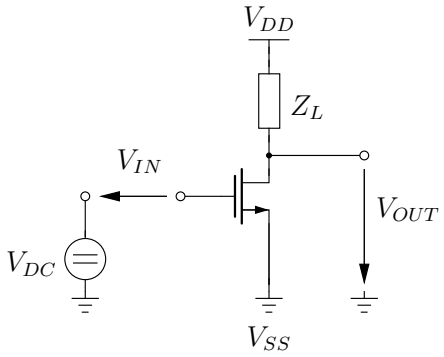
2.6. LNA Topology Review

The LNA is usually the first component in the signal path of an integrated wireless receive chain. The weak signal received at the antenna is fed into the LNA. In order to absorb as much signal power as possible from the antenna, the LNA needs to provide a sufficiently matched input impedance. The main purpose of the LNA ideally is noiseless amplification of the receive signal. Being the first element on chip in the receive chain the LNA is likely to dominate the noise performance of the whole chip (cf. (2.9)). Generally speaking, LNAs in modern integrated wireless receivers are simple transistor amplifiers consisting of a limited number of elements. The more elements the LNA consists of, the more likely it is to be noisy because the individual devices will add their noise contribution. Although a high gain at the beginning of the receive chain is favourable for the noise performance of the whole receiver, the increased linearity requirements imposed on the succeeding blocks of the chain demand a trade-off between noise and linearity performance of the receiver. There are basically two popular classes of single-transistor amplifiers: the common source (CS) and the common gate (CG) amplifier. Both classes aim at utilising the CMOS transistor as a voltage-controlled current source. The transistor works as a transconductor that converts the RF input voltage into an RF current. The RF current is then routed to an internal LNA load Z_L where it causes a voltage drop. In general, the load Z_L of the amplifying transistor is a complex impedance. Broadband LNAs will use purely resistive internal loads $Z_L = R_L$ whereas frequency selective LNAs will prefer resonant tanks e.g. $Z_L = j\omega L \ll 1/(j\omega C_L)$ tuned to resonate at the frequency of the wanted signal. The external load of an LNA is usually the input impedance of the succeeding mixer stage Z_{MIXER}. Z_{MIXER} is empirically assumed to be of strong capacitive nature as the input stage of most active mixers is a CMOS transconductance stage.

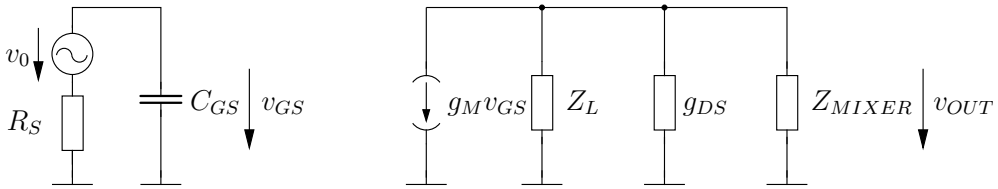
2.6.1. Common Source LNA

The basic circuit topology for a CS LNA is depicted in Fig. 2.4(a). The RF input signal V_{RF} is applied to the gate terminal of the amplifying transistor. The potential of the source node is fixed. Analysing the small signal equivalent circuit of the CS LNA (Fig. 2.4(b)), we calculate

$$\frac{v_{out}}{v_0} = -g_M Z''(1 + sR_S C_{GS}) \tag{2.36}$$



(a) Large signal schematic.



(b) Small signal equivalent circuit with an input port (v_0, R_S) and a load (Z_{MIXER}).

Figure 2.4.: Basic common source LNA topology.

with

$Z'' = \quad Z_L \| 1/g_{DS} \| Z_{MIXER}$
Z_{MIXER} input impedance of succeeding circuit block (usually the mixer)

for the voltage gain of the CS LNA.
While a purely resistive load $Z_L = R_L$ is probably best suitable for wide-band applications, an LC-tank $Z_L = 1/(j\omega C_L) \| j\omega L_L$ is more suitable for applications that require frequency selective behaviour because of the impact of Z_L on the voltage gain v_{OUT}/v_0 of the CS topology (cf. (2.36)). It is worth noting that an external load impedance (here Z_{MIXER}) ends up in parallel to the internal load impedance Z_L and the drain source transconductance g_{DS} for small signal calculations. This bears three important consequences:

- It is not possible to increase the gain of the topology significantly by increasing Z_L if Z_L does not dominate Z'' e.g. $Z_L \gg Z''$.

- An increased g_{DS} limits the gain achievable with CS LNA (for a fixed g_M).

- As, in general, the input impedance of a mixer circuit is of capacitive nature the gain of the CS LNA will exhibit an inherent low pass frequency characteristic.

By first order approximation the input impedance of the CS topology is dominated by the gate-source capacitance C_{GS} of the amplifying transistor and thus varying with frequency (cf. (2.37)).

$$Z_{INPUT} = \frac{1}{sC_{GS}} \tag{2.37}$$

The input impedance is purely imaginary. A power matching to a source with a purely resistive source impedance e.g. $R_S = 50\,\Omega$ is not feasible without additional matching elements. Cancelling the capacitive input impedance with serial inductors is not sufficient for power matching as the input impedance totally lacks a real part component. In a low-cost implementation it is preferable to reduce the quantity of additional matching elements to a minimum in order to save the costs for external components or die area.
Assuming that the channel thermal noise is the most dominant noise source in the simple CS LNA (neglecting the induced gate noise and noise contributions of the load Z_L) the noise factor of the CS LNA topology is

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_M R_S}(1 + \omega^2 R_S^2 C_{GS}^2) \tag{2.38}$$

$$= 1 + \frac{\gamma}{\alpha}(\frac{1}{g_M R_S} + g_M R_S(\frac{\omega}{\omega_T})^2) \tag{2.39}$$

where

$$\omega_T = g_M/C_{GS}.$$

Besides terms that are constant over frequency we note a term proportional to ω^2 in 2.39. The increase in the noise factor relates to the low-pass for the input signal formed by the source impedance R_S and the gate-source capacitance C_{GS}. It is obvious that the noise factor can be improved by increasing the transconductance g_M of the amplifying transistor.
Due to the drawbacks associated with the input power matching of a simple CS LNA we investigate more advanced CS LNA topologies.

2.6.1.1. CS LNA with shunt feedback

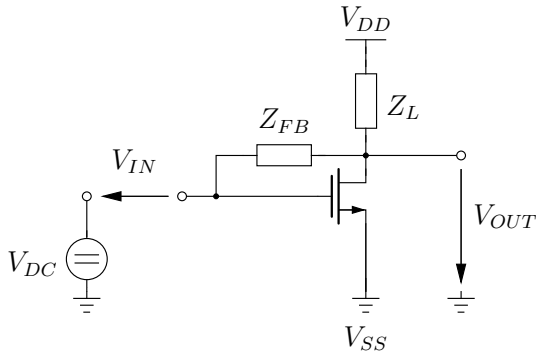
Another modification of the CS LNA is illustrated in Fig. 2.5(a). The circuit is basically a CS amplifier with a feedback from the output node to the input node.

From the small signal equivalent circuit in Fig. 2.5(b) we can derive the voltage gain for the loaded amplifier to be

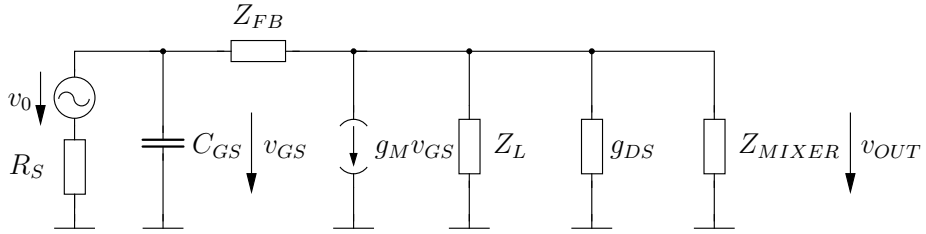
$$\frac{v_{OUT}}{v_0} = \frac{Z''(1 - g_M Z_{FB})}{R_S + Z'' + Z_{FB} + sR_S C_{GS}(Z_{FB} + Z'') + g_M R_S Z''} \tag{2.40}$$

where

$Z'' =$ $Z_L \| 1/g_{DS} \| Z_{MIXER}$
Z_{MIXER} input impedance of succeeding circuit block (usually the mixer).



(a) Large signal schematic.



(b) Small signal equivalent circuit with an input port (v_0, R_S) and a load (Z_{MIXER}).

Figure 2.5.: Common source LNA topology with shunt feedback.

The input impedance of the amplifier LNA is given by

$$Z_{INPUT} = \frac{Z_{FB} + Z''}{1 + g_M Z'' + sC_{GS}(Z_{FB} + Z'')}. \tag{2.41}$$

In [47] the input impedance Z_{INPUT} for a CS LNA with a feedback capacitor $Z_{FB} = 1/(sC_{FB})$, a resistive internal load $Z_L = R_L$ and a capacitive external load $Z_{MIXER} = 1/(sC_{MIXER})$ is investigated under specific constraints. Neglecting C_{GS} the input admittance is split into its real and imaginary part:

$$Re\{1/Z_{INPUT}\} = R_L C_{FB}\omega^2 \frac{C_{FB} + g_M R_L(C_{MIXER} + C_{FB})}{R_L^2(C_{MIXER} + C_{FB})^2\omega^2 + 1} \tag{2.42}$$

$$Im\{1/Z_{INPUT}\} = \omega C_{FB} \frac{R_L^2 C_{MIXER}(C_{MIXER} + C_{FB})\omega^2 + 1 + g_M R_L}{R_L^2(C_{MIXER} + C_{FB})^2\omega^2 + 1}. \tag{2.43}$$

Applying a set of simplifications ($g_M R_L \gg 1$, $C_{MIXER} \gg C_{FB}$ and $\omega \approx 1/(R_L C_{MIXER})$ to ((2.42) and (2.43)) the author of [47] concludes that for proper choice of parameters real part input matching is possible:

$$Re\{1/Z_{INPUT}\} = \frac{g_M C_{FB}}{2C_{MIXER}} \tag{2.44}$$

$$Im\{1/Z_{INPUT}\} = \omega C_{FB}(1 + \frac{g_M R_L}{2}). \tag{2.45}$$

It is also pointed out that the topology exhibits low voltage gain at high frequencies due to the bandwidth limitation at the output node introduced by R_L and C_{MIXER}. In addition replacing the feedback impedance Z_{FB} with feedback capacitor essentially means inserting a gate-drain capacitance on purpose. Of course the well-known Miller effect is linked to a gate drain capacitance of the CS LNA. Although the shunt feedback helps the input power matching compared to the CS amplifier without feedback, the feedback CS LNA will need extra compensation of the imaginary part of the input impedance for proper power matching. Another point worth noting is that the feedback branch deteriorates the noise performance as it provides a direct path from the input node to the output node. This direct path also affects the backward isolation of the LNA. From the (2.44) we see that the real part of input admittance is inversely proportional to the external load capacitance of the LNA. The explicit interaction of the LNA input impedance and the mixer input impedance proves that the LNA and the mixer design is closely linked and hard to separate.

2.6.1.2. Inductively Source Degenerated CS LNA

The inductively source degenerated CS LNA (Fig. 2.6(a)) is an advanced version of the basic CS LNA. From Fig. 2.6(b) the voltage gain can be calculated to be

$$\begin{aligned}\frac{v_{OUT}}{v_0} =&(\frac{(1+(Z^{'}+sL_S)g_{DS})sC_{GS}(R_S+1/(sC_{GS})+s(L_G+L_S))}{Z^{'}(s^2L_SC_{GS}g_{DS}-g_M)}\\ &-\frac{sL_S(s^2L_SC_{GS}g_{DS}-g_M)}{Z^{'}(s^2L_SC_{GS}g_{DS}-g_M)})^{-1}\end{aligned} \tag{2.46}$$

where

$$Z^{'} = \ Z_L \| Z_{MIXER}.$$

If we assume that g_{DS} is almost zero in a first order approximation we can simplify (2.46) to

$$\frac{v_{OUT}}{v_0} = -\frac{g_M Z^{'}}{1+s(R_SC_{GS}+g_ML_S)+s^2(L_G+L_S)C_{GS}} \tag{2.47}$$

We now prove that the inductively degenerated CS LNA can be power matched to a signal source with a purely resistive source impedance by calculating the input impedance Z_{INPUT}.

$$Z_{INPUT} = \frac{L_S}{C_{GS}}(\frac{g_M - s^2L_SC_{GS}g_{DS}}{1+g_{DS}(Z^{'}+sL_S)}) + \frac{1}{sC_{GS}} + s(L_G+L_S) \tag{2.48}$$

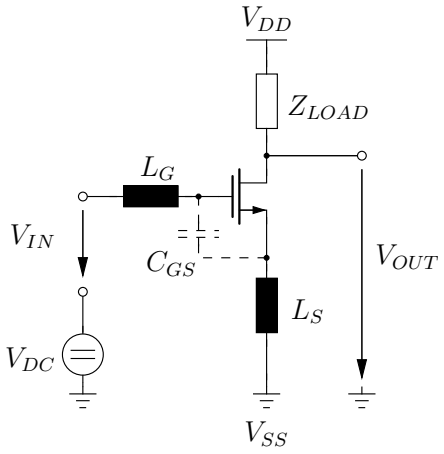
If we simplify (2.48) by setting $g_{DS}=0$ we can find a frequency $\omega = \omega_0$ with

$$\omega_0^2 = \frac{1}{C_{GS}(L_S+L_G)} \tag{2.49}$$

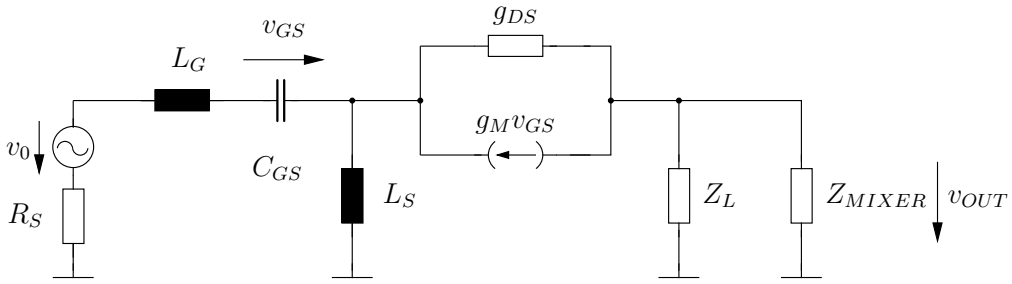
for which the imaginary part of Z_{INPUT} is equal to zero:

$$Z_{INPUT}|_{\omega=\omega_0, g_{DS}=0} = \frac{g_ML_S}{C_{GS}} + j0. \tag{2.50}$$

Thus a power match of the inductively source degenerated CS LNA is feasible. Assuming a g_M chosen by the analogue designer for the amplifying transistor and a C_{GS} associated to the tran-



(a) Large signal schematic.



(b) Small signal equivalent circuit with an input port (v_0, R_S) and a load (Z_{MIXER}).

Figure 2.6.: CS LNA topology with inductive source degeneration.

sistor dimensions w/l necessary for the chosen g_M under the bias conditions at hand, the designer is free to chose the inductance L_S. After the real part of (2.50) is set to the desired impedance e.g. $50\,\Omega$, the designer can use the second degree of freedom to set the inductance L_G in (2.49) so that the imaginary part of in the input impedance Z_{INPUT} is equal to zero at the frequency of interest $\omega = \omega_0$.

The author of [3] calculates the noise factor F for an unloaded CS LNA with inductive source degeneration (taking channel noise, gate noise and correlated noise into account) to be

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega_0}{\omega_T}\right)\left[1 + \frac{\delta\alpha^2}{5\gamma}(1+Q^2) + 2\,|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right] \tag{2.51}$$

where

$$\begin{aligned} Q &= 1/(\omega_0 C_{GS} R_S) \\ c &= j \cdot 0.395 \\ \omega_T &= g_M/C_{GS} \text{ zero current gain transit frequency.} \end{aligned}$$

It is observed that quality factor Q of the input resonant circuit reduces the noise contribution of the thermal channel noise whereas the noise contribution of the induced gate noise is increased.

Thus an optimum Q_{OPT} resulting in a minimum noise factor F_{MIN} can be derived:

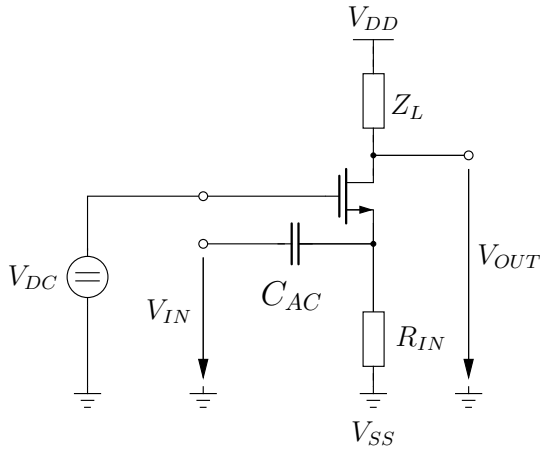
$$Q_{OPT} = \sqrt{1 + 2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2}} \tag{2.52}$$

$$F_{MIN} = 1 + \frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right)\frac{2\delta\alpha^2}{5\gamma}Q_{OPT} \tag{2.53}$$

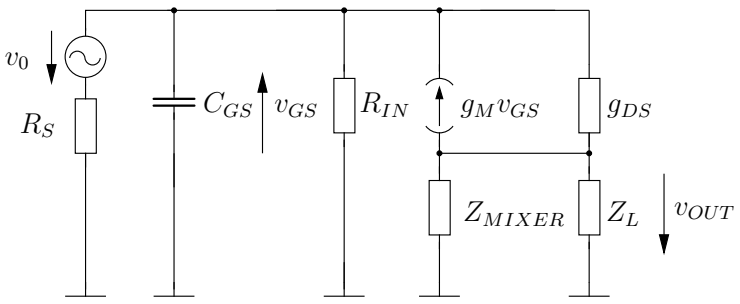
The inductive degeneration offers the possibility of low-noise matching for a CS LNA. The drawback of this configuration is that perfect power matching is limited to a single frequency ω_0 only. That is why the CS LNA with inductive degeneration is not suitable for wideband applications. Another drawback is the fact that two area consuming inductances L_S and L_G are necessary for this topology.

2.6.2. Common Gate LNA

In the CG LNA topology (Fig. 2.7(a)) the RF input signal is applied to the source terminal of the amplifying transistor. From the small signal equivalent circuit (Fig. 2.7(b)) we can calculate the voltage gain (2.54) and the input impedance (2.56) of the topology.



(a) Large signal schematic.



(b) Small signal equivalent circuit with an input port (v_0, R_S) and a load (Z_{MIXER}).

Figure 2.7.: Common gate LNA topology.

$$\frac{v_{OUT}}{v_0} = \frac{Z^{'}(g_{DS}+g_M)}{R_S(g_{DS}+g_M)+(1+R_S/R_{IN}+sR_SC_{GS})(1+Z^{'}g_{DS})} \quad (2.54)$$

$$\frac{v_{OUT}}{v_0}|_{g_{DS}=0} = \frac{g_M Z^{'}}{g_M R_S+(1+R_S/R_{IN}+sR_SC_{GS})} \quad (2.55)$$

$$Z_{INPUT} = \frac{R_{IN}(1+Z^{'}g_{DS})}{(1+sR_{IN}C_{GS})+R_{IN}(g_{DS}+g_M)} \quad (2.56)$$

$$Z_{INPUT}|_{g_{DS}=0} = \frac{R_{IN}}{(1+sR_{IN}C_{GS})+g_M R_{IN}} \quad (2.57)$$

$$Z_{INPUT}|_{g_{DS}=0,C_{GS}=0} = \frac{R_{IN}}{1+g_M R_{IN}} \quad (2.58)$$

with

$$Z^{'} = Z_L \| Z_{MIXER}$$

In contrast to the CS LNA, the CG LNA is a non-inverting topology (cf. (2.36) and (2.54)). The resistor R_{IN} is needed as it provides a *dc* current path for the drain source current of the amplifying transistor. If the amplifying transistor is reduced to a voltage controlled current source in a first order assumption, the transconductance g_M and the resistor R_{IN} connected in parallel determine the input impedance Z_{INPUT} of CG LNA. This inherent purely resistive wideband input impedance (2.58) is the great advantage of the CG LNA over the CS LNA. The drawback of the CG LNA is that its noise behaviour is inferior to the CS LNA. The author of [3] calculates the noise factor F (neglecting the noise contribution of the induced gate noise and R_{IN}) of the CG LNA to be

$$F \approx 1+\frac{\gamma}{\alpha}\frac{1}{g_M R_S} \quad (2.59)$$

In order to improve the noise performance it is desirable to increase g_M. However, the maximum acceptable g_M is limited by the input power matching requirement. In case of perfect power matching ($g_M R_S = 1$ and $1/g_M \gg R_I N$) the expression for F is reduced to

$$F \approx 1+\frac{\gamma}{\alpha} \quad (2.60)$$

where

$\alpha =$ $g_M/gd0$
$\alpha =$ 1 for long channel devices
$\alpha \leq$ 1 for short channel devices.

For a short channel amplifying transistor with an optimistic $\gamma = 2$, (2.60) limits the noise figure to $NF_{MIN} \geq 4.77\,\text{dB}$ for a CG LNA in case of a perfect power match.
If we sacrifice the perfect power match we get [44]

$$F \approx 1+\frac{\gamma}{\alpha}\frac{1-S_{11}}{1+S_{11}}. \quad (2.61)$$

Assuming that $S_{11} = -10\,\text{dB}$ ($\gamma/\alpha \geq 2$) is still acceptable we can increase the g_M of the amplifying transistor and achieve a noise figure as low as $NF \geq 3.09\,\text{dB}$ for the CG LNA.
In favour of the CG LNA the author of [3] mentions that the CG LNA topology is superior to

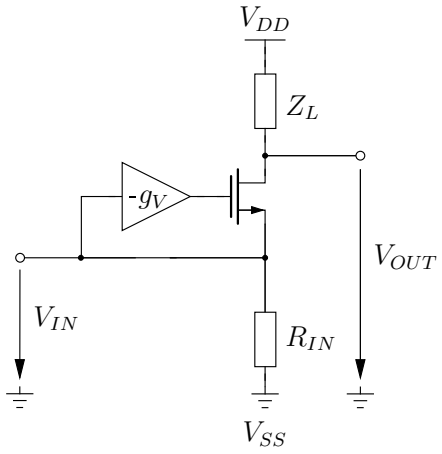


Figure 2.8.: G_M boosted CG LNA adapted from [3]. No biasing included.

the CS LNA in terms of reverse isolation and stability. As the Miller effect on the gate drain capacitance of the amplifying transistor does not exist, the CG LNA can easily do without a cascode stage.

2.6.2.1. CG LNA with GM-Boosting.

The author of [3] suggests a CG LNA topology (Fig. 2.8) that overcomes the trade-off between noise performance and the input matching requirement by introducing an inverting gain $-A_G$ between the source terminal and the gate terminal of the amplifying device. The resulting noise factor F and input impedance Z_{INPUT} for $R_{IN} \gg g_M$ are

$$F = 1 + \frac{\gamma}{\alpha} \frac{1}{(1+g_V)^2 g_M R_S} \tag{2.62}$$

and

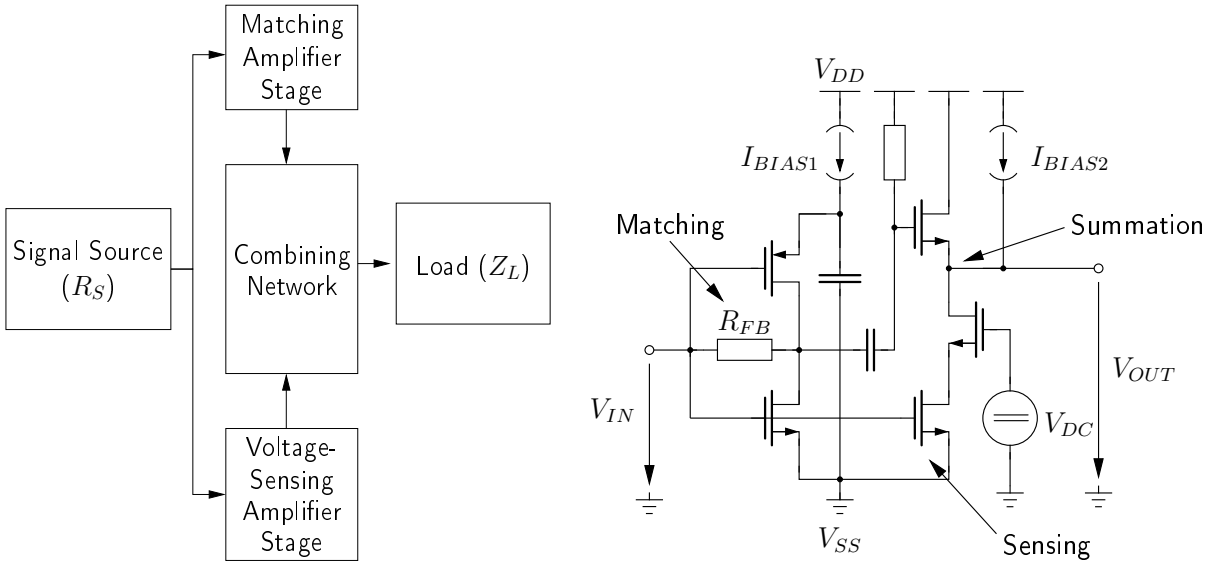
$$Z_{INPUT} = \frac{1}{(1+g_V)g_M}. \tag{2.63}$$

Bearing the input matching requirement $Z_{INPUT} = R_S$ in mind we find a noise figure improvement by the factor $(1 + g_V)$ compared to (2.60). The author of [3] implements the necessary inverting gain $-g_V = -1$ by a pair of cross-coupled capacitors between pseudo-differential branches. Switching from a single-ended topology to a differential or pseudo-differential topology should not be considered a drawback of the G_M-boosting CG LNA. Due to the manifold sources of disturbances especially in SoC solutions (e.g. coupling from the digital domain) a differential LNA topology is intended for the final LNA implementation.
Adding active devices to the LNA circuitry in order to increase g_V beyond unity helps the noise performance according to (2.62) but the active devices will likely introduce new noise sources to the LNA circuitry and spoil the positive virtues of G_M-boosting. Furthermore, the author of [3] points out that the G_M-boosted CG LNA needs a cascode stage in order to preserve backward isolation and stability. A cascode stage implies additional noise and needs additional voltage headroom. The LNA topology suggested in [3] does not use a resistor at the source node of the amplifying transistor but an inductor. Furthermore, the suggested LNA applies an inductor for the load impedance Z_L. The usage of inductors instead of resistors helps the noise perfor-

mance of the LNA but increases the die area consumption of the LNA and inherently increases the manufacturing costs of the receiver chip. In [3] no actual CMOS LNA implementation is presented but merely simulation results ($S_{21} = 10.4\,\text{dB}$, $NF_{MAX} = 1.69\,\text{dB}$, $IIP_3 = 2.69\,\text{dBm}$, $I_{DC} = 3.6\,\text{mA}$, $f = 5.6\,\text{GHz}$ for a schematic-based LNA operated from a 1.8 V supply in a 180 nm CMOS technology.
The same group of authors pursuit the G_M-boosting approach and published actual measurement results ($S_{21} = 9.4\,\text{dB}$, $NF_{MAX} = 2.5\,\text{dB}$, $IIP_3 = 7.6\,\text{dBm}$, $P_{DC} = 3.4\,\text{mW}$, $f = 5.8\,\text{GHz}$) in [37]. As an on-chip transformer is used to provide $g_V = 1$ besides the load inductor the presented LNA consumes a relatively large die area of 0.9 mm by 0.7 mm. Thus the LNA design in [37] is not suited for low-cost mass production. It is evident that the inductor values and the die area consumption of the inductors increase if the design is adopted for usage below $f = 2\,\text{GHz}$. Nevertheless the LNA presented in [37] is well suited for low power applications.

2.6.3. Noise Cancellation Techniques

The previous sections discussed CG LNA topologies that provide broadband input matching at the cost of inferior noise performance and CS LNA topologies that offered acceptable noise performance at the cost of inferior matching properties. The author of [8] investigates LNA topologies that exploit noise cancellation techniques and exhibit wideband input matching. A conceptional block diagram is presented in Fig. 2.9(a). The path of the RF input signal splits directly at the input of the circuitry after the RF signal source. One path contains an amplifier stage that preserves input power matching (e.g. a CG LNA or a CS LNA with shunt feedback structure). The other path contains a voltage sensing amplifier stage with a high input impedance (e.g. a CS amplifier stage). Thus the former stage dominates the input impedance while the latter stage can sense not only the RF input signal but also the noise contribution across the input source. So the sensing amplifier amplifies not only the RF input signal on purpose but also the noise. The two paths are combined in a way so that the RF input signal components add up while noise components from both paths cancel each other. The underlying assumption is that the amplification in the sense path can be freely chosen to match the noise contribution of the input matching path and that identical delays are introduced to the signals along both paths. The cancellation effect does only account for the noise contribution of the input matching device, but this is considered one of the most prominent contributors to the overall noise performance (cf. (2.9)). In the examples given in [8] the constructive superposition of the RF signal respectively destructive superposition of the noise is implemented with the help of simple inversions in the paths. The most intuitive way of combining both paths is adding currents at a node in the circuitry before turning the current into a voltage by means of a load impedance Z_L. As the noise cancelling is a feed-forward architecture it is pointed out that it does not exhibit the risk of potential instability. In addition to the noise cancelling effect a distortion cancelling effect is observed as well by the author of [8].
Bandwidth restrictions in both paths caused by device and layout parasitics degrade the benefits of the noise cancellation technique. Furthermore, the LNA employing noise cancellation dissipates a relatively large amount of power for use in a low-power receiver. The exemplary single-ended circuit implemented in [8] (Fig. 2.9(b)) consumes 14 mA from a 2.5 V supply ($G_V = 13.7\,\text{dB}$, $NF_{MAX} = 2.4\,\text{dB}$, $IIP_2 = 12\,\text{dBm}$, $IIP_3 = 0\,\text{dBm}$, $150\,\text{MHz} \leq \text{f} \leq 2000\,\text{MHz}$). As we will later see in Section 3.2 the achieved IIP_2 is much too low for a GSM receiver to pass the GSM specification and would enforce a differential set-up that in turn even doubles the approximate



(a) Conceptional block diagram.

(b) LNA implementation.

Figure 2.9.: Noise cancelling technique [8].

current budget of the LNA. Besides, the employed cascode stages require a high supply voltage for the LNA.

2.7. Mixer Topology Review

In a physical implementation of a receiver the mixer links together LNA and the baseband blocks. Mixer circuits in down-conversion applications like receivers shift the frequency spectra of the RF input signal to intermediate frequency (IF) or baseband (BB) frequency. The mixing process, a convolution in the frequency domain (Fig. 2.10), is a multiplication in the time domain (cf. (2.65)). The mathematical principal of operation can be illustrated as

$$V_{IF}(t) = V_{RF}(t) \cdot V_{LO}(t) \tag{2.64}$$

$$V_{IF}(t) = A_{RF}\cos(\omega_{RF}t) \cdot A_{LO}\cos(\omega_{LO}t) \tag{2.65}$$

$$= \frac{A_{RF}A_{LO}}{2}(\cos((\omega_{RF}-\omega_{LO})t) + \cos((\omega_{RF}+\omega_{LO})t)). \tag{2.66}$$

The RF signal as well as the LO signal contain no *dc* offset for simplicity. A *dc* offset in either input signal e.g. $V_{LO}(t) = A_{LODC} + A_{LO}\cos(\omega_{LO}t)$ instead of $V_{LO}(t) = A_{LO}\cos(\omega_{LO}t)$ will result in an input signal feed-through to the output:

$$V_{IF}(t) = A_{LODC}A_{RF}\cos(\omega_{RF}t) + \frac{A_{RF}A_{LO}}{2}(\cos((\omega_{RF}-\omega_{LO})t) + \cos((\omega_{RF}+\omega_{LO})t)). \tag{2.67}$$

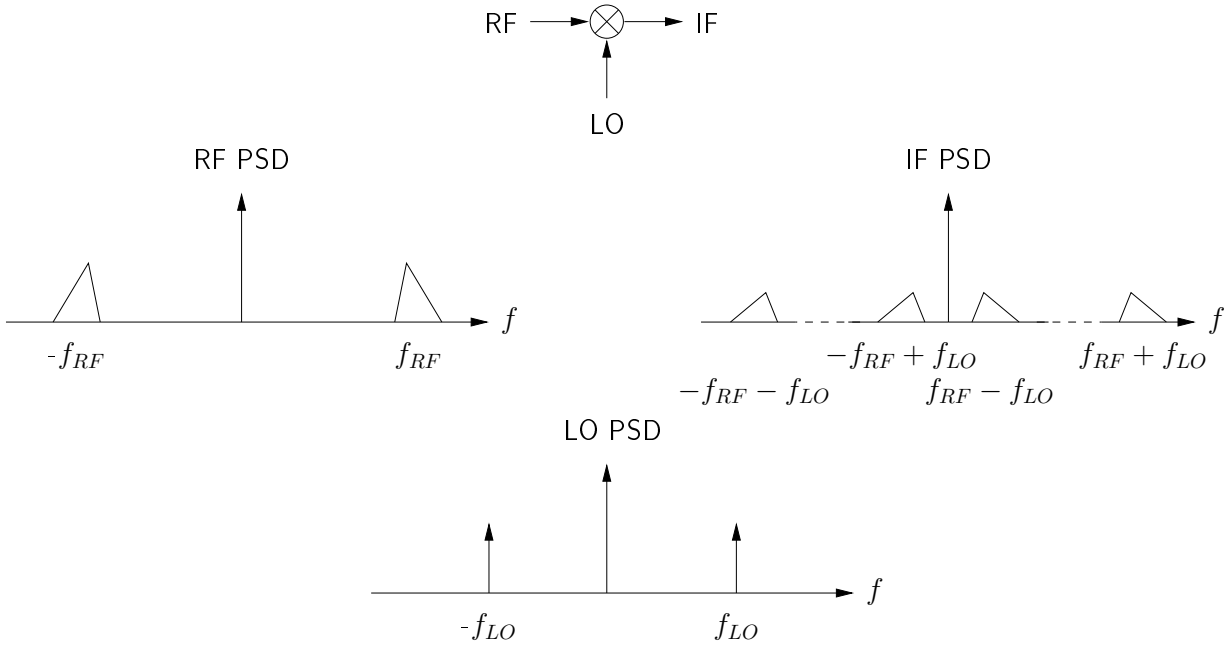


Figure 2.10.: Frequency conversion basics.

A *dc* offset in the RF signal will result in an LO signal-through to the output.
Every single-ended unbalanced signal inherently contains a *dc* biasing offset. This is one of the reasons that a differential design with differentially fed input signals (RF and LO) is superior to a single-ended mixer design. In addition a differential design is less prone to be affected by second-order distortion or coupling based distortion e.g. from a digital circuit integrated on the same die. Mismatches between the differential lines tamper with the balancing of signals.
Although (2.66) shows that an up-conversion ($\omega_{RF}+\omega_{LO}$ term) takes place simultaneously with the down-conversion ($\omega_{RF}-\omega_{LO}$ term), we will ignore the up-conversion term in the following as it is located far from the term of interest on the frequency axis. With ω_{RF} and ω_{LO} closely spaced in the Gigahertz range, a spectral component at $\omega=\omega_{RF}+\omega_{LO}\approx 2\omega_{RF}$ will easily be rendered insignificant by the low-pass filtering in the receive chain.
Signals directly leaking between the three ports of a mixing circuit cause self-mixing. A signal mixing with itself generates a *dc* component that may saturate succeeding BB or IF blocks. This is especially true if the large LO signal leaks to the RF input. The level of port-to-port isolation of the mixer stage is also crucial for the performance of a direct-conversion receiver where the centre frequency of the wanted signal is shifted to *dc* and the wanted signal power may be much less than that of the self-mixing products (cf. Section 3.2.3).
Mixer circuits can be subdivided into several classes:

Unbalanced Mixers. Both, the RF and the LO input signal are single-ended signals with a non-zero *dc* component. The output spectrum contains frequency components at the frequencies of both input signals and *dc* besides the wanted output frequencies.

Single-balanced Mixers. One of the input signals is a differential signal while the other input signal is a single-ended signal. The spectra of the output signals contain only components

at one of the frequencies of the input signals besides the wanted output frequencies.

Double-balanced Mixers. Both input signals are fully differential signals. The output spectrum is free of components at either one of the input frequencies.

Linear multiplying Mixers. As the name suggests these circuits perform a linear multiplication of two input signals which possess a physical meaning [12].

Switching Mixers. The LO signal is a square wave that switches the elements of a commutating stage hard between the on-stage and the off-stage. The multiplying operation is reduced to a mere dimensionless inversion [12].

Passive Mixers. These circuits merely perform a shift in the frequency spectra but the conversion gain is 0 dB or below. The signal is not amplified. There might even be a conversion loss. These circuit does not consume stand-by power.

Active Mixers. The signal conversion gain from input to output is positive. The noise contribution of the mixer stage to the noise performance of the complete receive chain is reduced.

Assuming a mixer with a current commutating stage made up of ideal switches controlled by square wave with zero *dc* offset and 50 % duty cycle (balanced LO signal) we can develop the square wave into a Fourier series

$$V_{LO}(t) = A_{LO} \cdot \sum_{k=0}^{+\infty} \frac{4}{(2k+1)\pi} \sin((2k+1)\omega_{LO}t). \tag{2.68}$$

Inserting (2.68) into (2.64) we obtain

$$V_{IF}(t) = A_{RF}A_{LO}\cos(\omega_{RF}t) \cdot (\sum_{k=0}^{+\infty} \frac{4}{(2k+1)\pi} \sin((2k+1)\omega_{LO}t)) \tag{2.69}$$

$$= \frac{4}{\pi}(\frac{A_{RF}A_{LO}}{2}(\cos((\omega_{RF}-\omega_{LO})t) + \cos((\omega_{RF}+\omega_{LO})t))) + \dots . \tag{2.70}$$

If we now calculate the conversion gain $g_{V,CONV,IF}$ as ratio of output signal at IF to input signals we find that the frequency conversion is burdened with a factor of

$$g_{V,CONV,IF} = \frac{2}{\pi} \quad \text{or} \quad \mathrm{G_{V,CONV,IF}} = -4\,\mathrm{dB}. \tag{2.71}$$

For an unbalanced LO square wave signal the conversion burden is even larger

$$g_{V,CONV,IF} = \frac{1}{\pi} \quad \text{or} \quad \mathrm{G_{V,CONV,IF}} = -10\,\mathrm{dB}. \tag{2.72}$$

These theoretical maximum conversion gains are always smaller in reality as the calculations neglected finite switching time [12]. Now the benefits of active mixer cells become more appar-

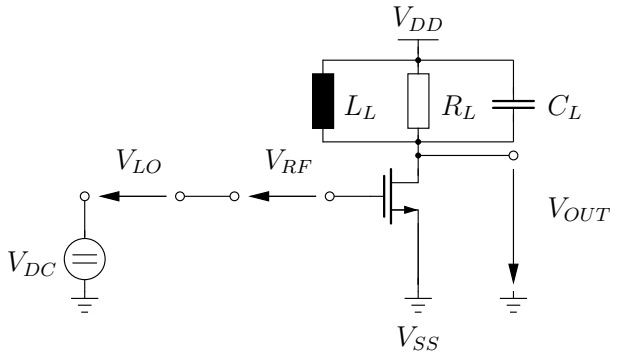


Figure 2.11.: Simple square law mixer. The load is a parallel resonant circuit tuned to IF.

ent. Active mixers can overcome the loss in signal strength related to the conversion process and actually provide conversion gains $G_{V,CONV,IF} \geq 0\,\mathrm{dB}$. Thus we focus on active mixer implementations in this work.
In general it is considered wise to design LNA and mixer circuits as a unit and not separate from each other. The performance of both circuit blocks strongly interacts e.g. changing the mixer input stage directly changes the load conditions of the LNA. In LNA designs with poor backward isolation the mixer input stage even affects the LNA input impedance.
Modern receivers often use complex signal processing at BB resp. IF (cf. Section 3.3). Complex signal processing requires the down-conversion of an in-phase (I) and a quadrature (Q) signal. This in turn requires two phase-shifted LO signals. It is common practice to generate LO signals with a phase shift of 90° necessary for a quadrature mixer by dividing the output frequency signal of a voltage controlled oscillator (VCO) running at twice the desired LO frequency by two. During physical implementation the matching between the I and the Q path deserves special attention in order to avoid amplitude and phase mismatches.

2.7.1. Square Law Mixer

Among the family of mixer topologies that exploit non-linear device characteristics the square law mixer (Fig. 2.11) is fairly simple to understand. The basic circuit topology resembles a CS amplifier with two input signal sources connected in series. The square law mixer's principle of operation is based on the quadratic term in the device equation (4.4) of a CMOS FET. Thus the output voltage is

$$V_{OUT} = Z_L \frac{\mu C_{OX}}{2} \frac{w}{l} (V_{GS} - V_{TH})^2 \tag{2.73}$$

where

$$\begin{aligned} V_{DC} &= V_{TH} \\ V_{GS} - V_{TH} &= V_{RF} + V_{LO}. \\ V_{RF} &= A_{RF} \cos(\omega_{RF} t) \\ V_{LO} &= A_{LO} \cos(\omega_{LO} t) \end{aligned}$$

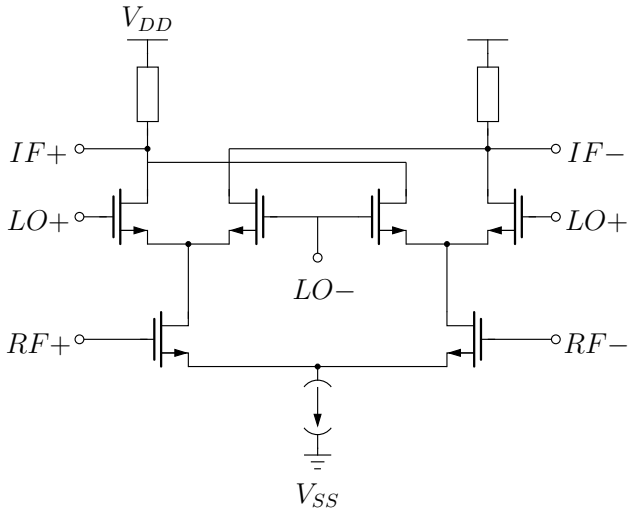


Figure 2.12.: Double balanced Gilbert cell mixer.

$$V_{OUT} = Z_L \frac{\mu C_{OX}}{2} \frac{w}{l} (V_{RF}^2 + 2V_{RF}V_{LO} + V_{LO}^2). \tag{2.74}$$

$$\begin{aligned} V_{OUT} &= Z_L \frac{\mu C_{OX}}{4} \frac{w}{l} A_{RF}^2 (1 + \cos(2\omega_{RF}t)) \\ &+ Z_L \frac{\mu C_{OX}}{4} \frac{w}{l} A_{LO}^2 (1 + \cos(2\omega_{LO}t)) \\ &+ Z_L \frac{\mu C_{OX}}{2} \frac{w}{l} A_{RF}A_{LO} (\cos((\omega_{RF} - \omega_{LO})t) + \cos((\omega_{RF} + \omega_{LO})t) \end{aligned} \tag{2.75}$$

As depicted in Fig. 2.11 the load Z_L of the square law mixer can be a parallel resonant circuit tuned to resonate at the wanted IF frequency. While the undesired higher frequency terms $\omega = 2\omega_{RF}$, $\omega = 2\omega_{LO}$ and $\omega = \omega_{RF} + \omega_{LO}$ in (2.75) can easily be filtered out by means of a low-pass filter, the wanted term $\omega = \omega_{RF} - \omega_{LO}$ and the *dc* terms deserve special attention. In a direct conversion receiver these terms overlap. In a low-IF receiver they may not overlap but they are spaced closely in frequency. A large *dc* component of the IF signal respectively BB signal is prone to saturate the IF/BB circuit blocks. Simple means like *ac*-coupling require large capacitance values at IF/BB frequency.
As the RF and the LO signal use the same input terminal the RF to LO isolation of the square law mixer is poor [45]. Even if one of the input signals is applied to the gate terminal and the other signal is applied to the source terminal this mixer topology experiences increased coupling between both inputs across the parasitic gate-source capacitance of the amplifying transistor.

2.7.2. Gilbert Cell Mixer

The double balanced Gilbert cell mixer (Fig. 2.12) has dominated low-IF receive mixer architectures for years because of the low cross-talk performance achievable [12]. The input stage is a differential pair that works as a transconductance stage for the RF input signal voltage. Once the input signal is turned into a current it is fed to a current commutating stage, the switching quad, which is controlled by the LO signal. On top of the switching quad load impedances turn the

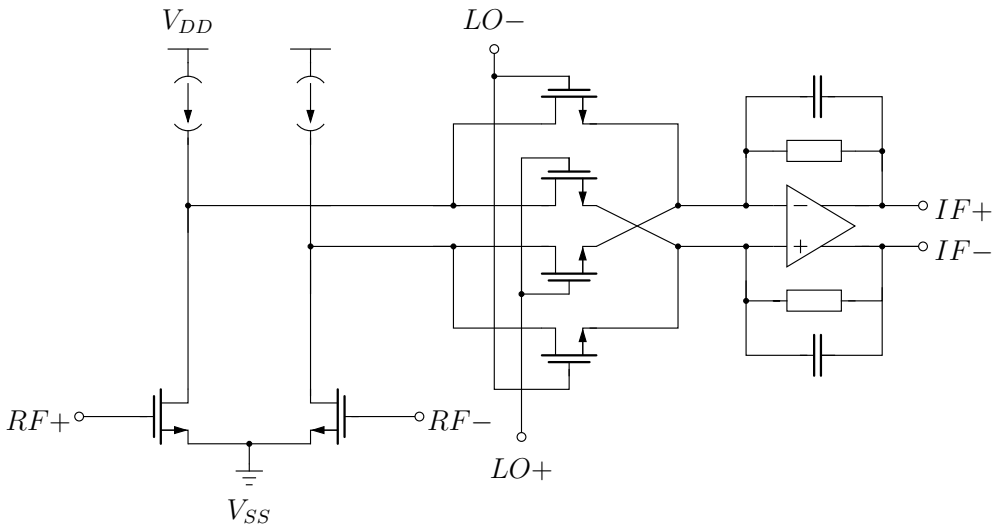


Figure 2.13.: Double balanced Gilbert cell mixer with passive switches and a current mode output. The operational amplifier serves as first pole of the BB filter. Common mode control not shown.

current that is switched between the right and the left branch of the topology into a detectable voltage drop. The load impedances can be purely resistive but might also be low-pass RC shunt loads or resonant tanks if more selective frequency characteristics are desired. The RF signal is always applied to the transconductance stage and not to the switching quad. This is because the RF signal needs linear amplification whereas the switching quad merely alternates the polarity of the current flowing into the load and is therefore driven hard. Driving the switches between on-state and off-state with a large swing square waveform provides clean switching as it reduces time jitter at the moment of switching in the presence of a noisy switch control voltage. Furthermore the linearity performance of the mixer is affected by the transconductance stage only. In order to provide a low on-resistance the switches need to be large in width w. A large width on the other hand requires powerful LO buffers to drive the switches. The driving capability goes hand in hand with an increased current consumption. Another disadvantage of large switches is that they form increased coupling-capacitances in the off-state. This results in poor isolation and degraded LO to IF feed-through. In the classical Gilbert cell mixer the switching quad is biased to operate in the saturation region carrying the *dc* bias current of the transconductance stage [40]. The *dc* bias current in the switches provokes a major flicker noise contribution to the output signal making the classical Gilbert architecture unattractive for direct-conversion receivers. In addition the basic concept of the Gilbert architecture, stacking a current source, a transconductance stage and the switching quad on top of each other sets a certain enlarged minimum level of voltage supply headroom necessary for the classical Gilbert cell mixer.

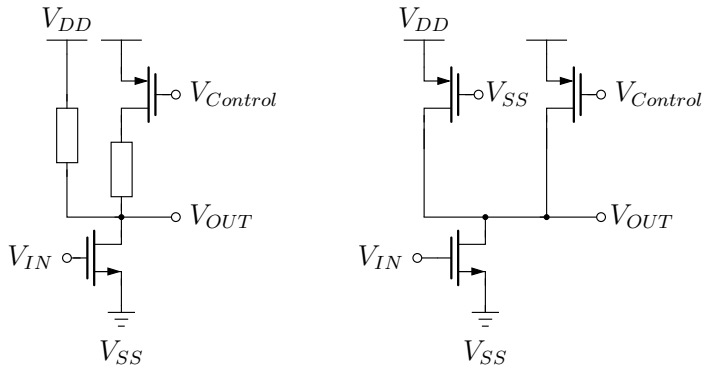
2.7.3. Passive switching Mixer with Current Output

The mixer circuit depicted in Fig. 2.13 is based on a Gilbert cell mixer but it is optimised in three ways for use in a low-voltage direct conversion receiver. First of all the output stage is not voltage mode but current mode. The commutated current is directly fed to an active low-pass

filter. The operational amplifier (opamp) provides a low impedance input node not only at BB or IF frequency but up to the bandwidth restrictions of the opamp. Thus there is almost no voltage swing at the mixer output and evidently no voltage clipping. The opamp in low-pass configuration is the first pole of the baseband filter and simultaneously converts the mixer output current into a voltage swing. Operating at BB respectively IF frequency the active filter pole can easily introduce serious gain to the receive signal. Being integral part of the channel filtering the additional die area consumption and power consumption of the opamp are acceptable. As the opamp introduces new noise sources to the receiver the opamp has to be designed with care. The design of a rail-to-rail opamp is best suited to exploit the available voltage headroom and to prevent saturation of the receiver when blocker signals are applied.
Second, the switches are operated in passive mode meaning that they carry no *dc* bias current from the input stage. This bears the advantage that they do introduce much less flicker noise to the BB/IF signal compared to the classical switching quad in Section 2.7.2. In fact the reduced flicker noise in the output signal makes mixers with passive switches attractive for direct conversion receivers. The switches are biased near threshold voltage [40]. As the voltage at the source respectively drain nodes of the switches is also the common mode voltage of the opamp input this topology needs an additional common mode control block [40].
Third, the *dc* current source of the differential input stage is omitted for operation from a low supply voltage. Omitting the current source is a trade-off between reduced balancing and gained voltage headroom.

2.8. Circuit Reconfiguration and Calibration

Modern integrated circuits designed in deep sub-micron CMOS technologies have a growing need of post-fabrication calibration and reconfiguration before they are delivered to a customer from an industrial background. Aside from the enormous demands on reconfigurability of software defined radios for multi-mode operation [34], even receiver circuits focusing on single-mode operation, like the GSM receiver presented in this work, are subjected to severe process technology variations that have to be compensated by reconfiguration. In addition deep sub-micron circuitry is more vulnerable to the effects of layout parasitics and difficulties in the profound modelling of the available devices. The shortened time to market with a reduced number of pre-product test-chip runs requires the designer to implement circuits with a considerable degree of flexibility and calibration mechanisms in order to overcome pre-tape-out uncertainties. In the limited time-to-market software simulation tools are not able to foresee all of the manifold effects e.g. emerging from SoC integration.
A typical receive chain of an integrated receiver will employ gain control in order preserve adequate signal reception under different scenarios of operation. Operating the whole receive chain in the high gain mode is necessary when the received signal strength is low and the best possible sensitivity is required. In the presence of strong blocking signals or strong wanted signals a receiver operating in high gain mode is sure to suffer from saturation effects as the dynamic range of FETs is shrinking and the supply voltage is reduced with technology scaling (cf. Section 4.3). Therefore gain control is exercised in various blocks of the receive chain.
This section will focus on gain control mechanisms and calibration of amplifying circuits and on means to adjust the bandwidth and centre frequencies of frequency selective circuits.



(a) Internal load switching with impedances and switches ($R_{ON} \rightarrow 0$).

(b) Internal load switching with active transistor loads ($R_{ON} \gg 0$).

Figure 2.14.: Switching between different load impedances.

Load Impedance Switching (Fig. 2.14). This mechanism controls the gain by changing the impedance value of the load of the amplifying transistor. The load can consist of impedances in parallel with individual switches connected in series. The switches need to be dimensioned with care. On the one hand the switches have to be sized large enough that their on-resistance is rendered insignificant compared to the impedance connected in series. On the other hand the parasitic capacitances associated with the physical dimensions of the switches in the non-conducting state have to be small enough in order to provide sufficient RF isolation. Alternatively active loads can be used. This bears the advantage that the switches do not need extra voltage headroom. The width of the active load transistors controls their on-resistance. The dimensioning of the active load transistors is subjected to trade-offs concerning their on-resistance, off-state RF isolation and *dc* current carrying capacity set by bias conditions of the amplifying device. If a high ohmic load impedance is needed the *dc* voltage drop across an active load is smaller than across an ohmic resistor carrying the *dc* bias current of the amplifying transistor. The voltage headroom saved by the active load transistor helps linearity whereas the inherent non-linear characteristic of the active load deteriorates linearity.

Signal Bypassing (Fig. 2.15). The most intuitive way of changing the transfer characteristic of a circuit block is to provide a shunt path. Instead of passing through a certain circuit block the signal is routed to another block in the receive chain. All available signal paths need to be separated by switches in order to prevent the unintended interaction of signals passing through the different paths. These switches, usually FETs are far from ideal switches. They are non-linear resistors. Neither the on-resistance is zero, nor is the off-resistance infinite. By the way, doubling-up a complete circuit block produces a large overhead e.g. in terms of die area. For low-cost solutions more refined approach of calibration and reconfiguration is needed.

Current dumping cascode (Fig. 2.16). The amplifying transistor and the cascode transistors are made up of bundles of transistors connected in parallel. The gate potential of the

cascode bundles can be controlled and so the path of part of the RF signal current is controlled. The current is either dumped or routed through the load. The more RF current is routed through the load the higher the voltage swing. This mechanism also controls the effective width and inherently the gain of the amplifying transistor. The disadvantage of the concept is that in all of the non-maximum gain modes bias current is simply dumped.

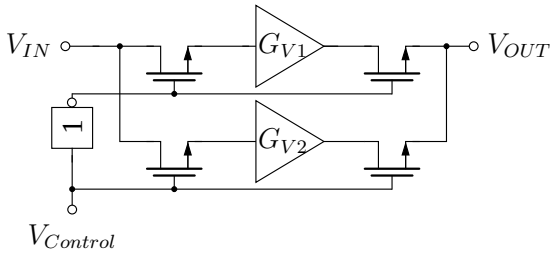


Figure 2.15.: Signal Bypassing.

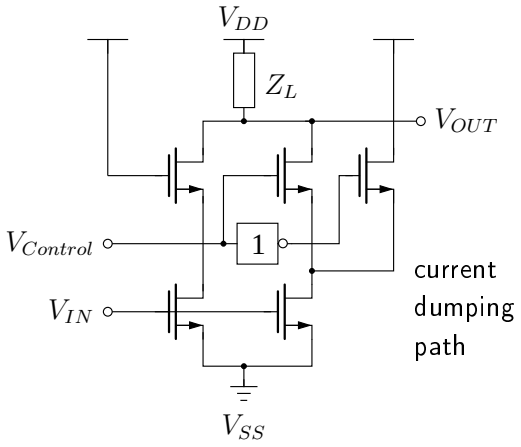


Figure 2.16.: Current dumping cascode.

Output swing divider (Fig. 2.17). A voltage divider is applied to the load impedance of an amplifying transistor. Controlled switches route the full or reduced voltage swing to the output of the circuit block. The amplifier circuit itself always works in high gain mode. The benefit of the lower gain is in the relaxed linearity requirements for the succeeding stages.

LC-Tuning (Fig. 2.18). The resonant frequency of circuits that utilise LC tanks as load impedances can be tuned by placing capacitor arrays in parallel to the load inductor. This technique is especially popular for tunable oscillators. A switch in series to the tuning capacitance will reduce the quality factor of the resonant circuit. The same restrictions as mentioned before apply concerning the use of CMOS switches in RF circuits.

RC-Tuning (Fig. 2.19). The frequency characteristics of filters are often ruled by a product of resistor and capacitor values. Thus the effects of process technology variations can be compensated by either adjusting the resistor or the capacitor value. A straight forward approach for a configurable low-pass filter is depicted in Fig. 2.19. Here the resistance value is tuned. Beware that in this example not only the low-pass characteristic but also the gain of the active filter is affected by a change of the resistor value. When faced with the choice between switching the resistance and/or the capacitance value the decision depends on individual implementation. Different absolute values of the elements to be shunted or connected in series, the die area consumption of the additional elements, the susceptibility of the different alternatives to parasitic effects etc. demand an individual solution.

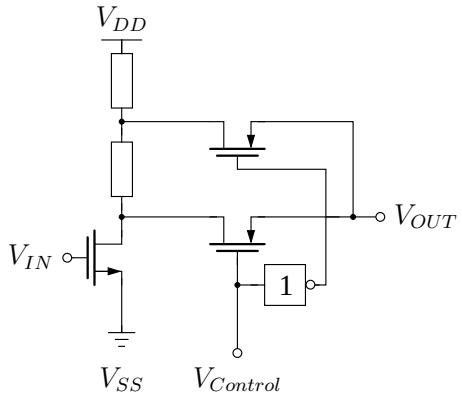


Figure 2.17.: Voltage divider for the output voltage swing.

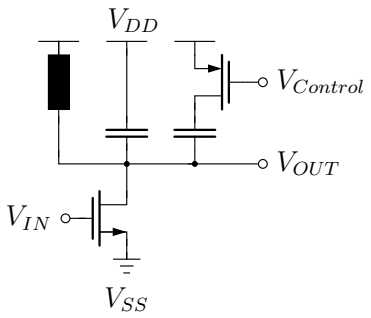


Figure 2.18.: LC resonant circuit tuned by capacitor array.

Conductance-Trimming (Fig. 2.20). Conductance-trimming is also sometimes referred to as R-trimming. In order to compensate for the process technology variation of the sheet resistance on chip, circuits that are performance sensitive to the absolute value of a resistors e.g. a differential amplifier stage can use tunable resistor arrays in order to calibrate these resistors. During front-end testing a defined bias current respectively bias voltage is fed to a reference resistor. The voltage drop across the resistor respectively the current flowing through the resistor is measured and burned into a control logic. The information is translated into a binary weighted bit word and distributed on chip to the circuit blocks. There the bit word controls a set of switches that adjust the resistance value of interest. With a bit word of e.g. n binary weighted bits and resistance values in the switching matrix it is possible to adjust resistance values within a range of $\pm(2^n/2)$ percent in 1% steps. Best accuracy is achieved if the resistor matrix is made up of resistors identical to the reference resistor. This minimizes the pairing errors due to e.g. different connection metalisation resistances related to different numbers of contact vias in the physical implementation of the resistors. The implementation of resistormatrix instead of a single fixed resistor consumes additional die area. The same restrictions as mentioned before apply concerning the use of CMOS switches in RF circuits.

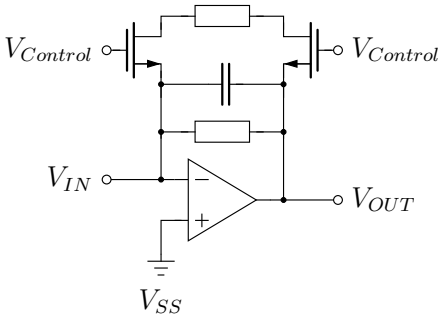


Figure 2.19.: Adjustment of a system $\tau = RC$ time constant by exemplary adjusting the resistance value.

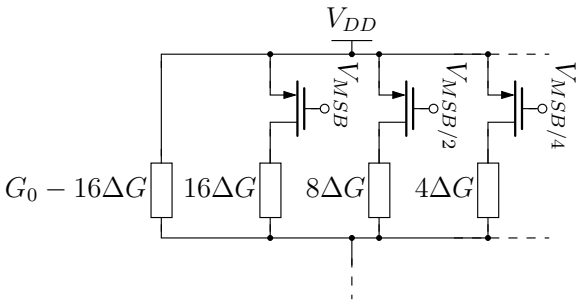


Figure 2.20.: Conductance trimming for a resistor.

Adjustments of Bias Settings. Last but not least adjustable bias settings (reference voltages and bias currents) are a popular means to compensate minor performance variations after the chip is fabricated at the cost of an increased complexity of the bias network.

In general it is preferable to design a chip that works without reconfiguration during front-end or back-end testing. These kinds of testing increase the production costs of a chip especially in mass production. However a reduced time-to-market, the complex nature of SoC integration and sub-micron process technology variations can justify post-fabrication configuration and calibration costs. During the evaluation of testchip designs a high post-fabrication configuration potential of components offers valuable flexibility to the RF designer and reduces the need for additional testchip runs.

3. The GSM System and its Catalogue of Requirements for the Receiver Front-End

As discussed in Chapter 1 GSM is the most popular standard for mobile wireless communications around the globe today. It is a circuit-switched mobile communications standard optimized for constant data rates and has been the first fully digital standard of the second generation of mobile communication networks.
In 1982 the Groupe Spéciale Mobile (GSM) took up the task to develop a Pan-European standard for mobile communications. As a result the standard definition for GSM900 was agreed on and published in 1990. One year later, 1991, the definition for DCS1800 (Digital Cellular System) was settled. Another year later, in 1992, the first commercial GSM nets in Germany (D-net and E-net) have been launched.
Stepping from the first analogue generation (1G) to the digital domain for 2G offers several advantages. By the means of digital information theory it is possible to exploit the limited bandwidth available much more efficiently. Additionally, error checking has been incorporated in the coding of the transmitted data.
Besides, the digital handsets emit significantly less power than their analogue counterparts and thus preserve a pre-longed time of service despite being operated from smaller battery cells. Another benefit of the reduced power dissipation is that the cell size of the cell based mobile network could be reduced. This allows for more cells in a given area. The number of cells in turn is linked to the capacity of a mobile network.
A variety of new digital services like Short Messaging Service (SMS) or E-mail, to name the most prominent, became available for the users of mobile handsets with the emerging digital mobile communication.
The main drawback of the digital solution is its limited range. The decay curves for digital transmissions are steeper than for analogue transmissions. The number of base stations in less populated areas has to be increased beyond capacity considerations.

3.1. The GSM Standard

Most of the GSM specifications relevant for the design and implementation of an analogue receiver front-end are given in [39]. However, a more intuitive introduction to the GSM standard definitions is given in [58]:
GSM coordinates frequency division duplexing (FDD) and time division multiple access (TDMA). The available frequency band is split into to a frequency range for upstream from the handset to the base station (uplink) and one for downstream from the base station to the handset (downlink). The duplex spacing between transmit and receive for e.g. GSM900 is $f_{DS} = 45\,\text{MHz}$. Each frequency range carries a number of channels that are spaced at $\Delta f = 200\,\text{kHz}$ distance [39]. The carrier frequencies transport eight time-divided channels. Each time frame is $t_{TDMA} = 4.615\,\text{ms}$ long. The time frames in turn are subdivided into eight timeslots [22]. The 156.25 bits in a times-

lot are transmitted in form of bursts of $t_{BURST} = 15/26\,\text{ms}$ in length (cf. Fig. 3.1). Table 3.1 gives an overview about the commercially used GSM frequency bands that are in the focus of this work.

As the transmit and receive operation are separated by three time slots it is possible to use a

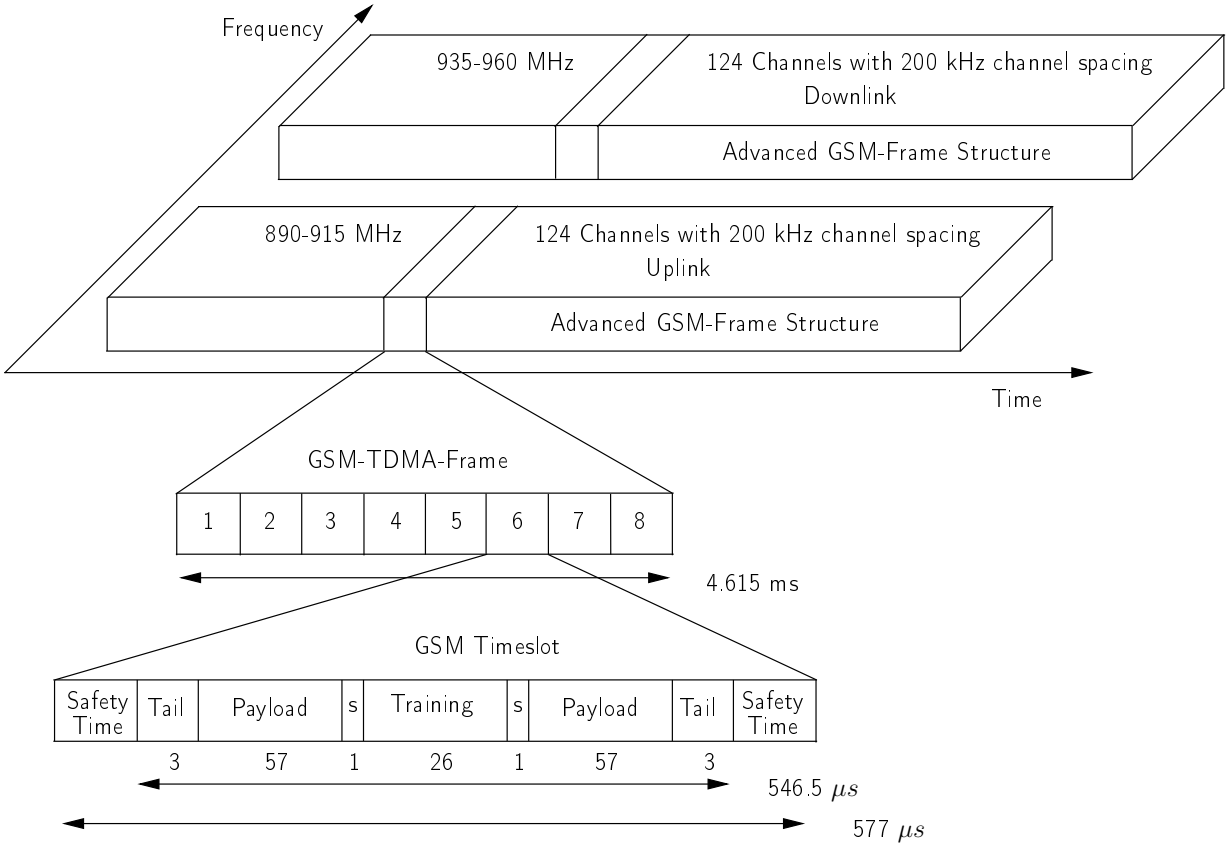


Figure 3.1.: Frequency division duplex and time division multiple access for GSM900 [58].

single antenna for the transmit and the receive operation.

In order to increase the immunity to interference the frequency pair for uplink and downlink can be changed periodically with a rate of $217\,\text{s}^{-1}$. This procedure is called frequency hopping [22].

The gross data rate is about $r_{GR} = 156.25\,\text{bit}/(15/26 \cdot 10^{-3}\,\text{s}) = 270.833\,\text{kbit/s}$ for every timeslot. The resulting data rate for a time frame t_{TDMA} is $r_{TDMA} = r_{GR}/8 = 33.9\,\text{kbit/s}$. After subtracting the bits needed for synchronisation of the time frame, user specific channel controlling and channel coding, a net bit rate of $r_{NET} = 13\,\text{kbit/s}$ is effectively left for data transmission (in case of voice data).

The modulation type for GSM is gaussian minimum shift keying (GMSK). GMSK is a digital phase modulation with a constant amplitude that codes one bit per symbol.

The envelop delay determines the theoretical maximum range for GSM. If the delay is too large a transmitted burst is not received in the appropriate timeslot on the other end. In order to compensate for delay, certain bits, the timing advance, are used to tell the transmitter to send its burst prior to the assigned timeslot. The timing advance can take values from 0 to 63. These values directly correspond to multiples of the time spend for transmitting one bit $T_{BIT} = 1/r_{GR}$. If the timing advance takes its maximum value of 63, the burst is transmitted a complete TDMA

Table 3.1.: Frequency table for the most anticipated commercial GSM frequency bands [58], [39].

Name	Uplink MHz	Downlink MHz	Region	Comment
GSM850	824-849	869-894	America	sometimes referred to as GSM800
GSM900	876-915	925-960	Africa, America, Asia, Australia and Europe	includes EGSM and PGSM
DCS1800	1710-1785	1805-1880	Africa, America, Asia, Australia and Europe	sometimes referred to as GSM1800
PCS1900	1850-1910	1930-1990	America	sometimes referred to as GSM1900

time frame before the intended reception (accounting for the time it takes to travel back and forth along the channel). For an electro-magnetic wave travelling at the speed of light the calculations limit the theoretical range of transmission between handset and base station to about 35.4 km. In urban areas this range is often reduced to a few hundred meters due to multi-path fading.

3.1.1. Enhancements of GSM

GPRS is classified as 2.5G. It is an extension to 2G GSM. The data transfer is organised packet-switched instead of circuit-switched and offers additional services like Multimedia Messaging Service (MMS) and Internet communication services. Due to the packet-switched nature of GPRS it is possible for multiple users to share the same transmission channel. Furthermore it is possible to utilise several timeslots in parallel for one user if the net load is low. GPRS has been initially introduced in 2003 in Northern America. GPRS requires a higher signal to noise ratio for proper transmission compared to GSM.
Another enhancement of GSM is EDGE (Enhanced Data Rates for GSM Evolution), also referred to as enhanced GPRS (EGPRS). Although it is technically a 3G standard it is often classified 2.75G. The main difference between EDGE and its predecessors is the additional modulation scheme 8-PSK (eight phase shift keying). 8-PSK enables data transfers of three bits per symbol and thus higher data rates. As with GPRS, EDGE can adapt the modulation and coding scheme to the quality of the transmission channel. The benefits are higher data rates and more robustness towards interferers. In fact the theoretical maximum data rate can be as high as 473.6 kbit/s for 8 timeslots.

3.2. Interpretation of the GSM Specifications

All of the building blocks of the receiver front-end need to be specified in terms of sensitivity, gain, linearity and power consumption. In order to derive the design specifications for the individual blocks of the receiver front-end it is necessary to take a closer look at [39] first. Starting from the dynamic range required for a GSM receiver in a commercial handset (also referred to as

mobile station (MS)), a system budget will be developed. The system budget sets performance requirements for the cascaded circuit blocks of the proposed receiver.
Note that it is common practice in [39] to name a bit error rate (BER) or a frame erasure rate (FER) value that is to be met in a certain scenario. These error rate values have to be interpreted before detailed specifications for the analogue circuit blocks can be derived.
Generally most of the standard definitions for the four targeted GSM bands coincide e.g. in terms of blocking performance. Exceptions for a particular frequency band will be covered in the final block specifications (Section 3.4.2), but it is not in the scope of this work to point out all particularities in detail. A general overview will be given and the information needed to develop the block specifications is presented.
In addition to the official performance requirements derived from [39] in Section 3.4 a final block specification will contain high-performance requirements that have been agreed on in cooperation with a business partner or customer from an industrial background. In order to be capable of competing on the market the final target block specifications (Section 3.4.2) will be harder to meet than the first set of reference specifications derived from the official GSM testcase scenarios. Section 3.2 (and later Section 3.4) do not raise a claim of completeness of GSM receiver front-end specifications. These sections merely illustrate how an exemplary set of specifications is derived from the testcase scenarios given in [39].

3.2.1. The Reference Sensitivity

[39] defines the reference sensitivity level as the minimum signal level at the input of the receiver for which a given performance e.g. $BER \leq 10^{-4}$ is met. For a typical mobile handset this minimum reference sensitivity level is $P_{RS} = -102\,\text{dBm}$. The BER or FER value that is tolerated depends on the type of channel. For speech channels an $FER \leq 1\%$ is typically tolerated.
From this reference sensitivity level a maximum noise figure can be calculated for the analogue part of the receiver with

$$NF_{MAX} = P_{RS} - 10\log(kT \cdot BW/(1\,\text{mW})) + (\text{C/N})_{\text{RXO}}, \tag{3.1}$$

where $kT \cdot BW$ is the available noise power at a power-matched receiver input in the signal bandwidth BW and $(C/N)_{RXO}$ is the carrier to noise ratio (in dB) needed at the analogue receiver output for demodulation with a given FER.
With $P_{RS} = -102\,\text{dBm}$, $T = 273\,\text{K}$, $BW = 200\,\text{kHz}$ and $(C/N)_{RXO} = 9\,\text{dB}$ we obtain

$$NF_{MAX} = 9.8\,\text{dB} \tag{3.2}$$

at room temperature for GMSK modulation [51].
The authors of [21] suggest a static $NF_{MAX} = 7\,\text{dB}$ for GSM900 including a margin of 3 dB.

3.2.2. Blocking Scenarios

In [39] manifold blocking tests are given for a commercial GSM receiver (cf. Fig. 3.2 - Fig. 3.6). The typical test set-up consists of 'a useful signal [the wanted signal], modulated with relevant supported modulation (GMSK or 8-PSK), at frequency f_0, 3 dB above the reference sensitivity level' and a 'continuous, static sine wave signal [the blocking signal] at a level as' and at a

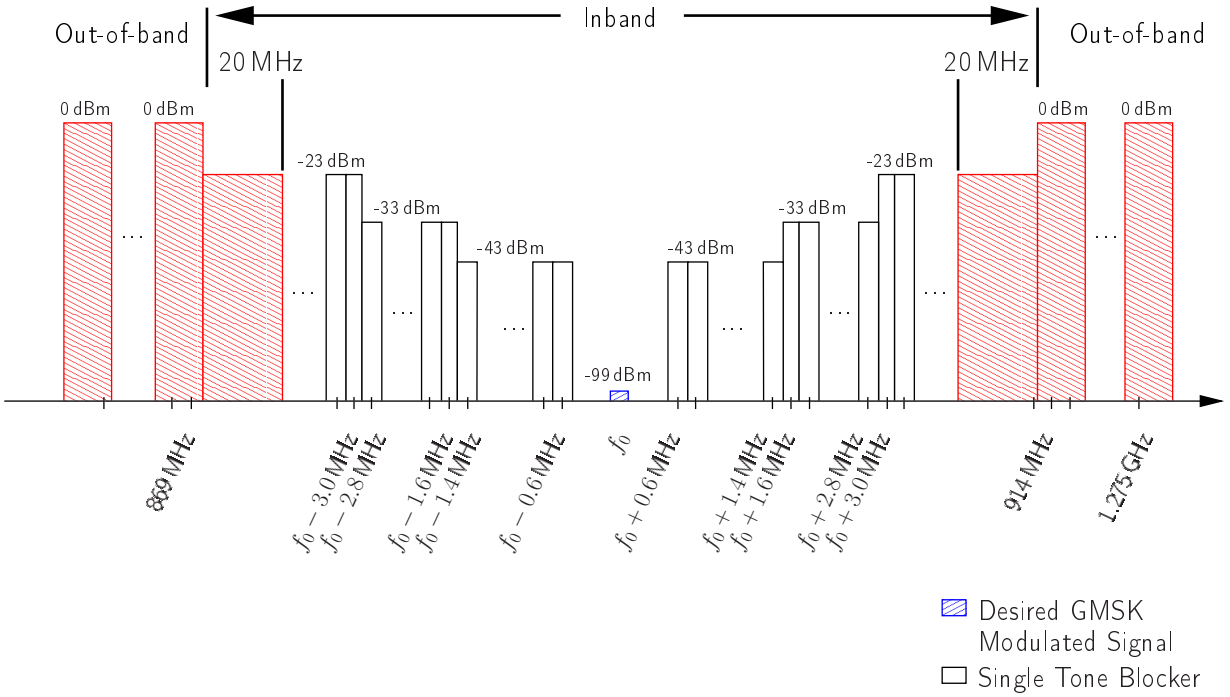


Figure 3.2.: Blocking profile for GSM850 [39].

frequency offset (discrete increments of 200 kHz) as specified in [39] that are simultaneously applied to the receiver input. The receiver must be able to demodulate the wanted signal with a certain maximum error rate. Two kinds of blocking signals are distinguished, in-band-blockers and out-of-band blockers, according to their position in the frequency spectrum. For a set of user-assigned frequencies the blocking requirements are relaxed. The frequencies in this set are called the spurious response frequencies.
This section exemplary elaborates on the blocking scenario for a GSM900 mobile station receiver (cf. Fig. 3.3). The GSM900 blocking scenario (EGSM not included) differs from the standard blocking scenarios that are similar for the four GSM bands of interest in the way that there is an extra frequency range of 10 MHz (guardband) to the lower end of the band and a range of 20 MHz beyond the upper end of the band that extends the in-band frequency range for 3 MHz-blockers. The signal level for all out-of-band blockers is 0 dBm. Passing the sensitivity test when the 3 MHz blocker is applied, is usually considered the most difficult blocking specification to meet [51].

3.2.3. Second Order Distortion

The author of [29] identifies four sources of second order distortion in wireless receivers:

- RF to LO leakage in down-converters. This effect describes the phenomenon of coupling from the mixer LO input signal to the RF signal input. The leakage signal mixes with itself thus generating spectral components at dc.

- Common-mode excitations. Especially circuit blocks that perform a single-ended to differential conversion e.g. BalUns are likely to introduce a non-zero common mode gain to the receive chain.

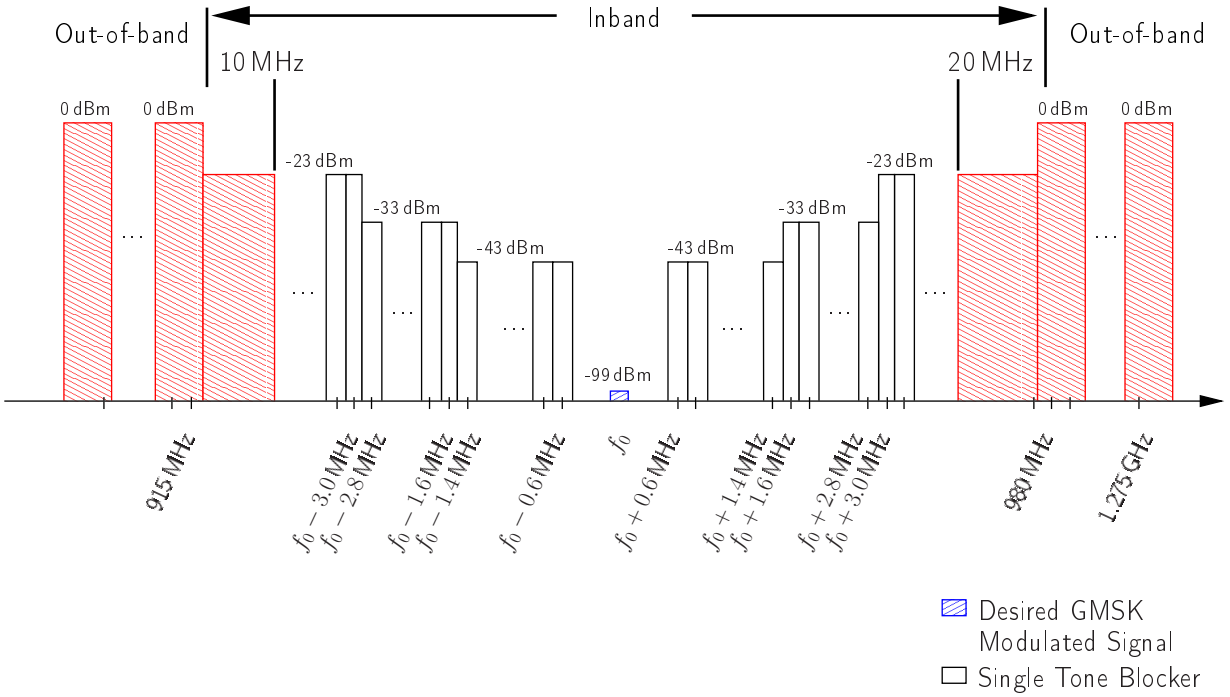


Figure 3.3.: Blocking profile for GSM900 [51].

- Device non-linearity. Due to the quadratic nature of the transfer function e.g. of a MOSFET second order spectral components are generated when non-linear devices are used in circuit blocks. Second order non-linearities give rise to second order spectral harmonics.

- Device mismatch in the mixer circuit. Whereas device mismatch in the mixer input stage (transconductance stage) is considered insignificant, device mismatch in the switching quad of a mixer e.g. variations of threshold voltage is indicated as a potential source of distortion but is not investigated in detail.

Especially for integrated direct conversion receivers second order distortion is a major problem. These receivers suffer from the lack of appropriate channel filtering [50], [29].
The second order intermodulation effects are characterised in terms of the second order intercept point (IP_2). In [39] two test scenarios are mentioned that determine the necessary IP_2 for a GSM receiver.
One set of these scenarios is the blocking scenario described above (cf. Section 3.2.2). The authors of [51] consider the *dc* component generated by the 3 MHz blocker of the DCS1800 specification most challenging for the baseband blocks of a receiver. The basic idea for calculation of the IP_2 is that a circuit block can be characterised by the use of a non-linear transfer function $y(t)$ (cf. (2.25)). In order to guarantee that the reception of the wanted signal is negligibly degraded by the generated even order intermodulation products it is defined that the power of the second order distortion products has to be at least 15 dB below the power of the desired signal. This results in the following equation for IP_2 [51]:

$$IP_2(\text{dBV}) = 2P_{BL}(\text{dBV}) + 9\,\text{dB} - P_{SIG}(\text{dBV}). \tag{3.3}$$

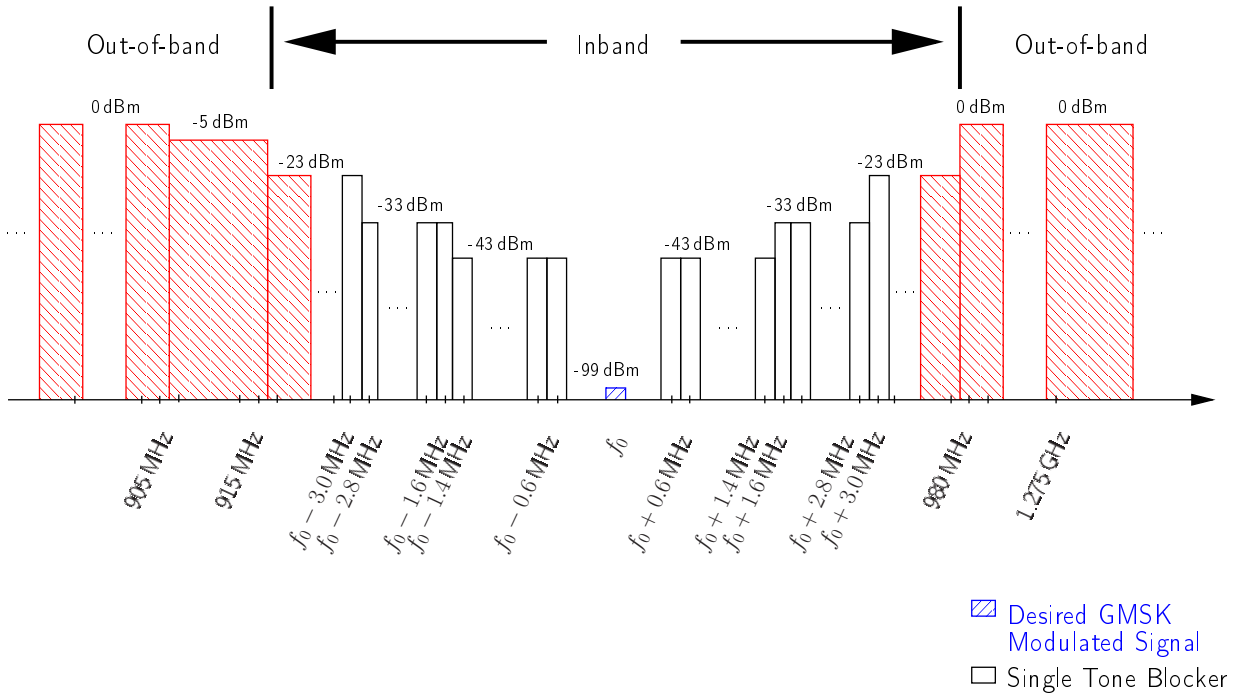


Figure 3.4.: Blocking profile for EGSM [51].

Table 3.2.: Values for the IIP_2 required for a GSM MS receiver according to formula (3.3) given in [51]. No front-end frequency selectivity is considered.

P_{BL} [dBm]	P_{SIG} [dBm]	IIP_2 [dBm]	comment
−23	−99	62	e.g. GSM850 and GSM900 MS
−26	−97	54	e.g. DCS1800 class 1 or 2 MS
−26	−99	56	e.g. DCS1800 class 3 MS

In (3.3) we assume that the desired signal and the second order component see equal gain and no filtering in the receiver front-end. Table 3.2 lists IIP_2 values for GSM receivers calculated according to (3.3) assuming the receiver input is power matched to a 50 Ω source impedance. If we follow the development of (3.3) in [51] attentively, we notice that starting from the blocking scenario (single-tone test case) the formula is adapted to a two-tone intermodulation test case by applying a corrections term of 6 dB.

In order to estimate the IP_2 for the baseband blocks of an integrated GSM receiver, for which the IP_2 specification is considered most challenging, the power gain of the analogue front-end blocks has to be added to the IIP_2 values given in Table 3.2.

The author of [12] calculates an $IIP_2 = 57$ dBm for a hypothetical two-tone interferer test case with power levels of $P_{SIG} = P_{RS}$ and $P_{INT} = -29$ dBm handling the interferer like a two-tone interferer instead of a TDMA AM interferer.

Authors like [29], [12] or [21] focus on the amplitude modulation (AM) suppression characteristics mentioned in [39] in order to determine the IP_2 performance relevant for a GSM MS receiver. This notion is backed by the fact that a simple two tone-interferer test case where static sine

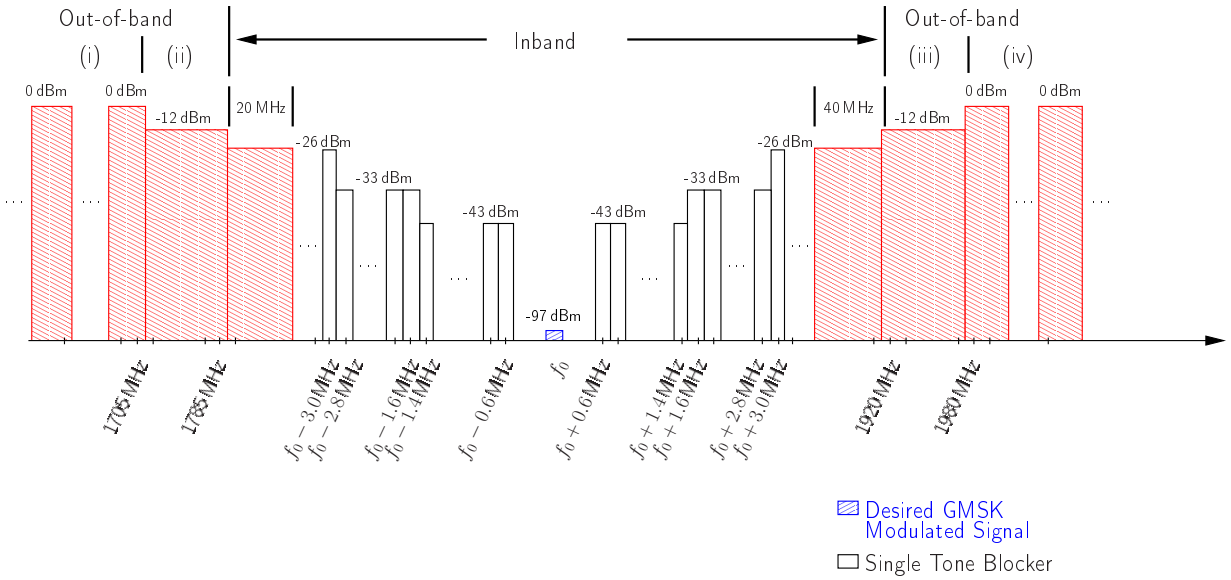


Figure 3.5.: Blocking profile for DCS1800 [51].

waves are input to the receiver generate a static offset. By the means of offset compensation circuits for baseband blocks this offset can be rendered to insignificance [29]. If the static offset is of moderate impact with regard to the input range of the baseband filters or the ADC it can be ignored in the analogue domain and be filtered very efficiently in the digital domain.
For the AM suppression test case a modulated wanted signal at the frequency f_0 3 dB above the reference sensitivity level and a GSM modulated TDMA signal at frequency f and a power level of $P_{INT} = -31\,\text{dBm}$ are applied simultaneously to the receiver. The interferer is one timeslot active and 'at least two channels separated from any identified spurious response'. Both, interferer and wanted signal have a frequency offset of $|f - f_0| \geq 6\,\text{MHz}$ which is an integer multiple of 200 kHz. The transmitted bursts shall 'be synchronised to but delayed in time 61 and 86 bit periods relative to the bursts of the wanted signal' [39]. The fact that the interferer transmits in bursts only and is not a static signal forestalls attempts of a dc offset compensation for the AM suppression test.
From link simulations it is determined that a delay of 74 bit times is the worst case scenario for the delay of the interferer burst. Furthermore it is reported in [29] that a channel to interferer ratio $(C/I)_{BB} = 5\,\text{dB}$ at baseband is sufficient in order to maintain the required error rate performance. Using (3.4) an $IIP_2 = 46\,\text{dBm}$ is estimated ($P_{SIG} = -99\,\text{dBm}$).

$$IIP_2 = 2P_{INT} + C/I - P_{SIG} \tag{3.4}$$

In [12] a slightly different approach is developed for estimating a necessary $IIP_2 = 46\,\text{dBm}$ based on the assumption that a channel to noise and interferer ratio $C/(I+N) = 9\,\text{dB}$ is needed in the receiver front-end. The issue of adapting the requirements for the AM suppression test case with modulated blockers to a two-tone interferer test case which is common practice in measurement laboratories is addressed by the use of a correction term.
The author of [21] states that in order for a receiver to pass the GSM AM suppression test an $IIP_2 \geq 45\,\text{dBm}$ is needed.

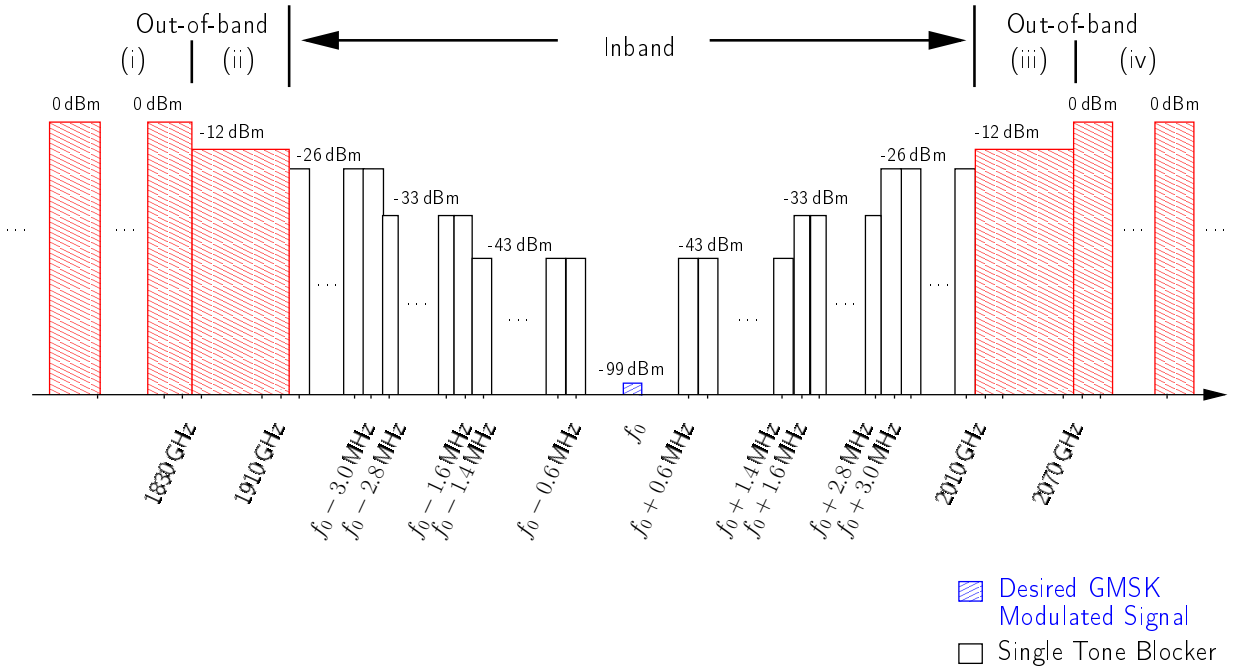


Figure 3.6.: Blocking profile for PCS1900 [51].

3.2.4. Third Order Intermodulation Test Cases

In the third order intermodulation test case two interference signals, a static sine wave at frequency f_1 and a modulated signal at frequency f_2, with a power level of P_{INT}=-49 dBm and a modulated wanted signal at frequency f_0 3 dB above the reference sensitivity level are applied to the receiver input simultaneously. The receiver is required to maintain a $BER \geq 10^{-3}$ equivalent to $(C/I)_{RXO} \geq 9$ dB. The frequency offset between the unmodulated interferer and the modulated interferer is $|f_1 - f_2| = 800$ kHz and $f_0 = 2f_1 - f_2$ respectively.
The basic idea for deriving the required receiver 3rd order intercept point IP_3 is that the intermodulation product IM_3 generated by the two interference signals shall not violate the sensitivity requirement for the receiver. Assuming that the thermal noise at the receiver output and the 3rd order intermodulation product IM_3 are uncorrelated, the presence of both components must not raise the noise and/or distortion floor higher than the level required for appropriate demodulation (cf. Fig. 3.7).
For a desired signal of $P_{SIG} = -99$ dBm ($= P_{RS}$+3 dB) at the antenna, a required overall carrier to noise ratio $(C/(I+N))_{RXO} = 9$ dB and a rise of the input referred noise and/or distortion floor by 3 dB (distortion and noise floor at equal levels and both referred to the input) the maximum input referred noise level allowed P_{NMAX} for either noise and/or distortion is

$$P_{NMAX} = P_{SIG} - (C/(I+N))_{RXO} - 3\,\text{dB} = \text{IM}_3 = -111\,\text{dBm}. \tag{3.5}$$

With (3.5) the $IIP3$ can be calculated to be

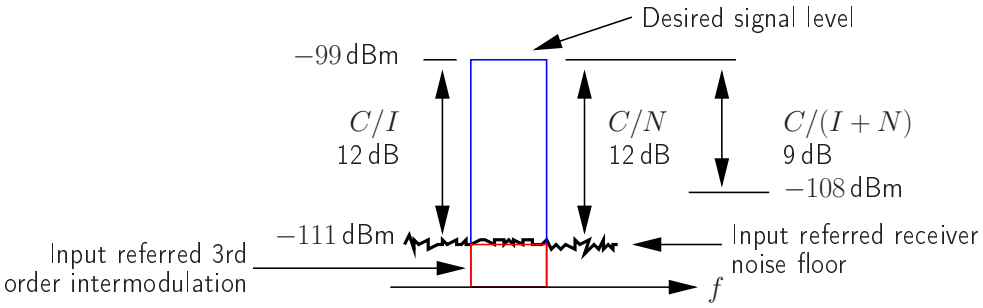


Figure 3.7.: Maximum allowed noise and distortion floor with regard to the 3rd oder intermodulation test case [51].

$$IIP_3 = P_{INT} + \frac{P_{INT} - IM_3}{2} = -18\,\text{dBm}\ [51]. \tag{3.6}$$

Neglecting the rise of the overall noise floor due to the contributions of uncorrelated thermal noise and intermodulation products and assuming a $C/I \geq 8\,\text{dB}$ sufficient for demodulation the author of [21] approximates an $IIP_3 = -20\,\text{dBm}$ necessary for GSM systems.

3.3. Receiver Topologies

3.3.1. Heterodyne Receiver

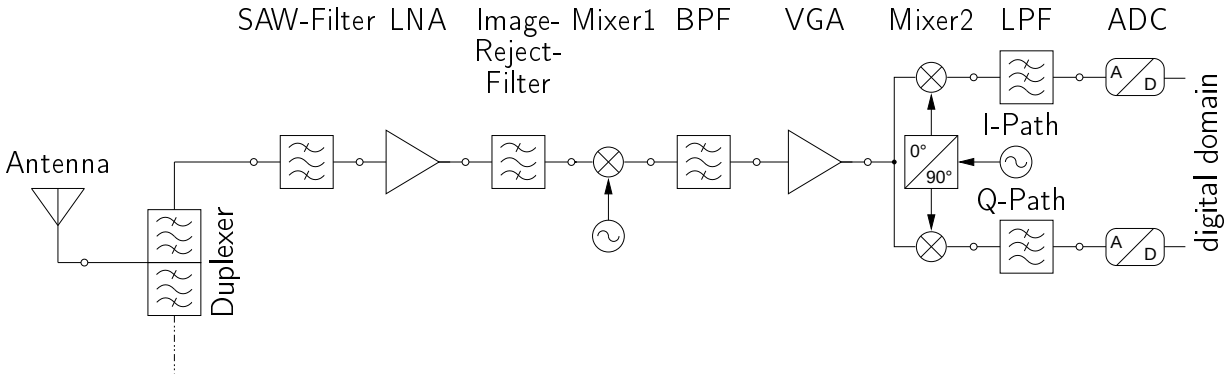


Figure 3.8.: Simplified heterodyne quadrature receiver schematic.

The heterodyne receiver concept (cf. Fig. 3.8) has dominated receiver topologies for wireless communications in the past. The wanted signal is down-converted to an intermediate frequency (IF) in a first mixer stage before the demodulation and conversion to baseband in a second quadrature mixer stage. The channel selection is performed on the intermediate frequency by an IF filter with a fixed frequency characteristic. Before the first down-conversion another filter is needed. The filter is referred to as image reject filter. Assume an unwanted signal with the same distance in frequency from the local oscillator (LO) signal as the wanted RF signal but on the far side of the LO signal. The down-conversion process shifts the unwanted signal to the same spectral frequency as wanted RF signal. The unwanted signal is referred to as image signal (IM)

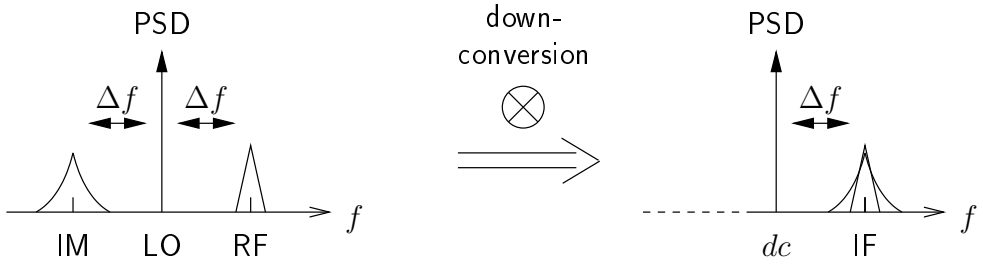


Figure 3.9.: Image frequency problem without an image-reject-filter prior to the down-conversion.

in literature (cf. Fig. 3.9) [47]. Before the first down-conversion the image signal needs to be eliminated otherwise it will overlap with the wanted signal at the IF. For this purpose a highly selective band-pass filter (BPF) is inserted after the LNA into the receive chain.

The lower the intermediate frequency chosen, the closer the image frequency is to the wanted RF signal. As a result an image-reject filter with a high quality factor Q is needed. In fact the required quality factor is so high that it is not possible to integrate the necessary filter elements e.g. capacitors. The necessity of external elements makes this filter an expensive component of the heterodyne receiver. In addition to the external SMD components the package of the integrated circuit (IC) needs to be larger and needs to provide extra pins in order to connect the external components. Thus the external BPF is not attractive for cheap mass-production. Choosing a large IF on the other hand relaxes the image-reject filter requirements but requires a channel selection filter with a higher selectivity as the channel bandwidth is fixed while the centre frequency is enlarged.

Another consequence of the off-chip implementation of the BPF is that the LNA needs to be able to drive a load as low as the $50\,\Omega$ input impedance of the filter. Furthermore, the output of the LNA has to comply to a mandatory power-match to the filter input [25].

As the split of the signal path into an in-phase (I) path and a quadrature (Q) path takes place in the quadrature mixer stage shortly before the ADC in the receive chain the mismatch between both paths does not impose severe design constraints on the receiver.

Although favourable because of immunity to interferers and selectivity heterodyne receivers are not the topology of choice for modern wireless receivers as they are not suitable for cheap monolithic integration [12].

3.3.2. Zero-IF or Direct-Down-Conversion Receiver

Besides, zero-IF receiver, the topology in Fig. 3.10 is known by the name of direct-down-conversion receiver in literature. Another name that is often used simultaneously is homodyne receiver. Classically the term homodyne has been used for coherent reception only [47].

The zero-IF receiver converts the RF wanted signal directly to the baseband. The frequency of the LO used for down-conversion in the mixer is equal to the carrier frequency of the wanted signal. The wanted frequency spectrum is down-converted to around *dc*. Whereas double-sideband AM signals can be down-converted by simple mixers, frequency modulated (FM) or quadrature-phase-shift-keying (QPSK) signals need quadrature mixers. This is due to the fact that the positive and the negative part of the input spectra overlap after down-conversion. In order to separate both parts which may carry different information quadrature outputs are needed [47].

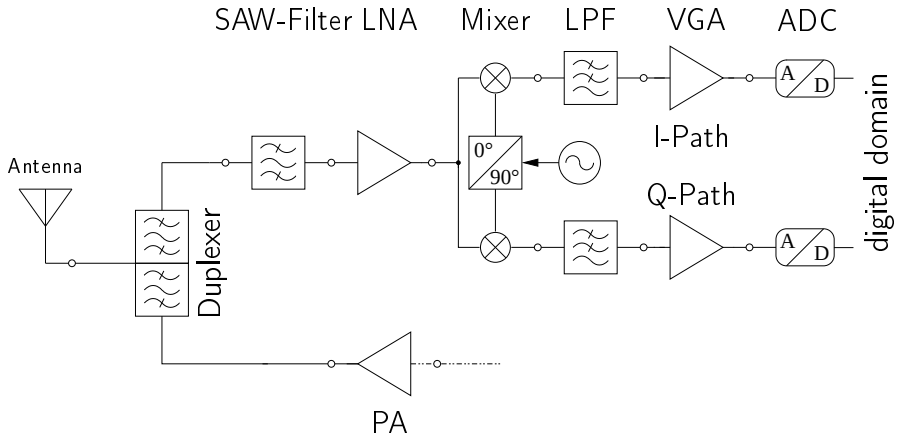


Figure 3.10.: Simplified zero-IF quadrature receiver schematic.

At first glance the direct conversion receiver looks intriguingly simple. No time-consuming frequency planing is required. The down-conversion process is straight forward. The image frequency problem mentioned in Section 3.3.1 is inherently eliminated in the zero-IF concept as there is no image frequency. Consequently no expensive highly selective image rejection bandpass filter is needed. Instead an active low-pass filter (LPF) which can be integrated with the receiver front-end will do the channel filtering. The monolithic integration of the LPF into the front-end bears the advantages of a free choice for the LNA output impedance and imposes no power-matching constraints between the integrated front-end blocks. The absence of an external image-reject filter makes the receiver smaller and cheaper to manufacture which is a key issue for high volume production. If the dynamic range of the ADC allows for it, the LPF just needs to perform a coarse selection. Proper channel filtering can be implemented very effectively in the digital baseband. Furthermore, the ADC can be operated at low sampling frequencies due to the direct conversion to *dc*. This usually goes along with significant power savings compared to ADCs operating at higher frequencies.
Summing up all the advantages in favour of the zero-IF receiver it seems a simple low-power low-cost receiver topology best suited for SOC implementation. Although the concept of a direct conversion receiver was introduced in 1924 it has become popular for mobile radio applications no sooner than the late 1990s. Still it is sometimes considered more suitable for *SiGe* or BiCMOS process technologies than for standard CMOS process technologies [21]. However, direct conversion receivers implemented in industrial CMOS technologies are in the focus of intense research because of the superior cost-effectiveness compared to other more expensive process technologies [15].
One of the disadvantages of the direct conversion of the RF signal to *dc* is the degradation of the BB SNR due to flicker noise. In order to preserve the signal quality despite the presence of flicker noise the receiver needs sufficient gain before the BB (cf. (2.9)). State of the art direct conversion receiver front-ends accumulate about 20 to 30 dB of voltage gain in LNA and mixer. Increasing the gain in the first blocks of the receive chain challenges the linearity requirements of the receiver front-end blocks.
Other significant problems arise from *dc* offsets in the receive chain at BB (cf. Section 3.2.3). These offsets have several origins:

- LO self-mixing. The isolation between the RF signal input port of the mixer and the LO

signal port of the mixer is finite. A certain amount of the LO signal leaks to the RF input port. In the frequency conversion process a resulting *dc* component emerges. The same is true for leakage between the LO signal port and other input ports of preceding circuit blocks in the receive chain on chip because of substrate coupling. If the LO signal is fed externally there may also be coupling effects between bondwires [47].

- Interferer self-mixing. This phenomenon is similar to LO self-mixing but this time strong interferer signals leak from the LNA or mixer RF signal input port to the LO signal port of the mixer [21].
- Transmission self-mixing. In a full-duplex transceiver the PA transmission signal may leak to the receive LO signal input port of the mixer via substrate coupling and may leak via the finite duplexer isolation between receive and transmit path to the receive signal input port. The down-conversion generates unwanted self-mixing components at *dc* [21].
- Second order distortion. Second order distortion is a major problem for direct conversion receivers [29]. The second order harmonic of the RF input signal mixes with the second order harmonic of the LO signal in the mixer stage [21]. In addition it is possible for two strong interferers or an interferer with an amplitude modulation to cause in-band and *dc* components in the baseband blocks due to second order distortion effects.

The generated *dc* offsets may saturate the BB stages of the receive chain succeeding the mixer and thus prevent the amplification of the wanted signal. As the leakage signals and/or the interferers vary with time e.g. when the MS is moving the undesired *dc* offsets vary too. The most intuitive approach for getting rid of the *dc* offsets is to apply *ac* coupling or other high-pass filtering between the BB blocks. However, as the wanted signal has a frequency spectrum close to *dc* and may actually include a *dc* spectral component if the modulation is not *dc*-free, the filtering elements i.e. capacitance values required are unreasonably large. An ongoing calibration or offset-cancellation is a more adequate means. Especially TDMA systems like GSM with idle time slots qualify for calibration solutions like auto-zeroing [21],[47].
An LO signal leaking to the antenna port is not only a concern in terms of self-mixing in zero-IF receivers but also in terms of in-band emissions to other MS for receivers in general. Generally speaking, the allowable emission level for wireless MS ranges from -80 dBm to -60 dBm [21].
As mentioned before a direct-conversion receiver makes use of a quadrature architecture. The quadrature architecture implies an I and a Q path in the mixer stage and the succeeding BB stages. The signal processing in two separate paths can introduce amplitude and phase mismatch to the two signals. Especially the high gain of the BB blocks will amplify small mismatches. Careful design and layout of integrated circuits mitigates the mismatch issue which has been more significant in times of discrete receiver implementations rather than for monolithic implementations. As a rule of thumb an amplitude mismatch below 1 dB and a phase mismatch of less than 5° between I and Q path are acceptable in homodyne receivers according to the author of [47]. Self-evidently the amount of mismatch that can be tolerated depends on the modulation scheme used.

3.3.3. Conventional Low-IF Receiver

The author of [12] claims that the conventional low-IF receiver is a special kind of homodyne receiver. It has been developed in order to overcome the design challenges in terms of *dc* offsets, flicker noise and low-frequency distortion a classical direct conversion receiver suffers from. The

RF signal is down-converted to a frequency other than *dc* but lower than the IF of a heterodyne receiver in the first mixer stage. The low-IF receiver avoids expensive external image-reject filters prior to the first mixer and thus benefits from a low component count similar to that of the direct conversion receiver. According to [12] channel selection can be implemented in two ways:

- After the first (quadrature) down-conversion the signal is applied to a complex baseband filter e.g. polyphase (PP) filters (cf. Fig. 3.11). The demodulation usually takes place in the digital domain.

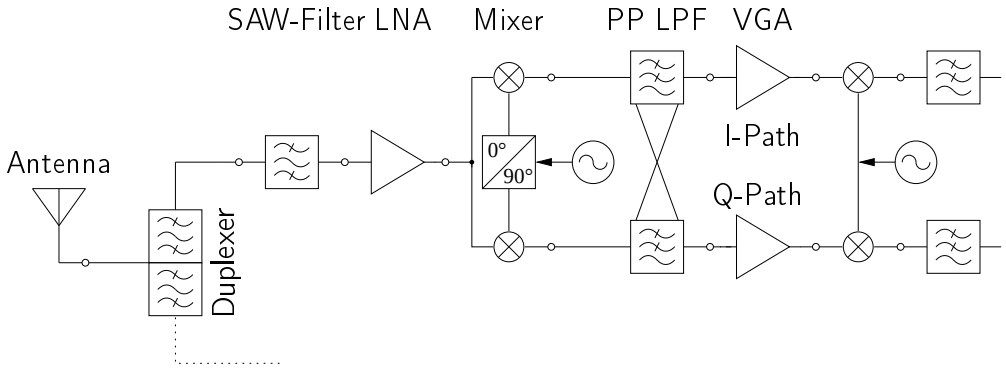


Figure 3.11.: Simplified low-IF receiver schematic with a complex bandpass filter [12].

- After the first (quadrature) down-conversion the signal is applied to real baseband filtering and then subjected to a mixer in Weaver or Hartley architecture with four multipliers which shift the complex spectrum in one direction only (cf. Fig. 3.12). This is done at the expense of an increased current budget.

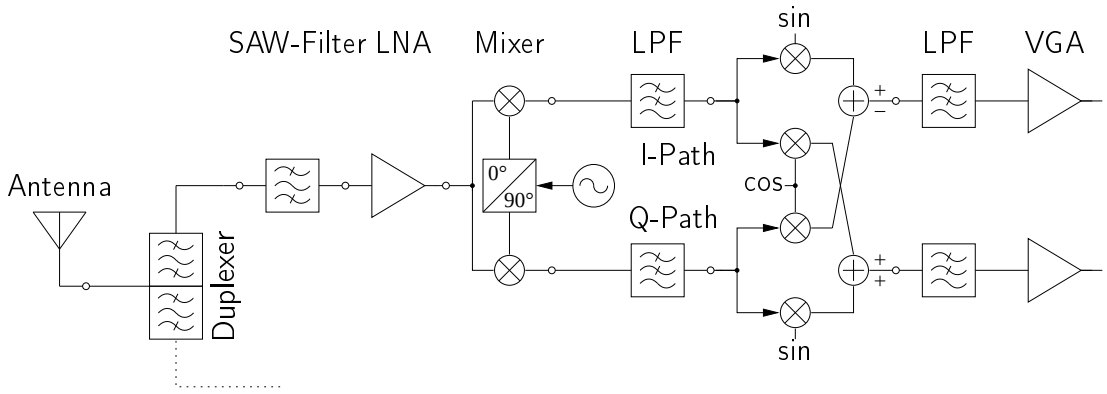


Figure 3.12.: Simplified low-IF receiver schematic with real baseband filter [12].

The principle of out-phasing of certain parts of the spectra in order to achieve sufficient image-rejection imposes high challenges on the I-Q balance in low-IF receivers. Besides, a channel selection in the digital domain demands high-performance ADCs because the wanted signal can be small compared to strong image signals [12].
The author of [43] describes the low-IF receiver topology as a cross-product of a homodyne and a heterodyne receiver. In an investigation of the differences between image-reject low-IF and

I-Q-based low-IF receivers the interference properties and filtering requirements with focus on Bluetooth applications are discussed. A trade-off between image-rejection and channel selectivity depending on the choice of the IF similar to the trade-off mentioned in Section 3.3.1 is observed. It is reported that in the case of sophisticated processing of the complex signal (cf. Fig. 3.13) the lower bound of the IF is only limited by ac-coupling or flicker noise constraints.

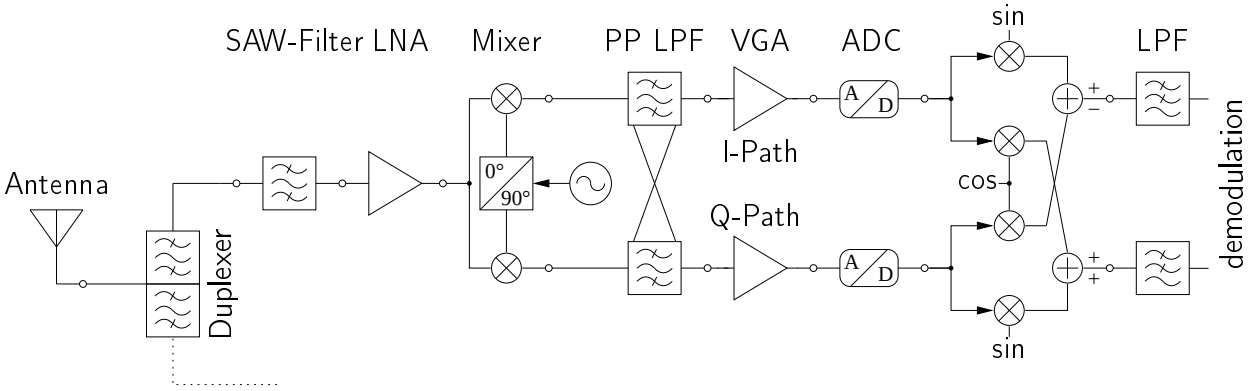


Figure 3.13.: Simplified low-IF receiver schematic [43].

3.3.4. Receiver Topology of Choice

With the focus on a low cost, low power solution for entry level phones the receiver topology of choice is the direct-conversion or zero-IF receiver. Although it imposes design challenges like handling and avoiding *dc* offsets or flicker noise for the baseband blocks, the low component count and simple architecture makes the zero-IF receiver very attractive for modern wireless receivers and monolithic SoC integration.
For the time being an external band selection filter is integral part of all three state-of-the-art receiver topologies introduced. As the image-rejection issue is inherently solved in the zero-IF approach, the concept for filtering is reduced to channel selection filtering. The frequency conversion of the received signal to *dc* enables the use of active LP filters for channel selection. Compared to BP filters e.g. PP filters which are required in the low-IF or heterodyne receiver approach the implementation of the LP filters is less complex in structure.
On the one hand the limited number of stages in the zero-IF architecture e.g. only one analogue mixer stage, eases the linearity requirements for the individual blocks in the receive chain. This is especially important with regard to the blocking scenarios of the GSM standard [39]. On the other hand the effects of second order distortion impose tough requirements on the IP_2 especially of a zero-IF receiver (cf. Section 3.2.3).
Last but not least this work aims to compare the performance of two receiver front-ends in a 130 nm and in a 65 nm standard CMOS technology respectively. As the given receiver topology in the 130 nm CMOS technology is a direct-conversion receiver it makes sense to investigate a direct-conversion topology in a 65 nm process technology for best comparison.

3.4. Specification of Circuit Blocks

3.4.1. System Link Budget

The goal of this system budget planning is to distribute the overall gain of a receive chain necessary for adequate reception on the individual circuit blocks in the receive chain while balancing the noise contributions of these circuit blocks. Depending on the modulation scheme that is used by a certain mobile communication standard, e.g. GMSK is used for standard GSM and 8-PSK for GSM EDGE, a certain SNR is required for demodulation with a given BER or FER.
In addition a system budget calculation helps to evaluate the contributions of individual circuit blocks to the overall non-linearity.
Be aware that the system budget calculations presented in this section can only cover an exemplary set of specifications. It is beyond the focus of this work to derive a complete set of specifications for a GSM receiver front-end.
In general, (2.9) can be utilised in order to approximate the total noise factor of cascaded noisy circuit blocks. The calculation involves the knowledge of the individual power gains of the cascaded blocks. Due to the difficulties in defining impedance levels in an integrated circuit defining a power gain introduces similar difficulties. The only well-defined impedance level is usually the input impedance of the receive chain respectively the input impedance of the LNA e.g. $50\,\Omega$. Thus we chose a different approach for calculating the noise contributions. Based on the assumption that the noise in the relevant frequency band is subjected to the same transfer characteristic as the wanted signal, an equivalent input noise source for every noisy circuit block can be defined and be referred back to the input of the receive chain. Assuming that the noise sources of the individual blocks are not correlated, the spectral noise density contributions in V^2/Hz add up along the receive chain. Furthermore, assuming that the noise bandwidth is equal to the signal bandwidth, an SNR before, respectively after, every circuit block can be calculated. Using (2.4) we can determine the cascaded NF after every block in the receive chain.
The calculation of the total IP_3 of the cascaded stages of the receive chain is straight forward using (2.32) when the IP_3s of the individual circuit blocks are given.
Table 3.3 gives specifications of the individual blocks in the receive chain, while Table 3.4 presents the performance of the cascaded receiver front-end blocks.
For the calculations presented in Table 3.4 a signal and noise bandwidth of $BW = 0.2\,\mathrm{kHz}$ is assumed for the receiver front-end. The thermal noise densities are assumed to be valid for an on-chip temperature of $T = 40^\circ\,\mathrm{C}$. The overall noise figure $NF = 7\,\mathrm{dB}$ is in accordance with Section 3.2.4 leaving a margin of almost 3 dB in order not to violate the requirements of [39] at higher temperatures and in order to account for process technology variations from nominal conditions.

3.4.2. A Refined List of Specifications

Table 3.4 lists system budget calculations based on a set of minimum requirements derived from [39] in the previous sections. For a company involved in the competition on the global market for mobile handsets it is desirable not only to fulfil these minimum requirements but to gain a performance advantage over competitors' products. While the noise figure $NF = 7\,\mathrm{dB}$ of the reference performance receiver in Table 3.4 indicates a sensitivity of about $\mathrm{P} = -105\,\mathrm{dBm}$, high-end receiver front-ends for GSM achieve much better sensitivities of e.g. $\mathrm{P} = -110\,\mathrm{dBm}$.
Table 3.5 lists GSM receiver specifications for a more advanced receiver front-end. These specifications have been agreed on with the project partner from an industrial background.

Table 3.3.: Reference specifications for the analogue receiver front-end that satisfy the performance requirements in [39].

BalUn Specification		
Input impedance	[Ω]	50
Output impedance	[Ω]	200
Voltage gain G_V	[dB]	6
Insertion loss NF	[dB]	2.0

LNA Specification		
Input impedance	[Ω]	200
Voltage gain G_V	[dB]	18
Input referred noise source	[nVrms/$\sqrt{\text{Hz}}$]	1
Noise figure NF	[dB]	3.3
Input referred IP_3	[dBm]	-16
Input referred $CP1$	[dBm]	-25

Mixer Specification		
Voltage gain G_V	[dB]	12
Input referred noise source	[nVrms/$\sqrt{\text{Hz}}$]	10
Input referred $IP3$	[Vrms]	1.5

Baseband Filter Specification		
Voltage gain G_V	[dB]	24
Input referred noise source	[nVrms/$\sqrt{\text{Hz}}$]	15
Input referred $IP3$	[Vrms]	3

3.5. Conclusion

After a brief introduction to the GSM mobile communication system, the test scenarios defined in the official 3GPP GSM specification for mobile handsets [39] have been discussed and analysed. From these scenarios a set of performance metrics for the thermal noise figure, even and odd order distortion has been derived for an analogue GSM receiver front-end.
Based on a profound literature review of conventional wireless receiver architectures with their advantages and disadvantages it has been concluded that a direct-conversion or zero-IF receiver architecture is the most appropriate for low-cost monolithic integration of a GSM transceiver.
In a next step a system link budget has been calculated for an analogue GSM receiver front-end in order to distribute the gain, noise and non-linearity contributions of the individual circuit blocks in the receive chain. This system budget analysis sets the reference requirements for a GSM receiver handset in accordance with [39]. Additionally a set of specifications for a high-performance GSM receiver front-end is presented.

Table 3.4.: System link budget calculations based on the reference performances for a GSM receiver front-end.

		Antenna	BalUn	Matching + LNA	Mixer	BBF
Signal Level at Block Output	[Vrms]	$2.5{\cdot}10^{-6}$	$5.0{\cdot}10^{-6}$	$4.0{\cdot}10^{-5}$	$1.6{\cdot}10^{-4}$	$2.5{\cdot}10^{-3}$
Noise Density at block output	[nVrms/$\sqrt{\text{Hz}}$]	$4.6{\cdot}10^{-10}$	$1.2{\cdot}10^{-9}$	$1.2{\cdot}10^{-8}$	$6.3{\cdot}10^{-8}$	$1.0{\cdot}10^{-6}$
Cascaded Voltage Gain at Block Output	[dB]	0	6	24	36	59
Cascaded SNR at Block Output	[dB]	21.6	19.6	17.2	15.0	14.8
Cascaded NF	[dB]	0.0	2.0	4.4	6.6	6.8
Cascaded IP3 Input Referred	[Vrms]	∞	∞	$3.5{\cdot}10^{-2}$	$3.3{\cdot}10^{-2}$	$2.7{\cdot}10^{-2}$

Table 3.5.: Refined set of specifications for a high performance GSM receiver front-end.

Block	Performance	Unit	Min.	Typ.	Max.	Comment
LNA + Mixer + LPF	f_{RX1}	[MHz]	869		894	GSM850
	f_{RX2}	[MHz]	925		960	GSM900
	f_{RX3}	[MHz]	1805		1880	GSM1800
	f_{RX4}	[MHz]	1930		1990	GSM1900
	G_V	[dB]		60		
	NF	[dB]		3	5	
	$CP1i$	[dBm]	-25			interferer @ 3 MHz offset
	IIP_2	[dBm]	38			interferer @ 6 MHz offset
	IIP_3	[dBm]	-18			interferer spacing 800 kHz
LNA	G_V	[dB]	21	25	27	
	NF	[dB]		2	3	Spot-noise @ 80 kHz
Mixer + LPF	G_V	[dB]		35		
	input referred noise voltage density	[nV/$\sqrt{\text{Hz}}$]		5	7	Spot-noise @ 80 kHz

4. CMOS Process Technology Characteristics and Scaling

This chapter discusses standard CMOS process technology characteristics and how they are affected by the scaling of modern process technology generations. The author's focus is on scaling aspects that have pre-dominant consequences for the design of integrated analogue low-cost low-power circuits. After the basic device components in integrated circuits and their implementation in sub-micron technologies in general have been introduced, the performance of a selection of devices relevant for the realisation of the wireless GSM receiver front-end application is profoundly investigated in a model based device comparison for a 130 nm and a 65 nm CMOS technology. The chapter is concluded by the prospects of future trends in technology scaling and integrated analogue circuit design.

4.1. Basic Components

4.1.1. Resistors

Resistors in integrated circuits can have various implementations. However, as these implementations are not in the focus of intense research only the most common resistor implementations found in literature are listed.

- Some process technologies do not offer explicit resistor devices at all.

  (a) Transistors working in the triode region replace explicit resistor devices. The MOS-resistors can form compact resistors but have loose tolerances as the resistance value depends on the threshold voltage of the device and charge carrier mobility in the conducting channel. Besides MOS-resistors have a high temperature coefficient (TC) and are quite non-linear [35].

  (b) Resistors can also be made from source-drain diffusions. These devices suffer from a significant junction capacitance and high voltage coefficient. Thus their application primarily limited to circuits operating at low frequencies and with a reduced dynamic range. Modern process technologies that define source-drain diffusions by ion-implanting achieve low resistivities and $TC \approx 500 - 1000\,\mathrm{ppm/^\circ C}$ [35].

  (c) Metal resistors made from aluminium or copper with a resistivity of $50\,\mathrm{m\Omega/\square}$ are of practical use for very low ohmic resistors around $10\,\Omega$. A typical temperature coefficient for aluminium made resistors is $3900\,\mathrm{ppm/^\circ C}$ [35].

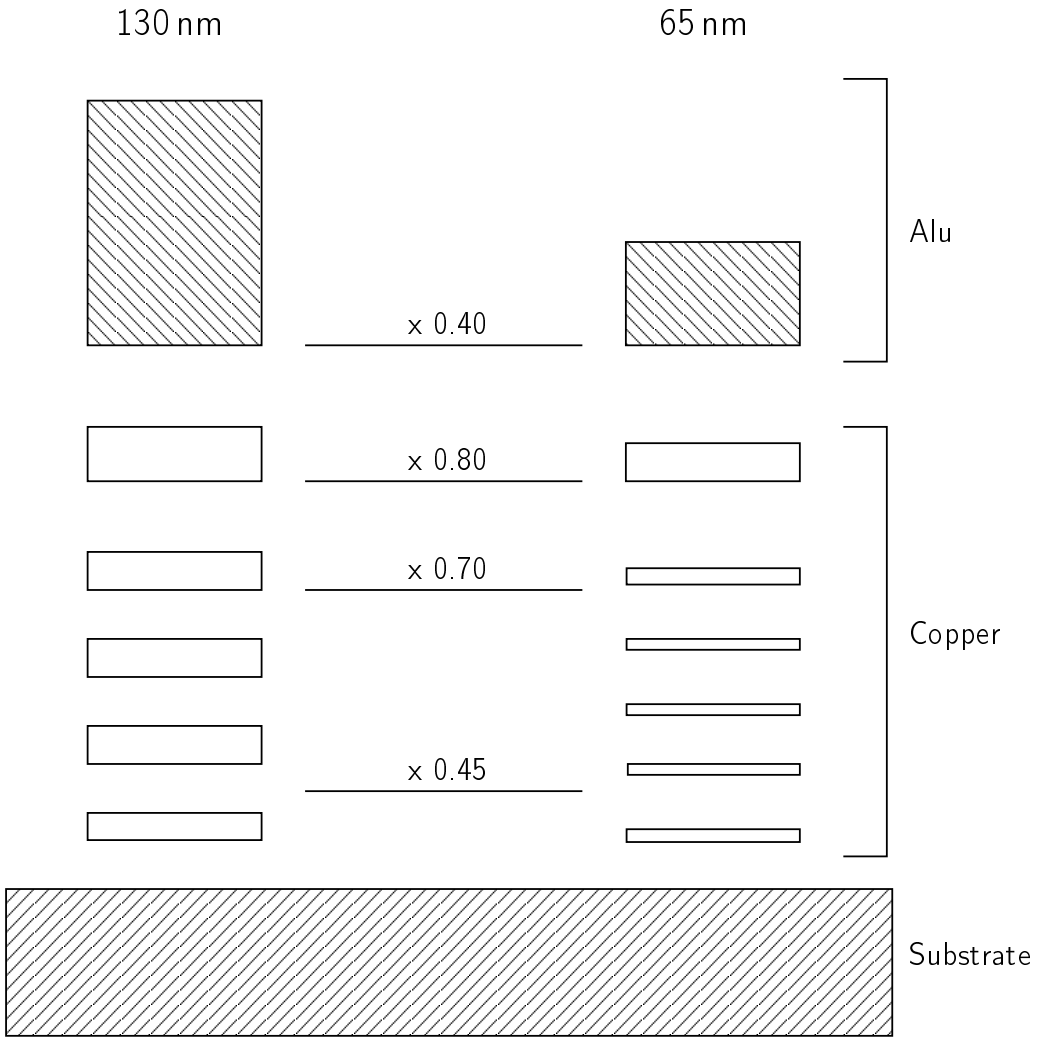


Figure 4.1.: Schematic drawing of the metal stacks for a 65 nm and a 130 nm process technology [14].

- Poly resistors are the standard resistors in RF CMOS circuits. Poly silicon is integral part of CMOS technologies as it is the prominent material used for transistor gates today.

  (a) As most poly is silicided e.g. in order to lower the gate resistance, typical values of resistivity are low and about 5-10 $\Omega/\square$. The tolerances for absolute resistance values are poor i.e. 35 %. Silicided poly resistors offer a moderate $TC \approx 1000\,\mathrm{ppm/^{\circ}C}$ in combination with low parasitic capacitance and a low voltage coefficient.

  (b) For unsilicided poly resistivity values about one order of magnitude higher than for silicided poly are reported. Unfortunately the tolerances increase up to 50 % and the TC ranges widely depending on the processing details.[35].

4.1.2. Capacitors

Modern sub-micron CMOS technologies offer different types of capacitor implementations:

Metal Insulator Metal Capacitor (MIM-cap). A MIM-cap is a standard horizontal parallel plate capacitor with a dielectric insulator between its metal layers. The advantages of these capacitors are that they are very linear devices with a low TC. The overall TC of the capacitor is governed by the TC of the permittivity ϵ_{DIEL} of the dielectric layer. The disadvantage of the MIM-cap is that the bottom plate of the capacitor forms a parasitic capacitance with the substrate. In general the achievable capacitance density is low as the isolation layers between the metal layers are rather thick in order to reduce the parasitic capacitance between metal layers. Some process technologies offer optional MIM-cap devices with special high permittivity inter-level dielectric between top metal layers. When the horizontal geometrical dimensions (width w and length l) of the capacitor plates are small and comparable to the thickness t of the isolation layer between the plates fringing capacitances start to dominate the device. The capacitance of the device is given by (first order approximation [35])

$$C \approx \begin{cases} \epsilon_{DIEL}\frac{w \cdot l}{t} & \text{if } w, l \gg t \\ \epsilon_{DIEL}\frac{(w+2t)\cdot(l+2t)}{t} \approx \epsilon_{DIEL}\left[\frac{wl}{t} + 2w + 2l\right] & \text{if } w, l \leq t. \end{cases} \tag{4.1}$$

The capacitance density of a plate capacitor can be increased by connecting multiple metal layers to a sandwich structure.
Later in this section the term MIM-cap is reserved to optional capacitor implementations between the top metal layers. The insulator between the capacitor plates is often a higher ϵ_{DIEL}-dielectric. Ordinary capacitor implementations with parallel horizontal metal plates will be referred to as HPP-caps. HPP-caps use the default SiO_2 as dielectric insulator.

Vertical Parallel Plate Capacitor (VPP-cap). As the adjacent spacings between metals that pass the design rule checks of modern process technologies are shrinking with technology scaling these spacings are smaller than the vertical distances between metal layers. Thus the possibility for effective capacitor implementations build from vertical metal structures arises. Vertical 'plates' can be formed from via arrays (Fig. 4.2). As with the MIM-caps, VPP-caps are linear devices with a low TC. Aside from the limitations imposed by the manufacturability of minimum spacings between metal structures in the same metal layer, the reduced thickness of the isolator in between the metal structures bears the risk of an electrical breakdown of VPP-cap structures at peak voltages. Thus there is a limit for the maximum capacitance density that can be achieved with VPP-cap for a given insulator or dielectric.

MOS-Capacitor (MOS-cap). Another possible implementation for a capacitor in a CMOS technology is the use of the gate capacitance of a transistor. The drain, source and bulk terminal of the transistor device are electrically shortened and form one terminal of the capacitor device. The other terminal of the capacitor device is formed by the gate terminal. The capacitance density of the MOS-cap benefits from the thin gate oxide layer of modern submicron process technologies ($t_{OX} \leq 10\,\text{nm}$). MOS-caps are infamous for a low capacitance densities, high losses and highly non-linear behaviour if biased incorrectly. The device needs to be operated in strong inversion ($V_{GS} \gg V_{TH}$). Even if the device is biased correctly the TC will be higher than for the other two capacitor types that have been introduced before.

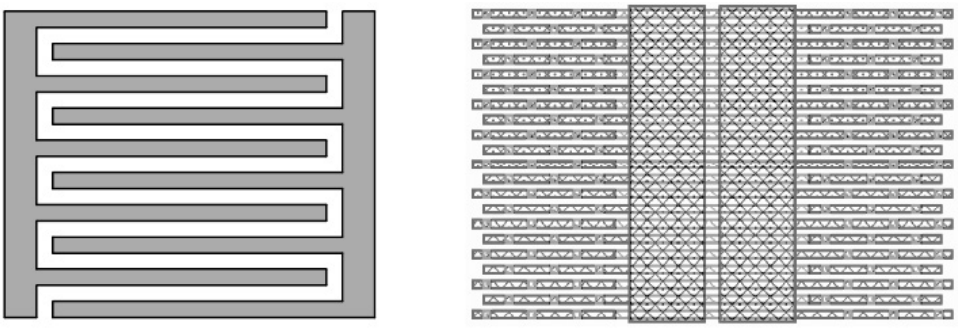


Figure 4.2.: Sight view (left) and top view (right) of a VPP-cap [26].

In order to generate a device with the a high quality factor $Q = g_{DS}/(2\pi fC)$ a transistor with the minimum allowable channel length has to be chosen [35].
Because of the their non-linear characteristics (C vs. V_{GS}) MOS-caps are also used on purpose as varactors for the frequency-tuning of LC-based oscillators.

A combination of the multiple capacitance implementations. In order to design a capacitor with a capacitance density higher than the individual capacitance density values of the three introduced types of capacitors, a combination of shunt connected devices can be used. One feasible approach is to place a MIM-cap or VPP-cap over a MOS-cap in the physical implementation.

4.1.3. Inductors

In general inductors with inductance values $1\,\text{nH} \leq L \leq 10\,\text{nH}$ are comparatively large area consuming structures in modern GSM receivers. That is why low-cost integration and miniaturisation strives to avoid coils. In addition to the disadvantages from the cost-effectiveness point of view due to the huge die area consumption, integrated coils require increased simulation and modelling efforts. 3-D field solvers are necessary in order to generate decent simulation models. Whereas capacitor models, resistor models and transistor models are available in the default libraries coming with a modern design package, default coil libraries are often hard to find.
The receiver front-end circuits presented in this thesis completely do without the use of coils. Nevertheless a coarse abstract about coil implementation is given.
An inductor (Fig. 4.3) is not only characterised by its inductance value L but also by its quality factor Q and its resonant frequency f_R. Q and f_R are commonly defined by

$$Q = \frac{2\pi fL}{R} \tag{4.2}$$

and

$$f_R = \frac{1}{2\pi\sqrt{LC}} \tag{4.3}$$

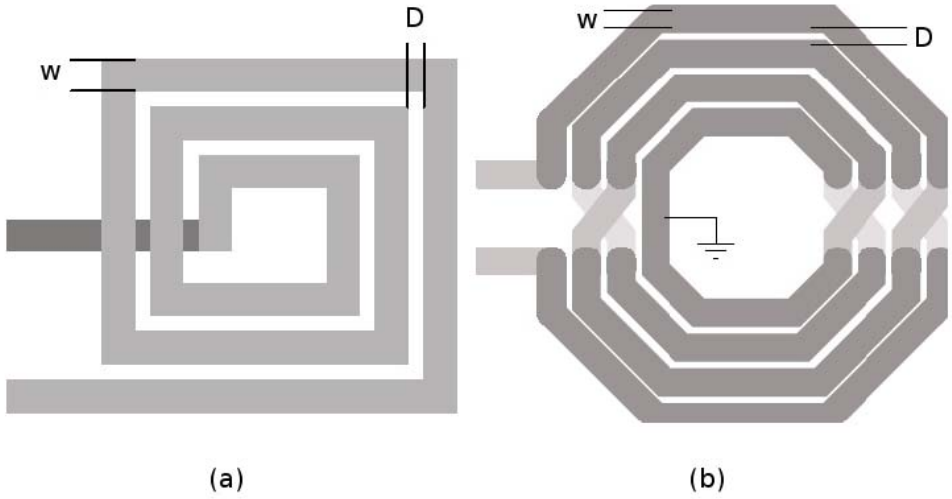


Figure 4.3.: a) Square shaped coil. b) Octagonal shaped coil. D denotes the distance between windings, w denotes the average width of the windings [14].

where

R Ohmic resistance accumulated along the coil windings
C Parasitic capacitance between the windings.

If a certain high Q is required for an application e.g. a VCO with low phase noise, the designer is forced to use an increased line width w and/or multiple metal layers for the implementation of the coil. A larger path width w and the use of multiple metal layers or closely spaced windings reduces the ohmic resistance of the coil. The outer windings of an integrated coil often use larger path widths than the inner windings in order to keep the overall resistance low on a pre-longed signal path. Wide metal paths, multiple layers or closely spaced windings introduce larger parasitic capacitances C between windings. The increased capacitance lowers the resonant frequency of a coil. This is the most dominant trade-off in integrated coil design. The potential of a CMOS technology for coil implementation can be estimated to a large degree by characteristics of the technology metal stack (Fig. 4.1). The specific resistances of the metal layers, the thickness of the metal layers and the vertical distances between metal layers determine the performance of a coil. There is a clear trend in standard CMOS technologies to reduce the metal thickness of the metal layers. Furthermore, the resistance of metal interconnects between layers (vias) increases. As a result the resistance that accumulates along the windings of a coil R grows. Another trend in standard CMOS process technology is to reduce the substrate resistance by increased substrate doping with every technology generation. The lower substrate resistance increases the losses of coils which in turn causes additional degradation the achievable Q. In addition the noise coupling and eddy currents into the substrate are increased when the substrate resistance is lowered [14]. The lower substrate resistance originates from the digital heritage of modern CMOS technologies being abused for analogue RF CMOS. Digital designers benefit from a lower substrate resistance because it helps to prevent latch-up effects and helps the fast travelling of signals across the lines [41]. Some technologies offer optional thick top metal layers. These top metal layers are better suited for high Q coil implementation than the standard metal layers. As the technology options are charged extra they are usually avoided for low cost implementations.

4.1.4. Field Effect Transistors (FET)

4.1.4.1. Long Channel Device Equations

The equations presented in Section 4.1.4.1 are adopted from literature [19], [35]. As the author's focus is on the application of metal oxide semiconductor field effect transistors (MOSFETs) rather than on device physics of MOSFETs, vital equations are presented but not derived in detail. The classical derivation is based on summing up travelling charges along the conducting channel of the FET. The equations are given as they are still taught in university lectures although they are inaccurate when it comes to modelling short channel effects in modern deep sub-micron technologies (cf. Section 4.1.4.2).
Nevertheless these equations prove useful when evaluating the perspectives of RF CMOS scaling and come in handy when it comes to analytical calculations.
In the following we assume that the conducting channel of the transistor is operated in inversion: $V_{GS} > V_{TH}$.

4.1.4.1.1. Triode region or Ohmic region The triode region of operation of a MOSFET ($V_{DS} \leq V_{GS} - V_{TH}$) is characterised by the fact that the drift velocity of the charge carriers is determined by the horizontal electric field. A conducting channel with minority charge carriers is build up underneath the gate oxide. The channel is in inversion.

$$I_D = \frac{\mu C_{OX}}{2} \frac{w}{l} (2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2)(1 + \lambda V_{DS}) \tag{4.4}$$

where

$C_{OX} =$	ϵ_{OX}/t_{OX}
$V_{TH} =$	$V_{TH0} + \gamma_S(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$
$\gamma_S =$	$(1/C_{OX})\sqrt{2q\epsilon_{SI}N_A}$
$\phi_F =$	$(kT/q)\ln(N_A/n_i)$
$n_i =$	$\sqrt{N_C N_V} exp(-E_G/(2kT))$
V_{TH0}	Threshold voltage for $V_{SB} = 0\,\mathrm{V}$
ϕ_F	Fermi level
V_{SB}	Source-bulk voltage
ϵ_{Si}	Permittivity of silicon
N_A	Acceptor doping density
N_C	Density of the allowed states near the edge of the conductance band
N_V	Density of the allowed states near the edge of the valence band
E_G	Bandgap of silicon at $T = 0°\,\mathrm{C}$.

I_D denotes the drain current. μ is the charge carrier mobility. C_{OX} is the gate oxide capacitance per unit area. w and l describe the physical dimensions (width and length) of the transistor. $V_{GS} - V_{TH} = V_{OV}$ is also sometimes referred to as overdrive voltage. $\lambda = 1/V_{EA}$ is the reciprocal of the Early-Voltage and characterises the channel length modulation. Channel length modulation is insignificant in the ohmic region but is added to (4.4) for completeness . For $V_{DS} \ll V_{OV}$, I_D is proportional to V_{DS}. The transistor behaves like a resistor. This is why this region of

operation is also called ohmic region [19].

4.1.4.1.2. Saturation region or Active region The saturation region ($V_{DS} \geq V_{GS} - V_{TH}$) is the conventional operating regime for MOSFETs. The movement of charge carriers in the device is limited by velocity saturation as the conducting channel underneath the gate oxide is pinched-off. The pinch-off region is in depletion instead of inversion. The classic equation for calculating the drain current I_D of a MOSFET (including channel length modulation) is given by

$$I_D = \frac{\mu C_{OX}}{2} \frac{w}{l} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}). \tag{4.5}$$

From (4.5) the small signal input transconductance g_M can be derived as

$$g_M = \frac{\partial I_D}{\partial V_{GS}}. \tag{4.6}$$

$$g_M = \mu C_{OX} (1 + \lambda V_{DS}) \frac{w}{l} (V_{GS} - V_{TH}) \tag{4.7}$$

With (4.5) the expression $V_{GS} - V_{TH}$ can be replaced in (4.7) by

$$V_{GS} - V_{TH} = \sqrt{\frac{2 I_D}{\mu C_{OX} (1 + \lambda V_{DS})} \frac{l}{w}}. \tag{4.8}$$

Thus resulting in

$$g_M = \sqrt{\frac{2 I_D \mu C_{OX}}{1 + \lambda V_{DS}} \frac{w}{l}}. \tag{4.9}$$

The transconductance-to-current ratio derives to

$$\frac{g_M}{I_D} = \frac{2}{V_{OV}}. \tag{4.10}$$

The transition frequency is calculated to be

$$f_T = \frac{1}{2\pi} \cdot \frac{g_M}{C_{GS} + C_{GD} + C_{GB}}, \tag{4.11}$$

with

$$C_{GS} \approx 2/3 \cdot w l C_{OX}.$$

The drain-source transconductance is given by

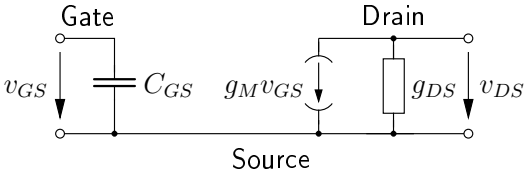


Figure 4.4.: Small signal equivalent circuit of a long channel MOSFET in saturation region.

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}}. \tag{4.12}$$

$$\Rightarrow g_{DS} = \frac{\lambda \mu C_{OX}}{2} \frac{w}{l} (V_{GS} - V_{TH})^2 \tag{4.13}$$

4.1.4.2. Short Channel Device Equations for the Active Region

The charge carrier velocity in the conducting channel is defined as $v_d = v_{MAX} = \text{const}$ for the active operation region of a transistor in the short channel regime. Literature gives a value for electron saturation velocity in silicon of about $v_{MAX} = 10^5$ m/s [19], [35] and [41]. In contrast to long channel devices where the saturation current is bound to the value of the current when the channel is pinched off, the current saturates with the carrier velocity in short channel devices.

A first order approximation for the carrier drift velocity v_d is

$$v_d = \frac{\mu E}{1 + E/E_C}. \tag{4.14}$$

E_C is the critical strength of the electrical field E where v_d has reached half the value extrapolated from low field mobility where $v_d = \mu E$ is still valid [19].
A high electric field drives the charge carriers into the scattering-limited velocity saturation $v_{MAX} = \mu E_C$ (Fig. 4.5). Based on a constant v_{MAX} the drain current is formulated as

$$I_D = v_{MAX} \frac{\epsilon_{OX}}{t_{OX}} w \left(\frac{V_{GS} - V_{TH}}{1\,\text{Volt}}\right)^{\alpha} \cdot 1\,\text{Volt} \tag{4.15}$$

with

$$\alpha \quad = 1..2, \text{ typically } \alpha = 1.4 \text{ [41]}.$$

An $\alpha \geq 1$ fits measurement results but the units in (4.15) are not consistent if we do not normalise to 1 Volt. Setting $\alpha = 1$ implies that the travelling charge carriers enter the channel already at terminal velocity and do not need to be accelerated in the channel itself (cf. Sec. 4.1.4.1).
In [19] α is set to 1 and thus the drain current I_D is described as a linear function of the overdrive voltage V_{OV}. Furthermore I_D is independent of the channel length l. This is because the charge in the channel as well as the time required to cross the channel is proportional to l. Additionally I_D is directly proportional to v_{MAX}.

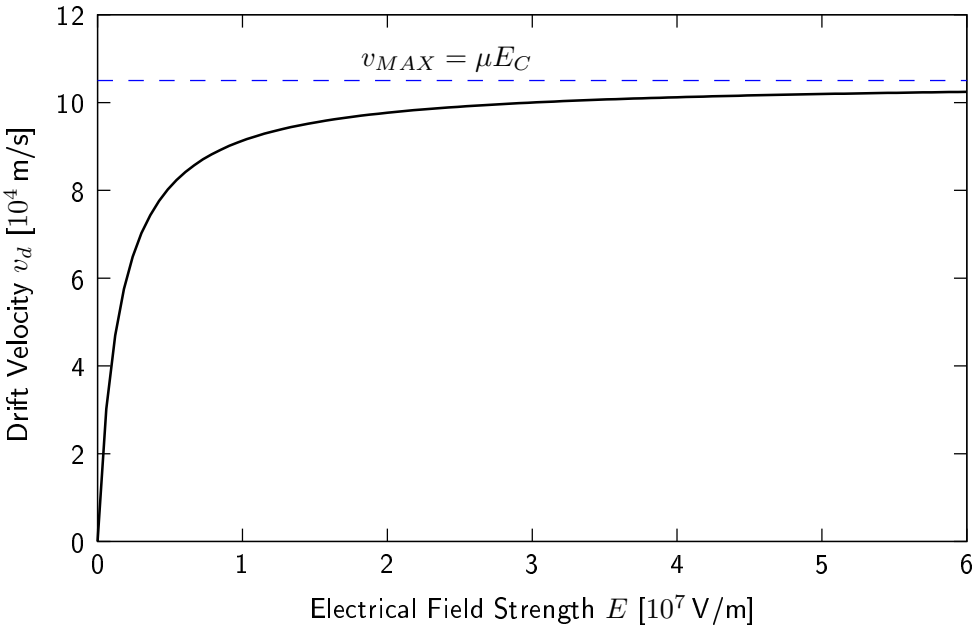


Figure 4.5.: Electron drift velocity vs. electrical field strength in the short channel regime. Numerical values for $E_C \approx 1.5 \cdot 10^6\,\mathrm{V/m}$ and $\mu_n = 0.7\,\mathrm{m}^2/(\mathrm{Vs})$ adopted from [19].

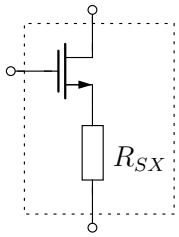


Figure 4.6.: For large signal computation a short channel transistor is modelled as an ideal long channel device with a series resistor R_{SX} connected to the source node [19].

For large signal computing of a short channel device in the saturation region it is suggested to add a series resistance R_{SX} at the source node of an ideal square law device (Fig. 4.6).
A simplified device equation

$$I_D \approx \frac{\mu C_{OX}}{2(1+\mu C_{OX}\frac{w}{l}R_{SX}(V_{GS}-V_{TH}))}\frac{w}{l}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) \tag{4.16}$$

with

$$R_{SX} \quad = (E_C \mu C_{OX} w)^{-1}$$

is presented.

The small signal input transconductance for a short channel MOSFET in the active region is

derived to

$$\lim_{E_C \to 0} g_M = wC_{OX}v_{MAX}. \tag{4.17}$$

From (4.17) it is evident that g_M is independent of V_{OV} and does not increase with a scaling of the transistor length l [19].
The transconductance-to-current ratio

$$\lim_{E_C \to 0} \frac{g_M}{I_D} = \frac{1}{V_{OV}} \tag{4.18}$$

is reduced compared to the long channel regime (cf. (4.10)).

So far only the effects of the high horizontal electric field in short channel devices have been taken into account. The vertical field strength draws charge carriers in the channel close to the silicon-to-gate-oxide-interface. This interface is prone to have surface imperfections like dangling bonds etc. which degrade the mobility of the charge carriers travelling. As the vertical field strength is not constant along the channel, exact calculations have to take the degradation effect into account right from the start of the derivation of device equations. For simplicity, however, the degradation effect is commonly modelled by replacing the 'nominal' mobility μ with an effective mobility μ_{eff} after deriving the device equations the classical way [35], [19]

$$\mu_{eff} = \frac{\mu}{1 + \theta V_{OV}}, \tag{4.19}$$

where θ is the normal-field mobility degradation factor. The value of θ is dependent on the gate oxide thickness and is obtained empirically. For an oxide thickness of $t = 10\,\text{nm}$, θ typically ranges from $0.1\,\text{V}^{-1}$ to $0.4\,\text{V}^{-1}$ [19]. It is expected that θ increases with reduced oxide thickness.

An ambitious modelling approach is presented by the author of [59], taking both, horizontal and vertical electrical field, into account.

$$\mu_{eff} = \frac{\mu}{1 + \theta_G V_{OV} + \theta_B V_{SB}} \cdot \frac{1}{1 + V_{DS}/(lE_c)}, \tag{4.20}$$

θ_G is called the voltage degradation factor modelling the effect of the gate potential. θ_B is called the voltage degradation factor modelling the effect of the gate potential.

4.1.4.3. Sources of Noise in CMOS Transistors

For a CMOS transistor there are three known major noise sources: Flicker noise, induced gate noise and thermal channel noise.

4.1.4.3.1. Flicker Noise is also known as $1/f$-noise or pink noise. As the name suggests the spectral density is reciprocally proportional to frequency. Although the reasons for flicker noise are not exactly known, it is commonly understood that flicker noise is a surface phenomenon [35]. Crystal imperfections, certain defects, impurities or dangling bonds at the interface between silicon and the gate oxide trap and release travelling charges in random fashion with time con-

stants that give rise to the typical $1/f$ characteristic. A direct current flowing is necessary as the noise phenomenon depends on travelling charges [19]. Bipolar transistors being bulk devices exhibit less flicker noise. In surface devices like FETs the effect is more significant. PFETs with charge travelling in buried channels have superior noise performance to NFETs. A mathematical description for the drain current flicker noise density in a MOSFET is given by

$$\overline{i_{nf}^2} = \frac{K}{f}\frac{g_M^2}{wlC_{OX}^2}, \tag{4.21}$$

where

K	empirically determined constant (may vary for different devices or processing runs [35])
g_M	transistor transconductance
f	frequency
w	transistor width
l	transistor length
C_{OX}	gate oxide capacitance per gate area

The corner frequency up to which flicker noise is the dominating noise contribution of a FET is often used to compare different devices. For modern process technologies this corner frequency can reach up to a few 100 MHz. For low-frequency low-noise applications it is suggested to enlarge the device area in order to reduce the flicker noise contribution [48]. This seems contradictory at first thought because the critical interface area is enlarged but the also enlarged gate capacitance filters the generated noise.
It is also worth noting that flicker noise is most prominent in active devices, but it is also present in carbon resistors. Furthermore, it should be noted that the infinity of the flicker noise density for $f = 0\,\text{Hz}$ is merely a theoretical but not a practical problem as a measurement at *dc* requires an infinite measurement duration [35].

4.1.4.3.2. Thermal Channel Noise From an abstract point of view a MOSFET is basically a voltage controlled resistor. Thus the resistive channel generates thermal noise. An analytical expression for the thermal spectral noise density has been derived by [57]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}, \tag{4.22}$$

with

k	Boltzmann constant
T	absolute temperature
g_{d0}	drain-source conductance at V_{DS}=0 V.

The factor γ is reported to be $\gamma \approx 2/3$ for long channel devices [35] and $2 \leq \gamma \leq 3$ or even larger for short channel devices [1], [19]. The author of [48] gives an exemplary $\gamma \approx 2.5$ for a 250 nm CMOS process technology.
When it comes to excess thermal noise in short channel devices the term 'hot electrons' is often used in literature. Recent theoretical and experimental work disproves hot carrier effects in the high electric field as the cause of the observed excess noise [35].

4.1.4.3.3. Induced Gate Noise According to the author of [35] the thermal agitation of charge carriers in the conducting channel and the resulting fluctuating channel potential of a FET induce a noisy gate current by capacitive coupling. The resistive gate material also adds its contribution. The mechanism is called induced gate noise and its spectral density is described by

$$\overline{i_{ng}^2} = 4kT\delta g_g \tag{4.23}$$

with

$$\delta \approx 2\gamma \tag{4.24}$$

$$g_g = \frac{\omega^2 C_{GS}^2}{5 g_{d0}} \tag{4.25}$$

$$\omega = 2\pi f. \tag{4.26}$$

Induced gate noise can be neglected at low frequencies but dominates the noise behaviour of a FET at high frequencies. The transistors investigated in Section 4.2.1.4 of this work exhibit dominant flicker noise for frequencies beyond $f = 10\,\mathrm{GHz}$ (cf. Fig. 4.18). In noise calculations the induced gate noise source is represented by a current source $\overline{i_{ng}^2}$ and a conductance g_g in parallel to the gate-source capacitance of the FET. Due to its origin induced gate noise source is correlated with the thermal noise source $\overline{i_{nd}^2}$. Literature expresses the correlation as

$$c \equiv \frac{\overline{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{nd}^2} \cdot \overline{i_{ng}^2}}} \tag{4.27}$$

and gives a value of $c = -j0.395$ for long-channel FETs [35]. The negative sign depends on the reference directions.

4.1.4.3.4. Shot Noise Shot noise (also referred to as Schottky noise) is only present when there is a *dc* current I_{DC} flowing across a potential barrier in a non-linear device. The granular nature of the electric charge that passes the potential barrier (electrons hopping across the barrier) is responsible for the emergence of the effect. Due to the randomness of the electrons behaviour the spectral density characteristic (cf. (4.28)) is white in the radio frequency range [35].

$$\overline{i_{ns}^2} = 2qI_{DC} \tag{4.28}$$

with

$$q \quad = 1.6 \cdot 10^{-19}\,\mathrm{C}$$

For a FET only the gate leakage current fulfils the constraints necessary for the emergence of shot noise. As the gate leakage current can usually be neglected for FETs in first order approximation, shot noise is only of minor concern for this work. The author of [35] gives $18\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ per mA of *dc* current flowing as a rule of thumb. Shot noise is more relevant for bipolar transistors or diodes.

4.1.4.3.5. Noise Conclusion We can summarise that at low frequencies the noise spectral density of a FET is dominated by the flicker noise contribution. For high frequencies the noise behaviour is dominated by the induced gate noise. In between the noise behaviour is ruled by the thermal noise floor.

4.2. A Model based Device Comparison between a contemporary 130 nm and a 65 nm CMOS Technology

Before we start with the actual device comparison the two CMOS process technologies will be briefly introduced. The names used for the technologies in this thesis are chosen according to the minimum allowable drawn channel length l for transistor devices. A schematic drawing of the metal stacks in both technologies is shown in Fig. 4.1. The 130 nm process technology offers five copper layers aside from the aluminium top metallisation. The 65 nm process technology offers six copper layers aside from the aluminium top metallisation. In Table 4.1 the important features of both technology generations are summarised.

Table 4.1.: Features of the compared CMOS technology generations .

Feature	Unit	130 nm Technology	65 nm Technology
Transit frequency f_T	[GHz]	95	180
Gate oxide thicknesses t_{OX}	[nm]	2.2 5.2	1.8 2.8 5.2
Default supply voltages V_{DD}	[V]	1.5 2.5	1.2 1.8 2.5
Relative substrate resistance R_{SUBS}	[%]	100	88
Relative oxide capacitance C_{OX}	[%]	100	126
Relative sheet resistance lowest copper layer R_{M1}	[%]	100	234
Relative sheet resistance lower copper layers R_{M2-M4}	[%]	100	186
Relative sheet resistance medium copper layers R_{M5}	[%]	100	137
Relative sheet resistance upper copper layer R_{M6}	[%]	-	100
Relative sheet resistance aluminium top layer R_{ALU}	[%]	100	227

The transit frequency for the 65 nm technology is reported to be about twice as high as for the 130 nm technology for minimum device size.
Furthermore, we see from Table 4.1 that gate oxide thickness does not scale proportional to the minimum channel length. The scaling of the gate oxide thickness is far less aggressive. The author of [14] claims that the scaling in modern CMOS technologies is less aggressive because

the gate leakage current grows exponentially with a reduction of the oxide thickness leading to unacceptable higher static currents.
As expected the substrate resistance decreases with the scaling of the technologies making especially the design of high Q integrated coils more difficult (Section 4.1.3).
As the metal layers are thinner in the 65 nm technology (cf. Fig. 4.1) the wiring resistance increases with the sheet resistance of the metal layers. The increase ranges from 37 % to 127 %. The enlarged wiring resistance affects the implementation of all kinds devices i.e. supply connections have increased series resistance, LNA input lines contribute more noise to the receiver etc. when the same dimensions are chosen for these lines as in the implementation in the 130 nm technology.

4.2.1. Wired NFET Standard Cells

In this section we will compare the performance of three NFET test devices with ratio $w/l \approx 1000$. The physical dimensions of the test devices that are investigated are chosen on purpose. Whereas technology manuals usually contain performance characteristics like f_T or V_{TH0} of minimum devices, performance documentation for larger devices suitable for e.g. RF amplifiers is hard to find. The performance characteristics are extracted from the *dc* operating point parameters the spice models offer. With respect to the subject of this thesis especially RF amplifying for LNA circuits are in the focus of the comparison.
The first unit cell transistor with a channel length $l = 120\,\text{nm}$ and a width of $w = 6.52\,\mu\text{m}$ is implemented in a 130 nm standard CMOS technology. The unit cell model contains metal wiring up to the fourth metal layer. The second unit cell transistor with a channel length $l = 120\,\text{nm}$ and a width $w = 6.52\,\mu\text{m}$ is implemented in a 65 nm standard CMOS technology. The third unit cell transistor uses the minimum channel length $l = 60\,\text{nm}$ of the 65 nm standard CMOS technology and a width $w = 4.00\,\mu\text{m}$. The device cells of the 65 nm technology include metal wiring up to the first metal layer.
All three unit cells are implemented with four gate fingers. The unit cells are shunt connected in bundles of n =18 devices for the $w = 6.52\,\mu\text{m}$ devices, respectively in bundles of n =15 devices for the $w = 4.00\,\mu\text{m}$ devices. The electrical connection is made using the Spectre device multiplier option. Thus total ratio $n \cdot w/l = w_{TOT}/l \approx 1000$ for test devices. The deviation in the total ratio w_{TOT}/l is less than 2.2 % between the three test devices.
As the metal wiring included in the transistor models of the 65 nm and the 130 nm technology differs, the performance comparisons made will probably favour the 65 nm technology especially when it comes to frequency dependent characteristics. Nevertheless, as the models of the unit cells offered by the design packages provide the best modelling accuracy ('best-guess') to the RF designer at the early design stages (pre-layout) they are considered appropriate for a model based device comparison. All device models are based on UC Berkeleys' well known BSIM4 spice transistor model [13].
The test devices with $l = 120\,\text{nm}$ channel lengths help to illustrate the different characteristics of two geometrically equal devices in different technologies. The third device with a channel length of $l = 60\,\text{nm}$ is implemented in order to point out the different characteristics of two devices with different channel lengths in the same 65 nm technology.
The device implemented in the 130 nm technology with $l = 120\,\text{nm}$ channel length will be referred to as device I. The devices the $l = 120\,\text{nm}$ and $l = 60\,\text{nm}$ implemented in the 65 nm technology will be referred to as device II respectively device III (Table 4.2).
All simulations are performed at a junction temperature of $T = 40^\circ\,\text{C}$. This temperature value

Table 4.2.: Geometry data of the three test devices.

	Length of unity cell	Width of unity cell	Number of cells connected in parallel	w_{TOT}/l	Technology node
Unit	[nm]	[μm]	[1]	[1]	[nm]
device I	120	6.52	18	978	130
device II	120	6.52	18	978	65
device III	60	4.00	15	1000	65

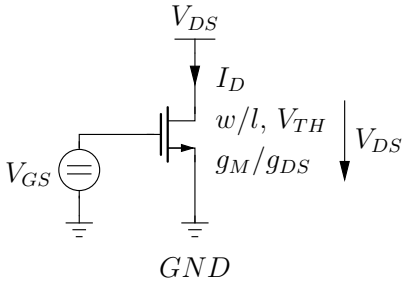


Figure 4.7.: Test circuit for the characterisation of a regular NMOSFET.

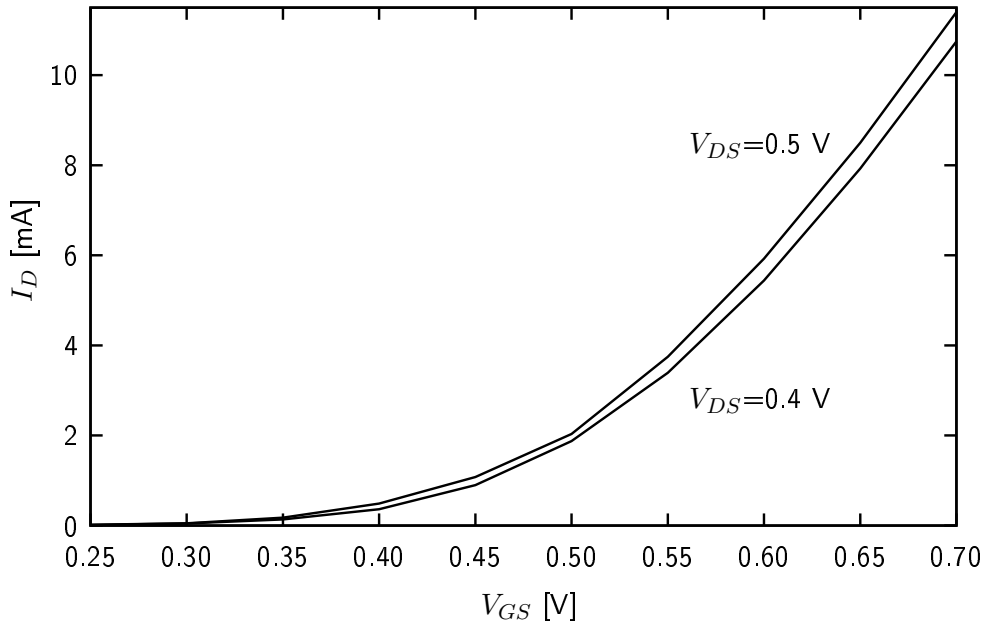
is higher than room temperature. It is considered more appropriate for the simulations as the on-chip operating temperature is above room temperature especially for an analogue transistor in an integrated packaged single-chip design.

Figure 4.7 depicts the simple test circuit used to characterise the performance of the transistor test devices.

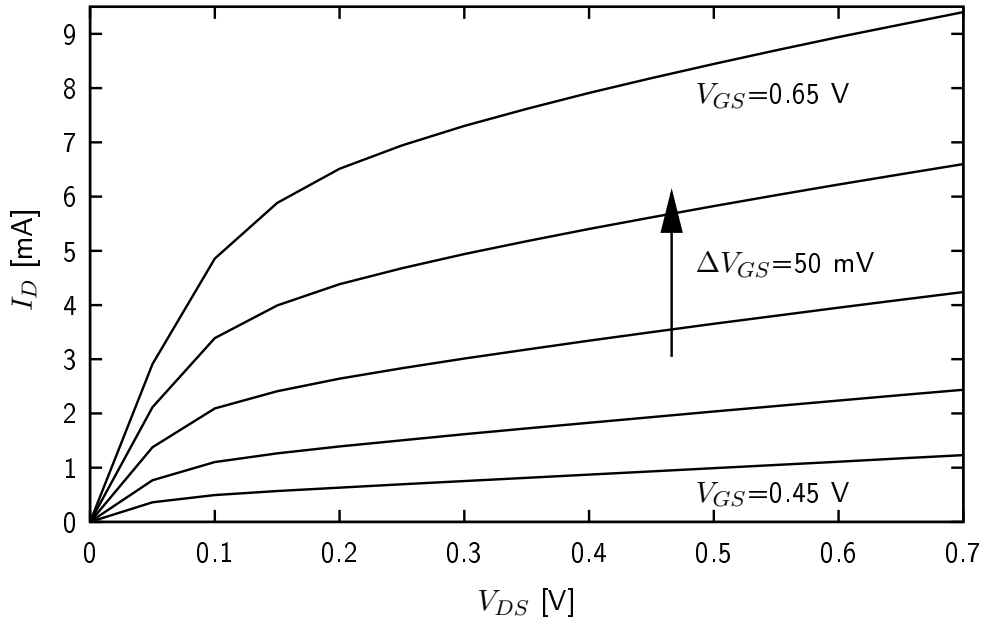
4.2.1.1. Input/Output Characteristics of the Test Devices

We will begin the characterisation of the three test devices by recording the input and output characteristics of the devices (Fig. 4.8(a) to Fig. 4.10(b)).

As this section focuses on the comparison of transistor cells suitable for use e.g. in integrated RF LNAs we can limit the reasonable operating region for the devices. First of all we want to operate the CMOS transistors in the saturation region. Following the classical constraints for the saturation region, we demand $V_{DS} \geq V_{GS} - V_{TH}$. Secondly, the drain source voltage or voltage headroom available for the device will be limited. With a nominal supply voltage of $V_{DD} = 1.5\,\mathrm{V}$ for the 130 nm technology and $V_{DD} = 1.2\,\mathrm{V}$ for the 65 nm technology it is appropriate to assume $0.3\,\mathrm{V} \leq V_{DS} \leq 0.5\,\mathrm{V}$ for an amplifying transistor. In an actual circuit implementation an amplifying transistor is likely to operated in series e.g. with an active respectively passive load and a current source. We choose $V_{DS} = 0.4\,\mathrm{V}$ for the test devices unless noted otherwise. The threshold voltages for the three test devices are listed in Table 4.3. These values for the threshold voltages are provided by the circuit simulator. In general the threshold voltages in the 65 nm technology are higher than for the 130 nm technology. For the test device III V_{TH} is more than $\Delta V_{TH} = 100\,\mathrm{mV}$ higher than for device I in the 130 nm technology. We assume the analogue designer is free to chose the gate potential V_G respectively the overdrive voltage $V_{OV} = V_{GS} - V_{TH}$ of the transistor for optimum bias conditions as long as $V_G \leq V_{DD}$ and $V_{DS} \geq V_{GS} - V_{TH}$. These

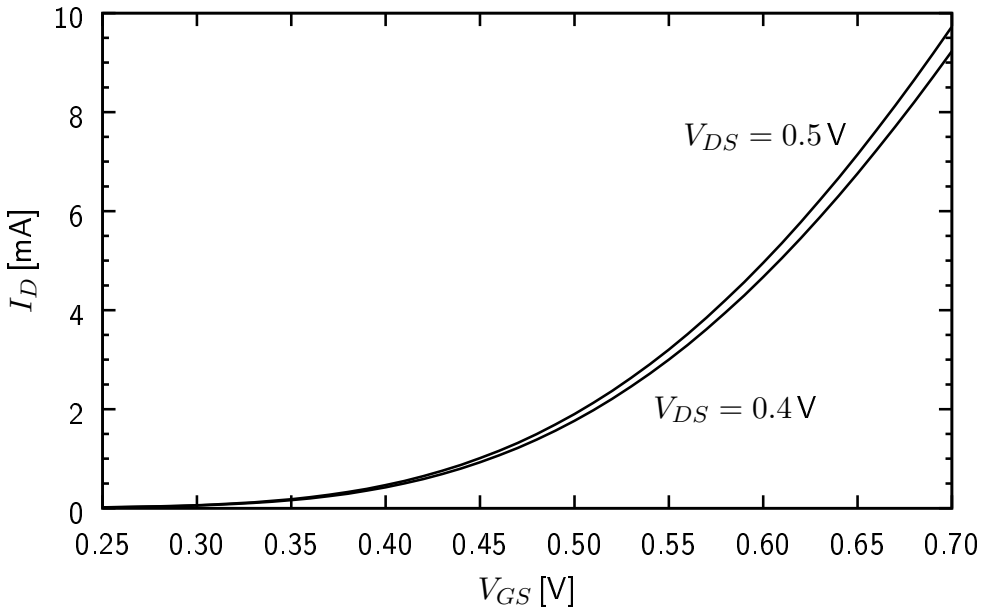


(a) Input characteristic.

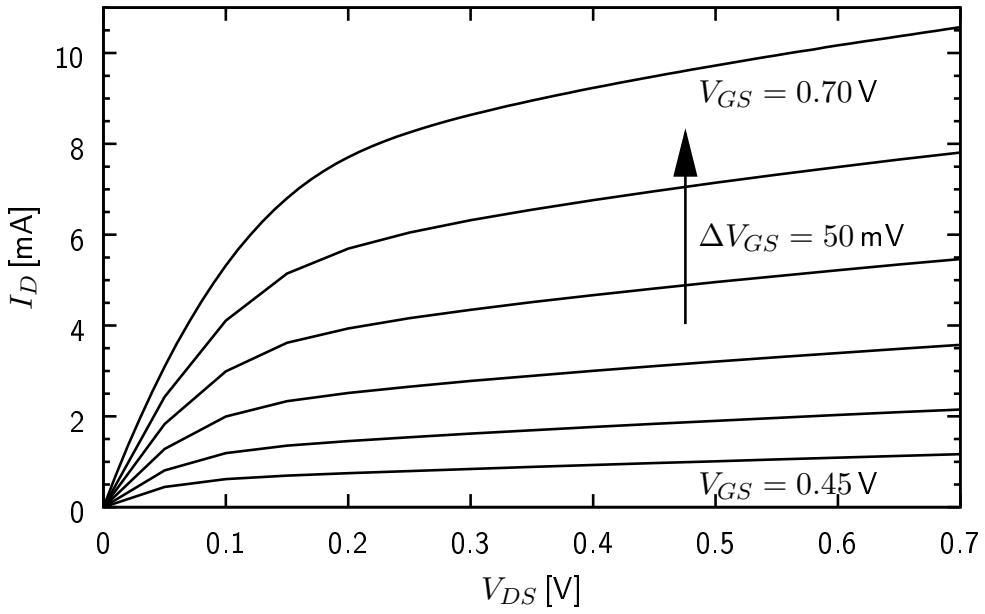


(b) Output characteristic.

Figure 4.8.: Characteristics of an NFET with l =120 nm, w=6.52 μm, n=18 (w_{TOT}/l = 978) (device I) in a 130 nm CMOS technology.

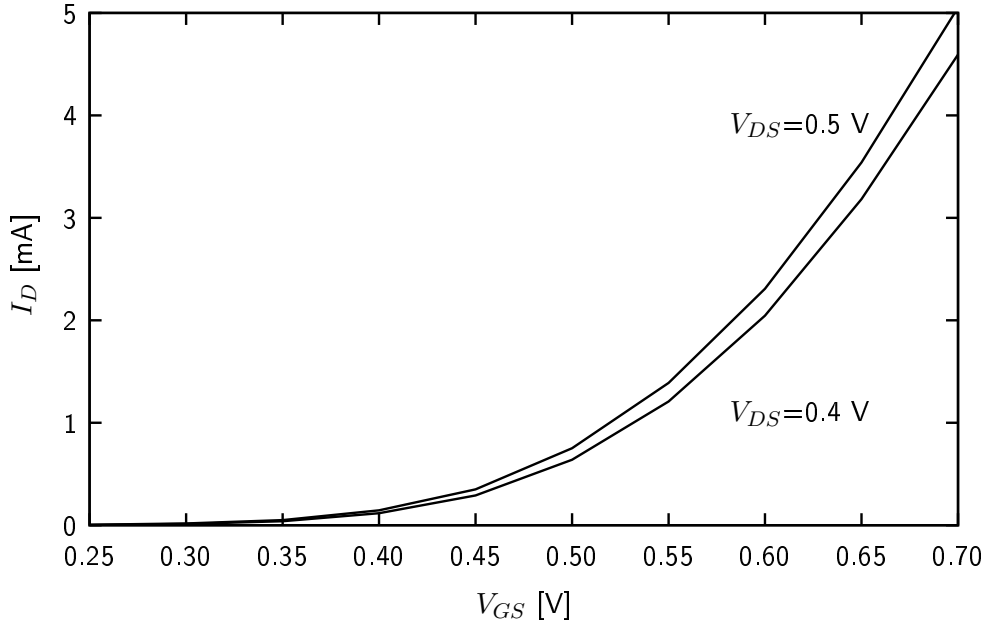


(a) Input characteristic.

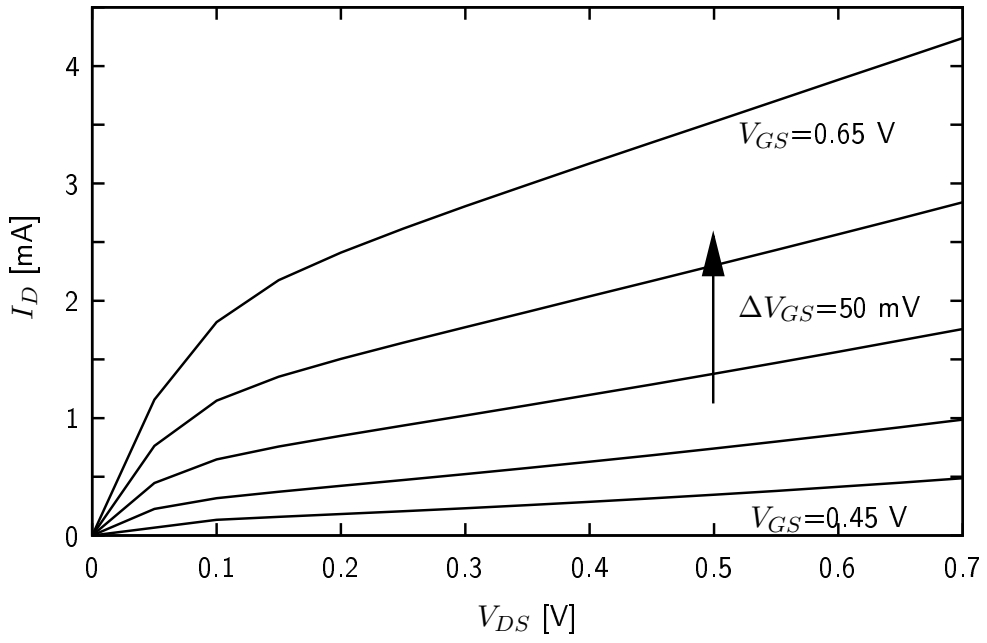


(b) Output characteristic.

Figure 4.9.: Characteristics of an NFET with l =120 nm, w=6.52 μm, n=18 (w_{TOT}/l = 978) (device II) in a 65 nm CMOS technology.



(a) Input characteristic.



(b) Output characteristic.

Figure 4.10.: Characteristic of an NFET with l =60 nm, w=4 μm, n=15 (w_{TOT}/l = 1000) (device III) in a 65 nm CMOS technology.

Table 4.3.: Comparison of the threshold voltages V_{TH} of the three test devices for different V_{DS}.

	Threshold voltage $@V_{DS} = 0.4\,V$	Threshold voltage $@V_{DS} = 0.5\,V$
Unit	[mV]	[mV]
I. $l = 120\,\text{nm}$ in $130\,\text{nm}$	453	451
II. $l = 120\,\text{nm}$ in $65\,\text{nm}$	490	488
III. $l = 60\,\text{nm}$ in $65\,\text{nm}$	571	564

are not considered severe design constraints.
Another point of interest to the analogue designer is the *dc* current consumption of an amplifying circuit. In times when low-power circuits for mobile communication are subject of intense research efforts we impose a constraint on the maximum allowable drain current I_D of the test devices. From the output characteristics of the test devices I (Fig. 4.8(b)) and II (Fig. 4.9(b)) we find that limiting V_{GS} to $V_{GS} \leq 0.7\,\text{V}$ ($V_{OV} \leq 247\,\text{mV}$ for device I, $V_{OV} \leq 210\,\text{mV}$ for device II (cf. Table 4.3)) in turn limits the drain current of these devices to $I_D \approx 9\,\text{mA}$. This current budget is far more than we will want to spend on a single amplifying transistor in a low-power LNA. The empirically obtained value $I_D \approx 2\,\text{mA}$ is considered more adequate by the author. However, for reasons of an objective and more complete comparison, further investigations will feature gate source voltages up to $V_{GS} = 0.7\,\text{V}$ despite the high associated current consumption of device I and II. Nevertheless it should be noted that increasing the overdrive voltage of device I and II to more than $V_{OV} = 50\,\text{mV}$ leads to a severely increased current budget for the transistors. From the simulation results for the intrinsic amplification potential of the devices illustrated in Fig. 4.13 it will become clear that increasing V_{GS} beyond $0.7\,\text{V}$ respectively $V_{OV} = 129\,\text{mV}$ for device III (cf. Table 4.3) is also not appropriate. The details will be elaborated later on in this section.
In order to account for the previously mentioned different threshold voltage values, future simulation results are presented referred to the applied overdrive voltage. The threshold voltage variation is less than $\Delta V_{TH} = 1\,\text{mV}$ in the input voltage range of interest $0.45\,\text{V} \leq \text{V}_{\text{GS}} \leq 0.70\,\text{V}$.

4.2.1.2. Comparison of the Amplifying Potential

In the first order model a CMOS transistor is nothing but a voltage controlled current source. The constant factor between input voltage and output current in this first order model is the input transconductance g_M of a transistor. The simulation results for g_M of the three test devices is depicted in Fig. 4.11. For moderate $V_{OV} \leq 90\,\text{mV}$ device II exhibits the largest g_M. For small $V_{OV} \leq 30\,\text{mV}$ device III exhibits a larger g_M than device I but the g_M of device III is always inferior to the g_M of device II. In general the dependence of g_M on V_{OV} is strongest for device I. From (4.17) we expect that the g_M of device II is twice that of device III. However, simple short channel theory does not prove itself for this comparison. Most noteworthy the g_M of all three devices depends on V_{OV}. The relation of g_M and V_{OV} appears to be quite linear up to moderate V_{OV} as suggested by (4.7). Table 4.4 offers a comparison of the achievable g_M for identical I_D and identical V_{DS} of the three devices (cf. (4.9)). We note that for the bias conditions mentioned the designer can acquire the largest g_M from device I in the 130 nm CMOS technology. The g_M of device III with $l = 60\,\text{nm}$ is lowest.

Table 4.4.: Comparison of the amplifying potential of the three test devices for identical $I_D \approx 2.08\,\text{mA}$ and $V_{DS} = 0.4\,\text{V}$.

.

	V_{OV}	g_M	g_{DS}	g_M/g_{DS}	g_M/I_D
Unit	[mV]	[mS]	[mS]	[1]	[S/A]
I. $l = 120\,\text{nm}$ in $130\,\text{nm}$	56.2	27.0	2.3	11.8	13.0
II. $l = 120\,\text{nm}$ in $65\,\text{nm}$	24.5	23.2	1.6	14.5	11.2
III. $l = 60\,\text{nm}$ in $65\,\text{nm}$	28.6	20.5	2.7	7.6	9.9

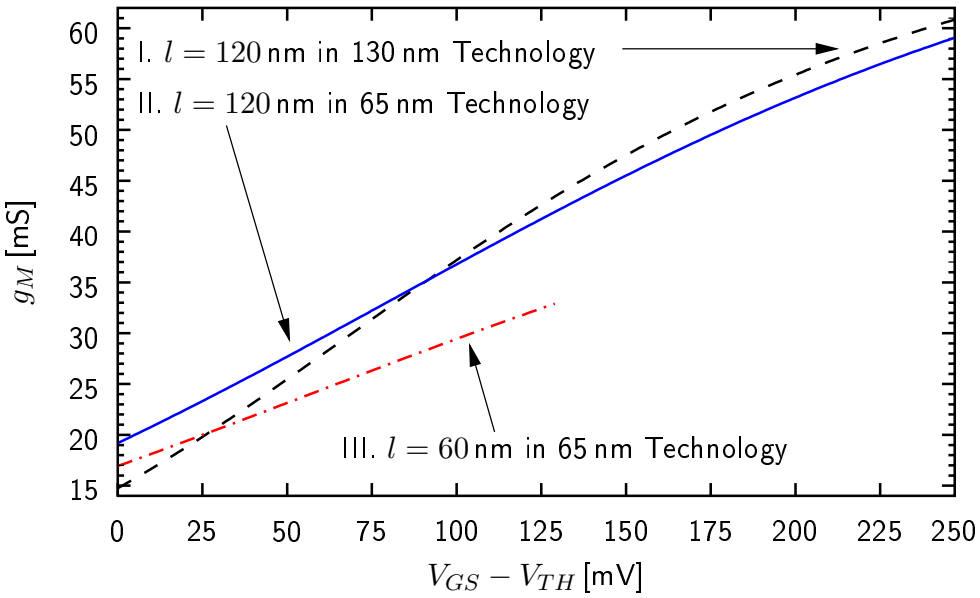


Figure 4.11.: Comparison of the transconductance g_M vs. $V_{GS} - V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

Investigating only the g_M of the three devices is not sufficient in order to judge the RF amplifying potential of the devices. The output conductance g_{DS} depicted in Fig. 4.12 is also of importance since (2.36) and (2.54) stress that in the commonly known LNA circuit topologies the voltage gain of the amplifiers is set by g_M of the active transistor and by a shunt circuit of an external load resistor and g_{DS}. Expressed in other words that means that the voltage gain of an amplifier cannot be raised beyond a certain limit set by the g_{DS} of the amplifying transistor. The g_{DS} of device III is always larger than that of the devices I and II for identical V_{OV} (at least 20 % up to moderate overdrive voltages). The g_{DS} values increase for all three devices with the applied V_{OV}. Furthermore, the absolute values for g_{DS} ranging up to 5 mS for moderate overdrive voltages suggest that the commonly made assumption of $g_{DS} \to 0$ made for simple calculations is far from true for modern sub-micron CMOS technologies.
Picking up the idea that the voltage gain of CS LNA or CG LNA is ruled by g_{DS} of the amplifying device we can define the maximum intrinsic voltage gain of a transistor by setting the absolute value of g_{DS} in relation to its g_M. Adding an external load impedance to an amplifier will always

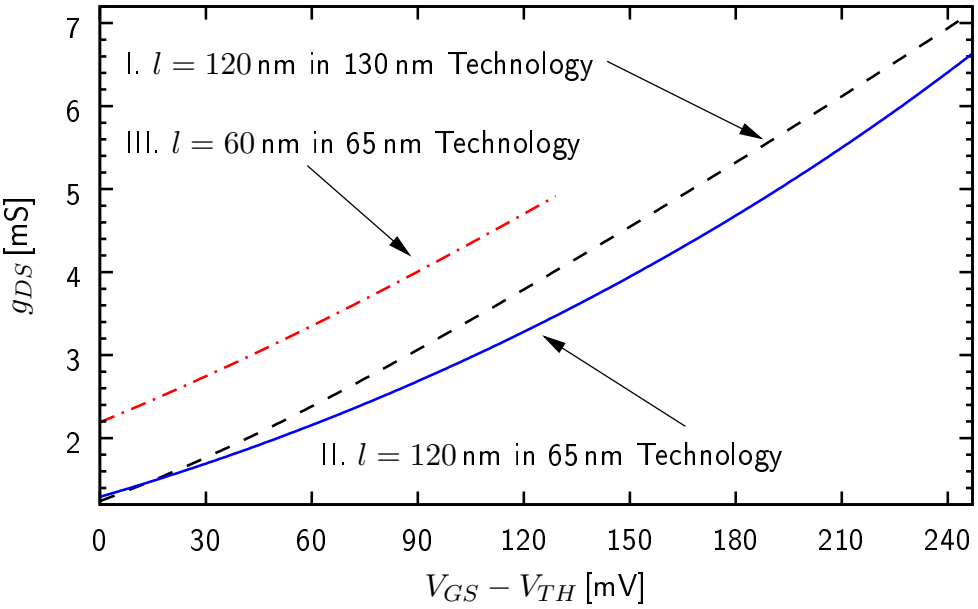


Figure 4.12.: Comparison of the output conductance g_{DS} vs. $V_{GS} - V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

result in a voltage gain smaller than g_M/g_{DS} as the overall impedance of a shunt load circuit is always smaller than the smallest impedance of the shunt connected elements. The comparison of the ratio of g_M/g_{DS} (cf. Fig. 4.13) gives the best insight into the intrinsic amplifying potential of the test devices. Finally we see what has been hinted on earlier. Increasing V_{OV} to values $V_{OV} \geq 120\,\text{mV}$ for device III lowers g_M/g_{DS} to 7. The value $g_M/g_{DS} = 7$ is considered the lower limit of the amplifying potential of an active transistor in an amplifier implementation. That is the reason why larger V_{OV} for device III have been excluded from this comparison. Although the value of 7 is chosen somewhat arbitrarily we are confident that most designers of analogue circuitry will agree to a similar value. Keep in mind that a load impedance connected to the drain node of the transistor in an LNA implementation will further reduce the available voltage gain.

As expected from the previous observations device II performs best a given V_{OV}, whereas the intrinsic amplifying potential of device III is worst. For low V_{OV}, g_M/g_{DS} of device II overcomes g_M/g_{DS} of device I by almost 25 %. For the same low V_{OV} the g_M/g_{DS} of device II overcomes the g_M/g_{DS} of device III by almost a factor of two. The g_M/g_{DS} of device I still overcomes the g_M/g_{DS} of device III by 50 % for low V_{OV}. When we analyse g_M/g_{DS} for the devices under identical bias conditions for all three devices in terms of voltage headroom and bias current spent (Table 4.4), we come to similar conclusions regarding the intrinsic amplifying potential. Device II offers the best g_M/g_{DS}, device III offers the worst g_M/g_{DS}.

With low-power circuitry in the focus of intense research an additional comparison of the ratio g_M/I_D is worth taking a closer look at. The fraction g_M/I_D expresses how much transconductance a designer obtains for a certain amount of *dc* current spent on an amplifying transistor. This comparison clearly favours device I. Whereas *dc* current exploit of device II and device III in the 65 nm technology differs by about 10 % in favour of device II, device I surpasses even the g_M/I_D of device II by 30 % for low V_{OV}. The conclusions drawn from Table 4.4 for identical bias

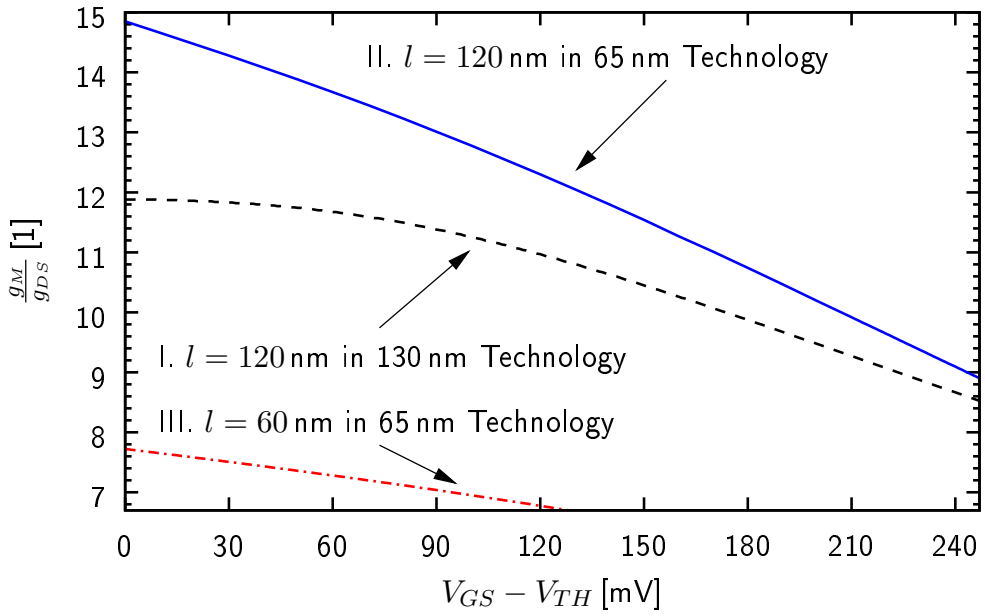


Figure 4.13.: Comparison of the intrinsic amplifying potential g_M/g_{DS} vs. $V_{GS}-V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\mathrm{V}$ and $w/l \approx 1000$.

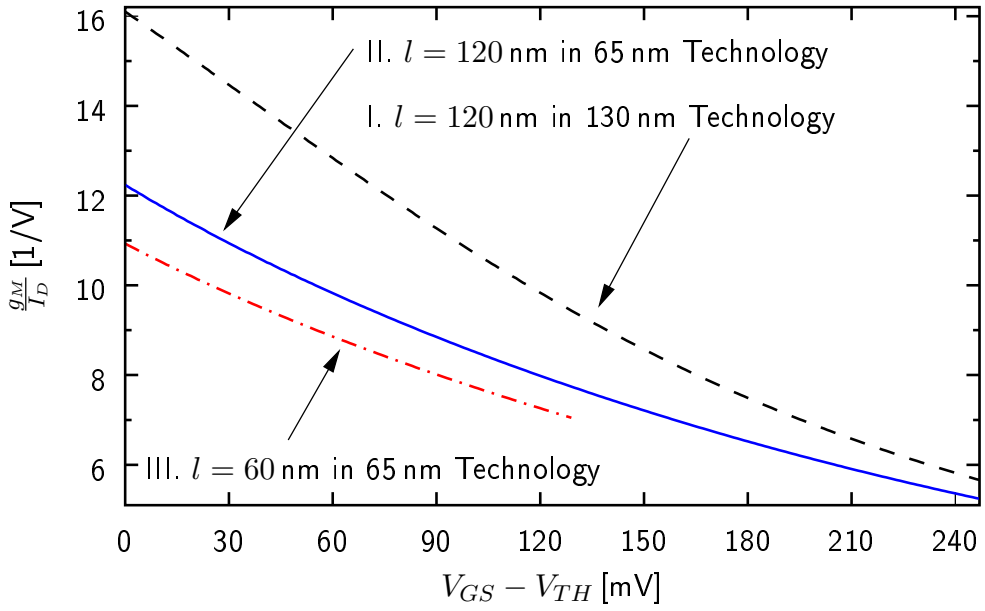


Figure 4.14.: Comparison of the transconductance g_M achieved per *dc* current I_D spent vs. $V_{GS}-V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\mathrm{V}$ and $w/l \approx 1000$.

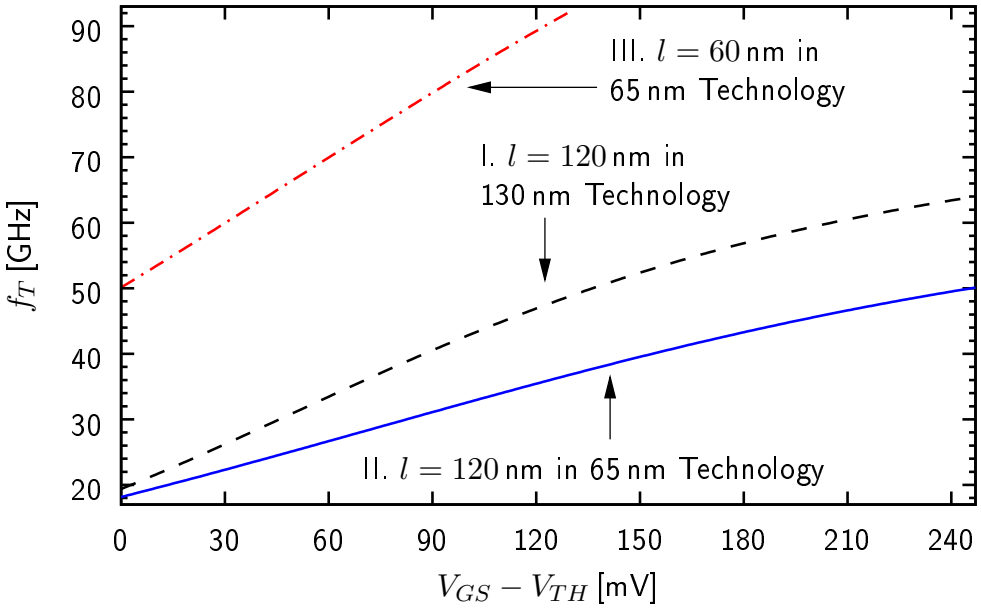


Figure 4.15.: Comparison of the calculated transit frequency f_T vs. $V_{GS} - V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

Table 4.5.: Comparison of the calculated f_T of the three test devices for identical $I_D \approx 2.08\,\text{mA}$ and $V_{DS} = 0.4\,\text{V}$.

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	V_{OV}	f_T
Unit	[mV]	[GHz]
I. $l = 120\,\text{nm}$ in $130\,\text{nm}$	56.2	32.5
II. $l = 120\,\text{nm}$ in $65\,\text{nm}$	24.5	21.4
III. $l = 60\,\text{nm}$ in $65\,\text{nm}$	28.6	59.3

conditions for the three devices in terms of voltage headroom and bias current also make device I the device of choice when a certain amount of available *dc* current is be to used most efficiently in an amplifying circuit.

The transit frequency f_T of the three test devices has been calculated according to (4.11) and is compared in Fig. 4.15. Not surprisingly device III benefits from the smallest dimensions of the three devices resulting in the highest f_T. Although device II outperformed device I in terms of g_M, f_T calculated for device II is lower. This indicates higher parasitic capacitance values associated to the gate terminal of a transistor in the 65 nm technology compared to a transistor implementation in the 130 nm technology with similar lateral dimensions.

The focus of this thesis is on the implementation of a GSM receiver front-end operating an RF signal frequency $f_{RF} \leq 2\,\text{GHz}$. At first glance $f_T \geq 18\,\text{GHz}$, about one decade higher than f_{RF}, for all three test devices seems high enough for the target application. Remember that the device geometry for the application circuitry can still be adjusted if necessary. Figure 4.15 illustrates that a higher f_T is easy to achieve when higher V_{OV} respectively I_D is applied.

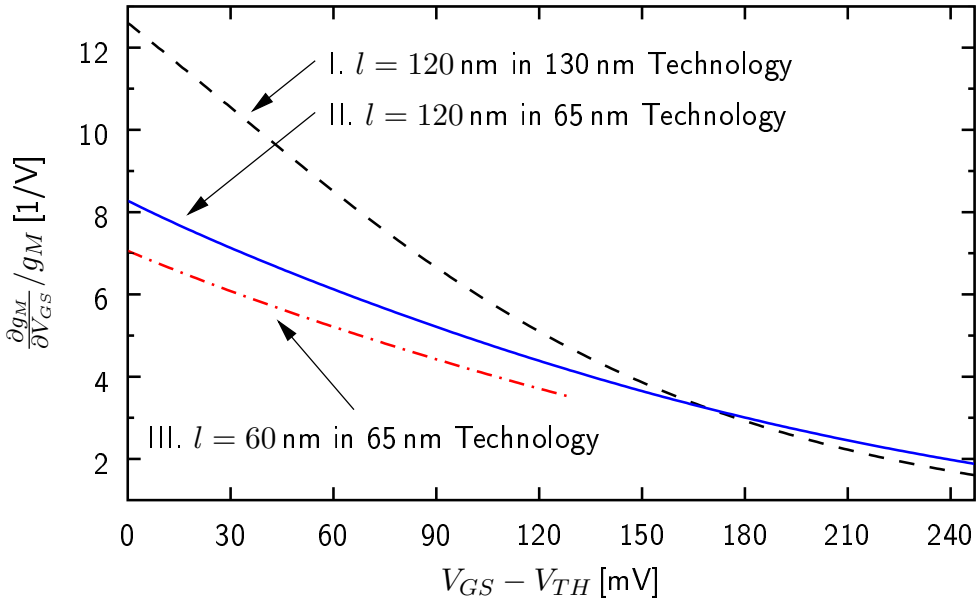

Figure 4.16.: Comparison of the ratio of the derivative of the transconductance to the transconductance $\frac{\partial g_M}{\partial V_{GS}} / g_M$ vs. $V_{GS} - V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

4.2.1.3. Linearity

One of the linearity characteristics for an amplifying device is its even order distortion. Following a Taylor Series approach a quantitative measure for the even order distortion of a transistor is given by

$$\frac{\partial^2 I_D}{\partial V_{GS}^2} = \frac{\partial g_M}{\partial V_{GS}}. \tag{4.29}$$

The term $\partial g_M / \partial V_{GS}$ needs to be referred to g_M because it gains its significance only presence of an appropriate g_M i.e. a small $|\partial g_M / \partial V_{GS}|$ does not necessarily describe a useful linear amplifying device if the overall g_M is close to zero.
The plots in Fig. 4.16 reveal that device I exhibits the largest even order distortion relative to its absolute transconductance up to moderate V_{OV} values. Device III performs best here. These tendencies are confirmed by the data listed in Table 4.6 when the comparison is made at a bias point with an identical I_D. However, we have to keep in mind that when we use an amplifying transistor in a differential stage, theory tells us that for ideal matching even order distortion is cancelled in a differential system. The even order non-linearity that challenges the performance of a wireless receiver originates from several sources in a complex system (cf. Section 3.2.3). The even order distortion of the single individual transistor device is only of minor concern for the performance of the differential receiver front-end presented in this thesis.

Another important linearity characteristic of an amplifying transistor e.g. in an LNA implementation is its odd order distortion performance. Other than the even order distortion, odd order distortion does not ideally cancel in a system with a balanced signal path. In order to specify a quantitative measure for odd order distortion we compare the second derivative of the transconductance for the gate source voltage $\partial^2 g_M / \partial V_{GS}^2$ over the absolute value of the transcon-

Table 4.6.: Comparison of the linearity performance metrics of the three test devices for identical $I_D \approx 2.08\,\mathrm{mA}$ and $V_{DS} = 0.4\,\mathrm{V}$.

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	V_{OV}	$\frac{\partial g_M}{\partial V_{GS}}/g_M$	$\frac{\partial^2 g_M}{\partial V_{GS}^2}/g_M$
Unit	[mV]	[1/V]	[1/V^2]
I. $l = 120\,\mathrm{nm}$ in $130\,\mathrm{nm}$	56.2	8.8	10.7
II. $l = 120\,\mathrm{nm}$ in $65\,\mathrm{nm}$	24.5	7.3	17.4
III. $l = 60\,\mathrm{nm}$ in $65\,\mathrm{nm}$	28.6	6.1	7.0

ductance g_M (cf. (4.29)). From the classical long channel theory expressed in (4.5) we expect $\partial^2 g_M/\partial V_{GS}^2 \leq 0$. The term $(\partial^2 g_M/\partial V_{GS}^2)/g_M$ exhibits a strong relation to Section 2.4:

$$\sqrt{\left|(\frac{\partial^2 g_M}{\partial V_{GS}^2})/g_M\right|^{-1}} \propto \sqrt{\left|\frac{\alpha_1}{\alpha_3}\right|} \propto A_{1dB} \propto A_{IP3}, \tag{4.30}$$

when first order modelling a transistor as a voltage controlled current source.
However simulation results depicted in Fig. 4.17 prove that $\partial^2 g_M/\partial V_{GS}^2$ is positive for low V_{OV}. An ideal linear device operating without any distortion is defined by $\partial^2 g_M/\partial V_{GS}^2 = 0$. Thus a deviation from the zero, positive or negative, $|\partial^2 g_M/\partial V_{GS}^2|$ describes the non-linear behaviour in a general sense. Most noteworthy the comparison reveals that device I suffers from the strongest distortion for small overdrive voltages. Under identical bias conditions for the three devices in terms of voltage headroom and bias current device I shows moderate non-linearity levels compared to the devices II and III. Interestingly the linearity performance of device III is best under these bias conditions. This goes along well with the idea that lead to (4.16) for the large signal modelling of a short channel device.

4.2.1.4. Noise Performance Comparison

In order to compare the noise performance of the three test devices, the devices are biased to an operating point for which the input transconductance g_M of the devices is identical. This is considered reasonable due to the dependence of e.g. thermal noise and flicker noise on g_M according to theory (cf. (4.21) and (4.22)).
The flicker noise corner frequency that is extracted from the output current noise spectra in Fig. 4.18 is about $f_C = 10\,\mathrm{MHz}$ for all test devices with a channel length $l = 120\,\mathrm{nm}$. The corner frequency extracted for device III with $l = 60\,\mathrm{nm}$ channel length is about three to four times that of the 120 nm devices I and II. The flicker noise spot density in $\mathrm{A}/\sqrt{\mathrm{Hz}}$ at $f = 1\,\mathrm{kHz}$ of the $l = 120\,\mathrm{nm}$ devices is about half that of the $l = 60\,\mathrm{nm}$ device. If we compare the flicker noise density at 1 kHz of device II and III we find that it is in good accordance with (4.21) for two devices in the same technology but with different geometry. Theory predicts a ratio of 2.0 whereas the model based simulation results indicate a ratio of 2.2 for the noise levels. The increased flicker noise levels for transistors with gate lengths $l = 60\,\mathrm{nm}$ is especially relevant for baseband circuits. These circuits will prefer transistors with longer gate lengths.
The thermal noise density levels in $\mathrm{A}/\sqrt{\mathrm{Hz}}$ of the three test devices extracted at $f = 5\,\mathrm{GHz}$

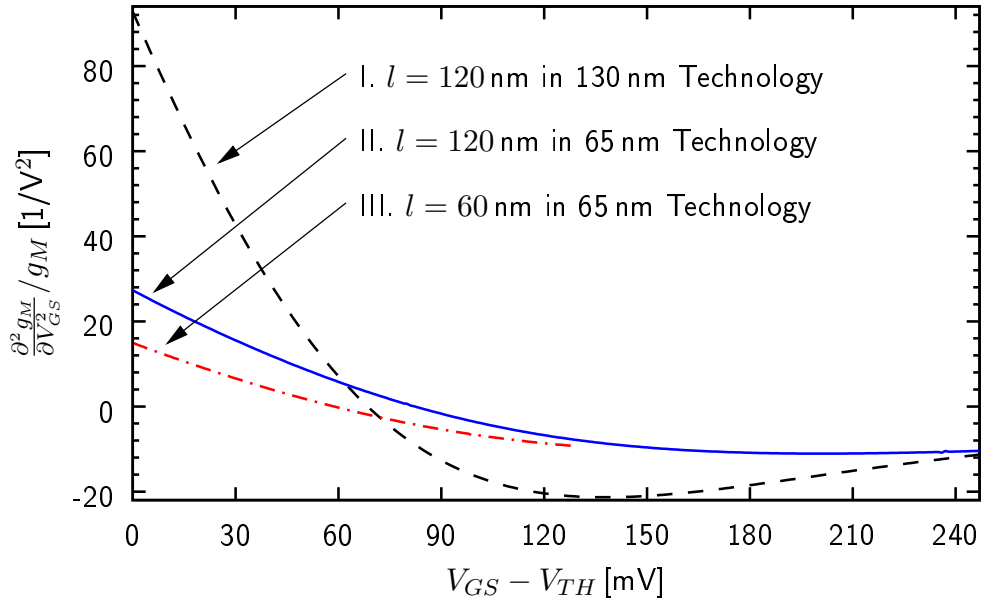


Figure 4.17.: Comparison of the ratio of the second derivative of the transconductance to the transconductance $\frac{\partial^2 g_M}{\partial V_{GS}^2}/g_M$ vs. $V_{GS} - V_{TH}$ of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

differ by 20 %. The thermal noise density level of device I is lowest, the thermal noise level of device III is highest. The increased thermal noise level affects the noise performance of circuit blocks operating at RF e.g. LNA circuits. Due to larger parasitic capacitances associated to longer transistor gates and the higher operating frequency, these circuit blocks cannot as easily use transistors with longer gate lenghts in order to overcome the inferior noise performance of small transistors as has been suggested for baseband circuits in the previous paragraph.
Detailed performance metrics for the comparison of the noise performance are given in Table 4.7. Induced gate noise affects the noise performance only for frequencies well beyond $f = 10\,\text{GHz}$ and is thus not considered relevant for the applications in the focus of this work.
Figure 4.19 illustrates the noise performance of the three devices in terms of the equivalent input noise voltage density. The plot is given to make this analysis complete but is not discussed in detail as the depicted results are equivalent to those in Fig. 4.18.

For completeness reasons additional noise simulation curves for identical overdrive voltages V_{OV} and identical drain currents I_D are placed in Appendix A.3 of this work.
Appendix A.3 also contains additional plots that compare the further performance characteristics of the three test devices.

4.2.2. Capacitors

We are now going to compare the capacitance density that different capacitor devices offer in the 130 nm and the 65 nm process technology. The 130 nm technology offers MIM-caps placed in the top metal layers whereas the 65 nm technology offers VPP-caps for analogue RF design. The VPP-caps consist of multiple layers. The via structure can reach down from metal layer 5 to the

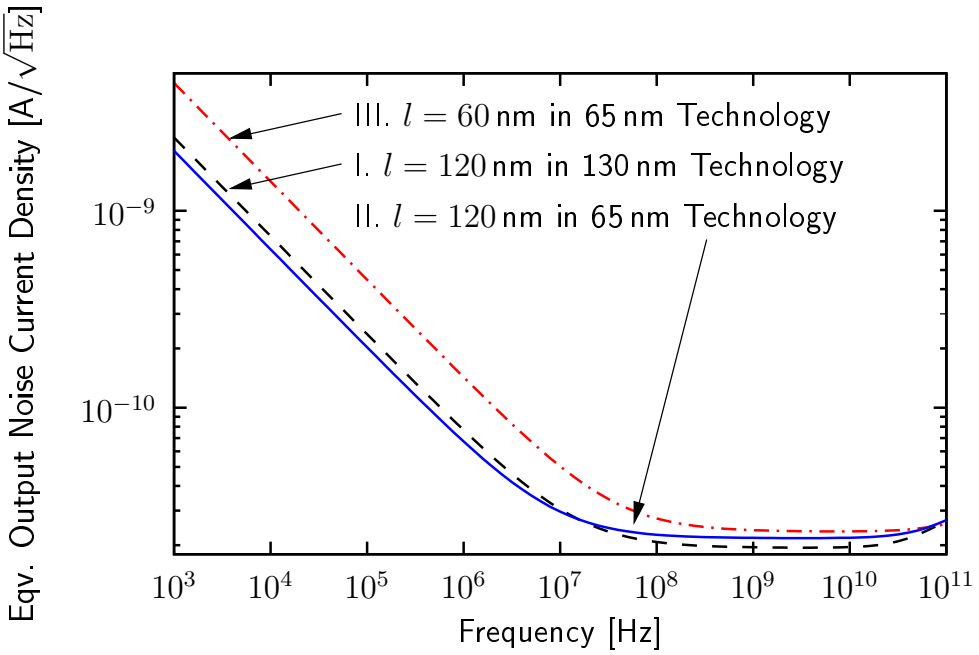


Figure 4.18.: Comparison of the equivalent output noise current density of the three test devices for $V_{DS} = 0.4\,\mathrm{V}$, $w/l \approx 1000$ and $g_M = 20.6\,\mathrm{mS}$.

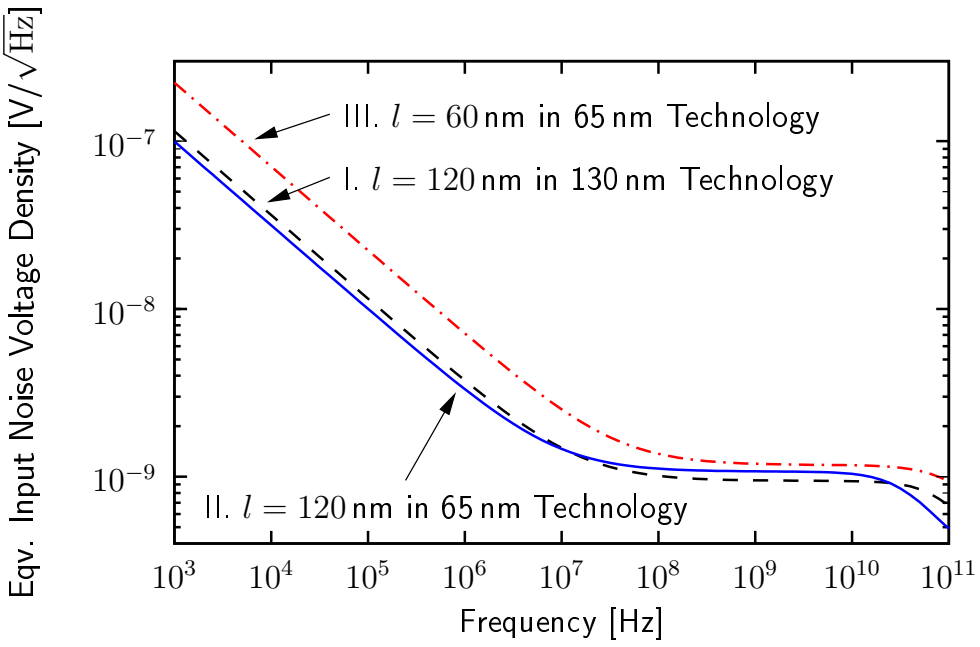


Figure 4.19.: Comparison of the equivalent input noise voltage density of the three test devices for $V_{DS} = 0.4\,\mathrm{V}$, $w/l \approx 1000$ and $g_M = 20.6\,\mathrm{mS}$.

Table 4.7.: Comparison of the output referred noise characteristics of the three test devices when biased to the same input transconductance $g_M \approx 20.6\,\text{mS}$ ($V_{DS} = 0.4\,\text{V}$) extracted from Fig. 4.18.

	I_D	V_{OV}	Thermal noise density @5 GHz	Flicker noise corner frequency	Flicker noise density @1 kHz
Unit	[mA]	[mV]	[pA/$\sqrt{\text{Hz}}$]	[MHz]	[nA/$\sqrt{\text{Hz}}$]
I. $l = 120\,\text{nm}$ in 130 nm	1.4	28.6	19.5	13	2.4
II. $l = 120\,\text{nm}$ in 65 nm	1.7	8.2	21.8	9	2.0
III. $l = 60\,\text{nm}$ in 65 nm	2.1	28.6	23.5	40	4.5

first metal layer 3, metal layer 2 or even metal layer 1. Both technologies offer horizontal parallel plate sandwich capacitors (HPP-caps) between the lower metal layers but without a high-k dielectric and NMOS-caps with special n-well implant. The HPP sandwich capacitors range from metal layer 1 up to metal layer 4 in the 130 nm technology whereas they reach up to metal layer 5 in the 65 nm technology. The MOS-caps are similar to NFET devices in the physical design but consist of an additional implanted n-well that encloses source and drain diffusions.

When comparing the capacitance densities of the different types of capacitors in Table 4.8 it turns out that the capacitance density of the MIM-caps is 12 % to 24 % higher than that of the VPP-caps reaching down to metal layer 1. The difference in capacitance density is even higher if we compare MIM-caps with VPP-caps reaching down to metal layer 3 as the capacitance density of the VPP-caps is down by half. The reason MIM-caps are compared directly to VPP-caps is that these types of capacitors are typically used for compact capacitors of moderate size in the RF signal path. As the MIM-cap occupies the top metallisation only it is advantageous over the VPP-caps because it offers the opportunity to place wiring or substrate devices underneath the capacitor in physical designs and its physical vertical distance to the substrate reduces parasitic effects. Thus for the analogue RF designer looking for compact capacitor devices with a linear characteristic the MIM-cap in the 130 nm technology offers a capacitance density that is about two to three times higher than that of the VPP-cap (reaching down to metal 3 only) in the 65 nm technology. However, it should be noted that a capacitance in the RF signal path (aside maybe from large *ac* coupling capacitances) is not likely to significantly contribute to the overall die area consumption of a complete wireless transceiver as the capacitance values required e.g. by baseband filtering applications will be much larger because of the lower operating frequencies.
Another kind of linear metal capacitors are the HPP-caps. Compared to the VPP-caps and MIM-caps the capacitance density is low due to the low-k_{DIEL} dielectric and thus these devices are of limited practical use for high integration low-cost designs. However, we observe a ratio of more than two for the capacitance density of HPP-caps in the 65 nm technology and the 130 nm technology.
The MOS-caps bear the highest capacitance densities in the comparison. Being notorious for their non-linearity and their TC 'pure' MOS-caps are not likely to be found in the signal path of an analogue receiver. The capacitance density of MOS-caps in the 65 nm technology and the 130 nm technology is very similar.
If higher capacitance densities are required in analogue circuit design for a compact physical implementation, the possibilities of capacitor-combination-devices have to be investigated. The

Table 4.8.: Comparison of the capacitance density that can be achieved in the process technologies compared here. Capacitance densities for VPP-caps without brackets are given for devices that range from metal 5 down to metal 1. Capacitance densities for VPP-caps in brackets are given for devices that range from metal 5 down to metal 3. All capacitance densities are referred back to the density of a 100 fF MIM-cap in the 130 nm technology.

	130 nm Technology	65 nm Technology
	Relative capacitance density	
	[%]	
MIM-cap@100 fF	100.0	x
MIM-cap@10 pF	94.8	x
VPP-cap@100 fF	x	76.3 (36.8)
VPP-cap@10 pF	x	88.3 (48.0)
MOS-cap@100 fF	260.4	270.7
MOS-cap@10 pF	260.4	263.2
HPP-caps@100 fF	13.1	31.9
HPP-caps@10 pF	13.9	30.4

author of [26] reports that e.g. with a shunt connected circuit of VPP-caps and anti-parallel MOS-cap structures the die area saving can be up to more than 50 % compared to default VPP-caps. Sophisticated device sizing of the anti-parallel MOS-caps will eliminate the overall device non-linearity almost completely. These devices appear suitable where large capacitance values $C \geq 1\,\text{pF}$ are necessary for circuit operation at baseband frequencies or even for frequency ranges of a few Megahertz.

4.2.3. Inductors

As no coil implementations have been available in the design libraries of the technologies at hand and there are no coils used in the front-end circuits discussed in this work, a design comparison for coils is not presented.

4.3. What to expect from Conventional CMOS Scaling?

This section discusses the expectations on the performance of down-scaled CMOS transistors. The term 'conventional' in the headline of this section is used to express that the presented results are derived from CMOS shrink implementations of the past.
We have already seen from (4.17) that theory tells us that in the presence of short channel effects the transconductance g_M of a FET becomes independent of the channel length l and the overdrive voltage V_{OV}. It does no longer improve for a given width w with the scaling of the minimum feature size l as the long channel equation (4.9) suggests.
From (4.18) we see that not only the absolute value of the transconductance g_M but also the

value of the transconductance referred to the DC drain current spend is cut down by a factor of two compared to the long channel regime (cf. (4.10)).
If we assume that (4.11) is valid for short channel FETs as well as for long channel FETs and we insert (4.9) into (4.11), we obtain

$$f_T \propto \frac{V_{OV}}{l^2} \tag{4.31}$$

for the transit frequency of a long channel device whereas inserting (4.17) into (4.11) predicts

$$f_T \propto \frac{v_{MAX}}{l} \tag{4.32}$$

for a short channel device. It is assumed that C_{GS} dominates the input capacitance for both types of devices. In practice, however, the influence of the overlap capacitances in a short channel device may even reduce the achievable transit frequency by a factor of three [35]. Evidently short channel effects limit expectations of speed enhancements with technology scaling.
The authors of [60] claim that less bias current is necessary to achieve a given transit frequency or a specific noise figure when the transistor length decreases.
At first glance a lower flicker noise is expected with technology scaling from (4.21) as the gate oxide thickness shrinks and the gate capacitance increases for fixed device dimensions w and l. This positive virtue is overcompensated because the gate oxide is no longer pure thermal oxide but nitrided oxide in advanced process technologies. The inferior dielectric-surface interface may actually lead to an increased $1/f$ noise [60].
The issue of a lowered supply headroom and a decreased device linearity is addressed in [55]. For short channel devices with $V_{DS} = 1.5\,\mathrm{V}$ and $V_{SB} = 0\,\mathrm{V}$ it is observed that

- the device linearity $V_{IP3} \propto \sqrt{g_M/(\partial^2 g_M/\partial V_{GS}^2)}$ (gate-source input voltage for which the device transfer characteristic reaches the IP_3) decreases along with the channel length l and that the local minimum of the distortion vs. V_{OV} is moved to lower gate overdrive voltages V_{OV} when the channel length is reduced. The trend of decreasing linearity is true not only for transistors with different channel lengths in a specific technology node (cf. Fig. 4.20) but also for a full scaling in different technology nodes (cf. Fig. A.9). The trend of decreasing linearity is true for NMOS as well as PMOS transistors.The reason is the increasing effect of series resistance and velocity saturation.

- the device linearity V_{IP3} decreases along with the channel length l for a constant drain current I_D and a given channel width w (cf. Fig. A.11) at different technology nodes. In order to maintain a constant V_{IP3} it is suggested to scale down the channel width w along with the channel length l.

- intense substrate doping levels N_A help to increase the local minimum of linearity V_{IP3} vs. V_{OV} and help to move the local maximum of linearity to higher overdrive voltages V_{OV} (cf. Fig. A.12). The reason given is an increase in body effect.

- the local minimum of device linearity decreases along with the gate oxide thickness t_{OX}. The reason is a decrease of the body effect and an increase in poly depletion. The minimum distortion vs. I_D or respectively minimum distortion vs. V_{OV} occurs at a constant drain current I_D respectively a constant gate overdrive V_{OV} independent of the varied oxide thickness (cf. Fig. A.13 and Fig. A.14). For high gate overdrive voltages V_{OV} device distortion is governed by the velocity saturation of charges travelling in the conducting channel.

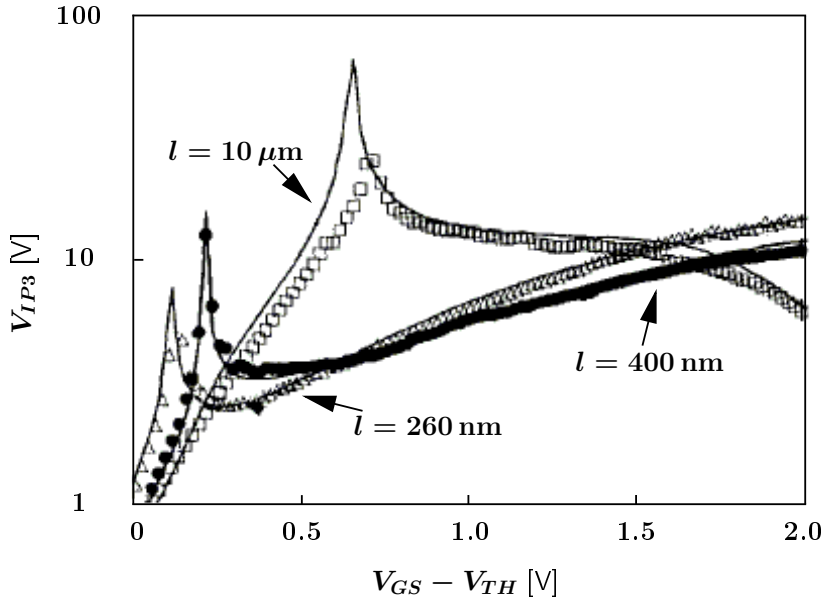


Figure 4.20.: Device linearity of NFETs given as V_{IP3} vs. V_{OV} for different channel lengths l in a specific CMOS technology for $t_{OX} = 10\,\text{nm}$, $N_A = 5 \cdot 10^{17}\,\text{cm}^{-3}$ and $w = 10\,\mu\text{m}$. Dots indicate measurement result results. Lines indicate simulation result results [55].

In a model based device comparison between transistor devices implemented in the available 130 nm and 65 nm CMOS process technology, the trends presented in [55] could only partly be confirmed. The model based comparison (cf. Fig. 4.21) investigates V_{IP3} vs. V_{OV} of a transistor with $l = 120\,\text{nm}$ in the 130 nm technology, a transistor with $l = 60\,\text{nm}$ and a transistor with $l = 120\,\text{nm}$ in the 65 nm technology. It is observed that in the 65 nm technology the local minimum of V_{IP3} moves to lower overdrive voltages with a decreasing channel length, which is in accordance with [55]. But it is also observed that V_{IP3} is inferior in the 130 nm technology compared to minimum channel length devices in the 65 nm technology for $V_{OV} \leq 200\,\text{mV}$. This contradicts the results presented in [55]. In addition it is pointed out that due to the high overdrive voltage and due to the high drain-source voltage $V_{DS} = 1.5\,\text{V}$ applied in [55] and the model based comparison of V_{IP3} in Fig. 4.21, the power consumption of the devices under test is relatively large ($P > 15\,\text{mW}$).

The author of [60] proposes to take advantage of the velocity saturation in the short channel regime by applying a high gate bias in order to linearise FETs. This approach also suffers from an increased *dc* power consumption.

Table 4.9 summarises a comparison of device characteristics of four generations of process technologies. Most interestingly, although the absolute g_M value increases with the shrink in technology, the achievable gain of a transistor g_M/g_{DS} decreases. This is because the increase in the drain-source transconductance g_{DS} overcompensates the improved g_M.

Besides, Table 4.9 indicates the emergence of drawbacks not only for analogue circuit designers with technology scaling. Digital designers have to cope with a severely increased power consumption of their blocks. The current flowing into the gate of a FET increased nearly by five orders of

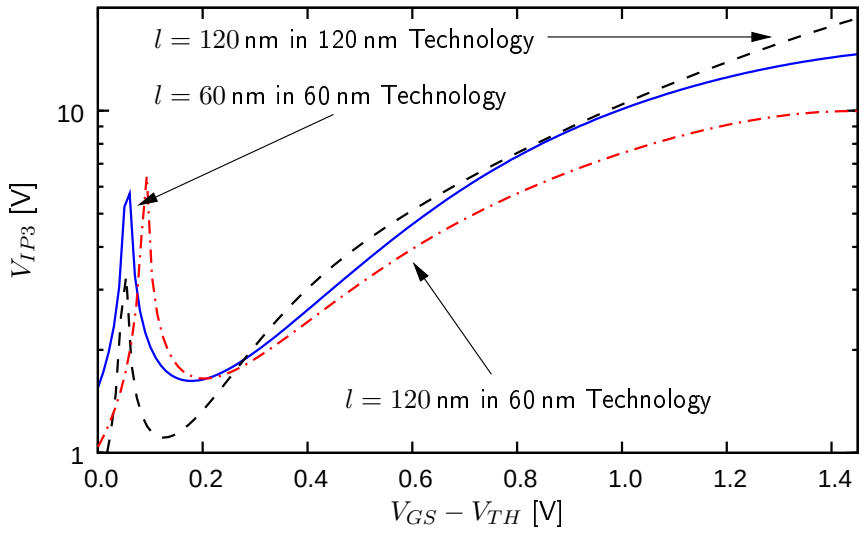


Figure 4.21.: Model based device comparison of V_{IP3} for the 130 nm and the 65 nm process technology. The device width is $w = 13.04\,\mu$m and the drain-source voltage for all three devices is $V_{DS} = 1.5\,$V.

magnitude with a technology scaling from l=250 nm to l=90 nm. In addition the on to off ratio I_{ON}/I_{OFF} degrades by a factor of 500 at the same time.

4.4. Conclusion

The former engine for advancements in shrinking modern process technologies has ran out of fuel for analogue circuit design below $f = 10\,$GHz. With the design of analogue circuit blocks for mobile applications of the 2 G to 4 G generations of communication in focus there is no need for further improvements of f_t. The noise performance, the achievable gain and the linearity are the more crucial performance characteristics of active devices. Especially the analogue RF designer is encouraged to resist the habit to chose transistors with a minimum allowable channel length by default. In order to preserve the amplifying potential of the transistor a non-minimum channel length is often helpful rather than harmful. For current mirror implementations the use of transistors with an extended gate length is commonly accepted and advised. For RF applications operating far from the transit frequency of the employed transistors the use of devices with an extended channel length will surely become common practice in the future in order to preserve the analogue character of the device.
Not only the inferior noise performance of the individual transistor device itself, but also the combination with a lower amplification potential raises the lower boundary of the dynamic range in analogue circuit designs (cf. (2.9)).
The upper boundary for the dynamic range is diminished by a lowered supply voltage from one technology generation to the next. Concerning the influence of technology scaling on the linearity of individual transistor devices different results are presented. According to the model based device comparison the higher order distortion referred to the transconductance of the transistor devices of the 65 nm process technology is superior to that of the 130 nm technology. According

Table 4.9.: Comparison of FET device characteristics for various technology generations [60] .

Process	0.25 μm ('98)	0.18 μm ('00)	0.13 μm ('02)	0.90 μm ('04)
V_{DD} [V]	2.5 (1x)	1.8 (0.7x)	1.2 (0.5x)	1.0 (0.4x)
I_{DSAT} [μA/μm]	600 (1x)	600 (1x)	550 (1x)	850 (1.4x)
I_{OFF} [nA/μm]	0.1 (1x)	0.02 (2x)	0.32 (32x)	7 (700x)
I_{GATE} [nA/μm]	2.5e-5 (1x)	1.8e-3 (100x)	0.65 (5e4)	6.3 (7000x)
I_{ON}/I_{OFF} [10e6]	60 (1x)	30 (0.5x)	1.7 (0.03x)	0.12 (0.002x)
g_M [mS/μm]	0.3 (1x)	0.4 (1.3x)	0.6 (2x)	1.0 (3.3x)
g_{DS} [μS/μm]	7.7 (1x)	15 (2x)	42 (5.4x)	100 (13x)
g_M/g_{DS} [1]	39 (1x)	27 (0.7x)	14 (0.36x)	10 (0.26x)
f_T [GHz]	30 (1x)	60 (2x)	80 (2.7x)	140 (4.7x)
Delay [ps/gate]	45 (1x)	30 (0.7x)	15 (0.3x)	11 (0.24x)
C_G [fF/gate]	0.47 (1x)	0.35 (0.7x)	0.25 (0.5x)	0.16 (0.34x)
C_J [fF/gate]	0.83 (1x)	0.80 (1x)	0.88 (1.1x)	0.66(0.8x)

to the measurement results found in [55] the linearity of transistor devices deteriorates with the progress in technology scaling from $l = 350\,\text{nm}$ to $l = 180\,\text{nm}$ for a fixed w.
The physical reality of a diminished dynamic range in modern analogue circuits strongly contradicts the system architecture demands for state-of-the-art wireless transceivers, not to mention the tightened demands of future wideband, multi-standard applications.
Although the impact of technology scaling on the performance of integrated coils has not been elaborated, it has become clear that the changes in the metal stack and the lowered substrate resistance that go along with technology scaling corrupt the prerequisites for successful integrated high Q inductor design.
Besides it has been shown that there is a need to enhance the capacitance density of capacitor devices suitable for linear analogue RF design if the trend of process technology scaling continues. Although minimum allowable horizontal spacings between metal structures that can be manufactured shrink with technology scaling the risk of electrical breakdowns prevents an unhindered increase of the capacitance density of VPP-caps.
High speed digital circuitry will benefit from future CMOS process technologies in terms of higher transit frequencies f_t and smaller delays per gate but at the expense of higher power losses.

5. The Implemented Receiver Front-end

In this chapter we will evaluate the performance of the analogue receiver front-end implemented in a 65 nm standard CMOS technology. The receiver front-end is part of a complete GSM transceiver testchip implemented in a cooperation with a business partner from industrial background. Modern IC design depends on evaluation by simulation to a large degree thus the first part of the evaluation will be simulation based. Testchip runs are time-consuming expensive endeavours for sub-micron process technologies as the related costs for the generation of masks for lithography are high and die area is expensive. Additionally, the sets of design rules for the physical implementation get more and more complex for every technology generation. Thus the engineering efforts that have to be undertaken before a physical chip design is ready for tape-out and fabrication increase. After the testchip design is handed to the semiconductor device fabrication two to three months are likely to pass before the evaluation of a hardware demonstrator in a measurement laboratory can even begin. As the functionality integrated in modern ICs is very complex, the necessary measurement set-up e.g. protocols for the configuration of the chip also become very complex. In contrast to the enormous efforts listed before the time-to-market is getting ever shorter. Summing-up, the need for sophisticated pre-tape-out evaluation by simulation is self-evident in order to reduce the number of testchip iterations before a design reaches a product ready status [31]. Nevertheless, testchip runs are invaluable for performance evaluation. The complicated mechanisms that e.g. lead to cross-coupling between analogue and digital circuit blocks, the emergence of spur signals in single-chip implementations are often too complex to be software simulated before tape-out. In addition the employed modelling and the simulation set-ups need to be counter-checked with the physical reality in the measurement laboratory. Thus the chapter is concluded with measurement results for the implemented receiver front-end from an actual testchip run.

5.1. The Proposed Receiver Front-End Topology

The proposed front-end topology for the analogue front-end of the direct-conversion receiver is depicted in Fig. 5.1. One low band LNA (LBLNA) and one high band LNA (HBLNA) operate on the quadrature mixer with passive switches. The frequency conversion is succeeded by the active third order lowpass filter structure. LNA and mixer have a voltage mode interface. The mixer and the baseband filter (BBF) have a current mode interface. The advantages of a current mode interface between mixer and baseband filter have been discussed in Section 2.7.3.

5.2. Low Noise Amplifier

5.2.1. Testbench

The testbench (Fig. 5.2) for the LNA simulations models the RF signal path from the antenna to the mixer input stage. The antenna is modelled as a single-ended input port with a 50 Ω source impedance. The single-ended to differential (balanced) conversion in the signal path will

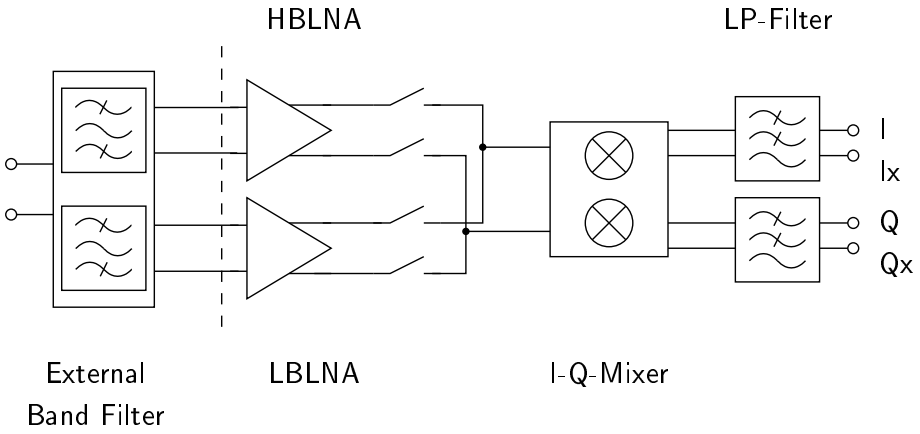


Figure 5.1.: Block diagram of the implemented analogue receiver front-end.

be realised by a surface acoustic wave (SAW) filter on the final PCB in the cell phone. The SAW filter provides appropriate band filtering. In the simulation testbench the single-ended to differential conversion is modelled by an ideal BalUn (balanced-unbalanced) as no S-Parameter data are available to model the SAW filter more accurately. The SAW filter does not only perform a single-ended to differential conversion but also converts the value of the impedance-level from 50 Ω to 150 Ω. The manufacturer of the SAW filter also specifies a required inductive termination L_{TERM} in parallel to the 150 Ω. The inductance value of the termination varies for the different GSM bands. The target values are listed in Table 5.1. Along with the impedance transformation goes a voltage gain G_V (not a power gain G_P). The voltage gain is also listed in Table 5.1. As the simulation software can only calculate S_{11} correctly for matching to a purely real source impedance, a capacitance C_{EQV} is inserted into the testbench that compensates the termination inductance at mid-band frequency. The value for C_{EQV} is calculated by the simple formula

$$C_{EQV} = \frac{1}{\omega^2 L_{TERM}}. \tag{5.1}$$

The necessary values for C_{EQV} are given in Table 5.1. This work-around gives exact results for S_{11} only at mid-band frequency. As the matching characteristics are relatively broadband in nature compared to the bandwidth of the GSM bands the inaccuracy in the S_{11} calculations are considered acceptable. In fact the input matching characteristics are even acceptable if we apply only one set of matching elements to both GSM low bands and both GSM high bands, respectively, instead applying individual matching elements to all four bands as we will see in Section 5.4.2.2. The proposed matching network consists of a passive serial element Z_S in every branch of the differential signal path and one shunt connected element Z_P between the RF signal lines. In general, the topology can be of a Z_S-Z_P or Z_P-Z_S type. The naming convention used here gives the matching element that is closest to the chip input first. The default matching topology that has been used for the simulations is the L_S-L_P type. The fall-back topology is of L_P-C_S type. The component values that have been calculated from the input impedance of the LNAs in the four GSM bands are listed in Table 5.2(a) and Table 5.2(b). The quality factor Q of the SMD matching elements, especially the Q of the inductors, that are used for the matching network is limited. For the simulations the Q of inductors $L \leq 10\,\text{nH}$ is assumed $Q = 30$, for larger inductors $10\,\text{nH} \leq \text{L} \leq 30\,\text{nH}$, $Q = 20$ is assumed. Modelling the matching inductors with a

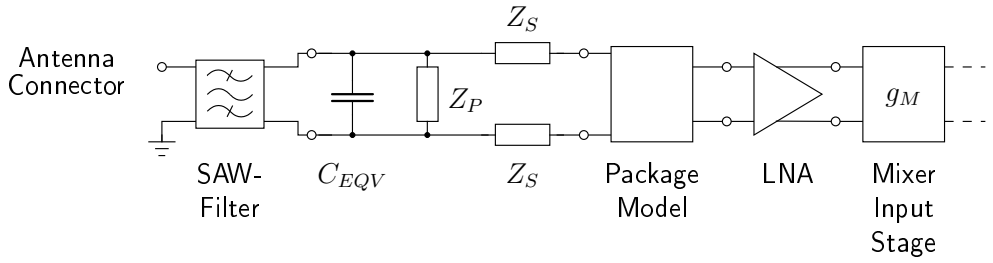


Figure 5.2.: Schematic of the LNA testbench topology.

Table 5.1.: Desired impedance for the termination of the SAW filter, required compensation capacitor C_{EQV} and voltage gain G_V associated with the impedance transformation (at mid-band frequency).

Band	G_{TERM}	L_{TERM}	G_V	C_{EQV}
	[S]	[nH]	[dB]	[fF]
GSM850	1/150	82	4.6	397
GSM900	1/150	82	4.6	348
DCS1800	1/150	15	3.6	497
PCS1900	1/150	18	4.0	366

limited Q is vital for the estimation of the noise performance of the LNA. Aside from the Q value of the SMD component itself the soldering contacts of the components to the PCB will degrade the quality factor of the matching network in the laboratory. That is why the conservative approximations of $Q \leq 30$ are used. The manufacturers of SMD inductors guarantee quality factors of $Q \approx 60$ for 0402 SMD components in the frequency range of interest for GSM applications. As SMD capacitors are available with an inherently higher Q value (e.g. $Q \gg 100$) capacitors (if used) are modelled with an infinite Q in simulations. A secondary effect of modelling the matching network with a limited Q is that the voltage gain from the input of the matching network to the output of the matching network will be lower than for the ideal case with an infinite Q.

Following the RF signal path on a PCB we have 3-4 mm of line length before the signal enters the BGA (ball grid array) package. The die itself is mounted into the package in flip-chip technology. This part of the RF signal path, beginning after the last solder pads for the matching elements and ending with the bumps that actually make the contact to the die, has been modelled in Ansoft's field simulator HFSS. The resulting S-Parameter data file has been incorporated into the testbench. The geometrical dimensions and material data for the 3-D field simulations have been adopted from a draft of the expected implementation of the system platform in the phone. For explicit time domain simulations a simplified package model in the form of a short Spice netlist has been available. As the spice netlist models the PCB-package interconnection less accurately than the S-Parameter data it is used only for time domain simulations.
The load impedance of the LNA in the receiver front-end is given by the mixer input stage. That is why the mixer input stage has been used to terminate the LNA in the testbench. As the low band LNA and the high band LNA operate on the same mixer in the implemented front-end both

LNAs are always present in the testbench. The output of the second LNA resembles a significant part of the total load impedance. Neglecting either the mixer input stage or the second LNA affects the simulation results to a large degree.
All simulations are performed at a junction temperature $T = 40\,°\mathrm{C}$ unless noted otherwise.

5.2.2. Proposed Topology

The proposed LNA circuit topology is depicted in Fig. 5.3. Generally speaking, the LNA consists of two cascaded common-source differential amplifier stages (DS1, DS2) with global feedback (C_{FB}). Two cascaded amplifying stages overcome the gain limitations of a simple common-source amplifier with capacitive feedback (cf. Section 2.6.1.1). Furthermore, the LNA topology exhibits moderate current consumption and does not use die area consuming integrated inductors.
The internal load impedances of both differential amplifier stages are purely resistive (R_{L1} and R_{L2}). The internal load impedance of the second differential stage is implemented as a voltage divider ($R_{L2} = R_{L21} + R_{L22}$). With the help of PMOS-switches either the full voltage swing (HG) or a fractional part of the total output voltage swing (LG = $\overline{\mathrm{HG}}$) is fed to the mixer. This voltage gain step helps to reduce the linearity requirements of the succeeding stages of the receiver. The LNA itself always works in the full gain mode for the sake of a constant input impedance.
In order to help the input power matching to a low source impedance $|Z_{SOURCE}| \approx 150\,\Omega$ the capacitances C_{FB} provide global feedback. As this method of setting the input impedance strongly depends on the voltage gain of the LNA it becomes clear why the LNA has to provide a constant gain at its output to the feedback branch. The switches that are used to select the output voltage swing also isolate the low band LNA from the high band LNA and vice versa as the front-end will work either in low band or in high band mode.
Local capacitive feedback (C_{GD}) at DS2 allows for trade-offs between gain, noise performance and input-impedance.
The intentionally inserted input capacitance (C_{GS}) also affects the gain and the noise-performance.
The *dc* bias voltage of the gate terminals of DS1 is set by an internal voltage divider. As it has been mentioned in the previous section the RF chip receive inputs are balanced and free from any external common mode voltage. The *dc* bias voltage of the gate terminals of DS2 is set by the *dc* potential of the drain terminal of DS1. The biasing current for every differential stage can be set individually by a current mirror. This feature provides the designer with an additional degree of freedom.
Both differential stages make use of R-trimming. The principle of operation of R-trimming has already been introduced in Section 2.8. The implementation of R-trimming has been omitted in Fig 5.3 in order to keep the schematic well arranged but it is illustrated in Fig. 2.20.
The RF inputs of the LNA have been ESD protected by a diode network between the signal lines and the supply lines. The ESD circuits have been provided 'as is' by the project partner from industrial background. As the ESD protection affects the LNA input impedance and noise performance including the ESD circuits is necessary for sophisticated LNA simulations.
The LNA topology is operated from a $V_{DD} = 1.4\,\mathrm{V}$ supply. This is more than the default supply voltage of $V_{DD} = 1.2\,\mathrm{V}$ for the thin gate oxide transistors of the 65 nm technology (cf. Section 4.2). Nevertheless, the life-time expectations for the LNA operating in a temperature range from $-30°\,\mathrm{C} < \mathrm{T} < 85°\,\mathrm{C}$ in a GSM system comply with the project partner's requirements for the life-time expectations of the whole GSM transceiver chip.

Two different design strategies have been pursued during the LNA design:

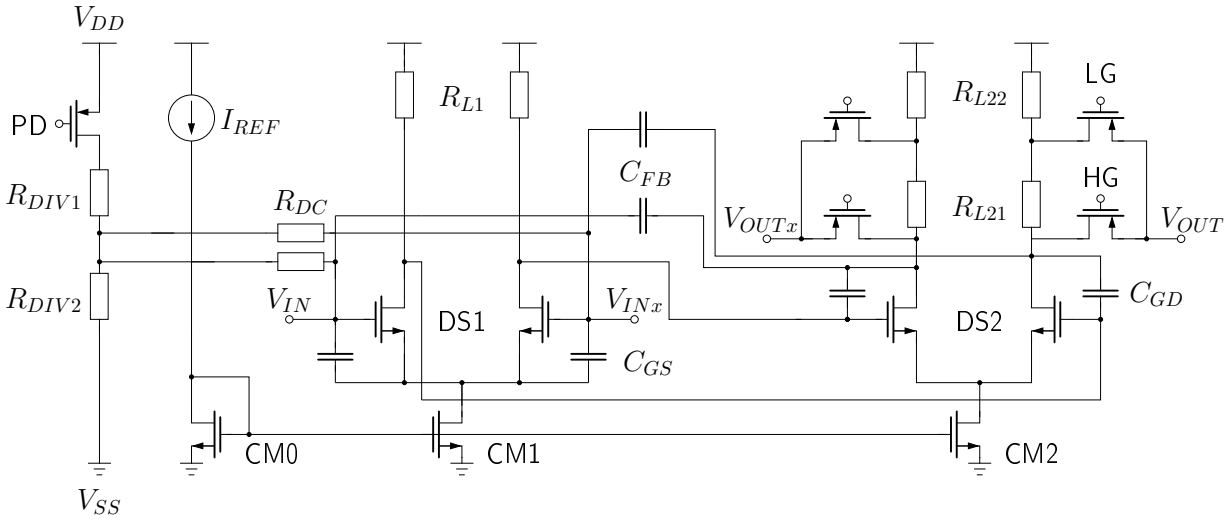


Figure 5.3.: Schematic of the implemented LNA topology. Additional R-trimming has been implemented but was omitted in this schematic drawing.

Minimum Die Area Strategy. The HBLNA uses minimum channel length transistor devices for the differential pairs in DS1 and DS2. The thick-gate devices of the current mirrors CM1 and CM2 use the minimum gate length for these devices in the HBLNA. The capacitances C_{GS} and C_{GD} have been omitted in the HBLNA in a trade-off for gain vs. achievable input return loss. In conclusion the HBLNA is optimized for minimum die area consumption. Besides the reduced dimensions of the transistor devices in DS1 and DS2 will introduce reduced parasitics to the RF performance of the HBLNA.

Advanced Analogue Performance Strategy. The gate lengths of the differential pair in DS2 of the LBLNA have been extended to $l = 115\,\text{nm}$ in order to achieve a better amplifying potential g_M/g_{DS} (cf. Fig. 4.13). The extended gate length $l = 380\,\text{nm}$ of the transistors of the current mirrors CM1 and CM2 of the LBLNA increases the output resistance of these current mirrors. In conclusion the LBLNA incorporates the knowledge gained from the model based design comparison in Section 4.2.1. The increased device dimensions are expected to help the analogue performance of the LBLNA in a trade-off for increased die area consumption.

5.2.3. The Design Process and Tooling

It has already been indicated that the simulations for the LNAs have been done in a two-step set-up. The performance of the LNA can only be evaluated properly when the LNA is matched to the input source. Thus in a first simulation it is necessary to determine the unmatched LNA input impedance. With the knowledge about the input impedance appropriate component values for the matching elements are calculated. Thereafter the actual performance simulation is started. The two-step set-up has been automated with the help of script-files.

These script-files are processed by MUNEDA's WiCkeD, a circuit optimiser that can be integrated with the Cadence design environment. WiCkeD provides a powerful analogue design environment (if used correctly). It is essential to provide WiCkeD with a set of thoroughly chosen constraints for the parameterised circuit topology at hand before the actual design process can begin. A typical constraint that has been used during the design of the LNA is e.g. the operation of transistors in the saturation region. In addition to imposing constraints on individual devices, groups of devices need to be merged to functional units that require sets of constraints. A simple current mirror e.g. demands a comparable drain-source voltages on the primary and the secondary side in order to mirror the current from primary to secondary side with the ratio of the gate width on the secondary side to the gate width on the primary side. Furthermore, all design parameters need to be limited by reasonable boundaries before the actual design and optimisation process starts. It is in the designer's responsibility to identify reasonable parameter ranges for every design parameter. These reasonable parameter ranges can be limited by the feasibility of a controlled physical implementation of a device, die area consumption, cost considerations, device modelling accuracy and many other aspects.
The intersection of the parameter ranges set by the defined device and structure constraints and the parameter ranges considered reasonable by the analogue designer span a multi-dimensional space of potential solutions. WiCkeD offers the tools to systematically navigate through this space and to find a performance optimum within this space. Aside from the possibility to alter design parameters manually, it is also possible to chose between an analytical and a stochastic circuit optimiser. The actual performance optimisation does start no sooner than all constraints are fulfilled. The analytical optimisation operates on performance gradients whereas the stochastic optimisation picks random points from the solution space and checks for performance improvements. That is why it is recommended to use the latter optimisation approach first and then to switch to the analytical approach when the performance metrics and design parameter values consolidate in a local optimum. Due to the nature of the problems and trade-offs in analogue circuits any given circuit optimiser will only find local optima if the solution space is not very limited in size. The analogue designer has to manually alter the design parameters occasionally in order to make sure he covers as much of the solution space as is possible in a set time-frame and to make sure he/she decides for the most appropriate optimum with its trade-offs.
Although the LNA circuit consists of relatively few elements the interactions of the device parameters are very complex. Altering the width of a transistor in DS1 e.g. directly affects the gain of the LNA, the noise performance, the input impedance and the linearity performance. Often the improvement of a performance requires trade-offs with other performances. WiCkeD proves a valuable tool for the graphical visualisation of these trade-offs. By processing the results of sensitivity analyses and performance gradients relating to parameter changes and handing them to the designer WiCkeD makes the designer aware of the manifold correlations between all of the performance metrics in focus.
The information WiCkeD processes is often gained from an increased number of simulation runs. These numerous simulation runs require computational resources. The distribution of batch jobs to multiple PCs in a computer cluster is a very effective feature of the WiCkeD software.

5.2.4. Layout

During the physical layout of the LNA extreme care has to be paid to implementing a symmetrical RF path. A symmetrical layout is a prerequisite for a good IP_2-performance which is crucial for

a direct conversion receiver (cf. Section 3.3.2). That is why the LNA layout (Fig. 5.4) has an axis of symmetry. Elements that require good local matching like the load resistors of the differential stages (R_{L1} and R_{L2}) and the differential stages (DS1 and DS2) themselves are placed as close to the axis of symmetry as possible.
The wide transistors of the differential stages are made up of shunt connected unit cells. Strictly speaking, the use of unit cells contradicts the classical layout approaches for enhanced matching properties commonly taught in lectures on IC design i.e. common centroid or interlaced gate fingers. Nevertheless, transistor unit cells offer several advantages. First of all the transistor model files of design packages for process technologies best fit the physical reality for a limited range of geometries due to varying parasitic effects. The more the transistor geometries deviate from the reference transistor on which modelling is based e.g. extremely wide transistors the less accurately the model file describes the behaviour of the device that is actually being implemented. Secondly, arrays of unit cells are relatively comfortable to connect. There is no use in putting enormous efforts into implementing e.g. the transistors of a differential stage in common centroid technique with interlaced gate fingers for the sake of perfect matching if the accumulated layout parasitics (i.e. ohmic resistance of paths and vias and capacitances between wirings) severely deteriorate the RF performance of the differential amplifier stage.
In general, metal routing over active RF devices should be reduced to a minimum.
Circuit sub-blocks that are not relevant for RF performance like static digital control blocks or current mirrors operating at *dc* are moved to the side of the LNA layout cell. The connections of these blocks to blocks operating at RF frequency are routed to the axis of symmetry before being symmetrically distributed to performance relevant RF blocks.
When it comes to placing the LNA layout in the floorplan of the complete chip it is considered wise to give the RF inputs of the LNA first priority. Routes should be short and straight. An empirical rule of thumb estimates that for $1\,\Omega$ of series resistance accumulated on the path from chip RF input to the gate terminals of DS1 degrades the noise figure of the LNA by $\Delta NF \approx 0.2\,\mathrm{dB}$. Low ohmic RF input traces of the LNA impose a design trade-off between the accumulated ohmic resistance and the parasitic capacitances resulting from wide metal paths on the designer.
The die area consumption for the LBLNA is $0.012\,\mathrm{mm}^2$ and $0.009\,\mathrm{mm}^2$ for the HBLNA excluding bumps and ESD protection, respectively.

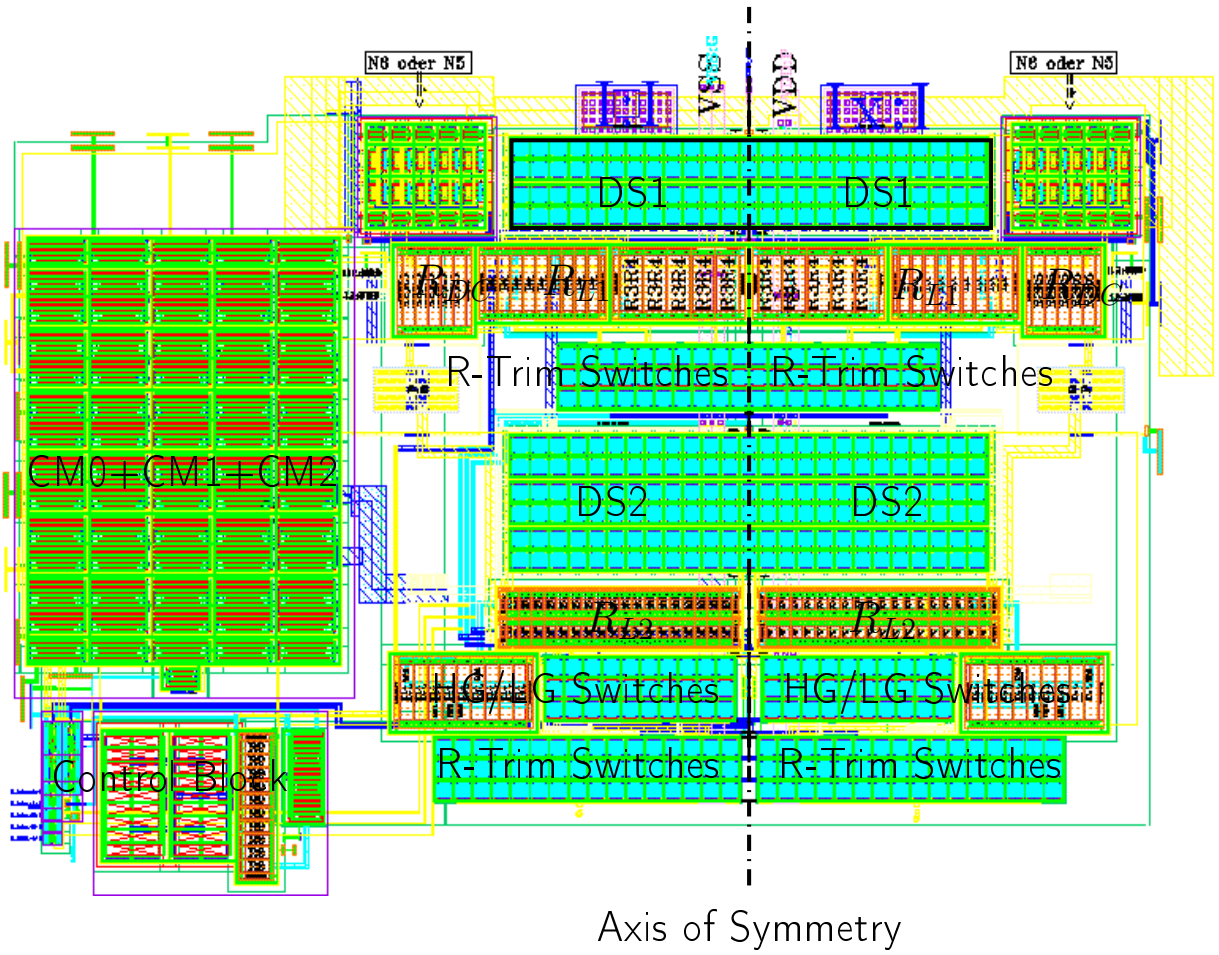


Figure 5.4.: Symmetrical LNA Layout.

Table 5.2.: Proposed matching elements for the LNAs for input power matching to the SAW-Filter.

(a) Low band LNA.

		Unit	GSM850		GSM900	
			schematic	extracted	schematic	extracted
Z_{IN} @	$\Re\{Z_{IN}\}$	[Ω]	69	65	69	61
mid-band	$\Im\{Z_{IN}\}$	[Ω]	−120	−130	−118	−125
$L_S - L_P$	L_S	[nH]	4.1	5.0	3.7	4.3
	L_P	[nH]	19.1	18.3	18.3	16.7
$L_P - C_S$	C_S	[pF]	3.8	3.1	3.6	3.0
	L_P	[nH]	18.1	18.4	17	16.7

(b) High band LNA.

		Unit	DCS1800		PCS1900	
			schematic	extracted	schematic	extracted
Z_{IN}@	$\Re\{Z_{IN}\}$	[Ω]	30.5	25.6	31.0	23.7
mid-band	$\Im\{Z_{IN}\}$	[Ω]	−111	−108	−110	−103
$L_S - L_P$	L_S	[nH]	2.2	2.2	2.1	2.0
	L_P	[nH]	4.6	4.2	4.6	4.1
$L_P - C_S$	C_S	[pF]	1.8	1.6	1.5	1.3
	L_P	[nH]	6.6	6.6	6.5	6.1

5.2.5. Simulation Results

The simulation procedure takes place in two steps. In the first step only the unmatched LNA input impedance is extracted from an S-parameter simulation. In the second step the values of the matching elements are calculated for the band of interest, entered into the testbench and the simulation for the extraction of the actual performance is run.
The simulations are performed for the nominal process corner, a junction temperature of $T = 40°\,\mathrm{C}$ and a nominal supply voltage of $V_{DD} = 1.4\,\mathrm{V}$ for the LNA unless noted otherwise.
The Tables 5.2(a) and 5.2(b) list the simulated input impedances and the matching element values that have been calculated for the GSM low and high bands. A comparison of matching element values that have been calculated for both low bands and both high bands, respectively, suggest an acceptable input return loss ($S_{11} < -10\,\mathrm{dB}$) will be possible even if a combi-matching network is chosen for both low bands and both high bands respectively.

5.2.5.1. Nominal Simulation Results

Table 5.3(a) summarises the nominal simulation results for the implemented low band LNA. Table 5.3(b) gives the nominal simulation results for the implemented high band LNA. The tables compare not only the performance based on pre-layout schematic level simulations results but also the post-layout simulation performance results with extracted parasitics. The plots in Fig. 5.5 to Fig. 5.8 illustrate the performance characteristics in detail for the implemented LNAs in more detail.

Table 5.3.: Summary of the nominal simulation results for the LNAs ($G_{V,AVG}$ excluding gain related to impedance conversion). V_{DD} is set to 1.4 V.

(a) Low band LNA.

Characteristic		GSM850		GSM900	
		schematic	extracted	schematic	extracted
$S_{11,MAX}$	[dB]	−31.6	−29.2	−29.8	−27.4
$G_{V,AVG}$	[dB]	22.7	21.4	22.1	20.8
ΔG_V	[dB]	0.09	0.05	0.11	0.07
NF_{MAX}	[dB]	1.6	1.7	1.6	1.7
$CP1i$	[dBm]	−22.9	−22.4	−22.6	−22.2
IIP_3	[dBm]	−12.7	x	−12.5	x
I_{DC}	[mA]	9.3	9.0	9.3	9.0

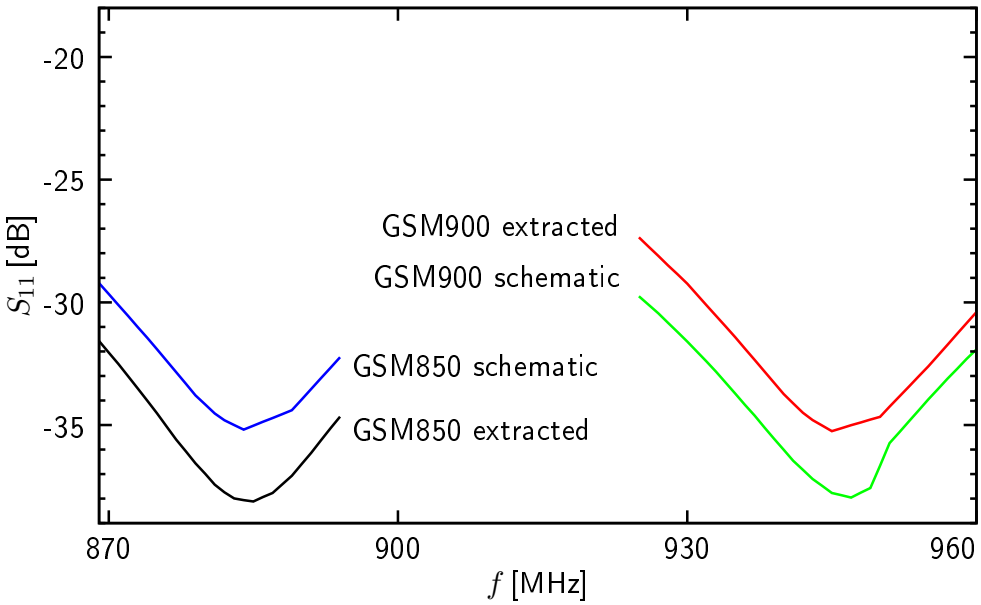
(b) High band LNA.

Characteristic		DCS1800		PCS1900	
		schematic	extracted	schematic	extracted
$S_{11,MAX}$	[dB]	−20.2	−19.0	−21.9	−20.0
$G_{V,AVG}$	[dB]	20.4	19.0	19.7	18.4
ΔG_V	[dB]	0.15	0.19	0.07	0.12
NF_{MAX}	[dB]	2.2	2.3	2.1	2.3
$CP1i$	[dBm]	−23.2	−22.7	−23.2	−22.8
IIP_3	[dBm]	−13.7	x	−14.1	x
I_{DC}	[mA]	9.9	9.7	9.9	9.7

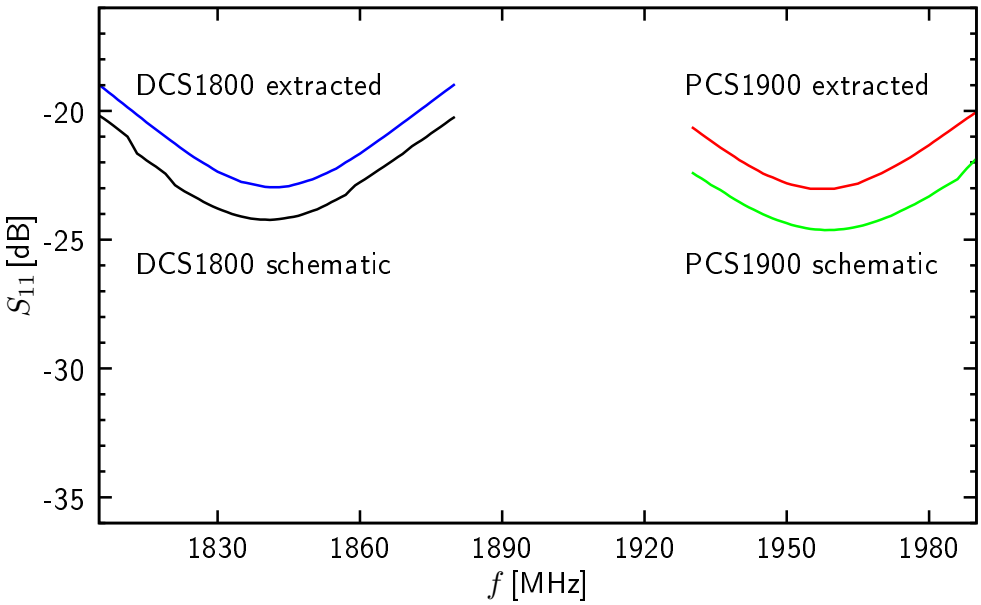
The simulation results labelled 'extracted' include the device parasitics and interconnection wiring parasitics. It is obvious that these simulation results are inferior to the purely schematic based simulation results (labelled 'schematic') throughout all performance characteristics.
As the number of components and the number of nets in the netlist severely increase when the parasitics are extracted, extracted simulations need large computational resources.
Large computational resources are needed especially for the large-signal analysis e.g. extraction of the 1 dB compression point $CP1$ and the third order intercept point IP_3. The in-band $CP1$ requires a single-tone large signal analysis. Here a time-domain periodic-steady-state (PSS) solver has been applied as its convergence properties are known to be robust for circuits that are driven into strong non-linearity. However, the two-tone analysis that is required for the extraction of the IP_3 can be performed much more effectively by a harmonic balance (HB) solver. In short, the PSS solver tries to find a periodic operating point in the time domain for the largest large-signal period (fundamental tone) using a Newton-algorithm whereas HB solver solves the circuit equations in the frequency domain. Finding the steady-state in a simulation with two large-signal tones ($f_1 < f_2$), closely spaced in frequency ($f_1 - f_2 = \Delta f \ll f_1$), in the time domain involves simulating one period $T = 1/(\Delta f)$ with a time step size $\Delta T < 1/f_2$. The HB solver merely solves the circuit equations for a limited set of discrete frequencies (f_1, f_2 and the intermodulation products $2f_1 - f_2$, $2f_2 - f_1$).

5.2.5.2. Input Return Loss

From Fig. 5.5(a) and Fig. 5.5(b) it can be seen that for all four GSM bands a sufficient input return loss $S_{11} \leq -19\,\mathrm{dB}$ has been achieved.



(a) GSM low band LNA.



(b) GSM high band LNA.

Figure 5.5.: Simulation results for the input return loss S_{11} of the implemented LNAs with L_S-L_P type matching network.

Table 5.4.: Details of the voltage gain distribution in the LNA stages for the GSM900 and the PCS1900 band at mid-band frequency (schematic simulations).

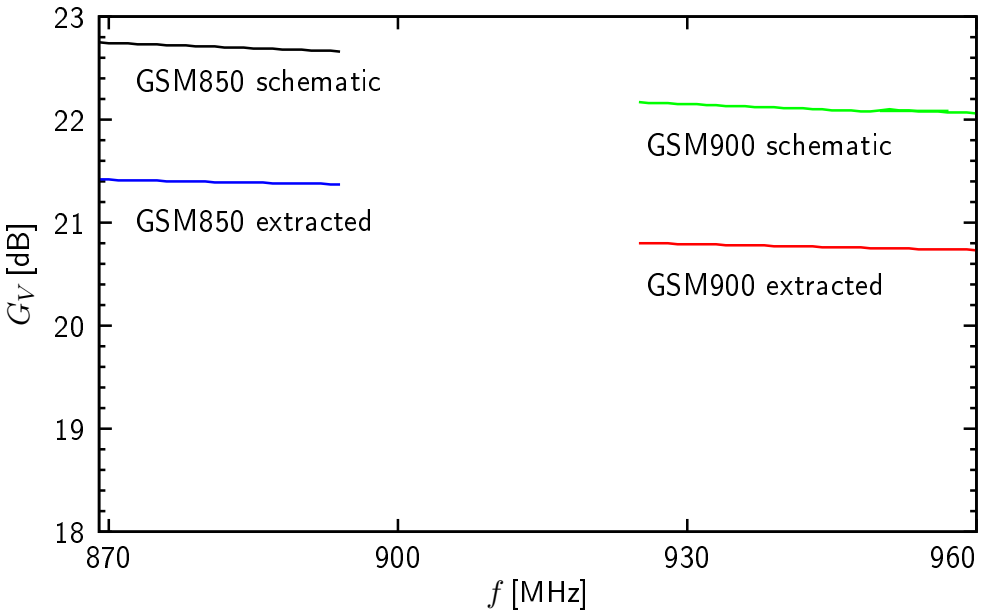
Stage	Contribution to G_V	
	GSM900	PCS1900
	[dB]	[dB]
Matching Network	2.8	5.0
DS1	8.7	7.4
DS2	10.5	7.3
Total G_V	22.0	19.7

5.2.5.3. Voltage Gain

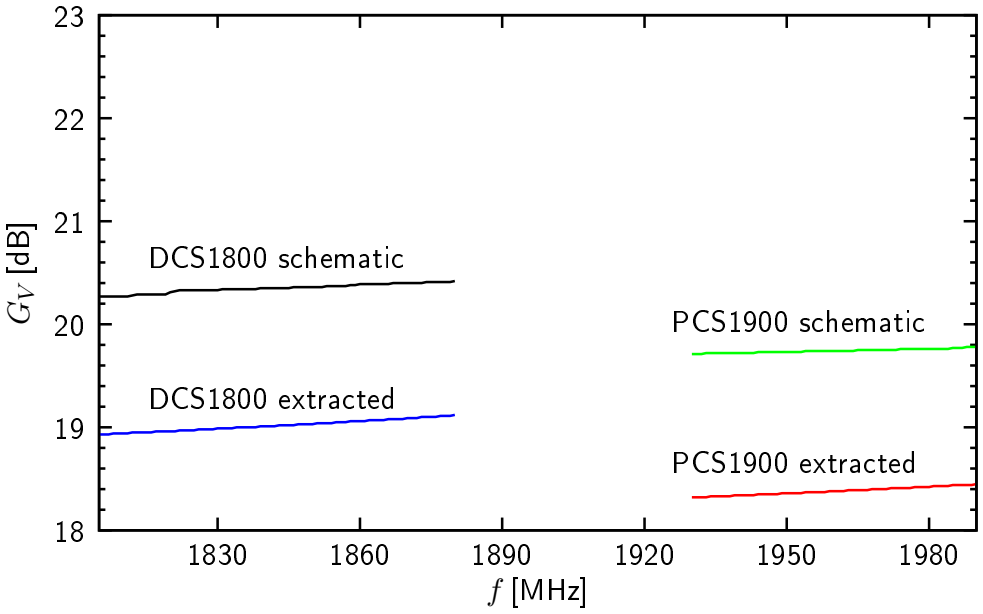
The voltage gain G_V vs. frequency f of the LNAs is depicted in Fig. 5.6(a) and Fig. 5.6(b) for all four GSM bands. The plots do not include the gain related to the impedance conversion of the SAW filter in the testbench in order to enable a fair and convenient comparison to LNA implementations of other authors (potentially matched to other impedance levels). The omitted gain is listed in Table 5.1 and can easily be added by the reader.
The low band LNA achieves about 2 dB more gain than the high band LNA. At the high band frequencies parasitic capacitances affect G_V stronger than at the low band frequencies. Thus a lower voltage gain in the GSM high bands is in accordance with the expectations. The variation of the voltage gain within a single band is less than $\Delta G_V = 0.2\,\text{dB}$ and thus almost constant. The drop of the voltage gain when comparing schematic level simulation results with simulation results including extracted parasitics is moderate for all four GSM bands. This indicates the effectiveness of the performance optimised physical designs of the LNAs.
The details about the generation of G_V in the LNAs in the GSM900 band and the PCS1900 band at mid-band frequency are investigated in Table 5.4. The three stages that contribute to the total G_V are the matching network and the first and the second differential amplifier stage (DS1, resp. DS2) of the LNAs, respectively. We see that the resonance of the matching network generates $\Delta G_V \approx 2.2\,\text{dB}$ more gain for the HBLNA than for the LBLNA. This means that gain of the HBLNA is more sensitive to the matching network. Low-Q matching elements will severely degrade the performance of the HBLNA. Another interesting difference between both LNAs is the increased gain in DS2 of the LBLNA. The increase in gain has been achieved by setting the length of the NFET devices in DS2 to $l = 115\,\text{nm}$ instead of $l = 60\,\text{nm}$ (cf. g_M/g_{DS} investigation in Section 4.2.1.2).
The requirement nominal $G_V > 18\,\text{dB}$ (excluding the voltage gain of an impedance conversion in a BalUn or SAW filter) specified in Section 3.4.2 has been met for all GSM bands.

5.2.5.4. Noise Performance

The noise figure NF vs. frequency f is illustrated in Fig. 5.7(a) and Fig. 5.7(b). The noise performance in the low bands is good whereas in the high bands it is moderate. Nevertheless, the minimum requirement $NF < 3.3\,\text{dB}$ specified in Section 3.4.2 has been met. The inferior noise performance in the GSM high bands fits to the expectations suggested by the theory of



(a) GSM low band LNA.

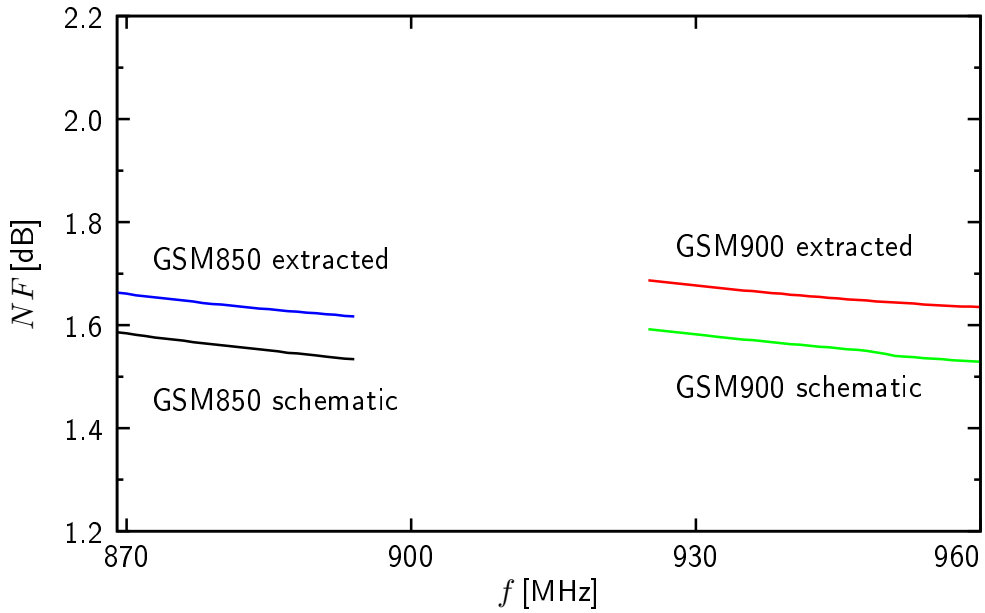


(b) GSM high band LNA.

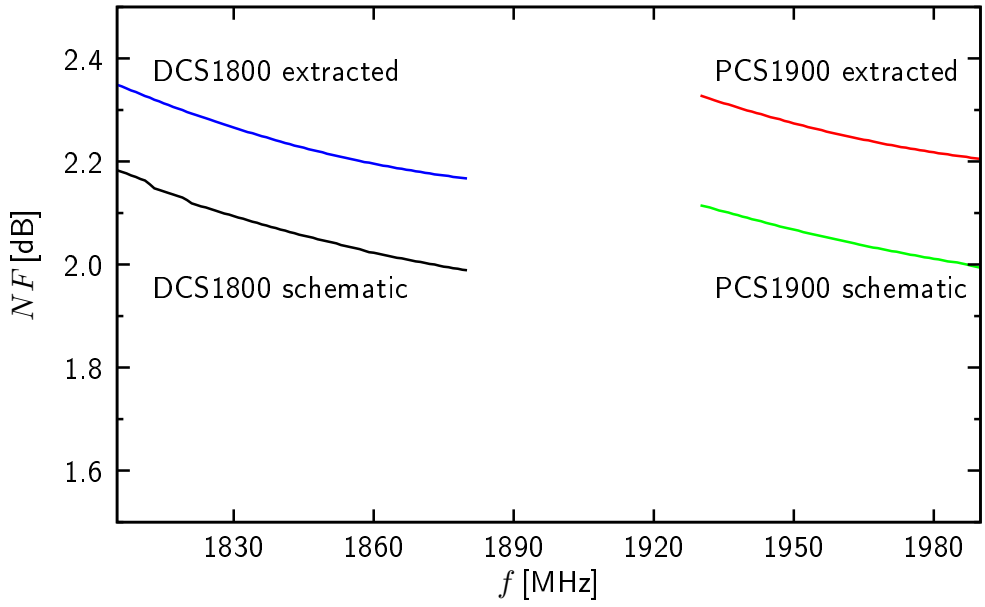
Figure 5.6.: Simulation results for the voltage gain G_V of the implemented LNAs (excluding gain related to impedance conversion).

noisy circuits with respect to the relatively low gain that has been achieved for the GSM high bands. Another point worth noting is that the minimum NF is not located at mid-band frequency whereas the minimum of S_{11} is centred at mid-band frequency. This strongly indicates that the matching network chosen according to input power matching constraints does not meet noise matching requirements. For the implemented LNA topology noise matching and power matching are not identical.

The noise contributions of the individual circuit elements in the LNA circuits is investigated



(a) GSM low band LNA.



(b) GSM high band LNA.

Figure 5.7.: Simulation results for the noise figure NF of the implemented LNAs.

in detail in Table 5.5(a) and Table 5.5(b). The noise contributions of transistors in the LNAs originate mainly from the thermal channel noise (id) and only a small share originates from flicker noise (fn). Ohmic resistors exclusively contribute thermal noise (rn). We see that for the low band LNA the thermal noise of the source impedance contributes almost 70 % of the total noise power whereas in the high band LNA the thermal noise of the source impedance contributes only 62 % of the total noise power. This indicates a better noise performance of the low band LNA. It is worth noting that the input matching network (L_S, L_P) and the package modell (Package) contribute more than 12 % to the total noise power in the high band LNA and only less than 4 % to the total noise power for the low band LNA. It is concluded that in order to achieve a good noise performance it is vital for the chosen LNA topology to have an adequate input impedance. The input impedance dictates the values of the necessary matching elements. A small shunt inductor ($L_{P,HB} < 1/3L_{P,LB}$) severely increases the noise contribution of the matching network. The input impedance of the high band LNA could not be changed to a more adequate value without sacrifycing voltage gain. As the voltage gain of the high band LNA is already relatively low, a trade-off between noise performance and voltage gain has been chosen. The high band LNA is inherently more difficult to match as a given input capacitance dominates the input impedance more than for the low band LNA because of the higher frequency of operation ($f_{RF,HB} \approx 2f_{RF,LB}$).
In general the rest of the contributions of the different circuit elements to the total output noise adhere to the expectations. The transistors of the differential pair of the first LNA stage (DS1) contribute dominantly to the total noise. Other relevant noise contributions come from the load resistors (R_{L1}) of DS1 and the transistors of the differential pair of the second LNA stage (DS2).

5.2.5.5. Linearity

The achieved linearity performances for $CP1$ and IP_3 are summarised in Table 5.3(a) and Table 5.3(b). In Fig. 5.8 a sweep of the input power in the GSM900 band at $f = 942.5\,\text{MHz}$ is plotted. The sweep drives the circuit into saturation. The GSM specification [39] defines linearity testcases like the third order intermodulation testcase. The frequencies of the interferer signals ($\Delta f = 800\,\text{kHz}$) are in-band signals for the receiver circuit blocks prior to channel filtering like LNA and mixer. These interferer signals are located in the stop-band of the base-band filter. Thus the LNA and the mixer dominate the odd order linearity performance in these testcases. Both the simulation results for the $CP1i$ and the IIP_3 leave more than a margin of 4 dB to the performance specified in Section 3.4.2 for the odd order distortion performance of the GSM receiver front-end.

5.2.5.6. Process Variations and Statistics

Table 5.6(a) and Table 5.6(b) list the simulation results for the implemented LNAs for extreme process technology corners and extreme temperatures. The simulation results are based on netlists that include parasitic devices extracted from the layout of the LNAs. It turns out that a variation of the voltage gain $\Delta G_V \approx 2.5\,\text{dB}$ has to be expected for extreme performance corners of the LNAs.
The reference current for the current mirrors of the LNAs has been constant for all simulations in Table 5.6(a) and Table 5.6(b). When the LNAs are embedded into the receiver front-end these

Table 5.5.: Investigation of the (schematic based) spot noise contributions in the LNAs at $f_{RF} = 942.5\,\text{MHz}$ for the low band LNA and at $f_{RF} = 1960\,\text{MHz}$ for the high band LNA, respectively. The total input referred noise power density is $0.93\,\text{nV}/\sqrt{\text{Hz}}$ for the low band LNA and $0.98\,\text{nV}/\sqrt{\text{Hz}}$ for the high band LNA, respectively.

(a) Low band LNA.

Component	Noise Type	Contribution to total noise power	Accumulated NF
		[%]	[dB]
Source Impedance	rn	69.83	0.00
L_P	rn	1.06	0.07
L_S	rn	1.60	0.16
Package	rn	1.23	0.24
dc biasing DS1	rn	0.58	0.27
C_{GS}	rn	0.02	0.27
DS1 NFETs	id,(fn)	19.50	1.28
R_{L1}	rn	1.75	1.36
R_{TRIM} DS1	rn	0.36	1.38
DS2 NFETs	id,(fn)	3.00	1.51
R_{L2}	rn	0.21	1.52
HG switches	id	0.56	1.55
R_{TRIM} DS2	rn	0.04	1.55
Δ	all	0.26	0.01

(b) High band LNA.

Component	Noise Type	Contribution to total noise power	Accumulated NF
		[%]	[dB]
Source Impedance	rn	62.42	0.00
L_P	rn	5.92	0.39
L_S	rn	3.70	0.62
Package	rn	2.81	0.79
dc biasing DS1	rn	0.85	0.84
C_{FB}	rn	0.02	0.84
DS1 NFETs	id,(fn)	18.92	1.81
R_{L1}	rn	1.50	1.88
R_{TRIM} DS1	rn	0.40	1.89
DS2 NFETs	id,(fn)	2.68	2.01
R_{L2}	rn	0.24	2.02
HG switches	id	0.60	2.05
R_{TRIM} DS2	rn	0.04	2.05
Δ	all	−0.10	0.07

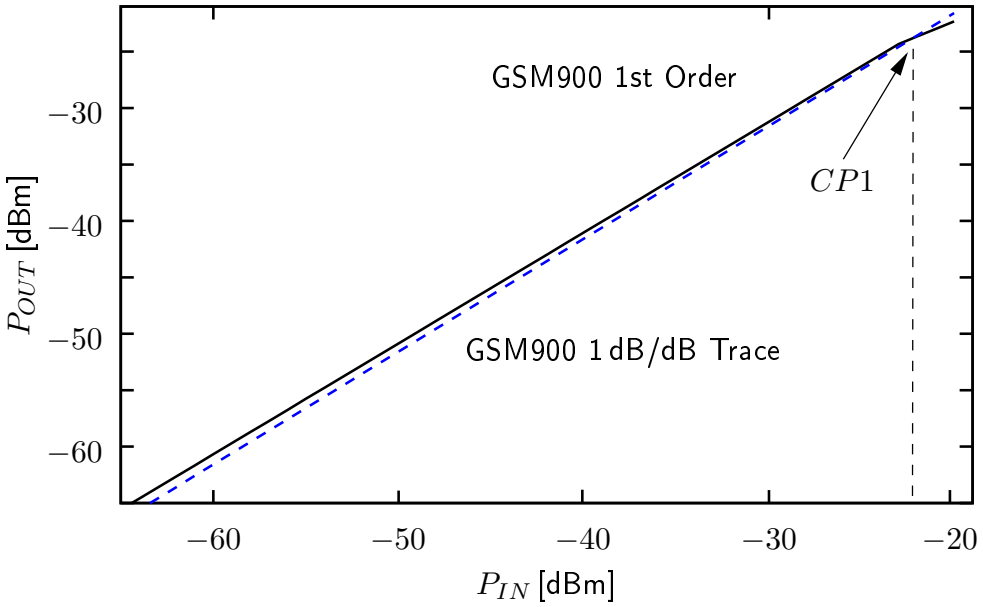


Figure 5.8.: Simulation results for the 1 dB compression point $CP1$ of the implemented low band LNA in the GSM900 band ($f = 942.5\,\text{MHz}$).

reference currents are derived by applying a bandgap voltage to a reference resistor. In order to reduce the variation of the reference current due to a variation of the sheet resistance $R_\square$, R-trimming (cf. Section 2.8) is used for the reference resistor in the implemented front-end. R-trimming is also used for the load resistors of the differential stages of the LNAs in order to reduce the gain variation of the LNAs. The effect of R-trimming on the voltage gain of the LNA is difficult to simulate as there is no process technology corner available for simulation that varies the sheet resistance only. An additional variation of e.g. the transistor technology parameters with the different available process corners masks the effects of the applied R-trimming.

The simulation results for the statistical analyses of the performance of the implemented LNAs are listed in Table 5.7(a) and Table 5.7(b). The Monte Carlo analysis considers both process technology variations and mismatch effects. The $n = 100$ simulations have been performed for a junction temperature of $T = 40°\,\text{C}$ and a supply voltage of $V_{DD} = 1.4\,\text{V}$. The matching elements and other elements of the testbench are not subjected to statistical variations, only the LNA core block with the LBLNA and the HBLNA cell.

5.2.5.7. Reference Performance in the 130 nm Technology

In Table 5.8 we find a summary of the performance of the LNAs in the reference GSM receiver front-end that has been implemented in the 130 nm technology. As the general structure of the LNAs is not changed in the 65 nm designs, the performances of the circuits have to face a direct comparison. We see that the performance of the reference LNAs is in deed comparable to the performance achieved in this work. But it turns out that the performance of the 130 nm design is superior to the 65 nm implementation even when bearing in mind that the 130 nm implementation is a product-ready design that has undergone manifold design iterations. Although we know from the comparison of the 130 nm and the 65 nm technology in Section 4.2.1.3 that the

Table 5.6.: Performance evaluation for the LNAs (with extracted parasitic devices) for extreme process corners and temperatures. The supply voltage is set to $V_{DD} = 1.3\,\mathrm{V}$. G_V does not include voltage gain related to impedance transformation prior to the LNA input.

(a) GSM Low band example: GSM900.

Parameter or Performance	Unit						Max. Deviation
T	[°C]	40	−30	110	40	40	
corner		nom	nom	nom	slow	fast	
$G_{V,AVG}$	[dB]	20.5	20.9	19.6	18.9	21.3	2.4
ΔG_V	[dB]	0.1	0.1	0.1	0.1	0.0	0.1
NF_{MAX}	[dB]	1.7	1.4	2.1	1.8	1.7	0.7
$S_{11,MAX}$	[dB]	−27.7	−25.0	−25.5	−24.5	−25.5	3.2
I_{DC}	[mA]	8.7	8.4	9.0	7.8	9.2	0.8

(b) GSM High band example: PCS1900.

Parameter or Performance	Unit						Max. Deviation
T	[°C]	40	−30	110	40	40	
corner		nom	nom	nom	slow	fast	
$G_{V,AVG}$	[dB]	18.0	18.5	17.0	16.2	18.9	2.6
ΔG_V	[dB]	0.1	0.1	0.2	0.1	0.2	0.2
NF_{MAX}	[dB]	2.4	2.0	2.9	2.5	2.4	0.5
$S_{11,MAX}$	[dB]	−19.9	−18.7	−21.5	−19.4	−21.2	2.8
I_{DC}	[mA]	9.3	8.9	9.7	8.3	9.9	1.6

linearity performance of the NFET devices in 65 nm improves, we find that the overall linearity of the LNA circuits is degraded. This is credited to the higher gain and lower supply voltage of the 65 nm LNAs. The most significant performance drawback of the 65 nm design is its noise performance especially in the GSM high bands.

Table 5.7.: Simulation results for the statistical analyses of the implemented LNAs for $n = 100$ simulation runs at $T = 40°$ C in the GSM900 band and the PCS1900 band repectively.

(a) GSM900.

Performance	Unit	GSM900			
		schematic based		incl. extracted parasitics	
		Expected Value μ	Standard Deviation σ	Expected Value μ	Standard Deviation σ
$S_{11,MAX}$	[dB]	-27.1	2.1	-26.4	1.8
$G_{V,AVG}$	[dB]	22.0	0.2	20.7	0.2
NF_{MAX}	[dB]	1.59	0.04	1.69	0.03
I_{DC}	[mA]	9.3	0.2	9.0	0.1

(b) PCS1900.

Performance	Unit	PCS1900			
		schematic based		incl. extracted parasitics	
		Expected Value μ	Standard Deviation σ	Expected Value μ	Standard Deviation σ
$S_{11,MAX}$	[dB]	-21.2	1.2	-20.0	0.8
$G_{V,AVG}$	[dB]	19.7	0.2	18.3	0.2
NF_{MAX}	[dB]	2.12	0.03	2.33	0.03
I_{DC}	[mA]	9.9	0.2	9.7	0.2

Table 5.8.: Reference data of the nominal performance according to simulation results (including extracted parasitics) for the LNA implemented in the 130 nm technology. The typical voltage gain $G_{V,TYP}$ includes gain corresponding to the impedance transformation in an SAW-Filter after the antenna.

Band	$G_{V,TYP}$	NF_{TYP}	$CP1i$	IIP_3	$I_{DC,TYP}$	$\Re\{Z_{IN,TYP}\}$	$\Im\{Z_{IN,TYP}\}$
	[dB]	[dB]	[dBm]	[dBm]	[mA]	[Ω]	[Ω]
GSM850	24.4	1.3	-20.4	-9.9	8.7	104	-156
GSM900	23.8	1.3	-20.2	-8.8	8.7	99	-149
DCS1800	24.2	1.5	-21.2	-11.5	11.0	72	-136
PCS1900	23.6	1.6	-20.9	-11.3	11.1	66	-130

5.3. Mixer and Baseband Filter

The implemented LNAs that has been introduced in the previous section is embedded into a direct conversion receiver front-end for GSM. The quadrature down-conversion mixer and the baseband filter in the analogue front-end have been provided 'as is' by the project partner. Nevertheless, all front-end circuit blocks i.e. LNA, mixer (Fig: 5.9) and the BBF (Fig. 5.10) have been designed in close interaction. As has been mentioned earlier the design of the LNA cannot be separated from the design of the mixer cell. The mixer cell is the load for the LNA cell and the mixer input influences the achievable gain and noise performance of the LNA. Even the LNA input impedance is influenced by the mixer input stage due to the finite reverse isolation of the LNA. The baseband filter in turn is the load stage of the mixer. Aside from the interactions between the front-end circuits due to the load stage - input impedances relations, succeeding stages share the common mode level at the output and input of the circuit blocks, respectively. For voltage mode interfaces these common mode levels can be decoupled by *ac*-coupling capacitors. For current mode interfaces the common mode levels can not be decoupled that easy. Because of the area consumption of appropriate *ac*-coupling capacitors (even at RF frequencies e.g. $C \geq 3\,\mathrm{pF}$) *ac*-coupling is not always desirable. Moreover, the parasitic capacitances from the signal line to ground that are associated with *ac*-coupling capacitors deteriorate the RF performance of the circuits. Typical size of parasitic capacitances to ground ranges from 3 % to 5 % for the VPP-caps of the employed 65 nm process technology.

5.3.1. Proposed Topology

The mixer cell (Fig. 5.9) that is used in the implemented direct-conversion receiver front-end is a double balanced quadrature mixer with passive switches (cf. Section 2.7.3). The mixer input stage has a voltage mode interface to the LNA outputs. Coupling capacitors enable setting an independent *dc*-biasing of the mixer input stage. The interface type between mixer output and baseband filter input is current mode. It is for this reason that the performance evaluation is done for the unit of mixer cell and baseband filter by default. The output of the baseband filter is of the voltage mode type. For completeness reasons it is pointed out that the current mode interface between mixer cell and baseband filter requires the implementation of a common mode regulation as the *dc* levels of the circuit blocks cannot be decoupled. The details of the common mode regulation are not covered in this work.
The input stage of the mixer cell is a balanced transconductance stage. Besides the two differential stages of the LNA it is the third amplifying stage in the receiver front-end. The path of the generated RF current splits after the differential input pair into the path to the current commutating stage of the inphase and the quadrature branch. Both current commutating branches, inphase and quadrature, are electrically separated from each other by cascode transistors. Whereas the *dc* path continues with the PMOS current mirrors, the dynamic signal passes through the passive (*dc* current-free) switches to the baseband. A capacitor connected between the output lines shortens RF signals at the IF output.

The filter succeeding the quadrature mixer (Fig. 5.10) operates at baseband frequency and converts the output current of the mixer into a voltage. Furthermore the filter takes care of the channel filtering and anti-aliasing filtering before the ADC. The filter consists of two stages. The first stage (BBF1) is a simple balanced active transimpedance lowpass filter with a corner frequency of $f_C = 700\,\mathrm{kHz}$. As the input stage (PFET differential pair) of the operational am-

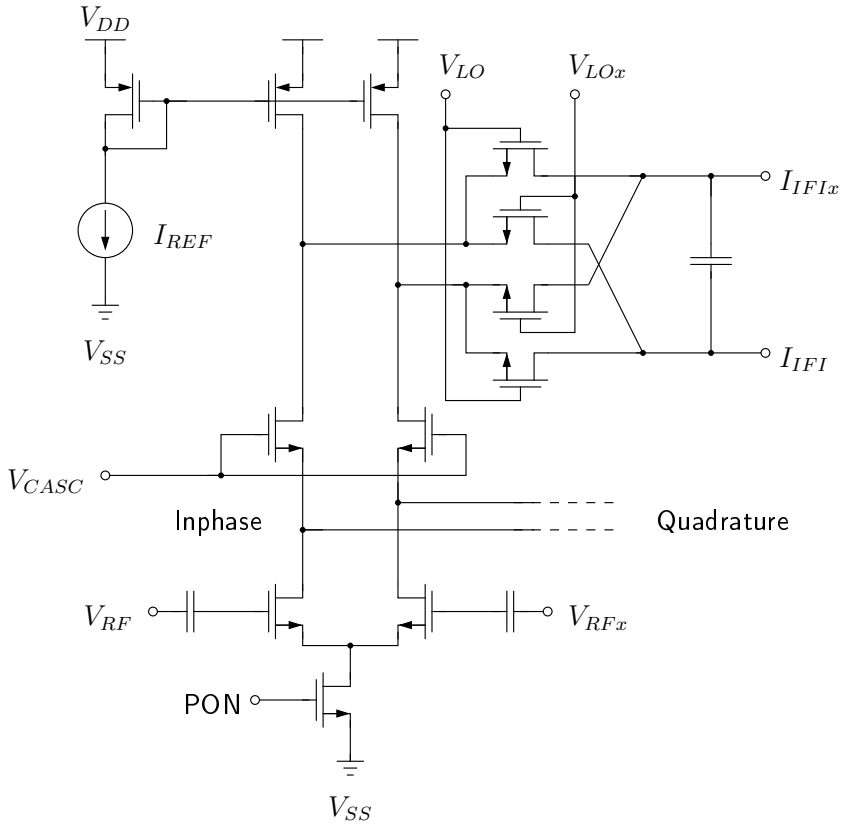


Figure 5.9.: Schematic of the implemented quadrature mixer cell. The applied common mode regulation is not shown.

plifier (opamp) in BBF1 has a dominant influence on the flicker noise noise performance of the complete analogue receiver front-end, the two-stage opamp has been designed with special care e.g. the lengths of the PFET input transistor devices has been elongated until their flicker noise contribution has no longer dominated the overall flicker noise of the front-end.
The second stage of the filter (BBF2) is a balanced multiple feedback active filter structure with a corner frequency $f_C = 163\,\text{kHz}$. The multiple feedback structure implements two frequency poles with a single opamp. Another advantage of the multiple feedback implementation of the second stage, is that the gain of the filter stage can be set separately from the corner frequency of the filter. The two-stage opamp used in BBF2 is a standard miller-compensated opamp design.
The transfer functions of both filter stages (BBF1 and BBF2) are given by:

$$T_{BBF1} = \frac{R_1}{1 + sR_1C_1} \tag{5.2}$$

$$H_{BBF2} = -\frac{R_3}{R_2}\frac{1}{1 + C_2(R_3 + R_4 + \frac{R_3R_4}{R_2})s + 2C_2C_3R_3R_4s^2} \tag{5.3}$$

$$\omega_0 = \frac{1}{\sqrt{2C_2C_3R_3R_4}} \tag{5.4}$$

$$Q = \frac{R_2\sqrt{2C_2C_3R_3R_4}}{C_2(R_2R_3 + R_2R_4 + R_3R_4)}. \tag{5.5}$$

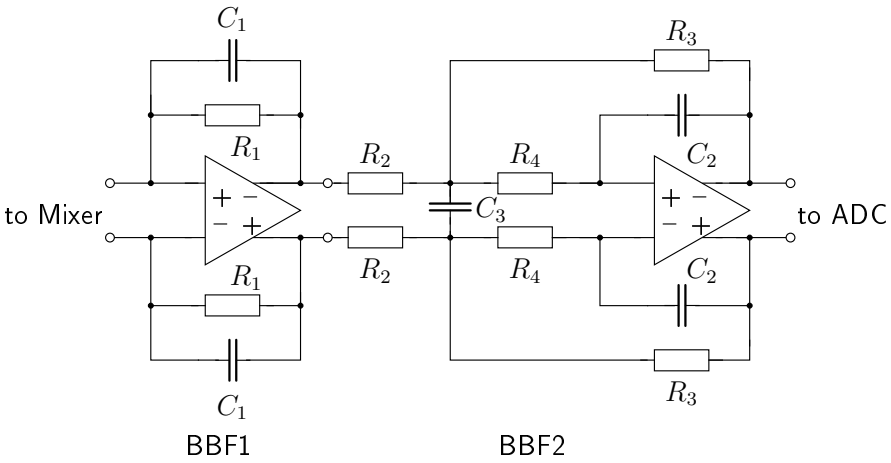


Figure 5.10.: Schematic of the implemented baseband lowpass filter.

Unlike the RF performances of the LNA or the mixer, the transfer characteristics of the baseband filter are described fairly accurately by the ideal mathematical expressions in (5.2) and (5.3). In Fig. 5.11 the transfer characteristics are illustrated.
The total voltage gain of the mixer cell and BBF1 is $G_V = 26.2\,\mathrm{dB}$ in high gain mode. BBF2 adds another voltage gain of $G_V = 10.3\,\mathrm{dB}$ to the analogue receive chain in high gain mode. The resistor values in the baseband filter can be switched in order to implement two gain steps in BBF1 and three gain steps in BBF2. That way the total gain of the baseband filter can be adjusted by $\Delta G_V = 24\,\mathrm{dB}$. The inband 1 dB compression point has been simulated to be $CP1i = -12\,\mathrm{dB}$ (clipping) while the nominal third order intercept point is $IIP_3 = 17\,\mathrm{dBm}$.

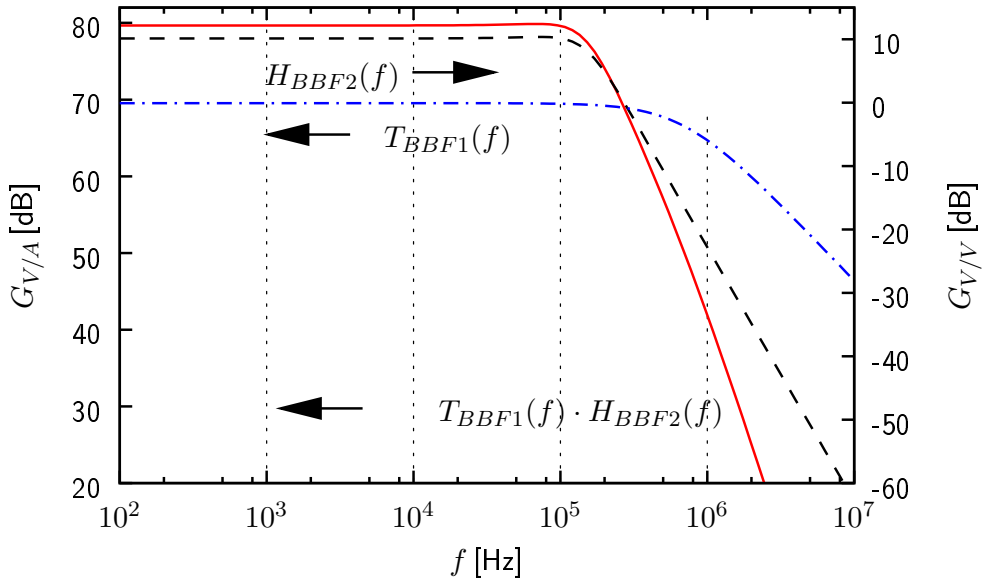


Figure 5.11.: Transfer functions of the baseband filter.

5.4. Performance of the Analogue Receiver Front-End

5.4.1. Simulation Results

This section elaborates on the performance of the analogue receiver front-end. The circuit blocks that have been evaluated separately in the previous sections are now merged together to a direct-conversion receiver front-end.
As the simulation set-up for the complete analogue front-end is very complex the set-up has been reduced to the essential components. This means that e.g. most biasing circuits have been excluded from the testbench in order to reduce the time and amount of computational resources necessary for the evaluation. Furthermore, the performances for all four GSM bands are not evaluated separately, but GSM850 and GSM900 are summed up in a general low band simulations (869 MHz$< f <$960 MHz) respectively DCS1800 and PCS1900 are summed up in general high band simulations (1805 MHz$< f <$1990 MHz). This simplification is appropriate as the performance of the LNAs has shown little discrepancy in both low bands respectively both high bands. It has already been pointed out in Section 5.2.5 that an acceptable input power match for both low bands respectively both high bands can be reached with combi-matching networks. Remember that the band selection filter characteristic of an SAW-filter in the final telephone implementation is not modelled in the testbenches. In addition the mixer is a broadband circuit that operates on all four GSM bands without a significant band selection characteristic, there is especially no selectivity between both low bands respectively both high bands.

5.4.1.1. Input Return Loss

The simulated input return loss S_{11} that has been achieved during front-end simulations is illustrated in Fig. 5.12. The simulations indicate an $S_{11} < -16$ dB which is considered an acceptable power match.

5.4.1.2. Voltage Gain

The simulation results for the voltage gain of the receiver front-end are plotted in Fig. 5.13(a) and Fig. 5.13(b). The gain is extracted after the first and after the second stage of the BBF. It can be seen that the gain of the receiver front-end is about 60 dB in the pass band of the BBF. The gain in the low band mode is about 2 to 3 dB higher than the gain in the high band mode. This difference in gain between low and high band operation matches to the differences in gain that have been simulated between low and high band LNA. Outside the BBF pass band we see the steep decline of the channel selection frequency characteristic of the BBF. The fact that loss in gain between schematic simulations and simulations including extracted parasitics is only about 3 dB for the whole receiver front-end indicates that the physical layout implementation of the front-end is highly optimized for analogue circuit performance.

5.4.1.3. Noise Performance

Another important performance characteristic of the receiver front-end is the noise performance. The simulation results for the noise performance are plotted in Fig. 5.14. The overall NF for baseband frequencies $f_{IF} > 10$ kHz is dominated by the noise performance of the LNA. This is

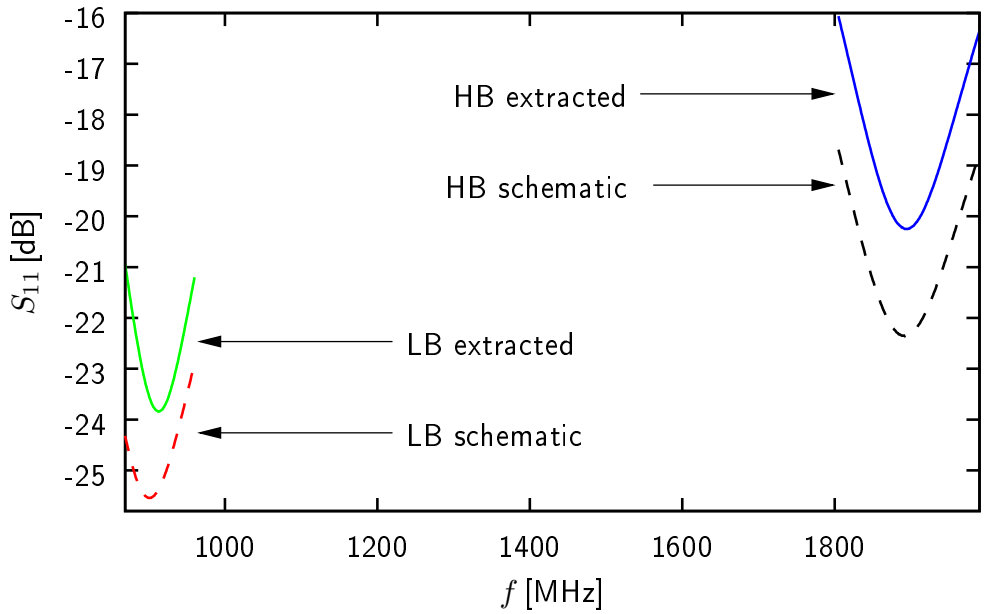


Figure 5.12.: Simulation results for input power match S_{11} vs. RF input frequency f_{RF} of the receiver front-end for the combi-matching for the GSM low bands and the high bands, respectively.

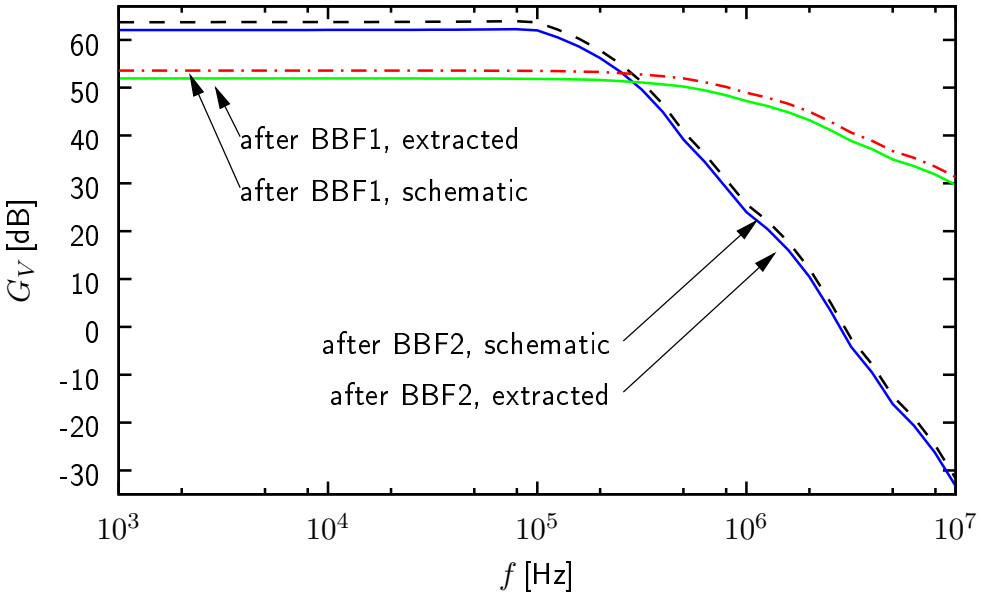
especially true for the high band mode of operation. Below $f_{IF} < 10\,\text{kHz}$ the overall NF rises from the thermal level due to the impact of flicker noise. The flicker noise is contributed to a large degree by the BBF.

5.4.1.4. Linearity

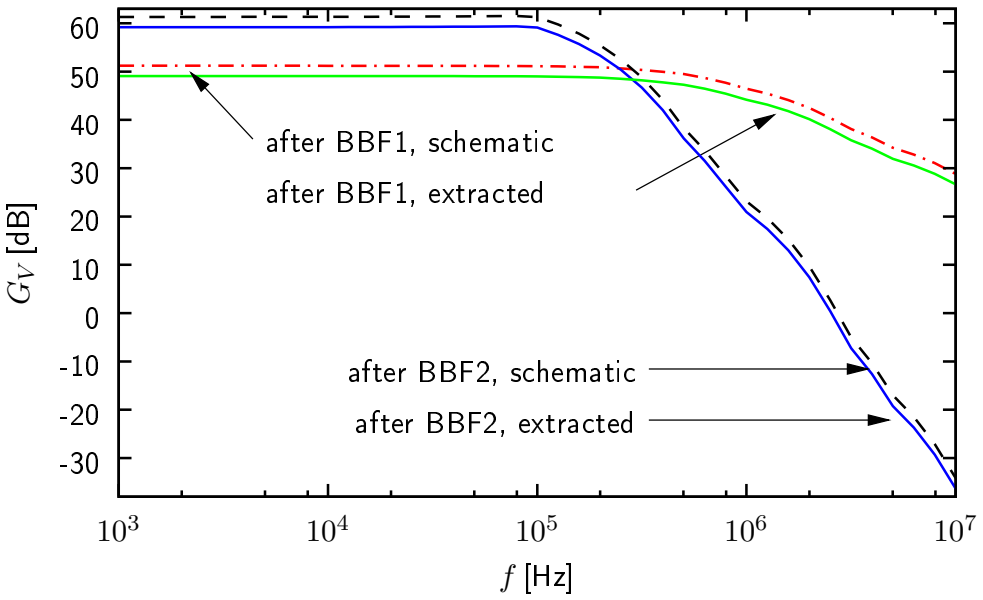
Large-signal linearity analyses for the overall receiver front-end could not be performed at a satisfactory level due to convergence issues of the available simulation software and a lack of computational resources for the complex simulations. The IIP_3 for the receiver operating in the low band has been extracted from schematic level simulations with the RFDE harmonic balance solver. The results are listed in Table 5.9. However, the harmonic balance solver failed for the high band mode of operation. As we will see from the measurement results in the next Section 5.4.2 the linearity performance for the low band mode and the high band mode of operation is almost identical.

Table 5.9.: Simulation results for the IIP_3 of the implemented receiver front-end (schematic based).

Band	P_{IN}	IM_3 @ $f_{IF} = 30\,\text{kHz}$	IIP_3
	[dBm]	[dBm]	[dBm]
LB	-70	-113.6	-16.1
LB	-65	-100.3	-16.9



(a) GSM low band mode.



(b) GSM high band mode

Figure 5.13.: Nominal simulation results for the voltage gain G_V of the receiver front-end in the GSM bands vs. baseband frequency f_{IF}. The voltage gain is depicted after the first filter pole (BBF1) and after second baseband filter stage (BBF2). The LO frequency is set to $f_{LO} = 914.5\,\text{MHz}$ for the GSM low band mode and to $f_{LO} = 1897.5\,\text{MHz}$ for the GSM high band mode, respectively.

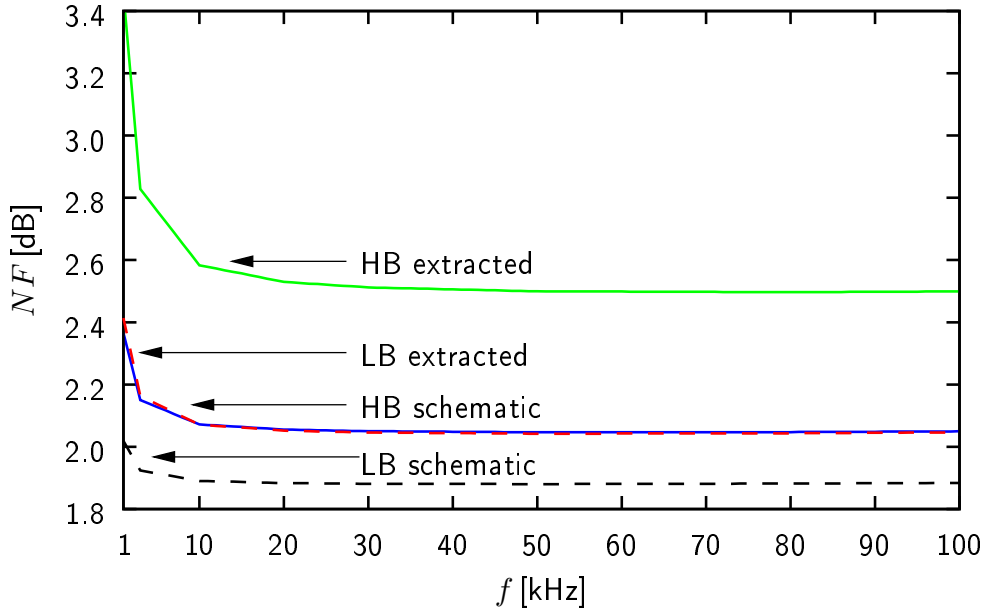


Figure 5.14.: Simulation results for the noise figure NF of the receiver front-end vs. baseband frequency f_{IF}. The NF is extracted after the after second baseband filter stage (BBF2). The LO frequency is centred at $f_{LO} = 914.5\,\text{MHz}$ for the low bands respectively at $f_{LO} = 1897.5\,\text{MHz}$ for the high bands.

5.4.2. Measurement Results

The measurement results presented in this section have mostly been recorded manually. The complexity of the analogue and digital functionality integrated on the testchip surpasses the analogue receiver front-end that is covered in this thesis by far. In order to properly evaluate the performance of the analogue front-end a large overhead in configuration and programming of registers has to be dealt with. An automated measurement set-up has only been available for the measurements of the achieved input matching. Thus the amount of data points that have been taken during most measurements is limited. Furthermore, the time frame during which the measurement equipment has been available has been very limited. Thus only a limited set of testcases has been recorded from a limited number of testchip samples.
The RF input signal is fed to the evaluation board via SMA connectors. The testchip does not provide the individual outputs for the circuit blocks of the analogue front-end of the receiver. The output voltage of the analogue front-end has been measured at baseband frequency behind the second stage of the BBF.
During the initial setting-up operation of the testchip it has become clear that the 2.5 V power supply (V_{DD2}) suffers from a serious design flaw. A misplaced tie-down diode at the gate of a PFET dummy device in a bandgap reference voltage source is forward biased when V_{DD2} is raised significantly beyond $V_{DD2} = 2.1\,\text{V}$. Although the faulty bandgap reference voltage source is outside the focus of this work it affects the analogue performance of the implemented receiver front-end. For voltages higher than 2.1 V the electrical behaviour of the 1.25 V bandgap output voltage exhibits a hysteresis. When V_{DD2} is raised e.g. up to 2.7 V the bandgap output voltage breaks down to half of its target value and recovers only when the supply voltage is lowered to $V_{DD2} = 2.1\,\text{V}$. The design flaw directly affects the bandgap voltage sources in the biasing circuits

for the implemented analogue front-end and for the DCO (digitally controlled oscillator). The buffers succeeding the bandgap voltage sources suffer from a lowered output voltage and exhibits an extremely poor power supply rejection ratio when operated from a 2.1 V supply instead of a 2.5 V supply. This makes the impact of the design flaw on the analogue performance even worse as the reference voltages or reference currents in the complete analogue receiver front-end derived from the output voltage of bandgap buffer become noisy and deviate from their target values. In order to guarantee stable operation the supply voltage of the 2.5 V domain of the complete analogue front-end had to be lowered to a default value of 2.1 V for the measurements. As a consequence all internal reference currents for the analogue receiver front-end are down by approximately 10 % compared to the nominal values according to simulation. The design flaw has been corrected in subsequent testchip designs. Unfortunately, new testchip samples have not been available before the completion of this work. But simulation results indicate that the performance issues related to the design flaw in the bandgap reference voltage source will be overcome in future testchip designs.
The measurement results that are presented have been corrected for losses related to the measurement set-up like cable losses, insertion losses of the BalUns etc.
The measurement equipment used consisted of Agilent 'E3631A' *dc* bias sources, Rhode and Schwarz 'FSQ 8' spectrum analysers, Rhode and Schwarz 'SMIQ 06B' signal generators and Rhode and Schwarz 'ZVB 8' network analysers.

5.4.2.1. DC Current Consumption

The simulated current consumptions of the circuit blocks are compared to the measured current consumption in Table 5.10.
It can be seen that both LNAs consume less current in reality than has been simulated. This might indicate ohmic losses in the current mirror that set the *dc* currents through both stages of the LNAs. Due to the design flaw that affects the bandgap circuits and the bandgap buffer however there is a possibility that the reference current in the primary current mirror branch of the LNA is reduced, too. For the circuit blocks of the front-end that are operated from 2.1 V instead of 2.5 V the reduced current consumption can be traced back directly to the reduced supply voltage.
Along with the reduced current consumption we have to expect performance degradation for the complete analogue front-end in terms of e.g. gain and linearity.

5.4.2.2. Input Return Loss

The general layout of the evaluation board for the testchip in the area of the chip input differs from the best-guess that has been used for pre-tape-out simulations. Whereas the chip input impedance has been optimised for matching to an external SAW band selection filter during simulations, the evaluation boards have been equipped with a BalUn for band selection, impedance transformation (50 Ω to 200 Ω) and single-ended to differential conversion. The frequency characteristic of the BalUn is not as selective as the frequency characteristic of the SAW-Filter that is in focus for the final system on the PCB in the phone. In fact it is possible to measure both GSM low bands respectively both GSM high bands with a single Balun without severe performance degradation.

Table 5.10.: *DC* current consumption of the front-end blocks.

Block	I_{DC} Simulation	I_{DC} Measurement	V_{DD}
Unit	[mA]	[mA]	[V]
LNA LB	9.0	6.8	1.4
LNA HB	9.7	7.1	1.4
Divider LB	6.9	6.4	1.4
Divider HB	3.9	5.8	1.4
Mixer	7.5	5.5	2.1
BBF	6.6	4.3	2.1

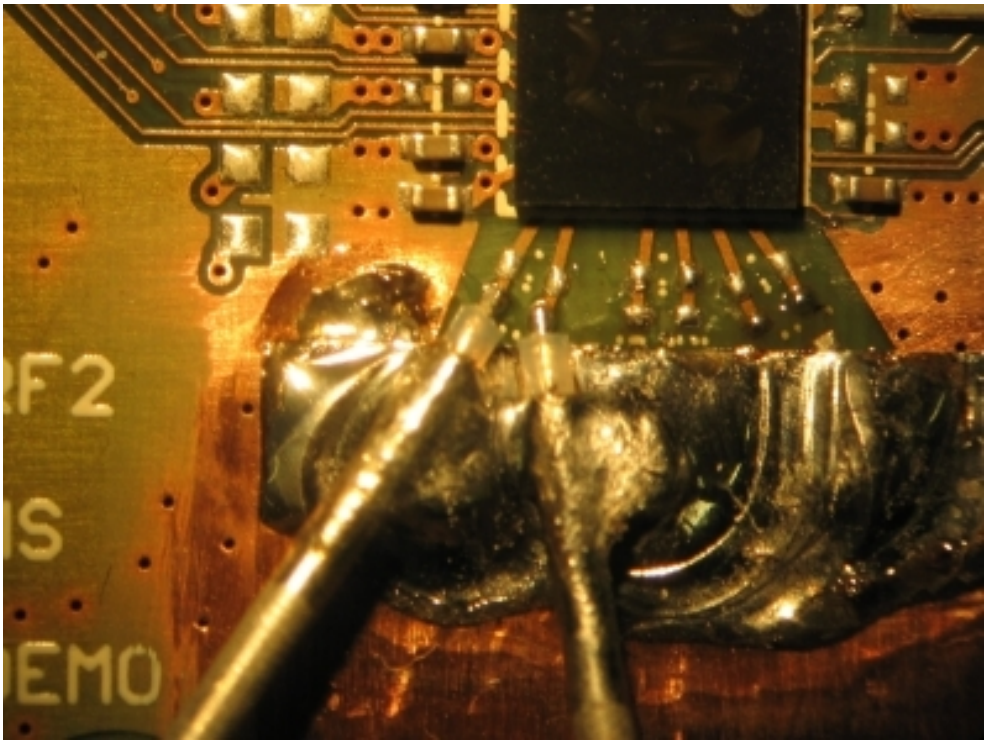


Figure 5.15.: Photograph of the chip input for the improvised measurements of the chip input impedance with shielded lines soldered close to the chip input.

In addition a rough estimation adds $L = 1\,\text{nH}$ of series inductance for every millimetre of signal line length on the evaluation PCB. Thus the determined SMD component values necessary for proper input power matching of the chip cannot be expected to be identical in simulations and the actual measurements.
Furthermore, no S-parameter board has been available in order to accurately determine the unmatched input impedances of the testchip. The input impedance of the unmatched chip inputs have been obtained from measurements with modified evaluation boards (Fig. 5.15) that allow for a connection of shielded lines close to the chip input and provide a decent RF ground plane. Although the set-up for the measurements has been improvised acceptable input matching per-

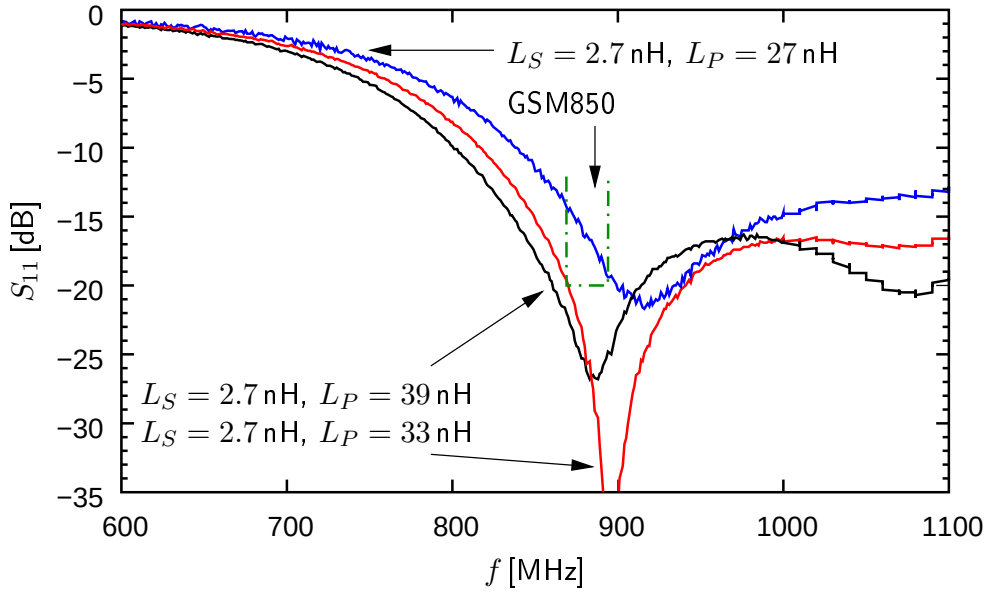
Table 5.11.: Final values that where chosen for the matching elements (in $L_S - L_P-$topology) on the evaluation board (column 2 and 3). The matching proposed for a combi-matching of both low respectively both high bands are listed in column 4 and 5.

Band	individual match		combi-match	
	L_S	L_P	L_S	L_P
Unit	[nH]	[nH]	[nH]	[nH]
GSM850	2.7	39	2.7	33
GSM900	2.7	33		
DCS1800	2.2	8.2	2.2	8.2
PCS1900	1.5	8.2		

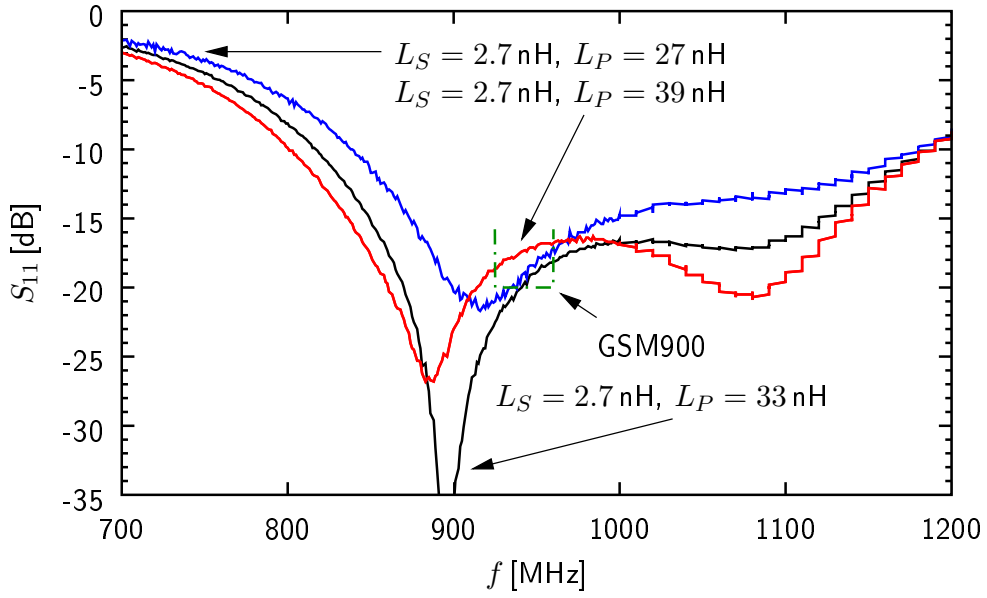
formance has been achieved with a very limited number of iterations from the data obtained from the improvised measurements. The data plots in Fig. 5.16(a) to Fig. 5.17(b) illustrate the input power match S_{11} for the four GSM bands (850, 900, 1800, 1900). Although the chip inputs are the same for both low bands respectively both high bands the BalUns and the components of the matching networks are specifically chosen to provide the best possible matching for the individual GSM band. Each plot contains data not only for the final matching elements (cf. Table 5.11) that have been soldered onto the evaluation board but also data from the iterations to the best matching network elements. For the input power match an automated measurement set-up has been available. Table 5.11 also lists the matching elements that are proposed for a combi-matching of both low bands respectively both high bands. Even with the combi-matching network $S_{11} < -14\,\text{dB}$ has been measured for all GSM bands.
Simulation results for receiver front-end with $V_{DD2} = 2.1\,\text{V}$ do not indicate severe deterioration of the input return loss.

5.4.2.3. Voltage Gain

As the voltage gain (Fig. 5.18(a) and Fig. 5.18(b)) has been recorded manually only three data points have been taken for every frequency band and evaluation board. The output voltage has been measured at a baseband frequency of $f_{IF} = 30\,\text{kHz}$. The measurement results confirm that neither the matching network nor the frequency characteristics of the equipped BalUns introduce severe selectivity to the frequency characteristics of the testchip performances. The relatively small decrease in gain in the frequency range $869\,\text{MHz} < f < 960\,\text{MHz}$ respectively $1805\,\text{MHz} < f < 1990\,\text{MHz}$ is credited to a large degree to the lowpass characteristics of the LNAs rather than the frequency selectivity of the input network on the same evaluation board. In general the measured evaluation board equipped with a BalUn and matching network for the GSM850/1800 bands tends to exhibit up to $\Delta G_V \approx 1.5\,\text{dB}$ more than its counterpart equipped with a BalUn and matching network for the GSM900/1900 bands. Due to the limited number of samples measured it can not be concluded whether the difference in gain is a systematic property related to the different BalUns and matching networks or a stochastic property of the testchip samples equipped on this boards.
In the high band mode of operation we lose up to $\Delta G_V \approx 4\,\text{dB}$ compared to the low band mode of operation. The simulation results in Table 5.3(a) and Table 5.3(b) suggest that a gain difference



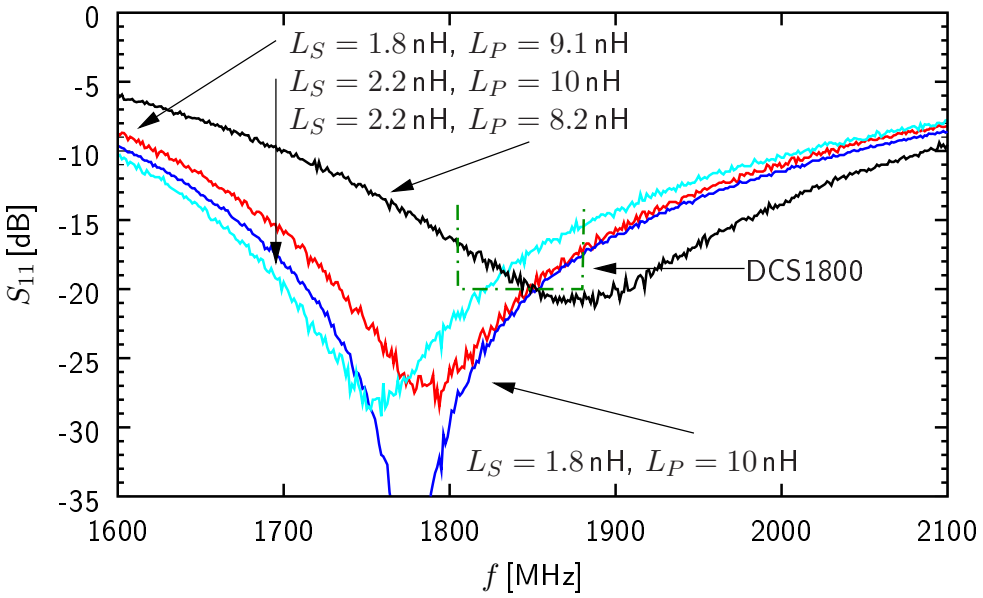
(a) GSM850.



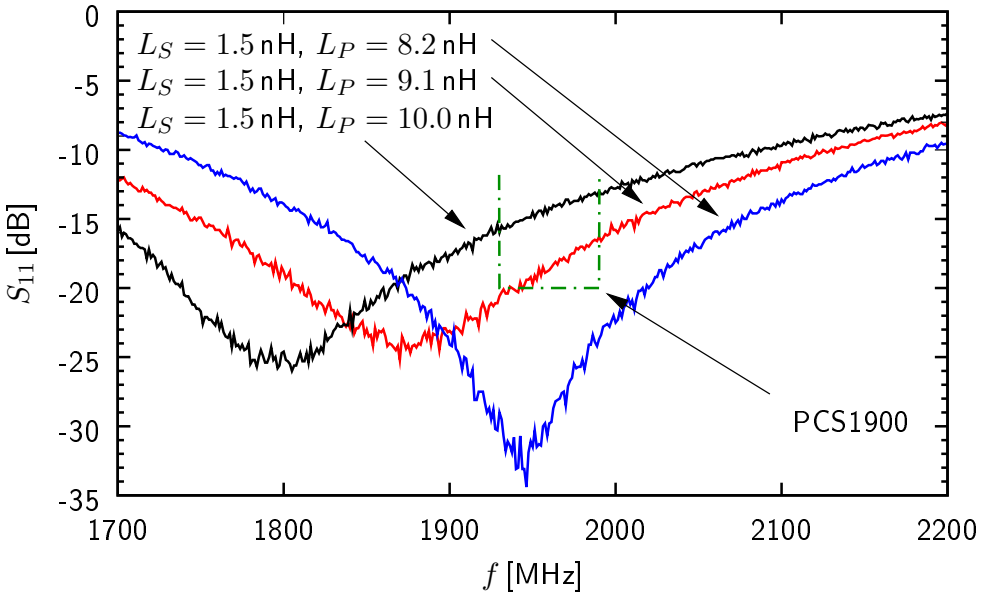
(b) GSM900.

Figure 5.16.: Input return loss S_{11} measured for the GSM low band inputs of the testchip with different matching elements. The dotted line indicates the band of interest.

of $\Delta G \approx 2.4\,\mathrm{dB}$ can be traced back to the LNAs in the front-end.
Simulation results for the receiver front-end with a lowered supply voltage $V_{DD2} = 2.1\,\mathrm{V}$ in the 2.5 V domain and the associated reduced reference currents indicate a voltage gain of $G_V = 60.8\,\mathrm{dB}$ at $f_{RF} = 914.5\,\mathrm{MHz}$ and $G_V = 58.0\,\mathrm{dB}$ at $f_{RF} = 1897.5\,\mathrm{MHz}$ (extracted parasitics included; $f_{IF} = 30\,\mathrm{kHz}$). Keeping in mind the fact that the testbench had to be simplified to enable the complex front-end simulations the simulation results match the measurement results



(a) DCS1800.

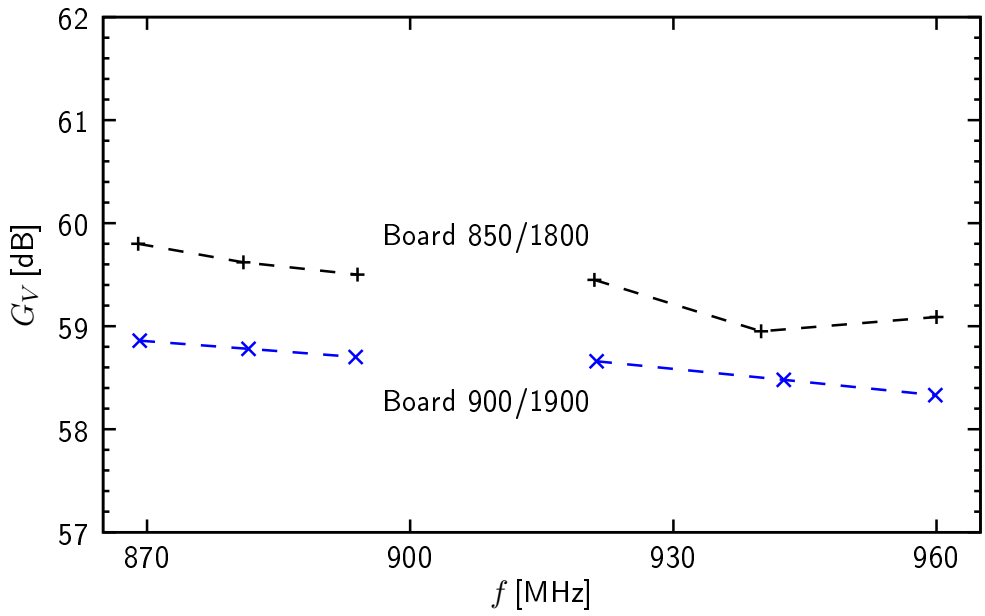


(b) PCS1900.

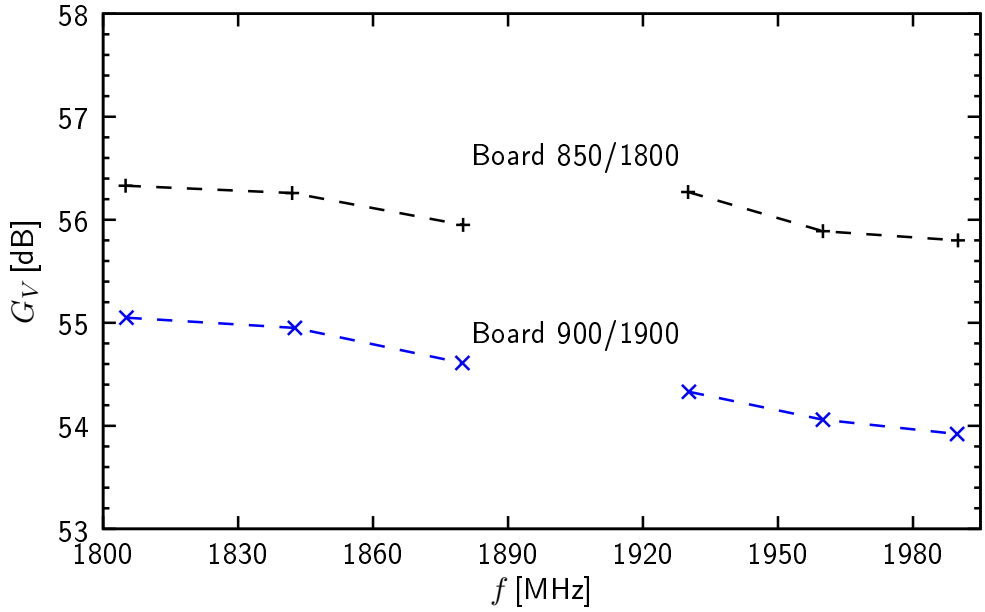
Figure 5.17.: Input return loss S_{11} measured for the GSM high band inputs of the testchip with different matching elements. The dotted line indicates the band of interest.

fairly accurately.

In Table 5.12 the measurement data for the gain steps implemented for the LNAs and the BBF is presented. The resulting overall ΔG_V is $\Delta G_{V,LB} = -43.2\,\mathrm{dB}$ for low band operation and $\Delta G_{V,HB} = -40.5\,\mathrm{dB}$ for high band operation if both LNA and BBF are set to low gain mode.



(a) GSM low bands.



(b) GSM high bands.

Figure 5.18.: Measurement results for the voltage gain G_V in the GSM bands vs. RF input frequency f_{RF} ($f_{IF} = 30\,\text{kHz}$). The boards equipped with BalUns and SMD matching elements for the different GSM bands show only a slight deviation in gain. V_{DD} is set to 1.4 V. V_{DD2} is set to 2.1 V.

Table 5.12.: Measured voltage gain steps of the receiver front-end blocks LNA and BBF.

	GSM850	GSM900	DCS1800	PCS1900
LNA ΔG_V[dB]	-19.5	-19.4	-16.9	-16.8
BBF ΔG_V[dB]	-23.7			

5.4.2.4. Noise Performance

As mentioned at the beginning of this section the design flaw in the bandgap reference voltage source is responsible for noisy bias currents that affect not only circuit blocks that are nominally operated from a 2.5 V supply but also blocks like the LNA that is nominally operated from a 1.4 V supply. Furthermore, the operation of the mixer cell and the operational amplifiers in the BBF from a 2.1 V supply instead of a 2.5 V supply will deteriorate the noise performance of the analogue front-ends blocks.
The measured noise performance is listed in Table 5.13. The measurement results given are for two testcases. In one testcase the LO signal is fed externally, in the other testcase the LO signal is generated internally by the integrated DPLL (digital phase locked loop) of the testchip. Whereas the measurement results are comparably stable for the high bands it turns out that the internal LO signal generation suffers from severe performance issues. The measured NF especially for the GSM850 band is unreasonably high. When the LO signal has been generated internally spur signals emerging in the band of interest due to the design flaw in the DCO biasing prevented sophisticated measurements of the noise performance. When the LO signal has been fed externally the impact of the impedance mismatch at the LO chip input is responsible for lack of sophisticated measurement data.
The source of the spur signals in the GSM850 and GSM900 band caused by the DPLL has been identified by a focus team and thus noise performance data in accordance with the simulation results are expected from the measurements of future testchips.
Simulation results for the receiver front-end with a lowered supply voltage $V_{DD2} = 2.1\,\text{V}$ in the 2.5 V domain and the associated reduced reference currents indicate a noise figure of $NF = 2.5\,\text{dB}$ at $f_{RF} = 914.5\,\text{MHz}$, $f_{IF} = 1\,\text{kHz}$ and $NF = 2.1\,\text{dB}$ at $f_{IF} = 80\,\text{kHz}$, respectively $NF = 3.8\,\text{dB}$ at $f_{RF} = 1897.5\,\text{MHz}$, $f_{IF} = 1\,\text{kHz}$ and $NF = 2.7\,\text{dB}$ at $f_{IF} = 80\,\text{kHz}$ (extracted parasitics included). Thus simulation (in the high band mode) and the measurement results for the noise performance match even better than the results for the voltage gain. The deviation of the results only in the low band mode underlines the conclusion that the noise performance in the low band mode is degraded by some circuit block not under investigation in this work during the measurements.
For the measurement of the noise performance a Noise Com NC346 noise source has been used.
The data in Table 5.14(a) and Table 5.14(b) gives an idea how the different circuit blocks in the receiver front-end contribute to the total noise according to simulation (including extracted parasitics, $V_{DD2} = 2.1\,\text{V}$). The table gives simulation results for $f_{IF} = 1\,\text{kHz}$ and for $f_{IF} = 80\,\text{kHz}$. At $f_{IF} = 1\,\text{kHz}$ the opamp in BBF1 adds a significant flicker noise contribution to the overall noise while the other stages of the receiver front-end mainly contribute thermal noise. At $f_{IF} = 80\,\text{kHz}$ flicker noise contributions are negligible and the thermal noise contributions dominate the overall noise. Then the noise contribution of BBF1 and BBF2 is very small.
It is interesting to see that if we follow the low band signal path up to BBF1 the accumulated

Table 5.13.: Measured spot noise figure NF at $f_{IF} = 80\,\text{kHz}$ for the analogue front-end at $T = 25\,°\text{C}$.

NF				
VCO	GSM850	GSM900	DCS1800	PCS1900
	[dB]	[dB]	[dB]	[dB]
internal	(6.7)	(3.4)	2.9	3.1
external	(7.1)	2.4	2.9	3.3

noise figure is almost equal for $f_{IF} = 1\,\text{kHz}$ and $f_{IF} = 80\,\text{kHz}$. The significant flicker noise contribution of the opamp in BBF1 is responsible for the difference in the accumulated noise figure at the end of BBF2.
The sum of the individual contributions in Table 5.14(a) and Table 5.14(b) do not add up to a full 100 % as only a limited numbers of contributions could be considered when analysing the simulation results.

5.4.2.5. Linearity

The measurement results for input referred IP_3 are listed in Table 5.15. The testcase resembles the intermodulation distortion testcase from [39] where two interferer signals located at a frequency offset $\Delta f = 800\,\text{kHz}$ and $\Delta f = 1600\,\text{kHz}$ from a wanted signal at f_0 generate an intermodulation product in the channel of interest.
As there is no significant deviation in IIP_3 performance to be expected between the individual low bands respectively the individual high bands Table 5.15 lists only one IIP_3 for the low bands and one for the high bands. As an attempt to measure the IIP_3 when the voltage of the nominal 2.5 V supply is raised from 2.1 V to 2.4 V does not indicate a significant improvement it is concluded that the IIP_3 of the receiver front-end is dominated by the LNA. The LNA is not affected if the supply voltage of the nominal 2.5 V domain is raised as it is operated from $V_{DD} = 1.4\,\text{V}$ and the interferer signals are not damped by any frequency selectivity of the LNA. The latter mentioned facts underline the dominant impact of the LNA odd order distortion performance. Table 5.16 summarises the measurement results for the 1 dB compression point measured with the desensitisation method where a large blocking signal is applied with certain frequency offset (here $\Delta f = 3\,\text{MHz}$) to the small wanted signal. Analytical theory gives $CP1i = P_{Blocker} + 3\,\text{dB}$ [12]. As this measurement also quantifies the odd order distortion performance of the analogue receiver front-end as does the measurement of the IP_3 we expect $CP1$ to be almost constant when V_{DD2} is switched between 2.1 V and 2.4 V for the same reasons mentioned in the discussion of the IP_3 measurements.

For reasons of completeness $CP1$ has also been determined with classical direct single-tone measurements. The results are listed in Table 5.17. When a large signal is in the wanted channel the odd order distortion caused by every block in the receive chain adds to the overall odd order distortion. The fact that the reduction in G_V (cf. Table 5.12) does not linearly translate into the increase in the overall $CP1i$ between the measurements is credited to the contribution of multiple blocks in the receive chain adding to the overall distortion. It is no longer possible to make reasonable assumptions about dominant contributions of individual circuit blocks.

The measurement results for the IIP_2 of the analogue front-end are listed in Table 5.18. The

Table 5.14.: Simulated noise contributions in the receiver front-end (including extracted parasitics, $V_{DD2} = 2.1\,\mathrm{V}$).

(a) Low band mode.

Block	Contribution	Accumulated NF	Contribution	Accumulated NF
	@$f_{IF} = 1\,\mathrm{kHz}$		@$f_{IF} = 80\,\mathrm{kHz}$	
	[%]	[dB]	[%]	[dB]
Input Source	56.02	–	61.51	–
Matching element L_P	8.53	0.62	9.37	0.62
LBLNA	18.62	1.72	20.90	1.74
Mixer input stage	1.74	1.81	1.54	1.81
Mixer switching stage	3.22	1.97	3.53	1.97
LO buffer	0.04	1.97	0.00	1.97
BBF1	5.31	2.22	0.07	1.97
BBF2	0.62	2.25	0.32	1.99
Not considered Δ	5.90	0.25	2.76	0.12

(b) High band mode.

Block	Contribution	Accumulated NF	Contribution	Accumulated NF
	@$f_{IF} = 1\,\mathrm{kHz}$		@$f_{IF} = 80\,\mathrm{kHz}$	
	[%]	[dB]	[%]	[dB]
Input Source	41.32	–	54.29	–
Matching element L_P	10.32	0.97	13.56	0.97
HBLNA	11.84	1.86	16.44	1.91
Mixer input stage	3.08	2.07	3.02	2.06
Mixer switching stage	5.07	2.39	7.00	2.40
LO buffer	0.04	2.39	0.00	2.40
BBF1	22.86	3.59	0.23	2.41
BBF2	0.74	3.63	0.58	2.44
Not considered Δ	4.73	0.21	4.88	0.21

Table 5.15.: Measured input referred IIP_3. RF input signals at $f_1 = f_0 + \Delta f$ and $f_2 = f_0 + 2\Delta f$ with $\Delta f = 800\,\text{kHz}$ and $f_{IF} = 30\,\text{kHz}$.

	$IIP_3@V_{DD2} = 2.1\,\text{V}$	$IIP_3@V_{DD2} = 2.4\,\text{V}$
Band	[dBm]	[dBm]
LB	-16.3	-16.3
HB	-16.2	-16.4

Table 5.16.: Input referred blocker power $P_{Blocker}$ of a blocker signal at a frequency offset of $\Delta f = 3\,\text{MHz}$ from the wanted signal that leads to a decrease in the gain of the wanted signal of 1 dB and calculated $CP1i$. (desensitisation measurement).

	$P_{Blocker}@V_{DD2} = 2.1\,\text{V}$	$P_{Blocker}@V_{DD2} = 2.4\,\text{V}$	$CP1i$
Band	[dBm]	[dBm]	[dBm]
LB	-29.7	-29.2	≈ -26.5
HB	-28.7	-28.7	≈ -25.7

Table 5.17.: Measured input referred in-band $CP1$ with LNA and BBF in high gain mode (column 1) and low gain mode (column 2) at $f_{IF} = 30\,\text{kHz}$.

	$CP1i$ high gain mode	$CP1i$ low gain mode
Band	[dBm]	[dBm]
LB	-47.8	-20.5
HB	-44.0	-20.4

Table 5.18.: Measured input referred IIP_2. RF input signals at $f_1 = f_0 + \Delta f$ and $f_2 = f_0$ with f_0 at mid-band frequency and $f_{IF} = 30\,\text{kHz}$.

IIP_2 [dBm]	Board	V_{DD} [V]	Band	Δf [MHz]
33.9	850/1800	2.1	DCS1800	−6
34.0	850/1800	2.1	DCS1800	+6
43.4	850/1800	2.4	DCS1800	+6
30.1	850/1800	2.1	DCS1800	+10
39.1	900/1900	2.1	GSM900	−6
38.4	900/1900	2.1	GSM900	+6
42.2	900/1900	2.4	GSM900	+6
42.2	900/1900	2.1	GSM900	+10
37.5	900/1900	2.1	DCS1800	+6
43.0	900/1900	2.4	DCS1800	+6

testcase set-up used for the measurements resembles the AM suppression testcase from [39] where interferer signal is spaced $\Delta f = 6\,\text{MHz}$ from the wanted signal. Additional measurements have been performed with the interferer signal at a frequency offset of $\Delta f = 10\,\text{MHz}$.
The data in Table 5.18 proves that the IIP_2 performance improves significantly when the supply voltage in the nominal 2.5 V domain is raised. This corresponds with the theoretical expectations. Theory tells that the even order distortion performance especially of a direct-conversion receiver is dominated by the baseband circuit blocks (cf. Section 3.2.3). As the baseband blocks, especially the operational amplifiers in the BBF, are operated from the 2.5 V supply domain the IP_2 performance responds to a raised supply voltage in this supply domain. For future testchips without the design flaw that prevents the setting $V_{DD2} = 2.5\,\text{V}$ a superior IP_2 performance is expected. In its current implementation the receiver front-end violates the IIP_2 specification given in Table 3.5 if operated from $V_{DD2} = 2.1\,\text{V}$.
On the same PCB with the same testchip sample the IIP_2 is about the same for low band and high band operation. This suggests that none of the LNAs introduces severe even order distortion to the front-end.

5.5. Conclusion

The implemented receiver front-end consisting of two LNAs, a quadrature mixer and baseband filter has been introduced and evaluated by simulation and measurements. Especially the performance of the LNA that is in the focus of this work has been elaborated on in detail.
In general the analogue receiver front-end is working and functional. Although the achieved performance characteristics challenge the high performance specifications listed in Section 3.4.2 the general functionality has been confirmed and proven by measurements. Thus the transfer of the GSM receiver front-end from the 130 nm process technology to the 65 nm technology is considered a success.
Two major design flaws that tamper with the performance of the investigated testchip have been

found, identified and will be overcome in subsequent front-end implementations. Special measurement testcases indicate that severe performance improvements are to be expected once the design flaws have been overcome. New measurement results have not been available when this work has been handed in.
The software design environment helped to estimate the performance of the testchip profoundly prior to a physical tape-out. Simulations and measurements confirm that the performance of the front-end is superior in the low band mode of operation. As the baseband operation does not differ between low band or high band operation the performance degradation in the high band mode is credited to the RF part of the analogue front-end. This notion is confirmed by a comparison of the low band and high band LNA simulation results. Parasitic effects affect the high band LNA more than they affect the LBLNA.
It has already been stated that general functionality of the receiver front-end in 65 nm CMOS has been achieved and the performance metrics obtained from measurements indicate values similar to the implementation in the 130 nm technology. However this performance has been achieved with enhanced efforts in calibration and trimming. Although post tape-out tuning mechanisms are not covered in detail in this work their contribution to the achieved performances must not be underestimated.

6. Prospects of Technology Scaling for Analogue RF Circuitry

Having analysed CMOS process technology scaling from 130 nm to 65 nm in Chapter 4 it is now time to take a look at future scaling trends of CMOS process technologies.
At the beginning of this chapter we will evaluate the performance prospects for analogue RF circuit design of future CMOS technologies based on the lessons learned in this work. The chapter will continue with a brief outlook on new integrated devices that are promising candidates for replacing conventional devices. New approaches for overcoming the short-comings of current technology issues are introduced. As the engine for the on-going shrink of CMOS technologies is economical benefit, costs savings for typical wireless applications are analysed thereafter.

6.1. Performance Evaluation of Conventional CMOS Shrinks

Without doubt new CMOS technology nodes bring large benefits for circuit design in the digital domain e.g. in terms of speed and power *ac* consumption. There is one prominent drawback known from conventional CMOS technology scaling for the digital domain and that is increased gate leakage currents and the resulting power consumption in static operation.
For the analogue domain drawbacks and limits of upcoming process technology generations have partly been discussed in Section 4.3. Thus we present only a brief outlook here.

Amplifying Potential. The amplifying potential of CMOS transistors reduces with CMOS scaling for minimum transistor devices. Thus these minimum devices will find less and less usage in analogue circuit design except for applications far beyond the lower gigahertz range. In the application example of this work, a GSM receiver front-end operating at a frequency no higher than $f = 2\,\mathrm{GHz}$, transistors with a gate length $l > l_{MIN}$ are employed even in the RF signal path (cf. Section 5.2.2). In Section 4.2.1.2 it is shown that the amplifying potential g_M/g_{DS} of a device improves over the amplifying potential of a device from a previous technology generation for similar bias conditions when the transistor dimensions l, w are not scaled at the cost of a reduced transit frequency (cf. Fig. 4.15).

Transit Frequency. As it has already been indicated above, analogue designers will favour transistors with a sophisticated amplifying potential over transistor devices with an extremely high f_T if not absolutely necessary for the target application. Nevertheless higher transit frequencies will be achieved with minimum transistor devices of future CMOS technologies.

Flicker Noise. We have seen in Table 4.7 that the noise performance deteriorates with a reduced channel length. Especially the corner frequency severely increases for the technology step from 130 nm to 65 nm that has been investigated in detail. This deterioration will impose

constraints on the design of analogue circuitry operating at low frequencies e.g. analogue BB circuitry of receiver front-ends. Longer gate lengths of transistor devices as well as improved circuit topologies e.g. a mixer cell with passive *dc* current-free switches help to mitigate the increased flicker noise.

Supply Voltage and Reliability. Thinning SiO_2 gate oxides require the supply voltage to be scaled down with technology generations for reliability reasons. For SiO_2 gate oxides a feasible lower limit of $t_{OX} \approx 1 - 2\,\text{nm}$ for reliability and thermal stability is expected. In addition the enormous maximum packing density that is achieved by minimum active devices in digital applications requires a reduction of the supply voltage and power consumption in order to prevent thermal breakdowns. The lowered supply voltage has reached a level where it tampers with the performance of classical analogue circuit topologies e.g. using cascodes require a $V_{DD} > 0.8\,\text{V}$. The figures of merit achieved with low voltage topologies in general fall behind conventional topologies. The operation of active devices in the sub-threshold region moves into the focus of research [33]. New innovative topologies are required for the analogue design to advance in the presence of low supply voltages. Devices with thicker gate oxides are available in modern CMOS technologies but the fabrication of these devices requires additional processing steps which is reflected in higher mask and manufacturing costs.

Parasitic Devices. With the shrinking physical dimensions of the implemented devices the parasitics (resistances and capacitances) associated with circuit components generate a growing influence on the overall performance. The routing of signal lines and interconnections will have a dominant impact on circuitry made up of minimum devices.

Passive Components. Among the passive components of an IC capacitors and inductors are the most critical to implement.
It has already been said that the capacitance density of VPP-caps is expected to scale with CMOS technology as the vertical structures move closer. For analogue designers with a need for linear devices VPP are the capacitors of choice in modern CMOS technologies. In contrast to MIM-caps they do not need additional processing steps. When higher capacitance densities are needed different types of capacitor realisations connected in parallel e.g. MOS-CAPS and VPP-CAPS can be used. MOS-CAPs offer a high capacitance density but they also introduce non-linearity to the circuit. Creative means to compensate this inherent non-linearity are in the focus of research (cf. Section 4.2.2).
The performance and the quality factor of integrated inductors suffers from the digital heritage of a low ohmic substrate and an increased resistance of the interconnect metal. Due to the die area consuming nature of coils analogue designers strive to avoid coils in integrated chip design. This trend is sure to continue as integrated inductors do not scale with the technology generations if the operating frequency does not increase.

Reconfiguration. Reconfiguration is an important aspect in modern system design. Explicit reconfiguration in order to gain flexibility e.g. a switching between multiple services reduces the hardware need for parallel hardware resources. Picking a special service from multiple

available services is excessively exercised in transceivers in the software defined radio approach.

Calibration. Due to reduced performance margins post tape-out calibration will become more vital in the future of analogue RF CMOS design. The analogue designer has to foresee shortages related to process technology variations and to implement means to overcome these shortages if necessary. Shortages can be related e.g to an increased difficulty in modelling the device behaviour when the device is subjected to electro-magnetic disturbances in a single-chip integration.

6.2. Definition of Future CMOS Technology Nodes

The ITRS 2007 predicts the extension of Moore's Law for more than a decade [11]. CMOS transistors with a gate length $l = 10\,\text{nm}$ are announced for 2021 for usage in wireless communication devices in [10]. CMOS process technologies beyond the 22 nm node are considered realistic [49]. The progress in the miniaturisation of transistors will continue to set the pace of process technology scaling.
Conventional single-gate planar FETs have been pushed close to their performance limits during CMOS scaling in the past. Research publications indicate that conventional planar bulk transistors will be succeeded by vertical metal multi-gate devices [27], [38] with FinFET architecture [28] or SON (Silicon On Nothing) architecture [16]. These multi-gate devices promise improved channel control and reduced short-channel effects. Self-alignment of the two or more gates to each other and to the drain and source regions has been demonstrated among other manufacturing properties that guarantee compatibility to conventional CMOS process technologies. Literature presents encouraging statements about increased transconductance, decent sub-threshold characteristics that enable high on/off channel current ratios and a suitability for low voltage operation of the devices. High-k_{DIEL} dielectric materials are prone to replace the conventional SiO_2 gate oxide without degradation of the interface characteristics or reliability and are even reported to reduce gate leakage currents by more than 10 % stepping from 65 nm to 45 nm [38]. High k_{DIEL} gate oxides increase the gate oxide capacitance C_{OX} of the transistors and thus the transconductance of the devices (cf. 4.9). With the transconductance especially the flicker noise is expected to increase $i_{nf} \propto g_M^2$ according to (4.21). The first processors manufactured in 45 nm CMOS with hafnium based k_{DIEL} gate oxides have been shipped in 2007 [38].
It can be observed that there is a tendency to increase the number of interconnect metal layers. Section 4 reports 5 copper layers for the 130 nm technology compared to 6 copper layers for the 65 nm technology while 9 copper layers reported for a 45 nm technology in [38]. The insulator between the interconnect layers will be low-k_{DIEL} material in order to reduce capacitive coupling between layers. Thus simple horizontal parallel plate capacitors will not improve their capacitance density in the future. VPP-caps have the most perspective use in future analogue RF design with a tendency to increase their capacitance density as minimum lateral dimensions are shrinking.
Special analogue and RF options that e.g. provide thick top metals for coils or higher ohmic substrate for noise isolation and reduced cross-talk will likely be available in future CMOS processes, too. Whether these options are chosen for analogue design is pre-dominantly a matter of production costs.

6.3. Cost Considerations

The topic of costs associated with the shrink of CMOS technologies is often discussed contradictorily. When considering the implementation of an IC in a new process technology generation for reasons of a more cost effective implementation the functionality of the IC has to be investigated beforehand in order to calculate the shrinking potential of the IC.
We will focus on the die area costs of integrated wireless chips running in high volumes. For ICs in mass production the die area costs dominate the overall costs of the IC production.
It is approximated that the area consumption of digital functionality A_{DIG} is approximately proportional to the square of the minimum gate length l

$$A_{DIG} \propto l^2. \tag{6.1}$$

In contrast, the area consumption of analogue functionality is only expected to scale approximately proportional to l

$$A_{ANA} \propto l. \tag{6.2}$$

The total die area consumed by the system is given by

$$A_{TOT} = A_{DIG} + A_{ANA}. \tag{6.3}$$

Moreover, the cost multiplier k per silicon area ranges from $k = 1.2$ to $k = 1.4$ from one technology node n to the next $n+1$ (n integer ≥ 0). The actual value of the cost multiplier is depending on time. When a new CMOS process technology node emerges on the market and silicon access is limited k will be high. When more foundries offer silicon access k will lower. As a first-time-right tape-out is very unlikely for a new product k will already be below its peak value when a chip enters mass production.
The total die area costs for a system $K(n)$ respectively $K(n+1)$ implemented in two succeeding technology nodes n and $n+1$ can be expressed as

$$K(n) = K_0(n) \cdot (A_{DIG}(0) + A_{ANA}(0)) \tag{6.4}$$

$$K(n+1) = (K_0(n) \cdot k) \cdot (A_{DIG}(n+1) + A_{ANA}(n+1)) \tag{6.5}$$

where

$K_0(n)$ Cost per die area in technology node n.

If we now formulate the shrinking potential s_i of functionality i

$$s_i = \frac{A_i(n+1)}{A_i(n)} = \text{const} \,\forall\, n, \tag{6.6}$$

and express the relative area consumption a_i of functionality i

$$a_i = \frac{A_i(1)}{A_{TOT}(0)}, \tag{6.7}$$

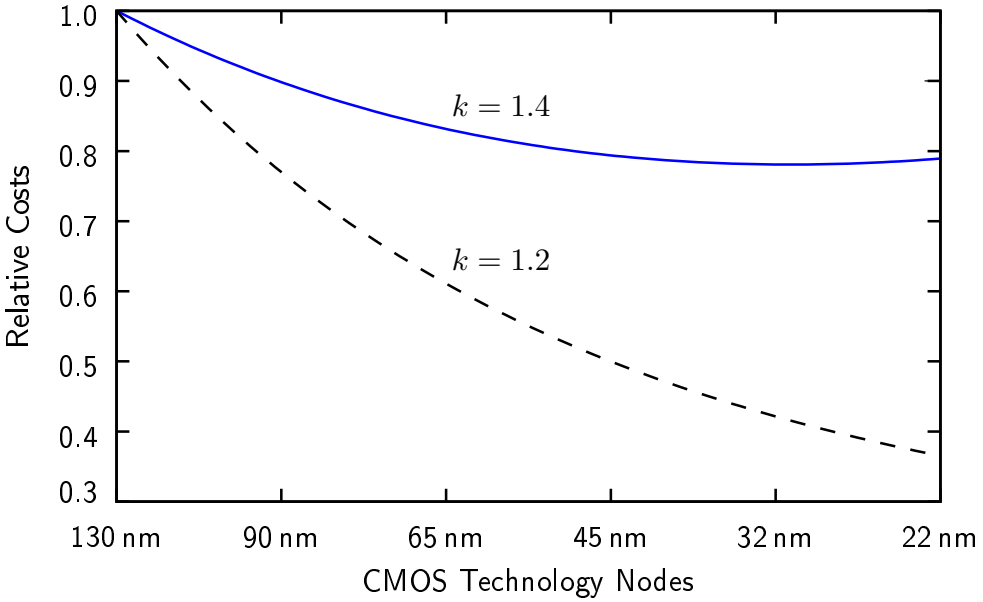


Figure 6.1.: Relative die area costs vs. CMOS process technology node for a SoC product ($s_{DIG} = 0.56$, $a_{DIG} = 2/3$ and $s_{ANA} = 0.80$, $a_{ANA} = 1/3$ in 130 nm CMOS).

the total die area cost at technology node n is expressed by

$$K(n) = K_0(0) \cdot k^n \cdot \sum_{0}^{\forall i} (a_i \cdot s_i^n). \tag{6.8}$$

Equation 6.8 is graphically illustrated in Fig. 6.1 for an SoC product with a fixed feature set e.g. a low cost GSM cell phone. The assumptions $a_{DIG} = 2/3$ and $a_{ANA} = 1/3$ seem reasonable [7]. The plots compare the effect different cost multipliers have on the overall die area costs. Whereas the total die area consumption decreases with every successful shrink the total die area costs do not. The costs run into saturation and even begin to rise again. The ratio $(a_{DIG}/a_{ANA})|_n$ decreases with every new technology node. Thus the total shrinking potential s_{TOT} of the SoC is reduced and ultimately converges to the shrinking potential of the analogue functionality s_{ANA}. For a chip dominated by analogue functionality we expect no economic benefit from technology shrinking as $s_{ANA} \cdot k \approx 1$.
In the example in Fig. 6.1 the die area costs for $k = 1.2$ decrease for the next 5 upcoming technology generations whereas the costs reach a minimum for $k = 1.4$. Even before this minimum is reached the cost advantage stepping from one generation to the next vanishes. If more than the pure die area consumption is considered for calculation of the chip costs (e.g. increased engineering costs for the transfer of a system to a new process technology node) the economical total minimum of production costs is reached beforehand.
If we take a closer look at SoC solutions that incorporate an enlarged feature set and extended information processing capabilities e.g. a 3G mobile communication device, the ratio a_{DIG}/a_{ANA} may deviate from the example in Fig. 6.1. On the one hand generations of wireless communication systems will demand more sophisticated digital processing resources. On the other hand upcoming multi-mode, multi-band mobile transceivers also introduce more complex, often re-configurable analogue and RF functionalities. Figure 6.2 contains parametric plots for various k and ratios

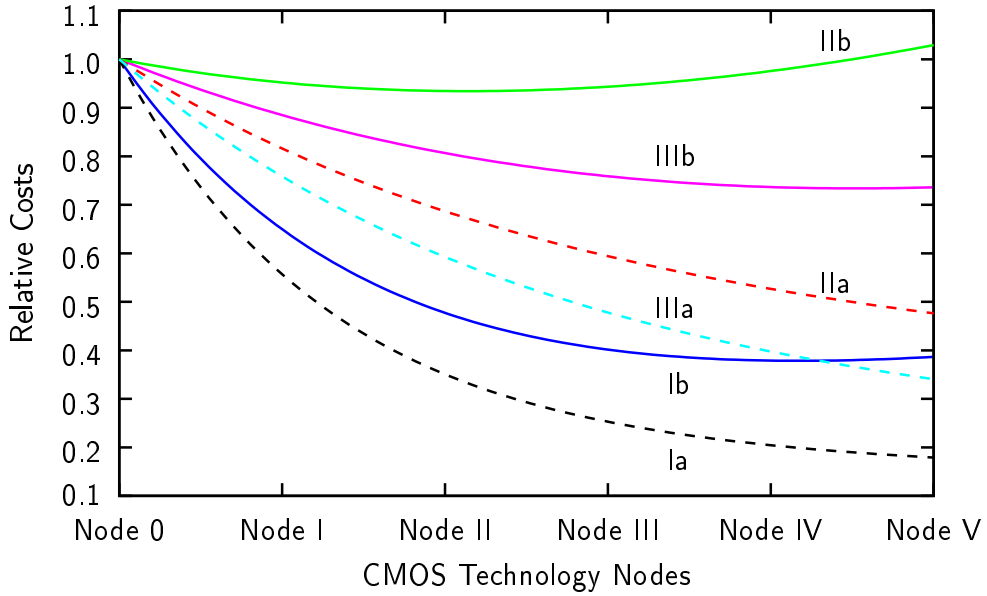


Figure 6.2.: Relative die area costs vs. CMOS process technology node for a SoC product in various scenarios extrapolated from the 130 nm CMOS node. I: $a_{DIG}/a_{ANA} = 4/1$, $s_{DIG} = 0.38$, $s_{ANA} = 0.80$; II: $a_{DIG}/a_{ANA} = 1/1$, $s_{DIG} = 0.56$, $s_{ANA} = 0.80$; III: $a_{DIG}/a_{ANA} = 7/3$, $s_{DIG} = 0.56$, $s_{ANA} = 0.80$. Dotted lines a $k = 1.2$, solid lines b $k = 1.4$.

a_{DIG}/a_{ANA} in order to get a feel for the die area cost development.
Plot I in Fig. 6.2 evidences that for a SoC with a relatively large proportion of digital functionality ($a_{DIG} = 0.80$) at node 0 (high-end 3G product), the die area cost reduction per technology node is diminished beyond node III even for an optimistic assumption about the shrinking potential of the digital functionality $s_{DIG} = 0.38$. The dominant cost reductions are achieved only by the first shrinking processes.
Plot II in Fig. 6.2 shows that for an equal die area consumption of analogue and digital functionality ($a_{DIG}/a_{ANA} = 1.00$) a reduction of die area costs is only possible for a low cost multipliers ($k \ll 1.4$).
Plot III in Fig. 6.2 resembles a contemporary mobile low-cost transceiver ($a_{DIG}/a_{ANA} = 7/3$). The economical decision about whether the transition to a new technology node makes sense strongly depends on the value of the cost multiplier at the time of mass production.
In conclusion the ratio of digital to analogue functionality a_{DIG}/a_{ANA} as well as the assumed cost multiplier k determine the optimum technology node for a system with a given feature set from the die area cost point of view. As analogue functionality exhibits a lower shrinking potential than digital functionality the die area of every application with fixed feature set will eventually become dominated by the analogue functionality unless new concepts are developed that render the analogue functionality obsolete. The analysis has stressed the mass production sector. For chips being fabricated in small numbers with engineering costs in the same order of magnitude as the pure die area costs a shrink in technology might not be advisory at all. Furthermore for especially analogue and RF dominated system parts do not exhibit sufficient shrinking potential to justify the step to a new process technology node. Only the integration with the digital baseband on to the same die justify a shrink. In an extended analysis sub-blocks that exhibit

less than $s_{ANA} = 0.80$ or no shrinking potential at all e.g. pads ($a_{PAD} = 0.08$, $s_{PAD} = 0.90$), coils ($a_{NO} = 0.30$, $s_{NO} = 1.00$) need to be considered in a more complex model for the die cost estimation. These sub-blocks will reduce the economical benefits of shrinks in technology for given systems. For a system with analogue or non-shrinking functionality dominating the die area consumption i.e. if the digital functionality has already been subjected to severe shrinking efforts, a system in package solution with the digital functionality on a separate die may present an appropriate economical solution.
Nevertheless the sheer power consumption of a complex system implementation with increased digital functionality (extended feature sets of mobile electronic devices in high-end products) in a contemporary CMOS process technology can enforce the implementation in a new process technology node for reasons of pure feasibility instead of economical considerations.

The assumptions made in this section about the relative die area consumptions of different functionality and the corresponding shrinking potential agree with estimations made in [23].
Beside the die area costs engineering costs for the implementation of systems in upcoming technology nodes will contribute an increased amount to the total fabrication costs in the future. Especially the physical implementation, relying on extended rule sets with manifold interdependencies, demands immense engineering power.
A last point worth mentioning is that a proceeding miniaturisation and integration lead to a reduction of the die area costs of next generation mobile devices while the back-end-of-line costs for verification and reliability testing are on the rise.

6.4. Conclusion

There is no doubt that the shrink of CMOS process technologies in general will continue in the decade to come. Even today the production of transistor devices with gate lengths $l < 10\,\text{nm}$ is possible in the laboratory. The production of these transistor devices at a large scale is merely concern of time and costs.
We have seen that especially analogue and RF design with conventional devices is about to reach performance limits. Conventional CMOS scaling will introduce hardly any benefit in terms of analogue performance. A lowered amplifying potential, a deteriorated noise performance and a lowered supply voltage challenge the design skills of analogue designers around the globe. Thus post tape-out trimming and calibration options are vital in order to maintain the performance of analogue circuitry. The physical implementation of the designed circuits is also more challenging than ever. The layout complexity and the number of interdependencies steadily grow.
However, innovative implementations of new device types like FinFETs and SONFETS with high-k_{DIEL} gate oxides and metal gates are entering mass production and are expected to surpass the performance of classical MOSFETs. Awareness of the difficulties of modern CMOS design (analogue and digital) has stimulated versatile research activities in the field of CMOS process technology realisation.
Furthermore, a simple cost calculation model has been developed for die area costs. It has been elaborated on the economic shrinking potential of applications consisting of different amounts of analogue and digital functionalities. Additional aspects that affect a calculation of the total cost structure of semiconductor applications have been pointed out.
It is concluded that the CMOS era is not over and Moore's Law will prove true in middle-term.

Theory predicts functional transistors for gate lengths down to $l = 2\,\mathrm{nm}$ [49]. The usage of standard CMOS for analogue and RF design will require new innovative design implementations and technology definitions.

7. Conclusions

This work investigates the impact of recent CMOS process technology shrinks on analogue and RF integrated circuit design. Two LNAs in a wireless communication application serve as an application example for the investigation. The two LNAs have been implemented in a contemporary 65 nm standard CMOS process technology for usage in a low-cost low-power mobile 2.5G GSM receiver front-end. The first LNA serves the GSM low bands GSM850 and GSM900 whereas the second LNA serves the GSM high bands DCS1800 and PCS1900. The underlying LNA architecture, consisting of two cascaded common source differential stages with capacitive feedback, achieves appropriate gain, noise and linearity performance at moderate current consumption while omitting die area consuming integrated inductors.
The LNAs are embedded into the zero-IF receiver front-end of a complete GSM SoC transceiver solution that will enter mass production by the beginning of 2009. Due to the manifold interdependencies and interactions with other receiver front-end components like the quadrature down-conversion mixer, the LNAs have been designed and evaluated in the context of a complete analogue receiver front-end in close cooperation with a business partner from the industrial wireless communication background.
The performance specifications for the receiver front-end and the individual circuit blocks have been derived directly from the official 3GPP GSM system specifications. With the specification requirements in mind it has been elaborated on the choice of a direct-conversion receiver as the most reasonable wireless receiver topology for low-cost mass-production in standard CMOS technologies. The zero-IF receiver has a relative simple topology with a low component count. With the image signal rejection issue inherently solved, the direct-conversion receiver can do without the expensive external image-reject filter that other receiver architectures need. Saving the external filter severely reduces the bill of material for the receiver. Thanks to the benefits of integrated circuit design over a discrete implementation design challenges of a zero-IF receiver like even order distortion can be overcome. Other design challenges i.e. the impact of flicker noise on the receiver sensitivity are countered by an innovative mixer architecture with a passive current-commutating stage and a careful design of the receiver baseband circuit blocks.
The developed GSM transceiver is a transfer and adaptation of a 130 nm GSM chip to the special environment introduced by a 65 nm low-power CMOS process technology. Consequently the impact of CMOS technology scaling on analogue and RF circuit design in terms of amplifying potential, noise and linearity performance has been analysed in a profound model based comparison of transistor unit cells and passive components in a 130 nm and a 65 nm CMOS process technology. It is illustrated that the amplifying potential of transistors g_M/g_{DS} with minimum gate lengths l is severely deteriorated ($g_M/g_{DS} < 10$) when going from $l = 120\,\text{nm}$ to $l = 60\,\text{nm}$ devices. It is in the responsibility of the analogue designer to trade the transit frequency f_T for g_M/g_{DS} by increasing $l > l_{MIN}$ in analogue designs in modern CMOS process technologies. Moreover, an inferior noise performance (drain current noise and flicker noise) is observed for minimum channel length transistor devices. It is also shown that for realistic bias conditions the individual transistor device with $l = 60\,\text{nm}$ exhibits less odd order distortion than with $l = 120\,\text{nm}$.
The analysis of the potential of modern CMOS technologies for analogue circuit design is enriched

by analysis results found in scientific publications on the subject.
The performance of the designed and implemented analogue circuit blocks of the receiver front-end have been evaluated by pre-layout and post-layout circuit simulation results with a special focus on the LNAs. The LNAs achieve satisfactory input return loss $S_{11} < -19\,\text{dB}$, a voltage gain $G_V > 18.3\,\text{dB}$, in-band input referred compression points $CP1i > -22.8\,\text{dBm}$ and input referred third order intercept points $IIP_3 > -14.1\,\text{dBm}$ in all four GSM frequency bands. The noise figures are an excellent $NF < 1.7\,\text{dB}$ for the GSM low bands and $NF < 2.3\,\text{dB}$ for the GSM high bands (including losses of the matching elements). Both fully differential LNA topologies have a moderate current consumption of $I_{DC} < 9.7\,\text{mA}$.
Furthermore, the simulation results for the complete receiver front-end are backed by a series of measurement results of actual testchip samples. During the measurement process design flaws in the power supply concept have become evident. The origins of the design flaws that deteriorate the analogue performance have been identified and have been overcome for future tape-outs. As new measurement results for the improved demonstrators have not been available in time the deteriorating impact of the design flaws has been confirmed by simulations. The general functionality of the receiver front-end has been proven even in the presence of the design flaws. The complete receiver front-end achieves a voltage gain $G_V > 58.3\,\text{dB}$ and a noise figure $NF < 2.4\,\text{dB}$ in the low band mode. In the high band mode $G_V > 54.0\,\text{dB}$ and $NF < 3.1\,\text{dB}$ are achieved. The total input referred third order intercept point is $IIP_3 > -16.3\,\text{dBm}$ (interferer spacing $\Delta f = 800\,\text{kHz}$; cf. GSM intermodulation testcase) while the input referred second order intercept point is $IIP_2 > 42.2\,\text{dBm}$ with the interferer at a frequency offset of $\Delta f = 6\,\text{MHz}$ (cf. GSM AM suppression testcase).
The good accordance between simulation results and measurement results gives rise to superior product-ready performance expectations for future testchips. The overall transfer of the receiver front-end under investigation from a 130 nm CMOS technology to a 65 nm technology is considered successful.
The work is concluded by a summary of prospects of future CMOS process technology nodes with respect to analogue and RF circuit design. After the constraints and limits of conventional deep sub-micron CMOS devices have been pointed out, light is shed on promising approaches to overcome these roadblocks on the ITRS. The ongoing shrink of CMOS process technologies is driven by the semiconductor manufacturers' desire to integrate given electrical functionality on less die area and consequently reduce the production costs in mass production. Thus the economical benefits of future CMOS process technology shrinks are briefly investigated. It is stressed that significant economical benefits result only for the miniaturisation of systems with a large amount of digital functionality of extended feature sets. In addition it is underlined that the engineering efforts and increasing complexity of further technology shrinks will entail more dominant contributions to the overall manufacturing costs.

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A. Appendix

A.1. Abbreviations

Abbreviation	Meaning
2G	Second generation of mobile communication e.g. GSM
2.5G	Generation in between 2G and 3G
3G	Third generation of mobile communication
ac	Alternating current
ADC	Analogue to digital converter
AM	Amplitude modulation
BB	Baseband
BBF	Baseband filter
BiCMOS	Bipolar CMOS process technology
BOM	Bill of materials; component count of a system
BPF	Band-pass filter
CMOS	Complementary metal oxide semiconductor
dc	Direct current
DCS1800	see GSM1800
EDGE	Enhanced Data Rates for GSM Evolution, technically 3G mobile communication standard, but also referred to as 2.75G
EGPRS	Enhanced GPRS, see EDGE
EGSM	part of the GSM900 frequency band, downlink 925-930 MHz
FDMA	Frequency Division Multiple Access
FET	Field Effect Transistors
FM	Frequency modulation
GMSK	Gaussian minimum shift keying, modulation scheme used by GSM
GPRS	General Packet Radio Service, mobile communication standard for data-transfer, 2.5G mobile communication standard
GSM	Global System for Mobile Communications former Groupe Spéciale Mobile, 2G mobile communication standard, voice-only
GSM850	sometimes called GSM800; downlink 869-894 MHz
GSM900	Extended/Primary GSM-Band (E/P-GSM); downlink 925-960 MHz
GSM1800	Digital Cellular System (DCS-Band); downlink 1805-1880 MHz
GSM1900	Personal Communication System (PCS-Band); downlink 1930-1990 MHz
HB	Harmonic balance (algorithm for frequency domain based large signal analysis)
HBLNA	High band LNA
HPP-cap	Horizontal parallel plate capacitor

IC	Integrated circuit
IF	Intermediate frequency
LBLNA	Low band LNA
LNA	Low noise amplifier
LO	Local oscillator
LPF	Low pass filter
MIM-cap	Metal insulator metal capacitor
MOS-cap	MOSFET that is used as a capacitor
MOSFET	Metal oxide semiconductor field effect transistor
MS	Mobile station, mobile handset
NFET	Metal oxide semiconductor field effect transistor with negative travelling charges
opamp	Operational amplifier
PCB	Printed circuit board
PCS1900	see GSM1900
PGSM	Primary GSM, part of the GSM900 band, downlink 935-960 MHz
PFET	Metal oxide semiconductor field effect transistor with positive travelling charges
PSD	Power spectral density
PSK	Phase shift keying, modulation scheme, 8-PSK is used by EDGE
PSS	Periodic steady state (algorithm for time domain based large signal analysis)
QPSK	Quadrature phase shift keying
RF	Radio frequency
$SiGe$	Silicon Germanium process technology
SiO_2	Silicon dioxide
SMD	Surface mounted devices
SoC	System on chip; integration of analogue and digital signal processing on the same die
SONFET	Silicon on nothing FET
TDMA	Time Division Multiple Access
UMTS	Universal Mobile Telecommunications System
VLSI	Very large scale integration
VPP-cap	Vertical parallel plate capacitor

A.2. Symbols

Symbol	Unit	Comment
a_1	1	First coefficient of the non-linear transfer function of a circuit block
a_2	1/V	Second coefficient of the non-linear transfer function of a circuit block
a_3	$1/V^2$	Third coefficient of the non-linear transfer function of a circuit block
a_{DIG}	1	Relative proportion of the die area the digital functionality of a system consumes
a_{ANA}	1	Relative proportion of the die area the analogue functionality of a system consumes
a_{PAD}	1	Relative proportion of the die area the pads of a system implementation consume
A	V	Amplitude of a sine wave input signal
A_G	1	Signal gain (absolute value)
BER	1	Bit error rate
BW	Hz	Signal bandwidth
C	F	Capacitance value
C_{GB}	F	Gate bulk capacitance of a FET
C_{GD}	F	Gate drain capacitance of a FET
C_{GS}	F	Gate source capacitance of a FET
C_{OX}	F/m^2	Gate oxide capacitance per unit area
$(C/I)_{RXO}$	dB	Carrier to interferer ratio at the analogue receiver output
$(C/N)_{RXO}$	dB	Carrier to noise ratio at the analogue receiver output
$(C/(I+N))_{RXO}$	dB	Overall carrier to noise ratio at the analogue receiver output (including intermodulation products and thermal noise)
$CP1$	dBm or dBV	1 dB compression point; $CP1$ can be either input ($CP1i$) or output ($CP1o$) referred
D	m	Distance between windings of a coil
ϵ_{DIEL}	F/m	Dielectric permittivity of a dielectric material
ϵ_{OX}	F/m	Dielectric permittivity of the gate oxide of a transistor
ϵ_{Si}	F/m	Dielectric permittivity of the silicon
E_C	V/m	Critical horizontal electrical field strength of a FET
E_G	CV	Bandgap of silicon at $T = 0\,K$
δ	1	Gate noise coefficient; Correction term; $\delta \approx 2\gamma$
f	Hz	Frequency
f_{3dB}	Hz	3 dB Cut-off frequency
f_C	Hz	Flicker noise corner frequency
f_{DS}	Hz	Frequency spacing between uplink and downlink
f_R	Hz	Resonant frequency

f_T	Hz	Transit frequency; Current gain equal to zero
F	1	Noise factor
FER	1	Frame erasure rate
γ	1	Correction term
γ_S	$\sqrt{V}$	Substrate steering factor
g_{d0}	S	Drain-source transconductance of MOSFET at V_{DS}=0 V
g_{DS}	S	Drain-source transconductance of MOSFET
g_P	1	Linear power gain; Small signal parameter
G_P	dB	Power gain in decibels; Logarithmic representation of g_P
g_V	1	Linear voltage gain; Small signal parameter
G_V	dB	Voltage gain in decibels; Logarithmic representation of g_V
$\overline{i_{nd}^2}$	A^2/Hz	Mean square of the drain current thermal noise density
$\overline{i_{nf}^2}$	A^2/Hz	Mean square of the drain current flicker noise density
$\overline{i_{ng}^2}$	A^2/Hz	Mean square of the induced gate noise density
I_D	A	Drain current of a transistor
I_{DC}	A	*dc* current flow
IIP_n	dBm	Input referred n-th order intercept point
IP_2	dBm	2nd order intercept point
IP_3	dBm	3rd order intercept point
IM_n	dBm	n-th order intermodulation product (at the output of a non-linear circuit block)
$IRNV$	V/$\sqrt{\text{Hz}}$	Input referred noise voltage density
k	1	Die area cost multiplier when going from one technology node to the next
k_{DIEL}	1	Relative dielectric constant of a dielectric
K	C^2/m^2	Empirical constant used to describe $1/f$ noise
λ	1/V	Channel length modulation parameter of a transistor
l	m	Physical length of a device e.g. channel length of a FET
L	H	Inductance of a coil
μ	m^2/(Vs)	"Nominal" charge carrier mobility
μ_{eff}	m^2/(Vs)	Effective charge carrier mobility
m	1	Modulation index
n	1	Device multiplier
N_A	m^{-3}	Acceptor Doping density
N_C	m^{-3}	Density of the allowed states near the edge of the conductance band
NF	dB	Noise figure in dB
N_V	m^{-3}	Density of the allowed states near the edge of the valence band

OIP_2	dBm	Output referred 2nd order intercept point
OIP_3	dBm	Output referred 3rd order intercept point
ϕ_F	V	Fermi-Level
P	dBm	Power level
P_{RS}	dBm	Reference sensitivity level
P_{BL}	dBm	Blocker power at the receiver input
P_{INT}	dBm	Signal power of the interferer at the receiver input
P_{SIG}	dBm	Signal power of the desired signal at the receiver input
r_{GR}	bit/s	Gross bit rate for GSM
r_{NET}	bit/s	Net bit rate for GSM
r_{TDMA}	bit/s	Bit rate within a TDMA time frame of GSM
R	Ω	Ohmic resistance
R_S	Ω	Real part of the source impedance
R_{SX}	Ω	Resistance in the large signal model of a short channel FET
SNR	1	Signal to noise ratio
θ	V^{-1}	Normal-field mobility degradation factor
θ_B	V^{-1}	Voltage degradation factor related to the bulk potential of a FET
θ_G	V^{-1}	Voltage degradation factor related to the gate potential of a FET
t_{TDMA}	s	Time length of one of TDMA time frame
t_{OX}	m	Gate oxide thickness of a transistor
T_{BIT}	s	Bit length or period for GSM
TC	ppm/°C	Temperature Coefficient
q	C	Electronic charge (about $1.6{\cdot}10^{-19}$)
Q	1	Quality factor
V_{DS}	V	Drain source voltage of a transistor
V_{EA}	V	Early voltage of a transistor
V_G	V	Voltage potential of the gate terminal
V_{GS}	V	Gate source voltage of a transistor
V_{OV}	V	Overdrive voltage of a transistor; $V_{OV} = V_{GS} - V_{TH}$
V_{SB}	V	Source bulk voltage of a transistor
V_{TH}	V	Threshold voltage of a transistor
ω_T	s^-1	transit frequency of a FET (zero current gain)
w	m	Physical length of a device e.g. channel width of a FET
X_S	Ω	Imaginary part of the source impedance
$x(t)$	V	Input signal of a circuit block
$y(t)$	V	Output signal of a circuit block
Z_{IN}	Ω	Complex input impedance of a circuit block

A.3. Supplement to: A Model based technology comparison in Section 4.2

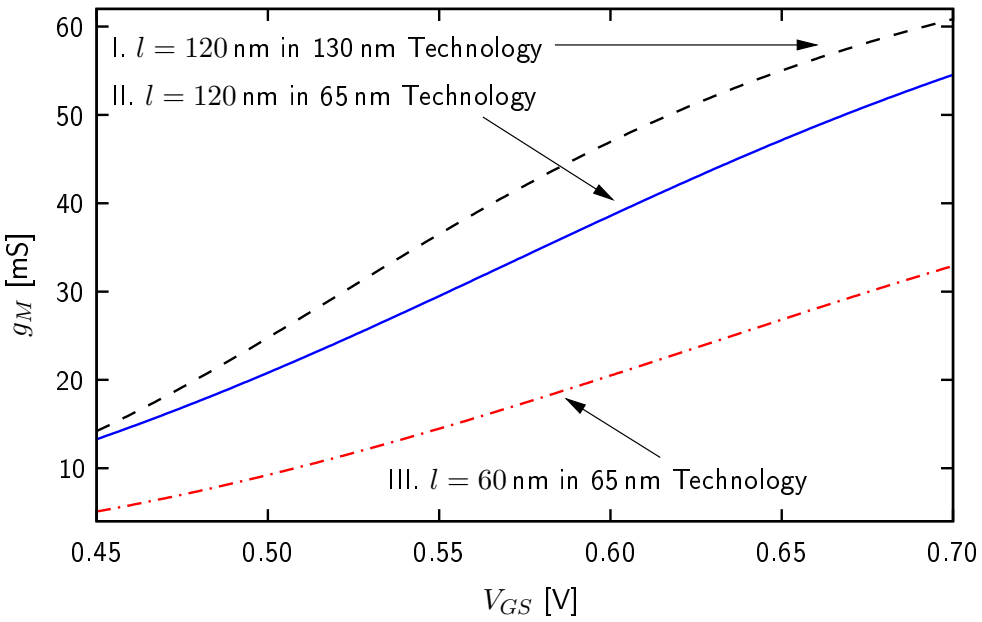


Figure A.1.: Comparison of the transconductance g_M vs. V_{GS} of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

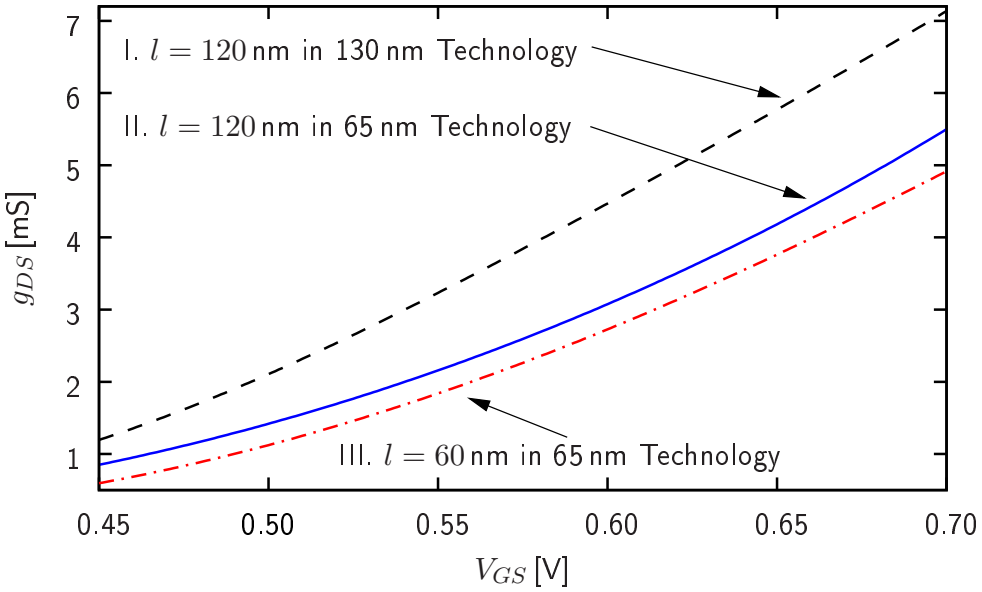


Figure A.2.: Comparison of the output conductance g_{DS} vs. V_{GS} of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

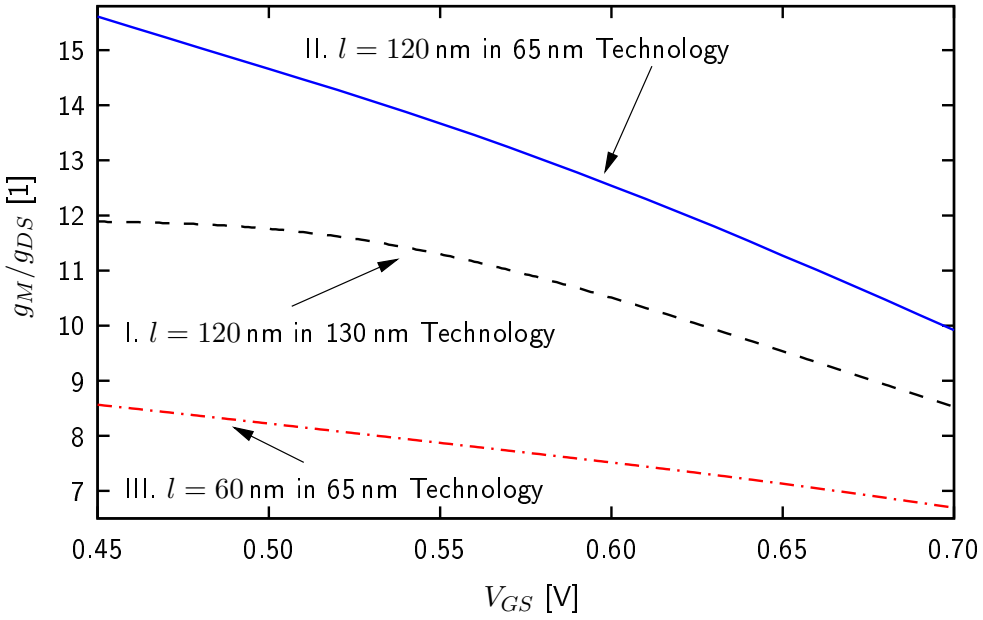


Figure A.3.: Comparison of the intrinsic amplifying potential g_M/g_{DS} vs. V_{GS} of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

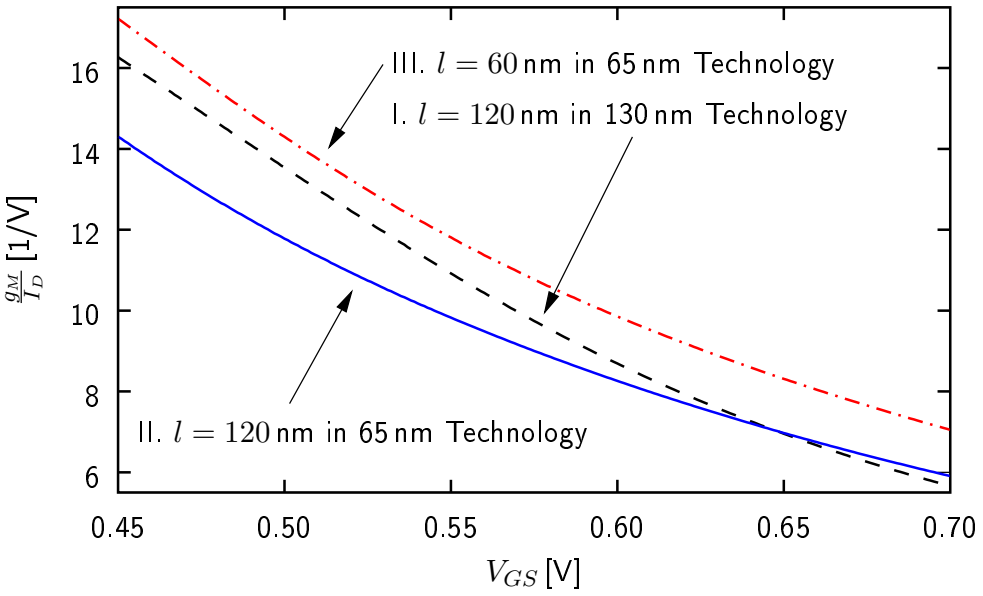


Figure A.4.: Comparison of the transconductance g_M achieved per *dc* current I_D spent vs. V_{GS} of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

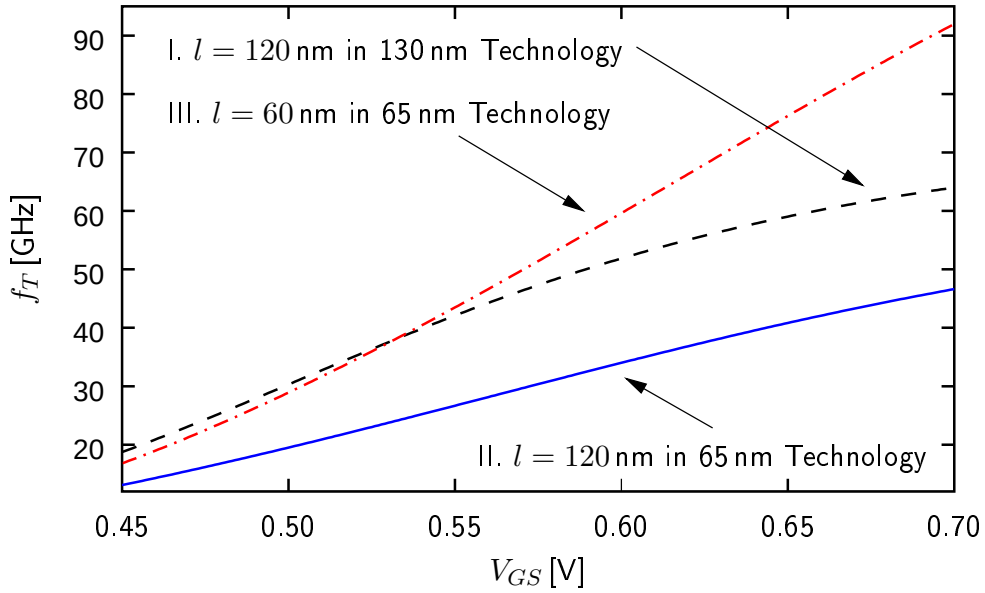


Figure A.5.: Comparison of the calculated transit frequency f_T vs. V_{GS} of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

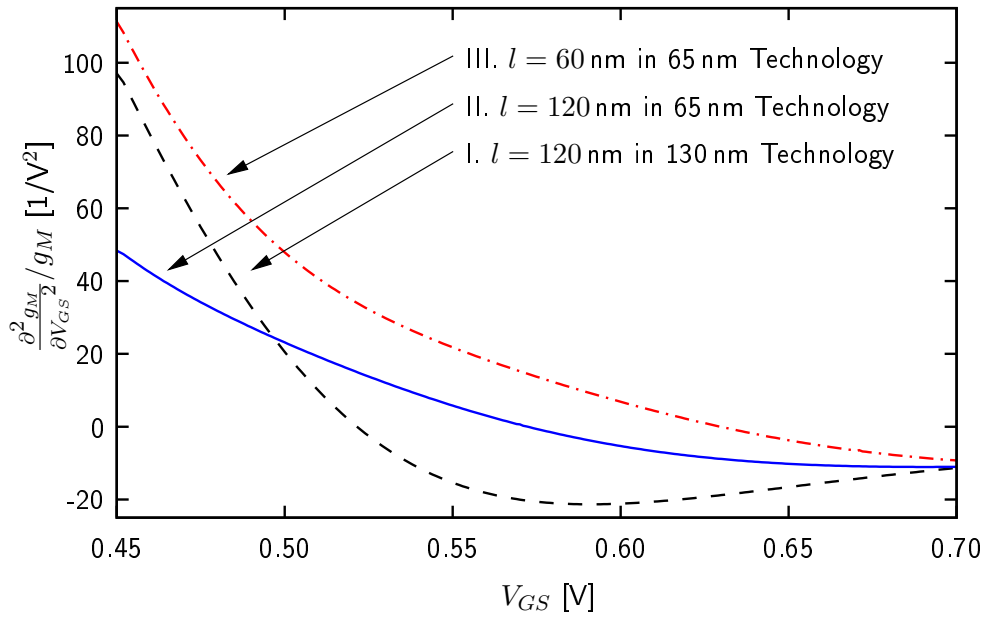
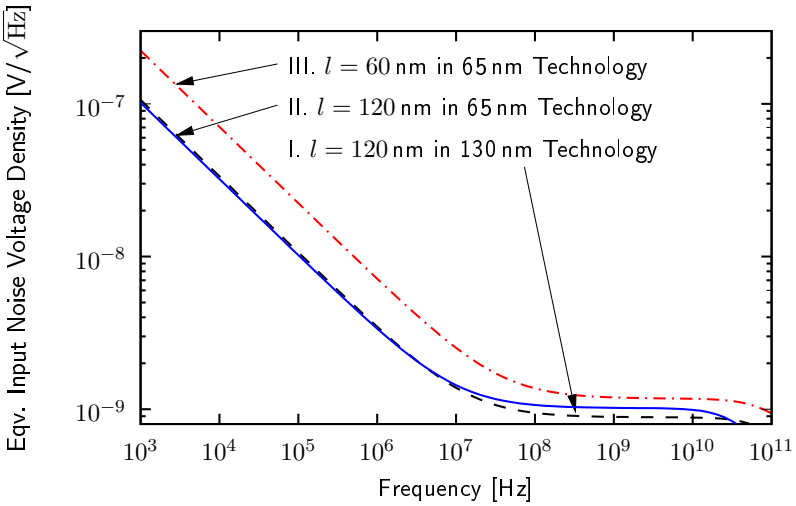


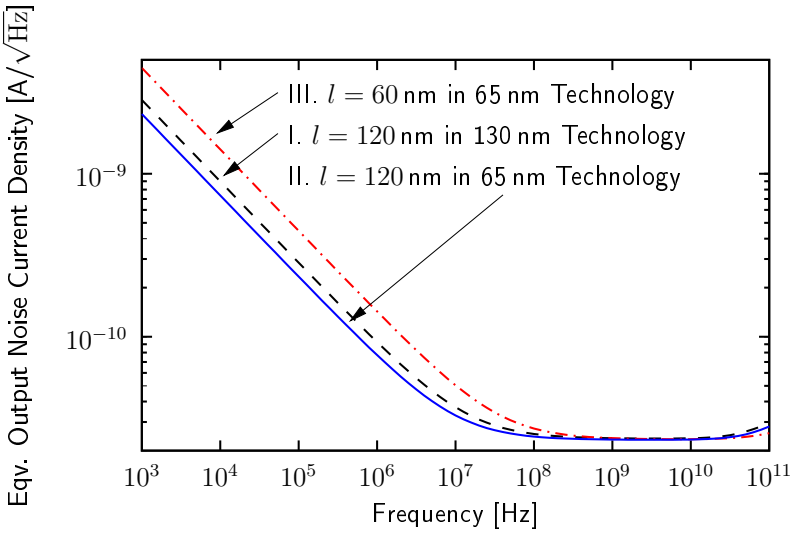
Figure A.6.: Comparison of the ratio of the second derivative of the transconductance to the transconductance $\frac{\partial^2 g_M}{\partial V_{GS}^2}/g_M$ vs. V_{GS} of the three test devices for $V_{DS} = 0.4\,\text{V}$ and $w/l \approx 1000$.

Table A.3.: Operating point parameters for the noise performance comparison of the three test devices in Fig. A.7(a) and Fig. A.7(b) for identical I_D and V_{DS} respectively
.

	I_D [mA]	V_{DS} [V]	V_{OV} [mV]	g_M [mS]
I. $l = 120\,\text{nm}$ in $130\,\text{nm}$	2.08	0.4	56.2	27.0
II. $l = 120\,\text{nm}$ in $65\,\text{nm}$	2.08	0.4	24.5	23.2
III. $l = 60\,\text{nm}$ in $65\,\text{nm}$	2.08	0.4	28.6	20.6



(a) Equivalent input noise voltage density.

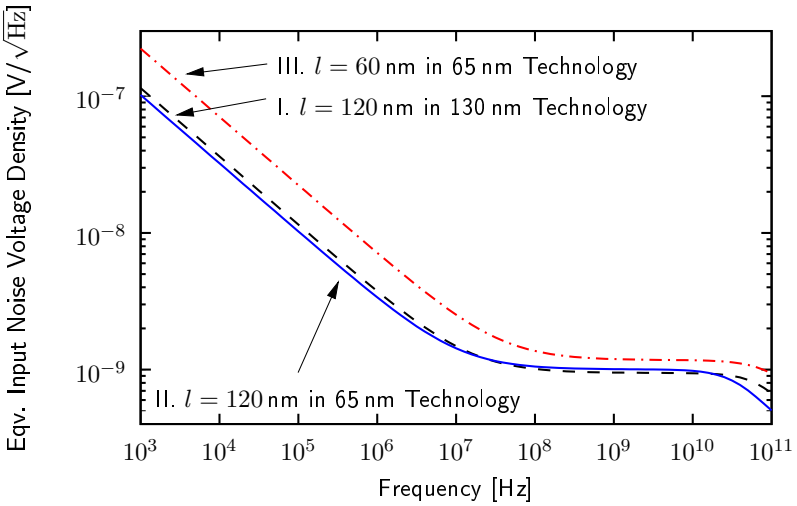


(b) Equivalent output noise current density.

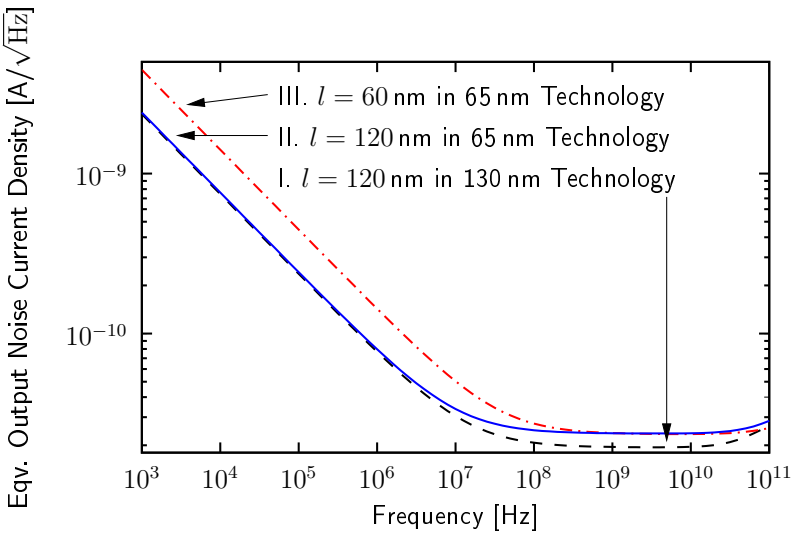
Figure A.7.: Comparison of the noise performance of the three test devices for $V_{DS} = 0.4\,\text{V}$, $w/l \approx 1000$ and $I_D \approx 2.08\,\text{mA}$.

Table A.4.: Operating point parameters for the noise performance comparison of the three test devices in Fig. A.8(a) and Fig. A.8(b) for identical V_{OV} and V_{DS} respectively
.

	I_D [mA]	V_{DS} [V]	V_{OV} [mV]	g_M [mS]
I. $l = 120\,\text{nm}$ in $130\,\text{nm}$	1.42	0.4	28.6	20.7
II. $l = 120\,\text{nm}$ in $65\,\text{nm}$	2.17	0.4	28.6	23.9
III. $l = 60\,\text{nm}$ in $65\,\text{nm}$	2.08	0.4	28.6	20.5



(a) Equivalent input noise voltage density.



(b) Equivalent output noise current density.

Figure A.8.: Comparison noise performance of the three test devices for $V_{DS} = 0.4\,\text{V}$, $w/l \approx 1000$ and $V_{OV} \approx 28.6\,\text{mV}$.

A.4. Supplement to: What to expect from Conventional CMOS Scaling in Section 4.3

This section illustrates the measurement results for CMOS transistor device linearity presented in [55]. Dots indicate measurement results, lines indicate simulation results in Fig. 4.20 and Fig. A.9 to Fig. A.14. For all presented measurements the bias conditions $V_{DS} = 1.5\,\mathrm{V}$ and $V_{SB} = 0\,\mathrm{V}$ are valid.

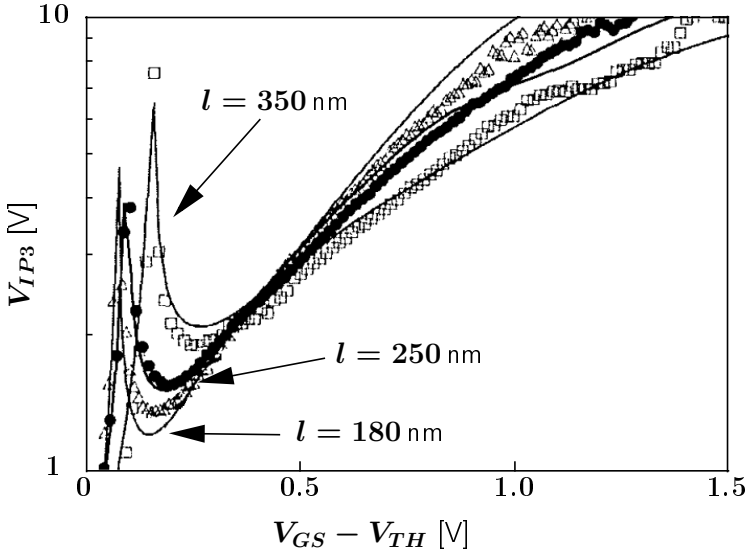


Figure A.9.: Device linearity of NFETs given as V_{IP3} vs. V_{OV} for transistors of different CMOS technologies with different minimum channel lengths l and $w = 10\,\mu\mathrm{m}$ [55].

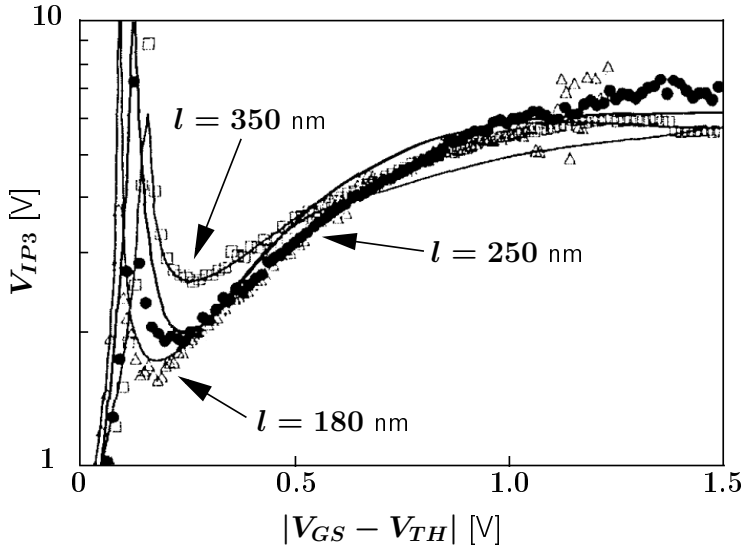


Figure A.10.: Device linearity of PFETs given as V_{IP3} vs. V_{OV} for transistors of different CMOS technologies with different minimum channel lengths l and $w = 10\,\mu$m [55].

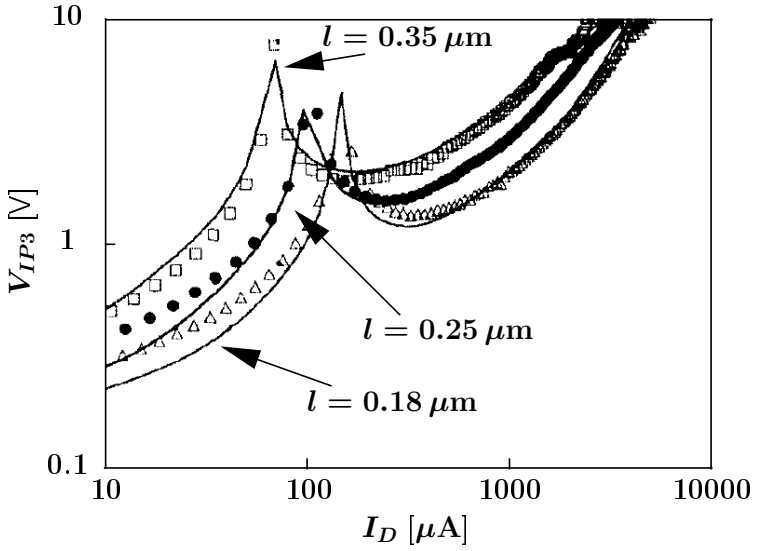


Figure A.11.: Device linearity of NFETs given as V_{IP3} vs. I_D for transistors of different CMOS technologies with different minimum channel lengths l and $w = 10\,\mu$m [55].

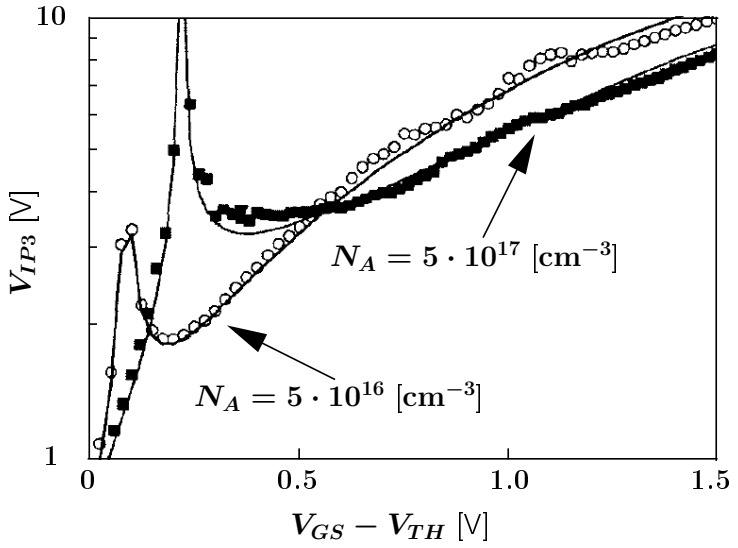


Figure A.12.: Device linearity of NFETs given as V_{IP3} vs. V_{OV} for different levels of substrate doping N_A, $w/l = 10/0.4\,\mu$m and $t_{OX} = 10\,$nm [55].

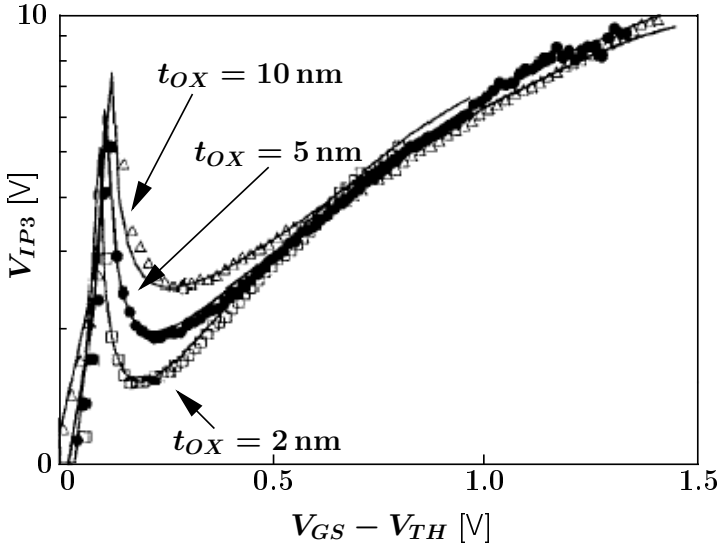


Figure A.13.: Device linearity of NFETs given as V_{IP3} vs. V_{OV} for different oxide thicknesses t_{OX}, $w/l = 10/0.26\,\mu$m and $N_A = 5 \cdot 10^{17}\,$cm^{-3} [55].

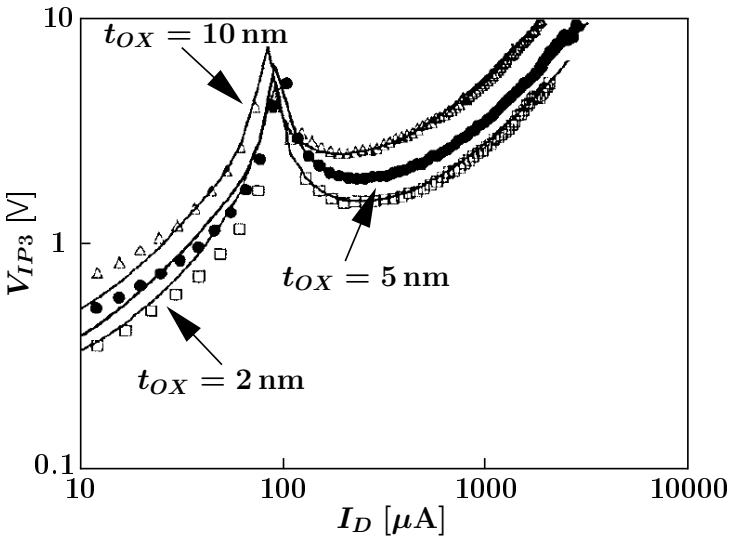


Figure A.14.: Device linearity of NFETs given as V_{IP3} vs. I_D for different oxide thicknesses t_{OX}, $w/l = 10/0.26\,\mu$m and $N_A = 5 \cdot 10^{17}\,\mathrm{cm}^{-3}$ [55].

A.5. Acknowledgements

The author would like to thank the following:

Annika thanks for keeping the boat afloat.

Choco, Ernesto, Gremlin, Naomi, Sugar and Teddy thanks for cheering me up when the sky was full of clouds.

Mom and Dad thanks for filling the cargo bay. Thanks for encouraging me to go on learning.

Thanks to the rest of my family back in my home town for providing a save haven.

Thanks to Prof. Dr.-Ing. S. Heinen for being my captain and supervisor on the long voyage.

Thanks to Prof. Dr.-Ing. J. Oehm for reviewing the ship's log.

Thanks for the support of the crew here at the Chair of Integrated Analogue Circuits. Thanks for endless discussions, thanks for co-reading (especially Toby and Ralf), thanks for barrels of Rum. Special thanks to Soeren for setting the course right and crossing the ocean for the first time.

Thanks to the project partner from industrial background. Thanks for the opportunity to implement, fabricate and measure some actual hardware demonstrators.

Thanks to Fabian for not abandoning your master and being a faithful servant.

Thanks to Jayesh for manning the crow's nest and keeping a look out for me for so long.

Thanks to Ramya. If you ever come across this "X" please contact me.

Thanks to Stanley, Kyle, Kenneth and Eric for entertainment.

Thanks to all who are disappointed by now because I forgot to list their names.

A.6. Curriculum Vitae

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Oct. 1997	-	Mar. 2003	Studies on Electrical Engineering and Information Technology Diploma Thesis "Development, Assembly and Programming of a Measurement Set-up for Electrical Characterisation of Ceramic Thin Films for Resistive, Non-Volatile Memory Application" RWTH Aachen University, Germany
Oct. 2001	-	Jan. 2002	Internship "Modeling of Thin Film BST Capacitors for Design Optimization" in Corporation with Analog Devices, Inc. Raleigh, North Carolina, USA
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		Sep. 2006	Young Engineers Prize Winner "A Multimode Receiver Front-End for Software Defined Radio" at the IEEE European Conference on Wireless Technologies (ECWT) 2006 Manchester, GB