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MASTER'S THESIS

CHANNEL EMULATOR RF MODULE TEST HARDWARE DEVELOPMENT

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ABSTRACT

The constant evolution of wireless communication systems set more and more stringent demands for the equipment used to test these systems. The hardware and software solutions used in the measurement equipment are extremely complex. Because of this complexity, the production process of these equipment needs to include strict testing.

In this thesis, a radio frequency (RF) tester module for production testing of channel emulator RF module is designed. The thesis begins with an introduction to the device that needs to be tested, the channel emulator RF module. This RF module is part of the Keysight Technologies' latest channel emulator model, PROPSIM FS16. The design of this thesis needs to enable the testing of the RF performance of the RF module transceiver.

Benefits of modular production principle are introduced on a general level, and the justification for the production testing is given. It is concluded that testing hardware in a modular testing system is necessary for ensuring the production flow and for ensuring that the final product fulfills the specifications promised to the customer.

Principles of RF testing are considered on a general level and the requirements regarding the designed RF tester module are presented. It is concluded that the RF tester module needs to route instrumentation signalling to the RF module. In addition, RF tester module needs to provide local oscillator signalling as well as DC power to the RF module.

In the design part, the hardware design of the RF tester module printed circuit assembly (PCA) is presented. General RF design principles are discussed and aspects regarding the RF tester module PCA are considered with details. These include isolation, crosstalk and noise.

Chosen components and the designed switching networks are elaborated and justified against the given requirements. It is found out that the instrumentation can be routed via a passive network, but the local oscillator networks need amplification to ensure correct power level. Active network power levels are verified with simulations and found out to be adequate. PCA layout design principles are reviewed on the extent that they play a prominent role in the RF PCA schematic design with the emphasis on the signal grounding issues.

Lastly, the verification and calibration of the designed PCA is described, and the validation of the RF tester module in the complete RF test system is presented. It was found out that some local oscillator signal levels are lower in the final design, than was expected based on the simulations. This caused some delay in the validation phase, by producing false negative test results. After test parameter adjustments, it was found out that the required tests can be executed successfully with the designed RF tester module.

Key words: PROPSIM FS16, RF testing, modular design, RF switching network.

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TIIVISTELMÄ

Langattomien tietoliikennejärjestelmien jatkuva kehitys asettaa aina vain tiukempia vaatimuksia niiden testaamiseen tarkoitetuille laitteille. Näissä mittalaitteissa käytetyt laitteisto- ja ohjelmistoratkaisut ovat äärimmäisen monimutkaisia. Tästä johtuen, nämä laitteet täytyy tuotantovaiheessa testata erittäin tarkasti.

Tässä opinnäytetyössä suunnitellaan RF-testimoduuli kanavaemulaattorin RF-moduulin tuotantotestaukseen. Aluksi esitellään testattava laite, eli kanavaemulaattorin RF-moduuli. Esiteltävä RF-moduuli on Keysight Technologiesin viimeisimmän kanavaemulaattorin PROPSIM FS16 osa. Tässä työssä esiteltävän laitteen tarkoituksena on mahdollistaa RF-moduulin lähetin-vastaanottimen suorituskyvyn testaaminen.

Modulaarisen tuotannon edut esitellään yleisellä tasolla, jonka jälkeen perustelut tuotantotestaukselle esitellään. Päädytään johtopäätökseen, että moduulien testaus tuotannossa on välttämätöntä, jotta tuotannon kulku ja asiakkaalle luvatut spesifikaatiot voidaan varmistaa.

RF-testauksen periaatteet käsitellään yleisellä tasolla, minkä jälkeen esitellään tämän työn RF-testimoduulin vaatimukset. Testimoduulin tulee reitittää testauksessa tarvittava instrumentaatio RF-moduulille. Tämän lisäksi RF-moduuli tarvitsee paikallisoskillaattorisignaalit ja DC tehonsyötön toimiakseen.

Suunnitteluosiossa käydään läpi RF-testimoduulin piirilevysuunnittelu. RF-suunnittelussa huomioon otettavat seikat käsitellään niiltä osin kuin ne ovat relevantteja tässä työssä. Näitä ovat isolaatio, ylikuuluminen ja kohina.

Valitut komponentit ja suunnitellut kytkinverkot esitellään ja perustellaan aiemmin esiteltyihin vaatimuksiin pohjaten. Havaitaan että instrumentaatiolle riittää pasiivinen kykentäverkko, mutta paikallisoskillaattorien verkkoihin tarvitaan vahvistusta. Aktiivisten verkkojen tehotasot testataan simuloinneilla ja havaitaan riittäviksi. Suunnittelun lopuksi käsitellään piirilevyn layout-suunnittelun RF-teknisesti tärkeimmät seikat, merkittävimpänä maadoitus.

Lopuksi työssä suunniteltu RF-testimoduuli verifioidaan ensin piirilevytasolla, kalibroidaan ja validoidaan lopullisessa testijärjestelmässä. Havaitaan että välitaajuusoskillaattoreiden signaali on alhaisempi kuin on arvioitu. Tämä aiheuttaa virheellisiä testituloksia ja viivettä testirajojen asettelussa. Testiparametrien säädön jälkeen voidaan todeta, että työssä suunniteltua RF-testimoduulia voidaan käyttää RF-moduulin testausjärjestelmässä.

Avainsanat: PROPSIM FS16, RF-testaus, modulaarinen suunnittelu, RF kytkinverkko.

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FOREWORD

The objective of this master's thesis was to develop hardware testing module for Keysight Technologies' Propsim channel emulator RF module. The opportunity for this work was offered by Keysight Oulu R&D, so firstly I would like to thank RF designer Mauri Impiö for introduction to channel emulator hardware secrets and for support during this thesis and other work-related matters. Also, cheers to my manager Seppo Salonen for fighting the bureaucracy to keep me on a payroll.

On the academy I would like to present my gratitude to Risto Vuohtoniemi and Juha-Pekka Mäkelä for guidance on this thesis. I have gained a lot of insight on academic writing.

In personal life I thank my parents for the constant support and understanding. Warmest thanks to my wife Petra for assistance in the fight against imposter syndrome, and for all your love.

Oulu, November 27, 2020

Mikko Luostarinen

LIST OF ABBREVIATIONS AND SYMBOLS

3GPP	Third Generation Partnership Project
5G NR	Fifth Generation New Radio
AC	Alternating Current
ADC, A/D	Analog to Digital Converter
AOI	Automated Optical Inspection
BB	Baseband
BOM	Bill of Materials
BS	Base Station
BW	Bandwidth
CW	Continuous Wave
dBm	Decibel relative to one milliwatt power
DC	Direct Current
DSP	Digital Signal Processing
DUT	Device Under Test
EoL	End-of-life
EMC	Electromagnetic Combability
FPGA	Field Programmable Gate Array
GPIB	General Purpose Interface Bus, IEEE 488.2
GUI	Graphical user interface
IC	Integrated Circuit
ICT	In-Circuit Testing
IF	Intermediate Frequency
IFLO	Intermediate Frequency Local Oscillator
JTAG	Joint Test Action Group
LAN	Local Area Network
LDO	Low-dropout regulator
LNA	Low Noise Amplifier
LO	Local Oscillator
LTE	Long Term Evolution
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MIMO	Multiple-Input Multiple-Output
NA	Network Analyzer
PCI	Peripheral Component Interconnect
PCB	Printed Circuit Board
PCA	Printed Circuit Assembly
PDN	Power Distribution Network
PA	Power Amplifier
PLCM	Product Lifecycle Model
PXI	Peripheral Component Interconnect Express
RF	Radio Frequency
RFLO	Radio Frequency Local Oscillator
Rx	Receiver
SA	Signal Analyser
SG	Signal Generator
SMA	Sub-miniature version A
SMP	Sub-miniature push-on

SPDT	Single-Pole Double-Throw
SP4T	Single-Pole Four-Throw
TRx	Transceiver
Tx	Transmitter
UE	Use Equipment
USB	Universal Serial Bus

Z	Impedance
R	Resistance
L	Inductance
C	Capacitance
f	Frequency
ω	Angular Frequency
π	Pi

1 INTRODUCTION

The constantly increasing demand for higher data rate, mobility and number of simultaneous users in contemporary wireless communication systems generate more and more challenges in the implementation of these systems. These demands cause the systems to move towards wider bandwidths for added throughput and to higher frequencies as the lower end of the communication spectra becomes too crowded. Similarly, to increase capacity, coverage and reliability of the communications, the number of antennas used in these systems is growing.

With multiple-input multiple-output (MIMO) schemes, more concatenated channels and higher-level modulations, testing these systems becomes more difficult, yet at the same time more important. With growing complexity, the possibility of a design fault is also increasing. One additional challenge in designing these systems is the time. This stems from the competition and the first-to-market aspect, an obvious contemporary example being the rush to 5G communication systems implementation. On the other hand, the importance of testing naturally stems from the loss of revenue (and market share) due to a faulty or out of specification design.

Testing of these wireless communication systems or parts of them can be done in the field i.e. in the real environment or in a communications laboratory. Between these two, the benefits of laboratory testing are numerous: the measurements are repeatable, cost effective, faster to implement and it is also easier to change the environmental variables to reflect a different scenario. In summary, lab-based testing is much more practical.

The single most significant cause of signal degradation in an end-to-end communication, and therefore the biggest contributor to the previously mentioned challenges in the design of wireless communication system, is the radio channel. These challenges are more and more evident especially when moving to higher (mmWave) frequencies. The degradations imposed on a wireless signal in a radio channel are path loss, fast and slow fading, reflections, scattering, diffraction, noise, delay, interference and Doppler shift. These are elaborated widely in literature; a good summary can be found in [1 p.345-352]. Because of the impracticality of testing in the real environment, as argued above, it is important to test these phenomena in a laboratory.

Generally, testing of a system can be done with a simulator or an emulator, the main difference between these is that the emulator aims to exactly replicate the system that it is emulating. This is done with the combination of hardware and software. Simulator on the other hand is usually a computer program which can be implemented with different programming languages and can be run in many different platforms. Its objective is to model the behaviour of the system it is simulating. Since the difference is not essential in the perspective of this thesis, the terms simulation and emulation are used interchangeably in the following.

Keysight Technologies' Propsim (Propagation simulator) channel emulator is one option to emulate the radio channel phenomena in laboratory conditions. The latest commercial model of the channel emulator at the time of writing this thesis is PROPSIM FS16. It enables users to implement repeatable and realistic channel model-based testing. More information can be found in [2].

Propsim emulator works such that it replaces the radio channel between the antennas in the wireless communication testing. The actual channel emulating is done mathematically in the digital domain with pre-defined emulation software models. Analog radio frequency (RF) parts of the emulator are responsible for signals to be down converted to baseband (BB) on the receiver side and naturally upconverted to RF from the BB on the transmitter side. The working principle of the emulator as well as RF operation are further elaborated in Chapter 2.

1.1 Scope and objective of this thesis

This thesis focuses on the production testing of RF parts of the emulator design. Most of the validation testing concerning communication systems described above applies also to the production testing of the channel emulator. The hardware design follows and tries to keep up with the ever-increasing complexity of modern communication systems. Integrated and simple solutions might not be feasible resulting extremely complicated hardware design taking into consideration the component count, and the performance of individual components or segments. Because of the complexity of the channel emulator, the parts of the system are divided into modules, which perform predefined tasks and interconnect to other modules. In hardware production testing, the modules must be tested as early as possible without the surrounding design to isolate the possible defects for an easier troubleshooting. The defects must be found fast and in a reliable fashion.

In this thesis, the development, verification and validation process of a RF tester module for the production testing of channel emulator RF module is presented. The RF tester module designed in this thesis consists of the printed circuit assembly (PCA) and the mechanical housing and front panel with RF connectors. The development process includes considering of what needs to be tested of the RF module, as well as the circuit design of the RF tester module PCA with the necessary signal routings, connections and level adjustments to comply with the given requirements. The hardware development process and RF requirements are further elaborated in Chapter 4 and the PCA design in Chapter 5.

The verification consists of manual testing of the PCA as far as it is possible on a plain board level. Mechanical assembly and calibrating the RF tester module are also a part of this phase. Lastly, the validation of the RF tester module in the final RF test system is presented. The RF test system consists of the RF tester module attached to a test rack and the needed instrumentation. The validation is done by executing the required tests to the RF module using the system above.

The outline of the rest of this thesis is as follows. In Chapter 2 the channel emulator working principle along with the RF module are elaborated. Chapter 3 presents the production of hardware modules as well as the need for production testing. RF tester module hardware requirements are described in Chapter 4. The actual design of the RF tester module is presented in Chapter 5. Verification and the validation process of the RF tester module are described in Chapter 6. Lastly the conclusions of this thesis are presented in Chapter 7.

2 PROPSIM CHANNEL EMULATOR

In this chapter, the latest model of Keysight's Propsim channel emulator is introduced. The working principle is presented on upper level and the hardware side is elaborated with focus being on the RF hardware operation.

2.1 PROPSIM FS16

The latest commercial model of Propsim channel emulator at the writing of this thesis is PROPSIM FS16. This version does not supersede the previous PROPSIM F64 but is a concurrent model. PROPSIM F64 is equipped with maximum of 64 transceiver (TRx) ports whereas FS16 has 16 bidirectional TRx ports. Both channel emulators are depicted in Figure 1. Detailed specifications for F64 can be found in [3]. FS16 can be thought of a more compact and cost-effective version of F64, although there are design distinctions also. The RF differences are elaborated in the RF module section 2.3.

PROPSIM FS16 can emulate radio channels for example between a mobile user equipment (UE) and a base station (BS). The emulations can be preconfigured 3GPP standard channel models such as 4G long term evolution (LTE) or 5G New Radio (5G NR) scenarios, or more customized test topologies. The emulations typically include radio channel phenomena such as changing multipath propagation environment, pathloss and blocking, Doppler effect caused by mobility as well as noise and interference caused by other users. FS16 can be used for 8x8 bidirectional MIMO testing. The system is scalable so that more massive MIMO testing is possible with additional units and configuration. Detailed capabilities and features for FS16 can be found in [2].

Channel emulator is used by connecting the test equipment to front panel connectors and running the emulations via a graphical user interface (GUI) operating in Windows environment. The emulations can be ready to run test scenarios, like stated above, or they can be customized by user with Propsim modelling tools via GUI. Propsim includes software tools for user to create channel models and emulations. Since the emulations are file-based, they are fully repeatable and easily modified and configured. Test signals used in emulations are real world signals generated by the external test equipment.

Figure 1. PROPSIM F64 and PROPSIM FS16.

2.2 Hardware operation

As in most modern telecommunication systems, the main signal processing in Propsim is done in the digital domain. The digital signal processing (DSP) takes place in field programmable gate arrays (FPGAs) controlled by test controller software. On the other hand, the signals in a radio channel are high frequency RF signals, so they need to be converted into BB for the emulations. Naturally the BB signals need to be upconverted back to RF after the emulations. In Propsim, this is done with a transceiver in the RF module.

The computational power of Propsim FPGAs needs to be huge since the emulations are real-time and can be relatively massive. The need for computational power and large number of separate channels results in a complex and power-hungry hardware. All FPGAs and RF parts naturally need individual power supply and cooling systems. This leads to a modular hardware solution that consists of a frame with individual control unit and separate channel units which are responsible for the abovementioned RF to BB transition and channel emulation computing. Channel units themselves consist of separate modules, like the earlier mentioned RF module, which is elaborated next.

2.3 RF module operational description

The RF module of Propsim channel emulator consists of a RF signal router and transceivers with input-output connectors located in the emulator front panel. Connectors have changed from N-connectors in F64 to sub miniature version A (SMA) connectors in FS16. In addition, FS16 has the possibility to use unidirectional port configuration, so it can operate with 16 receiver and 16 transmitter ports.

The maximum frequency range of FS16 is from 3 MHz to 6 GHz, which differs from the F64's starting frequency of 450 MHz. Higher frequency limit can be extended to 43.5 GHz with

additional mmWave TRx unit. Bandwidth (BW) of a single FS16 channel is 160 MHz. The RF router enables combining up to eight channels, resulting in BW up to 1200 MHz, depending on the software configuration. Peak input power level above 100 MHz is +35 dBm and +15 dBm below 100 MHz. Output power level is +5 dBm peak with the bidirectional connector and +15 dBm peak when using the unidirectional transmitter connector.

On the receiver side, the input signal is a radio frequency signal from the front panel connector. The output signal from the RF module needs to be a low frequency signal suitable for analog to digital conversion (ADC) for DSP. This is achieved with a superheterodyne TRx. The TRx downconverts the incoming signals to BB in a two-step conversion using locally generated continuous wave (CW) signals. These are called radio frequency local oscillator (RFLO) and intermediate local oscillator (IFLO) signals, and they are generated in a separate module. Their usage is elaborated in RF tester module hardware requirements chapter. On the transmitter side the RF module is naturally responsible for upconverting the low frequency signal from baseband to a radio frequency signal. A general superheterodyne TRx RF parts can be seen in Figure 2.

Regarding component count, the TRx of the RF module is much more complicated than the general construction depicted in Figure 2. For example, the fading part of the channel emulation is done partially in the digital domain and partially at the RF module, so the TRx is responsible for the separation of different frequency band signals and level adjustment of signals. These are done with multiple filter banks, switches, amplifiers and attenuators. The detailed RF design is out of the scope of this thesis.

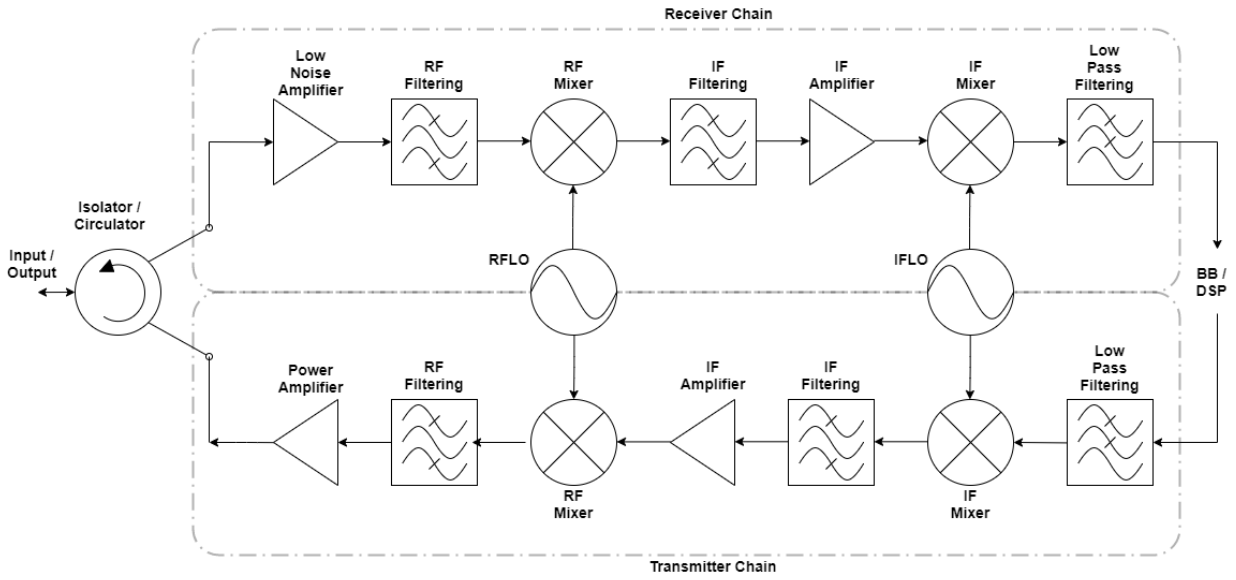

Figure 2. Superheterodyne transceiver RF parts.

3 PRODUCTION TESTING

In this chapter, the production flow of Propsim hardware is presented. Modular hardware manufacturing concept is elaborated, and the characteristics of manufacturing high-end test equipment are contemplated. Also, the need for modular testing is justified, focus being on the RF module testing.

3.1 Propsim production implementation

The production of the Propsim hardware is started by manufacturing the circuit boards by subcontractors. This includes lamination of the printed circuit boards (PCBs) and populating them with components, resulting in printed circuit assemblies (PCAs). Some testing is done to the PCAs already by the subcontractor. PCA testing might include flying probe testing, automated optical inspection (AOI), in-circuit testing (ICT) and DC tests. These are done mainly for quality assurance and early discovering of critical assembly faults such as short circuits or missing components and are elaborated for example in [4].

In the Propsim production, the PCAs are assembled into their corresponding mechanics resulting in a structure called a module. For example, the RF module consists of the transceiver, signal router and the mechanics responsible of connector housing, cable routing and shielding of the PCA signal traces. Correct mechanical assembly is especially important for the isolation and crosstalk reduction of RF signals.

After the individual modules are assembled, each one of them goes through a module test. After testing, the passed modules are combined, constituting a channel module. Channel modules are then assembled into a channel emulator with the hardware configuration according to customer request. One of the advantages of a modular construction is this ability to customize the final hardware configuration. After final testing is done to a complete emulator, the product is ready for shipping. Propsim production flow is illustrated in Figure 3. The most relevant phase regarding this thesis is the highlighted RF module test.

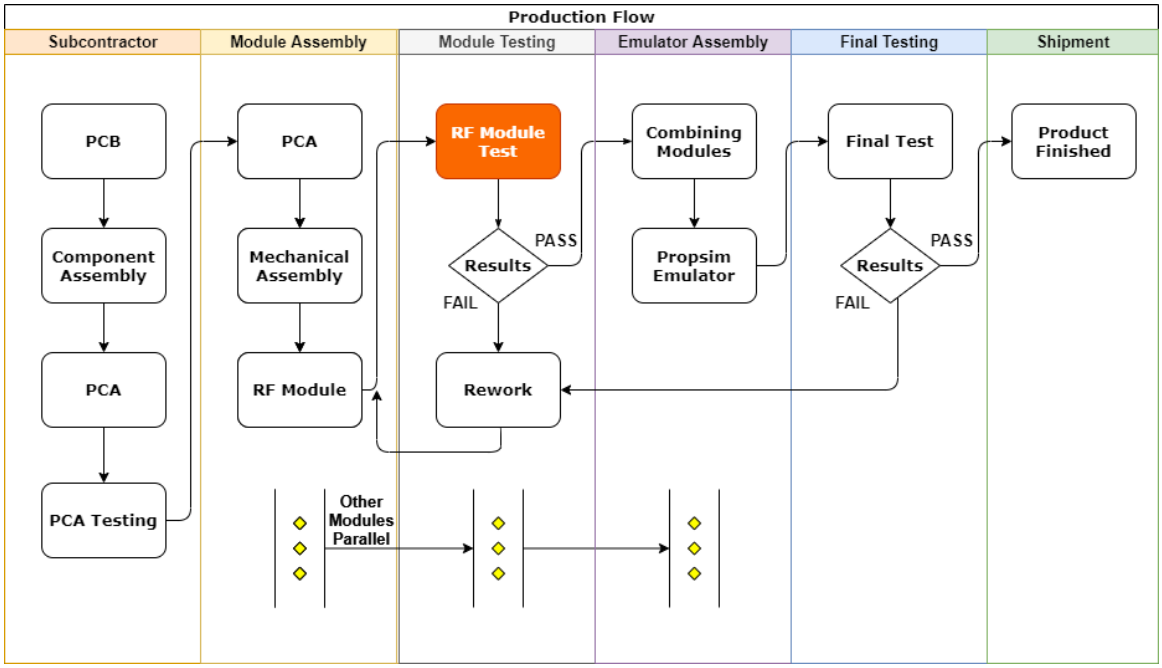

Figure 3. Propsim emulator production flow.

The exact amount of any Propsim model produced are company secrets, but it can be safely said that Propsim channel emulator manufacturing is not high-volume production in a traditional sense. Instead it is production of a high-end testing platform. This brings along some difficulties in both the production of the modules as well as testing them.

Imperative characteristic of any measurement equipment is that it outperforms the system that it is used to test. Consequently, the hardware design of the modules is relatively complicated, and the performance of the individual subsystems needs to be on a high level. The complexity of the design means that there are many PCAs with multitude of board-to-board interconnections between them. The assembly needs to be very accurate, since there are many potential places for a human error.

The high level of performance and the need for the subsystems to operate similarly means that the subsystems must be calibrated, and the final testing is quite rigorous. These are both very time-consuming phases, and any defects discovered in these phases bring on unacceptable delays in the production. Therefore, all the individual modules need to be tested, albeit it being laborious. It can be argued that it is much more costly to find out a possible defect in the later phases, let alone at the customer site.

As stated before, there are sixteen SMA connectors in one channel model and in a cabled test system the amount of RF cables and surrounding testing equipment such as analysers and relay boxes can be numerous. All these need to be properly specified, operational (for example no defective cabling) and within their calibration period so that the quality of the production process is not compromised.

3.2 RF module testing

The module testing is justified on research and development (R&D) side by the need to verify that the product functions according to the design specifications. On the production side it is justified by the fact that there are thousands of components and complicated signal routings in the final product which needs proper verification. The operational specifications promised to the customers are such that the individual components and sub-systems on hardware side must work exactly at the specified level. All parts affect the final performance and the hardware must not add uncertainties in the emulations.

In addition to possible component defects, with more and more complicated systems, the probability of a human error also increases. The faults, whether they stem from subcontractor or production phase, must be caught as early as possible to minimize rework time.

On the other hand, testing of individual PCAs thoroughly is too difficult and time consuming. Also, the interconnections between different PCAs or sub-systems would be impossible to test and some PCAs do not even function without external signals.

Therefore, testing on a module level in the production phase is the best compromise. As can be deduced from the previous chapter, the module testing is not a mass production testing, but more of a functionality test for finding out of specification shortcomings before the rest of the production phases. Another advantage of modular construction is the ability to test different modules in parallel, as seen in Figure 3. It is also easy to replace a faulty module to a tested and approved one.

The testing must be implemented semi-automatically with as simple set up as is possible. Obviously, since the modules are designed to work with interconnections to each other, this test system needs surrounding hardware such as signal generators and analysers. This sums up to a hardware test environment which is software controlled and has pass/fail tests and result

collection. The design and implementation of a module test environment is a task for the R&D; the requirements and hardware design of RF module test system are further elaborated in the following chapters.

4 HARDWARE REQUIREMENTS OF RF TESTER MODULE

In this chapter, the requirements of the RF tester module are elaborated. Firstly, a general RF test system development is considered. Secondly, Keysight hardware development process is presented, leading to the functional description of the RF tester module of this thesis. Lastly, more detailed requirements for the RF test system consisting of the RF tester module of this thesis are given. The actual design process of the RF tester module PCA is presented in Chapter 5.

4.1 General RF test system

On a general level, testing is needed for finding the weaknesses of a device before the customers do, as stated in [5 p.2]. This is true with RF testing also. The weaknesses or out of specification operation might stem from hardware defect or a human error. In any case they need to be addressed as early as possible. This calls for a test system that can carry out this task in a reasonable time and on an acceptable level.

RF test system development is a task of choosing right subsystems and interconnecting them with the system controller. These subsystems are the instrumentation, computing, switching and power sourcing subsystems. In RF test system, the instrumentation consists of the measuring and stimulus equipment or devices, such as analysers and generators. Equipment and devices might be used from this on when referring to the instrumentation.

Computing means the test system software control, for example test script drive and result collecting. Switching system means the relays that are used to route signals between the device under test (DUT) and the test system instrumentation. The power supply is naturally the part of the system that is responsible for powering the DUT and possibly other equipment. A generic RF test system is depicted in Figure 4. [6 p.2-3]

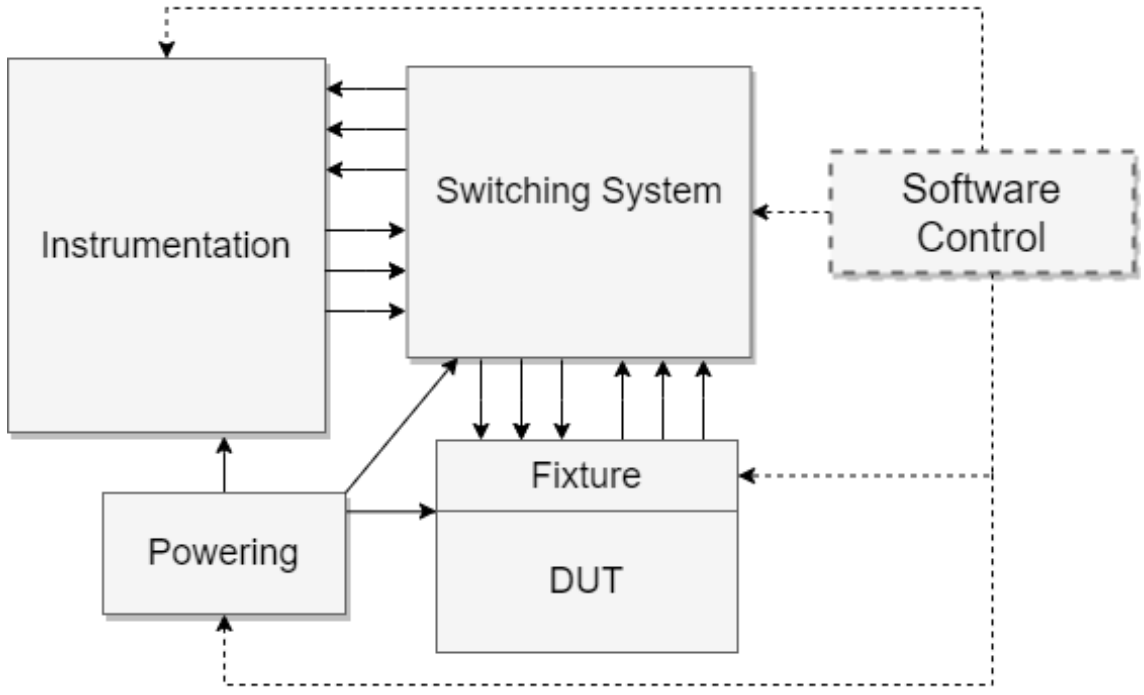

Figure 4. A generic RF test system.

A test fixture is a connection that provides the electrical and mechanical interfaces between the test system and the DUT. In a RF test system, the fixture usually houses the RF connectors for the instrumentation cabling. It may also provide power for the DUT. In Figure 4 the fixture is depicted between the DUT and the switching system. The fixture might be for example an accessory, where the DUT is placed and then the cabling is connected manually. [7 p.38.10-38.11]

The RF tester module presented in this this thesis can be considered a fixture. It consists of a PCA, mechanical housing for the PCA, and a front panel for RF connectors. These connectors are SMA for RF module connections and N-connectors for instrumentation cabling. RF tester module as a fixture with the RF module attached on top is shown in Figure 5.

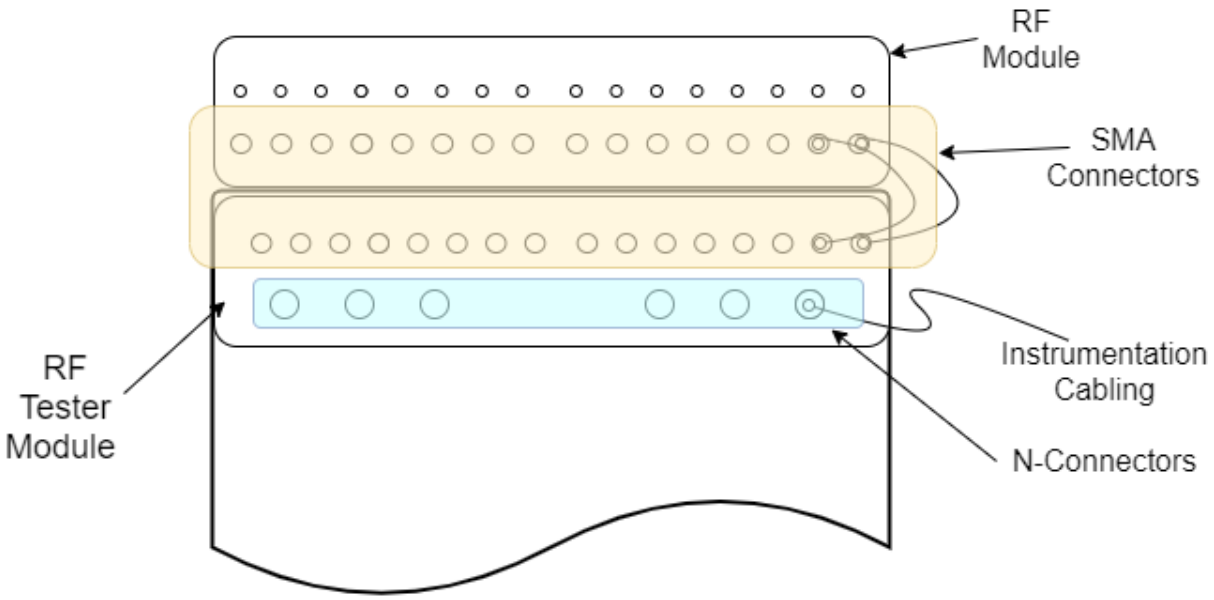

Figure 5. RF tester module with RF module on top.

Things to consider at the beginning of test system development are for example the directions of the signals, needed frequencies and needed RF power levels. It is also necessary to consider how the equipment is controlled, i.e. which instrumentation interface is used. Two most popular interfaces are general purpose interface bus (GPIB) and local area network (LAN). Another consideration is whether benchtop devices are suitable or if peripheral component interconnect express (PXI) instrumentation is needed. Of these two, the former have traditionally been used in cases where higher RF performance is needed, and the latter in modular, fully automated test systems where the space taken by the instrumentation is a factor [6 p.3].

In RF test system, the devices that take a signal as an input are signal analysers and power meters and devices that output signals are signal generators. Devices that both input and output signals are network analysers and vector signal transceivers, the latter being a combination of signal analyser and generator, one example shown in [8]. This list is in no means a comprehensive list of devices used in modern RF test systems but serves as an overview of necessary equipment in RF testing. In the test system of this thesis, benchtop equipment with LAN connection are used. [9 p.3-4]

4.2 Hardware development process

Normally Keysight hardware development process would follow a so-called product lifecycle management (PLCM) model, which is a typical version of such a model for a hardware and software company of this size. This PLCM includes such entities as development and shipping milestones and end-of-life (EoL) phase which completes the product lifecycle.

RF tester module design on the other hand differs substantially from this model. Firstly, the module is not intended for a customer (i.e. as a new sales item), but for the use of company's own production team. This means that PLCM phases such as initial production build with quality assurance and possible tear down processes are not relevant here. Secondly, the volumes of tester modules are very low. Therefore the design must be as simple and as robust as is possible with the given requirements, and the prototype testing together with validation are done in R&D. Lastly, phases such as type approval or electrical safety tests, which are very important in a customer product development, are not carried out here. Instead these are included in the validation phase.

Some similarities to a customer product design obviously exist. Most relevant of these phases regarding this thesis are the technical requirements definition, the hardware design phase which is presented in Chapter 5 and the validation phase which is discussed in Chapter 6. A simplified adaptation of Keysight's development process for RF tester module of this thesis can be seen in Figure 6.

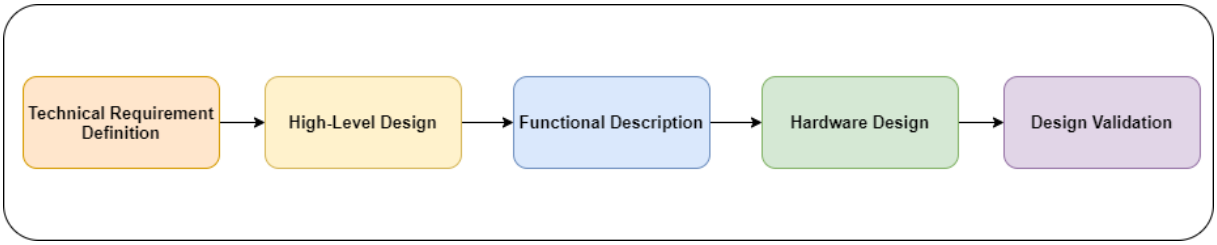

Figure 6. Hardware development process of RF tester module.

Technical requirements definition leads to a high-level design which outputs functional description and hardware requirements. Technical requirement means what needs to be tested and why. The RF module is presented in previous sections, but to summarise: Multichannel RF module signal chain needs to be tested. In the rest of this chapter, DUT refers to the RF module of the Propsim channel emulator. The reasoning for testing is justified in the previous chapters and the summary is: The performance of a complicated high-end measuring equipment needs to be verified.

This leads to a high-level design of the RF tester module: Router module for interconnecting signalling to DUT and measuring equipment for testing. Functional description is as follows: RF tester module routes local oscillator signals from the signal generators and provides DC power for the DUT to operate. In addition, the tester module is responsible for connecting input and output signals between the DUT and instrumentation as well as adjusting the signalling to a specified level if needed.

4.3 Functional description of the RF tester module

On a functional level, the RF tester module needs to provide the DUT all the needed signals for its operation. In addition, the tester module needs to route the test signals to the DUT as well as the output of the DUT to the measurement environment i.e. the instrumentation. The RF module test system with the RF module attached is shown in Figure 7.

The test system consists of a special test rack for production testing purposes, including a fixture, which in this case is the RF tester module. The cabinet housing and powering the test equipment is a standard instrumentation cabinet. Connections between DUT, fixture and instrumentation are coaxial cables. Controlling PC is connected to the test rack via a LAN connection. Note that all the coaxial cabling is not depicted.

In Propsim RF module testing, the needed equipment consists of a network analyser (NA), a spectrum analyser (SA) and three signal generators (SGs). The network analyser is used in whole RF chain amplitude and delay measurements and spectrum analyser in Tx output level measurements, as well as in spurious measurement. Two SGs are for the LO signals (RFLO and IFLO) and one for generating a RF test signal for the DUT receivers.

All of these are benchtop devices, mainly because they are readily available. New instrumentation is a considerable investment and while the harmonizing of measurement equipment is a pertinent issue on a company level, it is outside of the scope of this thesis.

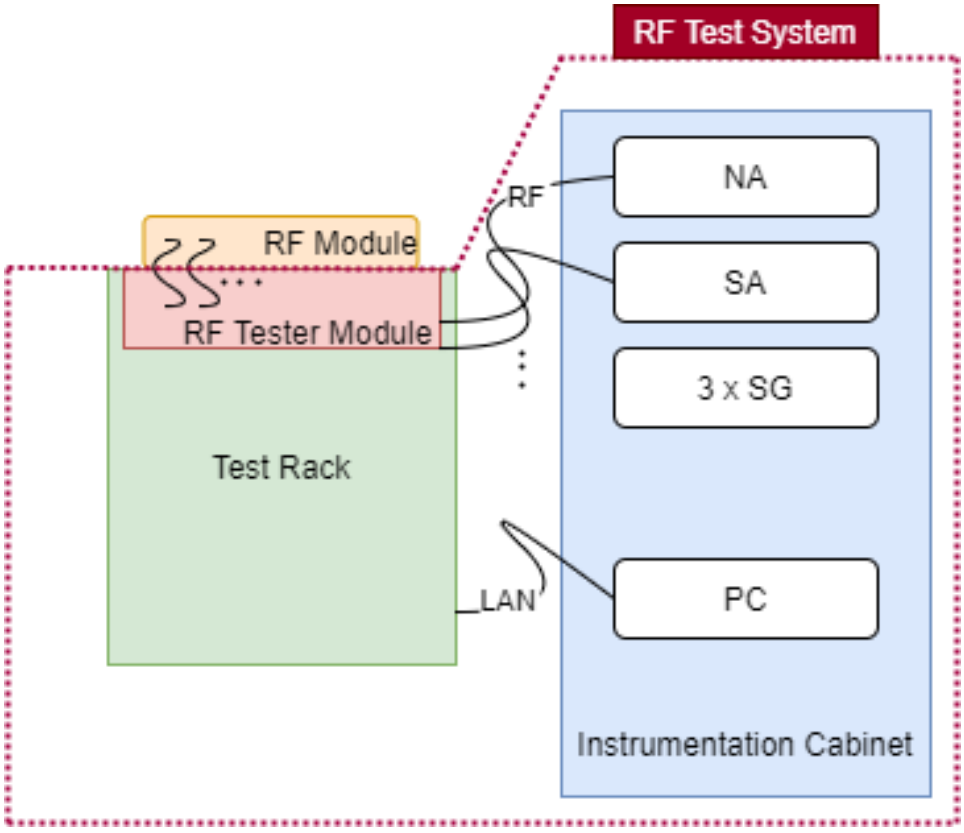

Figure 7. RF module test system.

4.4 RF requirements

Next, the RF requirements for the RF test system and further the RF tester module of this thesis are presented. Key requirements for any RF test system include:

- Signal power levels: devices' input dynamics need to be good enough so that all the signals of interest can be detected, or the output level high enough for the needed operation.
- Frequency range: what are the lowest and highest signal frequencies that need to be measured.
- Impedance matching: all the equipment need to have same impedances to mitigate measurement errors due to reflections.
- Isolation and crosstalk: how much of the signal is coupled across open circuit and between separate signal routes, respectively.
- Resolution and accuracy: for example, how close can the measured signals be in spectrum for them to be detectable or how much is there error in a power level measurement.

These are partially adapted from [9 p.4]. Relevant to the RF test system and RF tester module of this thesis are the following: suitable frequency range, good enough dynamics and LAN controllability. The instrumentation used is characterised for 50 Ω impedance and this needs to be taken care of in the tester module design. Isolation and crosstalk are issues that also need to be addressed in the design phase.

On the signal generation side, the RF tester module needs to route IFLO and RFLO continuous wave (CW) signals needed in the RF module transceiver mixing stages. The former can be done with frequency range of 1 GHz to 6 GHz and the latter in the range of 5 GHz to 9 GHz. Nominal power levels for these signals at DUT are +20 dBm and +3 dBm respectively. In addition, the tester module needs to provide a route for Rx test signal (also CW) in the range of 3 MHz to 6 GHz.

On the analyser side, the RF tester module needs to route Tx signal to a SA in the range of 3 MHz to 6 GHz and connect SA for spurious measurements and step attenuator test. Frequency range for spurious measurements is 5 MHz to 6 GHz and the needed dynamic range is at least -70 dBm to 10 dBm. The step attenuator test is done driving the attenuator with 0.5 dB steps from zero attenuation to full attenuation on two different CWs. The same frequency range and dynamics as in the spurious test suffice.

It is also required to connect Rx and Tx chains to NA for frequency response flatness and amplitude (gain) measurements. The frequency range needed is 10 MHz to 6 GHz and nominal signal level at DUT is -25 dBm. Additionally, a group delay measurement done with NA is a required test. Group delay is a measure of the signals travelling time through the DUT versus frequency and can be measured with same specifications as the flatness and amplitude mentioned before. A whole frequency range measurement in the range of 10 MHz to 6 GHz is also needed for each Rx and Tx chain.

Response flatness and amplitude measurements are not done extensively to whole frequency range, but to selected spot frequencies. The BW of single PROPSIM FS16 channel was mentioned to be 160 MHz, and this is naturally the BW used in flatness and amplitude measurements.

The abovementioned requirements can be achieved with a wide variety of equipment. Requirements and one suitable instrumentation setup are listed in Table 1. All instruments are

from Keysight's selection, for obvious reasons. Resolution and accuracy of these modern test equipment is more than adequate for the RF test system of this thesis.

Table 1. RF module test system requirements

Instrument	**Frequency Range Needed**	**Dynamic Range at Least**	**Power Level at DUT**	**Example Model**
SA	3 MHz to 6 GHz	-70 dBm to +10 dBm	N/A	UXA N9040B
NA	10 MHz to 6 GHz	-30 dBm to + 10 dBm	-25 dBm	PNA-X N5247A
SG1 (RFLO)	5 GHz to 9 GHz	TM	+3 dBm	PSG E8257D
SG2 (IFLO)	1 GHz to 6 GHz	TM	+20 dBm	PSG E8257D
SG3 RF Test Signal	3 MHz to 6 GHz	TM	0 dBm	PSG E8257D

In the Table 1, cells marked TM mean that there will be some amount of loss in the RF tester module route, which needs to be taken care of with amplification, so that the SG signals to DUT are at nominal level. For example: if SG max output power at 4 GHz is +14 dBm, needed IFLO level is +20 dBm and the losses through the tester module might be on the scale of 10 dB, at least 16 dB amplification is needed. This is considered further in Chapter 5.

Naturally, a frequency reference signal is needed for the instrumentation. A 10 MHz reference signal for all the devices is provided by test rack reference source (test rack in Figure 7). The instruments are connected in a daisy chain configuration, so every device in the chain needs to have external reference selected. All the instrumentation needs to be within their calibration cycle i.e. calibrated according to manufacturers' calibration procedures which are not elaborated here. The cabling between DUT, equipment and RF tester module needs to be specified for used frequencies.

5 RF TESTER MODULE HARDWARE DESIGN

In this chapter, the designed RF tester module PCA is presented. Firstly, general RF design principles are discussed. Then the parts selection process is elaborated. Secondly the signal switching network is covered. This includes the routings of IFLO, RFLO and instrumentation signalling with switches, splitters and amplifiers. The needed amplification is verified with simulations of the relevant routes. These are described in the RF switching network section. Thirdly, the power tree of the RF tester module is presented. Then a brief description of the needed field programmable gate array (FPGA) and its operation is given, and lastly the relevant parts of PCA layout design are introduced.

Verification of RF tester module PCA and validation of the whole RF test system is done after the module test design is complete. These are described in Chapter 6.

Ideally, a test system would be developed concurrently with the design that it is used to test, so that it would be feasible to verify the correct working of the DUT as early as possible. At least some kind of testing possibility should be in existence for the prototype, or the first round PCAs of the DUT design.

The development of a module test system is a multi-discipline effort. It involves software design (test software script), mechanical design (the housing of the tester module PCA), FPGA design (implementing the bitstream) and schematic design. The last one means the RF tester module PCA responsible of housing the components, connectors and power lines as well as control circuitry. Design decisions must be judged also based on how they impact the other phases of the process. For example, additional switches need additional control lines, and the chosen FPGA needs to have capability to support these. The concurrent development flow is presented in Figure 8.

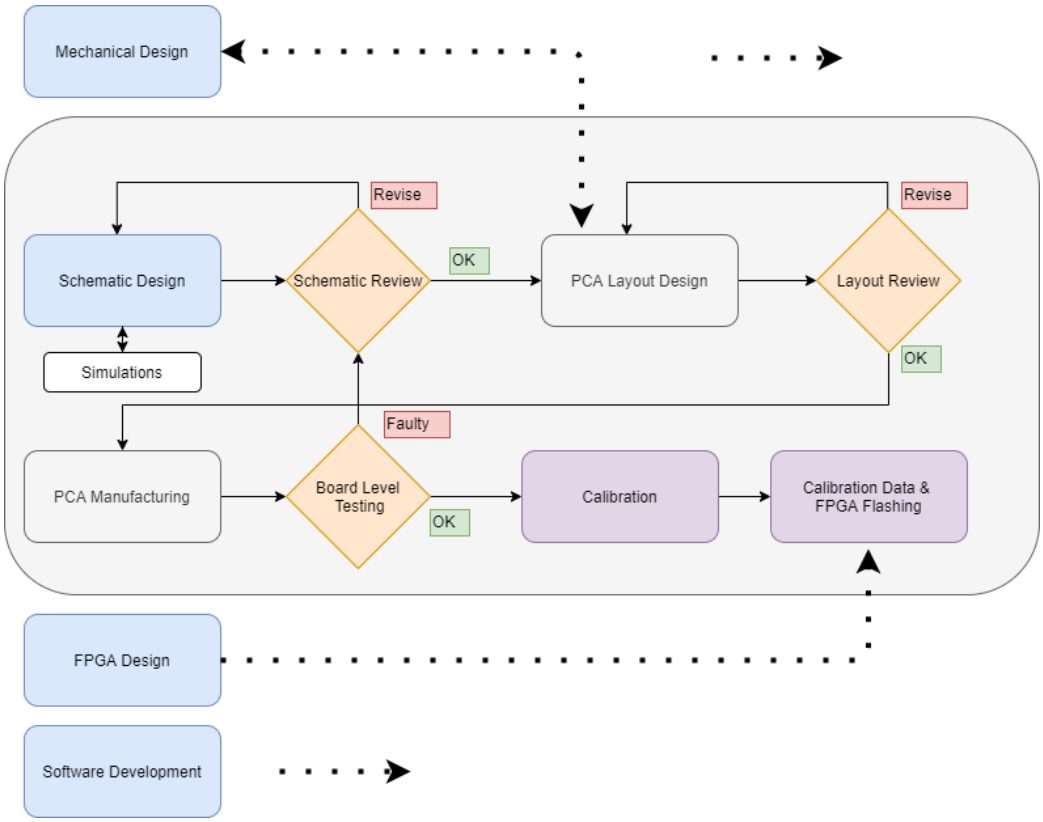

Figure 8. Concurrent development flow.

In practice, depending of company resources and DUT complexity, a lot of the above is done after the DUT design is complete. This stems from the fact that changes in the DUT might demand changes in the tester module also. For example, if a RF connector changes place in the DUT PCA layout, it requires a change in the DUT mechanics, which in turn forces a chance in the tester module layout and/or mechanics. Therefore, the hardware design is at best an iterative process, where advances in one area lead to progress in other areas.

Next, some characteristics of RF design on a general level are presented. These characteristics are discussed in relation to the RF tester module design, where applicable. In RF PCA design, it is beneficial to partition the board in different sections based on their functionality. Partitioning means that for example power supply related components are separated on one part of the board, FPGA and its peripheral components on one area and high frequency synthesizing components, such as oscillators on their own isolated part. RF connectors used in high frequency signal routing should be kept away from digital signalling. One example of functional partitioning is presented in Figure 9. There the low-level analog partition means DC power supply components, digital partition includes the FPGA chip and its peripheral components, and RF partition consists of for example RF signal traces, connectors and amplifiers. [10 p.2.3]

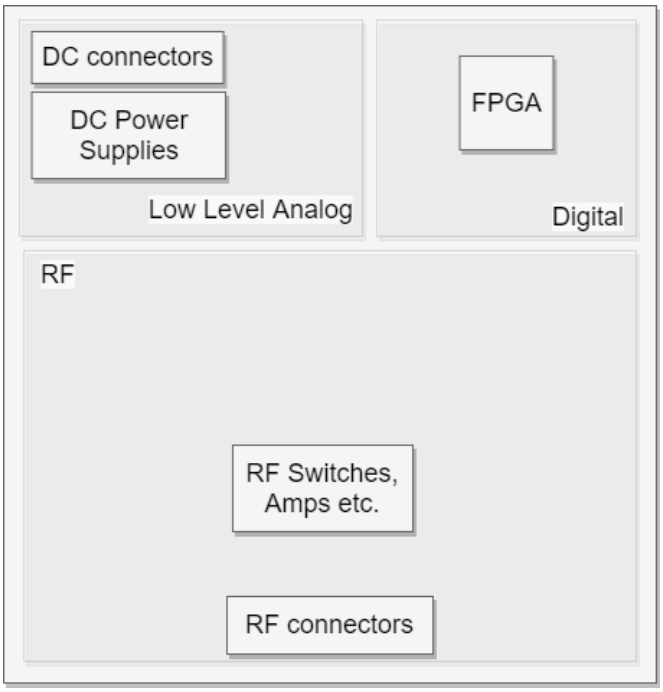

Figure 9. Functional partitioning of PCA.

Partitioning is one way to help mitigate the unavoidable difficulties in designing RF devices. These include such concerns as noise, isolation, crosstalk, impedance matching, delay, loss and electromagnetic combability (EMC). Since the designed RF tester module is mostly a switch network, most important design factors are noise, isolation and crosstalk. Proper impedance matching can be taken care of with component choices and signal loss with amplification.

Noise can mean the inherent thermal noise present in all electrical systems or any unwanted interference that corrupts the useful signal. Inherent noise is inescapable in RF systems, but its effect can be controlled by careful choice of components and design topologies [11 p. 487-488].

This means for example keeping power amplifiers (PAs) away from low noise amplifiers (LNAs) or separating switching regulators on their own partition. Outside noise can be stopped with shielding, i.e. mechanical housing of the PCA completely, or using some smaller conductive or magnetic covers [12]. These have their own challenges, such as they might be difficult to manufacture or assemble (i.e. expensive) or they might take up valuable PCB space. Noise inside a system can also be caused by crosstalk.

Crosstalk denotes the phenomena where a signal traveling on a trace (or the return signal on the ground path) induces an undesired signal in a nearby trace. This can be mitigated with proper separation of traces or with PCA layout design means, such as using different layers and careful grounding. Since RF components (and thereby several traces also) are dominantly placed on outer layers (top and bottom) of the PCA, mechanical housing is the solution [13 p. 277-278]. In RF tester module design all shielding is taken care of with RF tester module housing mechanics covering the RF parts on the bottom side. In testing phase, the RF module, referred to as the DUT from this on, is already assembled in mechanics. The housing of the DUT takes care of mechanical shielding on the top side of the RF tester module PCA.

Isolation means that when a circuit or a network (for example a switch) is open, no signal should be coupled through it. Regarding amplifiers, it is important that the amplifier circuit input and output be separated as much as possible. This helps in avoiding oscillations which might occur if the output amplified signal gets coupled back to input side. Crosstalk and isolation in the context of RF switches are depicted in Figure 10. where the leakage through unconnected part of a single-pole double-throw (SPDT) switch is presented on the lower switch (isolation) and coupling to a near-by trace is shown in the upper switch (crosstalk). These issues are revised in the layout section of this chapter.

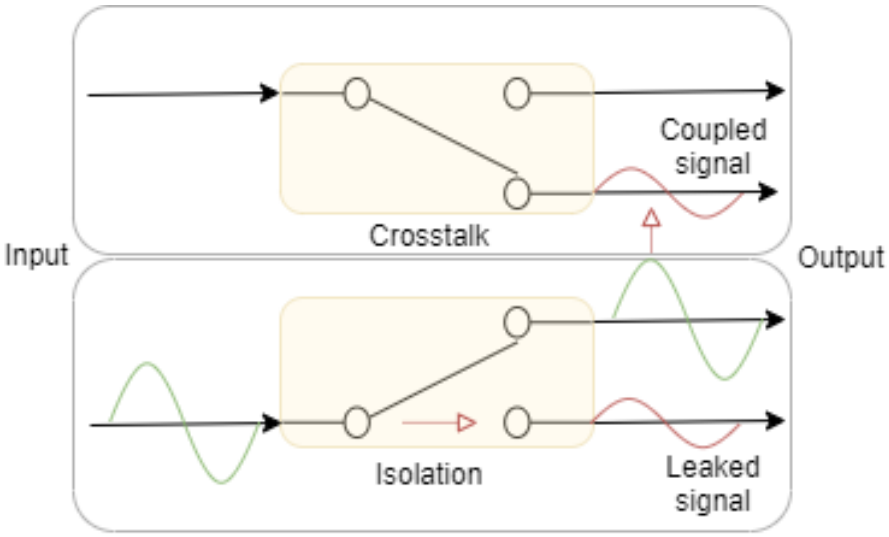

Figure 10. Crosstalk and isolation in RF switches.

5.1 Parts selection process

In the hardware design, one major aspect is the selection of parts. Regarding schematic design, this means selecting the components to perform the designed function, for example the splitting of the RF signal in a routing network. There are a lot of RF power splitters available to perform this task, and these components can come from many different vendors. The company to which

the design is developed, usually has a parts selection process, in which the different vendors are categorized.

For example, at Keysight it is recommended to use industry standard parts wherever possible. In the parts selection process, vendors are divided to preferred and non-preferred manufacturers. The term non-preferred manufacturer does not mean that it is forbidden to use these vendors, instead the guideline is that the design's bill of materials (BOM) must have a certain percentage (for example 80%) of the parts from the preferred manufacturers. The BOM is a listing of all the components in a design, such as the RF tester module. The component manufacturer categorisation is in the databook, from which the components are selected in the schematic design. The ratio of the preferred manufacturers' components in BOMs is monitored yearly as a part of the company's quality program.

Regarding the schematic design, the part selection is important for the persistence of the design. For example, some vendors might have problems to provide enough of the components during times of high demand, or there might be a disruption in the supply chain in unusual times. Therefore, it is important to choose parts that are industry standard and come from a dependable supplier. Part of the design process is to check the final design's BOM in company's part selection tool, for example to sort out components that may be nearing their EoL. In the schematic design, it is important to choose components that either have a distant EoL expectancy or have an alternative variant or vendor source.

5.2 RF switching network

The main functionality of the RF tester module is to route RF signals. This can be done with a network of routes including switches, splitters, connectors and other components, referred to a switching network. The RF tester module PCA design can be divided to three switching networks, RFLO, IFLO and instrumentation networks. The other components mentioned are enabling the operation of these networks. These are components related to powering, signalling and impedance matching for example.

The instrumentation network is responsible for connecting all the needed measurement equipment listed in the previous chapter to the DUT. Since this equipment is used to test DUT performance, there is no need to add amplification to these routes. The needed input power levels (at DUT) can be achieved with a passive network. In addition, the routes should be kept as simple as possible, so that for example additional amplification would not add to the measurement uncertainty.

The designed instrumentation switching network topology is presented in Figure 11. It includes a network analyser, routed to the DUT connectors so that it is possible to measure S-parameters on different input output pairs. S-parameters are complex values (i.e. including amplitude and phase) that indicate the transmission and reflection characteristics of a DUT. The numbering, for example S21 refers to the input and output ports respectively. S11 would implicate reflection measurement of port one. [11 p.174-175]

In the RF test system, the RF tester module instrumentation network enables for example a transmission (S21) measurement from Tx1 to Rx2. This is used in channel amplitude and flatness test. In the following the TRx i.e. the bidirectional port may be referred to as Com port. The requirement was to provide connection for each input output pair (from each Rx to a Tx port), and it can be seen in Figure 11 that this can be accomplished. It can also be noted that not all Tx and Com ports can be connected to each other. This is not necessary at this point but

might be an option in the future development. Other needed routes are SG to all the Com ports and Tx ports to SA routing, which can be realized with the designed topology.

The switches used are single-pole four-throw type (SP4T), which means that one input can be connected to one of the four outputs, or conversely, since these are bidirectional switches. The model is Analog Devices' HMC7992. The data sheet can be found in [14]. These are non-reflective switches (also called absorptive), which means that the ports that are not connected are terminated with 50 Ohm, as opposed to a reflective switch, that does not have the terminations and therefore signal is reflected from the not connected ports [15]. The switches have 45 dB isolation (at 2 GHz) and low insertion loss (0.6 dB at 2 GHz). They require one sided supply voltage (5 V is used) and two positive control voltages (3.3 V is used). The DC distribution of the RF tester module is further elaborated in power distribution chapter. The bandwidth is specified to be 0.1 to 6 GHz, but the switch can operate down to 10 kHz as stated in the data sheet.

Outputs and inputs of the RF module need to be tested on the front panel SMA connectors that the customer also uses. The Tx and Com ports depicted in Figure 11. are connected to the tester module front panel via coaxial cabling. Sub miniature push-on (SMP) connectors are used at the board end and SMA connectors at the front panel. All connections to and from PCA board use fixed attenuators and AC bypass capacitors. This is a standard RF design procedure for ensuring proper impedance matching and blocking of possible DC component in the signals.

DUT connects to the tester module front panel connectors via coaxial cabling. This means that the tester module front panel needs to have 16 SMA connectors. For testability this sets an obvious challenge, since each time 16 SMA connectors need to be connected. This can be accepted in a low volume production tester.

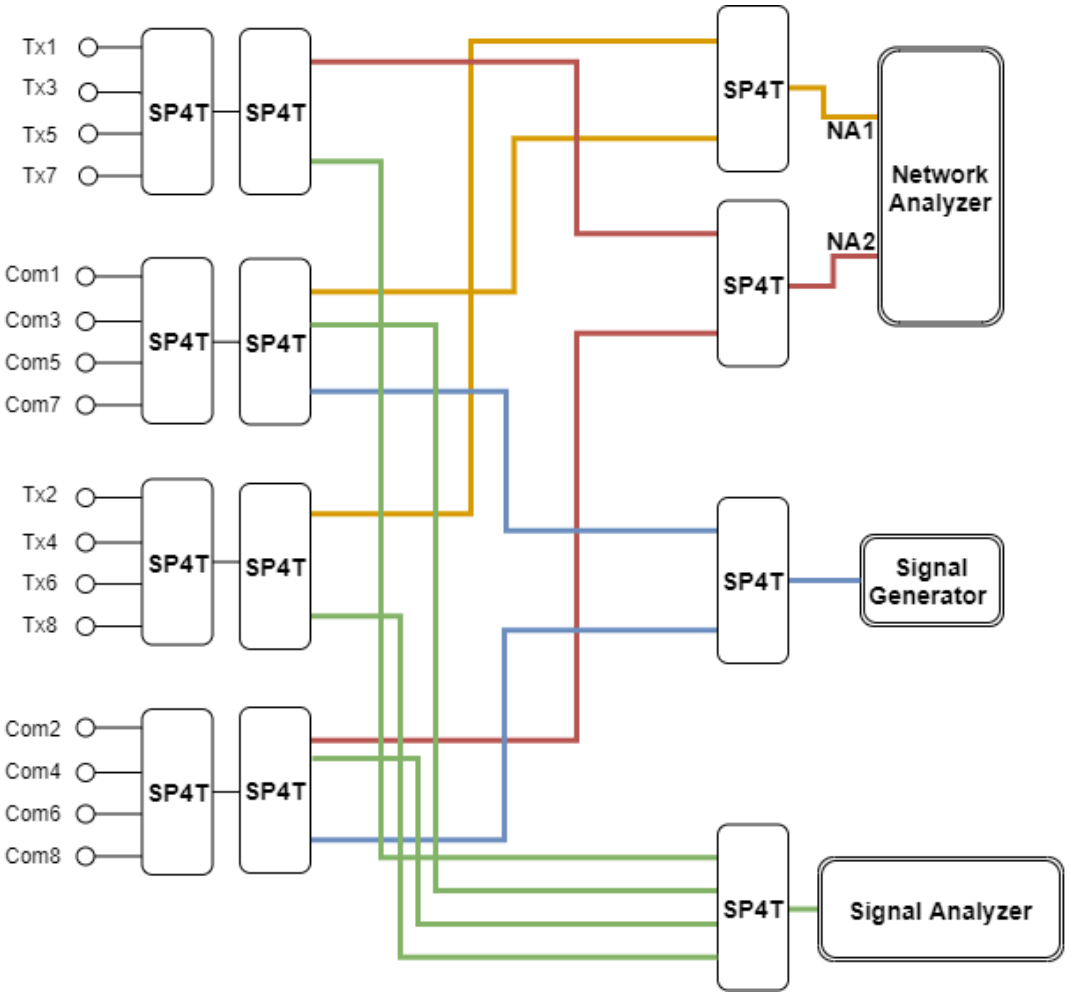

Figure 11. RF tester module instrumentation network.

In addition to the instrumentation network, the RF tester module must route IFLO and RFLO signals to the DUT. The IFLO and RFLO signals at DUT need to be on a specified level, so there needs to be some amount of amplification on these networks. Other difference to the instrumentation network is that LO signals must be available for multiple DUT inputs at the same time, so the networks consist of splitters in addition to switches and amplifiers. All together 16 IFLO and 16 RFLO signals are provided for the DUT. The passive structures of the designed networks are presented in Figure 12.

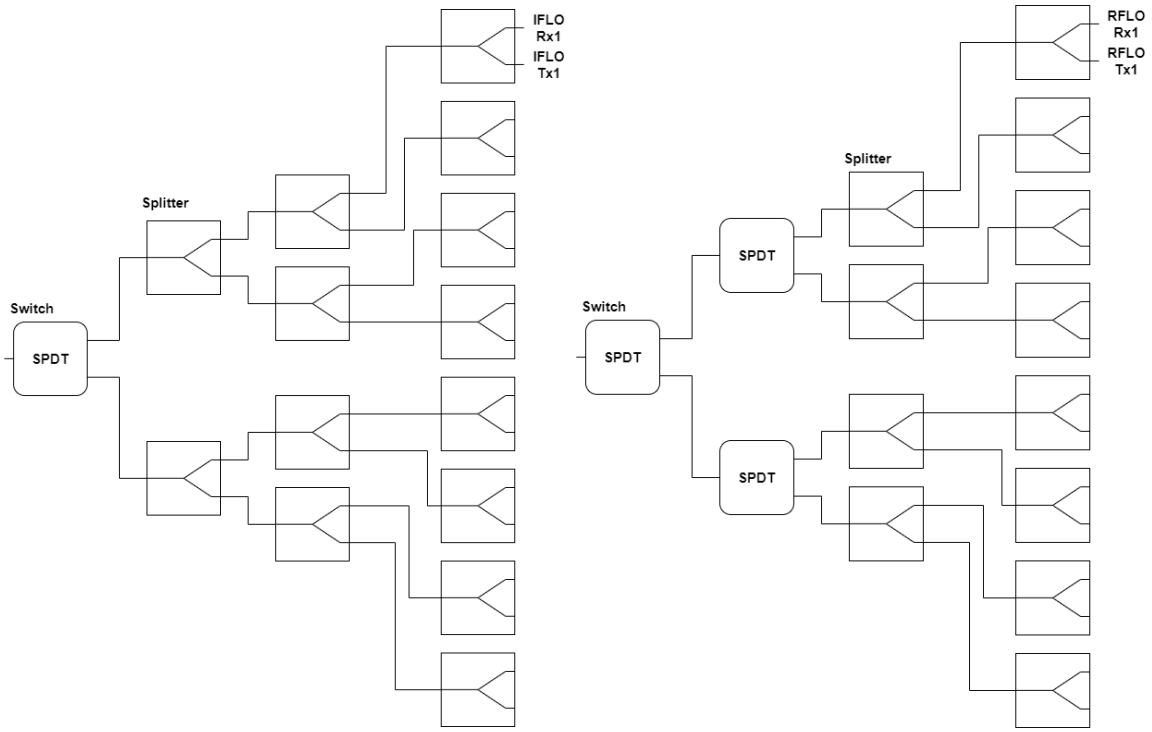

Figure 12. IFLO (left) and RFLO network passive parts.

Because of the needed amplification, it is beneficial to simulate these networks with active parts. The simulations are done with Keysight's Advanced Design System (ADS) using SnP-files for the purpose of ensuring correct signal levels at needed frequencies. SnP-files are manufacturer provided files that include S-parameters of the component in question [16]. Note that for clarity, the simulations show one route only.

The YAT_1+ components visible in the circuits are one decibel fixed attenuators used for improved impedance matching and reflection absorption. Although it may be argued that impedance matching with a fixed value of only 1 dB might not be ideal (as compared to for example a 3 dB YAT), the reasoning for the 1 dB YAT is that a standard size component can always be changed to a higher value (or to a zero dB YAT) if need be. This change can be done without a layout change by just a change in BOM. This is a big advantage, since any change in the layout is always a much slower and costlier operation.

Other peripheral components such as DC blocking capacitors are omitted in the circuits for clarity. The simulation model of the IFLO network is presented in Figure 13.

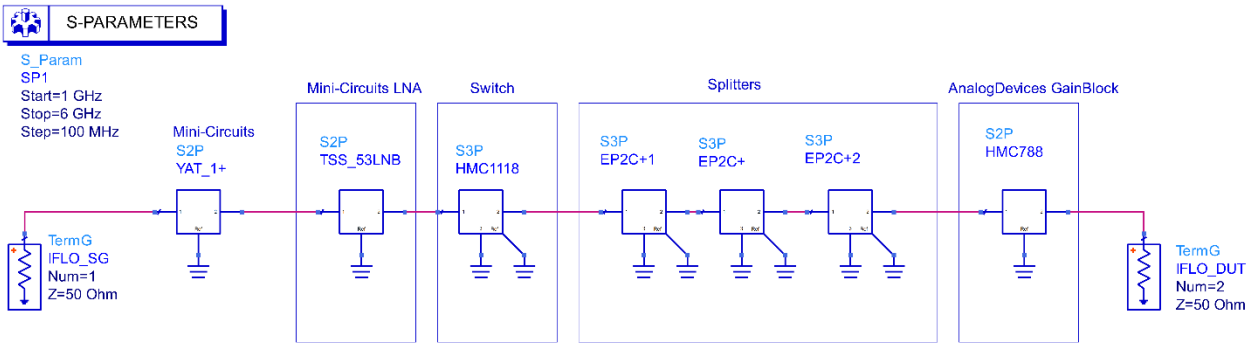

Figure 13. Simulation model of the IFLO Network.

In IFLO network, the chosen splitters are MiniCircuits' EP2C+ [17]. Power splitter is a passive device that takes an input signal and produces output signals with specific characteristics. These characteristics are phase and amplitude of the signals. In the case of RF tester module, it is desirable to have equal amplitude and good power handling. The attenuation of one power splitter is approximately 1 dB, on top of the 3 dB caused by the split in two.

The switches in the IFLO network are Analog Devices' HMC1118 [18]. These are single-pole double-throw (SPDT) type and use two-sided operation voltages: 3.3V and -2.5V.

The LNA used for the entire network is MiniCircuits' TSS-53LNB+ [19]. There are also Analog Devices' HMC788 gain blocks [20] at each output to ensure proper signal level at DUT.

RFLO network uses same type of switches and splitters as the IFLO network. The amplification is provided by Analog Devices' HMC7357LP5GE PA [21]. RFLO network simulation model is depicted in Figure 14.

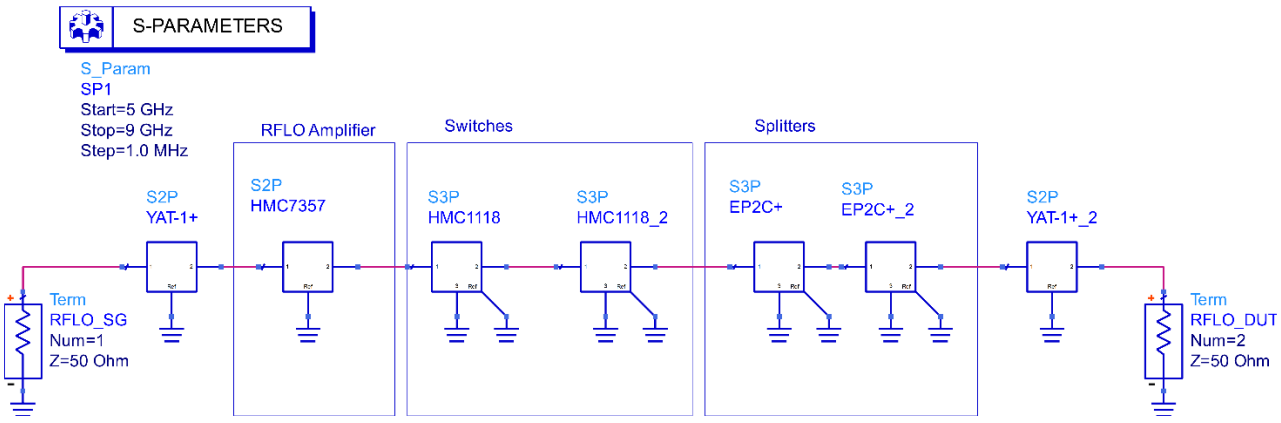

Figure 14. Simulation model of the RFLO Network.

Simulations show that the gain of the IFLO network is higher than 16 dB at the desired bandwidth which suffices for the needed IFLO level at DUT. RFLO network gain is higher than 17 dB for entire bandwidth. The results are presented in the Appendix 1 and 2.

As stated before, instrumentation connections from the board to the front panel and to the DUT are routed via coaxial cables. LO signals on the other hand are connected between PCAs

with RF board-to-board connectors. The connector type used is Rosenberger SMP. RF Board-to-board connection consists of the catcher's mitt, RF bullet and limited detent plug parts [22]. These are depicted in Figure 15 a) – c) respectively.

(a) Catcher's mitt (b) RF bullet (c) Limited detent plug

Figure 15. RF Board-to-board connection.

5.3 DC power and control signalling

After the RF switching networks designs are complete, the chosen components need DC power and control signalling. The former is done with a power distribution network (PDN), and the latter with a FPGA. The principle of operation of the designed PDN is such that the tester module gets 12 V DC main from the test rack. This is distributed with switching regulators and linear regulators so that larger voltage drops are done with switching regulators because they are more efficient. Smaller voltage drops are implemented with linear regulators nearer the actual components for improved noise control. The switching regulators are Analog Devices' µModule® (micromodule) regulators and the data sheet can be seen in [23]. Linear regulators are low-dropout (LDO) regulators from the same supplier [24]. The PDN of the RF tester module, also called a power tree, is depicted in Figure 16. Note that only one example of each LDO voltage and the powered components (loads) are shown. The currents at the load inputs are nominal currents adopted from the data sheets for directional purposes. These may and will vary in the active operation.

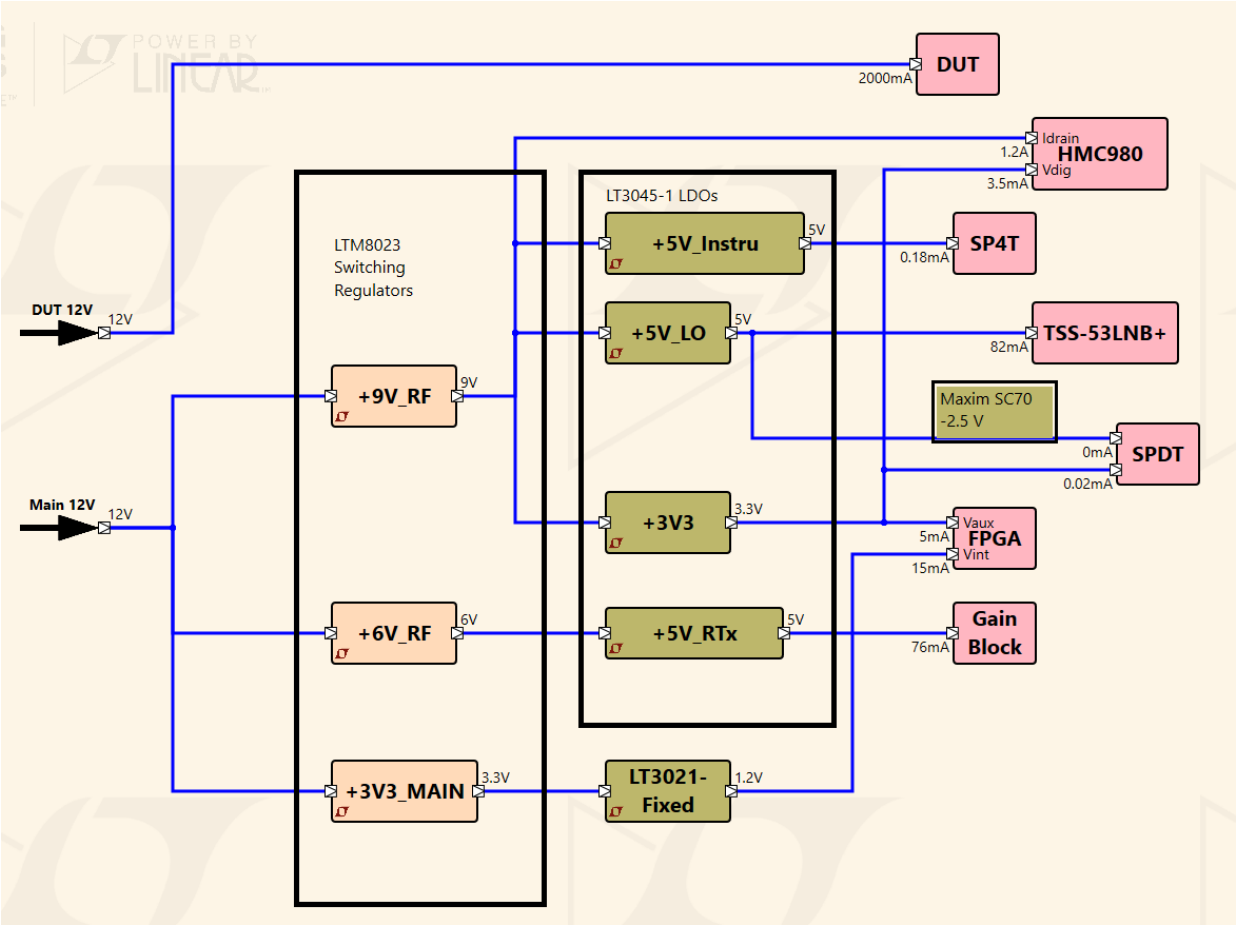

Figure 16. RF tester module power tree.

The earlier mentioned HMC1118 SPDT switches require two sided operating voltages. The negative voltages are created with an inverting charge pump (Maxim SC70 [25]). The RFLO PA (HMC7357) needs 8 V operating voltage which can be provided with HMC980LP4E bias controller integrated circuit (IC) which in turn needs 3.3 V and 9 V for its operation [26]. These are also depicted in Figure 16. The DUT's mains are provided via RF tester module PCA's DC partition.

Controlling the switch networks and enabling the DC powers is done with a FPGA. FPGA is a (re)configurable IC that performs logic operations according to a programmed bitstream. The used control voltages and enable signalling are 3.3 V positive.

For a schematic designer, the responsibilities regarding the FPGA are to provide the needed voltages for the FPGA operation and to ensure that the chosen model can produce the controlling needed. This means that the FPGA needs to have enough signal connections and these connections need to be able to drive the control lines i.e. provide the voltages and currents for the operation of the driven components. The chosen FPGA is Xilinx Spartan-6, and the data book can be found in [27]. As an example of the possible output voltages, a word monster: low voltage complementary metal oxide semiconductor (LVCMOS) class can be mentioned. This class includes a standardised voltage of 3.3 V which is correct control voltage for the switches used in this design.

5.4 PCA layout review

Layout design means the process of placing the components on the PCB structure. Other aspects of this process involve the connections between the components and vertical interconnect accesses, i.e. vias between the different layers of the PCB. These are done according to constraints (design rules) set by the company and the technology in question. A constraint set by the company might be the number of layers and a constraint set by the technology might be the width of a RF trace.

The RF interconnections on a PCA are transmission lines by nature. The basic transmission line theory is not in the scope of this thesis, but it can be found in [11 p.49-50]. In the printed circuit world, the visible lines on top and bottom layers of the PCB are called traces. The trace and the ground plane constitute a transmission line, on top and bottom layers of the PCA this is essentially a microstrip line [11 p.143-144].

The width, height and other dimensions, such as bending ratios of the traces are dictated by RF constraints in the schematic and layout design environments, but the schematic designer needs to be aware of these and check their sensibility. For example, the trace's width, thickness and height determine the impedance of the trace, so these need to be correct. The height in this case means the distance from the ground plane, i.e. the substrate thickness [10 p. 1.1].

One of the most important aspects of PCA design is to ensure a low impedance return path for the signals. All currents need a return path to the source, otherwise there would not be an electrical circuit. In this case the charge would just build-up somewhere or more likely find a return path on its own, both highly unwanted behaviour. While any AC current tries to find a low impedance path for the return signal, a high frequency (i.e. RF signal) current follows the path of least inductance. This is easily deduced from the definition of impedance

$$Z = R + j\omega L + \frac{1}{j\omega C}, \tag{1}$$

where R is naturally the (DC) resistance, $j\omega L$ and $j\omega C$ the inductive and capacitive reactance respectively. The implication of (1) is that frequency dependent part ($\omega=2\pi f$) causes inductive reactance to dominate at high frequencies. [28 p.2.2]

Layout design is a job for a specialist of this genre, and on a densely populated PCA containing RF and digital parts it might be a laborious one. There is usually a lot of collaboration between schematic design and layout design (and mechanical design). This might include such questions as placing the connectors in right angle or the order of components or perhaps the needed opening in the solder mask for proper grounding of the mechanics.

The RF tester module PCA is not a hugely populated board, so component placement on the top and bottom layers and routing the signalling and DC in the middle layers is relatively laxed. The DUT sets the constraints for the RF board-to-board connector placing regarding RFLO and IFLO signals. There is plenty of space for the traces, switches and splitters of these networks and isolating the needed amplifiers is easily done.

The most relevant phase of layout design regarding this design is the layout review. In the review, three important rules to check are RF operation versus DC signalling, (i.e. crosstalk control), isolation (i.e. RF connector and amplifier placement) and proper grounding. The first rule can be accomplished with routing the signals on different layers and taking care that the connections to components are done with decent separation of the signals i.e. control lines away from RF inputs. Via stitching must be used around RF traces (an example later).

The most difficult part of the tester module layout is the placing of the instrumentation connectors. Due to mechanical restrictions, all these need to reside on one edge of the board

(the edge facing the front panel). This is not ideal construction regarding isolation or crosstalk. The problem is mitigated by arranging the connectors so that the connectors in use at one time are separated from each other. A little relief is also available with mechanics, since there is some space for dividing walls. The instrumentation coaxial cables are connected to PCB with earlier mentioned SMP plugs (Figure 15).

As stated earlier, grounding means that the signals need to have a low impedance return path. This is accomplished with ground layers and the earlier mentioned via stitching. For example, the next layer beneath RF layer (top and bottom) needs to be a ground layer. Via stitching means that the RF traces are surrounded with ground paths, i.e. interconnections between top ground layer and the ground layer beneath the RF layer. The top ground layer is also called ground pour or ground flood. Via stitching is used because these grounds need to be at the same potential, and the best way to accomplish that is by connecting them together on many points. This also helps in tying up an isolated ground pour (island) to other ground plates, and thus preventing it from becoming a radiator. Lastly, the via stitching effectively prevents the microstrip trace from coupling to a nearby trace, and therefore increasing isolation (preventing crosstalk) between the traces. Stitching also makes sure that RF signal (electromagnetic wave) does not travel between two planes, by preventing this artificial waveguide. [29]

Final thing in the layout review, and closely related to grounding is to check that the design has proper solder mask openings for the mechanics. The solder mask means thin insulating coating on top of the PCB copper. The openings are marked in the output drawings generated in the layout process. The PCB and PCA suppliers manufacture and populate the boards according to these drawings. Inspection of these drawings is the last thing in the layout review.

Some of the placings for connectors, solder mask opening for mechanics and via stitching in the RF tester module layout are exemplified in Figure 17.

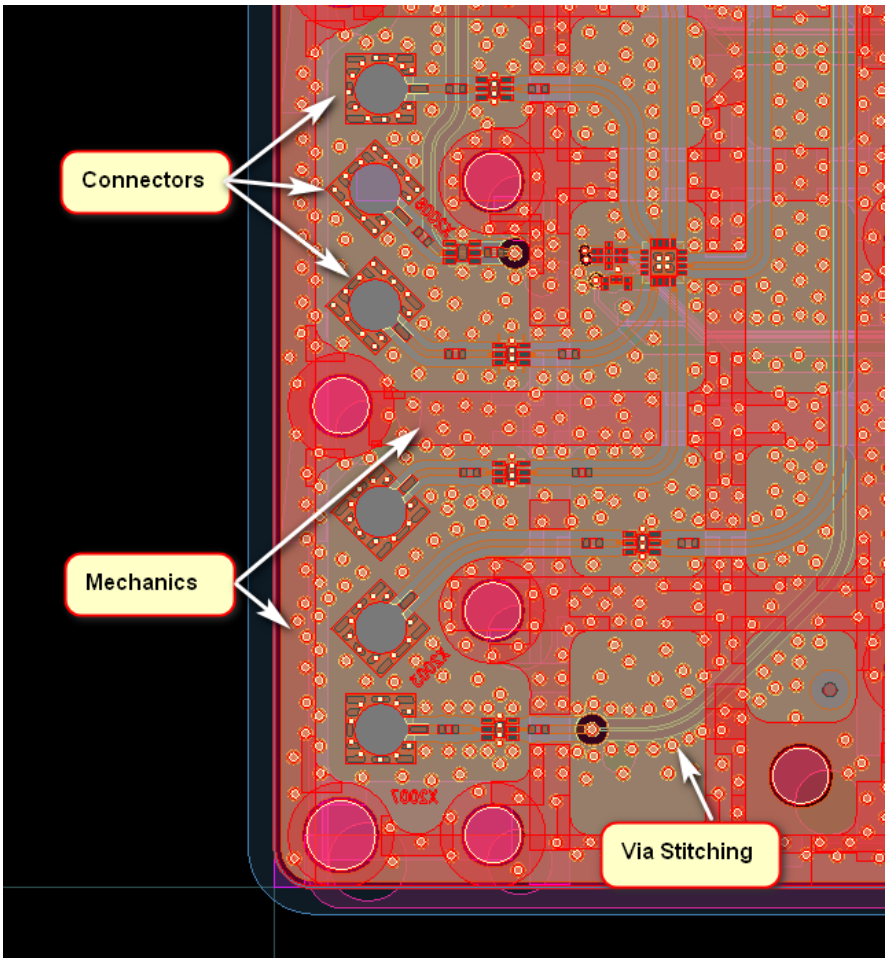

Figure 17. RF tester module layout example.

6 VERIFICATION AND VALIDATION

In this chapter, the verification and validation of the RF tester module is presented. Firstly, the bare board PCA functional verification is described. This means testing of the PCA and confirming that it works as intended during the design phase. Secondly, the calibration procedure and comparison of relevant signal levels against earlier simulations are given. Lastly, the validation of the RF tester module in the RF test system is examined. This means ensuring that the needed tests can be executed on the RF module.

6.1 Board level testing

In an ideal world, all the RF or other signal integrity aspects would be simulated with all the parameters of the final design. This is not usually feasible due to lack of time or human resources. Because of the possibility of a human error in the design or PCA manufacturing, it is customary to verify the correct operation of the board manually in the R&D laboratory after the PCA assembly is complete. This is usually done with a prototype board or with early series PCA board(s). The need for this testing stems from the fact that these boards are usually complex and therefore relatively expensive and difficult to manufacture. If there is a design, layout or another 'bug' or defect, the loss of money with a larger series would be considerable.

The amount of possible checks that can be done to a bare board naturally depends on the design. On the RF tester module PCA, it is possible to do DC power testing and signal routing tests. These are done by supplying DC power to the board and controlling the FPGA (which remains unprogrammed at this point) with a test program on a laptop and boundary scan connection [30 p.19]. The control signals are routed via two adapters, joint test action group (JTAG) - universal serial bus (USB) adapter, and a special made test adapter that attaches to the RF tester module board-to-board connector. RF signal routes were measured with a network analyser. Manual test set up is depicted in Figure 18.

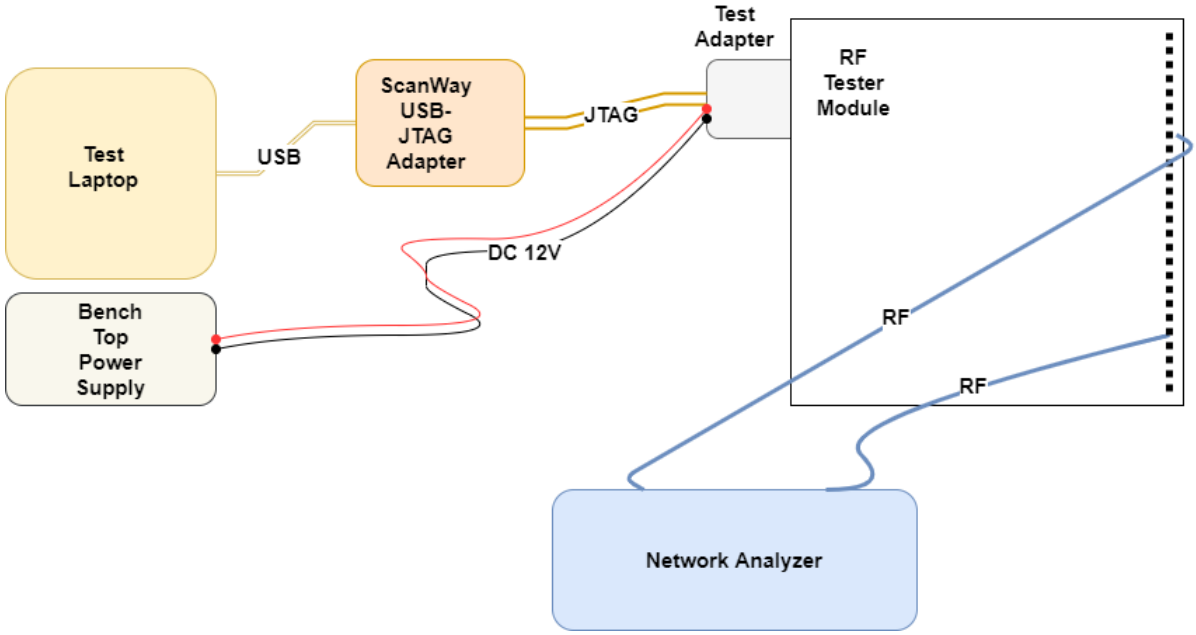

Figure 18. RF tester module manual test set up.

Regarding DC operation, the design presented no large problems. For example, current consumption with all supplies and amplifiers enabled was found out to be 2300 mA. More than half of that is due to the amplifier in the RFLO chain. The amplifier (HMC7357) is specified to draw 1200 mA, so this behaviour seems reasonable.

One strange thing was the enabling sequence of the amplifiers bias controller IC (HCM980LP4). The power up sequence presented in the data sheet states that firstly a 3.3 Vdig voltage should be presented and secondly the Vdd voltage, which then enables the generation of the drain and negative voltages to the PA. In the manual testing it was found out that after The Vdd was presented, the Vdig needed to be turned down and up again to power up the amplifier. This is trivial thing to implement with software control, but the reason for this behaviour was left unclear. The PDN operation was tested by measuring all the switching regulators and all the LDOs' output voltages with a voltmeter. These were found out to work as intended.

On the RF operation side, the tested routes were verified to work by sample testing. This means that only some of the routes were tested (justified later). One example of the tested routes is visible in Figure 19. This route is part of the instrumentation network, namely signal generator to Rx1 route.

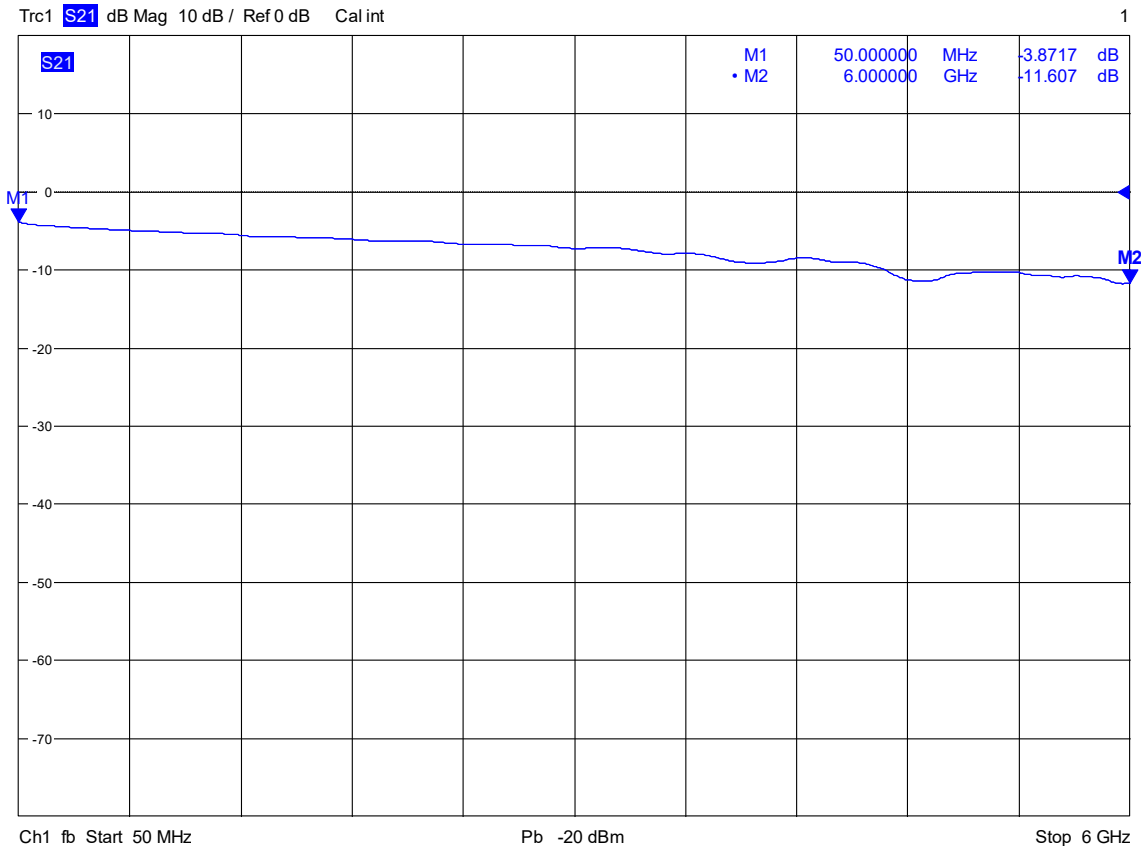

Figure 19. Transmission measurement of signal generator to receiver port 1.

The transmission, or S21 parameter measured with NA shows that there is 3.8 dB attenuation on the lower end of frequency spectrum, and 11.6 dB attenuation on the higher end. In the RF requirements section 4.4 it was estimated that the overall attenuation in the route might be on the scale of 10 dB, so this is expected behaviour of this passive route.

Other than the RFLO PA power up sequence, the designed RF switching networks were found out to work as expected. RF signals could be routed from the origins to the required destinations.

The problem with manual board testing is that it is very slow and laborious. For example, the NA cable connections must be made directly to the SMP plugs, which is rather difficult without supporting the cables, and might cause damage to connectors. With a switching network such as the RF tester module, possible routes are plenty, so just the basic functionality was tested at this point. RF calibration of the tester board is more automated and thorough test phase and it is presented next.

6.2 RF tester module calibration

All measuring equipment require calibration before they can be reliably used in measurements. In RF testing this stems from the nonidealities in the test system. These can be losses in the cables or delays in the signal paths. There are several methods of calibrating a system, depending on what characteristics need to be considered. For example, if only cable loss matters, calibration with a SA and power meter suffices. If the phase of the signals is of importance, vector measurements with a network analyser are needed. [31]

Regarding calibration in RF testing, the most important characteristic is signal power. For example, in a passive network, such as the RF tester module instrumentation network, there is naturally some amount of power loss. In the RFLO and IFLO networks, where there are amplifiers present, the power level is higher in the output than in the input, and therefore there is gain in the route.

The operation of the components in these networks vary, so the losses and gains of the individual routes are different, and for a measuring equipment, it is imperative that each individual route be measured. It was stated in the requirements chapter, that also group delay of the RF module needs to be measured. Because of this, also the delays of the RF tester module network routes are measured and recorded.

Calibration in the context of the RF tester module means that the RF routes are measured with a NA. The results are stored numerically on a file, which is later programmed to RF tester module flash memory. Calibration information is used in the RF test system for the purpose of removing RF tester module losses and delays from the RF test system measurements.

Calibration of the RF tester module is done with mechanics and front panel connectors (coaxial cabling) assembled. This is depicted in Figure 20, where the RF tester module i.e. PCA, housing and front panel mechanics with SMA and N-connectors are visible.

Figure 20. RF tester module assembled for calibration.

Calibration is done with a dummy housing mechanics (not visible in Figure 20) on top of the tester module PCA, to achieve same operation conditions as in the RF test system with RF module. Other than the mechanics, the calibration set up is like in Figure 18. The calibration software is semi-automated, and each RF route power levels and delays are recorded. Regarding this thesis, the interesting results are IFLO and RFLO levels, since on these routes there needed to be gain. Example gain measurements on the IFLO and RFLO routes are depicted in Figure 21 and Figure 22 respectively.

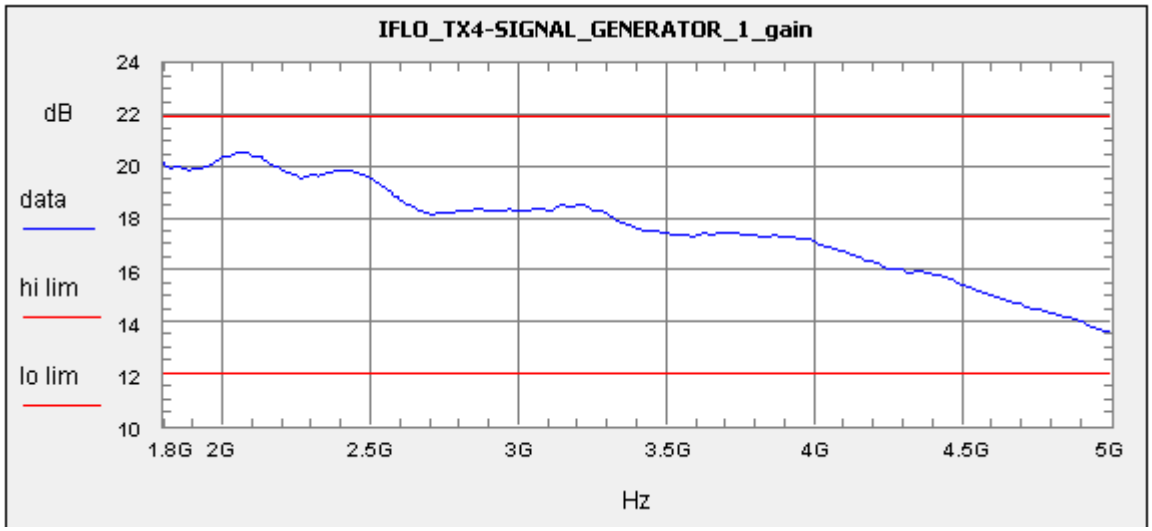

Figure 21. Tx4 IFLO route gain measurement in calibration.

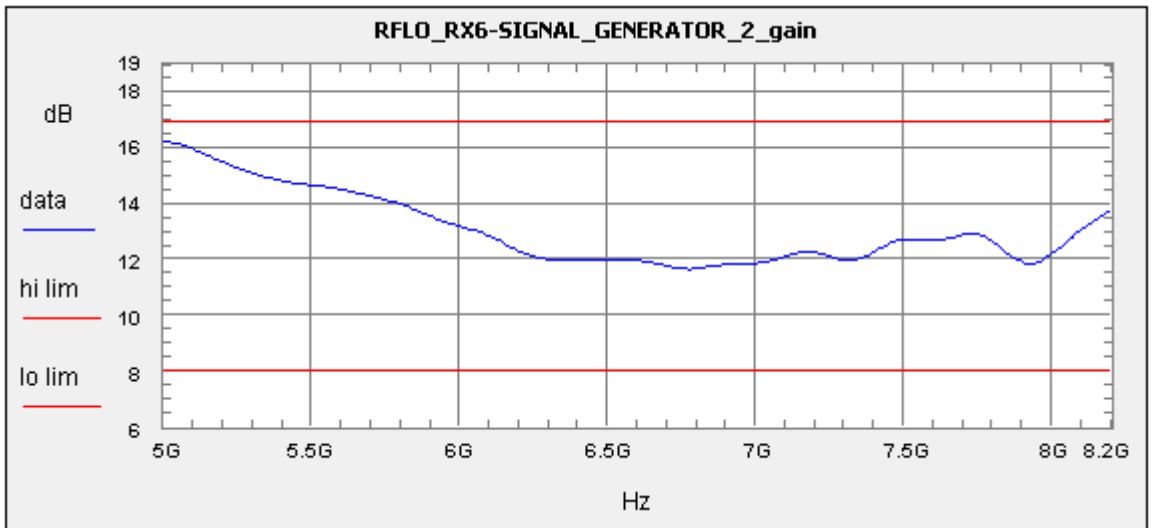

Figure 22. Rx6 RFLO route gain measurement in calibration.

When comparing these with simulations in the design chapter, it can be noted that the LO levels are lower than in the simulations, especially in the higher end of IFLO frequency range. This is not a large surprise, considering that in the simulations several real-life phenomena are omitted. These include for example substrate losses and attenuation due to coaxial cables from front panel to PCA. There could also be a slight impedance mismatch in the splitters, and some part of the RF signal might reflect and add destructively, depending on the phase of this reflected signal.

Other than the above, the calibration of the RF routes was successful. The power levels were determined to be suitable for the RF module to be validated in the RF test system, which is presented next.

6.3 RF tester module in the test system

Lastly, the operation of the RF tester module in the RF test system needed to be validated. This means ensuring the interoperability of the RF tester module, other test system hardware and the test software. The RF tester module must enable the tests described in the requirements chapter and the possible defects in the DUT must be found on an acceptable accuracy level. Tests are executed with a Python test program that controls the instrumentation and the RF tester module. The validation was done empirically by running the test script to a multiple DUTs and analysing the results in collaboration with test engineering and DUT designer.

After the RF tester module is assembled to a test rack, the calibration data collected in the previous section and the bitstream for the RF tester module FPGA are programmed to a flash memory. These can be done with Xilinx Vivado Lab program via JTAG connection. After this phase, the RF tester module was ready to be validated with the DUT. This was done naturally with a RF module attached on the RF tester module. The attachment is secured with screws from the top of DUT to the housing mechanics of the RF tester module.

The most difficult part of this validation phase was to set the yield correctly. This means that there should be as little false negatives as possible and zero false positives. False negatives mean that the test fails although there is no real defect on the DUT. False positive on the other

hand means that a defective DUT passes the test. These errors are called type I and type II errors, respectively. [32 p.41]

The former causes unnecessary troubleshooting, which in turn slows down the production process and may even lead to a real defect in the disassembly. The latter on the other hand may cause a failure in the subsequent phases, and once again slow down the production process. The worst case of a type II error means that the defect is found by the customer.

Largest problem found out in the validation was caused by the earlier mentioned lower than expected IFLO level at the higher end of the frequency range. This led to false negatives in the DUT testing, since a too low IFLO level at the mixer of the DUT causes the required amplitude test to have excessive ripple. This behaviour is depicted in Figure 23. The amplitude variation of the signal is presented on y-axis and the frequency naturally on the x-axis. The limits depicted in Figure 23, as well as in all the rest of the figures in this section, are descriptive only, and do not necessary reflect the real production specifications, or true signal power levels.

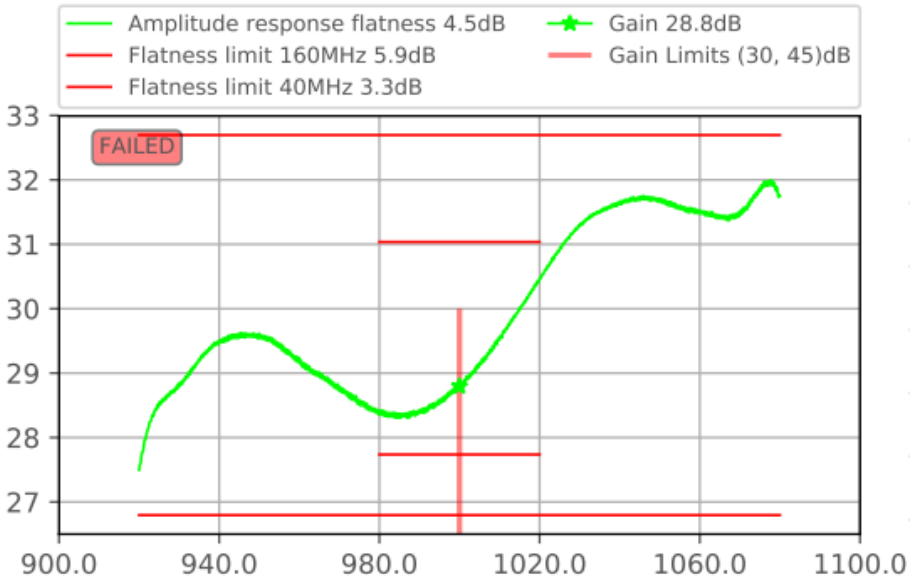

Figure 23. Amplitude response ripple on 160 MHz BW in flatness test.

The troubleshooting of this behaviour required a lot of additional testing, since this is one of the most important tests on the DUT. Without going into details of the RF module design, it can be said that the most important hardware section regarding this test involves component that has caused problems repeatedly. Therefore, setting the signal level correctly was on the other hand very important and on the other hand slow. Slowness was caused by the needed iterations to ensure that a out of specification behaviour would not be concealed by too lenient test specification.

This troubleshooting, and setting the yield correctly caused some delay in the validation of the RF test system. Since the signal level through the RF tester module was still sufficiently high, this could be fixed by adding a higher preset level to the IFLO signal at the test program script. Same test with proper IFLO signal levels is depicted in Figure 24, where the excessive ripple in the signal amplitude is no more present.

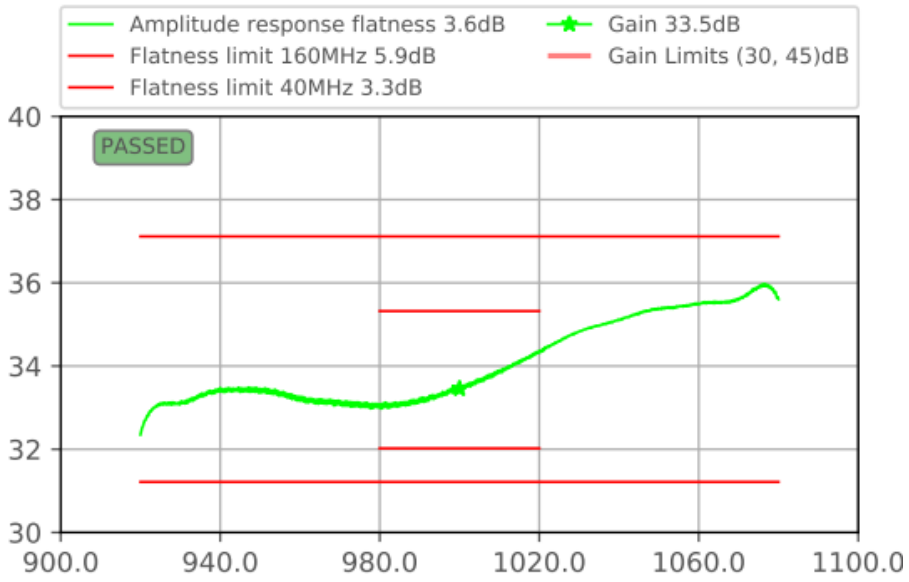

Figure 24. Amplitude response flatness test with correct IFLO level.

Other than the previous, the RF tester module was successfully validated in the RF test system and could fulfill the testing requirements. One test example is presented in Figure 25, where spurious artefacts in the spectrum of Tx to SA measurement can be seen. The spurious artefacts reside between 1 and 2 GHz and were caused by a defective PA. After troubleshooting and changing the PA, the spectrum was found out to be clear.

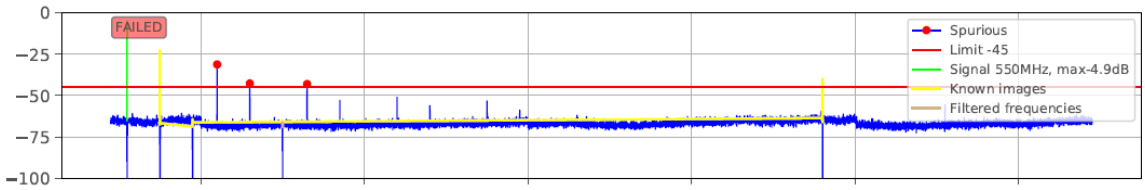

Figure 25. Spurious artefacts between 1 and 2 GHz in transmitter measurement caused by a defective PA.

Next, an example of a result caused by a human error mentioned many times in this thesis is shown in Figure 26, where in the Tx to Rx measurement, the Rx chain is in noise (blue trace) while there is signal in the Tx chain (measured with SA). The whole chain measurement is done with NA on 10 MHz to 6 GHz frequency range. The failure was caused by an assembly fault, more precisely a RF bullet (depicted in Figure 15) was missing.

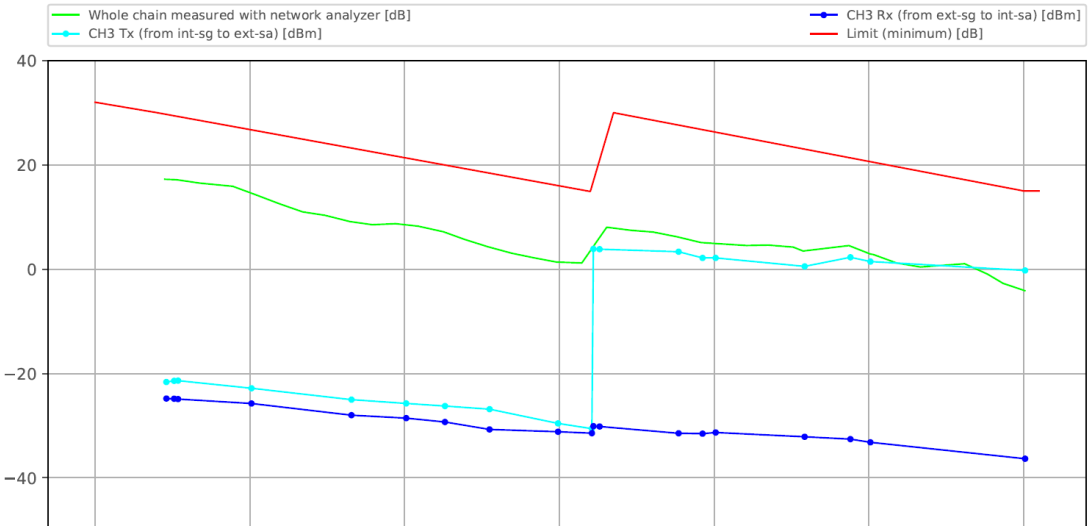

Figure 26. Failure in Tx to Rx NA measurement on 10 MHz to 6 GHz range caused by a missing RF bullet.

Lastly, a successful Tx flatness test is presented in Figure 27. As stated in the requirements section, the flatness needed to be measured on selected spot frequencies. Depicted are two spot frequencies, 1 GHz and 3.2 GHz, with 160 MHz wide measurement on each.

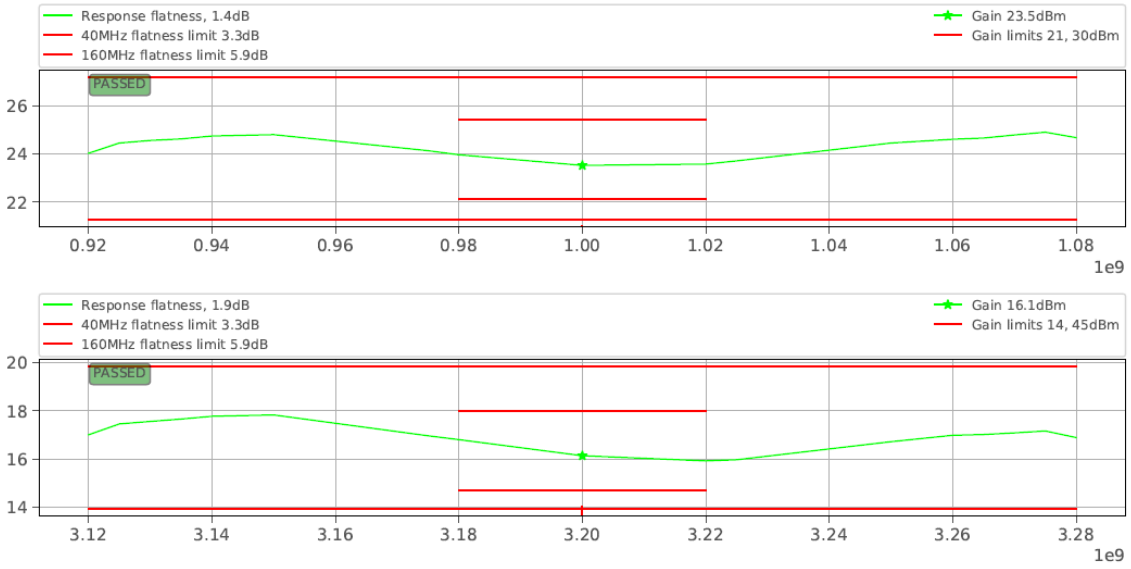

Figure 27. A successful Tx flatness test on 1 and 3.2 GHz frequencies with 160 MHz BW.

The completed RF module test system, used in the validation, is shown in Figure 28. It consists of the instrumentation cabinet with three signal generators, one signal analyser, one network analyser and a PC for running the test script. On the right, the RF module to be tested is attached to the RF tester module in a test rack, as was described in Figure 7 in chapter four.

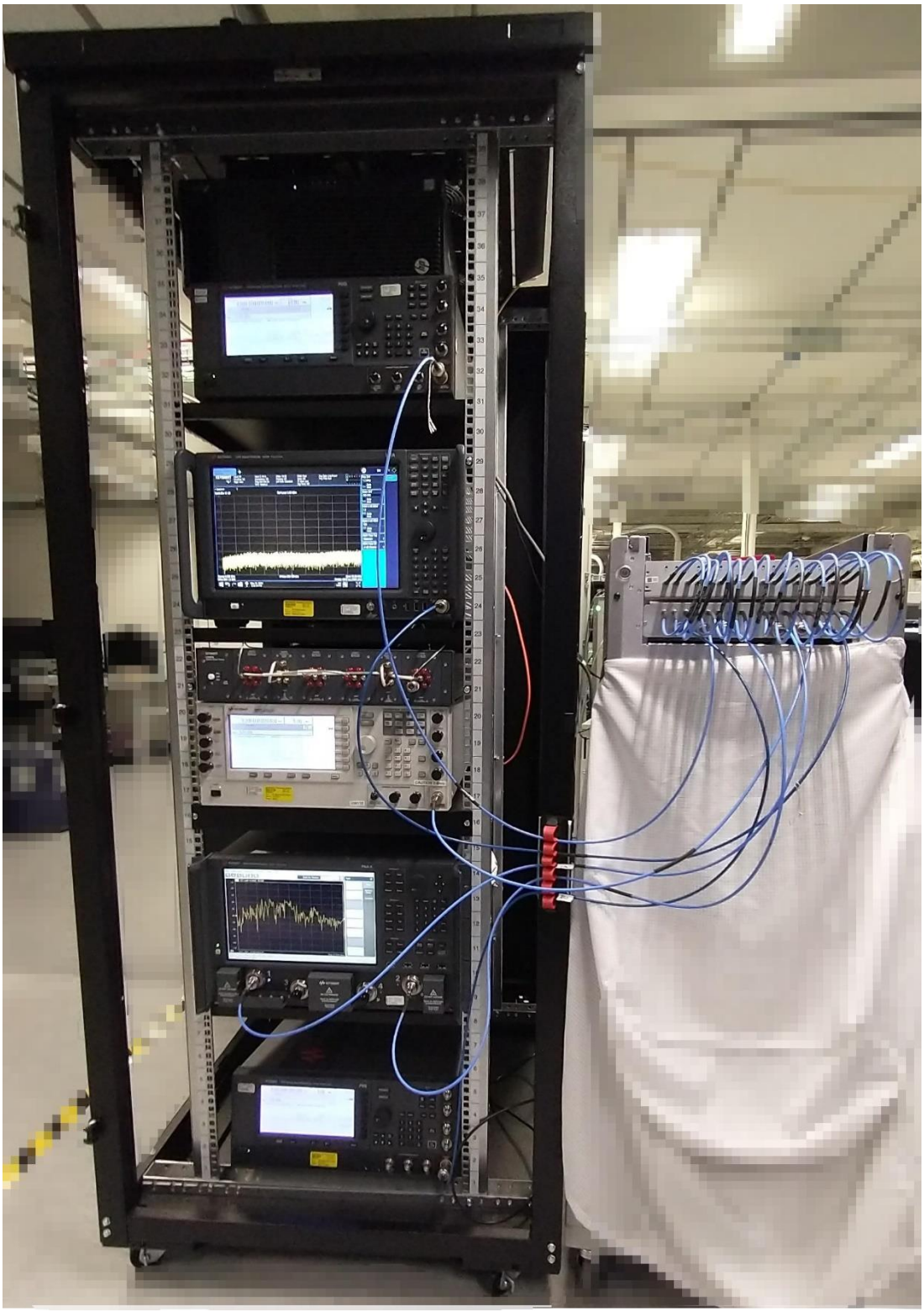

Figure 28. RF module test system.

7 DISCUSSION

Wireless communications are constantly developing toward wider bandwidths, higher frequencies and systems that include more and more inputs and outputs, i.e. MIMO schemes. This increasing complexity means that the requirements for the measuring equipment used in the development and validation testing of these systems are becoming more and more stringent. This stems from the fact that this equipment needs to outperform the specifications of the systems that they are used to test.

The aim of this thesis was to develop hardware testing capability for Propsim channel emulator radio transceiver. The channel emulator is one of the test equipment mentioned before. It is used to emulate the radio channel, for example between a base station and mobile user. The channel emulator consists of channel units which are responsible for the input and output of the signals to be tested. The radio transceiver parts are referred to as RF module and the developed tester part is referred to as RF tester module. The RF module is a part of channel emulator channel unit, and it is responsible for up- and down-conversion of the radio signals in Propsim radio channel emulations. This is accomplished with a super-heterodyne transceiver structure.

The RF tester module is responsible for routing RF signals to and from the RF module in the RF test system. The RF test system consists of the instrumentation, a PC for the test program, and a test rack, which in turn houses the RF tester module. In the RF test system, RF module is referred to as the DUT. RF tester module needs to provide DC powering for the DUT as well as local oscillator signals for DUT's operation. These are naturally the RFLO and IFLO signals needed in the super-heterodyne structures. In addition, the RF tester module is responsible for providing interconnections between the needed instrumentation and the DUT.

The need for production testing stems from the fact that modern RF measurement equipment, of which Propsim is one example, are very complex devices. One RF module has 16 RF connectors, eight bidirectional and eight output-only. This means that in one RF module, there are eight transceivers, and since Propsim is a measuring equipment, the performance of the individual parts needs to be on a high level. A defect in any part of the RF module means that the emulation performance is compromised. The complexity justifies the modular production of the Propsim channel emulator, and the modularity and complexity justify the need for module testing and further the need for the RF tester module of this thesis. In the production, defects in the modules need to be found as early as possible to avoid delays in shipments of the products and to achieve the performance level promised to customers in the specifications.

The hardware development process is such that firstly the requirements for the RF test system of the RF module are established. These requirements come from the tests that are needed to run on the DUT and they directly dictate the specifications of the RF tester module design. The RF module needs three types of input signals, RFLO, IFLO and the RF test signal. Therefore, three signal generators are needed, and the RF tester module needs to route these signals with appropriate power levels. The IFLO signal level at the DUT for example needs to be at +20 dBm for the correct operation of the transceiver, so some amount of amplification in the signal chain is needed. The LO routes with amplifiers are simulated in the design phase.

In addition to input signals, the RF tester module needs to connect network and signal analyser to the DUT. These are connected via instrumentation network in the RF tester module. The instrumentation network is kept as simple as possible (i.e. passive) for not to add uncertainty in the measurements.

The design phase comprises of the schematic design of the RF tester module PCA and the review of the PCA layout. The RF switching and splitting networks are designed for the

instrumentation and for the LO signals. The LO routes are simulated to ensure the proper power level of the signals at the DUT.

Proper partitioning in the PCA is essential for noise and interference reduction. These inherent issues can also be restrained with mechanical housing. In the schematic design the components are also provided DC power and control signals. The first is accomplished with a power distribution network, and the latter with FPGA. In power distribution network design, the important parameters are efficiency and noise. Used structure includes switching regulators followed by linear LDOs. The FPGA in charge of the control signalling needs to have enough available connections and current capability for driving the components. Xilinx Spartan-6 is a suitable FPGA for the design of this thesis.

In the layout design, the important details for the RF designer are to ensure proper routing of the RF signals. This means ensuring that aspects such as isolation, crosstalk and grounding are considered. Regarding isolation, it is important that inputs and outputs of a component be decently separated. Also, RF connectors on the PCA should either have distance between them, or to be grouped in such a way that active signals are separated. In the LO parts of the design this provided no problems, since there is plenty of space on the PCA in these partitions. The instrumentation network connectors on the other hand reside on front edge of the PCA, so the grouping was necessary. This was partly solved with mechanical walls. Crosstalk can be taken care of by ensuring that signal traces in the top and bottom layers have decent separation to DC control lines, and with a good amount of via stitching. The latter means that the ground layers are ‘tied’ together with conducting thru-holes. Last thing in the layout review is to ensure that the PCA has solder mask openings for the mechanical housing.

After the design of the RF tester module was complete, its functionality needed to be verified on a bare PCA board level. In this phase it was found out that the DC operation of the board was as designed, apart from the start up sequencing of the RFLO PA. This could be fixed with software, but the root cause for this behaviour was left for future inspection.

After the board level verification, the RF tester module needed to be assembled with the mechanics and calibrated. At this point the mechanical compatibility was also tested and proven to be as designed. The need for calibration stems from the fact that in RF design the most important parameters for the signals are power level and delay. The RF module passive parts naturally inflict power losses, that need to be compensated in the test program that controls the final RF test system. Delay measurement was part of the requirements, so the delay of the signals through the RF tester module need to be recorded.

In the calibration phase, it is noticed that the IFLO signal on the upper frequency band is considerably lower than in the design phase simulations. This not a huge surprise, since in the simulations some real-life phenomena are omitted for clarity and speed. These include substrate losses in the PCB material and possible reflections in the splitters, which might be caused by slight impedance mismatches. Other than the previous, the calibration phase was successful and revealed no surprises.

Lastly, the RF tester module was validated in the whole RF test system to ensure the needed tests were able to be carried out. The test system comprises of a PC for running the test script, the instrumentation needed in testing and a test rack that houses the RF tester module, to which the RF module to be tested is attached.

It was found out that one test produced false fails due to the previously mentioned too low IFLO signal level. There was some discrepancy in the signal level setting, due to calibration and test script co-operation, caused by too high expectancy of the IFLO signal level at the DUT. The difficulty was that at the same time there were problems with components that this test is used to test, and the too low signal level at DUT manifested in the same behaviour as the

component problems. The delay in the test yield setting was caused from separating the real failures in the test from the false negative test results. At the same time, it needed to be ensured that no defected DUTs would pass the test. After iterations, the signal levels at DUT could be set correctly, and the RF tester module could be validated to work as intended in the RF test system.

In conclusion, the designed RF tester module can be used in performing the intended tests. For future development, the recommendations are to check the DC start up operation of the RFLO PA. The amplification in this chain could also be separated to two stages. Currently, there is quite a lot of gain in an individual part of the RFLO network. The modifications in the PCA design depend on whether there is a need to develop the RF test system, mainly whether more stringent testing is needed. This could mean for example tests with more complex signals than CW.

The authors experience is that some component quality degradation related defects manifest themselves by gradual drop in for example receiver chain gain. Therefore, it would also be possible to extract statistical data from the RF test system, and gain added value on top of the tests being just pass/fail tests.

On the mechanical side of the hardware design, the development targets would be the attachment of the RF module on the RF tester module. Current solution uses DUT's screws for securing the modules together. Should there be a change in the mechanics of the channel unit, or in the mechanical design of the RF module, this securing system would be compromised. One solution is to use a securing system that is not dependable on the DUT mechanics. This could be an outside clamp that is a part of the test rack, or at least tightens the DUT to RF tester module against the test rack.

In schematic design, albeit the RF simulations can give information of what is to be expected, this information needs to be checked against experience and theory. There rarely is time to take all aspects into account in the design or simulation phases, and the practical testing may reveal something that was not thought of in the design phase. Therefore, it is always important to try to think ahead of what the unforeseen issue might be (i.e. what could go wrong). This way it will be easier to find a solution, should the unexpected happen.

Although the design of this thesis can be used in RF testing of the present hardware solutions, the evolution of the communication systems is continuous and with the transition to higher frequencies, the design of this thesis will also demand further development.

8 SUMMARY

In this master's thesis, RF tester module for Propsim channel emulator RF module test system was developed. Firstly, the device to be tested was presented. The need for the modular testing was established and justified based on the complexity and high performance demands of the device to be tested.

Next, the general development procedure of RF hardware was presented, which was followed by requirements for the RF test system and the RF tester module. Based on these RF requirements, the RF tester module was designed. This design process included the schematic design of the RF tester module switching network and the peripheral components that enable the operation of the design. A PCA layout review was part of the design work.

Lastly, the verification and validation of the designed RF tester module was performed. This included bare board testing of the PCA as far as it was feasible in the R&D laboratory. After this, the calibration of the RF tester module was done, and the RF performance was reflected to the requirements and simulations of the design phase. It was concluded that with some discrepancy in the DC operation of the chosen PA and with a minor lack of power level in the higher end of the IFLO signal, the design was suitable for validation in the whole RF test system. When running the RF tests on the RF module, the lack of power level in the IFLO signal was found out to cause some false fails. This caused a delay in the proper yield level setting of the RF test system.

After iterating the measurements and setting the RF power levels in the test program to reflect the calibration power levels correctly, the RF tester module was found out to work adequately in the RF test system, and the required tests could be performed on the RF module.

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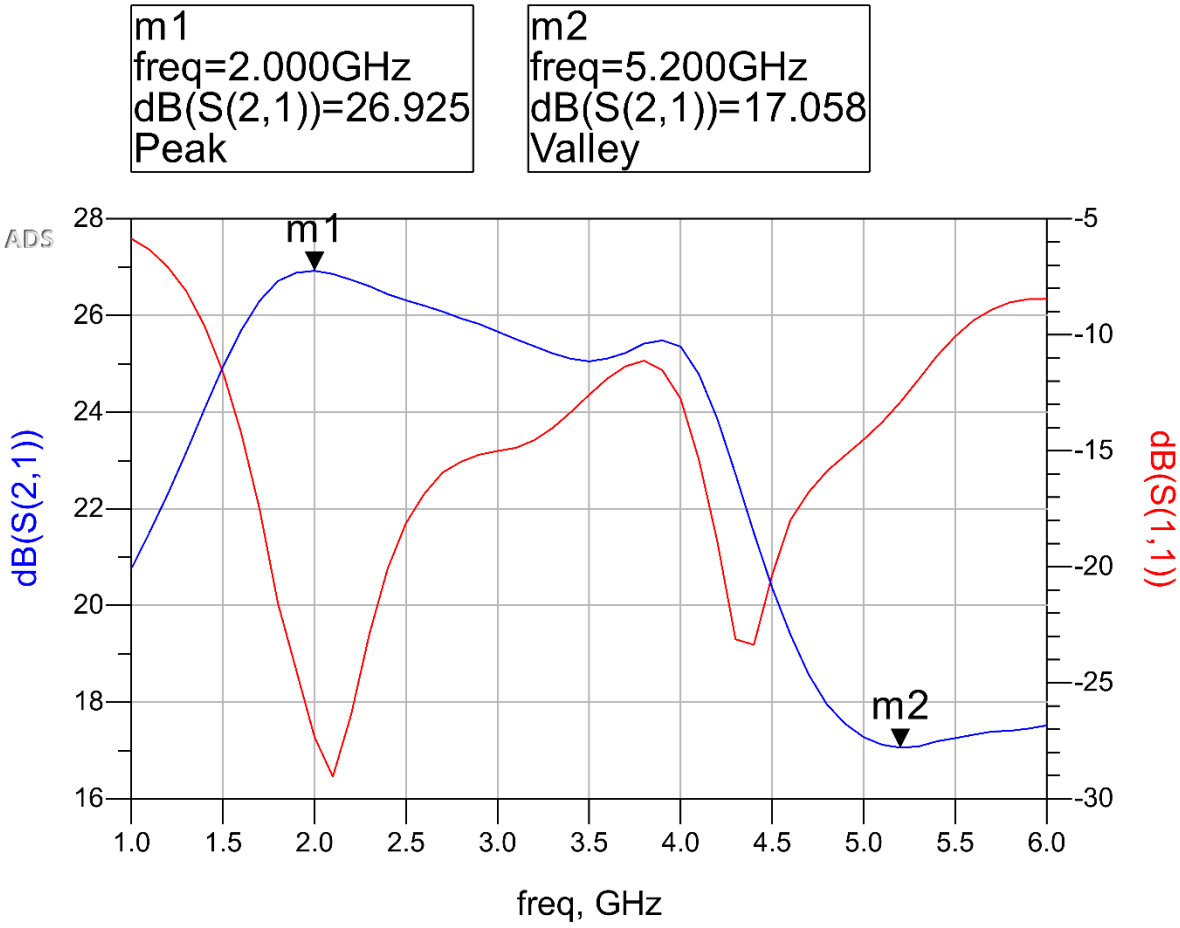
10 APPENDICES

Appendix 1 IFLO simulation results
Appendix 2 RFLO simulation results

Appendix 1 IFLO simulation results



Appendix 2 RFLO simulation results