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A New Boost Switched Capacitor Seven-Level Grid-Tied Inverter

Yang Gao [1], Weichi Zhang [2], Yahya Naderi Zarnaghi [3,4], Naser Vosoughi Kurdkandi [4], Chenming Zhang [2]

[1]School of Mechanical and Automotive Engineering, Yangzhou Polytechnic Institute, Yangzhou, China
[2] School of Engineering, Newcastle University, Newcastle upon Tyne, NE1 7RU, United Kingdom
[3] Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom
[4] Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran
Corresponding Author Email: weichi.zhang@ncl.ac.uk

Abstract: In this paper, a new switched capacitor-based multilevel inverter structure is suggested. The proposed topology can generate seven-level output voltage waveform using ten power electronic switches and two floating capacitors. This structure has the ability to boost the input DC voltage, up to 1.5 times. Although this topology can generate an output waveform with large number of levels, it does not increase the voltage stress on the power electronic switches. There is no need for capacitor voltage balancing in this structure since the capacitors are balanced through charging and discharging modes of operation. In addition, the suggested switched capacitor inverter reduces the number of input dc power supplies and uses a single dc source such as a Photovoltaic (PV) panel. Since the proposed inverter is an NPC based multilevel inverter topology, the leakage current is minimized and as a result the overall efficiency of the proposed system is increased. The operation modes and steady-state analysis of the proposed structure are explained in detail. In order to validate the feasibility of the proposed topology, some experimental results are presented in the grid connected mode of operation.

1. INTRODUCTION

Multilevel inverters have been a popular division of inverters for power conversion systems since it has been introduced in early 80s [1]. Basically, the multilevel inverters can be classified to three categories of, cascaded H-bridge inverters (CHB), flying capacitors (FC) and neutral point clamped inverters (NPC). Multilevel inverters are more efficacious than the conventional two-level inverters in generating high voltages output using lower rating elements. These inverters by the way, have some drawbacks such as, the need for a greater number of power electronic switches and supply sources and complex control methods. Multilevel inverters generate a staircase output voltage waveform, similar to a sinusoidal waveform and has a higher power quality compared with conventional inverters [2-4]. Multilevel inverters have several merits, one of which is minimizing total harmonic distortion (THD) of the output voltage waveform which is performed without increasing the switching frequency or decreasing overall efficiency of the system. In multilevel inverter topologies, as the number of output voltage levels increase, the total harmonic distortion decreases. As the loads are getting more sensitive and the customers are getting more concerned about the quality of power, the power electronic devices should be prepared for the new conditions [5-8]. In simple, compared with the conventional bipolar inverters, multilevel inverters have lower amount of harmonics at the output voltage waveform and is one of the best solutions to improve the power quality of the inverters. Meanwhile, these kind of multilevel inverters have not prevented the interest of improved structures [2, 9], that seeks higher efficiency, an enhanced number of generated output voltage levels, and optimized number of circuit components. It is worth mentioning that multilevel inverter structures mentioned above also have some disadvantages such as high voltage stress on power switches, capacitor voltage imbalance, absence of voltage boosting feature, and requirement of multiple power dc supplies. The CHB well visible in the literate, is a superior structure with increasing popularity for high and medium power applications because of its modular structure. On the other hand, new modules have been suggested to translocate only the H-bridge module to produce more output voltage levels with lower number of power electronic switches and derivers [10]. Recently, a symmetrical five-level sub module has been recommended in [11], which can produce several dc voltage levels with less number of power switches across H-bridge. Nevertheless, the same number of galvanically isolated sources was needed as in a conventional CHB. Accordingly, some presented papers support utilizing of asymmetrical structures in order to decrease the number of input dc sources. To address this issue, in [12] a new 15-level structure that uses four unequal dc power supplies is suggested. A module combining two T-type converters connected through four extra power switches, generating 7-level output voltage waveform is presented in [13]. Recently, several switched capacitor multilevel inverter topologies have been presented and attracted the attention of researchers [14-17]. This is due to their ability of boosting voltage by switching the utilized capacitors in series and parallel states with the input voltage dc sources instead of using a dc-dc boost converter or a bulky transformer. To maximize the output voltage level number, with lower count of power electronic elements, structures based on hybrid inverter have been presented. In hybrid structures, different conventional multilevel inverters are connected in series and parallel or cascaded connections. In general, the switched capacitor multilevel inverters use fewer number of circuit elements in comparison to conventional multilevel inverters. These topologies do not have the issues of capacitors voltage balancing through the periodically charging the capacitor to a reference value. This makes it possible to generate the higher number of output voltage levels using only one dc voltage input source. A new seven-level inverter structure with two asymmetrical dc power supplies has been suggested in [18]. This topology cannot guarantee the stability of the clamped capacitor voltage in steady-state and dynamic situations. A new single dc source cascaded seven-level inverter has been presented in [19] which needs complex control loops to balance the capacitors voltage is presented in. Another new structure of seven-level active neutral point clamped inverter has been presented in [20]. The disadvantage of this structures is that, it requires a large number of dc sources, to generate a higher number of output levels. Several modulation techniques such as carrier phase shift modulation, carrier disposition modulation, space vector modulation pulse width modulation (PWM) have been presented for multilevel inverter topologies [21, 22]. Although space vector PWM method enhances the output power quality by increasing the number of output voltage levels, it increases the number of basic vector. The increase in number of basic vectors, adds to the control complexity through introducing redundant switching states, which is not appropriate for 7-level inverters. The phase opposition disposition modulation technique is utilized in [23] to improve the operation of seven-level active neutral point clamped inverter. To have the modulation on mixed cascaded seven-level inverter, the SPWM technique with a single carrier is presented in [24]. In order to produce the gate pulse of the utilized power switches, two reference signals with opposite magnitude values are utilized in [25]. The total harmonic distortion (THD) of the output voltage waveform is lower and therefore the quality of output voltage waveform is higher, however the efficiency of the inverter is low. Recently, switched capacitor based multilevel inverters with ability to boost voltage and self-voltage balancing have been recommended in [26, 27]. These structures have two stages, combining a switched capacitor dc-dc converter with an H-bridge. Having the H-bridge in the structure, it present an inherent impropriety of cascaded multilevel inverters, i.e., the need for multiple isolated power dc supplies [14]. To overcome the mentioned disadvantage of multilevel inverters to have high voltage stress on the power electronic switches, in this paper a new multilevel inverter based on switched-capacitor topology is presented. This topology generates a seven-level output voltage waveform with voltage boosting capability having lower voltage stress across the power switches. The capacitor's voltage can be balanced without any complex control loop (with capability to self-balance the voltage). In order to produce a seven-level output voltage waveform, a single dc source is used in this structure. Rest of this paper is organized as follows; the proposed boost switched capacitor seven-level inverter is fully described in section II, and its operation modes are presented in section III. Ripple of utilized capacitor voltage is determined in section IV. Section V carries out a comprehensive comparison of proposed topology with other structures. To validate the accurate performance of the proposed switched capacitor inverter, some experimental results are obtained when it is tied to grid and these results will be presented in Section VI of this paper, last but not the least is the conclusion drawn in final section.

II. PROPOSED BOOST SWITCHED CAPACIOTR SEVEN LEVEL INVERTER

The proposed switched capacitor inverter is shown in Fig. 1, in which 10 power electronics switches are used to control two floating capacitors C_1 and C_2. It should be mentioned that all of the power switches are unidirectional expect switches S_5 and S_8. The proposed structure can be applied to the photovoltaic systems where the PV panel is assumed as the input dc source of the inverter. It should be noted that the proposed inverter is based on NPC topology, thus the common mode voltage is limited to half of dc-link voltage. Therefore, the common mode voltage is fixed which leads to reduced leakage current. Regarding the mid-point of dc-link capacitors, the suggested inverter administers to produce seven levels of output voltages with levels of $0.5V_{dc}$, V_{dc}, $1.5V_{dc}$, 0, $-0.5V_{dc}$, $-V_{dc}$, $-1.5V_{dc}$.

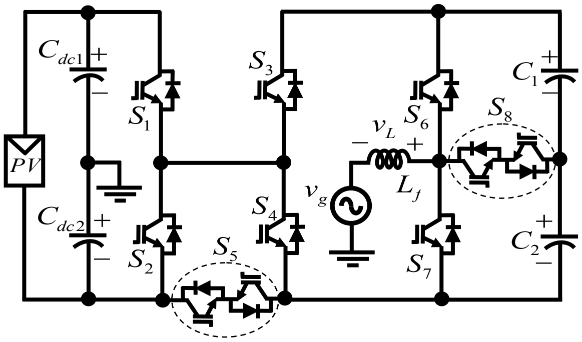


Fig.1. *Proposed 7-level switched capacitor boost inverter*

III. OPERATION MODES OF PROPOSED SEVEN-LEVEL INVERTER

In this section, the operation modes of the proposed topology are described in detail. The states of the switches S_1 to S_8 are presented in Table I and the ideal seven-level output voltage waveform is shown in Fig. 2.

Table I. Switching state

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Switch/level
1st	1	0	0	1	0	1	0	0	$1.5V_{PV}$
2nd	1	0	0	1	0	0	0	1	V_{PV}
3rd	1	0	1	0	1	1	0	0	$0.5V_{PV}$
4rth	1	0	1	0	1	0	0	1	0
5th	1	0	1	0	1	0	1	0	$-0.5V_{PV}$
6th	0	1	1	0	0	0	0	1	$-V_{PV}$
7th	0	1	1	0	0	0	1	0	$-1.5V_{PV}$

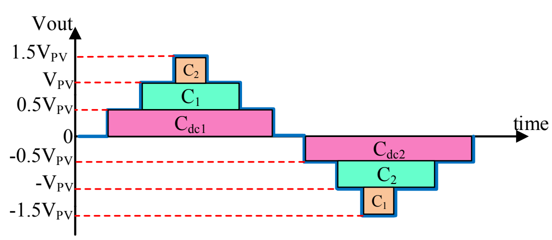


Fig.2. *Ideal seven-level output waveform*

Regarding Fig.2, it can be seen that the capacitor C_{dc1}, is in the output current path and transfers the power to the output, therefore capacitor C_{dc1}, is being discharged during and capacitor C_{dc2}, is being charged in this positive half-cycle. During the negative half cycle, capacitor C_{dc2}, is in the output current path and transfers the power to the grid while in the output current path and transfers the power, therefore capacitor C_{dc1}, is being charged in this half-cycle. Considering the mentioned facts, the charging time for capacitor C_{dc1} and capacitor C_{dc2} is the same which leads to natural balancing of capacitors. Similar to what is explained for Capacitors C_{dc1} and C_{dc2}, from Fig.2, it can be seen that Capacitors C_1 and C_2 are in the output current path for the same period of time. In other words, capacitor C_1, supports the generation of output voltages $+V_{PV}$ and $+1.5V_{PV}$, in the positive half-cycle while capacitor C_2 is being utilized in the same half cycle and is and is in the output current path while generating $+1.5V_{pv}$. As in the positive half-cycle, in the negative half-cycle, capacitor C_1 is utilized when generating $-1.5V_{PV}$ voltage and capacitor C_2 is being utilized for generating $-V_{PV}$ and $-1.5V_{PV}$. So it is clear that the Capacitors C_1 and C_2 are in the output current path for the same amount of time which leads to natural balancing of these capacitors. As a general note, it could be said that, since the operation of the circuit is symmetrical in the negative and positive half-cycle, the capacitor charging will be done in a balanced way naturally.

The equivalent electrical circuit of each operation mode is separately shown in Fig. 3 and Fig. 4. In these figures, the blue and red paths indicate charging direction of the capacitors and injected current to power grid respectively. In this topology each utilized capacitors is charged to half of V_{PV}. The operation modes of this topology are classified as follow;

Positive half-cycle

A) *First operation mode 0 V_{pv}*

The equivalent circuit of this mode is indicated in Fig. 3 (a). Considering this figure, it can be understood that the switches S_1, S_3, S_5 and S_8 are in ON-state. Therefore, the output voltage of the proposed inverter is equal to zero (V_{out}=0). It should be noted that during this mode, the capacitors C_1 and C_2 are in parallel with the input dc power supply. Each floating capacitor is charged to half of the input dc power supply $(V_{C1} = V_{C2} = V_{PV}/2)$. This guarantees the self-balancing of capacitors voltages.

In this mode the switches S_2, S_4, S_6, and S_7 are in OFF-state. The standing voltage of these switches can be obtained as follows:

$$V_{S4} = V_{S2} = V_{PV} \tag{1}$$

$$V_{S6} = V_{C1} = 0.5V_{PV} \tag{2}$$

$$V_{S7} = V_{C2} = 0.5V_{PV} \tag{3}$$

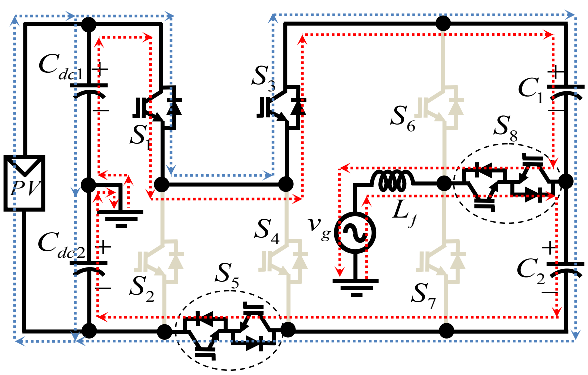
Also, in this mode the generated output voltage of the proposed switched capacitor inverter is equal to zero.

B) Second operation mode 0.5 V_{pv}

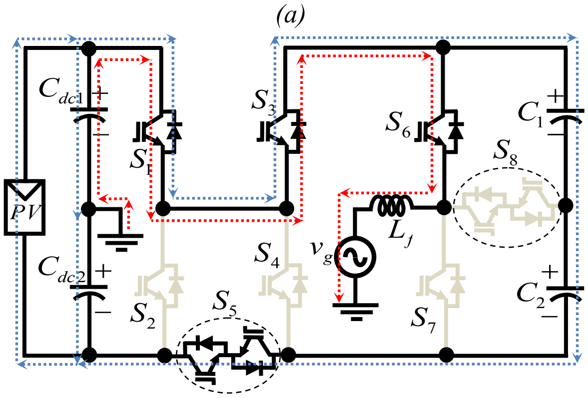
The electrical circuit of this mode is shown in Fig. 3 (b). In this mode, as in the previous mode, the capacitors are in parallel with the input source and are being charged to half of the input dc voltage $(V_{C1} = V_{C2} = V_{PV}/2)$ Considering Fig. 3 (b), it can be seen that, the switches S_1, S_3, S_5 and S_6 are in ON-state and the amplitude of generated output voltage level of the inverter is equal to 0.5 V_{PV}. In this mode, the switches S_2, S_4, S_7, and S_8 are in OFF-state. The standing voltage of these switches can be calculated as follows:

$$\begin{cases} V_{S2} = V_{S4} = V_{dc1} + V_{dc2} \\ V_{dc1} = V_{dc2} = 0.5V_{PV} \end{cases} \Rightarrow V_{S2} = V_{S4} = V_{PV} \tag{4}$$

C) Third operation mode 1V_{pv}



(a)



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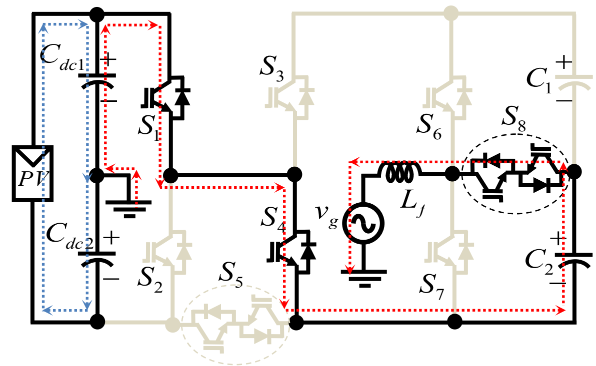

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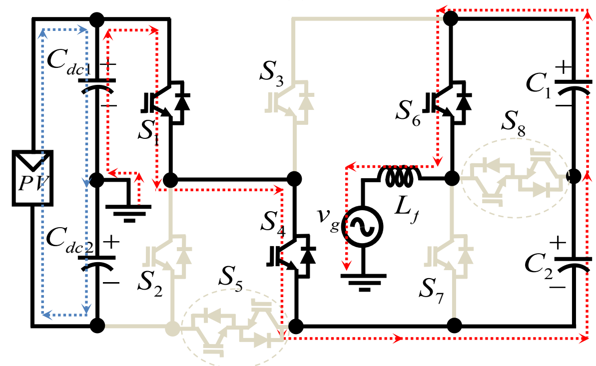
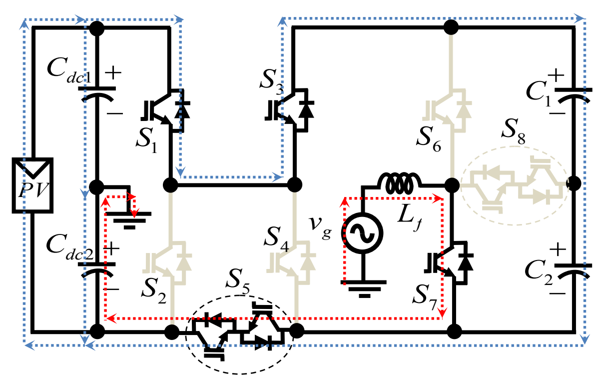
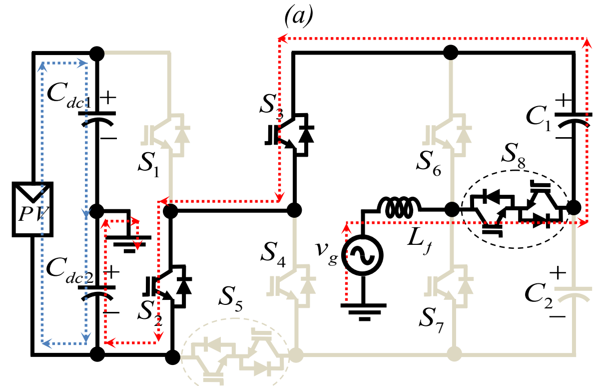


(d)

Fig. 3. *Operation modes in the positive half cycle: a) first operation mode, (b) second operation mode, (c) third operation mode, (d) forth operation mode*



(a)



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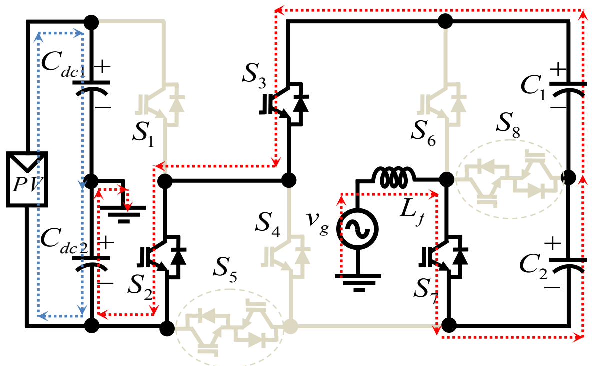


(c)

Fig.4*. Operation modes in the negative half-cycle: (a) fifth operation mode, (b) sixth operation mode, (c) seventh operation mode*

Fig. 3 (c) indicates the equivalent electrical circuit of the third operation mode, where the produced output voltage level equals to V_{PV}. The switches S_1, S_4, and S_8 should be turned on in this mode. So that the capacitor C_{dc1} and capacitor C_2 are connected in series and then discharged to the output. Therefore, the amplitude of produced out voltage level is equal to the sum of these mentioned capacitors voltage.

The standing voltage of switches can be achieved as:

$$V_{S2} = V_{S3} = V_{S5} = V_{PV} \tag{5}$$

$$V_{S6} = V_{C1} = 0.5V_{PV} \tag{6}$$

$$V_{S7} = V_{C2} = 0.5V_{PV} \tag{7}$$

D) Forth operation mode 1.5V_{pv}

Fig. 3(d) depicts the equivalent circuit of the fourth operation mode with the capacitor charging path and the path of injected current to the grid. In this mode, the switches S_1, S_4, S_6 are in ON-state. Under this condition, the capacitors C_{dc1}, C_1, and C_2 are in series connection and the total energy of all three capacitors is transmitted to the output of the proposed inverter. In this mode, amplitude of the generated output voltage level is equal to 1.5 V_{PV}.

$$\left(V_{out} = V_{C1} + V_{C2} + V_{dc1} = 1.5V_{PV}\right) \tag{8}$$

The standing voltage of switches can be obtained as:

$$V_{S2} = V_{S5} = V_{dc1} + V_{dc2} = V_{PV} \tag{9}$$

$$V_{S3} = V_{S7} = V_{C1} + V_{C2} = V_{PV} \tag{10}$$

Negative half-cycle

A) *Fifth operation mode -0.5V_{pv}*

The electrical circuit of this mode is shown in Fig. 4 (a), in which switches S_1, S_3, S_5, and S_7 are in ON-state in order to generate first output level of output voltage waveform in the negative half cycle. When the switch S_1, S_3, and S_5 are in ON-state, the capacitors C_1 and C_2 are connected in parallel with the input dc source. Therefore, each of mentioned capacitor are charged to half of the input dc source $\left(V_{C1} = V_{C2} = V_{PV}/2\right)$. By turning on the switch S_5 and S_7 the energy of capacitor C_{dc2} is discharged to the output of the inverter through the current path which is shown in red. In this mode the first level of the negative half cycle is generated. Also, the switches S_2, S_4, S_6, and S_8 are in OFF-state. Therefore, the standing voltage of these switches can be calculated as:

$$V_{S2} = V_{S4} = V_{dc1} + V_{dc2} = V_{PV} \tag{11}$$

$$V_{S6} = V_{C1} + V_{C2} = V_{PV} \tag{12}$$

$$V_{S8} = V_{C2} = 0.5V_{PV} \tag{13}$$

B) *Sixth operation mode -1V_{pv}*

Fig. 4 (b) shows the electrical circuit of this mode, which is to generate second level of output voltage waveform in the negative half cycle. This is achieved through switching the power switches S_2, S_3, and S_8 to ON-state. By turning on of the S_2 and S_3, the capacitors C_1 and C_{dc2} are in series connection. Meanwhile, the switches S_1, S_4, S_5, S_6, and S_7 are turned off. The standing voltage of these switches can be written as follows:

$$V_{S1} = V_{dc1} + V_{dc2} = V_{PV} \tag{14}$$

$$V_{S6} = V_{C1} = 0.5V_{PV} \tag{15}$$

$$V_{S4} = V_{S5} = V_{C1} + V_{C2} = V_{PV} \tag{16}$$

$$V_{S7} = V_{C2} = 0.5V_{PV} \tag{17}$$

C) *Seventh operation mode -1.5V_{pv}*

Fig. 4 (c) shows the equivalent circuit of the seventh operation mode. This mode will generate the third level of the output voltage waveform in the negative half cycle. In order to obtain this output level, the switches S_2, S_3, and S_7 are in ON-state, whilst other switches remain OFF-state as can be seen in this figure. Standing voltage of the switches can be calculated as:

$$V_{S1} = V_{dc1} + V_{dc2} = V_{PV} \quad (18)$$

$$V_{S4} = V_{S5} = V_{C1} + V_{C2} = V_{PV} \quad (19)$$

$$V_{S6} = V_{C1} + V_{C2} = V_{PV} \quad (20)$$

$$V_{S8} = V_{C2} = \frac{V_{PV}}{2} \quad (21)$$

IV. CALCULATION OF CAPACITOR VOLTAGE RIPPLE

The grid current in the proposed structure is divided into two dc-link capacitors with the same capacitance. This will lead to have the same average voltage on the capacitors. Voltage ripple of the capacitors of dc-link (V_{ripple}) can be calculated as:

$$V_{ripple} = 2V_{C,dc,P} \quad (22)$$

Here, $V_{C,dc,P}$ is the peak voltage of the dc-link capacitors. Considering a sinusoidal grid current, the voltage ripple can be rewritten as follows:

$$V_{ripple} = \frac{I_p}{(100\pi).C_{dc}} \quad (23)$$

Where I_P is the peak fundamental grid current. The capacitance of both utilized capacitors are the same.

$$C_{dc} = C_{dc_1} = C_{dc_2} \quad (24)$$

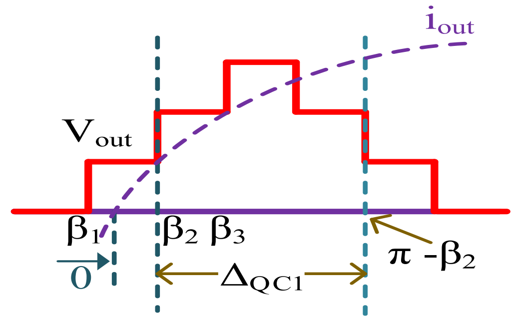


Fig. 5. *Discharging current of C_1 during positive half cycle*

In the other words, in order to calculate the voltage ripple of utilized capacitors C_1 and C_2, longest continues discharging period of the utilized capacitors are considered. With respect to Fig. 5, the integration of grid current from β_2 to $\pi - \beta_2$, electric charge flowing out from capacitor C_1 can be calculated as:

$$\Delta Q_{C_1} = \frac{1}{100\pi} \int_{\beta_2}^{\pi-\beta_2} I_p \sin(\omega t - \theta) d\omega t \quad (25)$$

Since the capacitor electric charge has a linear relation with capacitor voltage ($Q = CV$), the voltage ripple equation can be written as follows.

$$\Delta V_C = \frac{2I_p \cos(\beta_2)}{(100\pi).C} . \cos(\theta) \quad (26)$$

Where, $\cos(\theta)$, indicates the power factor (PF). It should be noted that, the capacitance value of floating capacitors C_1 and C_2 are the same.

$$C_1 = C_2 = C \quad (27)$$

Table II. Comparison of the proposed topology with other structures

Topologies	Number of switches	Number of diodes	Number of output levels	N. of floating capacitors	Voltage boosting capability	Stress voltage on switches are within V_{dc}
[28]	14	-	7	2	No	Yes
[29]	16	-	7	1	No	Yes
[26]	10	1	9	2	Yes	No
[27]	12	-	7	1	No	Yes
[30]	9	2	9	2	Yes	No
[31]	12	-	9	3	Yes	No
[32]	8	-	7	1	No	Yes
[33]	7	2	5	1	No	Yes
[23]	18	-	7	2	No	Yes

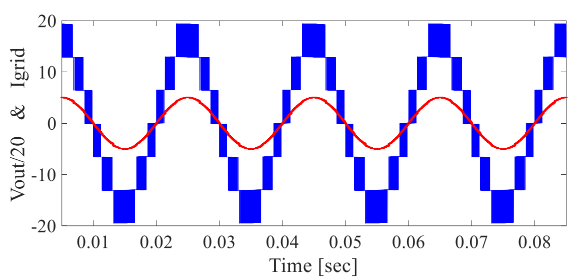
proposed	10	-	7	2	Yes	Yes

V. COMPARISION RESULTS

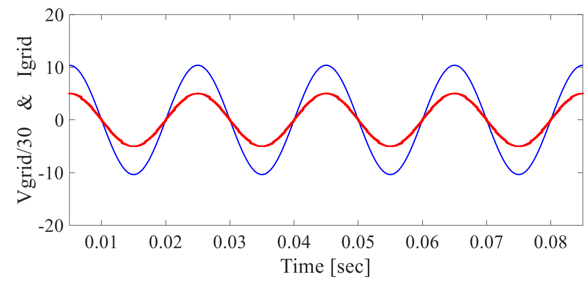
The proposed switched capacitor boost inverter is compared with most recent topologies and the summary of this comparison is presented in Table II. This comparison is made in terms of number of generated output voltage levels, utilized power switches, diodes, floating capacitors, voltage boosting capability, and standing voltage of power switches. Multilevel inverter structures ensures low voltage stress on power electronic switches [26], [33], with lack of voltage boosting capability. Considering Table II, in all of the presented topologies, voltage stress on power switches are equal to V_{dc} expect topologies [26], [31], and [32]. Consequently, the proposed topology in this paper can offer benefits not only in voltage boosting capability, it also mitigates the standing voltage on the switches, thus improving the lifetime of the devices.

VI. SIMULATION RESULTS

In this section, simulation results of MATLAB/Simulink are presented for the 7-level inverter, in this simulation, the peak input voltage magnitude is assumed to be 266 volts. 7-level output voltage with a peak magnitude of 400 volts with sinusoidal grid injected current with unity power factor is presented in Fig.6 (a). The proposed topology can also support the grid reactive power, therefore, grid injected current with output inverter voltage with different power factor are presented in Fig. 6(b), Fig. 6(c) and Fig. 6(d).



(a)



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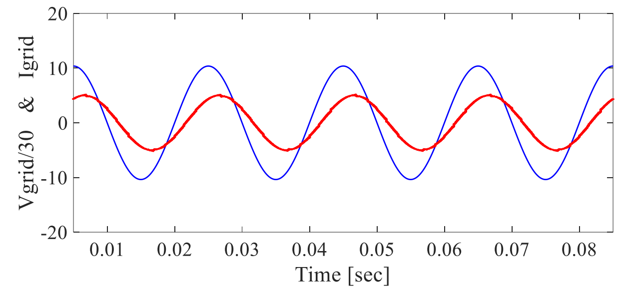

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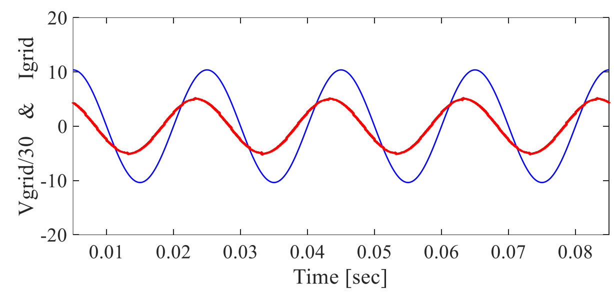
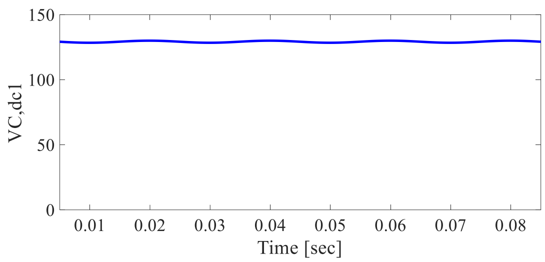


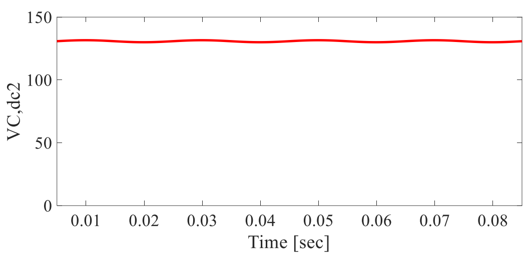
(d)

Fig.6. *(a) Inverter output voltage with sinusoidal grid current (b) Grid Voltage and current with unity power factor (c) Grid Voltage and current with lagging power factor (d) Grid Voltage and current with leading power factor*

Voltage waveforms of capacitors $C_{dc,1}$, $C_{dc,2}$, C_1, C_2, are shown in Figs 7. (a), (b), (c), (d). Regarding the presented waveforms, it could be seen that the capacitor voltage is adjusted to half of the input voltage and the capacitor voltage ripples are in an acceptable range.



(a)



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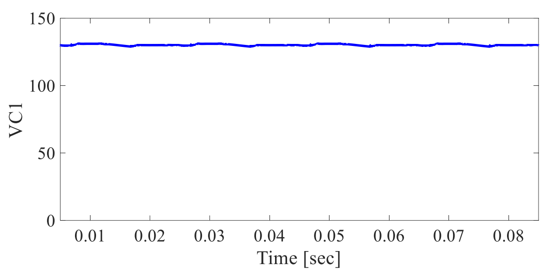

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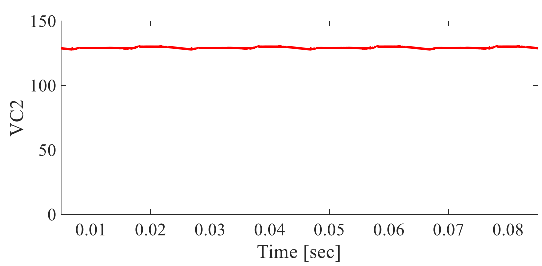
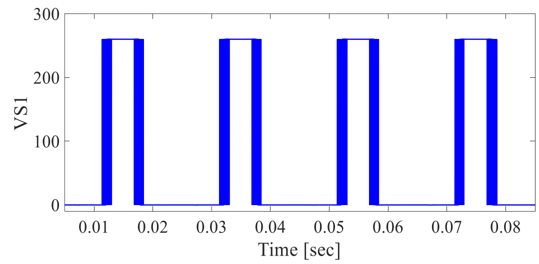


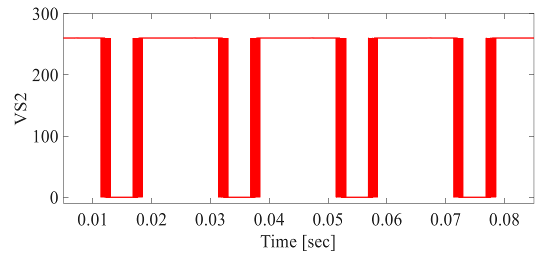
(d)

Fig. (7). *Utilized capacitor's voltage (a) Capacitor $C_{dc,1}$ (b) Capacitor $C_{dc,2}$ (c) Capacitor C_1 (d) Capacitor C_2*

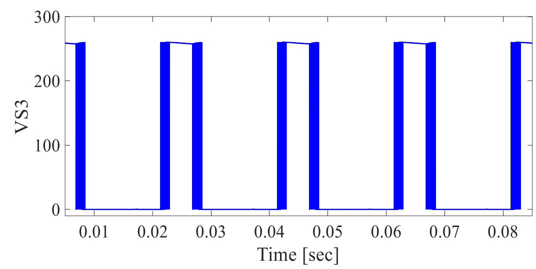
In addition, the voltage stress of the utilized switches S_1~S_4 are presented in Fig 8 (a) - (d), respectively. Also, the voltage stress of power switches S_5~S_8 are indicated in Fig. 9(a)-(d), respectively. Regarding the simulation results of voltage stress for switches S_5 and S_8, it could be understood that the voltage stress on the mentioned switches is bipolar, so for the accurate operating of the proposed topology, switches S_5 and S_8, should be composed of two back to back IGBTs.



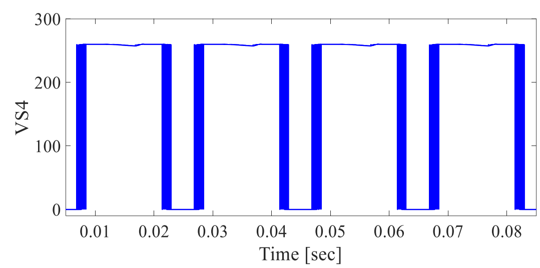
(a)



(b)

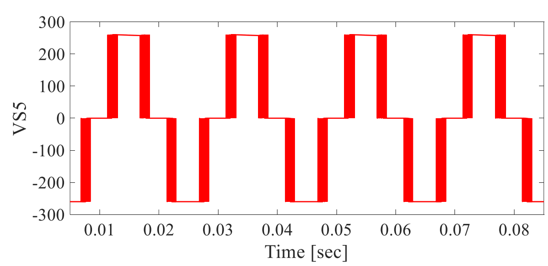


(c)

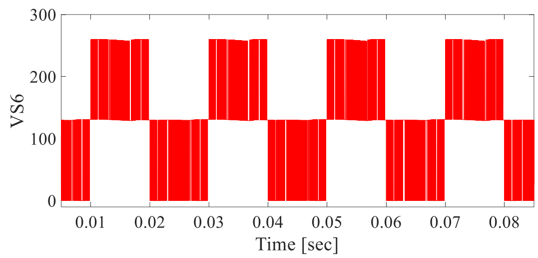


(d)

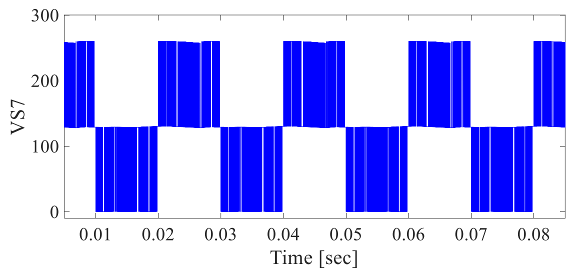
Fig. 8. *The voltage stress of (a) Switch S_1 (b) Switch S_2 (c) Switch S_3 (d) Switch S_4*



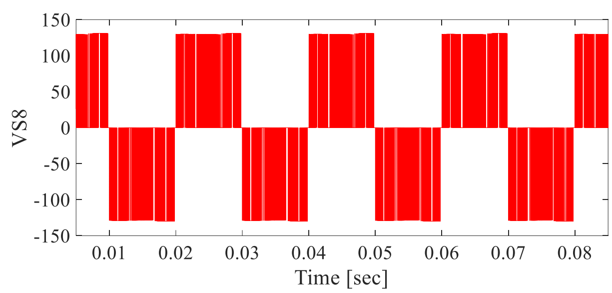
(a)



(b)



(c)



(d)

Fig. 9. The voltage stress of (a) Switch S_5 (b) Switch S_6 (c) Switch S_7 (d) Switch S_8

VI. EXPERIMENTAL RESULTS

Table III. *Details* of utilized elements and prototype specifications

Circuit Element	Type	Explanation
S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8	47N60C	650 V/47 A
Gate Driver	TLP 250	IC
Current transducer	LA55P	Hall effect Sensor
Microcontroller	Beagle Bone Black	ARM Cortex-A8
Grid frequency	50 Hz	
Sampling frequency	40 KHz	
C_1, C_2, C_{dc1}, C_{dc2}	Electrolytic	$2200\mu F$
L_f	Ferrite Core	1.5 mH

Experimental results are presented to validate the performance of the proposed switched capacitor inverter. A photograph of the proposed inverter prototype is depicted in Fig.10. Details of used elements and prototype specifications are presented in Table III. Since $2200\mu F$ is a standard commercial capacitor, the voltage ripple for capacitors C_{dc1} and C_{dc2} could be calculated based on following equation:

$$V_{ripple} = \frac{I_p}{(100\pi).C_{dc}} \tag{28}$$

It is worth mentioning that in this equation, I_P is the peak grid injected current and is equal to 5 Amps, therefore;

$$V_{ripple} = \frac{I_p}{(100\pi).C_{dc}} = \frac{5}{100\times\pi\times 2200\times 10^{-6}} = 7.24V \tag{29}$$

So the voltage ripple for capacitors C_{dc1} and C_{dc2} could be calculated as 7.24 Volts which is a reasonable value for the voltage ripple and could also be confirmed by the experimental results. Therefore, it could be said that 2200 Micro Farad is an appropriate value for the capacitors C_{dc1} and C_{dc2}.

In order to calculate the C_1 and C_2 capacitors value,

Since 2200 Micro farad is a standard commercial capacitor, the voltage ripple for capacitors C_1 and C_2 could be calculated based on following equation:

$$\Delta V_C = \frac{2I_P \times \cos(\beta_2)}{100\pi \times C} \times \cos(\theta) = \frac{2\times 5\times 0.866}{100\pi \times 2200\times 10^{-6}} \times 1 = 12.53V \tag{30}$$

So the voltage ripple for capacitors C_1 and C_2 could be calculated as 12.53 Volts which is a reasonable value for the voltage ripple and could also be confirmed by the experimental results. Therefore, it could be said that $2200\mu F$ is an appropriate value for the capacitors C_1 and C_2.

To verify the feasibility of the proposed inverter for grid-connected applications, experimental results are obtained in grid-connected operating mode. It is worth mentioning that the current control technique in [9, 34, 35] is used to generate the gate pulses of switches. In single-phase grid-connected inverters which are connected to a grid with 220 Volts RMS voltage, it is recommended for inverter to have an output of 360 to 400 volts. Since in this topology, the inverter output will be 1.5 times of input voltage, in order to have a 400 Volts output voltage, the input voltage should be 266 Volts. The input dc power supply used in the tests has an amplitude of 266 V. The seven-level output voltage waveform of the inverter with a peak value of 400 V and a sinusoidal output grid-injected current at the unity power factor (PF=1) are shown in Fig. 11(a). Regarding this figure, the grid injected power could be calculated from below equation

$$\begin{cases} P = \frac{1}{2} V_{g,\max} . I_{g,\max} . \cos(\theta) \\ \cos(\theta) = 1 \end{cases} \tag{31}$$

In which, $V_{g,\max}$ and $I_{g,\max}$ represent the maximum voltage and current of the grid, respectively, which are $220\sqrt{2}$ Volts and % Amps for the proposed topology. Replacing the mentioned values in (31), the grid injected power is calculated to be 0.77 kW. In order to verify the balanced voltage waveform of the utilized capacitors, the voltage across the capacitors C_{dc1}, C_{dc2} and C_1, C_2 are presented in Fig. 11(b) and (c) respectively. Considering this figure, it is clear that the capacitors have been balanced to half of input dc power supply value (V_{dc1}=V_{dc2}=113V, V_{C1}=V_{C2}=113V). Also, the voltage ripple of the utilized capacitors has an acceptable value.

The proposed inverter will also provide the reactive power support to the grid. In other words, the current injected to the grid can be in phase with grid (PF=1), or under conditions of leading PF and lagging PF. Fig. 12 shows the results of grid voltage and injected current from proposed inverter. Injected current under different power factors from unity power factor (PF=1), to leading PF and lagging PF, are indicated in Fig. 12(a), (b), and (c) respectively. Meanwhile, the standing voltage waveform of used power switches (S_1~S_8) are presented in Fig. 13, in which Fig. 13 (a) shows the standing voltage of switches S_1 and S_2. It is clear that the peak voltage stress across switch S_1 and S_2 is limited to only V_{PV}. The voltage stress on the power switches S_3 and S_6 are indicated in Fig. 13 (b). With respect to this figure, it is clear that the peak value of standing voltage of mentioned switches are equal to V_{PV}.

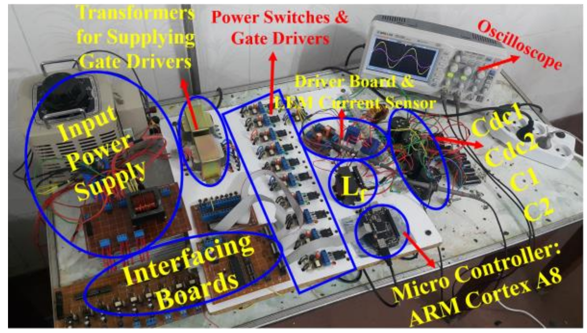
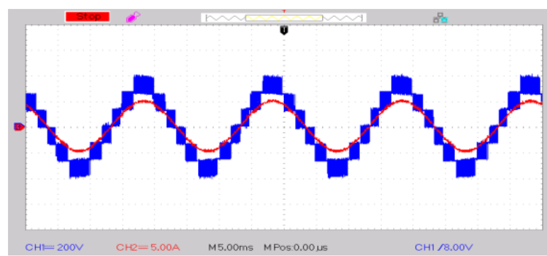
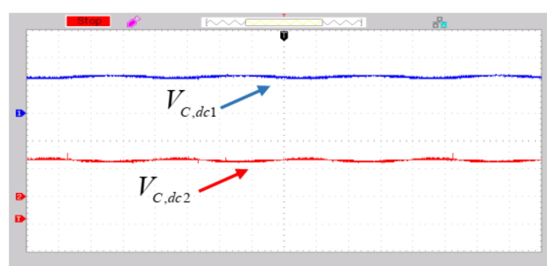


Fig. 10. *Laboratory prototype of the single phase grid tied proposed inverter used in the experiment.*

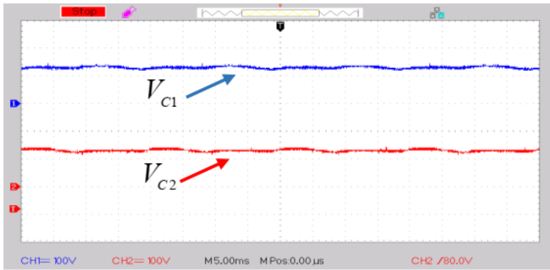
Also, standing voltages of power switches S_4 and S_5 are presented in Fig. 13 (c). The peak voltage stress across the switches S_4 and S_5 was limited to V_{PV}. Fig. 13 (d) shows the standing voltage of switches S_7 and S_8 where the peak standing voltage value for these switches are equal to $0.5V_{PV}$. With respect to this figure, the peak value of standing voltage of used power switches is about 266 V. Therefore, the utilized power switches withstand only friction of peak value of output voltage waveform in their OFF-state mode. Also, standing voltages of power switches S_4 and S_5 are presented in Fig. 13 (c).



(a)



(b)

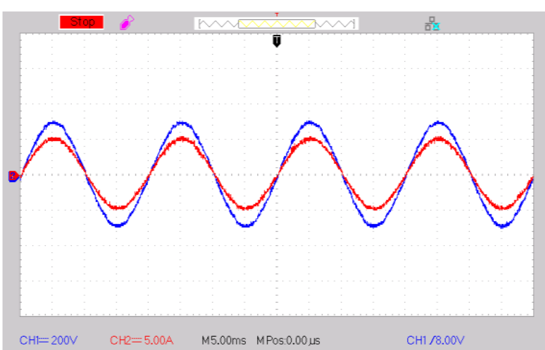


(c)

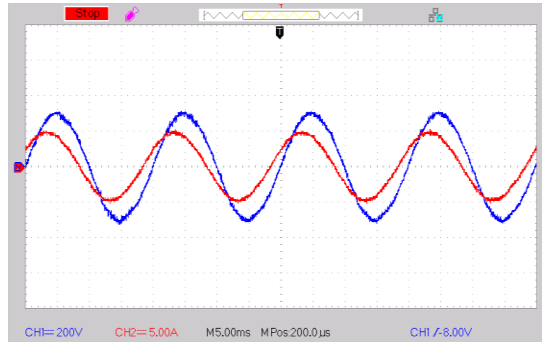
Fig. 11. *Experimental results: (a) Seven-level output voltage waveform of proposed inverter (200V/div) and grid-injected current (5A/div), (b) Voltage across capacitors C_{dc1} and C_{dc2} (100V/div), (c) capacitors C_1 and C_2 (100V/div)*

The peak voltage stress across the switches S_4 and S_5 was limited to V_{PV}. Fig. 13 (d) shows the standing voltage of switches S_7 and S_8 where the peak standing voltage value for these switches are equal to $0.5V_{PV}$. With respect to this figure, the peak value of standing voltage of used power switches is about 266 V. Therefore, the utilized power switches withstand only friction of peak value of output voltage waveform in their OFF-state mode.

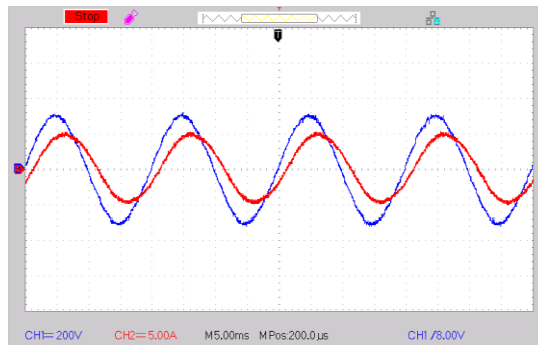
Finally, regarding presented experimental results, the accurate performance and feasibility of the recommended boost switched capacitor seven-level inverter for grid-connected applications is validated, which is also in good agreement with the provided mathematical analysis for the proposed topology. Also, comparing the results confirms the similarity between simulation and experimental results.



(a)

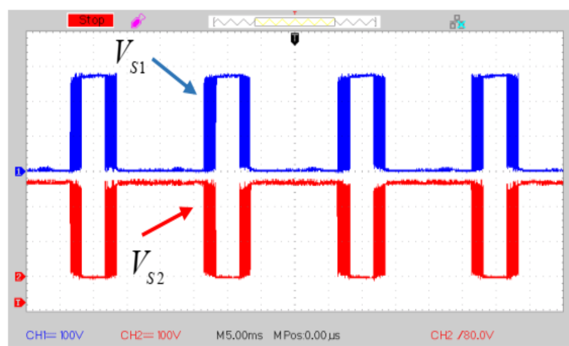


(b)

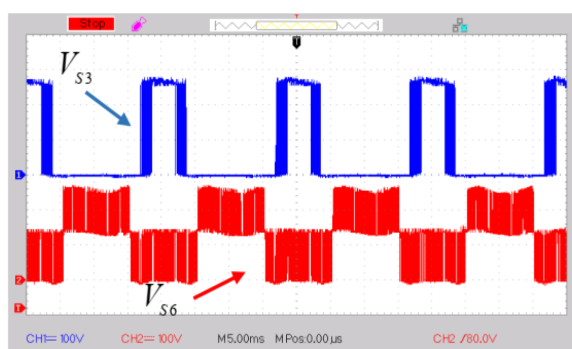


(c)

Fig. 12. *Waveforms of grid voltage (200V/div) and injected grid current (5A/div) under different conditions of power factor; (a) unity PF, (b) leading PF, and (c) lagging PF*



(a)



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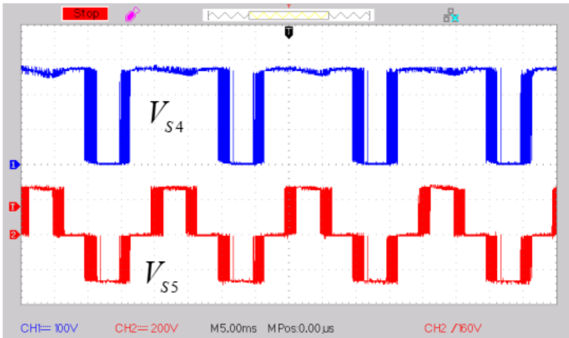
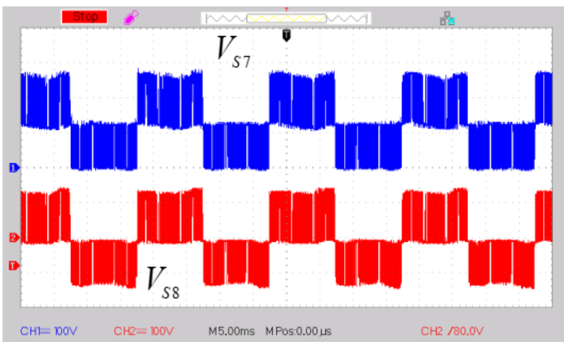


(c)



(d)

Fig. 13. *The standing voltage of utilized power switches (100V/div); (a) V_{S1} and V_{S2}, (b) V_{S3} and V_{S6}, (c) V_{S4} and V_{S5}, (d) V_{S7} and V_{S8}*

VII. CONCLUSION

In this paper, a new switched capacitor seven-level inverter topology with voltage boosting and reactive power support capabilities is presented. This structure combines the benefits of different multilevel inverter structures. The suggested switched capacitor inverter produces seven-level output voltage waveform using only ten power switches and two floating capacitors. The presented topology is grid connected with a significant drop in the leakage current thanks to the NPC topology. The peak value of output voltage is 1.5 times the input dc voltage which validates the boosting capability of the converter. One of the interesting features of proposed switched capacitor multilevel inverter is self-voltage balancing of floating capacitors and single power supply requirement. Moreover, design consideration and standing voltage calculations of the involved power switches have been discussed in this paper. Last but not the least, the feasibility and superiorities of the proposed switched capacitor inverter are compared with most recently introduced switched capacitor structures. Also, to verify the performance of the proposed inverter, experimental results are presented for the grid-connected mode of operation.

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