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No-Isolated High Gain DC/DC Converter with Low Input Current Ripple Suitable for Renewable Applications

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Abstract — **In this paper, a new non-isolated high voltage gain dc/dc converter with low input current ripple is proposed for renewable sources applications. The proposed converter combined SEPIC converter and voltage multiplier cells. In order to achieve high voltage gain, the proposed converter can increase the output voltage level using the voltage multiplier unit. The voltage stress across the semiconductors will be decreased compared to SEPIC, conventional boost converter. Therefore, using only one switch with lower resistance $R_{DS(on)}$, the overall efficiency of the proposed converter is increased significanly. In order to verify the theoretical analysis of the proposed converter and its accurate operation, a 150W prototype operating at 25 kHz is built and tested.**

***Index Terms*—** Non-Isolated, dc/dc converter, Single Switch, High voltage gain, low voltage stress.

1 INTRODUCTION

Nowadays, green sources and renewable power generations are one of the top field research for all countries in power electronics, especially for advanced governments. Since the output voltage magnitude of the renewable sources is usually low, there should be a high voltage gain dc-dc-ac converter for increasing the voltage magnitude and decrease the power losses of the system [1-4]. In the meantime, there are two types of dc-dc boost converters as an interface between the renewable sources and grid. Various high voltage gain dc–dc converter structures have been developed to increase the voltage level by using transformer. Also, the configuration optimally integrates voltage multiplier techniques in these works to achieve an ultra-high step-up gain of voltage conversion with low voltage stress and high efficiency [5, 6]. In fact, by increasing the turn's ratio value of the isolated dc/dc converters, it can create a high voltage level at the secondary side [7, 8]. The topology without coupled inductor techniques can be employed as dc-dc converter to boost the renewable sources voltages. It also other advantages of these structures, such as clamped switched voltage, high voltage gain, isolation of energy source from the load, and positive polarity for output voltage. However, selecting a large turn's ratio value causes to a high leakage inductance, and also can be produced a high voltage spike and high voltage stress across the power semiconductors (MOSFET and diode) [9, 10]. Moreover, the overall cost and volume of the system for isolated dc-dc converter will be high [11]. Many non-isolated structures can be obtained to achieve a high voltage gain with lower duty cycle value which can be solved the volume of the system issues [12]. There are many techniques for increasing the voltage gain of the non-isolated dc-dc converters such as voltage multiplier units (consist of diode-capacitor, switched-inductor), coupled inductor and other ways. The proposed converter is taken from a Dickson charge pump for increasing the voltage gain of the converter [13]. Diode-capacitor voltage multiplier unit (VMU) stages are integrated with two boost stages at the input. The VMU stages are used to increase the major boost in boost stages for obtaining a larger overall voltage gain [14]. The voltage gain of the converter depends on the number of VMU stages and duty cycle value of the input boost stages.

Switched capacitor techniques are used in [15] for increasing the voltage gain of the converter, which is consisting three capacitors and three diodes, is in charge of providing some of upper output voltage level derived on conventional switched capacitor topologies. In [16], a dc-dc converter is proposed based on conventional boost which the main drawbacks of the converter including pulsating input current, a high value of current in the start state and also a large number of power diodes and capacitors are required. In [17], the proposed topology is developed by combining boost and single-ended primary inductor converter with diode-capacitor unit to decrease the voltage stress values across the power switch and diodes. In [18], interleaved structures and coupled inductor techniques are used between the inductors due to increasing the power level and decreasing the cores. As a result, it can be said that these topologies above-mentioned drawbacks are mitigated at the expense of losing ultra-high voltage gain capability of the converter. In [19], a dc-dc converter based on coupled inductor method is presented to achieve a high voltage gain, where the main power switch is affected by leakage inductance and this causes to decrease the voltage gain of the converter. Generally, for limiting the relevant issue, using the active clamp circuit can be a good solution which is presented in [20] based on coupled inductor strategy. In [21], a transformer less current-fed dc-dc converter using

coupled inductor techniques to increase the voltage gain is presented. The input ripple of this converter is very low. Also, to decrease the maximum spike of the power switch is used an active snubber circuit (generated by leakage inductance) which causes to decrease the switching losses. In [22], some dc-dc converter topologies are compared with each other and conventional boost converter. Since, the conventional boost converter have many drawbacks (such as limitation of power level, limitation of increase duty cycle value and semiconductor loses) and it does not have any control over an input current. In fact, a large value of the input current leads to major problems to the power components (by increasing the rating value of the power components). The maximum voltage on power MOSFET is equal to the output voltage in a conventional boost converter. These problems can be easily overcome in modified structures with using extra devices. The modified structures can be improved some parameters as voltage gain, total power loss, overall efficiency and normalized voltage stress across power semiconductors.

In this study, a new dc-dc converter with high voltage gain and lower input current ripple is proposed suitable for renewable applications. The proposed converter uses a single power MOSFET and a combination of diode/capacitor/inductor for increasing the output voltage level. The voltage gain of the proposed structure is higher than the conventional boost and conventional SEPIC converters. In addition, using only one switch causes to decrease the power losses of the power MOSFET which the most power losses of dc-dc converters include semiconductor losses. Since the input current ripple and the output voltage level of the renewable sources are important issues in renewable power generation field, therefore it can be said that the proposed converter can be a good candidate for renewable applications. Performance of the proposed converter is provided in section 2. Finally, a laboratory prototype is built and tested in section 6.

2 PROPOSED CONVERTER AND PRINCIPLE OF OPERATION

Fig. 1 illustrates the power circuit of the proposed converter. The proposed converter is a non-isolated high step-up dc/dc converter using a single switch which consists of the input dc power supply, single switch in the input side and voltage multiplier units (consists of several capacitors, diodes and inductor). For simplify the operation analysis of proposed converter at continuous conduction interval and discontinuous conduction interval, the below assumptions are considered:

- The value of the input voltage is constant.
- All used elements of the proposed converter are ideal.
- All capacitors of the proposed converter are large enough, so the voltage of all capacitors considered constant values in one switching period.

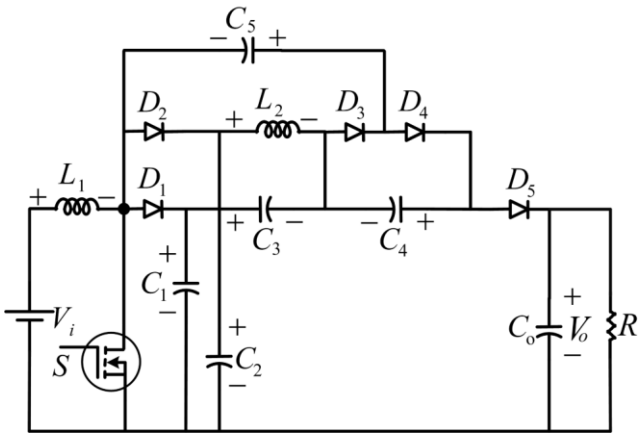


Fig. 1. The power circuit of the proposed converter.

Two time intervals are considered for each power switch in one period. DTs is ON-state time of the switch and (1-*D*)T_s is OFF-state time of the power switch.

2.1 CONTINUOUS CONDUSTION INTERVAL

Fig. 2 illustrates the Equivalent circuit of the proposed converter at this operation. The current of the inductor L_2 is almost considered linearly. Based on Fig. 2, operation states of the converter could be summarized as:

Interval 1 [$t_1 \le t \le t_2$ **]**

In this interval, the power switch (*S*) is turned on and all diodes are reverse biased expect the diode D_4. The inductor L_1 and L_2 are charged by the input power supply (V_i) and the current of the inductors L_1 and L_2 is linearly increased.

Interval 2 [$t_2 \le t \le t_3$ **]**

In this interval, the power switch (*S*) is turned-on and all diodes are reverse biased. The inductor L_1 and L_2 are charged by the input power supply (V_i).

Interval 3 [$t_3 \le t \le t_4$ **]**

In this interval, the power switch (*S*) remains on and all diodes are reverse biased expect the diode D_3. The inductor L_1 and L_2 are charged by the input power supply (V_i).

Interval 4 [$t_4 \le t \le t_5$ **]**

In this interval, the power switch (*S*) is turned-off and all diodes are conducting expect the diode D_3. The inductor L_1 and L_2 charge the output capacitor (C_o) and the current of the inductors L_1 and L_2 is linearly decreased.

2.2 DISCONTINUOUS CONDUSTION INTERVAL

Fig. 3 illustrates the Equivalent circuit of the proposed converter at discontinuous conduction interval (interval 3). Intervals 1 and 2 at discontinuous conduction interval are like states 3 and 4 at continuous conduction interval, respectively. Based on Fig. 3, interval 3 at discontinuous conduction interval could be written as follows:

Interval 3 [$t_3 \le t \le t_4$ **]**

In this state, the power switch (*S*) is turned-off and all diodes are reverse biased. The voltage across the inductors L_1 and L_2 will be zero. The stored energy at the output capacitor (C_o) is discharged to the output load (R). When the power switch is turned-on, this operation ends.

3 PERFORMANCE ANALYSIS

3.1 CONTINUOUS CONDUSTION INTERVAL

State 1: the power switch is on

In this state, the power switch (*S*) is turned-on. By notice the equivalent of this state can be written as follows equations:

$$V_{L1} = V_i \tag{1}$$

$$V_{L2} = V_{C2} + V_{C3} - V_{C1} \tag{2}$$

State 2: the power switch is off-state

In this state, the power switch (*S*) is turned-off. The equivalent of this state can be written as follows equations:

$$V_{L1} = V_i - V_{C1} \tag{3}$$

$$V_o = V_{C1} + V_{C4} - V_{C3} \tag{4}$$

$$V_{C1} = V_{C3} + V_{C5} \tag{5}$$

By applying the volt-second balancing law on the inductors L_1 and L_2 (the average voltage is zero for each inductor in one period). Based on (1)-(5) and Fig. 2, the voltage across the capacitors can be expressed as:

$$V_{C2} = V_{C4} = V_{C5} = \frac{V_i}{1-D} \tag{6}$$

Using (4)-(6), the voltage conversion ratio of the proposed converter (M) in continuous conduction interval can be obtained as;

$$M_{CCM} = \frac{V_o}{V_i} = \frac{2}{1-D} \tag{7}$$

3.2 DISCONTINUOUS CONDUSTION INTERVAL

State 1 [$t_1 \le t \le t_2$]

In this state, the power switch (*S*) remains ON and all diodes are reverse biased expect the diode D_3. The inductor L_1 and L_2 are charged by the input power supply (V_i).

$$V_{L1} = V_i \tag{8}$$

State 2 [$t_2 \le t \le t_3$]

In this state, the power switch (*S*) is turned-off and all diodes are conducting expect the diode D_3. The inductor L_1 and L_2 charge the output capacitor (C_o) and the current of the inductors L_1 and L_2 is decreased linearly.

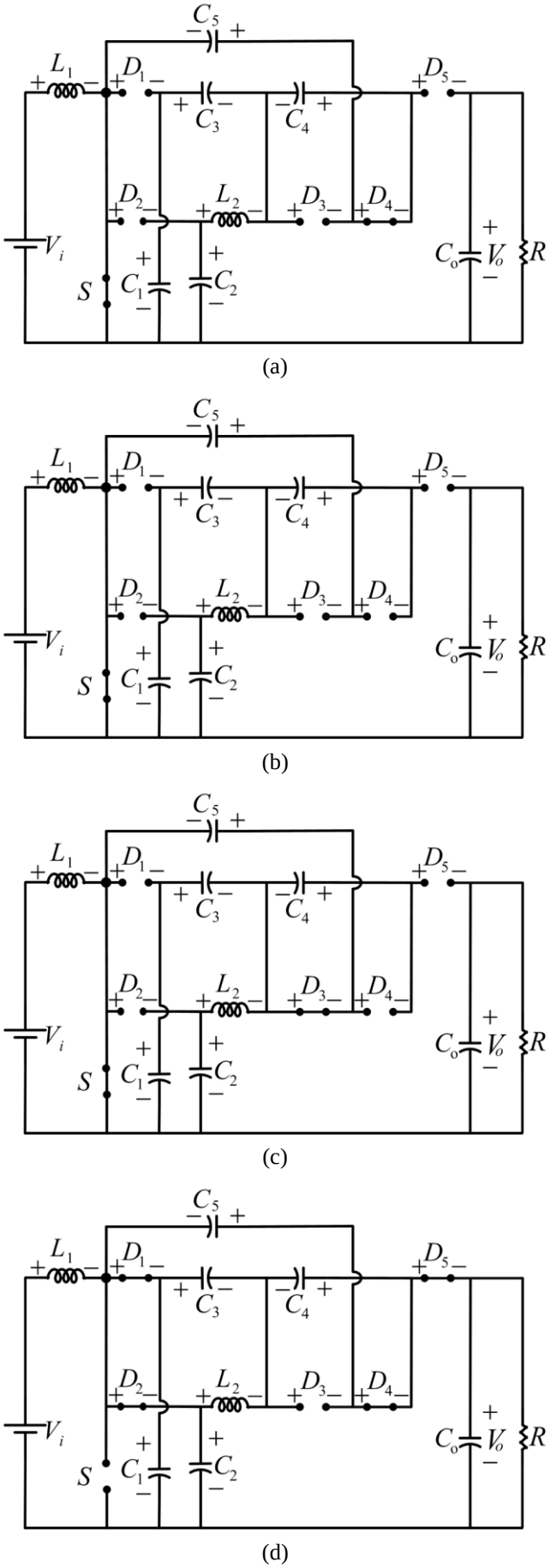


Fig. 2. The power circuit of the proposed converter at CCM operation

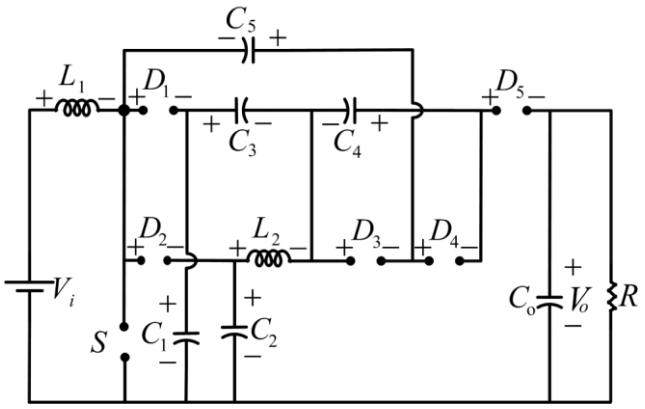


Fig. 3. *The power circuit of the proposed converter at discontinuous conduction interval (state 3)*

State 3 [$t_3 \le t \le t_4$]

In this state, the power switch (*S*) is turn-off and all diodes are reverse biased. The voltage across the inductor L_1 becomes zero.

$$V_{L1} = 0 \tag{9}$$

Based on equation (7), the duty cycle could be calculated as;

$$D = \frac{V_o - 2V_i}{V_o} \tag{10}$$

$$V_{C1} = \frac{16V_i}{15(1-D)} \tag{11}$$

$$DV_i + D'(V_i - V_{C2}) = 0 \tag{12}$$

The interval D´ is that from the beginning of duty cycle until the moment which the current of diodes reaches zero before the period ends.

$$V_{C2} = V_o - V_{C5} \tag{13}$$

$$\frac{V_o}{V_i} = \frac{2(1-D)}{1-D-DD'} \tag{14}$$

$$D' = \frac{(1-D)V_o + 2V_i(D-1)}{DV_o} \tag{15}$$

Based on Fig. 2(d), the average current across the diode D_o is equal to the output current (I_o);

$$\frac{1}{2}D' \times I' = I_o \tag{16}$$

Where,

$$\begin{cases} I' = I_{L1} + I_{L2} = \dfrac{DV_i}{f_s L_{tot}} \\ L_{tot} = \dfrac{L_1 L_2}{L_1 + L_2} \end{cases} \tag{17}$$

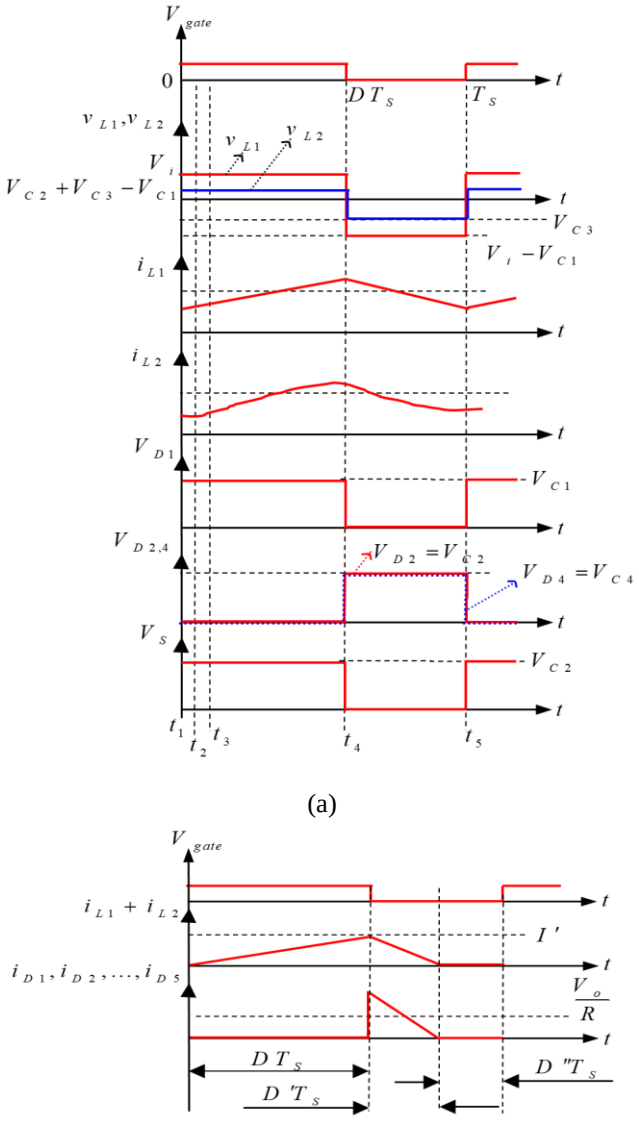
$$\frac{1}{2}D' \times \frac{DV_i}{f_s L_{tot}} = I_o \tag{18}$$

$$\frac{1}{2}\frac{(1-D)V_o + 2V_i(D-1)}{DV_o} \times \frac{DV_i}{f_s L_{tot}} = \frac{V_o}{R} \tag{19}$$

$$M_{DCM} = \frac{(1-D)RV_i + \sqrt{(1-D)^2 R^2 V_i^2 - 16(1-D)RV_i^2 f_s L_{tot}}}{4f_s L_{tot}} \tag{20}$$

During boundary conduction state, the voltage gain of the proposed converter in continuous conduction interval is equal to discontinuous conduction interval. Using (7) and (20), τ_B (is the boundary normalized inductor time constant) can be obtained as:

$$\tau_B = \frac{D^2(2-D)(1-D)}{2} \tag{21}$$



(a)

(b)

Fig. 4. *The main waveforms of the proposed converter,* (a) *in continuous conduction interval,* (b) *in discontinuous conduction interval*

Discontinuous conduction interval for the proposed converter happens when the current of diodes reaches 0 before the end of the switches OFF time. As it could be seen, Fig. 4 illustrates the main waveforms of the proposed converter in continuous conduction interval. Fig. 5 illustrates the relationship between τ_B and *D*. if, $\tau \ge \tau_B$ the proposed

converter operates in continuous conduction interval, else it will operate in discontinuous conduction interval. τ is boundaries time between continuous conduction interval and discontinuous conduction interval. Based on Fig. 5, the proposed converter can operate at discontinuous conduction interval when the duty cycle value is near to zero and 1. Therefore, the duty cycle value can be considered between 0.6 and 0.7 for more assurance that the converter work at continuous conduction interval.

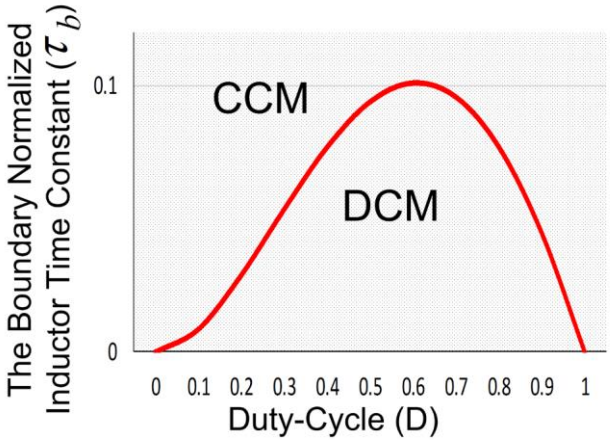


Fig. 5. *The boundary condition of the proposed converter*

4 ANALYSIS THE VOLTAGE STRESS SWITCH AND THE EFFICIENCY OF PROPOSED CONVERTER

4.1 ANALYSIS THE VOLTAGE STRESS ACROSS THE POWER SWITCH

Based on Fig. 2(d), the voltage stress across the power switch (*S*) of the proposed converter can be obtained as:

$$V_S = V_{C2} \tag{22}$$

By combining (6), (13) and (22), the normalized voltage stress across the power switch (*S*) versus difference duty-cycles can be obtained as;

$$M_S = \frac{V_S}{V_o} = \frac{1}{2} \tag{23}$$

4.2 INDUCTOR SELECTION

If the peak-to-peak inductor current ripple is considered ΔI_L, using Figs. 1 and 4, it can be concluded that $\Delta I_L = ri\ \%\ I_L$, the following equation can be written for inductor selection:

$$\begin{cases} L_1 = \dfrac{DV_iV_o}{r_1\% \times f_s \times P_o} \\ L_2 = \dfrac{14V_iV_o - 30DV_iV_o}{r_2\% \times 15(1-D) \times f_s \times P_o} \end{cases} \tag{24}$$

4.3 CALCULATION THE EFFICIENCY OF THE PROPOSED CONVERTER IN CCM OPERATION

To calculate the efficiency of the proposed converter ($\eta_{Converter}$), the parasitic resistances of power components are defined as:

- $r_{DS\text{-}on}$: on-state resistance of the power switch *S* (0.055),
- r_{L1} and r_{L2}: the equivalent series resistance (ESR) of inductors L_1 and L_2 (about 0.033),
- r_{D1}, r_{D2},…, r_{D5}: the equivalent series resistance of diodes D_1, D_2,…, D_5 (0.02)
- r_{C1}, r_{C2},…, r_{C5}, r_{Co}: the equivalent series resistance of capacitors C_1, C_2,…, C_5 and C_o (0.033).

The efficiency of the proposed converter could be calculated as,

$$\eta_{Converter} = \frac{P_o}{P_{in}} \times 100\% = \frac{P_o}{P_o + P_{losses}} \times 100\% \tag{25}$$

The power loss of the switch *S* ($A_{r_{DS-ON}}$) can be obtained as:

$$\begin{cases} A_{r_{DS-ON}} = r_{DS-ON} \times I_{S(\text{rms})}^{\ 2} \\ \qquad = \dfrac{r_{DS-ON}(2D + D - 1)^2 I_o^{\ 2}}{D^2(1-D)^2} \end{cases} \tag{26}$$

The overall power losses of the switch (A_s) consist of the power loss of the switch when the power switch is ON, therefore the switching losses could be written as follows,

$$\begin{cases} A_S = A_{r_{DS-ON}} + \dfrac{1}{6}A_{Switching} \\ \quad = (r_{DS-ON} \times I_{S(\text{rms})}^{\ 2}) + \dfrac{1}{6}(C_S V_S^{\ 2} \times f_S) \\ \quad = \dfrac{r_{DS-ON}(2D + D - 1)^2 I_o^{\ 2}}{D^2(1-D)^2} + \dfrac{1}{6}C_S\left(\dfrac{V_i}{1-D}\right)^2 f_S \end{cases} \tag{27}$$

Where, $A_{r_{DS-ON}}$ is ON-state power loss of the switch, r_{DS-ON} is ON-state resistance of the switch, C_S is parasitic capacitor of the power switch and V_s is stress voltage across the power switch.

Based on Fig. 1, the average current of the inductor L_1 is equal to I_i and, the average current of the inductor L_2 is equal to Io since the average current of each capacitor is zero in one period. Therefore, the conduction losses of the inductors L_1, and L_2 (A_{L_1,L_2}) can be achieved as,

$$\begin{cases} A_{L_1,L_2} = r_{L_1} \times I_{L_{1(\text{rms})}}^{\ 2} + r_{L_2} \times I_{L_{2(\text{rms})}}^{\ 2} \\ = r_{L_1}\left[\dfrac{2}{1-D} I_o\right]^2 + r_{L_2} \times I_o^{\ 2} \end{cases} \tag{28}$$

The forward resistance losses ($A_{RF_{(\text{Diodes})}}$) and voltage losses ($A_{VF_{(\text{Diodes})}}$) of the diodes D_1, D_2, …, D_5 can be achieved as:

$$A_{Losses_{D_1,D_2,...,D_5}} = A_{RF_{D_1,D_2,...,D_5}} + A_{VF_{D_1,D_2,...,D_5}} \quad (29)$$

$$\begin{cases} A_{RF_{D_1,D_2,...,D_1}} = \sum_{k=2}^{5} (r_{F_{D_k}} \times I_{F_{D_k(\text{rms})}}{}^2) \\ \qquad = (\frac{I_o}{1-D})^2 \left[\sum_{k=2}^{5} r_{F_{D_k}} \right] \\ A_{VF_{D_1,D_2,...,D_5}} = (\frac{I_o}{1-D}) \left[\sum_{k=2}^{5} \mathrm{V}_{F_{D_k}} \right] \end{cases} \quad (30)$$

The power losses of the capacitors C_1, C_2,…, C_5 and C_o can be obtained as,

$$A_{R_{C_1,C_2,...,C_5,C_o}} = r_{Co} \times I_{r_{C_{o(\text{rms})}}}{}^2 + \sum_{k=1}^{5} (r_{C_k} \times I_{r_{C_k(\text{rms})}}{}^2) \quad (31)$$

Using (24)-(31), the overall efficiency of the proposed converter can be obtained as,

$$\begin{cases} \eta_{Converter} = \dfrac{P_o}{P_o + P_{losses}} \times 100\% \\ P_{losses} = A_1 + A_2 + A_3 + A_4 + A_5 + A_6 + A_7 \\ A_1 = \dfrac{r_{DS-ON}\,(2D + D - 1)^2 I_o{}^2}{D^2 (1-D)^2} \\ A_2 = \dfrac{1}{6} C_S (\dfrac{V_i}{1-D})^2 f_S \\ A_3 = r_{L_1} \left[\dfrac{2}{1-D} I_o \right]^2 + r_{L_2} \times I_o{}^2 \\ A_4 = (\dfrac{I_o}{1-D})^2 \left[\sum_{k=2}^{5} r_{F_{D_k}} \right] \\ A_5 = (\dfrac{I_o}{1-D}) \left[\sum_{k=2}^{5} \mathrm{V}_{F_{D_k}} \right] \\ A_6 = \mathrm{r}_{R_{C_o}} \times I_{R_{C_{o(\text{rms})}}}{}^2 + \sum_{k=1}^{5} (\mathrm{r}_{R_{C_k}} \times I_{R_{C_k(\text{rms})}}{}^2) \end{cases} \quad (32)$$

Where, A_1, A_2, A_3, A_4, A_5 and A_6 are as:

$A_1 \rightarrow$ the power losses of the switches,
$A_2 \rightarrow$ the switching losses,
$A_3 \rightarrow$ the conduction losses of the inductors,
$A_4 \rightarrow$ the diodes forward voltage ($r_{FD} \times I_D$) losses,
$A_5 \rightarrow$ the diodes voltage drop (V_{FD}) losses,
$A_6 \rightarrow$ the power losses of the capacitors.

4.4 DYNAMIC RESPONSE

In this section, the dynamic differences of the proposed converter is provided. For achieving the average model of the proposed converter, the state-space averaging (SSA) model is used. The system equations of the proposed converter are obtained for third and fourth operation states (states first and second are ignored because they are small). In order to obtain the state space equations of the proposed converter, the following assumptions are considered:

- Power switch and all power diodes are considered ideal
- The input voltage source is considered constant
- Inductors L_1=L_2 are equal to each other's as L_1=L_2=L so that the parasitic series resistor of the inductors is considered r_L
- All capacitors are equal to each other's C_1=C_2=C_3=C_4=C_5=C_o=C so that the parasitic series resistor of the capacitors is considered r_C.

For analysis the dynamic response of the proposed converter and achieve to state equations, the small-time states (states 1 and 2) are ignored, and just states 3 and 4 are considered for obtaining of state equations. In space state, the response is the output voltage V_o. Dynamic performance of the proposed converter is analyzed with the small-signal frequency response (for each state of the proposed converter, the state space equation is calculated separately). All inductors are considered are equal and all capacitors are considered equal.

A PI controller and LPF (low passive filter) are used before duty cycle value of the proposed converter to control the output voltage. In fact, the output voltage of the proposed converter is measured and this value is compared to the desired amount of the output voltage ($V_{o,ref}$) which is considered as a reference. Therefore, when a change occurs between the output voltage of the proposed converter and a reference voltage ($V_{o,ref}$), the controller adjusts the output voltage of the proposed converter by selecting a proper amount for duty cycle. The proper duty cycle value is compared with a carrier wave, so the proper interpolated pulse is applied to the power MOSFET. The PI controller bloke has a gain and a time constant which this value is achieved by a trade-off. Fig. 6(a) illustrates the closed-loop small-signal transfer function based on the output voltage and duty cycle value. The magnitude (dB) and phase frequency response of the proposed converter is shown in Fig. 6(b).

5 COMPARISON STUDY

In this section, the proposed converter is compared with other converters from different aspects. TABLE 1 illustrates the comparison between the proposed converter and other structure based on voltage gain, normalized voltage stress across the power switches, and normalized voltage stress across the power diodes, number of switches, total devices number and efficiency. Regarding the normalized voltage stress across the semiconductors, the proposed converter is not proper for high power limits. By increasing the power limits of the proposed converter, the output voltage will be high, and the normalized voltage stress across the semiconductors is not dissembled. Generally, the power losses of the proposed converter will be fewer in the low and middle power levels and the efficiency of the proposed converter will be higher. Hence, the proposed converter is proper for low and middle power levels. The efficiency of the proposed converter is higher than the other structures such as Conventional boost converter, conventional SEPIC and

ZETA converter. In Table 1, *n* and *N* are the voltage multiplier units and turns ratio of the converter, respectively. As defined above, *M* is the voltage gain of the converters.

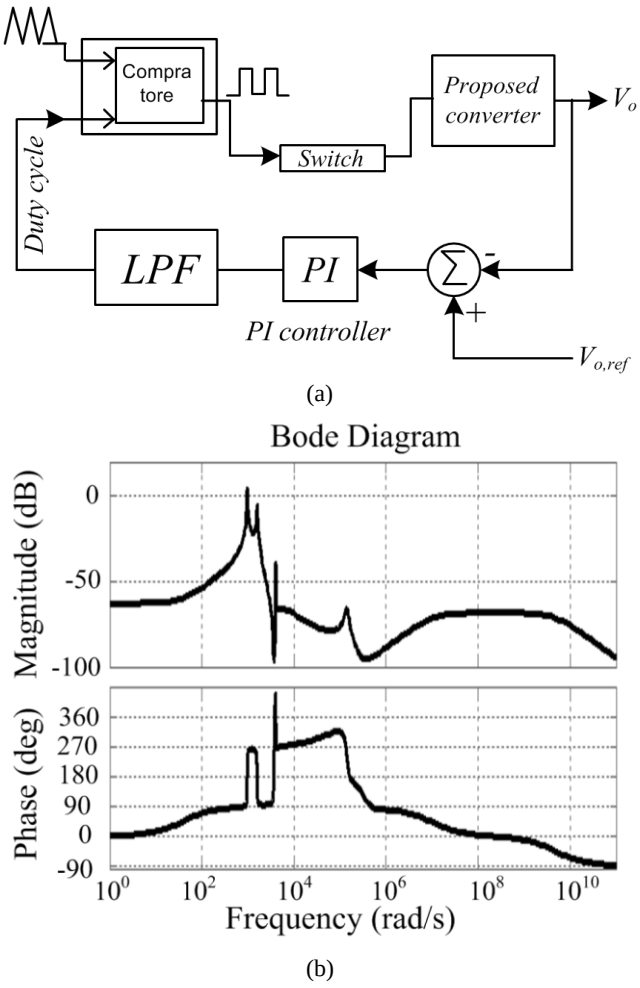


Fig. 6. *Dynamic response of the proposed converter, (a)* Control bloke for step change response, *(b)* Bode plot

5 COMPARISON STUDY

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5.1 VOLTAGE CONVERSION RATIO VERSUS DUTY-CYCLE

The voltage conversion ratio between the proposed converter and other structures is shown in Fig. 7(a). By observing this figure, it is clear that the voltage conversion ratio of the proposed converter is larger than the other structures. Achieving a high voltage conversion ratio with a lower duty cycle value leads to a decrease in the power switch losses. In addition, using a power switch with lower on state resistant causes to decrease the conduction losses and increase the overall efficiency of the converter. Generally, a proper voltage conversion ratio with low cost of dc-dc converters is one the important issues for renewable applications which the proposed converter has this advantage. Although the proposed topology seems to have a lower voltage gain for the duty cycles lower than 0.5 (low powers) seems to be lower than [27] but for the best operational range of duty cycles for DC-DC converters [0.5-0.7], the proposed topology has the highest voltage gain in comparison to all the proposed ones. It could be concluded that for the operational range of duty cycle for DC-DC converters, the proposed topology has advantages over the others, which is because of having higher efficiency and less switching losses.

5.2 VOLTAGE STRESS ON POWER SWITCHES

Fig. 7(b) illustrates the curves of the normalized voltage stress across power switches versus duty cycle for the proposed converter and different structures. The normalized voltage stress across the power switch is 0.5 for all power levels. Therefore, the proposed converter has not problems of the conventional boost and conventional SEPIC, also using power switch with lower on-state resistance and lower rating values causes a decrease in the lower losses and an increase in the overall efficiency. The maximum spike of the power switch is low, so there are no additional circuits for solving this issue which causes to increase the number of components and cost.

5.3 VOLTAGE STRESS ON POWER DIODES

Fig. 7(c) shows the normalized voltage stress across the power diodes versus voltage conversion ratio. By observing this figure, it can be said that the normalized voltage stress across the power diodes remains constant 0.5. The normalized voltage across the power diodes of the proposed converter is lower than the other structure except [24, 26]. However, the overall efficiency of the converter in Ref. [24] is lower than the proposed converter due to losses of the using transformer, and also the voltage gain of the converter in [26] is lower than the proposed converter. As a result, to generate

the same voltage gain for the proposed converter and converter in [26], converter in [26] must have a high duty cycle value. Therefore, the power losses for high duty cycle is one of the important issues.

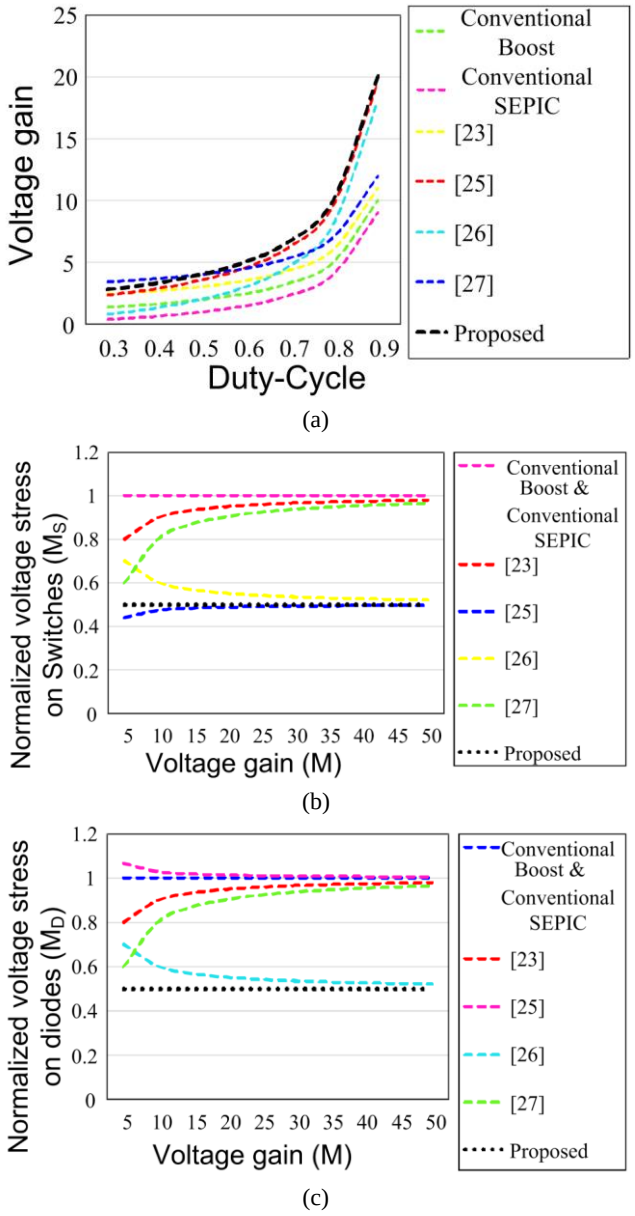


Fig. 7. *Comparison between the proposed converter and other structure*, (a) voltage conversion ratio versus duty-cycle, (b) voltage stress on MOSFET versus duty-cycle, (c) voltage stress on diodes versus duty-cycle.

As shown in Figs. 7(b) and (c), it can be said that the normalized voltage stress across the power MOSFET of the proposed converter and [25] are equal, however, the normalized voltage stress across the power diode in [23, 25] is larger than the proposed converter. In [24], the voltage gains of the converter, the normalized voltage stress across the power MOSFET and power diode are equal to the proposed converter when N is selected 1. However, the overall efficiency of the converter in [24] is lower than the proposed converter due to the existence of transformer.

6 EXPERIMENTAL RESULTS

In order to show the validity of the proposed converter performance and confirm the accuracy of the theoretical analysis, a prototype of the proposed converter is built and tested in the laboratory and also the experimental results of the laboratory prototype are provided in Figs. 8 and 10. Table 2 illustrates the characteristics of the power components.

Table 2 Characteristics of the components

Components	characteristics
Input voltage	24V
Duty cycle	0.7
Switching frequency	25kHz
Inductors L_1	1mH
Inductors L_2	580µH
Capacitors C_1, C_2, C_3, C_4, C_5	330µF
Capacitor C_o	470µF, 450V
MOSFET	IRFP260
Diodes D_1, D_2, D_3, D_4, D_5	MUR1560

The experimental results of the 150Watt laboratory prototype, with operating frequency of 25 kHz are provided. Table 3 illustrates the Maximum voltage, average and the rms current of the power semiconductors (diode/MOSFET) for simulation and experimental results.

Table 3 Simulation and experimental values of the power semiconductors (MOSFET/diode)

Max. voltage, Ave. and rms current of the MOSFET and diodes	Sim. values	Exp. values	unit
Peak voltage across MOSFET	79.40	79.60	V
Average current MOSFET	5.85	5.88	A
RMS current MOSFET	7.08	7.06	A
Peak voltage across diode D_1	84.9	85.05	V
Average current diode D_1	1.05	1.07	A
RMS current diode D_1	1.99	1.97	A

Based on Table 3, the obtained values for the power semiconductors both the simulation and experimental results are confirmed with each other as well. As a result, evidence show that the laboratory prototype is implemented based on the theory's correct calculations.

The voltage of the capacitors and the output voltage of the proposed converter are shown in Fig. 8. However, Fig. 8(a) illustrates the voltage of the capacitors C_1 and C_2. The voltage of the capacitors C_1 and C_2 are 79.1 V and 84.3 V, respectively which are calculated in equations (6) and (11). Fig. 8(b) illustrates the voltage of the capacitors C_4 and C_5. The values obtained for the capacitor voltages C_4 and C_5 are both about 79.1 which confirm (6).

Also, the output voltage of the proposed converter is shown in Fig. 8(c) which is about 151 V. Using (7) and Table 2 (based on duty cycle and input source voltage values), it can be said that the obtained values from the experimental result and theoretical analysis are in god agreement. Fig. 8(d) shows the 50% variation load of the proposed converter.

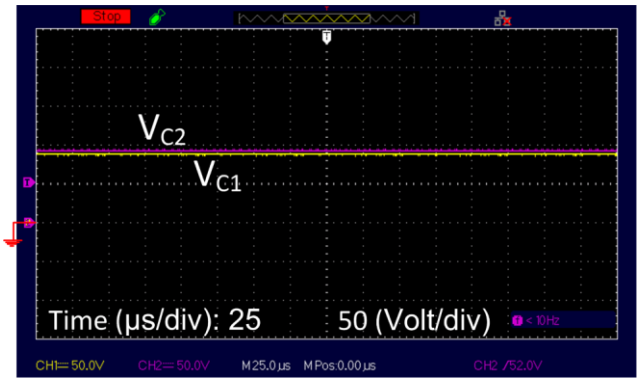
Table 1 The comparison between the proposed converter and the other structures

High step-up converter	Conventional boost	Conventional SEPIC	Converter in [23]	Converter in [24]	Converter in [25]	Converter in [26]	Converter in [27]	Proposed converter
Voltage gain [M]	$\frac{1}{1-D}$	$\frac{D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{1+N}{1-D}$	$\frac{3+D}{2(1-D)}$	$\frac{2D}{1-D}$	$\frac{2+n-(1+n)D}{1-D}$	$\frac{2}{1-D}$
Normalized voltage stress on switch	1	1	$\frac{M-1}{M}$	$\frac{1}{1+N}$	$\frac{2M-3}{4M-4}$	$\frac{M+2}{2M}$	$\frac{M-n-1}{M}$	0.5
Normalized voltage stress on diodes	1	1	$\frac{M-1}{M}$	$\frac{N}{1+N}$	$\frac{4M-3}{4M-4}$	$\frac{M+2}{2M}$	$\frac{M-n-1}{M}$	0.5
No. of switches	1	1	1	1	1	1	1	1
No. of diodes	1	1	3	3	4	2	n+3	5
Total devices number	4	5	8	10	11	8	3n+6	14
Power [W]	-	-	150	150	150	150	150	150
Eff. [%]	-	-	92.80	91.6	92.27	94.10	95.10	94.30

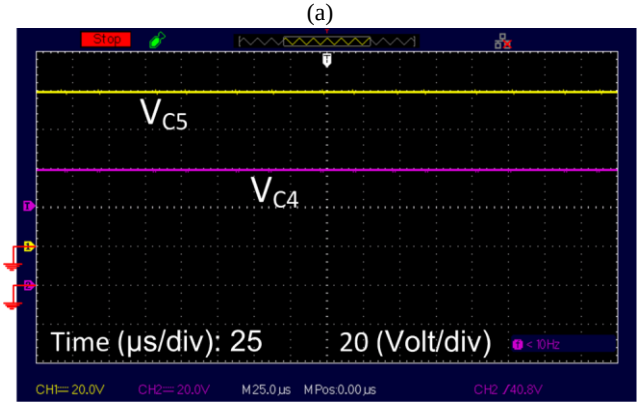
By observing this figure, it is clear that the output voltage has a dynamic changes and recovery time for this item is about 47ms. Generally, a step change at load value of the proposed converter causes to a small change at output voltage and power level which this is logical for each system. However, the proposed converter after about 50 ms maintains its steady state. Also, the output voltage of the proposed converter is shown in Fig. 8(c) which is about 151 V. Using (7) and Table 2 (based on duty cycle and input source voltage values), it can be said that the obtained values from the experimental result and theoretical analysis are in god agreement. Fig. 8(d) shows the 50% variation load of the proposed converter. By observing this figure, it is clear that the output voltage has a dynamic changes and recovery time for this item is about 47ms. Generally, a step change at load value of the proposed converter causes to a small change at output voltage and power level which this is logical for each system. However, the proposed converter after about 50 ms maintains its steady state.

Fig. 9 illustrate the maximum voltage across the power semiconductors (MOSFET and diodes). The maximum voltage stress across the power MOSFET is shown in Fig. 9(a) which is obtained to be about 79.60 V. Using (6) and (22), it can be said that the achieved value of the maximum voltage of the power MOSFET from the experimental result confirms the theoretical analysis. Fig. 9(b) illustrates the maximum voltage of the diode D_1 which is about 85V.

As shown in Fig. 4, it is clear that the maximum voltage of the diode D_1 is equal to V_{C1} which confirms the theoretical analysis results as well. Figs. 9(c) and (d), illustrate the maximum voltage of the diodes D_2 and D_4, respectively. The measured maximum voltage for both diodes D_2 and D_4 is 79.5 V about. This value confirms the obtained value of the theoretical analysis which is shown in Fig. 4. By observing Fig. 4, it can claimed that the normalized voltage stress on power semiconductors and the maximum spike of these components is lower in comparison to the conventional boost converter.



(a)



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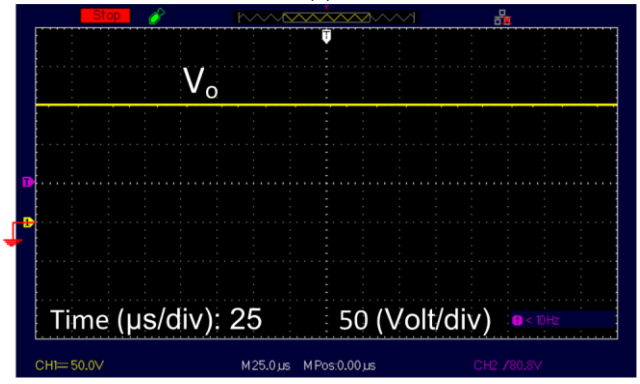
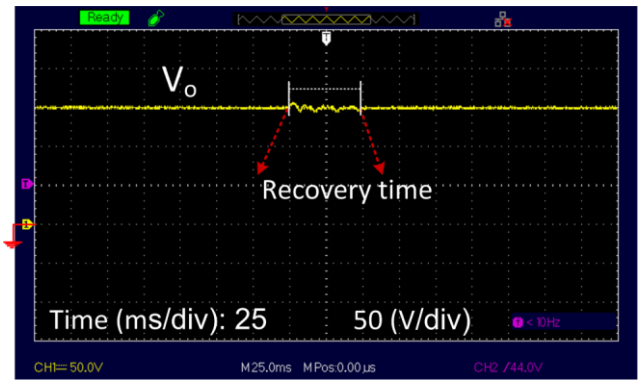
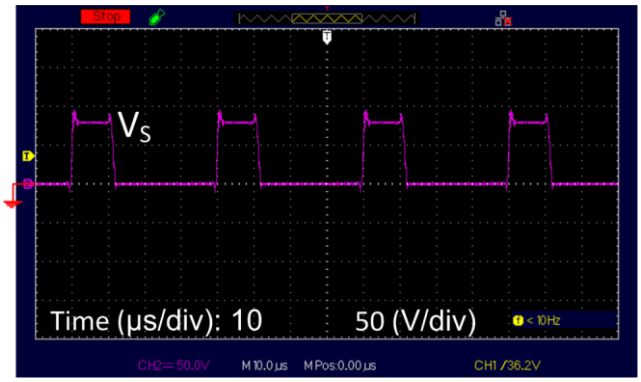


(c)

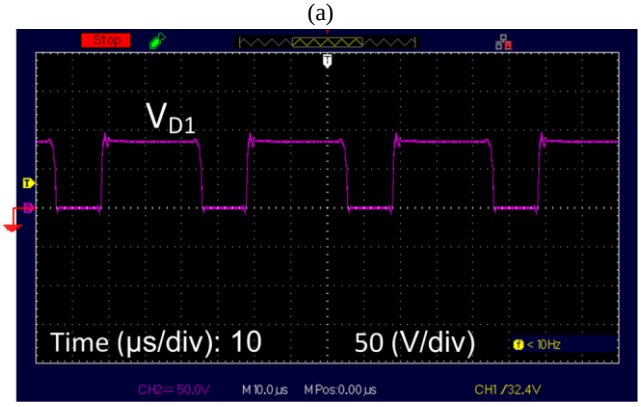


(d)

Fig. 8. *Experimental waveforms,*
(a) The voltage of the capacitors C_1 and C_2,
(b) The voltage of the capacitors C_4 and C_5,
(c) The output voltage V_o,
(d) 50% variation load



(a)



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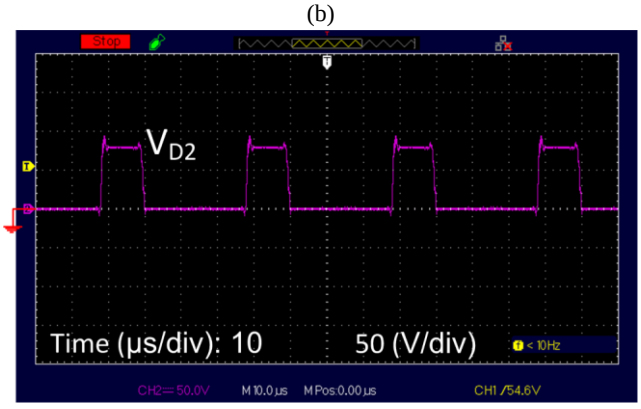
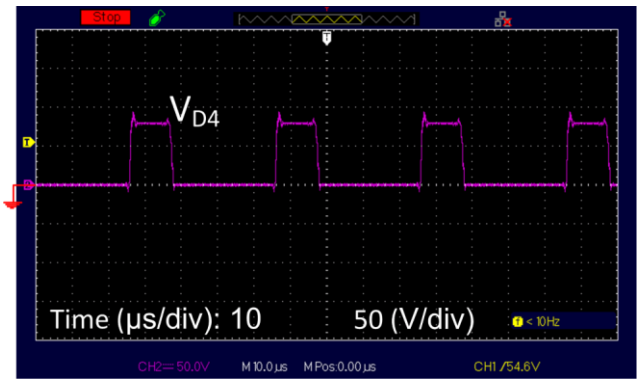


(c)



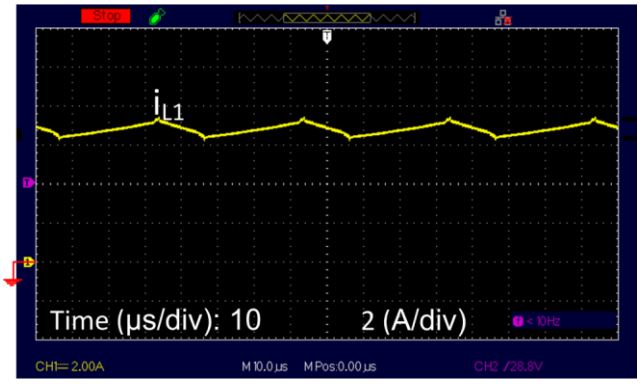
(d)

Fig. 9. *Experimental waveforms,*
(a) The maximum voltage of the MOSFET S_1,
(b) The maximum voltage of the diode D_1,
(c) The maximum voltage of the diode D_2,
(d) The maximum voltage of the diode D_4,

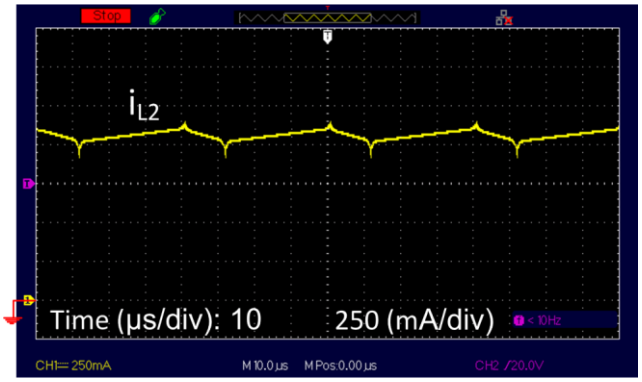
Fig 10 illustrate the current waveforms of the inductors L_1 and L_2. The current waveform of the inductor L_1 changes between 6.60A and 7.23A (the average current of the inductor L_1 is about 6.91A). The tolerance percentage of the inductor L_1 is about 9 percent. The input current of the proposed converter is the same the current of the inductor L_1. It is clear that the input current ripple of the proposed converter is suitable for renewable applications.

Fig. 10(b) illustrates the current waveform of the inductor L_2. The current ripple of the inductor L_2 is about 0.06 A which is shown in this figure (about 5%). The average current of the inductor L_2 is obtained 1.05A. It is worth mentioning that the ripple of the inductors has considered the peak-to-peak values.

Figs. 11 illustrates the measured efficiency of the proposed converter based on power level changes. Based on Fig. 11, the maximum efficiency of the proposed converter is 95.80% at 80W. Also, it can be said that the measured efficiency is obtained 91.50% for all power levels. The total power losses of the proposed converter which consist of semiconductor (switch and diode) power losses and series resistance power losses decrease the efficiency with about 4.30% percent (in fact this indicate the efficiency tolerances of the proposed converter for all power levels).



(a)



(b)

Fig. 10. *Experimental waveforms,*
(a) The current of the inductor L_1,
(b) The current of the inductor L_2,

As a result, based on comparison study and experimental result, it can be said that the overall cost of the proposed converter is decreased by selecting the lower rating for power devices which can be understood from the measured efficiency of the laboratory prototype.

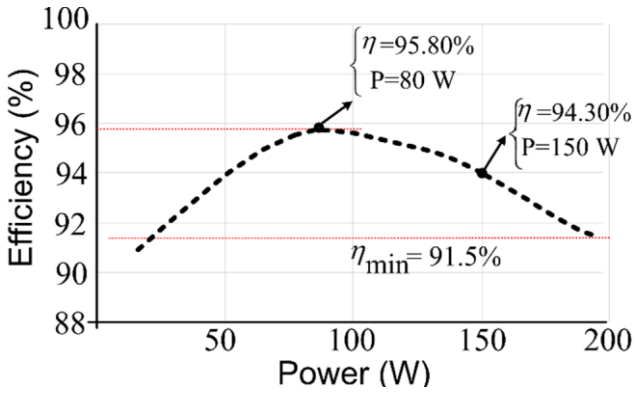


Fig. 11. *The efficiency of the proposed converter versus Power level changes*

7 CONCLUSIONS

In this paper, a new high step-up dc/dc converter with high efficiency for renewable energy applications (PV Panels) is presented. The proposed converter only has a single switch in the input side, so the power losses will be low. Because of having one switch, the control of the proposed converter could be simple. The on-state resistance of the power switch is low and the efficiency of the proposed converter is high. The proposed converter uses diode/capacitor combination to increase the voltage conversion ratio. A 150-watt prototype of the proposed converter is designed to perform the tests in operating frequency of 25 kHz and the calculated efficiency is 94.30%. The maximum efficiency of the proposed converter is about 95.8% at 80W. Theoretical and experimental results illustrate that the proposed converter is capable of achieving the overall efficiency higher than about 91.5% in all power levels. In addition, another advantage of the proposed converter is the low input current ripple, therefore it can be said that the proposed converter is a good candidate for renewable source based applications such as PV panels.

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