HELSINKI UNIVERSITY OF TECHNOLOGY
Department of Electrical and Communications Engineering

SAMI LALLUKKA

Programmable logic design for an optical access network

Thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Technology

Espoo 27th May 2003

Supervisor: Professor (pro tem) Samuli Aalto, HUT
Instructor: Lic.Sc. (Tech.) Kari Seppänen, VTT

Abstract

HELSINKI UNIVERSITY OF TECHNOLOGY   ABSTRACT OF THE MASTER'S THESIS

Author: Sami Lallukka
Name of the Thesis: Programmable logic design for an optical access network
Date: 27th May 2003   **Number of pages:** 99

Department: Department of Electrical and Communications Engineering
Professorship: S-38

Supervisor: Professor (pro tem) Samuli Aalto
Instructor: Lic.Sc. (Tech.) Kari Seppänen

The structure of communication networks is going to change in the future. Data-com, telecom and broadcast traffic is conventionally transported over separated networks, which is a major cost factor in network management for operators. In addition, legacy communication networks cannot provide adequate quality of service for the emerging interactive multimedia services. For this reason, the development of communications networks is heading towards flexibility and convergence.

At the moment, the bottleneck factor in the development of communication networks transfer speed is the complexity of the metropolitan area feeder networks. This has a considerable effect on the service quality in this area as well. The TEKES-funded OAN-project concentrates on developing a new and simpler metropolitan optical feeder network, which could be used to improve the quality of service in the metropolitan area.

This thesis has been prepared as a part of the OAN-project. In this thesis, the structure of the present communication networks is presented and its problems are discussed. Based on this discussion, the future structure of communication networks is illustrated. Furthermore, the HDL-implementation process with its aggregates will be discussed. Finally, a programmable logic design for the optical metropolitan feeder network prototype, implemented in the OAN project, is presented.

Keywords: FPGA, VHDL, DoS, optical feeder network

i

Tiivistelmä

TEKNILLINEN KORKEAKOULU | DIPLOMITYÖN TIIVISTELMÄ

Nimi: Sami Lallukka
Työn nimi: Optisen liityntäverkon ohjelmoitavien logiikkapiirien ohjelmoinnin suunnittelu
Päivämäärä: 27. toukokuuta 2003 | **Sivumäärä:** 99

Osasto: Sähkö- ja tietoliikennetekniikan osasto
Laboratorio: S-38

Valvoja: Professori (ma.) Samuli Aalto
Ohjaaja: TkL. Kari Seppänen

Tiedonsiirtoverkkojen rakenne elää muutoksen aikaa. Perinteisesti data-, puhelin- ja laajakaistaliikenne on siirretty erillisissä verkoissa, joiden samanaikainen ylläpitäminen tuottaa ylimääräisiä kustannuksia operaattoreille. Lisäksi uudet interaktiiviset palvelut vaativat toimiakseen sellaista palvelunlaatua, jota nykyiset tiedonsiirtoverkot eivät kykene tarjoamaan. Näiden epäkohtien johdosta tiedonsiirtoverkkojen kehityksessä tähdätään uusiin, entistä joustavampiin ja eri toiminnot yhdistäviin verkkoratkaisuihin, joissa tiedonsiirron palvelunlaadulla on entistä suurempi merkitys.

Tällä hetkellä tiedonsiirtoverkkojen kokonaistiedonsiirtonopeuden kasvun pullonkaulatekijäksi on muodostunut kaupunkialueiden syöttöverkkojen monimutkaisuus, millä on suuri vaikutus myös tiedonsiirron palvelunlaatuun. TEKES-rahoitteisessa OAN-projektissa kehitetään uutta ja yksinkertaisempaa kaupunkialueen optista syöttöverkkoratkaisua, jolla alueen palvelunlaatua saataisiin parannettua.

Tämä diplomityö on tehty osana OAN-projektia. Työssä kuvataan tiedonsiirtoverkkojen tämänhetkinen rakenne, tarkastellaan sen ongelmia ja tulevaisuuden kehityssuuntia, sekä esitetään pohdintojen pohjalta rakennettu malli tulevaisuuden tiedonsiirtoverkkojen rakenteelle. Työssä esitetään myös HDL-implementointiprosessiin kuuluvat työvaiheet sekä käydään läpi suunnitelma OAN-projektissa toteutettavan prototyypin ohjelmoitavien logiikkapiirien ohjelmaa varten.

Avainsanat: FPGA, VHDL, DoS, optinen syöttöverkko

Foreword

This thesis has been written in partial fulfillment of the requirements for the degree of Master of Science in Technology while participating in the OAN research project at VTT Information Technology, Broadband Communications.

On behalf of the employer, I would like to thank Markku Sipilä and Kristiina Hytönen for the possibility to write this thesis at VTT. Furthermore, I would like to thank all of my colleagues for their support and advice during the writing process; in particular, Kari Seppänen for his excellent ideas, guidance and proof reading; also, Risto Mutanen and Juha Zidbeck for their valuable advice and insights. Most of all, I would like to thank all of the VTT personnel located in the same premises for a splended atmosphere, especially, the gang in the coffee and lunch breaks. Finally, special thanks to my supervisor, Samuli Aalto at Helsinki University of Technology for excellent cooperation, careful proof reading and guidance.

I would also like to thank all of my family, relatives and friends, who have motivated me in my studies.

27th May 2003, Espoo, Finland

Sami Lallukka

Contents

Acronyms

ADM Add Drop Multiplexer

AN Access Node

APON ATM Passive Optical Network

APS Automatic Protection Switching

ASIC Application Specific Integrated Circuit

ASON Automatically Switched Optical Network

ASTN Automatically Switched Transport Network

ATM Asynchronous Transfer Mode

AWG Arrayed Waveguide Gratings

BER Bit Error Rate

BPON Broadband PON

CATV Cable Antenna Television

CLB Configurable Logic Block

CO Central Office

CPU Central Processing Unit

CRC Cyclic Redundancy Check

DCM Digital Clock Manager

DIP Diagonal Interleaved Parity

DLL Delay Locked Loop

DWDM Dense Wavelength Division Multiplexing

DoS Data over SDH

EFM Ethernet in the First Mile

EPON Ethernet PON

FDM Frequency Division Multiplexing

FEC Forward Error Correction

FIFO First In First Out memory

FPGA Field Programmable Gate Array

FSAN Full Service Access Networks

FTTx Fiber-to-the-x, where x stands for C (Curb), B (Building) or H (Home).

GFP-F Frame-mapped GFP

GFP-T Transparent GFP

GFP Generic Framing Procedure

GMPLS Generic MPLS

GPON Gb PON

GSM Global System for Mobile communication

HDLC High level Data Link Control

HDL Hardware Description Language

HEC Header Error Checksum

HUT Helsinki University of Technology

IEEE Institute of Electrical and Electronics Engineers

IOB Input/Output Block

IPsec IP Security

IP Internet Protocol

ISDN Integrated Services Digital Network

IST Information Society Technologies

ITU-T International Telecommunication Union, Telecommunication standard-isation sector

IWF Interworking Functions

LAN Local Area Network

LCAS Link Capacity Adjustment Scheme

LED Light Emitting Diode

LVDS Low Voltage Differential Signalling

MAC Medium Access Control

MAN Metropolitan Area Network

MPLS Multi Protocol Label Switching

N-ISDN Narrow-band ISDN

OAN Optical Access Networking

OLT Optical Line Terminal

OLT Optical Line Termination

ONT Optical Network Terminal

ONU Optical Network Unit

OPADM Optical Packet Add/Drop Multiplexer

OPR Optical Packet Router

OSI Open Systems Interconnection

OTN Optical Transport Network

OXC Optical Cross Connect

PCI Peripheral Component Interconnect

PDH Plesiochronic Digital Hierarchy

PHY Physical Layer

PLL Phase Locked Loop

POH Path Overhead

PON Passive Optical Network

POS Packet Over SDH

POTS Plain Old Telephone Service

PPP Point-to-Point Protocol

PSTN Public Switched Telephone Network

QoS Quality of Service

RAM Random Access Memory

RPR Resilient Packet Ring

SAN Storage Area Network

SDH Synchronous Digital Hierarchy

SNMP Simple Network Management Protocol

SONET Synchronous Optical Network

SRAM Static Random Access Memory

STM-1 Synchronous Transport Module 1

T1X1 Standards Committee T1 Telecommunications, Technical Subcommittee of Digital Hierarchy and Synchronization

TBS TelecomBus Serialiser

TDMA Time Division Multiple Access

TDM Time Division Multiplexing

TEKES National technology agency

TOH Transport Overhead

VCG Virtual Concatenation Group

VC Virtual Concatenation

VHDL VHSIC Hardware Description Language

VHSIC Very High Speed Integrated Circuit

VPN Virtual Private Network

VTT Technical Research Centre of Finland

VoIP Voice over IP

WADM Wavelength Add Drop Multiplexer

WAN Wide Area Network

WDMA Wavelength Division Multiple Access

WDM Wavelength Division Multiplexing

xDSL x-Digital Subscriber Line

List of Figures

List of Tables

Chapter 1

Introduction

The continuing development of computing and memory management capabilities of computers has brought out new challenges to networking technologies. The bandwidth is no longer a problem, but today it is the network management and more importantly the availability of new type of services, real-time and streaming media. The increase in bandwidth together with developments in end-user equipment, especially in wireless one, has encouraged researchers to find new ways to utilise this emerging possibility in communications. However, the quality of connection in two-way communication is sensitive for the end-to-end transmission delay. Today, most of the datacom networks suffer from long delays and especially from high packet delay variation, which makes the current situation even worse.

Enabled by the technologies already developed, the transfer speed in a point-to-point connection can be almost as high as we like. Point-to-point connections are used as building blocks of larger networks and the sufficient connection bandwidth is determined within the network. The available capacity of point-to-point connection can be most efficiently utilised in Wide Area Networks (WANs) and Local Area Networks (LANs), where the traffic is processed transparently leaving the technology specific processing for Metropolitan Area Networks (MANs) to handle. Most of the used telecommunication technologies come across in MAN, where a variety of conversions are needed between them. These conversions are slow and complex and have slowed down the development of metropolitan area networking, while other areas of networking have experienced major improvements. This is why the present MAN can be seen as a bottleneck for the transfer speed of the whole network [Inc02c].

1

1.1 Motivation

The National technology agency (TEKES)-funded project called Optical Access Networking (OAN) [1] is a three-year project with several participants. The goal of the project is to implement a test network for development of new metropolitan area services and network structures. In this project, most of the test network functionality will be implemented with programmable logic. Programmable logic devices can be programmed over and over again, which gives much flexibility to the design, because different variations of the programs can be easily tested. In addition, they are large of their size and provide efficient processing abilities for the design. Of course, this is only when these Field Programmable Gate Arrays (FPGAs) are programmed properly, which is my task in this project and more deeply discussed later in this thesis.

1.2 Goal

The goal of this thesis is to identify what kind of requirements the future optical access network gives for the underlying transport network, find ways to support these requirements, evaluate them and provide a Hardware Description Language (HDL) design for the FPGAs in the OAN network prototype.

1.3 Structure

After this brief introduction the rest of the thesis will be structured as follows. Chapter 2 introduces the reader to the characteristics of networks today, covering some of the networking history together with key technologies and methods. Chapter 3 carries on the issue and reveals the nature of the future communication networks. After that, in chapter 4 the research project called OAN is presented. Chapter 5 discusses the methodology of HDL-implementation. The options for the OAN HDL design are presented in chapter 6 and the final design in chapter 7. Finally, the conclusions of the thesis are presented in chapter 8.

---

[1]Discussed more deeply in chapter 4

Chapter 2

Communication networks today

The first remarkable development in long distance communication was the invention of optical telegraph in 1791 [Bel03]. Since then, the desire for topical information among people has been fulfilled with the help of inventions like electrical telegraph, telephone, radio and television. In all of these communication methods, the information from sender to receiver is transported over a certain transmission media, usually air or cable and today even optical fibre. The need for transmission media has lead to a development of communication networks, which have now evolved to a situation where three separated networks can be identified: telephony, data communications and broadcast networks [Arm97].

The overlaid structure of the communication networks today is depicted in figure 2.1. From the figure we can see that broadcast networks comprise of separated local and regional networks, which are designed for high downstream bandwidth and limited upstream bandwidth, providing communication from one to many. Because of the nature of the traffic, the bandwidth in datacom and telecom networks is usually the same in both directions. Differently from broadcast networks, telecom and datacom networks have some common parts in their structures. At least the core network is built in a way that both traffics could be transmitted over the same routes, not necessarily over the same physical network. From these networks, the telecom network was the first one to be built and eventually it reached almost every apartment worldwide[1]. Furthermore, the datacom networks exist mainly inside corporations as separated islands, which are then interconnected forming the Internet. The telecom network is mostly used for voice, but more often it is the end-users' only way to access datacom networks. For this reason, the common parts in telecom and datacom transport networks are the interconnections

---

[1]At least this was the case in industrial countries.

3

Table 2.1: Communication network characteristics in comparison, adopted from [Arm97].

	Telephone world (communication)	Data world (information)	Radio/TV world (entertainment)
Players	Telecom operators and suppliers	Computer and software industries, science	Consumer electronics, broadcasters, cable TV, content producers
Network coverage	Global and ubiquitous (office, home)	Islands, partly interconnected (office), Internet worldwide	Local and regional, scarcely national and continental (home)
Access media (and structure)	Twisted-pair copper, cellular radio (star, circuit switched)	Twisted-pair and coaxial copper, wireless radio (bus or star, packet switched)	Broadcast radio/TV, coaxial copper (tree, non-switched)
Standards	International (long-term oriented)	International or de facto (main players and alliances)	Regional and de facto (main players)

between corporations and the end-user Internet connections. Table 2.1 identifies the most important characteristics of telecom, datacom and broadcast worlds.

The rest of the chapter concentrates on identifying the functionalities of the communication networks today. The main concentration in this contemplation is on datacom networks, because the future communication development is mainly concentrated on this area. The examination is done from a hardware designer's point of view, covering only the lower levels of Open Systems Interconnection (OSI) -networking model [fS94]. Furthermore, telecom and broadcast networks are briefly discussed in various parts of the document.

2.1 Access network

The commonly used definition of access network is described in figure 2.2 [Gro] and the recently proposed interface specification in [MF01]. Access networks collect the small data flows from end-users in the distribution network area, which are then binded into larger flows in the feeder network area. The larger flows are then easier to transport at high speed in the backbone network. This kind of traffic flow behaviour is a result from a centralised service supply. Furthermore, the servers in the Internet are located in certain locations and the end-users need to access the server directly from their home computers. Usually, the end-user who wants to use services from the server are located in another part of the world and

BROADCAST NETWORKS

TV

RADIO

TV

CATV

CATV

DATACOM NETWORK

xDSL

SAN

SERVICE

LAN

Enterprise
Network

TELECOM NETWORK

BTS

BTS

TRANSPORT NETWORK

ADM

MAN

MAN

MAN

OXC

WAN
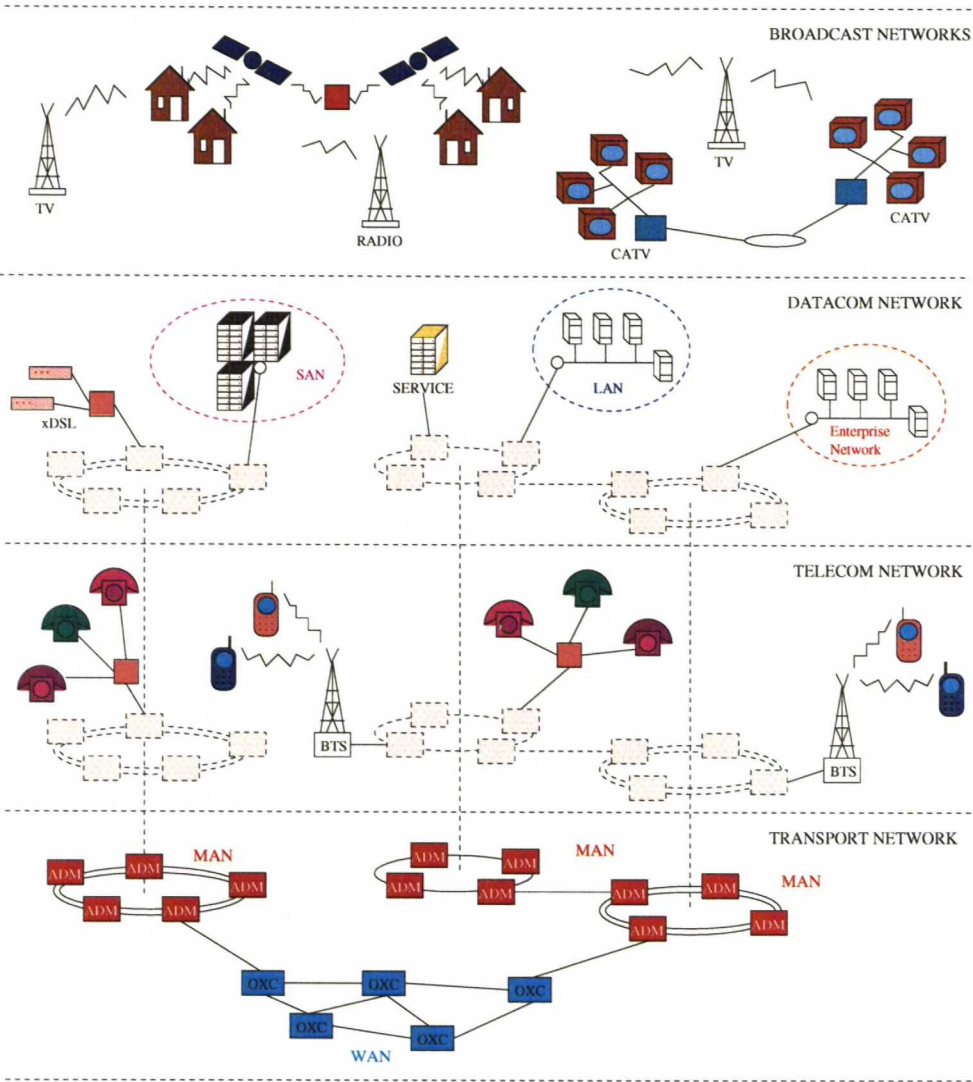
Figure 2.1: The overlaid structure of communication networks.

5
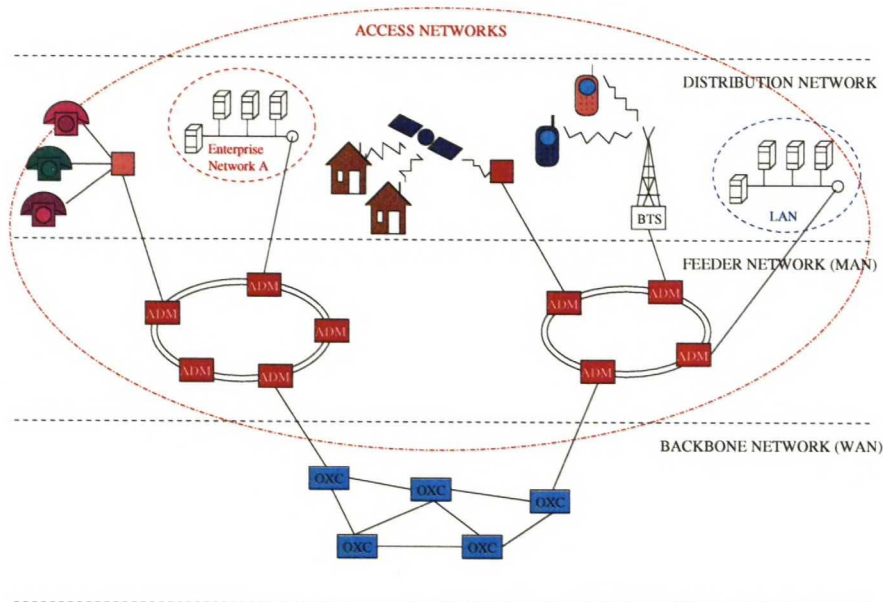
Figure 2.2: The definition of access network.

thus all of the traffic between the server and the user is transported over the core network. With this solution, almost all of the traffic in data networks will go through backbone networks.

2.1.1 Distribution networks

End-users are connected to worldwide networks over their own distribution networks. They have the possibility to access the core network with variety of different technologies available today. The access network acts as an interface between the end-user equipment and the core network, enabling the conversation between technologies located on both sides. Usually this means that the access network needs to make transport conversions from one technology to another and vice versa. Furthermore, the distribution network has a collecting purpose. For example, all of the data traffic from one building is usually collected and transported further over a single channel.

The local operators, who provide most of the equipment and, more importantly, the physical networks for the end users, control the markets in the access network area. Operators have spent a lot of money laying out the telecommunication networks reaching out to every apartment. Because of that, there is a lot of effort put
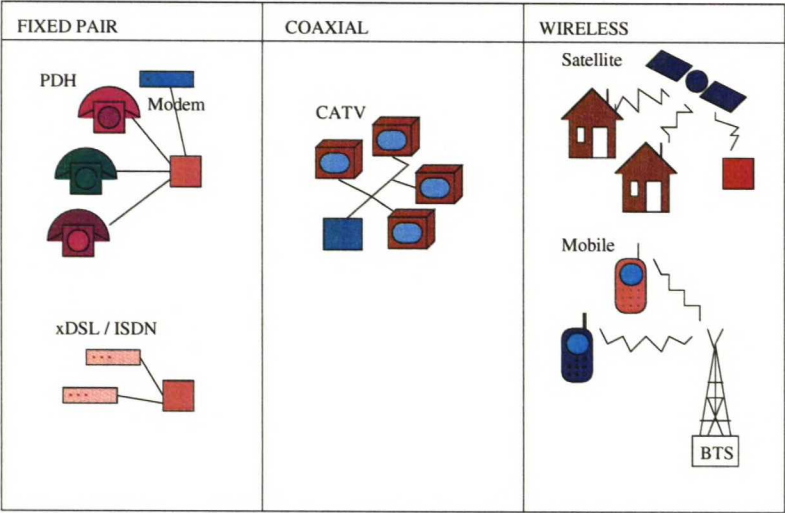
Figure 2.3: Access technologies in today's networks.

in the development of higher transfer speeds in twisted pair networks in order to provide better service to end-users within the existing networks. The efficient use of the old network infrastructure is vital, because in the present financial situation, operators cannot invest much money in building new networks, unless they get the profits from the old networks first.

Technologies

There is a variety of different technologies operating in the distribution network domain. This is mainly because electrical communication has evolved a lot during the time and most of the older solutions are still in use worldwide. It seems that these older solutions do not vanish at all, although new and more efficient solutions continually emerge to the market. Figure 2.3 presents the three main bases of the public access networks installed worldwide [LDA+98].

- **Twisted pair** — This infrastructure was originally installed for Plain Old Telephone Service (POTS) with big financial investments and presents now a large legacy network owned mainly by incumbent operators. However, the digitalisation of this network has commenced in order to support Narrowband ISDN (N-ISDN) and x-Digital Subscriber Line (xDSL) services, which provide a convenient way for the end-users to access the Internet.

7

- **Coaxial** — These networks were originally installed for Cable Antenna Television (CATV), which are analogue in nature and characterised by tree and branch structure, enabling large downstream bandwidth but limited upstream bandwidth.

- **Wireless** — The wireless transmission is quite new and rapidly growing field in digital communications. The air interface has its own limits to data transfer but the benefits seem to be worth the risk as the Global System for Mobile communication (GSM) has already shown to us. On the other hand, new ways to use the satellite transmission systems have emerged and together with the other systems, the phrase: "Future is wireless" does not seem so impossible after all.

Conversions between technologies are usually needed when small data flows are integrated into larger ones or vice versa. For example, telecom networks use Plesiochronic Digital Hierarchy (PDH) for that purpose. However, problems arise when improvements to transmission efficiency are needed and data flows from different technologies are attempted to converge into the same transmission pipe. This is mainly due to the issue that different technologies need different supporting activities, which cannot be efficiently offered at the same time in the same media. For that reason several transmission paths between the same endpoints are needed to build and maintain, which is of course resource consumptive and expensive.

This is mainly the situation between telecom and Storage Area Network (SAN) traffic or Internet and SAN traffic. For example, if a company has a phone centre, a separate data storage and an Internet connection, all of them need to be transported over separate fibres or cables. As an exception, the Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET)[2] technologies provide a convenient way to transport Internet and telecom traffic simultaneously over the same media. However, the data storage traffic cannot be transported with the help of SDH. And because of the implementation costs of the SDH technology, it is not suitable to be implemented outside MAN or WAN.

8
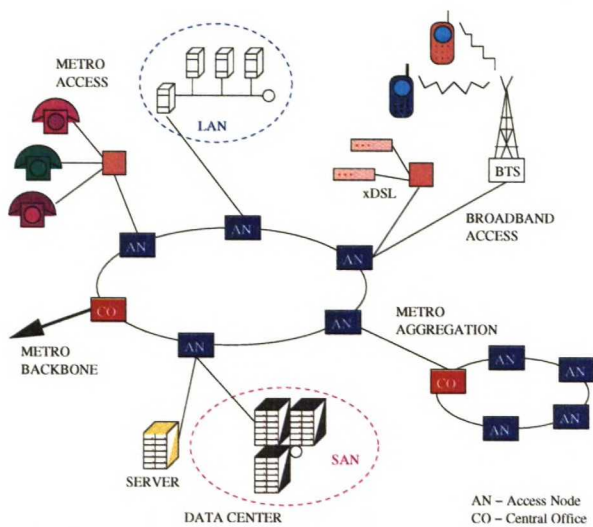
Figure 2.4: MAN traffic characteristics today.

2.1.2 Feeder networks

A typical MAN in today communications networks acts like a feeder network. The MAN has both an abstract and a specific definition, which are both defined in [Net03] with the following phrase:

"Conceptually, the MAN is a set of networks that work together to provide access and services in a metro region. Specifically, a MAN is a single, separate, identifiable "metro area network" that is owned and run by a single network operator, usually a service provider or carrier."

MANs collect the traffic from access networks and then feed it to the backbone network. The traffic in a MAN is typically transparent from access to access, from core to access or from access to core network. Herein the Access Nodes (ANs) are only responsible for separating the incoming and merging the outgoing traffic flows from and to the metro transport pipe. Sometimes, certain Interworking Functions (IWF) may be needed to convert different technologies between each other. Furthermore, Central Offices (COs) act as connection points between other MANs or backbone networks. This behaviour can be seen in figure 2.4, which also presents the different types of access traffic in MANs today [Inc02c] [Mol88]. The different types of traffic in MAN are more deeply discussed later.

---

[2]International Telecommunication Union, Telecommunication standardisation sector (ITU-T) has defined the SONET to be a subset of SDH, the acronym SDH is used in the rest of the thesis to refer both SDH and SONET.

Services

In order to function properly MAN has to offer certain services for access network technologies. First of all, the network configuration needs to be flexible, so that the changes in the network structure[3] can be managed quickly and without disturbing the traffic flow. At the same time the available bandwidth is allocated between different traffic flows in a way that data will not overflow in buffers and the utilisation of the bandwidth is as high as possible. In addition, several other services are provided depending on the MAN traffic type, presented in figure 2.4, and the following will list few of them [CSK88] [MHPG91].

- **Metro access** — This category includes variety of technologies, ranging from newly developed wireless technologies to older ones, which were used already in the early days of communication networks. From MAN, these technologies require the following services: LAN interconnection, support for voice, connection-oriented or connectionless services, switched or non-switched networking between hosts, broadcast and multicast traffic.

- **Broadband access** — This category includes more recent technologies, specialised in one or two way broadband transmission. The broadband transmission technologies over cable (CATV) or fixed pair (xDSL) are older than these newly developed wireless technologies, now emerging to market. Technologies in this category need multimedia, security and mobility enabling services from MAN.

- **Metro aggregation** — This category includes all the traffic between different MANs. This traffic is usually transported over a single pipe, where bandwidth allocation together with traffic monitoring services is required. This stands for both, incoming and outgoing traffic.

- **Data centre** — Technologies in this category are specialised in data processing and data storage. Corporations use data centres and for that reason they require secure and fast connections from and to MAN. In today's networks, connections to data centres use separated fibres, providing low delays and high bandwidths. The server traffic is more one way, from servers to end-users and is not so sensitive for delays.

- **Metro backbone** — This is the interface from MAN to backbone network. The traffic type here is similar to the connecting traffic between MANs, but it usually requires more bandwidth. For that reason the technologies used

---

[3]Adding and removing of nodes, fibre cuts or other errors.
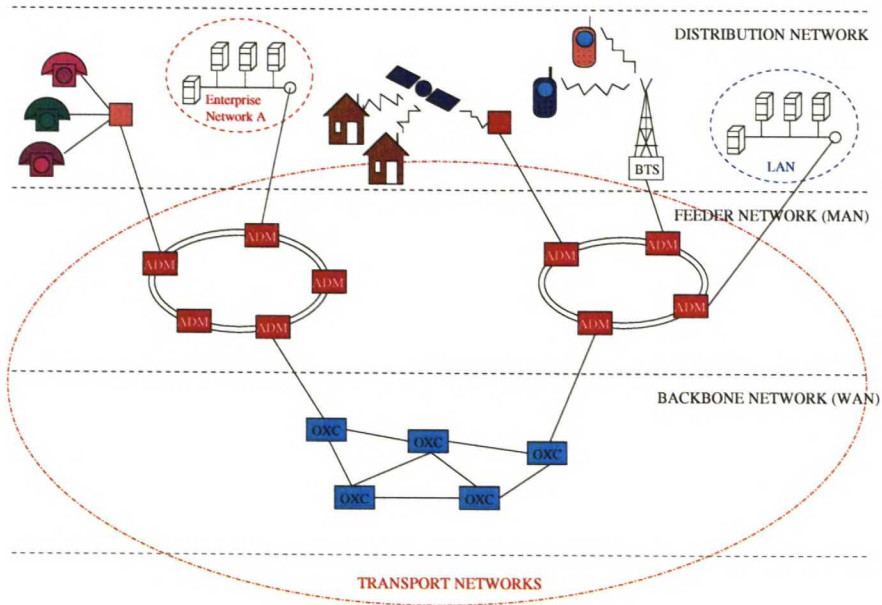
Figure 2.5: The definition of transport network.

here may differ from the technologies used connecting MANs. Depending on the technology (SDH, Asynchronous Transfer Mode (ATM), Packet Over SDH (POS), Dense Wavelength Division Multiplexing (DWDM)), bandwidth allocation and other higher layer management task are needed to support.

One important concept in data networks is the Quality of Service (QoS), which has attracted lots of discussion and is coming more important every day. It is a concept by which applications may indicate and even negotiate their specific service requirements to the network. Furthermore, the purpose is to define ways to guarantee certain delay and bandwidth limits for networking equipment [GJS03]. The need for QoS in networking emerges from the fact that the default service in many packet networks has been the best-effort service, where all applications get the same service. Now the amount of data traffic has increased and it is used in new ways. At the moment, the lack of strict delay and bandwidth guarantees prevents the connectionless transport to emerge into new areas.

2.2   Transport networks

The traffic characteristics in MAN and WAN differ from each other in transfer speed, connection distances and in service models. Still the transport network covers both of these areas, as depicted in figure 2.5. This is because the nature of transport networks is to provide fast data transfer activities, needed in both MAN and WAN. Furthermore, the transport network does not include services other than formed from the need to transfer data efficiently and error free from point-to-point. For this reason, the access network services provided by MAN are part of the feeder network functionalities, splitting the functionalities of MAN between transport and feeder networks.

Transport networks today are mainly optical and their bandwidths depend on the number of light paths included in the system. Adding more light paths into the network, the bandwidth can be increased enormously and the only limit seems to be the price of the equipment. However, these kinds of systems have just emerged to the markets and used mainly in the core network area. Furthermore, the most important transport networks, optical networks are more deeply discussed in section 2.4. In addition, high-bandwidth satellite connections can be used to transport data traffic as well.

2.2.1   Data centric services

In order to transport traffic efficiently, certain transporting functionalities are needed from the underlying network. As transport networks are composed of point-to-point links, the transporting functionalities they provide are mainly concentrated on monitoring the link state and the traffic flow. Herein the transported data flow is transferred as it is, without deeper processing of its content. Transport networks have their own management functions for network configuration, routing and maintenance. These tasks are responsible for forwarding data packets and directing dataflow towards the receiver. The following list will identify the main functionalities provided by data transporting networks.

- **Configuration, routing and maintenance** — These activities are responsible for building and updating of routing tables when the network is configured at the first time or when the structure of the network changes. The change in network structure can happen because of a fibre cut or when old nodes are removed or new ones added in the network. After these functions are performed properly, the forwarding of packets will be automatic.

12

- **Packet forwarding** — This operation is responsible for the forwarding of data packets. In other words, the incoming data packet is transmitted out from a specific port of the routing device. The routing table according to the address of the packet defines the output port.

- **Bandwidth allocation** — This activity is responsible for sharing the available bandwidth between connections or data flows. Higher priority flows will have stable connections and lower priority traffic is transported if there is still bandwidth left in the transportation pipe.

- **Link monitoring** — This functionality is responsible for the monitoring of the state of the transportation link between certain end-points. The management application is informed, whenever the link changes it state. The link can have different states or alarms, depending on the used technology.

- **Traffic balance** — This is an important activity when the full bandwidth of the transportation pipe needs to be utilised. Packet oriented traffic is bursty and it is possible that the channel transportation pipe is not wholly utilised all of the time, or the traffic in the channel exceeds the limit reserved for the channel. To keep the pipe full all of the time, the traffic needs to be balanced in an appropriate way.

- **Error monitoring** — usually the transport network tracks the Bit Error Rate (BER) of the transmission path or at least identifies the erred transmission blocks. In some cases, mainly in wireless transfer, the transmission errors can be corrected to a certain point in the receiver side.

2.2.2 Synchronisation

In the past, nodes in the network were connected asynchronously in a way that every node had their own clocks and the traffic in the network was received and transmitted with this clock. This resulted problems, because electricity[4] propagates at a certain speed. Depending on the distance from node to node, the synchronisation of the received data stream according to the receiver clock could be exact, totally out of synchronisation or something in between. If the network is out of synchronisation, it is very probable that the data cannot be read correctly and for this reason, synchronised networks were developed. The synchronisation resulted in better functioning networks and the transfer speed was increased rapidly together with the decrease in network delay. In synchronised networks, the nodes

---

[4]At that time, networks were all electrical.

13

| POINT–TO–POINT | STAR | TREE | RING | MESH |
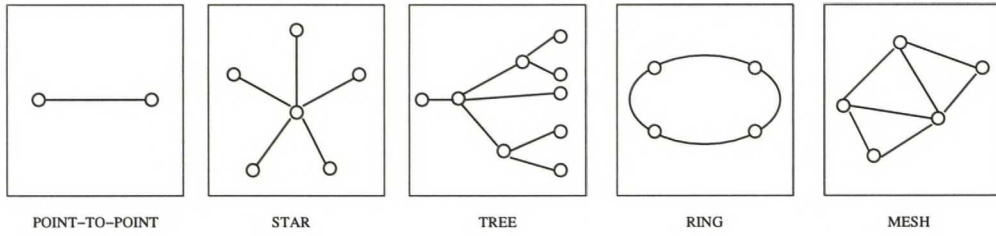
Figure 2.6: Topologies used in networks today.

synchronise their clocks according to incoming data. In the past, networks used general clock distribution as their synchronisation method, but today the Delay Locked Loop (DLL) and Phase Locked Loop (PLL) -methods are more widely used in transport networks world-wide. Together with clock synchronisation the networks need a common frame and network synchronisation methods as well, but these are specified separately within the technology limits [Bre02].

2.3 Network topologies

When building a network, you need to keep in mind, that the chosen network structure asserts certain limits for the functionalities that are possible to implement in the network. Although, some of the functionalities can be changed later by installing appropriate network equipment, it is worthwhile to examine different network structures in detail. Network structures are called topologies and today five types of network topologies can be identified: point-to-point, star, tree, ring and mesh. These topologies are all described in figure 2.6.

The basic building block of networks is the point-to-point link, from which all of the other topologies can be built. Network topology can be physical or logical, physical in how it is built and logical in how the network is configured. This phenomenon is used in datacom networks, where the use of a certain logical topology in a certain physical network can significantly decrease the routing effort. One example of separate logical and physical topologies is the Passive Optical Network (PON), where the physical topology of the network is a tree and the logical topology is a star. This way, a good reachability with easy management operations can be exploited. For further information, PONs are more deeply discussed in chapter 3. Furthermore, the characteristics of each of the presented topology are identified in the following list.

- **Point-to-point** — The point-to-point link is the basic building block of net-

14

works, where the lower level management and monitoring of network concentrates. The management of a point-to-point connection as such is easy and requires little management traffic. However, this is not the case when several point-to-point connections form a large network, because now the whole network is to be managed.

- **Star** — In the star network, every node can reach all of the other nodes through the central node. This results in good accessibility between nodes, but the downsize of this feature is that the central node needs to be capable of handling all of the traffic in the network. This topology is popular in smaller networks, because it is easy to build and maintain.

- **Tree** — The tree structure is widely used in terrestrial broadcast networks, like the CATV, because with this topology all of the end-users can be reached by simply forwarding the transmission down to the network. This results in a low cost and reliable network, because the forwarding equipment is simple and cheap. When this topology is used for two-way traffic, the upstream bandwidth is shared between all the users and often it is quite limited. On the other hand, the downstream bandwidth can be high, depending on the usage of the network.

- **Ring** — The ring topology is the most popular one in the metropolitan area, because it provides good survivability features and spreads over a large area providing good base for the access networks.

- **Mesh** — Nodes in the mesh topology have great amount of routes from one place to another and this results in a very complex network structure, especially when the amount of nodes is high in the network. In this structure, protection and accessibility levels can be high when appropriate routing methods are used. However, finding or developing these methods is a very demanding task and usually results in complex solutions.

2.4 Optical Networks

From the early 1980's, the telecommunication networks have evolved from asynchronous to synchronous and then optical, still trying to reach for all-optical techniques. SDH was the first functional optical network in the telecom driven industry. Now after two decades from its development this network is responsible for most of the transferred telecommunication traffic worldwide. However, it does

not support the transfer speeds typical to the core networks, and other technologies are needed for the purpose. Recently developed optical signal amplification and Wavelength Division Multiplexing (WDM) have revolutionised long-distance transport, resulting in capacity expansion, cost reduction and operations simplification in core networking [ASFG+98].

WDM is a technique where several light paths can be transported simultaneously in one fibre. This technique is already widely tested and implemented in the most important parts of the core networks. It seems that, in the future, this technique will be widely implemented in the other parts of the network as well. However, the complexity of the network management operations increases as the number of light paths in the network increases. This means that the cost of management is high, when there are a great number of light paths implemented in the WDM network. For this reason, the WDM is usually used to increase the capacity of the bottleneck links only. To ease the management operations in the WDM network, the concept called Optical Transport Network (OTN) has been developed. OTNs are WDM networks that have both, traffic and light path management systems implemented. There is a lot of flexibility how these OTNs can be deployed, depending on the transport services to be provided [Cav00]. Furthermore, the next three sections will give a more detailed presentation about the SDH, the WDM and the OTN technologies.

2.4.1 Synchronous Digital Hierarchy (SDH)

SDH was originally designed to replace PDH based networks in transmission of connection-oriented telecom traffic in the beginning of 1980's. At that time the connectionless packet traffic was not common and nobody expected that this situation would change much in the future. During the following years, SDH networks were widely implemented all over the world and SDH is now the most popular network technology used today. However, the nature of the data traffic has changed since the early days, and the optimisation of SDH networks to better support the connectionless data transfer has been a major issue during past few years. The reason for this development is the goal to provide better QoS for the emerging multimedia and real-time services.

The functionality in SDH is based on synchronised and standard sized frames, where the data packet or data stream can be inserted in any part of the frame, pointing its start with a specific pointer [Tek01]. This structure allows efficient monitoring and management functionalities to be implemented and transported inside SDH-headers. Furthermore, these headers give only three percent of extra

16

overhead to the transport. The pointer-processed insertion of data packets or data streams allows the frames to be filled wholly and no empty space is left between packets in the frame. In addition, SDH has its own hierarchical system of how different transmission technologies are inserted, first into containers and then into the SDH-frame [Gor00]. SDH supports electrical and optical transport, but the management of the network is done electrically.

From the network owner, the operators, point of view the optimisation of the old networks to better support the new requirements has been a major goal for their development tasks. Their purpose is to save expenses by exploiting old network infrastructure as much as it is possible. At the moment, it seems that this stands for the survival of SDH networks in the future. There are some advantages in the SDH technology already. It provides very efficient transport services and is the only one available today to transmit connection-oriented telecom traffic in its delay limits, allowing simultaneous connectionless transport. The hierarchical frame structure of SDH enables bandwidth allocation and management between several users, although the legacy contiguous allocation is not so efficient in allocation granularity [OSG02].

Packet over SDH (POS)

Clearly the development of networking has shown that the Internet Protocol (IP) packets would be the most popular form in transporting data in the networks. Few years ago somebody suggested that the most efficient way would be to transmit IP packets directly over fibre, without the complex OSI layer structure. After this the whole industry was talking about "IP-over light" and other synonyms for that. The more optimistic ones actually believed that this hype could be the truth after a few years of research [MBK01]. However, the research efforts made for the goal showed that it was not possible to have efficient transport of traffic without the functionalities provided by these OSI layers [BRM01] and the matter was soon forgotten. However, the discussion brought more attention to the already available IP over fibre techniques, especially easy to use IP over SDH techniques. These are briefly presented in the following list.

- **IP over SDH** — This technique enables the direct transport of IP-packets (Point-to-Point Protocol (PPP) in High level Data Link Control (HDLC) frames) over SDH-link. The transported IP-packet is mapped into a container, which is then inserted into an SDH-frame. This operation does not interfere with the other ongoing transporting actions, allowing other SDH transport as well.

17

- **IP over ATM over SDH** — This technique works similarly as the former one. The difference here is that first the IP-packet is mapped into ATM-frames, which are then mapped into SDH frame. With this method, a lot of bandwidth is lost into overhead, caused by ATM-headers. As a result, reliability and other functionalities of the ATM can be integrated into SDH. Still, because of the overhead, the efficiency of this method is low.

- **IP over Ethernet over SDH** — In this technique ATM is replaced with Ethernet. The use of Ethernet over SDH requires less overhead than the use of ATM over SDH. On the other hand, the services provided by the Ethernet are not as efficient as the ones, provided by ATM. However, Ethernet fulfils the requirements for normal transporting operations quite well.

2.4.2 Wavelength Division Multiplexing (WDM)

One of the research trends in today's networking is the development of all-optical network components and structures. This is an area, where a lot of development is needed before the final equipment can enter the markets. Before all-optical technologies, the WDM technology is the way to exploit the huge opto-electronic bandwidth mismatch in networking. WDM uses a technique called multiplexing, which is defined in [BP01] with a following phrase:

"Multiplexing is the simultaneous transmission of different messages over the communication network through a partitioning of the available bandwidth or other resource".

There are two types of multiplexing used in optical communication, Time Division Multiplexing (TDM) and Frequency Division Multiplexing (FDM), where the FDM is the method used in WDM. With the help of TDM, slower flows can be multiplexed consecutively into one light path, which is then easier to transport at higher speed. After TDM, WDM is used to multiplex the different light paths into the same fibre [Muk97].

By this way, multiple end-users may all have their own channels through a single fibre and the bandwidth of the network can be increased easily. Today the WDM technique is already widely used in core networks, and it is emerging into the MAN area as well. With the help of WDM the available bandwidth now exceeds the limit of 1 Tbps. The price of the WDM system is composed mainly of the number of optical channels needed, because every light path needs its own electrical and optical equipment and their management is complex [Muk97]. For this reason, the cost of the equipment exceeding the transfer speed of 1 Tbps is high.

18
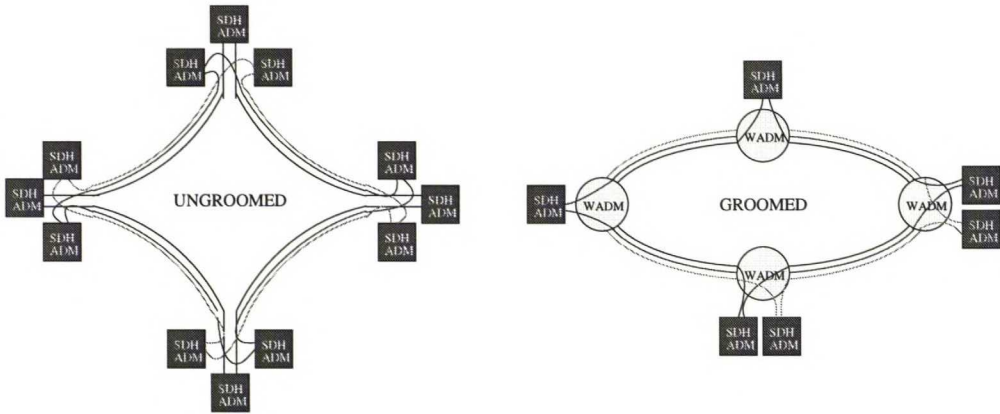
Figure 2.7: Traffic grooming in WDM networks.

Traffic Grooming

At the moment, it seems that WDM systems will be more widely utilised in networking in the future. This means that the number of light paths in the networks is going to increase, which increases the network complexity as well. The increased complexity brings new concerns into routing and network configuration tasks, and new solutions are needed in that area. In addition, every light path needs it own conversion equipment to convert the data from optical to electrical and vice versa. This equipment is relatively expensive, and it is good to try to decrease the number needed. Usually, there is no need to have a connection between each of the nodes in the network. The complexity of the network could be decreased for example by providing certain light paths between certain nodes, leaving some light paths unconnected. By this way the network could be divided into different logical topologies, independently from the physical topology. This manipulation of network light paths is called grooming and it is defined in [BP01] with the following phrase:

"Grooming is an industry term used to describe the optimisation of capacity utilisation in transport systems by means of cross-connections or conversions between different transport systems or layers within the same system".

With the help of grooming, the network could be optimised according to capacity utilisation or the number of Add Drop Multiplexers (ADMs) needed in the network. As an example, most of the traffic in ring network travels through consecutive nodes, which are only responsible for the retransmission of the traffic. The ungroomed situation of an example ring network is presented in the left side of figure 2.7. After grooming, few of the ADMs can be removed and the complex-

19

Table 2.2: The transmission speeds and frame period for the optical transport units in OTN.

Optical channel Transport Unit	Line Rate/Mbps	Frame Period/ms
OTU1	2666	48,971
OTU2	10709	12,191
OTU3	43018	3,035

ity of the network is decreased. This groomed situation is presented in the right side of figure 2.7. The extend of how much ADMs can be saved with grooming depends on the capacity needed between different nodes in the network. This needs to be considered separately in every case. However, the optimisation task becomes quite complex when the size of the network increases. For that reason, new algorithms for the optimisation task are continually been developed [LGP01]. In addition, grooming includes optimisation of multiple transport systems[5] and multiple layers of a single transportation system [BP01].

2.4.3 Optical Transport Network (OTN)

As discussed before, SDH cannot fully exploit the possibilities of the WDM technology. To ease the management tasks in WDM networks, ITU-T study group 15 has defined a new set of recommendations for optical transport networking [IT00b]. These include architectural, interfacing and management issues and from now on, I will apply to all them with the term Optical Transport Network (OTN). OTN has many similarities with SDH, like the hierarchical structure and frame format. This makes sense, because the OTN is an improved version of SDH and regarded as a lifeline to increase the capacity in the future networking [Tec]. Currently, there are three optical line rates defined for OTN, presented in table 2.2. The management of optical channels is the most important improvement in OTN. Furthermore, it has another new feature implemented in it, the Forward Error Correction (FEC).

When the line rate of a certain optical channel is increased, the BER of that channel will most probably increase too. This is because of the dispersion effect in fibres, caused by their physical characteristics. If the BER of the connection increases, more efficient error correction mechanisms will be needed to provide the same reliability as before. FEC is just the method for the purpose, although it

---

[5]Where the technology can be electrical, optical or microwave.

Table 2.3: The improvements in bit error rate (BER) when using forward error correction (FEC) with the Reed-Solomon RS(255,239) coding, adopted from [Tec].

BER without FEC	BER with FEC
10^{-4}	$5,0 \times 10^{-15}$
10^{-5}	$6,3 \times 10^{-24}$
10^{-6}	$6,4 \times 10^{-33}$

brings some amount of overhead into the transmitted frame. At the maximum, the code used in OTN can fix eight simultaneous errors and detect 16 simultaneous errors. This is when the Reed-Solomon RS(255,239) code is used [Tec]. The improvements in connection BER when this code is used are presented in table 2.3.

2.5 Survivability

The importance of survivability in networking has increased over the years and today the survivability issues are taken into account already in the network designing stage [DGA+99]. When designing survivable networks, the ideal goal is to achieve maximum survivability with minimum recovery time while maintaining the maximum resource utilisation. However, all of these goals are difficult to attain at the same time and usually some trade-offs between these goals are needed [ZD02]. Furthermore, the network structure, transmission media and the transmission technology together have their own effects for the survivability and all of these are needed to take into consideration when the network is designed. In addition, the cost of protection[6] could also be considered.

There are various protection mechanisms used in networks today. However, many of these can be used only with certain technology and in certain network structures. This decreases the number of available protection solutions and simplifies the survivability planning of networks. Furthermore, when designing the survivability scheme, we need to know which of the network layers are responsible for the recovery of each failure. Usually the recovery is designed to be quick enough so that the upper layers of the network do not even notice the failure. This means that the lower layers need to handle the protection, restoration and possible data losses in a very short period of time. This can happen only when the protection

---

[6]Bandwidth efficiency and equipment costs.

21

scheme is fully planned in advance [DGA⁺99].

Protection is the primary mechanism used to deal the failure. After the protection function is completed, restoration is used to provide new routes or additional resilience against further failures before the first failure is fixed [GR00]. Protection mechanisms can be divided into electrical and optical protection, which both can be divided into link or path protection mechanisms. At the moment, the communication development is concentrated on optical communication and for that reason, the optical protection methods have experienced great improvements. Furthermore, the optical protection mechanisms can be faster than the electrical protection mechanisms, but more important is that some optical methods can be used passively, requiring cheaper and less complex devices. This is why the optical protection is coming more popular in networking.

Chapter 3

Communication networks tomorrow

In the future the networks are heading towards flexibility and scalability enabling new ways for interoperability. The reason for this development can be derived from the overlaid network model, presented in figure 2.1, and from the emerging new services, which require more speed and new supporting functions from the underlying networks. This means that the traffic in communication networks is once again changing its characteristics. Previously, the change was from connection-oriented to connectionless transportation, but now a third type of traffic is emerging, called the real-time traffic [And02]. The real-time traffic has some of the features from both of the connectionless and connection-oriented traffic, but still the current network structure prevents the efficient transport of this traffic. Furthermore, all of these three network types need to co-exist in the networks. This together with the issues discussed in chapter 2 is pushing the development of communication networks towards convergence. The main target of discussion in this chapter is the characteristics of converge networks.

The problem in today's networks lies in the metropolitan areas, where the complexity of access networks is a real problem. The great number of different accessing technologies has been the reason for slow development in metropolitan area networking for a long time. This is a real problem, because the legacy network structure cannot provide adequate support for the real-time traffic. It seems that the present MAN structure is not going to survive anymore. In the future, MANs need to be more adaptive and more intelligent and this means modifications and developments to the current networks. For this reason, it is quite clear that the metropolitan and access network areas are going to be a target for major developments and improvements in the near future [LDA+98].

The speed of electrical signal processing in today's transport networks is mov-

ing closer to the physical limit of silicon. At the moment, it seems ineluctable that the limit will be reached some day and more advanced systems are needed to develop. The hope for finding faster data transportation methods has increased efforts in the development of all-optical communication solutions, which are considered to be the most technically superior in the long term [LDA⁺98][YYMD01]. The problem in electrical networking is not the bandwidth, but rather the speed of how many packets can be forwarded in a certain time. However, in all-optical networking the forwarding of packets could be faster, because there is no need for opto-electrical and electro-optical conversions. With WDM we can already easily increase the network link bandwidth to meet our requirements, but the management of large WDM networks is a much harder task and the equipment is more expensive. The cost of the equipment is much lower with optical equipment, especially when passive optical network elements are used. Furthermore, the complexity of the management operations may be decreased with optical networking.

3.1 Future characteristics

This section will discuss future network requirements and the realisation strategies concerning future networking in access, metropolitan and core network areas. The areas of research in telecommunications are briefly described together with the requirements and possible solutions for the future networking. The main goal is to find the characteristics of the future data traffic and service functionalities. But first, the most probable structure of the future communication network is illustrated in figure 3.1 [LDA⁺98][SS99][YJH⁺00][STS02][Con89] and more deeply discussed later in this section.

Today, the end-user behaviour has greater effect on the network requirements than it has had before. The wireless communication techniques and end-user equipment are developing rapidly, attracting more and more people to buy the equipment and start using the available wireless services. In addition, the amount of data traffic in communications networks will increase continuously, bringing scalability and multiservice requirements to the existing networks. Furthermore, the operators are tired of maintaining overlapping network structures and are ready to invest on converged network solutions to save money from the management operations and concurrently provide better service for end-users. Even more money could be saved with automatic fault tolerant networks, which could use automatic protection and restoration mechanisms for fast recovery after network failure. In addition, automatic switching and network management issues are coming more important also [HM02]. Yet, the end-users and enterprises are more and more
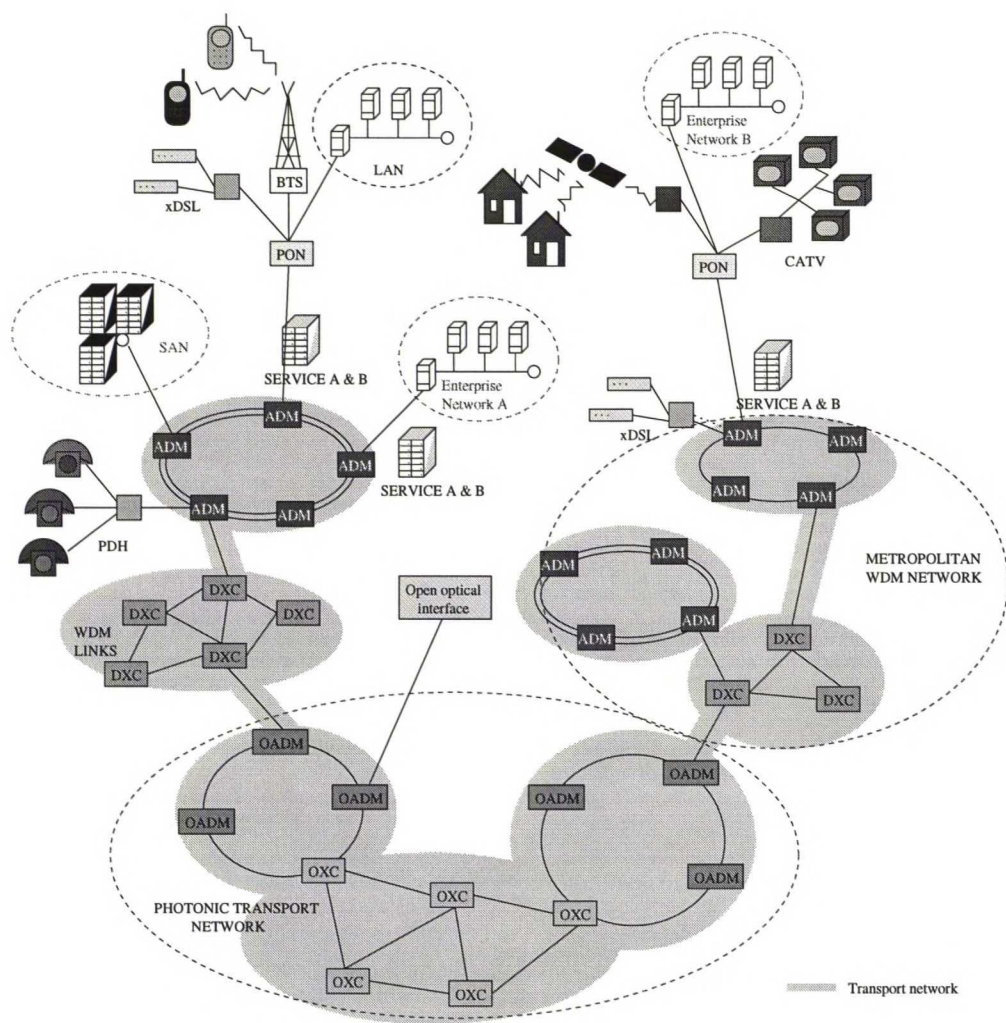
24

Figure 3.1: The structure of the future communication network.

concerned about the network security and information copyrights. These have developed into a major issue, due to Internet banking and shopping. All this has lead to a desire to develop a new kind of network, where traffic flow between endpoints would happen transparently in a way that the underlying network does not see or process the transported data at all.

Transparent transfer is one of the most often mentioned solutions for the problems in today's networking. This is because the network needs to support different kinds of services with different requirements. So far, providing separate networks for different tasks or technologies has been enough. With the help of transparent transfer, different networks could be integrated into single network architecture. In legacy networks, the transmitted data needs to be processed with required way in every network node and to provide the support for all of the available technologies has been out of the question. The transparent transfer provides a way to transport the traffic through the network without technology dependent processing tasks. This is done by encapsulating the data into certain technology, capable of handling the transportation tasks. ATM is one of the technologies providing transparent transfer. The reason why ATM is not used here is the already laid SDH network structures, which are not capable for efficient ATM-transport. On the other hand, the protection and survivability issues in ATM are not in the same level as in the SDH and the amount of overhead in ATM exceeds the amount of overhead in other networks. At least this is the truth so far. Anyway, the opinions on using ATM or other system as a new transport network vary considerably [Sep02].

3.1.1 Distribution networks

It seems that the number of access technologies is not going to decrease in the future but the opposite. This means that a greater number of conversions between technologies will be needed in the future. Supporting all of the needed interworking functions in the future in access region will result in complexity expansion and problems. This is not desirable, and one way to avoid this is to move the interworking functions towards distribution networks. This means that the transparent transfer will reach the access region as well. Together with this, the amount of bandwidth in access networks is going to increase in the near future when the multimedia services will come into the reach of people. The trend can already be seen as an increase of cable and xDSL connections on the end-user markets. At the moment, the most promising solution to solve the bandwidth increase and the interworking problems seems to be the PON, which allows transparent optical data transfer over MANs with low cost passive optical equipment [Com01]. The idea behind this solution is the passive optical feeder network, which collects the data

from the access domain and feeds it to the transport network for the transmission. The PON technology is more deeply discussed in section 3.2.1.

New wireless transmission techniques emerge to the market continuously. There are multiple developed and yet undiscovered ways to use these new technologies, which is why they are recognised as a part of the future access technologies. In the future, mobile equipment will come more intelligent and the need for bandwidth increases. However, it seems that high-speed transmissions cannot be supported over long distances and the user needs to accept the speed he or she gets. The wireless networking is said to move into a direction where mobile equipment can select the best technology for its purposes from all of the available wireless technologies [Tec02]. This switching between technologies does bring new considerations to wireless security. In addition, operators are searching new ways to exploit the existing CATV networks in data transfer as well.

3.1.2 Metropolitan area networks

As discussed before, the metropolitan area networking has been one of the main areas of research. This is because the legacy networks cannot fully support the new transportation requirements. The problem in MAN is the great number of access technologies, which creates complexity. Because of the complex structure, the transport network cannot provide an adequate QoS support. The most popular solution for these problems in the industry seems to be a flexible and scalable optical hybrid network [HV02]. The hybrid network is a network, where one or several transport technologies are supported directly over some other transport system. For example, this is the case in different Packet Over SDH (POS) technologies, where the other technology is supported over SDH. However, the POS solution as such is not flexible and scalable enough, and a scheme called Data over SDH (DoS) is developed for the purpose.

With DoS, the traffic flow between end-points will happen transparently, enabling more flexible transport with dynamic resource allocation and with the base for present and future services [GRF02]. It has a simple layered structure, which on the other side interfaces with access network technologies and on one side with transport network technologies. With this flexible interface, a variety of technologies could be transported simultaneously over a single transport network. This solution will decrease the amount of physical connections needed in networks, because now the telecom, SAN and datacom traffic can be transported simultaneously over a single fibre [MYMN02]. The DoS scheme is more deeply discussed later in the thesis.

27

Although the execution of interworking functions is moving towards distribution networks and end-user terminals, certain services still need to be supported in MAN level. One aggregate of these services is the network security, where the Virtual Private Network (VPN) seems to be the solution for enterprise networking and the IP Security (IPsec) a promising new technique to be used elsewhere. Furthermore, intelligent servers have been developed for some time, and when they are to be installed, services will move closer to end-users and there is no need to access them over the core network. This means that copies of the original service will be stored in the areas where the users of that service physically are. This will be responsible for the moving of the traffic from WANs to MANs [Inc02c]. Furthermore the operation of intelligent servers may require other services as well.

3.1.3 Transport networks

Transport networks today can handle the current traffic quite well. However, it seems that new techniques are needed when the users of the Internet are beginning to use more bandwidth consuming services. Although, the WDM technique is the key for high bandwidth, the speed of electrical data processing in transport networks cannot be increased unlimitedly from what it is now. Furthermore, the opto-electrical conversions are expensive and resource consumptive to implement, which is a major cost for network updates. For that reason, the research on the transport network side has mainly concentrated on developing all-optical or photonic networks, where the transmission would happen without electro-optical conversions and the network switching could be done almost in real-time. Furthermore, the WDM technology with all-optical packet switching is proposed to be the core technology in metropolitan area as well [HM02][YYMD01]. The increase of bandwidth is no longer the main goal in network development. The operators have calculated that one major cost factor for them is the network maintenance. Because of that, they would like to have all of their maintenance functions as automatic as possible in the future. This would mean more survivability features and ease of management, preferably remotely controlled. Furthermore, the characteristic of traffic has changed and to respond for the different transportation needs, networks need to be more scalable and flexible than before. The main issue here is the ability to allocate traffic into different pipes or channels, depending on the QoS requirements. Together with this, error monitoring, correction and protection issues are coming more important [Par02].

28

3.1.4 Optical networks

There has been a lot of success in all-optical networking area, but the real break-through solution or technology is still waiting to be found. It seems that reading information directly from light without opto-electrical conversions is a hard task and nobody so far has figured out how to do it. The research in this field continues intensively, although nobody even knows if any solution is possible to be found at all. In conventional networks, the whole packet is needed to convert from optical to electrical before re-transmitting. This is quite resource consuming, because the forwarding information is located in the packet header, which is only a fraction of the packet. To decrease the needed conversion effort, there have been suggestions that only the packet headers should be converted and the rest of the packet should be forwarded optically according to the packet header information. With this way, the speed of packet processing might be increased in networks. However, the solution requires that the rest of the packet will be stored somewhere while the header is processed. This cannot be done easily, although some solutions have already been found [DHL+03].

Meanwhile the most useful developments in optical networking are the more efficient routing techniques and architectures used in WDM networks. The industry term used to describe them is grooming, which was discussed in section 2.4.2. With grooming, the complexity of the network equipment can be decreased sufficiently. Nevertheless, more complex solutions have also been found, which concentrate on wavelength tuneable transmitters and receivers available to receive multiple wavelengths. However, the use of tuneable transmitters requires an implementation of a complex MAC protocol, because the reservation of the wavelength channels is not possible without it.

3.2 Future technologies

3.2.1 Passive optical networks (PONs)

There has been a hard competition between passive and active optical networking in access network area. The active technology can provide more efficient services to end-users than passive technology, but it needs more maintenance and more expensive components. The cheaper Passive Optical Network (PON) has become more popular, because it can provide low cost and adequate service to end-users [SK03]. It has forecasted to be the next breakthrough solution in last-mile network area. With PON, operators want to get rid of the electrical equipment on
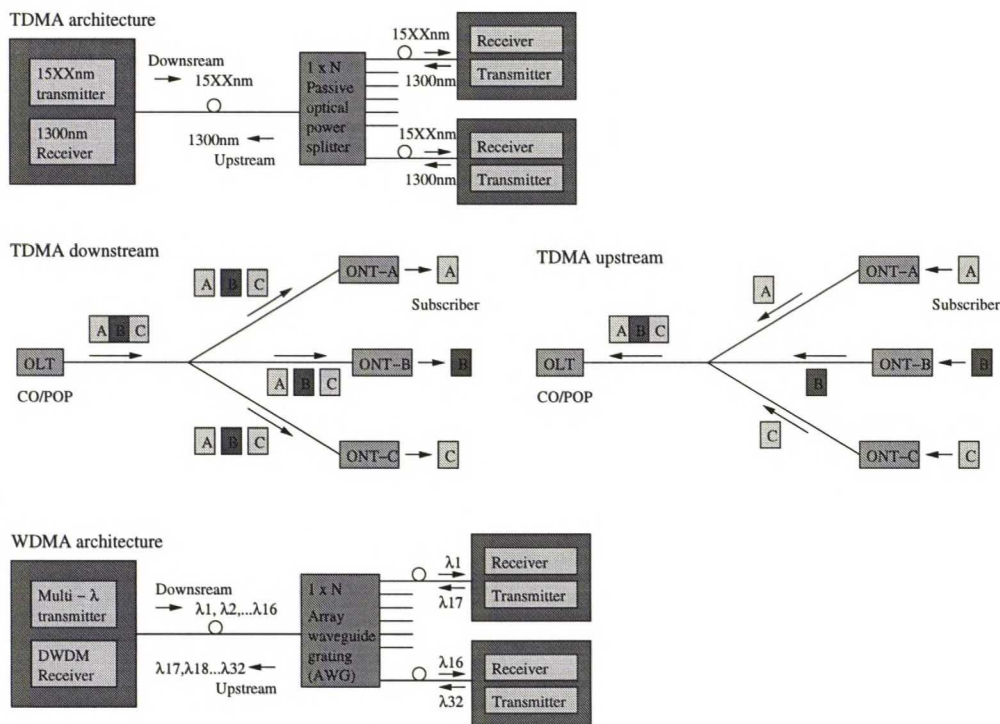
Figure 3.2: The architecture and principle of TDMA and WDMA PONs, adopted from [Com01].

the access network, which has requirements for electrical power and active parts. PON brings the optical network closer to end-users, providing more and cheaper bandwidth for households.

Depending on where the PON terminates, the system can be called Fiber-to-the-x (FTTx), where x can be: C (Curb), B (Building) or H (Home). PON can use single or multiple fibres for upstream and downstream traffic, with or without WDM. The principle of PON is to share the CO equipment and the feeder fibre among as many Optical Network Terminals (ONTs) as possible. This is illustrated in figure 3.2, where the architectures and principles of Time Division Multiple Access (TDMA) and Wavelength Division Multiple Access (WDMA) PONs are presented [Com01].

The establishment of Full Service Access Networks (FSAN) consortium was the first activity in PON area [Net02]. Its goal was to define a common standard for PON technology, which was the ATM Passive Optical Network (APON), announced in 1995 and later renamed to Broadband PON (BPON) [KP02]. Then years passed and the activity in PON area started again in November 2000, when

30

the Ethernet in the First Mile (EFM) task force was established by the Institute of Electrical and Electronics Engineers (IEEE) [SK03]. They were concentrating on standardising a 1.25 Gbps symmetrical PON system for Ethernet transport only. Then as an answer to the EFM's aims on Gb area, the FSAN released the Gb PON (GPON) recommendation [ITU02]. Meanwhile the work in EFM group was concentrated on developing the Ethernet PON (EPON), which is still under development. All of the different PON technologies are presented in the following list.

- **ATM based PON (APON)** — APON was the first PON system and it uses ATM as its bearer protocol. Later it was renamed to BPON, because from the name APON, people assumed that ATM services could be provided to end users, which was not the truth. Now the name BPON reflects the offering of broadband services, including Ethernet access, video distribution and high-speed leased line services. APON system has typical ATM like performance, including large overhead and low scalability with short delays and reliable operation [Net02].

- **Broadband PON (BPON)** — This is the presently used name for APON and it is based on ITU-T recommendations G.983.1 [IT98], G.983.2 [IT00d] and G.983.3 [IT01a].

- **Ethernet based PON (EPON)** — This is IP efficient and low cost PON, based on Ethernet technology. It supports voice transport together with data transport. EPON is scalable, but not so efficient in voice transfer [KP02].

- **Gigabit PON (GPON)** — This is an ITU-T recommendation for PON service requirements for speeds over 1 Gbps. GPON provides high bit rate support enabling the transport of multiple services in native formats and with high efficiency, especially data and TDM. It is the native PON and stands as a foundation for new PONs, not based on APON. In addition, GPON supports ITU-T standard Generic Framing Procedure (GFP) mapping and provides the best efficiency in voice and data transportation [Net02].

- **WDM-PON** — The name DWDM- or WDM-PON is used for PONs, where multiple wavelengths are used. This requires the use of more expensive optical equipment, but enables higher bandwidth [Com01].

One important factor in PONs is the variety of architectures and topologies where they can be used in the network. With this flexibility, the PON can be implemented almost everywhere easily. However, the physical tree, logical star topology seems

to be the most suitable for PONs [GCC92]. Scalability and security issues are also important. With a scalable system the bursts in traffic can be balanced and bandwidth increased easily. Furthermore, when all downstream traffic is sent to everyone in the network, like it is in TDMA PON system, encryption mechanisms are necessary to provide the minimum-security [KP02].

3.2.2 Resilient Packet Ring (RPR)

The Resilient Packet Ring (RPR) standard [Gro03] defines a data optimised network, providing both legacy TDM and differentiated packet-based services. The development of RPR started from the need to combine the advantages of both SDH and Ethernet. The RPR standard supports ring topology and fast protection mechanisms, exclusive to SDH, together with data efficiency, simplicity and cost advantages, exclusive to Ethernet. It is a multi-service transport protocol based on packets rather than circuits. Because of this, it can use the ring topology more efficient than SDH [All03]. RPR has also support for multicast and broadcast traffic together with VPN, which is emerging among companies worried about their data security.

RPR is a OSI-layer two Medium Access Control (MAC) protocol, supporting QoS in three different priority levels: high, medium and low. High priority service supports applications that require bandwidth guarantees and tightly bounded delay and jitter specifications (voice, video and circuit emulation applications). Medium priority applications are not sensitive for delay, but require bandwidth commitment. Low priority is for the best-effort traffic. The fairness control algorithm is responsible for the negotiation of bandwidth between stations and it is also used in congestion avoidance. In RPR, the nodes share the same multicast message and can strip unicast packets from their destination, achieving spatial reuse or bandwidth multiplication [All01].

RPR can operate together with SDH and 1 or 10Gb Ethernet, bringing ring topology's efficient protection available for Gb Ethernet. RPR operates with at least two counter-rotating rings available to transport working traffic. The automatic topology discovery is responsible for the network configuration, enabling automatic updates when the network structure is changed. Wrapping and steering are the protection methods used in RPR and illustrated in figure 3.3. These protection methods allow the restoration of operations in the limit of 50 ms, which is the desired level commonly known in networking [All03].

32
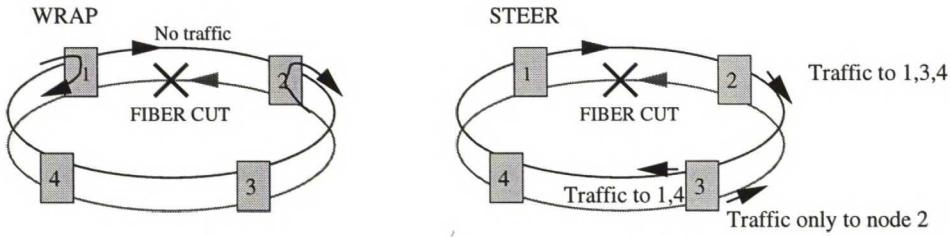
Figure 3.3: Protection mechanisms in RPR.

3.2.3 Data over SDH (DoS)

DoS is a newly developed network scheme to address the problems in today's MANs. It is a transport mechanism that provides means to accommodate various data interfaces into SDH efficiently. The allocation of bandwidth between these technologies can be done without disturbing the existing SDH traffic, e.g. telecom traffic, and it provides more efficient transport for SAN traffic. Together with a reliable transport network, DoS seems to be the solution for the problems in networking today [MYMN02]. It provides adequate QoS to new services and enables flexible transfer of variety of technologies over the same media [SZHVH02]. Together with the newly developed Automatically Switched Transport Network (ASTN) and automatic network configuring, its usability can be even better [BRM02]. The DoS scheme consists of three technologies: Generic Framing Procedure (GFP), Virtual Concatenation (VC) and Link Capacity Adjustment Scheme (LCAS), all standardised by ITU-T and Standards Committee T1 Telecommunications (T1X1) and briefly described next.

Generic Framing Procedure (GFP)

The transport services provided by DoS would not be possible without the development of GFP. It is an encapsulation protocol capable for efficient transport of both block-coded and packet oriented data with the help of its two mapping methods, Frame-mapped GFP (GFP-F) and Transparent GFP (GFP-T). The frame-mapping method provides transporting services for packet-oriented traffic, and the transparent method has a bandwidth efficient way to map block-coded data into the GFP-frame. Actually, GFP creates a transparent layer with two different interfaces, where the other one is the interface to the underlying transport technology and the other one the interface to the transported technology [HVSZ02][GW02]. This functional model of GFP is presented in figure 3.4.

With the help of GFP, variety of technologies can be efficiently transported sim-

33

Figure 3.4: Functional model of GFP, adopted from [HVSZ02].
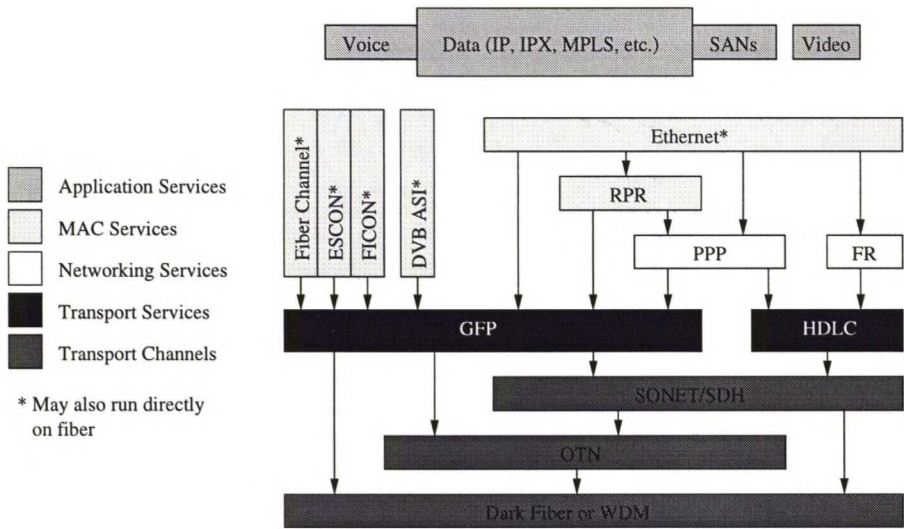
Figure 3.5: The protocol stack of the GFP, adopted from [HVSZ02].

ultaneously over the same transport media. These technologies are presented in figure 3.5, where the location of GFP in the protocol stack is also illustrated. In the future the number of technologies supported by GFP will increase with high probability, especially, if the DoS scheme is adopted by the industry. At this point, it seems that DoS will be implemented widely, because it can use the existing fibre infrastructure, and only the networking equipment need to be changed. So the costs for the implementation of DoS will be low, compared to other new technologies. In addition, GPON already has a support for GFP [Net02].

Virtual Concatenation (VC)

One weakness of SDH has been the lack of efficient allocation of bandwidth, which is very important for operators in today's networking. With efficient allocation methods operators can have better bandwidth utilisation together with improved service supply for their customers. In modern Ethernet links, the allocation of bandwidth can be changed very quickly with fine granularity. This has increased the competition between SDH and Ethernet in the metro and long haul networks. The situation is about to change with the new SDH networking equipment, supporting Virtual Concatenation (VC) and Link Capacity Adjustment Scheme (LCAS) [OSG02].

Table 3.1: The efficiency of virtual concatenation compared to contiguous concatenation. In the table, the acronym VC means Virtual Container, adopted from [HV02].

Contiguous Concatenation	Virtual Concatenation
10 Mb/s Ethernet: VC-3 (20%)	VC-12-12v (92%)
100 Mb/s Ethernet: VC-4 (67%)	VC-3-2v (100%)
1 Gb/s Ethernet: VC-4-16c (42%)	VC-4-7v (95%)

The basic principle of VC is quite simple. A number of smaller containers are concatenated and assembled, to create a bigger container that carries more data per second. This technique provides four advantages compared to the legacy contiguous concatenation used in conventional SDH networks: scalability, efficiency, compatibility and resiliency [OSG02]. More scalability and efficiency is achieved with smaller granularity as presented in table 3.1. VC works in legacy networks as well, and more compatibility is achieved by transporting data channels over old networks that do not support large contiguous channels at all. Furthermore, indi-

35

vidual members of a virtually concatenated channel are routed diversely, providing more resiliency for the transfer.

Link Capacity Adjustment Scheme (LCAS)

The bandwidth allocation with Virtual Concatenation (VC) is done only when the specific channel is configured. It doesn't have monitoring or adjustment functions to address the changes in traffic flow. LCAS is designed for this specific purpose and it can operate only together with VC. With LCAS the allocated channel sizes can be changed at any time without disturbing the traffic on the link. In addition, connectivity checks are performed continuously and failed links restored without intervention of the management software. Furthermore, LCAS can detect if the reserved channel is utilised wholly or not. If there is unused bandwidth reserved for a certain channel, LCAS can adjust the channel and give the extra bandwidth for others to use. In the same way it can also increase the capacity of the channel [OSG02].

3.3 Recent research projects

The research in communication area still continues despite of the recession in IT-industry. Today, several research projects are concentrating on metropolitan area networking. The main targets of the MAN development were already discussed earlier in this chapter and now a few of the recent research projects are presented. All of them concentrate on different sides of the metropolitan area networking. HARMONICS-project concentrates on access network developing and its goal is to create a WDM-PON system to be utilised in the last-mile networks. The MAN transport area is investigated in the project called IP-HORNET, where the goal is to develop a ring structured, WDM-based metropolitan transport network. And the core network side of the MAN is studied in the project called DAVID, where the goal is to develop a common packet-over-WDM transport solution for both MAN and WAN.

3.3.1 HARMONICS

Hybrid Access Reconfigurable Multi-wavelength Optical Networks for IP-based Communication Systems (HARMONICS) is a research project running from May
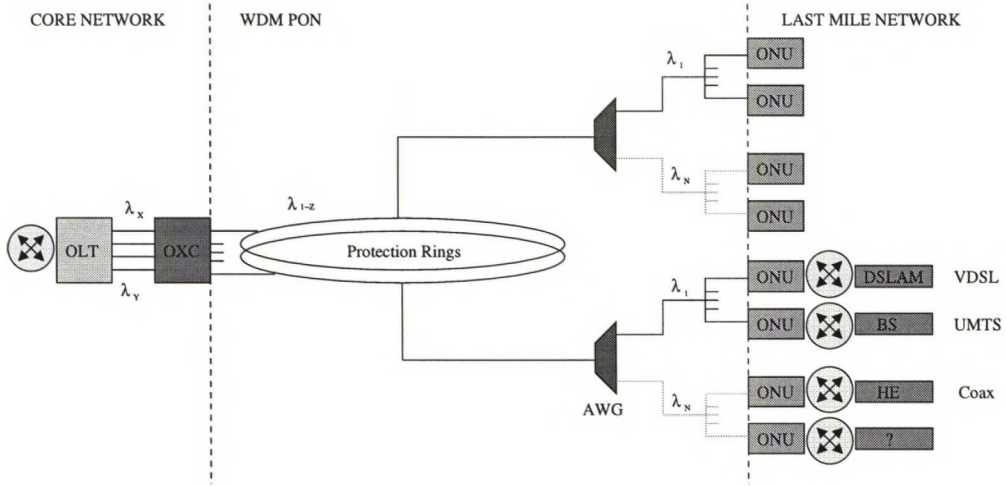
Figure 3.6: The architecture of the HARMONICS project, adopted from [EUb].

2000 to April 2003 within the framework of the Information Society Technologies (IST) programme of the European Union. The main objective of the HARMONICS consortium is to stimulate the convergence of access networks by realising a dynamically configurable fibre based feeder network infrastructure. The architecture of the HARMONICS network is presented in figure 3.6, where two main parts can be identified. First, the last-mile network connects end-users to the core network and any last-mile network capable of providing broadband QoS access is applicable in the HARMONICS system. Second, the optical feeder network either feeds the last-mile access networks or it directly connects the users to the core network [EUb].

The major innovation of the HARMONICS system is the WDM-PON that facilitates multi-Gbps capacity to a large number of Optical Network Units (ONUs) by means of a real passive network. The reference architecture studied in the project consists of up to a thousand ONUs. Sixteen ONUs share a wavelength channel, while eight channels are multiplexed on a fibre using passive Arrayed Waveguide Gratings (AWG). A total number of eight fibres are connected to an Optical Cross Connect (OXC) from protection rings. The OXC performs fast optical packet switching to a number of receivers at the Optical Line Termination (OLT). By doing so, the network is capable of redirecting the capacity to different locations, depending on the load. A novel wavelength-and-time MAC-protocol is designed to control the access of the ONUs of the different wavelength channels, as well as actuating the OXC.

As a conclusion, the most important achievement in this project will be the WDM

37
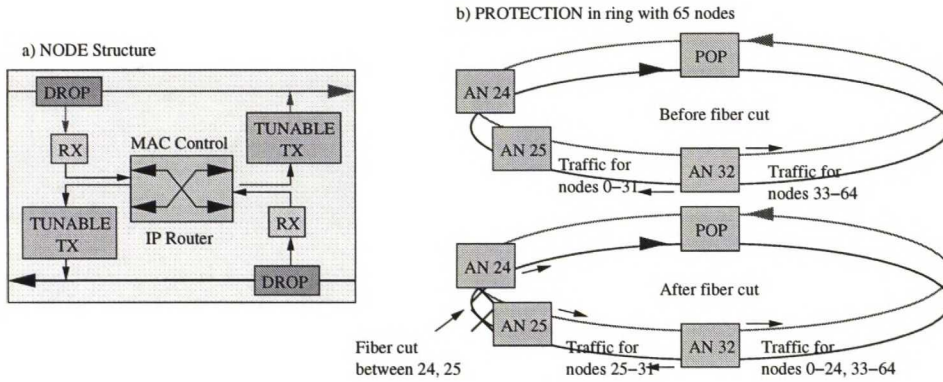
Figure 3.7: The architecture of the IP-HORNET project, adopted from [Lab00].

PON system together with the MAC protocol developed to control the optical channels and their TDMA allocation tasks. Already, the preliminary results had proven that the system can technically cope with the service demand and with the flexibility expectations of the network. Furthermore, together with the optical network results, two technologies: xDSL and HiperLAN/2 are more deeply studied in this project.

3.3.2 IP-HORNET

IP-based Hybrid Opto-Electronic Ring Network (IP-HORNET) is a next generation Internet project at Stanford University. The goal in the project is to address the needs of future MANs. The first generation called HORNET finished at 2000 and the development of the second generation began right after. The study in IP-HORNET concentrates on metropolitan WDM-rings and the data is transmitted directly over them, eliminating the need for inflexible SDH transport. The nodes in the ring use tuneable transmitters and fixed receivers and each node can be reached by transmitting with the wavelength, fixed to the receiver of that node. The structure of IP-HORNET node is illustrated in figure 3.7(a).

However, with this system, collisions in the network are most likely without specifically designed MAC-protocol. The MAC-protocol in IP-HORNET uses a separate control channel to transmit information about the states of the channels in the network. The transport frames are of fixed size and the information if the following frame of the channel is used or not is transported over control channel for each of the channels consecutively. With this configuration, it is possible that the transmitted packet is too large to fit in one frame. If the next frame is used,

38

information about an incomplete packet is included in the last byte of the frame and the transmitting of this packet continues when the next free frame is found in the same channel [Lab00]. Furthermore, the protection in IP-HORNET is carried out in a way that after fibre cut, the network is reconfigured to transport the traffic over existing routes, as depicted in figure 3.7(b). In the worst case, the performance of the network is the same as before the fibre cut and the restoration time is the same as the propagation delay in the fibre[1] [Lab00].

One of the results of the IP-HORNET project was the development of new architecture for the next generation metropolitan area network. With this architecture, the network infrastructure costs can be dramatically decreased compared to conventional networks. However, because of this structure, specific MAC and fairness protocols were needed to develop. This brings more costs to the design, but it is still cheaper than conventional solutions. A new survivability scheme was developed, providing full survivability after one fibre cut or node failure. The main developments were a new suite of protocols and the three new subsystems, a fast-tuneable packet transmitter, an asynchronous packet receiver and a linear optical amplifier [Lab00].

3.3.3 DAVID

The Data and Voice Integration over DWDM (DAVID) project contributes to key action IV of IST on "Essential Technologies and Infrastructure". The main objective is to propose a packet-over-WDM network solution, including traffic-engineering capabilities and network management, covering the entire area from MAN to WAN. The project will utilise optics as well as electronics in order to find the optimum mix of technologies for future very-high-capacity networks. In the metropolitan area region, the focus is on implementing MAC protocol for optical MANs. In the wide area region, the architecture of the project is multilayered, employing packet switched domains containing electrical and optical packet switches as well as wavelength routed domains [EUa].

The architecture of the DAVID network demonstrator is presented in figure 3.8, where the WAN consists of connected Optical Packet Routers (OPRs) and the MANs from several ring networks, which can share the same physical network. These ring networks, which consist of Optical Packet Add/Drop Multiplexers (OPADMs), are connected to the core network through a HUB. These networks have a unified control system called the Multi Protocol Label Switching (MPLS).

---

[1]Less than 1ms in a typical MAN.
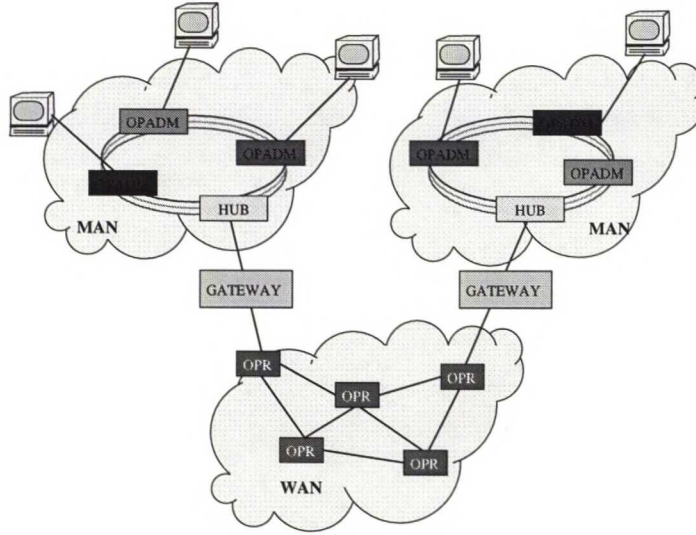
Figure 3.8: The outline of the DAVID project demonstrator, adopted from [EUa].

The duration of the DAVID project is from July 2000 to July 2003 and the results of the project have not been fully revealed yet. However, some of the findings can already be mentioned. First of all, optical networking is on its way, but still expensive. Second, the IP-over-DWDM solution for high capacity networks is not likely to be flexible, because IP is not as suitable a solution as single data-transport technology in the core network. And last, IP will be an important client layer interface for many years, especially when it can be the integrator for efficient control structures like MPLS and Generic MPLS (GMPLS) [EUa].

3.3.4 Discussion

All of the projects presented here concentrated on metropolitan area WDM net-working. In this area, dynamic wavelength allocation is the most popular method, although the utilisation of dynamic channels needs the implementation of the MAC-protocol [Ben02]. In addition, static wavelength-channels can be used to-gether with dynamic channels. The ring network seems to be the most desired physical topology for the metropolitan feeder network, because of the protec-tion capabilities it provides. Some studies concentrate on standards, which have already been developed or are under development, but others concentrate on find-ing new ways, which might be developed into standards later. The last-mile net-work will develop towards passive optical network solution, which can be seen from the number of solutions available in that area.

40

Chapter 4

Research project OAN

Optical Access Networking (OAN) is a TEKES-funded research project where VTT[1] Microelectronics, VTT Information technology and HUT[2] Networking laboratory together with few private businesses are participating. The duration of the project is three years and it will end in December 2003. The goal in OAN is to study metropolitan area networking, find the future requirements and development directions of that area and based on the results, eventually build a network demonstrator. The work is divided between different institutes in a way that the HUT Networking laboratory is responsible for the traffic modelling and algorithm development, the VTT Microelectronics is responsible for the implementation of the optical transport network and the VTT Information technology is responsible for the implementation of electrical parts and controlling software for the demonstrator.

4.1 OAN test network architecture

After some study in the metropolitan area networking, it came clear that the most usable and later expandable solution for the OAN demonstrator should be based on standards. In that time, the scheme called DoS was gaining great favour among specialists and when it was to be standardised, it was selected as the main architecture for the OAN test network. In addition to standardisation, DoS has other strengths as well. These were already discussed in chapter 3 and were notified in the final network architecture decision. The most important strengths were the

---

[1]Technical Research Centre of Finland (VTT)
[2]Helsinki University of Technology (HUT)

RPR	Ethernet	MPLS	PPP		
GFP				ATM	PDH
SDH / OTN					
WDM					

Figure 4.1: The network layer protocol stack of the OAN test network.

ability to use SDH or OTN as a transport technology and the support for simultaneous transfer of multiple technologies over a single transport technology. Furthermore, DoS provides the necessary flexibility and prerequisites for the possible future development of the OAN network architecture.

Although, DoS supports multiple technologies, some others like ATM and PDH need to be supported as well. Technologies supported by the OAN test network can be seen in the protocol stack, presented in figure 4.1. After the first stage of the network is operational, other functionalities can be added easily. Furthermore, the cost of the infrastructure has played an important role in the design of the OAN network, because only the most cost-effective solutions will success in today's markets. The selection of DoS was a major step towards cost savings and even more savings can be gained with the optical transport network solution, discussed later [Kai02].

The development of access network is not in the scope of the OAN project and only standard technologies will be supported in the access network side. The access network interface is implemented into a separate interface-card and the transport network interface to a separate router card. Data between these cards is transported with the help of specific transport protocol and a dedicated bus system. The system allows the interconnection of multiple router and interface cards, providing a considerable amount of flexibility for the OAN in the future. By developing a new version of the interface card, other technologies can be supported in the access network side. On the other hand, the functionality of the hub can be implemented easily with multiple router cards. This kind of support for modular structure is essential if the OAN network will ever to be commercialised. In the first revision of the OAN interface card, two Gb Ethernet and 2,5 Gbps SDH are supported as access network technologies.

The OAN transport network has ring as the physical topology and star as the lo-

42

gical topology. These are selected because the ring structure has efficient protection capabilities and the tree structure is cost effective. The OAN network attempts to fulfil all the requirements for future MANs, presented in chapter 3. The support for these functionalities is mainly based on DoS and in other functionalities supported by it. Furthermore, the OAN network utilises automatic configuration and Automatically Switched Transport Network (ASTN), and the management of the network is carried out with a standardised network management protocol, Simple Network Management Protocol (SNMP). However, at the first stage of the OAN test network implementation, only DoS will be implemented and other functionalities, like VPN, are left for later implementation.

4.2 OAN test network prototype

Prototype implementation is an important part of device centric development. With a fully functional prototype, early research conclusions can be tested and verified. Usually, the faults in the design development can be seen in this stage only. The first OAN prototype is planned strictly for testing purposes, and it will be used to test different metropolitan area networking schemes. The functionality of the prototype can be modified or increased whenever necessary, and these improvements can be easily verified right after implementation. This flexibility in the design is provided with Field Programmable Gate Arrays (FPGAs), which are responsible for most of the network functionality. The functionality of the FPGA is carried out with a specific program, downloadable to the chip. New programs can be downloaded to the chip whenever there is need to change the functionality of the FPGA. The OAN prototype has three different FPGAs, which provide relatively large amount of programmability, compared to the use of programmable logic today. Furthermore, these FPGAs have a great number of connection points and every important chip in the prototype is connected to them.

The implementation of the OAN prototype will be executed in co-operation between VTT Information Technology and VTT Microelectronics, which both have their own responsibility area in the project. VTT Information Technology is responsible for the design and implementation of the electrical part of the network, including all of the networking activities, starting from the link layer. VTT Microelectronics is responsible for the implementation of the transport network, which is a WDM network with optical protection. The physical equipment of the OAN node is fit into a standard CompactPCI-frame, which makes the node easy to install and move. The CompactPCI-frame includes a Central Processing Unit (CPU) card, which is used by the management software.
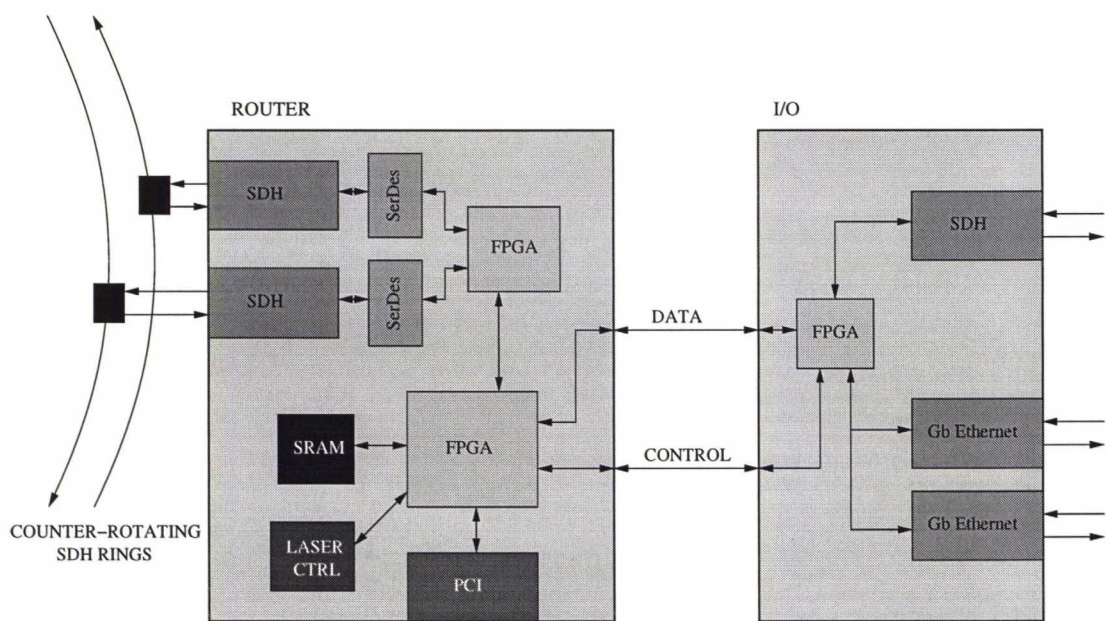
Figure 4.2: Simplified architecture of the OAN test network prototype node.

4.2.1 Functionality of the node

The design of the OAN prototype router and interface cards started with the identification of necessary supporting functions and interfaces. These were the control interface towards CPU, laser controller, test Light Emitting Diodes (LEDs), test points, connections between cards and the power supply for the system. The CPU can access the devices in the prototype through Peripheral Component Interconnect (PCI) bus. The interface is implemented with a specific PCI-interfacing chip. After the supporting functions were identified, it was time to specify the actual benefit functions of the system, the network functions. In the network part, the prototype exploits two counter-rotating 2,5 Gbps SDH rings with Automatic Protection Switching (APS) in the transport network side and two Gb Ethernet links together with one 2,5 Gbps SDH link in the access network side. The simplified prototype layout is presented in figure 4.2, where the different devices together with the connections between them are illustrated. Furthermore, the devices in the OAN prototype are presented in more detail in table 4.1.

SDH framing is a fully standardised procedure and there are several dedicated chips available for the purpose. In OAN prototype, the PMC-Sierra produced PM5381 chip was selected to be the SDH framer in both, router and interface (I/O) cards. To fully exploit the possibilities provided by Sierra's SDH chip, specific

44

Table 4.1: Devices attached to the OAN prototype node.

Type	Manufacturer	Location	Function
XC2V1000	Xilinx Inc.	I/O	FPGA
XC2V2000	Xilinx Inc.	Router	FPGA
XC2V6000	Xilinx Inc.	Router	FPGA
PM3386	PMC-Sierra	I/O	2x Gb Ethernet
PM5310	PMC-Sierra	Router	TelecomBus serialiser/deserialiser
PM5381	PMC-Sierra	Router&I/O	2,5 Gb/s SDH/SONET framer/deframer
PCI9030	PLX Technology	Router	Interface to PCI

TelecomBus serialises were needed to access the TelecomBus-line of the SDH-chips. With TelecomBus, the SDH data flow can be accessed with byte by byte basis, which is necessary for the DoS functionality. These serialises were PMC-Sierra's PM5310-chips, which are connected into the smaller FPGA (XC2V2000) in the router card. Furthermore, the smaller FPGA is connected to the larger FPGA (XC2V6000). The control channel from PCI, additional Static Random Access Memory (SRAM) together with the laser controller equipment are all connected to this FPGA as well. The interface card has only one FPGA (XC2V1000) and two PMC-Sierra's chips. One is the SDH framer and the other is a two port Gb Ethernet (PM3386). Both of these chips are connected to the FPGA, which is further connected to the larger FPGA in route-card.

4.2.2 Network structure

To keep the network complexity low, the OAN prototype network consists of only three to four nodes. One of the nodes works as a hub, connecting all of the other nodes to the core network and to each other. These connections are carried out with the help of WDM technology using Wavelength Add Drop Multiplexers (WADMs). With WADMs, all the nodes can strip their specific wavelength from the ring and by using wavelength tuneable transmitters, every node can have a single light path to the hub and back. This structure is depicted in figure 4.3(a), and its purpose is to avoid complexity and reduce the amount of intelligence in the network. In other words, the most desirable solution for the network would be physical ring — logical ring, where every node would have the ability to transmit data directly to all of the other nodes. However, this solution demands expensive wavelength converters to be installed in every node, together with a complex network management protocol. Because the most of the traffic in MAN is transmitted from or to backbone network, the more appropriate solution for the MAN

45

a) Physical ring, logical star topology in OAN　　　　　　**b) Data transfer procedure in OAN**
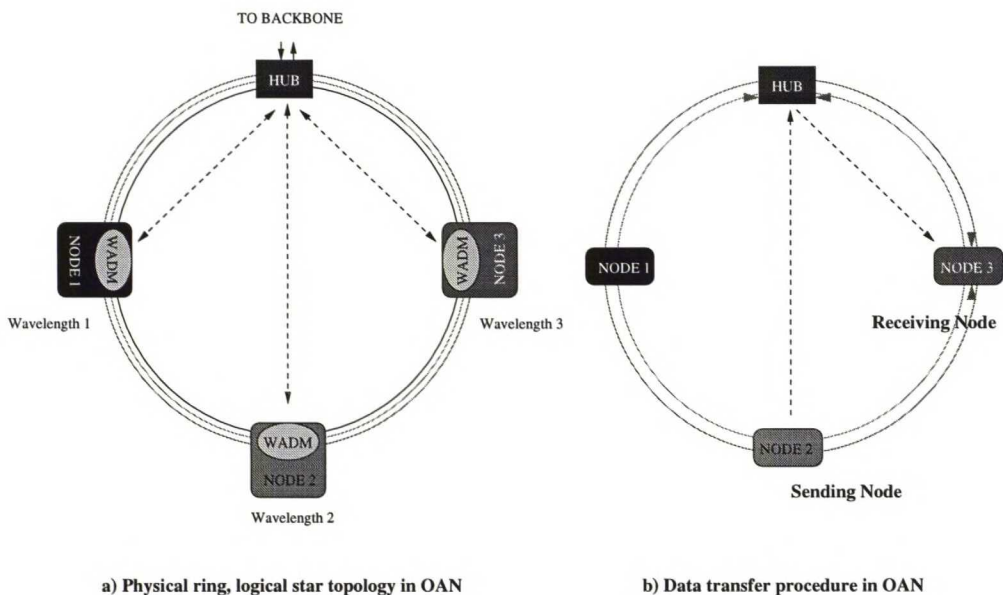
Figure 4.3: The network structure and data transmission process in the OAN test network prototype.

topology is the physical ring — logical star -network, which is the structure utilised in the OAN transport network [Kai02]. Furthermore, there is an option to add dynamic optical channels to the network later on, but this requires the implementation of the MAC-protocol.

The physical ring topology allows the realisation of all-optical network protection system, where the interaction of electrical network components is not necessary at all. This is contrary to the SDH's APS, where the detection of the link failure and the protection are done electrically. Although, the protection in the OAN is fully optical, the APS system will be implemented and tested as well. Furthermore, some kind of intermediate form from these two can be also developed. In the all-optical protection, the signal is transmitted to both directions in the ring. The receiver side compares the powers of the signals from both directions and selects the strongest one to be forwarded to the receiver. In this protection method, the size of the network has some effect to the operation efficiency, but the influence is inconsequential in the scale of typical metropolitan areas. Furthermore, the node to node data transmission procedure in the OAN test network is illustrated in figure 4.3(b).

46

Chapter 5

FPGA programming methodology

There are number of issues involved in the Hardware Description Language (HDL) design, especially if it is targeted to FPGAs. These issues together with the design methodology and implementation procedures are presented and briefly discussed in this chapter. The purpose of this discussion is to provide basic knowledge about the FPGA programming. In the programming process, desired functionalities are first described with a specific programming language and then downloaded into the FPGA device. The description languages used in HDL-programming are VHSIC Hardware Description Language (VHDL) and Verilog. Writing of the description, i.e., programming, can be done by an individual or several programmers, depending on the size and implementation time of the design. All programmers, as individuals, have their unique way to create code. Usually, the variety in coding styles is not desirable, especially if there is a need to make modifications or use the code afterwards. For that reason, clear coding principles and rules for operations are necessary for the programmers. This is the only way to get more unified code, the functionality of which can be easily understood.

5.1 FPGA basics

The FPGAs today provide lots of flexibility into the designs and for that reason, they are coming more and more popular among hardware designers. The flexibility comes from the possibility to program the chips over and over again and decreases the number of re-designing stages in prototype manufacturing. The re-programmability provides advantages compared to the Application Specific Integrated Circuit (ASIC) chips, which ones ruled the market. Opposite to the ASIC,
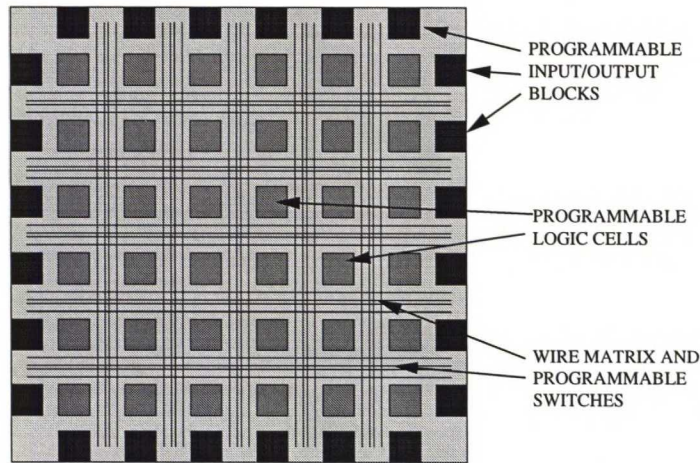
Figure 5.1: The basic structure of the FPGA-chip.

FPGA program can be tested and downloaded into the chip after the chip is manufactured. By this way, there is no need for a separated manufacturing verification, which needs to be re-designed every time the functionality of the chip changes. Furthermore, the re-programmability decreases the number of required prototype re-designing rounds. For these reasons, the FPGAs are mostly replacing the ASICs chips in prototyping. Because of the decreasing prices, FPGAs will be used more and more inside the final products as well. Furthermore, there are several FPGA manufacturers in the market, which all have several different FPGA models. The number of functionalities provided in a single chip is increasing rapidly, because of the hard competition. It has been forecasted that the gate count in one FPGA chip will be around 200 million in year 2005 [Bai03]. FPGAs are composed of programmable logic cells, programmable input and output pins and some architecture specific features, like multipliers, which are all connected together with the help of a programmable switch matrix. The common structure of a FPGA chip is illustrated in figure 5.1.

One has to keep in mind that the composition of the selected FPGA chips has effects on the design principles and so in the HDL implementation process. This is because different chips have different functional characteristics and the programming of these chips cannot be done similarly. For this reason, before the selection of the FPGA chip, it is good to have some understanding of the design to be implemented.

5.2 HDL-implementation process

The common HDL-implementation process consists of three aggregates, which all have their own responsibility area in the process. These are design planning stage, implementation stage and verification stage. Implementation and verification stages work together forming the design flow, where the result of the verification determines if modifications to the code are needed or not. Sometimes re-writing the code is not adequate to fix the error and modifications to the design specification may be needed as well.

5.2.1 Design planning

The most important task in the implementation process is the creation of the design specification document. This is the most important document during the whole implementation process and everything later on is based on the solutions presented in here. The design specification document covers the functionality of the whole design. The specification starts from the overall architecture and purpose of the design and then moves deeper into details. Depending on the design functionalities, the architecture is partitioned into several blocks and sub-blocks. Then the functionality of each block is described with necessary technical details. Furthermore, all of the interfaces between design blocks need to be specified with detail, so that combining of the blocks in the implementation stage would be as straightforward as possible. The specification document must be prepared with great carefulness, because all mistakes made here have multiple effects on the later implementation tasks.

5.2.2 Design flow

The coding of design blocks may begin after the design specification document is ready. The coding of components is only a part of the whole HDL design flow, which consist of several operations. These operations test, simulate and modify the code, forming the final FPGA specific version of the program. The design flow from the Xilinx point of view [Inc03] is presented in figure 5.2.

In the design flow, the code is verified and fixed as many times as it is necessary to fulfil the requirements stated in the specification document. After this, the code is synthesised and the correctness of the synthesis process is validated with simulation. Then the synthesised design is converted in the FPGA specific form,
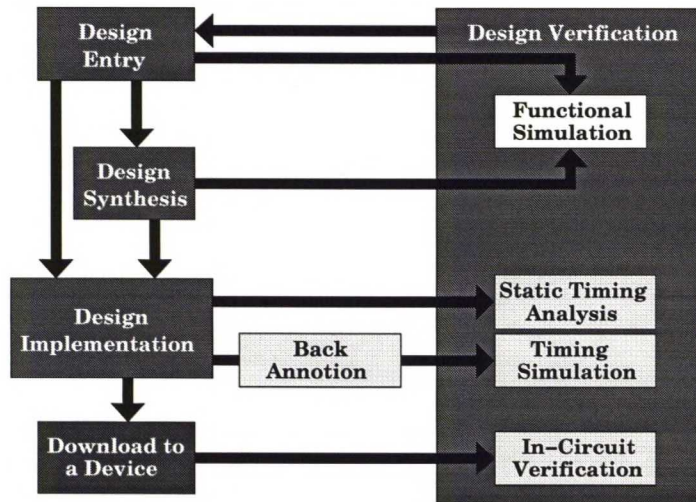
Figure 5.2: The HDL design flow according to Xilinx, adopted from [Inc03].

where timing simulation and static timing analysis can be done. If the timing analysis is not passed, some modifications to the design will be needed. After the analysis is passed, this FPGA specific form of the code can be downloaded into the FPGA-chip. The final functionality of the chip can then be validated with in-circuit validation.

5.2.3 Verification

The verification of the design can be performed in several hierarchical levels, at the same time with the design integration. By this way, different abstractions of the code can be verified efficiently. The validation is only responsible for verifying the functionality of the final design, and it does not test the functionality of the blocks with the same detail as it is possible in hierarchical verification. Validation is important, but it is not as good in locating errors as the hierarchical verification. Verification includes a lot of debugging. Debugging means that after a verification error, the code is fixed and then verified again as long as there are errors in the code. However, it is nearly impossible to define such a verification process or system that all of the possible error combinations can be checked. For that reason, there are always some errors left in the code when it is released to the market and users of the program act as final testers. Partly, this has lead to a situation, where more and more testing is left for the final users. Programming companies have cut down their manufacturing testing efforts and improved their supporting functions. With efficient support, problems in code can be fixed right after they have been

50
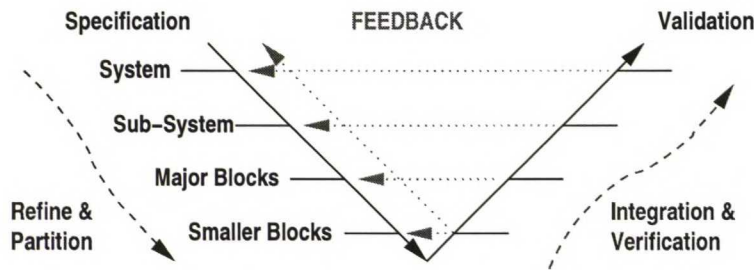
Figure 5.3: Verification as a part of design implementation process, adopted and modified from [Bai03].

noticed, and even more testing responsibility can be left for the users.

The verification process is usually performed from bottom to top by starting from bounded functionalities or small blocks and then moving towards larger aggregates, finally reaching the top level of the design. This is contrary to the process of creating the design specification document, where the refining and partitioning is done from top to bottom. The verification process as a part of implementation process is illustrated in figure 5.3. The verification process takes usually 50-70 percent of the total design implementation time. For that reason, it is advisable to build a verification plan for the design [Ber00]. The verification plan is a specification document, where the verification effort is specified. This includes the schedule and resources available for the verification, i.e. the personnel and the needed time. The verification specification document is build from the design specification document. Furthermore, in larger corporations implementation and verification might be done separately in different departments and then the verification personnel prepare the verification specification.

5.3 Design guidelines

There are a variety of different matters advisable to consider before the actual implementation can be started. These matters are called coding guidelines and they will help in creating clear design structures and understandable code, improving re-usability of the code. Furthermore, reductions in the total implementation time and in the possibility for functional problems can be achieved with good coding guidelines [Ope02]. Sufficient commenting and clear structure helps in understanding the functionality of the code. Furthermore, using common naming conventions throughout the design helps in identifying the different parts of the design or following certain signal through the architecture [Cor99].

51

A great number of different data files are produced in the HDL-implementation process and to manage these files, a clear file structure is needed to create. This structure is good to design already in the beginning of the project, so that all files are in right places right from the start. Furthermore, the purpose for which the code was produced has a big effect on the syntax of the code. The syntax can be quite different depending on whether it is implemented for simulation or for synthesis. In addition, the code can be produced in a technology specific way and in a performance driven way. The syntax of the implemented code should be stated in the design specification document.

5.4 Design quality

The quality of the design consists of all of the former described attributes. A design of good quality can be achieved only with careful planning and with clear rules. The design rules together with the guidelines need to be set in the beginning of the design project. It is good to make a design schedule and allocate the resources, so that enough time can be reserved for each design stage. The implementation tools are needed to select beforehand and the interoperability of the tools tested. After all of the necessary preparations are done appropriately, it is good to keep the implementation personnel informed for every changes and difficulties in the process. Of course the actual implementation process is needed to perform with adequate carefulness and by skilful personnel, but the weight of this fact can be relatively decreased with the former described preparations.

Chapter 6

HDL-design options

In this chapter, the design options for the OAN test network prototype FPGA programs are discussed. Before the actual discussion, we need to have some knowledge about the programmable architectures and their properties. For this reason, the architectures of the FPGAs together with the programming tools used in the implementation stage are presented. The overall functionality of the design must be defined first and the options for the implementation can be identified only after that. These options concentrate on different ways to achieve the desired functionality. By this way, all of the possible implementations can be compared and the most suitable one selected. Furthermore, with the help of this kind of contemplation, possible future development and functionality additions can be considered beforehand and possibly taken into consideration already in the first version of the design. This will help the future developments of the system.

6.1   Target architectures

The purpose in the OAN project is to implement as many of the test network functionalities as possible inside the FPGAs to achieve flexibility and reusability for the implementation. This purpose was clear already in the beginning of the project and, for that reason, the requirements for the FPGAs to be attached in the prototype were a large amount of programmable logic, a sufficient number of input and output pins and adequate operation efficiency. At the time of the selection, the Xilinx manufactured Virtex-II architecture was the most superior in size and efficiency and was selected as the architecture for OAN FPGAs. Xilinx provides the Virtex-II architecture in different chip sizes and the selection was
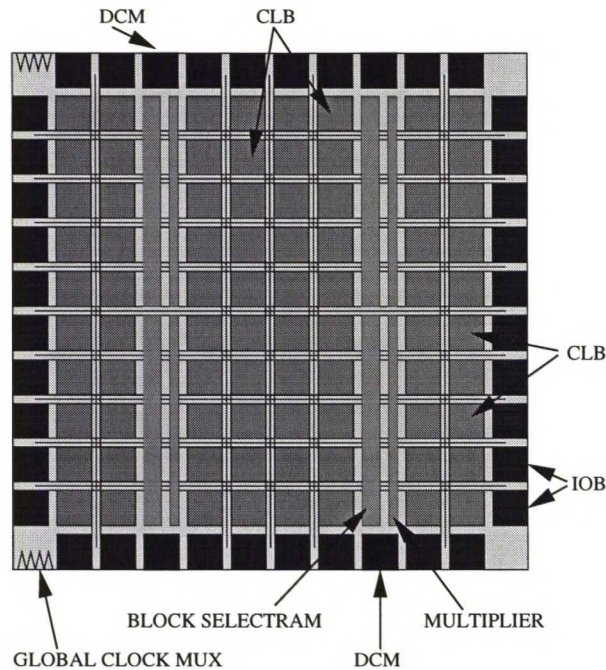
Figure 6.1: Virtex-II FPGA structure, adopted from [Inc00c].

made according to rough estimations about the size of the programs for each of the FPGAs and for the number of required input and output pins. From these prerequisites, the largest chip available at the time, the XC2V6000-FF1152, was selected as the base for router card operations and the XC2V1000-FF896 was considered to be large enough for the interface card operations. After some while, adjustments to the functionality of the router card were made and the TelecomBus serialiser/deserialiser chips were added to provide the access to the TelecomBus. The parallel TelecomBus interfaces has a great number of signals, and the number of required input and output pins for the router card FPGA exceeded all of the available FPGA sizes. For this reason, an extra FPGA was attached in the router card. This FPGA was selected to be the XC2V2000-FF896.

The architecture of Virtex-II, depicted in figure 6.1, has several architecture specific functionalities. These functionalities can be used to improve the efficiency of the design. The most usable functionalities are Digital Clock Managers (DCMs), global clock buffers, programmable Input/Output Blocks (IOBs), and selection of Random Access Memory (RAM) memories and hardware multipliers [Inc00c]. In addition, the Configurable Logic Blocks (CLBs) together with a programmable switch-matrix provide a flexible base for the implementation of programs. With the help of DCMs and global clock buffers, the clocking of the design can be man-

54

Table 6.1: The resources available in the prototype FPGAs, adopted from [Inc00c].

Device	XC2V1000-FF896	XC2V2000-FF896	XC2V6000-FF1152
System Gates	1,000,000	2,000,000	6,000,000
Distributed RAM Kbits	160	336	1,056
Multiplier blocks	40	56	144
Select RAM 18-Kbit Blocks	40	56	144
Select RAM (Kbits)	720	1,008	2,592
DCMs	8	8	12
I/O Pads	432	624	824

aged efficiently. Clock frequencies can be multiplied or divided, clock delays can be adjusted and clock phases modified. All this with minimum distortion. The programmable IOBs provide almost all of the possible I/O-standards for every input and output pin, together with digitally controlled impedance. The two-port Select RAM can be efficiently used for First In First Out memory (FIFO) implementation and some amount of distributed RAM memory can be used for other purposes as well. The hardware multipliers can be used to build superior multiplier structures. Furthermore, depending on the size of the FPGA chip, the resources for the functionalities vary. The amount of resources for selected chips is presented in table 6.1.

6.2 Programming tools

The programming tools presented here are used after the design specification is finished. Although these tools are not needed in the design stage of the implementation, it is good to start thinking at how these tools can be used best in the implementation. This is for the reason that some tools have special features, which can fasten the implementation stage if the design is done in an appropriate way. The tools used in the OAN project are presented in table 6.2. These tools are outlined according to the Xilinx design flow, presented in figure 5.2.

6.3 Design options

The defining of the overall functionality of the OAN prototype FPGAs can be started from the figure 4.2, where the most important devices together with their

55

Table 6.2: Programming tools used in different stages of the OAN design flow.

Design stage	Tool
Version management	Concurrent Versions System (CVS)
Entry	FPGA Advantage and Emacs
Verification	Modelsim 5.6
Simulation	Modelsim 5.6
Synthesis	Leonardo Spectrum
Implementation	Xilinx ISE 5.2
Timing analysis	Xilinx ISE 5.2
Timing simulation	Modelsim 5.6
Download to a device	Xilinx programmer
In-circuit verification	Xilinx Chipscope 4.2

connections in the OAN proto-board were illustrated. In the figure, the purposes of the FPGAs in both of the prototype cards can be seen. Here, the purpose of the interface card FPGA is to provide the access network interface towards access technologies, and the purpose of the router card FPGAs is to provide the interface towards the transport network. One guideline in the OAN project was to use standardised or industry accepted operating principles and methods. The purpose is to follow the same guideline in the HDL-design, and it is taken into account in the option defining stage as well.

The functionalities implemented in the OAN FPGAs can be divided into control and network functions. The network side of the prototype operates as its own aggregate, without the need for direct control. Control operations are used to monitor, adjust and set certain functionalities in the network. In addition, the control side provides the interface for the management software to access the information coming from the operating chips or from the networking functions. Furthermore, the already laid out wiring of the prototype does set some limits for the operations between devices, but this is considered separately in every case. The options for the design functionalities are discussed separately for the control and network operations in the next two sections.

6.3.1 Control functions

The purpose of the control functions is to provide a strict control over the devices in the prototype. The manufacturer specifies the controlling functions for most of the devices and the interface to them must be implemented according to this specification. In addition to the device interfaces, some other control functions are
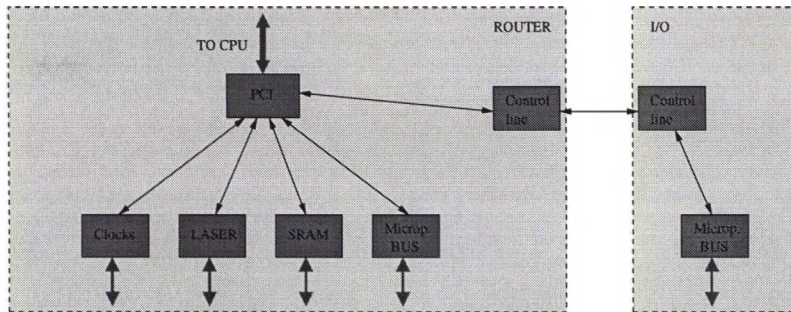
Figure 6.2: The formation of the control functions in the OAN prototype.

needed in the design. Both the router and the interface card have some number of controllable test points and LEDs to be used in the debugging and operating stages. Furthermore, both of the cards might need some sort of a clock controller to create and distribute different types of clocks in the design. From these assumptions, the architecture for the functional control blocks can be derived easily and it is presented in figure 6.2. Here, the microprocessor bus interface is provided for accessing the registers in the PMC-Sierra chips. The laser block is responsible for the controlling of lasers through digital-to-analogue converters and programmable potentiometers. The PCI -block is responsible for the interface towards the PCI-bus, from where the CPU can access the whole system. Furthermore, the SRAM-chips located in the router-card have their own interfaces.

In addition to the control blocks, the control procedure needs to be determined as well. It can be concluded quite easily, because there are no options available for the implementation. First of all, all of the control functions need to be accessible by the CPU, which uses the PCI-bus for the access. The operation in PCI-bus is address-based as well as most of the device interface operations. The register-based access is also the only way the CPU can control these operations. So the only solution is to make all of the functions controllable by simple register "write and read" commands.

However, the controlling interface between different FPGAs can not be done with simple register accesses. This is because the wiring does not allow enough connections between them [1]. For that reason, a specific control-data transport system is needed to develop between the FPGAs. These systems must be capable for two-way transport and must sustain the order of the control-data. In addition, some error detection and maybe correction will be needed in the communication channel implemented between cards. The wiring implemented in one card can be

---

[1]For controlling operations, there are 10 signals between router and interface-cards and 4 signals between the FPGAs in the router-card.
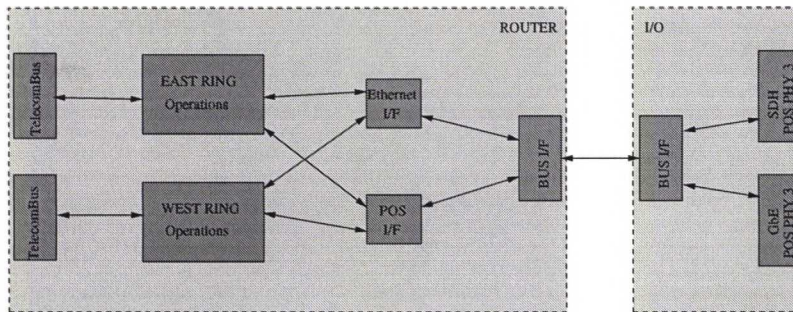
Figure 6.3: The overall functionality of the OAN network.

considered error free.

6.3.2   Network functions

Networking functions are not as straightforward as control functions, but the main functionalities can be identified quite easily and these are presented in figure 6.3. First of all, interfaces with PMC-Sierra device data portions need to be implemented in a special way, presented in the data sheets of the devices. These are the parallel TelecomBus-interfaces in the router card and POS-PHY level 3 interfaces in the interface card. The rest of the network functionality can be divided into few specific aggregates, presented in figure 6.3. In the router card side, the DoS operations for both of the SDH rings are performed separately and Ethernet and POS packet processing are done in different blocks. Furthermore, the router and interface cards need a bus interface to transport the data traffic between them, and the same bus may also be used to transport the control traffic. The options for the implementation of these functionalities are discussed next.

The first functional version of the OAN prototype is implemented with as low number of functionalities as possible, so that it could be get up and running as soon as possible. After the first version is operable, more functionalities can be added later with little adjustments or additions in the code. In the first stage only the Gb Ethernet together with POS interfaces are implemented. The purpose is to transport Gb Ethernet together with POS-data over the SDH rings in the OAN test network. The Gb Ethernet will be first supported with a single HUB, which can be later expanded to a bridge and then to a switch. The POS line-interface is responsible for the transport of POS-traffic between rings and the interface card. In the first stage, only the IP over SDH transport will be supported. Later the support can be expanded to other POS methods and to other SDH traffic as well.

58

The bus-interface between router and interface-cards needs a throughput of 10 Gb per second and for that reason it follows the PMC-Sierra specification POS-PHY Level 4 [Inc01a]. This bus will be later expanded to support multiple cards to be connected in the same bus.

The heart of the network operation is the DoS scheme, which is implemented for both of the rings separately. The DoS requires the implementation of several different technologies, VC, LCAS and GFP, which all have their specific functionalities. Furthermore, after the DoS processing, the data must be mapped into SDH-frames where it is transported over the OAN network. The parallel Telecom-Bus mapping requires the transported data to be mapped inside 16 Synchronous Transport Module 1 (STM-1) frame simultaneously, which is quite complicated. One solution for the ring implementation could be the all at once solution, presented in figure 6.4(a). Here the transmission side (TX) operates in the following way: the transmitted data comes from the Ethernet or POS interfaces and goes first into GFP-framer. The Ethernet and POS data are processed separately and handed further for the VC-processor, which classifies them into Virtual Concatenation Groups (VCGs). In the figure, the TDM-data means the telephone network traffic and it will be implemented in a later stage of the network development. After the data is assorted according to the destination and QoS or LCAS requirements, the creation of STM-1 frames can begin. SDH containers, created in the virtual concatenation stage, are mapped inside the STM-1 frames, which are then further mapped into the TelecomBus. These procedures are presented in more detail in [IT00c][IT00a][Inc01c] and discussed in the next chapter. Furthermore, the APS is responsible for forwarding of traffic towards the operating ring if there is a failure in the other ring.

However, the formation of the configuration memory is needed to consider. We could create all of the 16 STM-1 frames first in the memory and only after that map them into TelecomBus. The STM-1 consist of bytes in 9 rows and 270 columns, requiring a minimum of $16 \times 9 \times 270B = 38880B = 311040b$ of memory for a single SDH transport operation. In addition, another memory space would be needed for the creation of the second 16 STM-1 frames, while the first ones are mapped into TelecomBus. The amount of memory required here exceeds the available fast RAM memories inside the FPGA chips and does not seem so efficient in other ways either. It seems that restoring of the data is needed to do in the virtual concatenation stage, where different sizes of containers could be created for the STM-1 frames. The mapping of STM-1 frames into TelecomBus can then be done simultaneously as the creation of the frames. However, the implementation of the VCG-memories needs to be considered separately.

The all at once principle presented in figure 6.4(a) gives an idea of the operation,

59

a) Ring operations – The all at once –solution

b) Ring operations – The simple solution
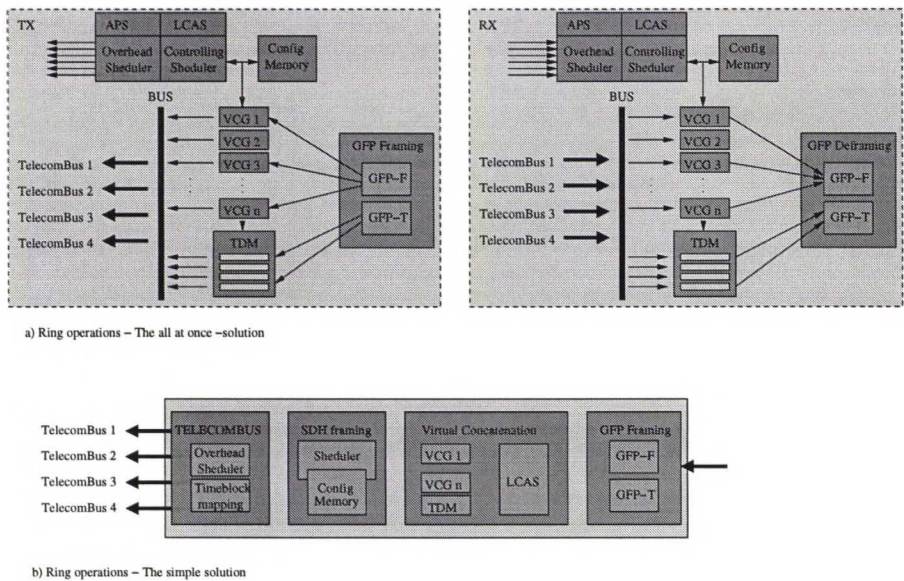
Figure 6.4: The overall functionality of the OAN network ring operations.

but is still quite complicated to implement. Especially when there is no need for the common configuration memory. The more suitable and efficient practice is to divide all of the functionalities into small aggregates, easy to implement and connect. By this way, the error probability in the design can be kept low in the beginning and the STM-1 frames can be created all simultaneously in parallel processes. Also, some amount of memory can be saved for other purposes and more flexibility achieved to the process. This more appropriate implementation with simpler stages is presented in figure 6.4(b). Here, all of the stages are responsible for operations dedicated to certain operations. The operations needed to perform are the same as described before, but now the interfaces between blocks are needed to specify. These blocks are more deeply discussed in the next chapter.

The implementation of the former presented ring operation is quite resource consumpting, especially when it is needed to implement for duplicate rings. As discussed in chapter 4, the prototype node has two FPGAs in the router card and the accomplishment of network operations is needed to divide between these FPGAs. This brings new considerations into the design, especially in the load balancing. Furthermore, specific transport and control interfaces between these FPGAs are needed to implement to support the needed activities. The needed activities depend on how the splitting of functionalities between different FPGAs is done. For this reason, it is better to start with the operation splitting task.

The available resources of the FPGAs determine what can be implemented on

each of the devices. First of all, we can calculate the requirements for the memory used in VCGs in the first stage of the OAN prototype implementation. If there is 16 of them in one direction, it takes together $4 \times 16 = 64$ VCGs in the design. One VCG will use one Select RAM memory primitive at a minimum and therefore the amount of Select RAM memory primitive available[2] in the smaller FPGA in the router card is not enough. So we need to split the ring operations between these two FPGAs. There are only two potential ways to split the ring operations. One is between the GFP and the virtual concatenation blocks, and the other is between SDH framing and TelecomBus mapping blocks. The third potential splitting between SDH framing and virtual concatenation blocks can be considered impossible, because of the number of connections needed between them. Furthermore, the TelecomBus mapping requires access to the SDH framing configuration information, which cannot be efficiently moved with the data. It seems that the splitting is needed to be done after the parallel TelecomBus mapping and the data with the overhead is needed to transport to the smaller FPGA for direct connection into the physical TelecomBus interface.

In this situation, the only way to avoid the need for transport protocol would be connecting the TelecomBus signals directly from the physical TelecomBus interface in the smaller FPGA to the larger FPGA. However, this is not possible because the two parallel TelecomBus interfaces requires together 248 signals and only 184 connections are implemented between the FPGAs in the router card. So a specific transport system is needed to develop between the FPGAs. The implementation of this transport protocol or system is more deeply discussed in the next chapter.

The physical network structure in the OAN prototype takes care of the network protection, as discussed in chapter 4. For this reason, the implementation of APS in the HDL design is not necessary, but it will be included in the design for future purposes. This is because the OAN is a metropolitan area test network and at the moment it seems that the protection and survivability features in this area will be even more important in the future than they have been before. Because of the small utilisation of the smaller FPGA, it would be nice to have at least the APS implemented there. However, APS requires information available in the SDH frames and it is needed to locate next to the SDH framing and deframing procedures.

---

[2]XC2V2000-FF896 has 56 Select RAM primitives as presented in table 6.1.

Chapter 7

HDL Design

Based on the discussions in the previous chapter, the design for the HDL implementation of the OAN prototype FPGAs is presented in this chapter. The presentation follows the structure of the design specification model, presented in chapter 5. Only the detailed technical definitions of the functionalities are left out to keep the number of the pages of this thesis in decent limits. The details presented here cover the main functionality of the design and interfaces between different blocks. Most of the functionalities are based on the results of the previous development in the industry and more accurate information can be found from the source literature. The reason why there is so much source information available is the original OAN suggestion that as much of the functionalities as possible should be based on standards. This is the truth only for part of the functionalities, but nearly all of the rest are based on industry recommendations or specifications. Furthermore, part of the design is a result of own development and these functionalities are presented with adequate details. This issue is further discussed in the following section.

7.1   Design functionality

The options for the implementation were discussed in the previous chapter and based on these assumptions, the overall design architecture is presented in figure 7.1. The network and control operations are separated from each other, because controlling of the network operations happens only with non-direct settings. The network side has two SDH-interfaces, west and east rings. Their operations are identical to each other, and the APS block is connected to both of them. The ring

operations are responsible for the building of the SDH payload and frame. The POS and GbE packet scheduler blocks direct the network packets into right directions, which are either towards one of the rings or towards the interface card. The POS-PHY level 4 interface is responsible for the transportation of data packets between router and interface cards and the POS-PHY level 3 interface is used for data packet arbitration between PMC-Sierra devices in the interface card. The FIFO controller handles the buffering of packets between POS-PHY interfaces. The I/O control is responsible for the controlling operations in the interface card. Otherwise the control side of the implementation is the same as presented in the previous chapter.

From the design blocks presented in figure 7.1, the functionality of TelecomBus, POS-PHY Level 3, POS-PHY Level 4, SRAM, PCI and microprocessor bus interfaces is provided directly by a set of industry specifications or device datasheets, to be presented later. The only thing left for designing, is the functionality and composition of the interface towards the other operations inside the FPGAs. Furthermore, all of the networking functionalities[1] are based on standards. The designing task here is to clarify how these standards can be supported by hardware solutions, because the standards specify only the needed operations, not the implementation. The rest of the design blocks need to be created purely by the designer. Here, one important part of the planning is defining the interfaces and operations between different blocks. In figures 7.2 and 7.3 the signals between different blocks in the FPGAs are presented together with more detailed design structures.

The larger FPGA in the router card is illustrated in figure 7.2, the smaller FPGA in the router card in figure 7.3(a) and the interface card FPGA in figure 7.3(b). These figures give some understanding on the operating principles of each of the interfaces. However, a more accurate description will be given later in the thesis, together with a detailed presentation of the functionalities of the design blocks. Furthermore, the interfaces between FPGAs are also discussed later.

7.2 Distribution of clocks

One important part of the network design is the clocking scheme. The SDH technology has specific requirements for the source clocks and clock synchronisation, which both need to be considered. The OAN prototype has a variety of different clock sources, illustrated in figure 7.4. First of all, the two oscillators loc-

---

[1]SDH, VC, LCAS, GFP, GbE and POS.

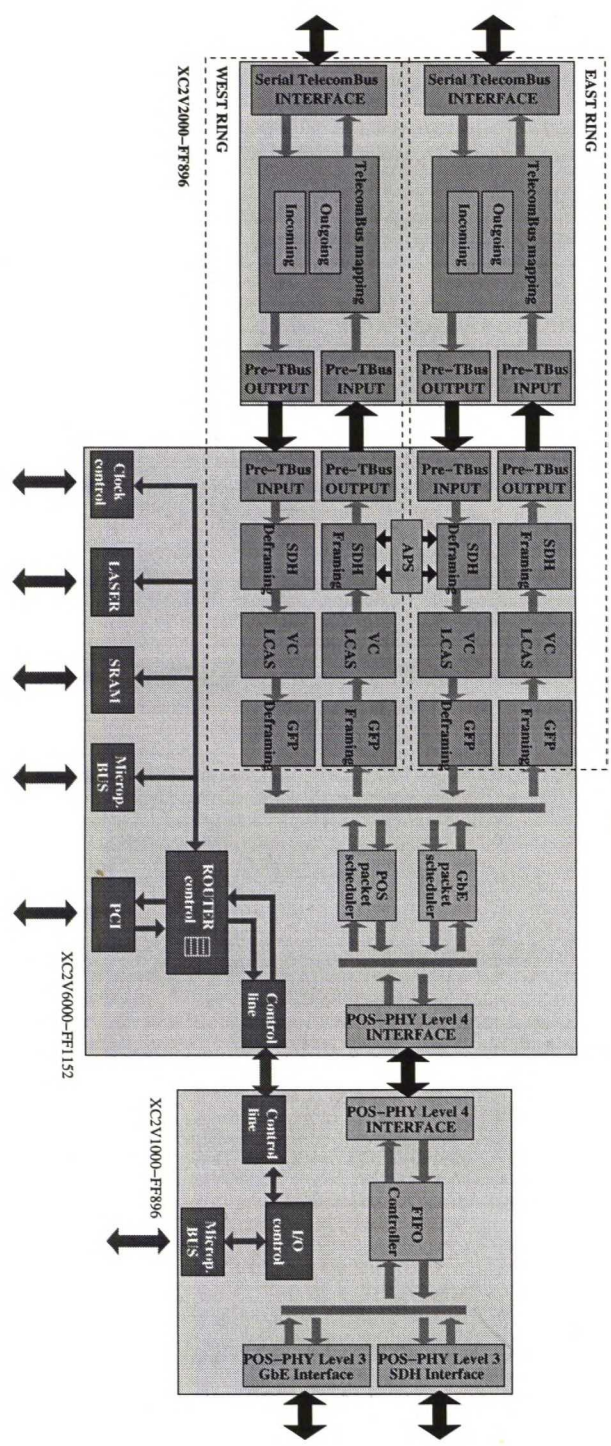Figure 7.1: The functionality of the FPGAs in the OAN prototype.

Figure 7.2: The block design for the larger FPGA in the OAN prototype.
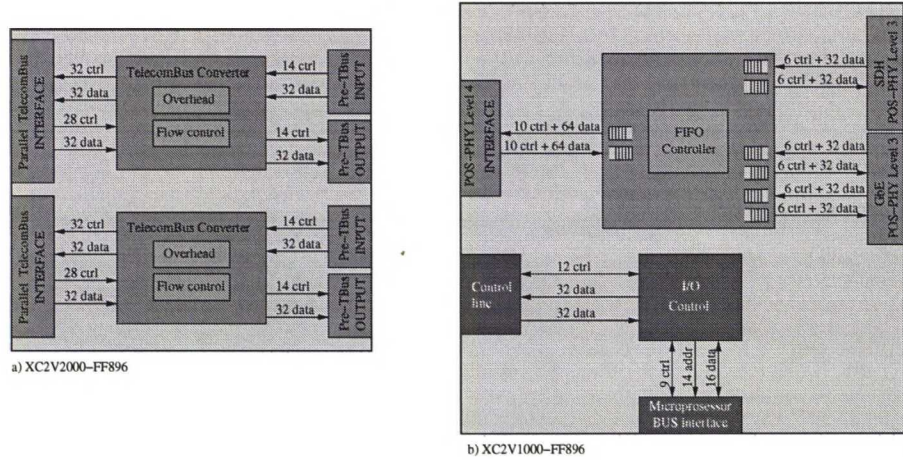
Figure 7.3: The block designs for the smaller FPGA in the router card (a) and for the FPGA in the interface-card (b).

65

Figure 7.4: The sources of clocks in the OAN prototype.

ated in the router card are the main ones. Secondly, all of the SDH-framer chips provide four different clocks, which are two selectable 8kHz/19.44MHz and two 77.76MHz clocks [Inc02a]. The SDH-framer clocks are synchronised according to the receiving or to the transmitting interface of the chip. The ability to change the synchronisation of the SDH-chips is important and different synchronisation can be achieved with the help of chip-specific PLLs. These PLLs are implemented in the router card and they have an accurate reference oscillator, from where the 77.76MHz and 155MHz clock-signals can be generated. The PLL synchronises its outputs according to the 77.76MHz input, coming from the larger FPGA. By changing the synchronisation of these PLL inputs, the synchronisation of the design clocks can be changed. The interface card needs to have some reference clock from the router card, although it has the four clocks from its SDH-framer. Furthermore, an external clock source can be attached to the front panel SMA-adapter.

Now the clocking scheme of the OAN prototype is clear and it is time to consider the clocking scheme for the FPGAs. According to series of interface specifications and other information it was possible to identify the different clock domains needed inside the design. These domains are illustrated in figure 7.5. The clock controller-block is responsible for the distribution and creation of all

66

the clocks in the design. The selection options for each of the clock frequencies are further discussed in the specification part of the clock controller or the other blocks respectively. All of the different clock domains are separated with special FIFO architecture, which have two ports, both operating with different frequencies. Without this kind of clock separating, different clock domains would be hard to implement in the design.

7.3 Control part

As it was stated earlier, the control part is responsible for the adjustment, setting and monitoring functions of the network part. Together with these, it has control interfaces towards all of the devices in the prototype, and it controls the LEDs and test points in the design. Of course, one important feature in the control part is the modification and distribution of the clocks in the design. Furthermore, the CPU needs to have access to read and write registers in all of the controllable devices. In addition, some amount of controlling ability is needed for the functions inside the FPGAs as well. For the controlling operations, every device has a certain number of registers, which can be read or written. In addition, the design control procedures require some number of registers to be created into the design. These registers are located in the router control block, and they are named as the Status/Control-registers and further discussed in the following.

7.3.1 Registers

All of the devices in the prototype can be controlled through a simple register "read and write" commands. For this purpose, all of the devices have a certain number of registers need to be accessed by the CPU. The address spaces for each of the devices is presented in table 7.1. The registers in the devices are only 16-bit wide and the 32-bit wide PCI-bus cannot access all of them. For that reason, simple address conversion is needed between the PCI-bus and the registers in the prototype. The mapping of each of the devices PCI-addresses is presented in table 7.2. In addition to the devices in the router card, the interface card has its own devices. However, these devices cannot be accessed in the same way as the devices in the router card and are left out from the PCI-addressing. The accessing of these devices is discussed in the next section.

The control functionalities need to be implemented inside the FPGAs are mapped into register read and write procedures in the Status/Control register. With re-
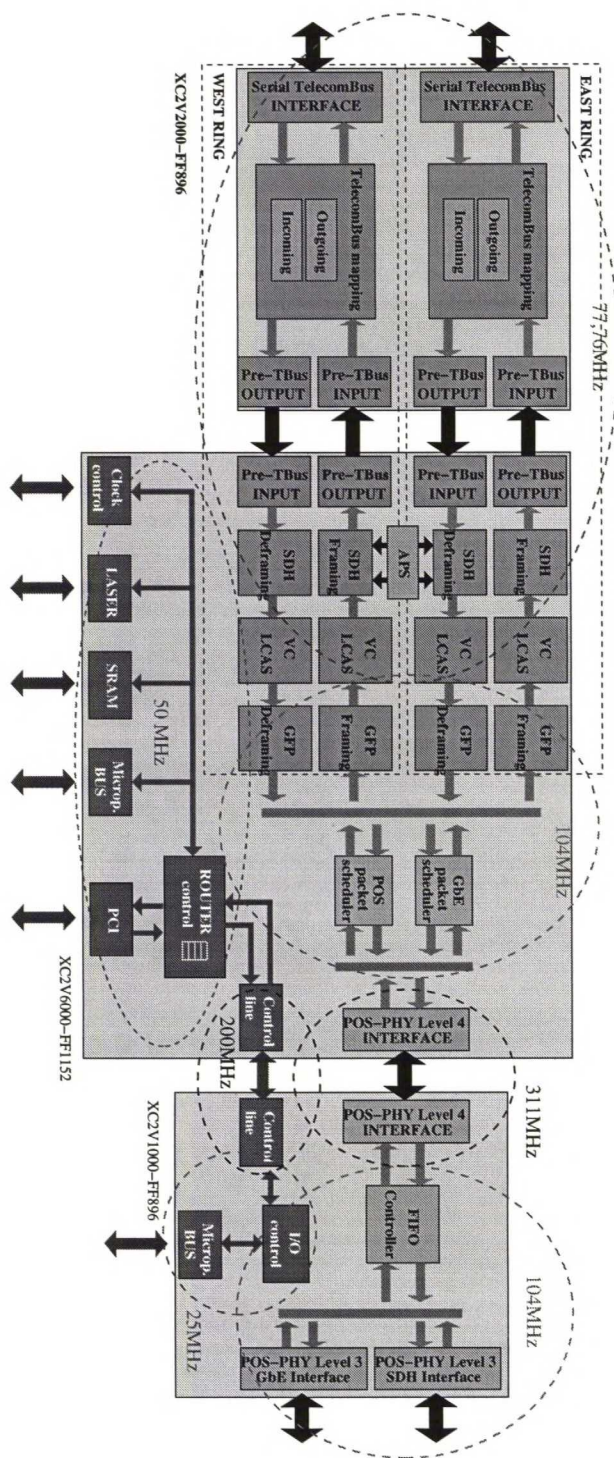
67

Figure 7.5: The clock domains in the OAN HDL design.

Table 7.1: The device address spaces in the OAN prototype.

Address space	Width	Chip
720H	11	PM3386 (Gbit Ethernet)
502H	12	PM5310 (TelecomBus serializer/deserializer)
890H	14	PM5381 (SONET/SDH framer/deframer)

Table 7.2: The address mappings in the Router control block.

Node address	PCI Address	Type	Board	Circuit/block
00000 - 00FFF	00000 - 01FFF	R/W	Node	Status/Control register
01000 - 01FFF	02000 - 03FFF	R/W	Node	S/UNI-2488 ring A (PM5381)
02000 - 02FFF	04000 - 05FFF	R/W	Node	S/UNI-2488 ring B (PM5381)
03000 - 03FFF	06000 - 07FFF	R/W	Node	PM5310 A
04000 - 04FFF	08000 - 09FFF	R/W	Node	PM5310 B

gister structure, the needed functionalities can be arranged and a specific address provided with each of them. The Status/Control register in the OAN prototype is used to give commands to different instances in the design. It can also be used for monitoring purposes, for example error monitoring or network statistics. Furthermore, in this case the access to the interface card is implemented through Status/Control-register. The address spaces in the Status/Control register is presented in table 7.3 and in each space, sufficient number of registers is defined for the potentially needed functionalities. All of the registers are 16-bits wide and they can be accessed with 32-bit address.

7.3.2 Accessing the interface card registers

The registers located in the interface card cannot be accessed similarly as the registers in the router card. The reason for this is the slow control connection between router and interface cards. The connection has a small number of signals, and the data must be transported in serial form. With the clock frequencies available for the purpose, the connection cannot be fast enough for the PCI-access. For that reason, another way or system is needed for the communication between the interface card and the CPU. This implementation block, named control line, is presented in detail later on in this chapter, but the procedure needed to access the registers in the interface card is illustrated here. The registers in the interface card are also 16-bit wide and to address all of them, a 15-bit wide address is needed.

Table 7.3: The address spaces of the Status/Control register.

Address	Description
0000	Identity (revision)
0001	Master reset
0002 - 000F	Reserved
0010 - 001F	Control line and I/O operation
0020 - 004F	Laser controller
0050 - 006F	Clock controller
0070 - 009F	VC operation
0100 - 012F	LCAS operation
0130 - 015F	GFP operation
0160 - 018F	APS operation
0190 - 021F	SDH framing and deframing operations
0220 - 024F	Interrupts and error detection
0250 - 04FF	Reserved
0500 - 07FF	Network statistics

The data and the address together with the register access command are transported from the router card to the interface card. The result of the read operation is then transported over the control line back to the router card.

The access operations of interface card registers uses two 32-bit wide registers for the read and write operations. These registers are located in the status/control register, where the address 0010 is reserved for the write and 0012 for the read -operations. The 32-bit wide registers are selected, because the data width of the PCI-interface is 32 bits. The operations towards interface-card require special handling from the management software. This means that the interface-card data, address and command need to be transported in the data part of the PCI-command. The execution is performed in a way that the "read and write" command, data and address are all written to the Status/Control interface card write register, from where the command is transmitted to the control line FIFO and further to the interface card. If the command was a read-command, the answer can be read from the Status/Control interface card read register after some specific amount of time. This register needs to be polled from time to time to check if some data has come from the interface card.

7.3.3 Clock controller

The clock controller block is responsible for the management of the clocks in the HDL design, because clocks of different frequency are needed in different parts

Table 7.4: Clock inputs and outputs in the clock controller block.

INPUTS	
Signal	**Frequency**
Front panel SMA	External
Oscillator	125 MHz
PM5381A PGMRCLK	8 kHZ / 19,44 MHz
PM5381A PGMTCLK	8 kHZ / 19,44MHz
PM5381A TCLK	77,76 MHz
PM5381A RCLK	77,76 MHz
PM5381B PGMRCLK	8 kHZ / 19,44 MHz
PM5381B PGMTCLK	8 kHZ / 19,44 MHz
PM5381B TCLK	77,76 MHz
PM5381B RCLK	77,76 MHz
OUTPUTS	
Signal	**Frequency**
POS PHY-3	104 MHz
POS PHY-4	311 MHz
PCI interface	50 MHz
Control line	200 MHz
SRAM interface	133 MHz
West ring synchronisation	77,76 MHz
East ring synchronisation	77,76 MHz

of the design. The clocks needed in the router card FPGAs are created using the Digital Clock Managers (DCMs), provided by the Virtex-II architecture. All of the clocks in the design are at equal phase and only frequency multiplying or dividing is needed for the creation of the desired clocks. Furthermore, this block is also responsible for the selection of the SDH ring synchronisation. The clock controller input and output clocks and their frequencies are presented in table 7.4.

7.3.4 PCI interface

The PCI-operation is a simple read or write access to register in a certain address. However, the configuration of the PCI-bus according to the PCI-standard is not so trivial. Before the PCI-bus is operational, the PCI-controller needs to ask, determine and give the addresses for all of the devices connected in the bus. This address is then used to access the devices in the bus. Furthermore, the physical accession to PCI-bus is not simple, and a PCI-interface chip was selected to convert the PCI-bus into its local bus, which is much simpler to access. In addition, the selected chip handles the PCI configuration process by itself. The PCI-bus used

in OAN has 32-bit wide address and 32-bit wide data. Most of the registers in the OAN prototype have 16-bit wide data and the less significant part of the PCI-data bus is used for them. In PCI-operation, the command is first written to the device, specified by the address, and the bus is halted as long as the ready-indication is received from the device. The PCI write-operation is thus quick, but the duration of the read operation depends on the target device. This is the reason, why the interface card register access was implemented in a special way.

The PCI-interface is implemented with the help of PCI9030-chip, which converts the PCI-bus into its local bus [Tec00]. The local bus is configurable and allows the use of clock frequency between 33-66 MHz and most importantly, multiplexing of address and data over the same bus. With multiplexing some of the input output pins in the FPGA can be saved for other use. The selected chip is widely used in the industry and it should function properly. Furthermore, the PCI standard has strict limits for the physical connection lengths between the PCI adapter and the PCI chip. For that reason, connecting the PCI bus directly to the prototype FPGA would have been too complicated and it was left out from the design.

The purpose of the PCI-interface block is to provide the interface to the PCI9030 local bus. The interface has two operations, read and write. The address and data for the read and write operations are multiplexed from the local bus and need to be changed into parallel form for the operations in the FPGA. The interface to the local bus is described with detail in [Tec00]. Furthermore, the interface to the router control has separated address and separated read and write data lines. It has a signal that indicates the start of operation and a signal that is asserted when the operation is ready. The operating clock for the local bus and for the interface is selected to be 50 MHz.

7.3.5 Router control

The router control block is the core of the control operations, and every command is transported through it. Its main operation is the address mapping between devices and control functions. Several devices can be attached to this microprocessor bus, but only one device can be accessed at a certain time. The accessed device is indicated with a chip-select signal and one purpose of the router control is to change the PCI-addresses into these chip-select signal assertions. Furthermore, the router control is responsible for converting the Status/Control register read and write operations into control functions in the design. The address mapping for each of the devices were presented in table 7.2 and the structure of the Status/Control register in table 7.3.

The router control block interfaces with all of the other control blocks in the router card. These interfaces were presented in figure 7.2 and more deeply covered in the specification of the respective blocks. Controlling of eight LEDs and several test points are one of the responsibilities of the router control. Furthermore, after the first version of the OAN network is operational, the router control block will be the block where automatic error detection systems and interrupt handling operations are to be implemented.

7.3.6 I/O control

Like the router control in the router card, the I/O control is an interface for the control operations in the interface card. The interface card has less controlling operations than the router card, and all needed ones are implemented in the I/O control block. In the first stage, there is no need to build a separate register structure in the interface card, because only the access to the device registers is needed. Furthermore, the clock control is implemented according to the specifications planned beforehand, and there is no need for the ability to change synchronisation. The chip-selects signals need to be controlled by the I/O control, like the eight LEDs and test points in the interface card. In the later versions of the design, the interrupt handling and some automatic monitoring can be implemented in the I/O control.

7.3.7 Control line

The control line is a simple one-bit parallel line interface with Cyclic Redundancy Check (CRC) error checking. It has a two-way transport for 36-bit wide data over three signals per transport direction. In addition to data transport, the block calculates a 4-bit wide CRC-checksum for the transported data in the transfer side and verifies it in the receiver side. If the checksum does not match, the transported data is ignored. The calculated CRC-checksum is polynomial and of form $X^4 + X + 1$. It will be calculated using the hardware implementation illustrated in figure 7.6.

The data to be transported is given to control line through a simple FIFO-interface. The 36-bit wide FIFO is located in the control line block and the 36-bit wide data sequences are transported in the order of their arrival. The FIFO interface consists of 36-bit data and full and write enable signals. The receive data interface is similar and consist of 36-bit data, empty and read enable signals. The control line blocks have FIFO interfaces with both router control and I/O control blocks.
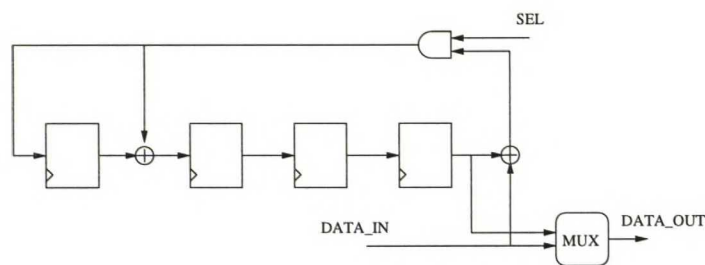
Figure 7.6: The HW implementation of a bitwise CRC operation.
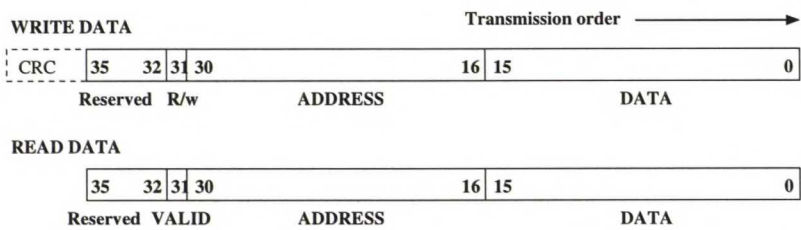
Figure 7.7: The composition of the data transported over control line.

Furthermore, the composition of the transmitted data in control line is presented in figure 7.7.

7.3.8 Microprocessor interface

The 16-bit microprocessor interface needed to be implemented here is commonly used in PMC-Sierra's chips. It uses a two-way 16-bit data interface, with device specific address, interrupt and chip-select signals, read and write command indication signals and address latch enable signal. The timing specifications for the interfacing signals are described in the device datasheets [Inc01b], [Inc01c] and [Inc02a] respectively. The router and interface cards both have their own microprocessor bus interfaces. These interfaces are otherwise identical, but the router card has more devices attached to it. The same implementation of the microprocessor interface can be used in both cards, because the router and the I/O control blocks are responsible for asserting the chip-select signals. The timing of the interface allows the use of a clock frequency of 25 MHz at maximum.

The router card microprocessor bus interface signals presented in figure 7.2 consist of reset, interrupt and chip-select signals to the devices in the router card and read or write command indication, data and address busses to the microprocessor bus. The signals in the interface card microprocessor bus interface, presented in

figure 7.3(b) are the same as in the router card, although the interface card has less devices attached than the router card and so less signals are needed in that interface.

7.3.9 SRAM interface

The router card has six $512k \times 36$ SRAM chips, which all have 2 MB of memory, providing together 12 MB of memory to be used in the operations in the router card. This memory is attached in the router card for the routing calculation purposes and is therefore not used in the first stage of the design implementation. However, the connections to the memory chips need to be tested and access to the memory is needed for that reason. The SRAM interface block provides access to the memory space. The six memory chips are connected with the larger FPGA, forming two larger memory blocks. One block is 144 bits wide and the other block is 36 bits wide, and they both have 19-bit address buses. The memories support single and burst read and write operations. The interface timing specification of the memory chips are presented in their datasheet [Ele01]. The connections between the router control and the SRAM interface block consist of separate data and address busses for each of the memory blocks together with three control signals for each of them. These control signals indicate the operation (read or write), the start of operation and the operation ready indication. The SRAM blocks operate at most at a frequency of 133 MHz, which is selected for their operating purposes.

7.3.10 Laser controller

The router card has two optical tranceivers[2], which can transmit with a wavelength of 1550 nm and receive wavelengths between 1300-1550 nm. The receivers are used in the SDH transport network, but the transmitters are used only for test purposes. In addition to the transceivers, the router card has two tuneable transmitters, controllable through the Status/Control register. These tuneable transmitters are used in the OAN transport network and can be disabled if needed. The laser controller block is responsible for the controlling of the tuneable laser modulation and bias currents together with their temperatures (wavelength). It is also responsible for the temperature monitoring of all of the lasers included in OAN. It has optional eight temperature monitoring interfaces for pump lasers used in optical amplifiers. These interfaces can be used for monitoring the network amplifiers.

---

[2]Transceiver is a device, which has both the transmitter and receiver implemented in it.

The laser settings on the card are analogue in their nature and for that reason analogue to digital converters are used when monitoring values from the lasers. In addition, digital potentiometers and digital to analogue converters are used when controlling the lasers. Here, following equipment are used: 12-bit ADC MAX1247 [Pro01], 12-bit DAC MAX531, [Pro97], single digitally controlled potentiometer (X9110) [Inc00a] and dual digitally controlled potentiometer (X9221) [Inc00b]. The monitoring and controlling operations are accessed through the Status/Control-register.

Control operations

These controlling tasks can be done for both tuneable lasers separately. Both modulation and pre-bias currents can be controlled manually or automatically. Asserting the right jumper in the router card will make the selection. In addition, both of the automatic and manual controllers can be accessed through the Status/Control register. Furthermore, all of the equipment mentioned here have a specific operation sequence, which can be found from each of their datasheets respectively. The values needed in these operations are preserved in the Status/Control register. The following list presents the laser controlling operations.

- **Set tuneable laser temperature (wavelength)** — Both tuneable lasers have their own controllers, which use the MAX531 digital to analogue converter. This converter has a specific operation sequence, which can be found from the MAX531 datasheet [Pro97].

- **Set tuneable laser pre-bias current** — Manual pre-bias current control is done with the help of a single digitally controlled potentiometer (X9110) [Inc00a] and automatic pre-bias current controlling with the help of dual digitally controlled potentiometer (X9221) [Inc00b].

- **Set tuneable laser modulation current** — Manual modulation current control is done with the help of a single digitally controlled potentiometer (X9110) [Inc00a] and automatic modulation current controlling with the help of dual digitally controlled potentiometer (X9221) [Inc00b].

Monitor operations

Laser monitoring operations use the Status/Control register as their control interface as well. The value of a monitored function can be checked by first asserting

the command into the register and after some while reading the result from other register. Nevertheless, a more desired option is to monitor the values continuously. The continuous monitoring asserts a new command for the analogue to digital converters over and over again and updates the result register after each operation. By this way, the most recent information is always available in the Status/Control register. This allows the implementation of an automatic monitoring system, where the monitored values are compared to some threshold value. If the threshold value is exceeded, an error condition exists. Automatic monitoring systems are implemented in the later stage of the design and not considered here. The following list presents the laser monitoring operations.

- **Monitor laser temperature** — Temperature monitoring can be done for all of the four lasers with a single four-channel MAX1247, which is implemented in the router card for that purpose. This converter has a specific operation sequence, which can be found from the MAX1247 datasheet [Pro01].

- **Monitor transceiver bias** — The bias currents of the transceivers can be monitored with a single signal, which indicates the end of life or laser OK conditions.

- **Monitor pump laser temperature** — The router card has an interface implemented, which allows the monitoring of 8 separate pump lasers temperature. Two MAX1247 is used for the interfacing purpose.

7.4 Network part

The network part of the design is responsible for all of the networking functions implemented in the design. This covers both the transport network functions and the access network functions. The transport network interface and functionality is implemented in the router card and the access network interface and functionality in the interface card. To transfer data between these interfaces, a special data transporting functionality needs to be implemented. The purpose of the transport network side is to implement the DoS functionality, and the purpose of the interface side is to make the access technology conversions.

7.4.1 POS-PHY level 3

The POS-PHY level 3 is an interface for the interconnection of Physical Layer (PHY) devices to Link Layer devices, recommended by PMC-Sierra. It provides

77
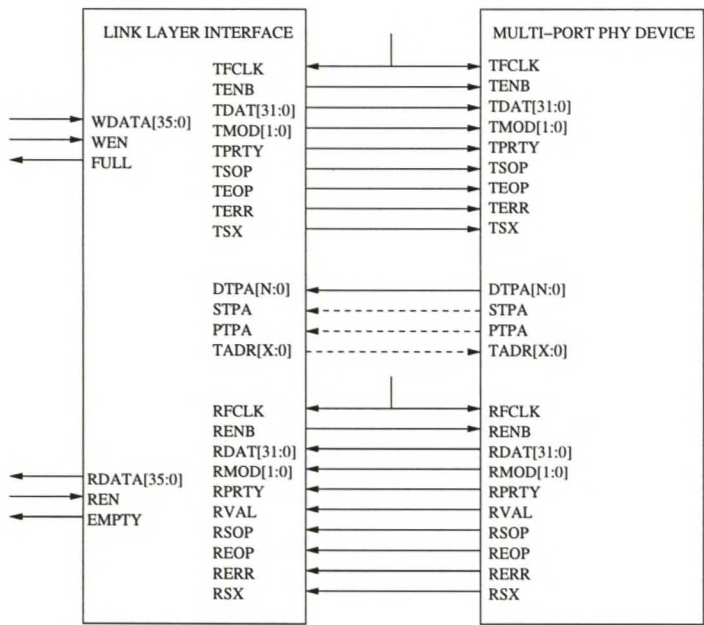
Figure 7.8: The signals in POS-PHY level 3 interface, adopted and modified from [Inc00].

a versatile bus interface for exchanging packets within a communication system. The interface implements the Packet Over SDH (POS), which provides adequate functionality for packet exchanging. The POS-PHY level 3 covers the application rates up to and including 2,4 Gbps. It defines the requirements for interoperable single and multi-PHY applications supporting variable packet sizes and flow control [Inc00]. Furthermore, there is no existing equivalent standard for POS-PHY interfaces.

The PMC-Sierra chips used in the interface card have the POS-PHY level 3 as their data interfaces towards the FPGA. The POS-PHY level 3 specification allows the use of multiple FIFOs in the PHY-device. The SDH chip has one FIFO and the Gb Ethernet chip two FIFOs. This is not a big difference, but it has some effect in the implementation of these interfaces. Furthermore, the SDH chip has a separate interface for transmitting and receiving the Transport Overhead (TOH) bytes of the SDH frame. The interface is presented in [Inc02a], and it needs to be implemented next to the POS-PHY level 3 data interface. The POS-PHY level 3 interfaces have 32 bits wide data bus and a variety of different control signals, presented in figure 7.8 and discussed with more detail in [Inc00].

The Gb Ethernet POS-PHY level 3 interface needs all of the signals presented

78

Table 7.5: The control sequences for packet transportation inside the OAN design.

Control	Description
0010	Start of transfer
0100	Start of packet
1000	End of packet

in figure 7.8 with the N value of 1 and X value of 1. On the other side of the link layer interface it needs double the number of interface signals specified in the figure. This is because the Gb Ethernet chip has two different Gb Ethernet ports and both of them needs to be accessed separately. On the other hand, the SDH POS-PHY level 3 interface does not require the signals named STPA, PTPA and TADR at all and it has only one DTPA signal. Furthermore, its link layer interface is similar to the figure. This is because all of the data from the SDH are coming over single port in the POS-PHY level 3.

The reason why all of these ports have a 36-bit wide data interface comes from the fact that the Virtex-II Select RAM primitives are provided with an extra storage space for the parity of each of the bytes saved. This means that in the case of 32-bit wide data, there is an extra space of 4 bits in the FIFO to be used for the parity preservation or something else. In the OAN design, this extra space is used for the preservation of information about the beginning and end of the packet boundaries in the data flow and for addressing the packets between Gb Ethernet and SDH chips. The control sequences starting from the most significant bit are presented in table 7.5. When the start of transfer indication is asserted, the design address of the following packet can be read from the eight less significant bits in the data bus.

7.4.2 FIFO controller

The FIFO controller block, located in the interface card is responsible for the mapping of the three 32-bit wide POS-PHY level 3 ports into one 64-bit wide POS-PHY level 4 transport FIFO. The boundaries of the data packets need to be preserved in the process and for that purpose, several control lines are provided in the interfaces. The SDH POS-PHY level 3 interface will transport traffic at a maximum of 2,4 Gbps and the Gb Ethernet POS-PHY level 3 interface at a maximum of 2,0 Gbps. Because of these speeds, the most significant 32 bits of the POS-PHY level 4 interface FIFO are reserved for the SDH data and the less significant 32 bits for the Gb Ethernet data. This means that the two Gb Ethernet
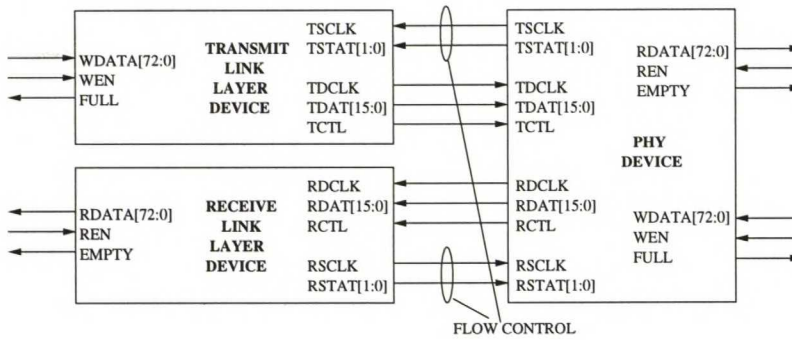
Figure 7.9: The signals in POS-PHY level 4 interface, adopted and modified from [Inc01a].

ports need to be merged into one port. This is done on a packet by packet basis, meaning that whenever a full packet is received in one of the Gb Ethernet ports, it will be forwarded to the POS-PHY level 4. The both Gb Ethernet ports should be given the same transport throughput and they should be read in alternating order.

7.4.3 POS-PHY Level 4

As well as the POS-PHY level 3 interface, the POS-PHY level 4 is an interface for the packet and cell transfer between a PHY device and a link layer device. However, the level 4 interface is specified for the speed of 10 Gbps per direction. This specification uses 16-bit Low Voltage Differential Signalling (LVDS) bus for the transfer of data between link layer and PHY devices, requiring a minimum of 311MHz-clock frequency with double-edge clocking and a minimum of 622MHz-clock frequency with normal single edge clocking [Inc01a]. The clock frequency required in the OAN implementation is not as high, because the required throughput is only half of the specified. The high frequency clocks are always hard to build and for that reason, the frequency used in the OAN POS-PHY level 4 implementation is 250 MHz with double-edge clocking. The 250 MHz clock can easily be multiplied from the 125 MHz reference clock. In addition, the interface has separate flow controls for both the receive and transmit interfaces [Inc01a]. The signals in the POS-PHY level 4 interface are presented in figure 7.9.

The interfaces with the other devices are implemented as 72-bits wide slave FIFO interfaces. The POS-PHY level 4 does not have a separate transport control interface, and information about the packet boundaries together with error monitoring bits are transmitted as separate payload control messages. The presence of a control word in the data-bus (TDAT, RDAT) is indicated with a specific control data
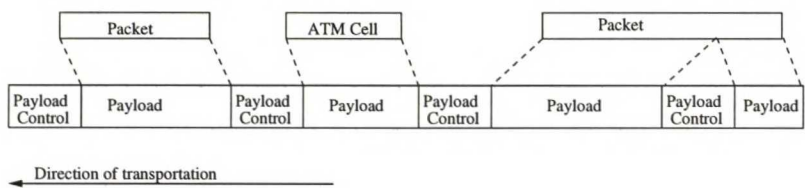
Figure 7.10: The transmission protocol in POS-PHY level 4 interface, adopted from [Inc01a].

indicator (TCTL, RCTL). The flow control is implemented in a way that FIFO status information (TSTAT, RSTAT) is provided from the receiving side of the interface. Furthermore, the transporting of different payloads over the interface is illustrated in figure 7.10. Here, the transmission starts with a payload control word. Several different control words are specified for transmission purposes and they are described more detail in [Inc01a]. The POS-PHY level 4 uses 4-bit Diagonal Interleaved Parity (DIP) coding for error detection in the data transmission and 2-bit DIP coding in the flow control. The DIP provides better error detection capabilities than single parity detection system.

7.4.4 Gb Ethernet (GbE) packet scheduler

At the first stage of the design implementation, the GbE packet scheduler is implemented as a single Ethernet hub. The hub forwards all of the received packets to all of its other ports. By this way the functionality of the system may be checked quickly, although the hub creates a great amount of extra traffic in the network. To avoid the extra traffic, the next stage of the GbE packet scheduler is a bridge, which forwards the traffic from each of the GbE ports located in the interface card, to a specified ring in the router card to be transported further. By this way the GbE over SDH may be implemented. The final stage of this block might be the Ethernet switch, which makes the selection for the transport direction according to the packet address. Furthermore, the interfaces in this block are 32-bit slave FIFO interfaces with the packet control indication signals.

7.4.5 POS packet scheduler

The POS packet scheduler will be responsible for all of the traffic transported over the interface card SDH-line. At the first stage of the implementation, the traffic consists of point-to-point traffic. This means that the IP packets are transported

81

with the help of Point-to-Point Protocol (PPP). The directing of packets requires the implementation of the PPP, which is left for a later time. At the test phase of the OAN network, the packets coming from different directions are forwarded to all of the other directions. This increases the traffic similarly as the hub implemented in GbE scheduler block, but provides an easy implementation to test the functionality in the other parts of the network. After the PPP support, ATM and Ethernet over SDH can be implemented as well. Furthermore, later expansions of this block concentrate on transporting all of the traffic supported by the SDH. The most important one is the telephone traffic.

7.4.6   GFP framing and deframing

In the GFP framing procedure, the transported data packet is encapsulated into the GFP frame. The structure of the GFP frame is presented in figure 7.11 and more deeply discussed in GFP standard [IT01b]. In the first version of the OAN design, the GFP blocks need to provide the support for mapping Ethernet and PPP packets into GFP frames. This requires the implementation of the GFP-F and the GFP-T is left to be implemented later. The GFP framing block is responsible for the packet insertion into the GFP frame and the deframing block is responsible for the extraction of the packet from the frame. In the framing process, the core Header Error Checksum (HEC) needs to be calculated for the core header and the payload area is needs to be scrambled with a $G(X) = X^{43} + 1$ polynomial scrambler. The core HEC is then checked and the payload scrambling removed in the GFP deframing process.

The GFP framing block receives the data from the packet schedulers one packet at a time. The framed packet is transported to a specific VCG in the virtual concatenation block, defined in the Status/Control register. This means that default settings are needed for all of the traffic types in the network, so that the GFP framer can transport the data into right VCGs. In the first stage of the OAN network, these traffic types are Gb Ethernet and POS. The interface towards virtual concatenation block consists of two FIFO interfaces and control signals required for them. The deframing block has similar interfaces as the framing block. Only the data are transported to opposite direction. The deframing block selects the deframed data from the incoming VCGs according to the status information provided by the control signals.
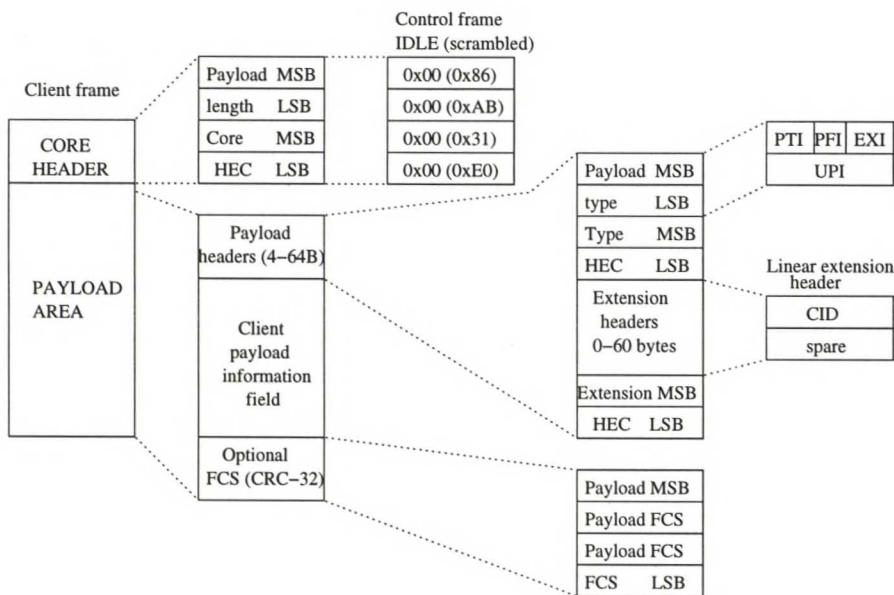
82

Figure 7.11: The structure of the GFP frame.

7.4.7 VC and LCAS

The virtual concatenation is responsible for the mapping of transported data into SDH containers. After the data are mapped into containers, they are equipped with a Path Overhead (POH) and forwarded to the SDH framer to be inserted into a SDH frame. There are several sizes of containers available for SDH and there exist several ways to map these containers into the SDH frame. More information about the containers and multiplexing procedures in SDH can be found from [IT00c] and [IT00a]. In this implementation, only the GFP and PPP frame mapping procedures are supported. The mapping of GFP and PPP data into SDH containers is presented in figure 7.12.

The current design has only two types of traffic to be transported and for that reason, two different mappings are needed. After the data come from the GFP framer, they are saved into VCG-memories. These memories receive the data byte by byte basis and transmit the data to the SDH framer nine bytes at a time. This means that the whole container needs to be built before it can be equipped with the POH and transported further. The structure of the VCG memories is illustrated in figure 7.13. Depending on the size of the memory and the size of the desired container, a various number of containers can be mapped inside one memory block. Furthermore, all of the VCG memories require some amount of control logic for their purposes. In the first implementation, 16 of these VCG

83
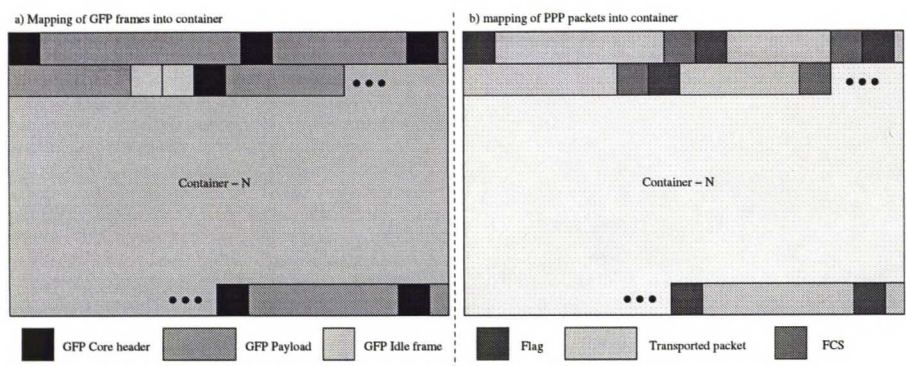
Figure 7.12: The mapping of different frames into SDH containers.
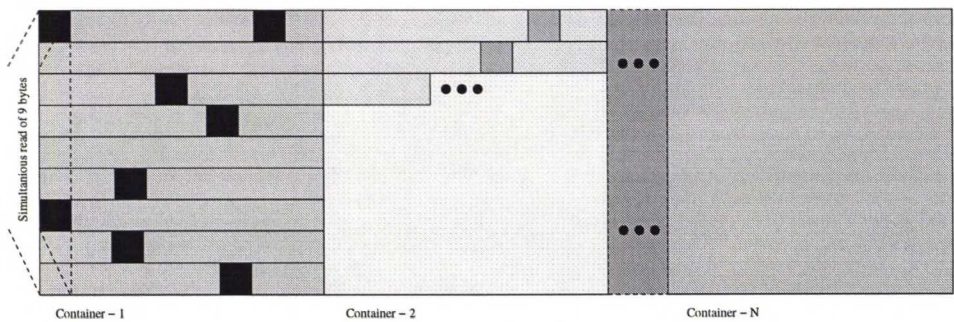
Figure 7.13: The structure of the Virtual Concatenation Group (VCG) -memories.

memory blocks are implemented, one for each of the STM-1 framers. These VCGs are divided between POS and Gb Ethernet transport in such a way that the Gb Ethernet gets 7 and the POS 9 VCGs. This is for the reason that the transportation of a Gb Ethernet over SDH requires a simultaneous use of 7 STM-1 frames. Furthermore, the interface signals between virtual concatenation and SDH framing blocks consist of the data and control signals of these memories.

The reserving of bandwidth for a certain channel in the SDH transportation means reserving of a certain number of containers for the channel transportation purposes. For this reason, all traffic other than best effort traffic needs to be have their specific connection settings specified in the Status/Control register. These settings are used in the virtual concatenation stage. The LCAS procedure exploits the H4 byte in the containers POH. It uses that byte to transport its control packets over the network. The sequence of how to use the H4 byte is presented in [IT00c] and [IT01c]. The transported control packet describes the state of the link during the next control packet. It has commands to add or remove members in or out of the group or inform that the transport does not support LCAS. Adding

and removing of VCG members increases or decreases the connection bandwidth respectively.

7.4.8 SDH framing

The transmission of data over TelecomBus requires a simultaneous framing of 16 STM-1 frames. The structure of the STM-1 frame is presented in figure 7.14, where the composition of the containers POH can also be seen. The STM-1 frame is formed by first selecting the content of the TOH bytes. Most of these bytes are fixed according to the SDH standard and cannot be modified or freely selected. However, the content of the AU-n pointer bytes (H1, H2 and H3) needs to be determined separately. As mentioned earlier, several alternatives of how to fill the STM-1 container with other containers exists, and the selected multiplexing sequence determines the content of these bytes. The formation of these bytes together with different container selections and multiplexing options can be found from [IT00c] and [IT00a]. At the first stage of the implementation, the STM-1 is composed with the following container-multiplexing sequence:

$$STM-1 \leftarrow AUG-1 \leftarrow 3 \times AU-3 \leftarrow VC-3 \leftarrow C-3$$

The containers and their POHs are created in the virtual concatenation block and then transported into SDH framer. After the completion of the TOH byte content selection, the containers are inserted into the frame according to the standards. Each of the 16 STM-1 frames is formed parallel in a way that the TelecomBus data flow can be created simultaneously. By this way, there is no need for a separate configuration memory, where the content of the frames must be preserved. At a later stage of the OAN implementation, efficient network functionality requires considerable increase in the number of VCG-memories.

The deframing of the STM-1 frames is performed similarly as the framing sequence. All of the 16 STM-1s are deframed in parallel. The received TOH bytes are either ignored or processed and the data are transported further to the receiving VCGs. The virtual concatenation block is responsible for the processing of the container POHs and separating the mapped data from the containers.

7.4.9 APS

The APS function is a switching function, where the protected or working data are directed into a beforehand-defined direction after an error situation exists in the network. Different APS functionalities are more deeply discussed in [Inc98]

85

				Section Overhead (SOH) 9 columns							Payload 261 columns		
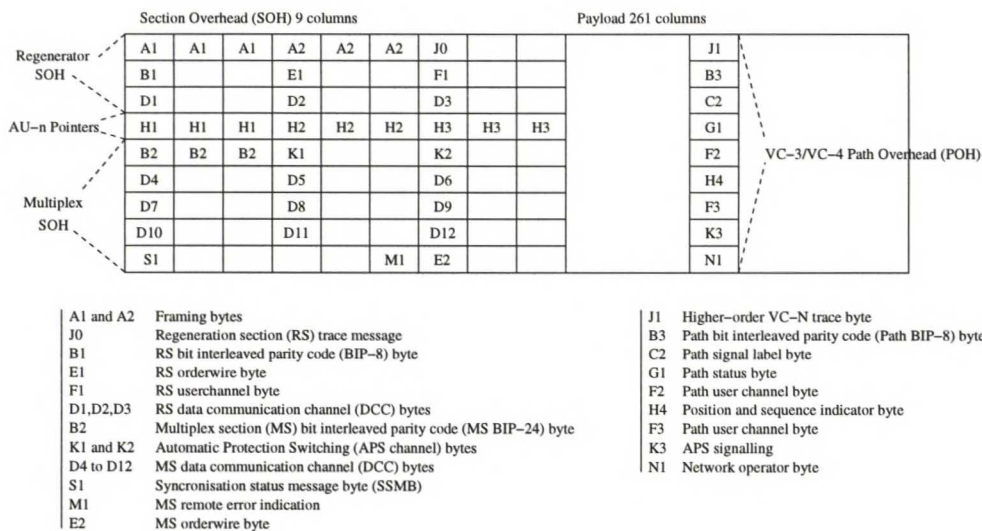
Figure 7.14: The structure of the STM-1 frame, adopted from [Tek01].

and [Inc02b]. The purpose in this implementation is to include the APS with such a switching ability that it can switch the signals between the preliminary TelecomBus interface blocks and the SDH framing and deframing blocks with all possible ways. By this way the APS switching sequence can be determined according to the specific error situation. Furthermore, the APS block can be used to provide loopback functionality in the design to be used for the testing purposes. The interface signals from the APS towards the other blocks are then the same signals required between the pre-TelecomBus and the SDH framer.

7.4.10 Parallel TelecomBus interface

The SDH framer chips have transmitting and receiving serial TelecomBus interfaces for the transmission of protection data, used in the APS protection. This protection data consists of four 8B/10B block coded STM-4 streams. The serial TelecomBus interface consist of four LVDS signal pairs, where each of the STM-4 data flow is transmitted at the speed of 777.6 Mb per second. Processing of serial data at this speed cannot be implemented in the Virtex-II architecture, so specific TelecomBus Serialiser (TBS) chip was selected to convert the data into parallel form. In this parallel form, the SDH data can be accessed on a byte-by-byte basis, which is essential for the DoS implementation. The signals in the parallel TelecomBus interface are presented in figure 7.15 and the functionality of the bus presented in [Inc01c]. The interface to the pre-TelecomBus consists of
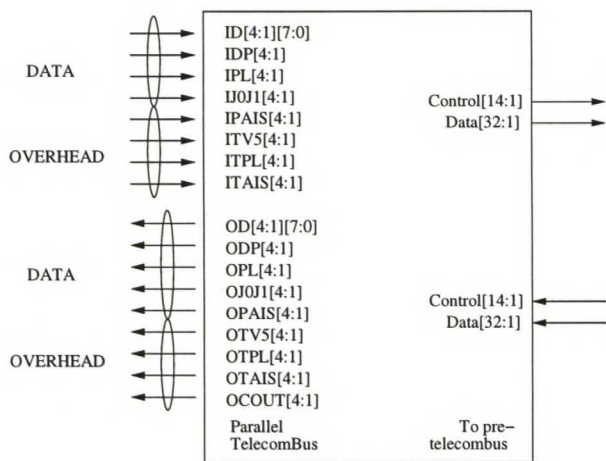
Figure 7.15: The signals in the parallel TelecomBus interface, adopted and modified from [Inc01c].

control and data signals, discussed more detail in next section.

7.4.11 Preliminary TelecomBus interface

The preliminary TelecomBus interface is used to transport the TelecomBus data from the larger FPGA to the smaller FPGA in the router card. Because there are only a limited number of signals available between the devices, specific protocol needed to be developed for the data transportation process, which provides information from the transported data on a byte by byte basis. As it was discussed in the previous chapter, the connection between FPGAs has 184 signals to be used for the pre-TelecomBus interface. These signals are divided between four interfaces, leaving 46 signals to be used in each of them. 32 of these signals are needed for the transportation of the data and 2 signals are left for the flow control. This means that the interface can use 12 signals to pass the byte basis information.

The required information in the TelecomBus can be divided into eight control characters presented in table 7.6. This means that each of the bytes transported over the pre-TelecomBus interface can be marked with a special TelecomBus character. By this way, the transportation of the TelecomBus data can be done synchronously over the FPGA limits, which means that the pre-TelecomBus signals are only connected from the APS block to the parallel TelecomBus block and the control characters are coded and decoded in these blocks respectively. So there is no need for a separate TelecomBus converter as presented in figure 7.3.

87

Table 7.6: Byte basis control code for Pre-TelecomBus interface.

Control	Description
000	Transport Overhead (TOH)
001	Payload Overhead (POH)
010	Payload
011	J0 byte
100	J1 byte
101	V5 byte
110	Alarm Indication Signal (AIS) high-order
111	Alarm Indication Signal (AIS) low-order

Chapter 8

Conclusions

In this thesis, the present structure of communication networks was studied and the requirements for future communication networks identified. Based on these requirements, a programmable logic design for an optical access network was presented to be implemented inside the Field Programmable Gate Arrays (FPGAs) of the OAN project network prototype.

8.1 Results

Today, three separate communication networks can be identified, telephony, data communications and broadcast networks. This overlaid network structure is complex to maintain, which causes extra cost to the operators. Furthermore, the complexity in the metropolitan area networks has become a bottleneck for the development of the transportation speed in the communication networks, and the emerging real-time and streaming media services cannot be supported by these networks. For these reasons, the development of communication networks is heading towards convergence. Converged networks are easier to maintain than the conventional networks, and all different access technologies are to be supported in hybrid transport systems. The Data over SDH (DoS) is one solution presented for the hybrid transport system in converged networks. It consists of separate transport and access network interfaces and a flexible Generic Framing Procedure (GFP) layer between them. This layer enables mapping of different access technologies over different transport technologies. In DoS, the network Quality of Service (QoS) is implemented with the efficient bandwidth reservation system provided by Virtual Concatenation (VC) and Link Capacity Adjustment

Scheme (LCAS). Furthermore, the utilisation of the Wavelength Division Multiplexing (WDM) enables faster increase of bandwidth in the networks.

The OAN project concentrates on developing the metropolitan area networking and based on the research, an optical feeder network prototype is being built. This prototype exploits the DoS scheme, which is implemented by programming the three FPGAs attached in the prototype board. The design presented in this thesis is a simplified version of the fully operational network. However, the design is structured in such a way that a fully operational network could be implemented only by updating the design blocks. The reason for simplified design implementation was the purpose to get the OAN test network operational as soon as possible. The use of the FPGAs allows the modification of the program over and over again, and to avoid problems, it is good to start with a small number of functionalities. Furthermore, the purpose was to present the simplified design with the amount of details typical of this type of design specification, but it was not possible within the scope of the thesis. For this reason, some of the functionalities of the design are presented lightly and the reader is guided to the source literature for more information.

8.2 Future developments

In the future, the functionality of the OAN test network should be increased. After the first version of the OAN test network is operational, additions to the programs can be made easily. The first additions should be the fully operational Gb Ethernet switch and fully functional SDH transport environment. This means that more Virtual Concatenation Groups (VCGs) need to be added for the VC and the rest of the SDH multiplexing sequences implemented. The connection between router and interface cards needs to be redesigned so that multiple cards can be connected together in both sides of the prototype. Furthermore, some improvements to the interface card register access procedure should also be made.

The network functionality is implemented in the larger FPGA in the router card, and the smaller FPGA is left almost unused. This unbalanced utilisation is not ideal, and some improvements should be made, especially when the network functionality is increased. The resources available in the larger FPGA may be too scarce for the future development, especially more internal memory might be needed in a later stage. For this reason, better resource utilisation for the smaller FPGA seems unavoidable. At least one possible solution exists for the purpose. It seems that the ring operations may be divided in such a way that the east ring operations may be implemented in the smaller FPGA and the west ring operations

in the larger FPGA. However, some difficulties with other functionalities may occur with this solution. At least the APS cannot be implemented similarly to the current design. For this reason, all the possible changes need to be considered separately.

The design of the implemented prototype was almost a success from the FPGA programming point of view. Some of the physical structures realised in the prototype brought difficulties in the program design, but mostly the physical solutions were proven competent. One problem was the division of the network functionalities between the two FPGAs in the router card. A solution for the problem was found, but it was not nearly a perfect one. Using only one FPGA in the router card would have made designing of the program easier and should be considered at least in the next revision of the prototype. In this revision it was not possible because of the large number of connection points needed, but the FPGAs have become larger since then, and it might be possible to have all connected into one FPGA. Furthermore, today there are SDH framing chips available on the market, which have the DoS functionality already implemented. Selecting this kind of chip to replace the SDH framer chip, TelecomBus chip and the DoS implementation in the FPGA, could decrease the number of connections needed in the router card. In addition, GFP has a support for direct Gb Ethernet transport, and the need for separate Gb Ethernet framer chip in the interface card should be considered in the next revision of the prototype.

91

Bibliography

[All01]   Resilient Packet Ring Alliance. An Introduction to Resilient Packet Ring Technology. White Paper, http://www.rpralliance.com, October 2001.

[All03]   Resilient Packet Ring Alliance. A Summary and Overview of the IEEE 802.17 RPR Standard. White Paper, http://www.rpralliance.com, August 2003.

[And02]   Per O. Andersson. Optical Network Trends. Presentation on Sunets Tekniska Rerensgrup, http://kokbok.sunet.se/trefpunkt/, March 2002. TREFpunkt Nr 6, Uppsala 13.03.2002.

[Arm97]   H. Armbruster. Information infrastructures and multimedia communications: different approaches of the telephone, data, and radio/TV worlds. *IEEE Communications Magazine*, 35(9):92–101, September 1997.

[ASFG+98]   Daniel Y. Al-Salameh, Mohammad T. Fatehi, William J. Gartner, Stan Lumish, Bruce L. Nelson, and Kamal K. Raychaudhri. Optical Networking. *Bell Labs Technical Journal*, January-March 1998.

[Bai03]   Brian Bailey. Total Verification. Mentor Graphics, Verification Seminars 2003, 10. March 2003. Espoo, Finland.

[Bel03]   Mary Bellis. The History of the Telegraph and Telegraphy. Webpages of What you need to know, 2003. http://inventors.about.com/library/inventors/bltelegraph.htm.

[Ben02]   K. Bengi. Access protocols for an efficient optical packet-switched metropolitan area ring network supporting ip datagrams. In *Eleventh International Conference on Computer Communications and Networks, 2002*, pages 284–289. IEEE, 2002.

[Ber00]   Janick Bergeron. *Writing Testbenches Functional Verification of HDL Models*. Kluwer Academic Publishers, 2000.

[BP01]   Richard Barr and Raymond A. Patterson. Grooming telecommunications networks. *Optical Networks Magazine*, 2(3):20–23, May/June 2001.

[Bre02]   Stefano Bregni. *Synchronization of Digital Telecommunication Networks*. John Wiley & Sons, Ltd., 2002.

[BRM01]   Paul Bonenfant and Antonio Rodriguez-Moral. Framing Techniques for IP over Fiber. *IEEE Network Magazine*, July/August 2001.

[BRM02]   Paul Bonenfant and Antonio Rodriguez-Moral. Generic Framing Procedure (GFP): The Catalyst for Efficient Data over Transport. *IEEE Communications Magazine*, 40(5):72–75, May 2002.

[Cav00]   Dirceu Cavendish. Evolution of Optical Transport Technologies: From SONET/SDH to WDM. *IEEE Communications Magazine*, 2000.

[Com01]   Terawave Communications. Next Generation Passive Optical Networks. White paper, http://www.terawave.com, January 2001.

[Con89]   J.K. Conlisk. Topology and survivability of future transport networks. In *Global Telecommunications Conference, 1989, and Exhibition. 'Communications Technology for the 1990s and Beyond'. GLOBECOM '89.*, pages 826–834 vol.2, 27-30 November 1989.

[Cor99]   Actel Corporation. Actel HDL Coding. Actel Corporation Style Guide, October 1999.

[CSK88]   G.H. Clapp, M. Singh, and S. Karr. Metropolitan area network architecture and services. In *Communications for the Information Age.*, volume 3, pages 1246–1254. Global Telecommunications Conference, 1988, and Exhibition., IEEE, 28 Nov-1 Dec 1988. Conference Record, GLOBECOM '88.

[DGA+99] P. Demeester, M. Gryseels, A. Autenrieth, C. Brianza, L. Castagna, R. Signorelli, G.and Clemenfe, M. Ravera, A. Lajszczyk, D. Janukowicz, K. Van Doorselaere, and Y. Harada. Resilience in multilayer networks. *IEEE Communications Magazine*, 37(8):70–76, August 1999.

[DHL+03]   H.J.S. Dorren, M.T. Hill, Y. Liu, N. Calabretta, A. Srivatsa, F.M. Huijskens, H. de Waardt, and G.D. Khoe. Optical packet switching and buffering by using all-optical signal processing methods. *Lightwave Technology*, 21(1):2–12, 2003.

[Ele01]   Samsung Electronics. 512Kx36 Pipelined NtRAM (K7N163645M). Datasheet, February 2001.

[EUa]   IST programme European Union. DAVID. Projects webpage, http://david.com.dtu.dk/. Duration July 2000 -July 2003.

[EUb]   IST programme European Union. HARMONICS. Projects webpage, http://www.ist-harmonics.net/. Duration: April 2000 - April 2003.

[fS94]   International Organisation for Standardisation. Open systems interconnection in general. ISO standard, 1994. ISO/IEC 7498-1:1994.

[GCC92]   M. Gerla, P. Camarda, and G. Chiaretti. Fault tolerant PON topologies. In *INFOCOM '92. Eleventh Annual Joint Conference of the IEEE Computer and Communications Societies*, pages 49–56 vol.1. IEEE, 4-8 May 1992.

[GJS03]   J. Gozdecki, A. Jajszczyk, and R. Stankiewicz. Quality of service terminology in IP networks. *IEEE Communications Magazine*, 41(3):153–159, March 2003.

[Gor00]   Walter Goralski. *SONET Second Edition*. McGraw-Hill, 2000.

[GR00]   O. Gerstel and R. Ramaswami. Optical layer survivability-an implementation perspective. *IEEE Journal on Selected Areas in Communications*, 18(10):1885–1899, October 2000.

[GRF02]   O. Gerstel, R. Ramaswami, and S. Foster. Merits of hybrid optical networking. In *Optical Fiber Communication Conference and Exhibit*, pages 33–34. OFC 2002, 17-22 March 2002.

[Gro]   Broadband Networks Group. Access Networks. Webpage. http://www.opto.eee.strath.ac.uk/BBN/.

[Gro03]   IEEE 802.17 Resilient Packet Ring Working Group. IEEE 802.17 Resilient Packet Ring (RPR) Standard. IEEE Standards, May 12th 2003. Draft ver. 2.2.

[GW02]   Steven S. Gorshe and Trevor Wilson. Transparent Generic Fram-
           ing Procedure (GFP): A Protocol for Efficient Transport of Block-
           Coded Data through SONET/SDH Networks. *IEEE Communica-
           tions Magazine*, 40(5):88–95, May 2002.

[HM02]   Pin-Han Ho and Hussein T. Mouftah. A Framework of Scalable Op-
           tical Metropolitan Networks for Improving Survivability and Class
           of Service. *IEEE Network*, 16(4):29–35, July/August 2002.

[HV02]   Enrique Hernandez-Valencia. Hybrid Transport Solutions for
           TDM/Data Networking Services. *IEEE Communications Magazine*,
           40(5):104–112, May 2002.

[HVSZ02]   Enrique Hernandez-Valencia, Michael Scholten, and Zhenyu Zhu.
           The Generic Framing Procedure (GFP): An Overwiev. *IEEE Com-
           munication Magazine*, 40(5):63–71, May 2002.

[Inc98]   PMC-Sierra Inc. Network Survivability Using Automatic Protection
           Switching (APS) over SONET/SDH Point-to-Point and Ring Net-
           works. Application note, PMC-960505, February 1998. Issue 3.

[Inc00]   PMC-Sierra Inc. POS-PHY Level 3 Saturn Compatible Packet Over
           Sonet Interface Specification For Physical And Link Layer Devices.
           Compatibility Specification, June 200. Issue 4.

[Inc00a]   Xicor Inc. X9110 Single Digitally-Controlled (XDCP) Poten-
           tiometer. Datasheet, November 2000. Revision 1.1.4.

[Inc00b]   Xicor Inc. X9221 Dual Digitally-Controlled Potentiometer (XDCP).
           Datasheet, June 2000. Revision 1.0.

[Inc00c]   Xilinx Inc. Virtex-2 Platform FPGA Handbook, December 2000.

[Inc01a]   PMC-Sierra Inc. A Saturn Packet And Cell Interface Specification
           For OC192 SONET/SDH And 10 Gigabit Ethernet. Interface Spe-
           cification, February 2001. Issue 6.

[Inc01b]   PMC-Sierra Inc. PM3386 S/UNI-2xGE Dual Gigabit Ethernet Con-
           troller. Datasheet, February 2001. Issue 6.

[Inc01c]   PMC-Sierra Inc. PM5310 TBS TelecomBus Serializer. Datasheet,
           November 2001. Issue 7.

[Inc02a]   PMC-Sierra Inc. PM5381 S/UNI-2488 User Network Interface for
           2488 Mb/s. Datasheet, April 2002. Issue 3.

[Inc02b]   PMC-Sierra Inc. SONET/SDH Automatic Protection Switching. Application note, PMC-2020827, May 2002. Issue 1.

[Inc02c]   Xilinx Inc. Next Generation Networking Technologies. Presentation in Metro-Optical Networking Forum, July 2002.

[Inc03]   Xilinx Inc. Xilinx 5 Software Manuals and Help. http://www.xilinx.com/support, 2003.

[IT98]   ITU-T. Broadband Optical Access Systems Based on Passive Optical Networks (PON). Recommendation G.983.1, October 1998.

[IT00a]   ITU-T. Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks. ITU-T Recommendation G.783, October 2000.

[IT00b]   ITU-T. Framework for Optical Transport Network Recommendations. ITU-T Recommendation G.871/Y.1301, October 2000.

[IT00c]   ITU-T. Network node interface for the synchronous digital hierarchy (SDH). ITU-T Recommendation G.707/Y.1322, October 2000.

[IT00d]   ITU-T. ONT Management and Control interface Specification for ATM-PON. Recommendation G.983.2, April 2000.

[IT01a]   ITU-T. A Broadband Optical Access System with Increased Service Capability by Wavelength Allocation. Recommendation G.983.3, March 2001.

[IT01b]   ITU-T. Generic Framing Procedure (GFP). ITU-T Recommendation G.7041/Y.1303, December 2001.

[IT01c]   ITU-T. Link capacity adjustment scheme (LCAS) for virtual concatenated signals. ITU-T Recommendation G.7042/Y.1305, November 2001.

[ITU02]   ITU-T, study group 15. *Recommendation of G.GPON.gsr - General Characteristics for Gigabit-capable Passive Optical Networks (GPON)*, December 2002.

[Kai02]   Antti Kaikkonen. Läpinäkyvä kaupunkialueen aallonpituuskanavoitu rengasverkko. Master's thesis, Helsinki University of Technology, December 2002.

[KP02]   Glen Kramer and Gerry Pesavento. Ethernet Passive Optical Net-
            work (EPON): Building a Next-Generation Optical Access Network.
            IEEE Communications Magazine, 40(2):66–73, February 2002.

[Lab00]   Stanford   University   Optical   Communications   Re-
            search   Laboratory.   IP-HORNET.   Projects   webpage,
            http://wdm.stanford.edu/iphornet/iphornet.html, 2000.

[LDA$^+$98] P. Lagasse, P. Demeester, A. Ackaert, W. Van Parys, B. Van
            Caenegem, M. O'Mahony, K. Stubkjaer, and J. Benoit. Roadmap
            towards the Optical Communication Age. A European view by
            the HORIZON project and the ACTS Photonic Domain, June 1998.
            Draft Edition.

[LGP01]   Ana Lardies, Rakesh Gupta, and Raymond A. Patterson. Traffic
            Grooming in a Multi-layer Network. *Optical Networks Magazine*,
            2(3):91–99, May/June 2001.

[MBK01]   A.R. Moral, P. Bonenfant, and M. Krishnaswamy. The optical In-
            ternet: architectures and protocols for the global infrastructure of
            tomorrow. *IEEE Communications Magazine*, 39(7):152–159, July
            2001.

[MF01]   Y. Maeda and R Feigel. A standardization plan for broadband access
            network transport. *IEEE Communications Magazine*, 39(7):166–
            172, July 2001.

[MHPG91]   K.S. Meier-Hellstern, G.P. Pollini, and D.J. Goodman;. A wireless
            service for the IEEE 802.6 metropolitan area network. In *Count-
            down to the New Millennium. Featuring a Mini-Theme on: Personal
            Communications Services*, volume 3, pages 1964 –1968. IEEE, 2-5
            Dec 1991.

[Mol88]   James F. Mollenauer. Standards for Metropolitan Area Networks.
            IEEE Communication Magazine, 26(4), April 1988.

[Muk97]   Biswanath Mukherjee. *Optical Communication Networks*. McGraw-
            Hill, 1997.

[MYMN02]   Kureina Murakami, Su-Hun Yun, Osamu Matsuda, and Mo-
            too Nishihara. New Transport Services for Next-Generation
            SONET/SDH Systems. *IEEE Communications Magazine*, 40(5):80–
            87, May 2002.

97

[Net02]   Flexlight Networks. GPON - The Next Big Thing in Optical Access Network: A Comparison Between EPON, APON and the Emerging GPON Technology. White paper, http://www.flexlight-networks.com, August 2002.

[Net03]   Foundry Networks. Metropolitan Area Networks. Application note, 2003.

[Ope02]   OpenCores.org.   OpenCores   Coding   Guidelines. http://www.opencores.org/, August 2002. Rev. 1.1.

[OSG02]   Fredrik Olsson, Jim Shupenis, and Alistair Gunn. Virtual Concatenation + LCAS. Technical report, Agilent Technologies, 2002.

[Par02]   Eugene Park. Error Monitoring for Optical Metropolitan Network Services. *IEEE Communication Magazine*, 40(2):104–109, February 2002.

[Pro97]   MAXIM Integrated Products. MAXIM +5V, low-power, voltage-output, serial 12-bit DAC MAX531. Datasheet, February 1997. Revision 6.

[Pro01]   MAXIM Integrated Products. MAXIM +2,7V, low-power, 4-channel, serial 12-bit ADC MAX1247. Datasheet, October 2001. Revision 2.

[Sep02]   Kari Seppänen. Transport services for converging networks. Licentiate's Thesis, October 2002. Helsinki University of Technology.

[SK03]   Gerry Pasavento Senior and Mark Kelsey. Gigabit Ethernet Passive Optical Networks. Wamin Optocomm Mfg. Corporation Publication, http://www.wamin.com, 2003.

[SS99]   A.A.M. Saleh and J.M. Simmons. Architectural principles of optical regional and metropolitan access networks. *Lightwave Technology*, 17(12):2431–2448, December 1999.

[STS02]   Toshiya Sato, Hiroki Takesue, and Toshihiko Sugie. Photonic Access and Metropolitan Area Networks for Broadband Services. In *Transparent Optical Networks, 2002, Proceedings of the 2002 4th International Conference*, pages 12–15, 2002.

[SZHVH02] Mike Scholten, Zhenyu Zhu, Enrique Hernandez-Valencia, and John Hawkings. Data Transport Applications Using GFP. *IEEE Communications Magazine*, 40(5):96–103, May 2002.

[Tec]   Agilent Technologies. An overview of ITU-T G.709. Application
            Note 1379. http://www.agilent.com/.

[Tec00]   PLX Technology.   PCI 9030 Data Book.   Data Book,
            http://www.plxtech.com, April 2000. Version 1.0.

[Tec02]   VTT Information Technology. Communications Technologies. The
            VTT Roadmaps. VTT Research notes 2146, 2002.

[Tek01]   Tektronix. SDH Telecommunications Standard Primer. Application
            note, August 2001. http://www.tektronix.com/.

[YJH⁺00]   Qiao Yaojun, Qi Jiang, Pu Hongtu, Chen Shuqiang, and Guan
            Kejian. A New Scheme for WDM-Based Passive Optical Access-
            network. Proceedings of ICCT2000, webpage http://www.ifip.or.at/,
            2000. Session S59.4.

[YYMD01]   Shun Yao, S.J.B. Yoo, B. Mukherjee, and S. Dixit. All-Optical
            Packet Switching for Metropolitan Area Networks: Opportunities
            and Challenges. *IEEE Communication Magazine*, 39(3):142–148,
            March 2001.

[ZD02]   H. Zhang and A. Durresi. Differentiated multi-layer survivability in
            IP/WDM networks. In *Network Operations and Management Sym-
            posium (NOMS)*, pages 681–694. IEEE/IFIP, 2002.