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ANALYSIS OF THREE SINGLE-STAGE CONVERTERS FOR POWER FACTOR CORRECTION

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ABSTRACT OF THE MASTER'S THESIS

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In this thesis three single-stage solutions for Power Factor Correction are analyzed. Analyzed topologies are: Boost Integrated with Flyback Rectifier/Energy storage/Dc-dc converter (BIFRED), Boost Integrated with Buck Rectifier/Energy storage/Dc-dc converter (BIBRED) and a modified Dither converter. The steady state equations and operational limits for the converters are deduced. Practical power range and peak current ratings, based on the analysis, are discussed.

Thesis includes design guidelines for high frequency Discontinuous Conduction Mode inductors. A 200 W prototype of BIFRED was built with the help of the design guidelines. The aim of the protype is to verify the steady state analysis and assess the quality of Power Factor Correction of the converter.

Keywords: Single-stage, Power Factor Correction, Line harmonics, EN 61000-3-2, BIFRED, BIBRED, modified Dither.

Teknillinen korkeakoulu **DIPLOMITYÖN TIIVISTELMÄ**

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Tässä diplomityössä on analysoitu kolmea yksiasteista ratkaisua tehokertoimen korjaukseen. Yksiasteisessa ratkaisussa tehokertoimen korjaus ja teholähteen lähtöjännitteen regulointi pyritään aikaansaamaan yhdellä aktiivisella kytkimellä. Analysoidut topologiat ovat: BIFRED, BIBRED ja modifioitu Dither.

Työssä johdetaan kyseisille topologioille pysyvän tilan yhtälöt ja toimintarajat. Yhtälöiden avulla pystytään määrittäämään mm. topologian ensiöpuolella sijaitsevan energivarastona toimivan ison kondensaattorin jännite kaikissa kuormitustilanteissa. Lisäksi tarkastellaan ratkaisuille sopivaa mielekästä tehoaluetta toimintarajojen puitteissa.

Työssä esitellään myös suunnitteluohjeita korkeataajuisten ja epäjatkuvalla toiminta-alueella toimivien kuristimien ja muuntajien suunnitteluun. Työtä varten rakennettiin 200W BIFRED, jonka avulla laskettuja tuloksia, pysyvän tilan analyysin onnistumista ja ratkaisun soveltuvuutta tehokertoimen korjaukseen arvioidaan.

Avainsanat: Tehokertoimen korjaus, yksiasteinen, verkkoharmoniset, EN-61000-3-2, BIFRED, BIBRED, modifioitu Dither

Preface

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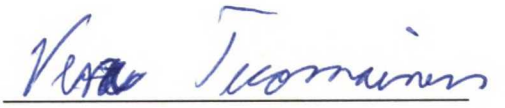

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Table of Contents

List of symbols and abbreviations

A_c	Cross sectional area of a ferrite core
A_e	Effective cross sectional area of a ferrite core
A_g	Cross sectional area of an air gap
$A_{g,e}$	Effective cross sectional area of an air gap
A_{min}	Minimum cross sectional area of the magnetic path in a ferrite core
b	Breadth of a bare conductor
b_a	Length of the center limb of a ferrite core
b_w	Winding breadth
$b_{w,min}$	Minimum winding breadth
B	Flux density
B_{peak}	Peak flux density
C	Capacitance of a capacitor
C_{oss}	Output capacitance of a MOSFET
d	Diameter of a conductor
DPF	Displacement Power Factor
D_1	Duty ratio of an active switch
$D_{2,n}$	Relative portion of the switching cycle when the DCM boost inductor current is decaying from the peak value to zero
f	Frequency
f_0	Resonance frequency
f_s	Switching frequency
F_l	Filling factor
F_r	Resistance factor
h	Effective height of a bare conductor
$I_{1,rms}$	Root Mean Square value of the line frequency component of the line current
I_D	Maximum continuous drain current of a MOSFET
I_{rms}	Rms value of the line current
I_n	n:th harmonic of the line current
I_{DC}	DC component of a current

$I_{D,avg}$	Average current through a diode
$I_{L2,peak}$	Peak value of the current through the inductor L_2
$I_{L,avg,n}$	Average value of n:th DCM boost inductor current pulse
$I_{L,peak,n}$	Peak value of the n:th current pulse through the DCM boost inductor
$I_{M,avg}$	Average magnetizing current of a transformer
I_{M0}	Value of the magnetizing current of a transformer at the end of a switching cycle
$I_{M,peak}$	Peak value of the magnetizing current of a transformer
$I_{refl,n}$	Average value of the n:th reflected DCM boost inductor current pulse
ΔI	A change in current
l_g	Length of an air gap
l_e	Effective length of a ferrite core
l_m	Length of the magnetic path
L_x	Inductance of the inductor x
L_M	Magnetizing inductance of the transformer
m	Mass
N	Number of turns in the winding of an inductor
N_1	Number of turns in the primary winding of a transformer
N_2	Number of turns in the secondary winding of a transformer
N_{1A}	Number of turns in the upper part of the primary winding of a tapped transformer
N_{1B}	Number of turns in the lower part of the primary winding of a tapped transformer
N_1/N_2	Turns ratio of a transformer
p	Number of winding layers
P	Power
P_h	Power loss in a ferrite core
$P_{h/V}$	Relative power loss in a ferrite core (per volume of the core)
$P_{h,avg}$	Average power loss in a ferrite core
$P_{h,max}$	Maximum allowed loss of a magnetic component
$P_{in,avg}$	Average input power
P_M	Average magnetizing power of a transformer
$P_{out,C}$	Average transferred power supplied by the bulk capacitor

$P_{\text{out,L1}}$	Average transferred power supplied by the DCM boost inductor
$P_{\text{pulse},n}$	Average power carried by the n:th DCM inductor current pulse
PF	Power Factor
R	Radius of the center limb of a ferrite core
ΔR	An add to the air gap radius due to presence of fringing flux
R_{DC}	DC resistance of a conductor
R_{S}	Value of the load resistance in the border of CCM and DCM operation
R_{load}	Load resistance
R_{th}	Thermal resistance
S	Apparent power
t	Time
t_{off}	Duration when the current through the switch decreases to zero
THD	Total Harmonic Distortion
T_{ambient}	Ambient temperature
T_{core}	Core temperature
T_{line}	Duration of the line cycle
T_{s}	Duration of the switching cycle
V	Volume of a ferrite core
V_{D}	Voltage across a forward biased diode
$v_{\text{in},n}$	Discrete line voltage
$V_{1,\text{rms}}$	Rms value of the line frequency component of the line voltage
V_{rms}	Rms value of the line voltage
$V_{\text{in,peak}}$	Peak value of the line voltage
V_{spike}	Peak value of the voltage spike caused by the leakage inductance of a transformer
V_{C}	Bulk capacitor voltage
$V_{\text{C,min}}$	Minimum bulk capacitor voltage
V_{C1b}	Voltage over the capacitor C_{1b}
V_{DSS}	Maximum drain-source voltage of a MOSFET
V_{out}	Output voltage
$V_{\text{L},n}$	Voltage over the DCM boost inductor in de-energizing phase.
V_{L2}	Voltage over the output inductor L_2
ρ_{c}	Conductivity of copper

μ	Permeability
μ_c	Permeability of copper
μ_0	Permeability of air
Δ	Penetration depth
φ	Parameter needed for the Dowell analysis
ϕ_1	Phase difference between the fundamental components of the line voltage and current
Φ	Flux
Φ_{peak}	Peak flux

AC	Alternating Current
C	Capacitor
CCM	Continuous Conduction Mode
D	Diode
DC	Direct Current
DCM	Discontinuous Conduction Mode
L	Inductor
rms	Root mean square
SMPS	Switched Mode Power Supply

1 Introduction

The standard EN 61000-3-2 /1/ sets strict limits for the harmonic content of the input current of a power supply. It is well known fact that input current of a traditional kind of Switched Mode Power Supply (SMPS) has abundant harmonic content. Therefore, need for low cost power factor correction is obvious. Power factor correction can be achieved by passive or active solutions. Passive solutions are usually too clumsy and bulky for small power supplies. On the other hand, active solutions require additional control circuit and switching device, which means increase in costs of the power supply.

Although the name of the thesis includes the words power factor correction it must be emphasized that it is more question of reduction of line current of a rectifier. This should become evident within the thesis.

Single-stage solutions have only one switching stage and consequently only one control circuit. However, despite of only one switching stage they are able to produce an acceptable input current and a regulated output voltage. These features make the family of single-stage converters attractive as low cost solutions for power factor correction. However, single-stage solutions have a few disadvantages such as the rise of the bulk capacitor voltage at light loads. A comparative study was carried out between three single-stage solutions from a practical point of view. The study concentrates on determining the steady state operation of the converters under practical limits such as the upper limit for the bulk capacitor voltage of 450 V. Three topologies were chosen to be evaluated as low cost solutions: BIBRED, BIFRED and a modification of the Dither converter, what we call here as Modified Dither.

The input current of traditional kind of SMPS and standard EN 61000-3-2 are briefly discussed in Chapter two. Two passive solutions and one active solution for power factor correction is shown and discussed. The three single-stage solutions are analyzed in Chapter three. Steady state operation of the converters and particularly the behavior of the bulk capacitor voltage are deduced and discussed. Peak currents and practical power range are also considered. Design guidelines for the magnetic components of BIFRED are provided in Chapter four. Losses in the core and winding, winding arrangements and thermal aspects are discussed. Measured results are included in

Chapter five to support the analysis and to verify that compliance with the standard is achieved. Finally, conclusions are made and topics for further research proposed in Chapter six.

2 Background of power factor correction

2.1 General

Traditional SMPS, for example the one in Fig. 2.1, has low power factor, which is due to the combination of the diode bridge and the large DC-capacitor C_1. An ultimate goal of the SMPS is to supply a smooth, regulated and, perhaps, isolated output voltage, which is usually processed from the sinusoidal line voltage. SMPS consist of three parts: an input rectifier, a high frequency inverter and an output rectifier. Purpose of the input rectifier is to convert the sinusoidal line voltage to a DC voltage. The input rectifier is composed of the rectifier bridge and the large DC capacitor. The bridge contains four diodes and the voltages before and after the bridge determine whether a diode in the bridge is able to conduct or not. The capacitor has three tasks to deal with: offer a DC input voltage for the inverter, balance the 100 Hz power swinging of the utility grid and provide an energy storage to cover sudden blackouts of the utility grid (lasting from couple of milliseconds to even tens of milliseconds). A large capacitor fulfills all of the requirements mentioned above because it is able to retain relatively steady DC voltage over itself and store a large amount of energy to cover the blackouts.

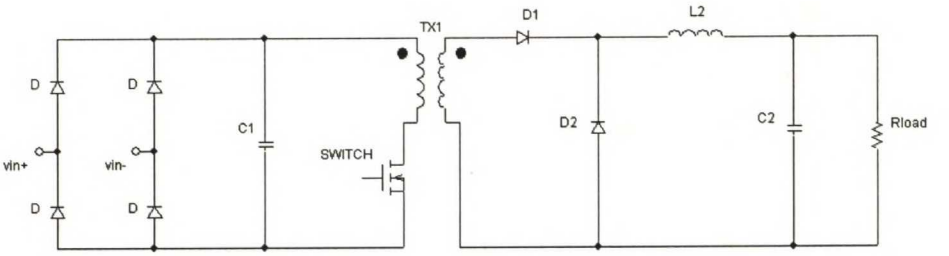

Figure 2.1 A forward type SMPS. The diode bridge and the capacitor C_1 form the input rectifier. The SWITCH, transformer TX1 and C_1 form the high frequency inverter. Diodes D_1 and D_2, inductor L_2 and capacitor C_2 form the output rectifier.

The bulk capacitor C_1 is charged to a voltage level equal to the peak line voltage every half line cycle. Since the capacitor is large in value, the voltage across it droops only a little bit during next half line cycle. On the other hand, the diodes in the bridge are able to conduct only when the line voltage is larger than the voltage over the capacitor. This means that the DC energy being consumed in the load and the energy consumed to losses in the circuit itself, have to be brought into the circuit in a very narrow strip of time, when the diodes are able to conduct. The resulting line current is composed of

narrow and high spikes. Rectified sinusoidal waveform, typical bulk capacitor voltage and the resulting distorted line current are presented in Fig. 2.2.

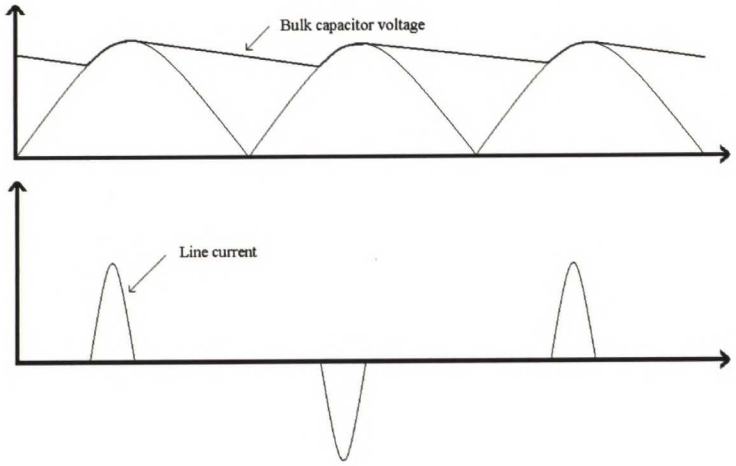

Figure 2.2 Rectified sinusoidal line voltage and a bulk capacitor voltage in the upper picture. The diodes in the bridge are able to conduct when the rectified line voltage reaches the bulk capacitor voltage. Resulting non-sinusoidal line current is shown in the lower picture.

2.2 Basic definitions

SMPS can be considered as a resistive load. Phase-lag between the line frequency components of the line voltage and the current is often negligible. Power factor *PF* /2/ is defined as the actual power drawn from the utility grid divided by the corresponding apparent power. Power factor is as follows

$$PF = \frac{P}{S} = \frac{V_{1,\mathrm{rms}} I_{1,\mathrm{rms}}}{V_{\mathrm{rms}} I_{\mathrm{rms}}} \cos\phi_1 \approx \frac{I_{1,\mathrm{rms}}}{I_{\mathrm{rms}}} DPF \approx \frac{I_{1,\mathrm{rms}}}{I_{\mathrm{rms}}} \tag{2.1}$$

where P stands for power, S for apparent power, $V_{1,\mathrm{rms}}$ for the rms value of the line frequency component of the line voltage, V_{rms} for the rms value of the line voltage, $I_{1,\mathrm{rms}}$ for rms value of the line frequency component of a line current, I_{rms} for the rms value of line current, ϕ_1 symbolizes the phase-lag between the fundamental components of the voltage and the current and $\cos\phi_1$ is the displacement factor *DPF*. SMPS is a tiny equipment compared to the utility grid. Line voltage distortion caused by a single power supply is negligible and thus V_{rms} and $V_{1,\mathrm{rms}}$ are approximately equal. As mentioned earlier, the phase-lag between the fundamental components of the voltage and the current is negligible in a diode rectifier. Therefore, the displacement factor $\cos\phi_1$ can be omitted and power factor *PF* can be approximated to be the ratio of the rms value of the line frequency component of the current to the rms value of the line current.

Another important factor is the total harmonic distortion *THD* /2/. *THD* describes the ratio of the root mean square value of the harmonic currents to the line frequency component of the line current. *THD* is as follows

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{2.2}$$

where the I_n denotes the rms value of the n:th harmonic of the line current and I_1 is the rms value of the line frequency component of the line current.

When the line voltage is not distorted, the power factor and the total harmonic distortion have a relation /2/ as follows

$$PF = \frac{1}{\sqrt{(1+THD^2)}} DPF \tag{2.3}$$

Crest Factor /2/ is defined as follows

$$\text{Crest Factor} = \frac{I_{s,peak}}{I_s} \tag{2.4}$$

Where $I_{s,peak}$ is the peak value of a current waveform and I_s the rms value of the current.

2.3 Harmonic standard EN 61000-3-2

The imminent introduction of the standard EN 61000-3-2 will set strict limits for line current harmonics of SMPS for the power supply manufacturers /1/. Main points of the standard are briefly presented in this chapter. The standard divides electric equipment to five classes: A, B, C, D and E. Selection chart for a class of an electric equipment is presented in Fig. 2.3.

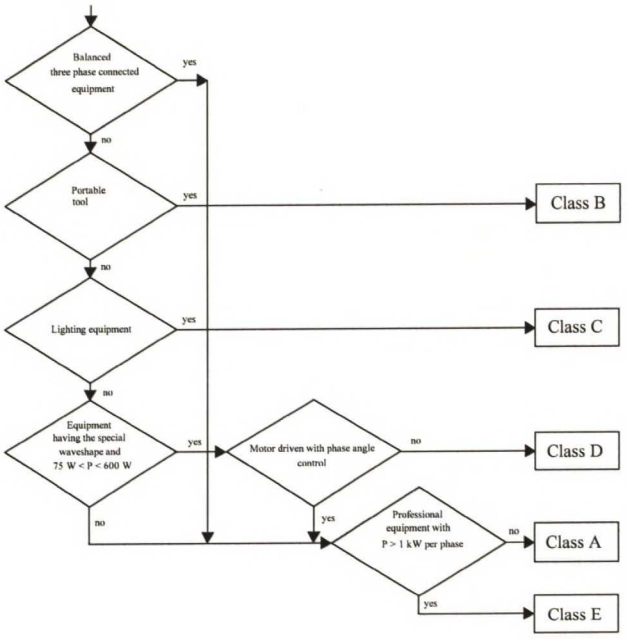

Figure 2.3 Selection chart for a class of an electronic equipment. The chart and thus the standard divides electric equipment into five different classes: A, B, C, D and E, /1/.

Classes A and D cover single-phase supplied electric equipment in the power range of 75 to 600 W. These two classes are of interest in the thesis. Whether an equipment belongs to class A or D is determined by a special template. The template is depicted in Fig. 2.4.

For the determination one has to set the waveform of a half line current to the template. The highest point of the waveform must coincide with the centerline of the template. If over 95 % of the current lies inside the template then the equipment belongs to the class D. If over 5 % of the current exceeds the template then the equipment is considered to belong to the class A. One must notice that the vertical axis of the template is relative.

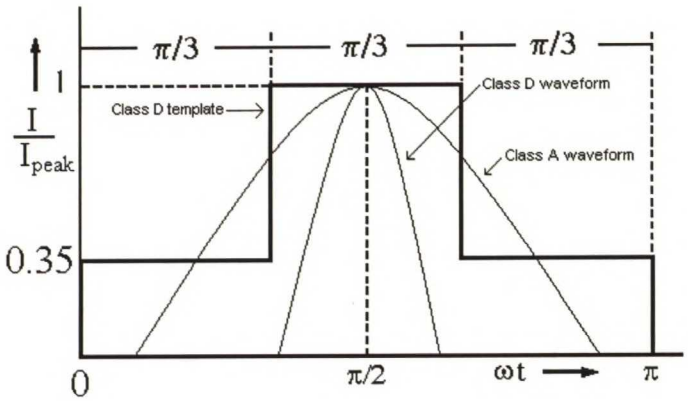

Figure 2.4 Special template for the determination whether an electric equipment belongs to the class A or D. Note that the vertical axis of the template is relative, /1/.

Current limits for the class A and D equipment are presented in Table 2.1. The limits are absolute values for the class A and relative for the class D. For example, for a 100 W SMPS the limit for the third harmonic is in the class A is 2.3 A and in the class D only 0.34 A. The class D penalizes high crest factor equipment. One example of equipment, which has a high crest factor, is depicted in Fig. 2.1. Current with high crest factor is known to have a very abundant harmonic content. Since the limits for the harmonic currents are very strict for the high crest factor equipment, it may be difficult to meet the limits with the traditional kind of SMPS. The conclusion is that manufacturers have to add power factor correction into their SMPS's in order to meet the limits set by the standard EN 61000-3-2.

Harmonic	Class A	Class D
n	A [rms]	mA [rms] / W
3	2.30	3.40
5	1.14	1.90
7	0.77	1.00
9	0.40	0.50
11	0.33	0.35
13	0.21	0.296
15>	2.25/n	3.85/n

Table 2.1 Limits for the line current harmonics in the class A and the class D. The limits are relative for the class D and absolute for the class A, /1/.

2.4 Passive solutions for power factor correction

A passive solution does not have an active switch. The simplest passive solution has an inductor added between the bridge and the bulk capacitor. The schematic of the solution is presented in Fig. 2.5. The inductor tries to spread the current waveform and bring down the peak of the current. If the inductor is large enough, the current will have a desired shape and the equipment will belong to the class A. Drawback of the solution is that the inductor operates at the line frequency. This relatively low frequency means that the inductor is large in value and size. The purpose of SMPS is to be a small size power supply and therefore the large size of the inductor is not desirable and the solution is impractical for low power level equipment.

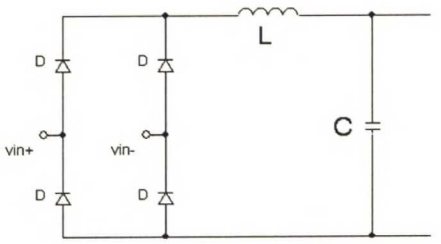

Figure 2.5 A simple passive solution for power factor correction. Inductor L is added between the bridge and the bulk capacitor C.

Another passive solution for power factor correction is presented in Fig. 2.6, /3/. Resonance frequency of the LC filter is tuned to the line frequency. Therefore, the filter represents zero impedance for the line frequency component of the line current and for the harmonics the filter represents a high impedance. Hence, the harmonics are attenuated to some extent. The resonance frequency of the filter is calculated as follows

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.5}$$

where the f_0 symbolizes the desired resonance frequency of the filter, L inductance and C capacitance. A few drawbacks are unfortunately found from the solution. For example, if the frequency is chosen to be 50 Hz, the corresponding values for the inductor and the capacitor are (for example) L = 20 mH and C = 500 µF. Again, the inductor is large in value and due to the low operation frequency it is large in size, too. On the other hand, a 500 µF AC-rated capacitor is definitely not an economic solution. It seems that this is not a convenient solution for a low power level equipment either.

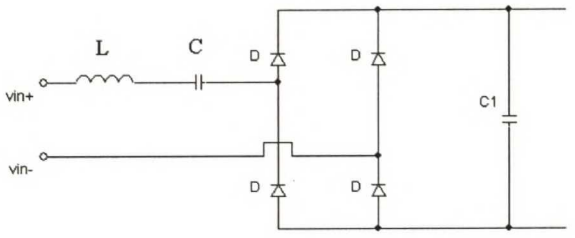

Figure 2.6 A passive solution for power factor correction. The LC-filter is tuned to attenuate the harmonic currents and pass the line frequency component of the current, /3/.

2.5 Active solution

The most popular way to attain a proper power factor is to add a boost converter between the bridge and the bulk capacitor, /4/. The two-stage solution, as we call it, includes two active converters: one to deal with the power factor correction and another to produce the desired output. The solution is depicted in Fig. 2.7. The boost converter operates at high frequency in order to keep the size of the boost inductor relatively small. There are many control methods for the boost converter found in the literature, /5/. The purpose of the converter, no matter how it is controlled, is to shape the input current of the SMPS to resemble the sinusoidal waveform. The solution is very effective and a unity power factor is almost attained. Drawbacks of the two-stage solution are: an additional switch and control circuit and more complicated circuit structure.

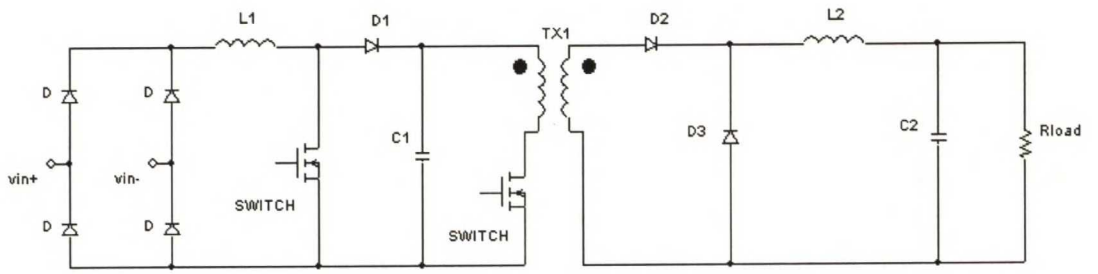

Figure 2.7 Two-stage solution for power factor correction. L_1, D_1 and SWITCH form the boost converter. The boost converter shapes the line current to resemble a sinusoidal waveform.

3 Some single stage solutions

Single-stage solution is a converter with only one active switching stage, which can be split to several switching devices in order to gain strength against voltage or current stresses, but only one control circuit is included in the converter. Consequently, a single-stage solution has only two operation modes: the switch is turned on or off. Single-stage solutions have two ultimate goals. They try to produce acceptable power factor correction and a regulated and isolated output voltage at the same time. These things are characteristic for them.

Three single stage solutions are presented in this chapter. The basic operation under steady state conditions is described and general equations ruling their behavior are deduced and presented. In the analysis all components of a converter are considered as ideal ones. This means that the conduction and switching losses are omitted and DC voltages throughout the converter do not have a ripple of any kind. The duty ratio D_1 of a switch is assumed to be constant for a certain load. This means that D_1 is adjusted to the constant value in order to get the output voltage V_{out} as desired. V_{out} is also considered to have an exact and constant value since one goal of a power supply is to produce the regulated output voltage. An EMI filter is an essential part of the converter. However, it does not have very much effect on the steady state analysis of a single stage converter and therefore it is omitted in the analysis.

In a line cycle there are $n = T_{line}/T_s$ switching cycles. T_{line} symbolizes the length of the line cycle and T_s is inverse of the switching frequency. Supposing that the switching frequency is considerably higher than the line frequency, the sinusoidal line voltage can be approximated to be constant during one switching cycle. We can write

$$v_{in,n} = V_{in,peak} \sin(\omega_{line} * n * T_s) \qquad \textbf{(3.1)}$$

where $v_{in,n}$ is the approximated constant value of the line voltage during the n:th switching period, $V_{in,peak}$ the peak value of the line voltage, ω_{line} the angular frequency of the line voltage. Here n ranges from 1 to T_{line} / T_s and it is assumed that $n = 1$ when $0 \leq t \leq T_s$ and $n = T_{line} / T_s$ when $(T_{line} - T_s) \leq t \leq T_{line}$, where t is time.

Single-stage solutions have only one switching stage and thus only one degree of freedom. However, they should be able to produce an acceptable power factor and a regulated output voltage. It is impossible to control two variables with only one degree of freedom. Consequently, one of the goals has to be achieved inherently or "free of charge". It is a well known fact that the current of a DCM boost converter tracks the feeding voltage waveform, if the switch operates at constant duty cycle, /6/. Good or moderate power factor can be expected if the current through the boost inductor tracks the sinusoidal waveform. Thus, the DCM operation of the boost converter is crucial for the single-stage solutions presented.

Current through the inductor consists of a sequence of triangular pulses, depicted in Fig. 3.1. Each switching cycle n causes a certain current pulse to flow through the inductor. The rise time of the pulse D_1T_s is constant all the time but the decaying time $D_{2,n}T_s$ and the height of the pulse $I_{L,peak,n}$ depend on the switching cycle n, which defines the voltage, Eq (3.1). This will be discussed for each topology separately.

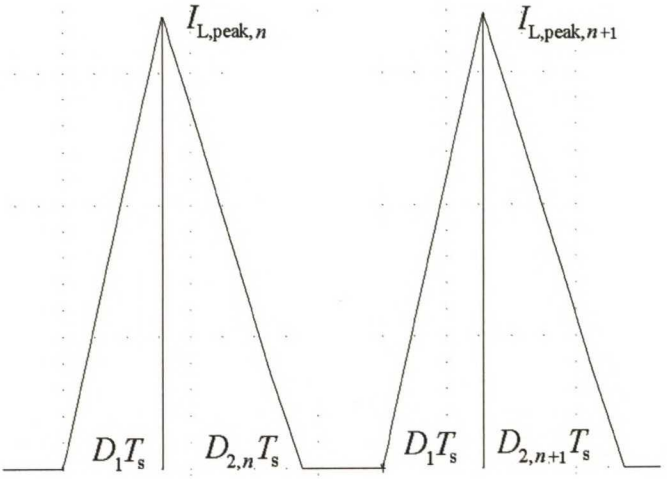

Figure 3.1 DCM inductor current. Current pulse developes during D_1T_s and decays during $D_{2,n}T_s$. The width and the height of the current pulse depend on the switching cycle n.

The current through the DCM inductor should remain discontinuous, e.g. $(D_1 + D_{2,n}) \leq 1$. Therefore, the condition $(D_1 + D_{2,max}) = 1$ defines the maximum available input power for the converter. $D_{2,max}$ denotes the value of $D_{2,n}$ when $v_{in,n} = V_{in,peak}$ and it is the critical instance of the line cycle.

In sections 3.1, 3.2 and 3.3 BIFRED, BIBRED and Modified Dither are analyzed respectively. In the following analysis DCM + CCM means that the input stage of the

converter operates in DCM and the output stage in Continuous Conduction Mode. Similarly, DCM + DCM means that both the stages operate in DCM.

3.1 BIFRED

3.1.1 General

BIFRED stands for Boost Integrated with Flyback Rectifier/Energy storage/Dc-dc converter /7/. The topology is shown in Fig. 3.2. It has only one switching stage and thus it is clearly a single-stage converter. BIFRED consist of three parts: an EMI-filter (L_f + C_f), a DCM boost converter and a flyback converter. The converters are little bit overlapped with each other. In the input side, inductor L_1, diode D_1, capacitor C_1 and switch form the boost converter. The capacitor C_1, switch, flyback transformer TX1 and the whole secondary form the flyback converter.

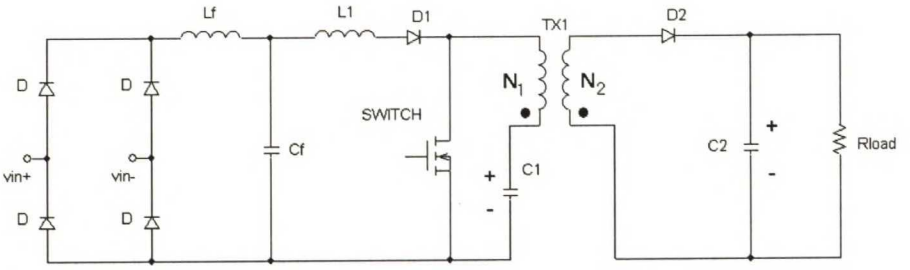

Figure 3.2 BIFRED /7/. L_f and C_f form the EMI-filter, L_1, D_1 and switch form the DCM boost converter and switch, C_1, flyback transformer and the whole secondary form the flyback converter.

One essential part of BIFRED is the EMI filter right after the rectifier bridge. The purpose of the filter is to reduce the noise caused by the DCM operation of the boost inductor and to provide continuous line current trough the bridge during a half line cycle. Continuous current enables the use of slow diodes in the bridge.

3.1.2 Operation

BIFRED has two operation modes: switch turned on or off. The operation of the converter in those two modes is briefly described in this section. Current paths for both of the modes are shown and applied voltages explained.

3.1.2.1 Switch on

When the switch is turned on, the line voltage is applied across the DCM boost inductor. The sinusoidal line voltage energizes the inductor and the current through the inductor starts to rise from zero to $I_{\mathrm{L,peak},n}$, which is defined as follows

$$I_{\mathrm{L,peak},n} = \frac{|v_{\mathrm{in},n}| D_1 T_\mathrm{s}}{L_1} \tag{3.2}$$

where L_1 denotes value of the inductance of the boost inductor and $v_{\mathrm{in},n}$ is from Eq (3.1). At the same time, the bulk capacitor voltage is applied to the primary winding of the flyback transformer. The output diode D_2 at the secondary side is reverse biased during this operation mode. Peak value of the magnetizing current of the transformer is as follows

$$I_{\mathrm{M,peak}} = I_{\mathrm{M0}} + \int_{nT_\mathrm{s}}^{nT_\mathrm{s}+D_1T_\mathrm{s}} \frac{V_\mathrm{C}}{L_\mathrm{M}} dt = I_{\mathrm{M0}} + \frac{V_\mathrm{C} D_1 T_\mathrm{s}}{L_\mathrm{M}} \tag{3.3}$$

where I_{M0} is the minimum value of the current after a switching cycle, V_C is the bulk capacitor voltage which is a constant in steady state and L_M magnetizing inductance of the transformer. The load draws energy from the output capacitor C_2.

Paths of the currents during the switch-on mode are illustrated in Fig. 3.3.

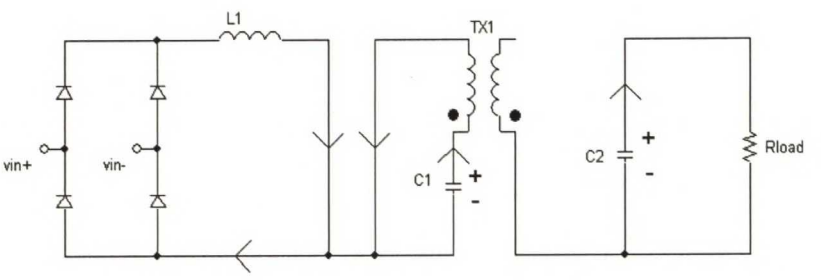

Figure 3.3 BIFRED during the switch-on mode. EMI filter is omitted. The rectified line voltage energizes the inductor L_1 and the flyback transformer is energized by the capacitor C_1. Both of the currents circulate through the switch. The load draws power from the output capacitor C_2.

3.1.2.2 Switch off

When the switch is turned off, the DCM boost inductor is de-energized. Voltage across the secondary winding of the flyback transformer is fixed to the output voltage V_{out} and

voltage across the primary winding is the output voltage multiplied by the turns ratio N_1/N_2. Therefore, the voltage over the boost inductor has the following value

$$V_{L,n} = v_{in,n} - \left(V_C + \frac{N_1}{N_2} V_{out} \right) \tag{3.4}$$

until the inductor is de-energize. At the same time, the magnetizing inductance of the flyback transformer reverses its polarity and the diode D_2 becomes forward biased. Consequently, the flyback transformer is de-energized to the capacitor C_2 and the load.

Paths of the currents during the switch-off mode are depicted in Fig. 3.4.

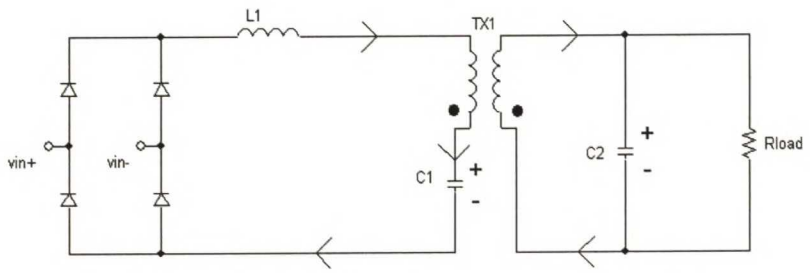

Figure 3.4 BIFRED during the switch-off mode. EMI filter is omitted. Boost inductor L_1 is completely de-energized and the flyback transformer is partly (DCM operation) or completely (CCM operation) de-energized during the switch-off mode.

3.1.3 Input stage

Eq. (3.2) reveals that the peak value of a current pulse is proportional to the discrete value of the line voltage. Peaks of the current follow the waveform of rectified line voltage if the duty ratio is kept constant. The current trough the boost inductor is depicted in Fig. 3.5.

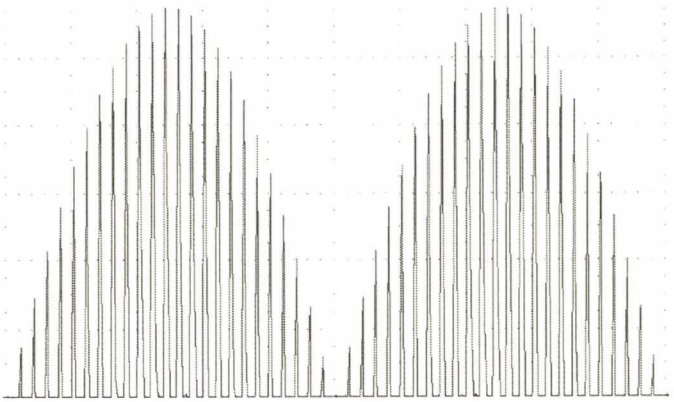

Figure 3.5 The current trough the DCM-boost inductor. Duty cycle is kept constant during the line cycle. The envelope of the waveform greatly resembles the rectified sinusoidal waveform despite of the fact that in the picture the switching frequency is only 50 times higher than the line frequency.

From Fig. 3.5 it is easy to see that the current of the DCM boost inductor does track the rectified line voltage waveform, as was desired. Consequently, a proper power factor can be expected.

Power is transferred to the circuit in triangular current pulses. One pulse carries a power

$$P_{\text{pulse},n} = \left|v_{\text{in},n}\right| I_{\text{L,avg},n} = \left|v_{\text{in},n}\right| \frac{I_{\text{L,peak},n}}{2}\left(D_1 + D_{2,n}\right) = \frac{v_{\text{in},n}^2 D_1 T_s}{2L_1}\left(D_1 + D_{2,n}\right) \tag{3.5}$$

where $P_{\text{pulse},n}$ is average power carried by a current pulse, $I_{\text{L,avg},n}$ the average value of the pulse, $D_{2,n}$ the relative portion of the switching cycle T_s when the triangular pulse is decaying. $D_{2,n}$ is to be calculated as follows

$$D_{2,n} = \frac{\left|v_{\text{in},n}\right| D_1}{V_C + \frac{N_1}{N_2} V_{\text{out}} - \left|v_{\text{in},n}\right|} \tag{3.6}$$

Eq. (3.6) is based on the fact that the average volt-second balance across the boost inductor should be equal to zero in steady state.

By summing the value of power associated to every pulse during a line cycle and dividing it by the amount of switching cycles, average input power is obtained. Average input power of BIFRED is as follows

$$P_{\text{in,avg}} = \frac{D_1 T_s}{2L_1}\left[\sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} v_{\text{in},n}^2\left(D_1 + D_{2,n}\right)\right] \times \frac{T_s}{T_{\text{line}}} \tag{3.7}$$

3.1.4 Output stage

The output stage of BIFRED is a regular flyback converter. When the switch is turned on, the bulk capacitor voltage is applied across the primary winding of the transformer as in a normal flyback converter. The flyback part can operate either in DCM or CCM. Because these two modes differ from each other radically, they are considered separately.

3.1.4.1 CCM operation

In CCM the output voltage of the flyback-stage is strictly defined by V_C, turns ratio and duty ratio. That is because the average volt-second balance across the magnetizing inductance of the flyback transformer has to be equal to zero. Hence, the output voltage is defined as follows

$$V_{out} D_1 T_s = \frac{N_2}{N_1} V_C (1 - D_1) T_s \Rightarrow V_{out} = \frac{N_2}{N_1} V_C \frac{D_1}{1 - D_1} \tag{3.8}$$

If the output voltage is regulated to a constant value, as assumed, the voltage over the bulk capacitor has to be as follows

$$V_C = \frac{N_1}{N_2} V_{out} \frac{1 - D_1}{D_1} \tag{3.9}$$

Steady state value of V_C is constant in DCM + CCM operation of the converter for a certain load because D_1 and V_{out} are assumed to be constants. However, if the load is reduced or increased then D_1 has to be adjusted to a new value in order to retain the constant output voltage. Consequently, V_C has also a new steady state value. The voltage over the bulk capacitor depends on the load: if the load is reduced the resulting new steady state voltage is higher than before the reduction and vice versa, if the load is increased the resulting steady state V_C is lower than before the increase.

The minimum value for the bulk capacitor voltage is defined by the peak line voltage $V_{in,peak}$. There is a danger, if the V_C falls below the $V_{in,peak}$, that the input stage enters to CCM operation at vicinity of the peak line voltage and DCM operation of the boost inductor is lost while the capacitor is being charged to the peak line voltage. To ensure proper operation of the converter, the condition

$$V_{C,min} \geq V_{in,peak} \tag{3.10}$$

should be fulfilled, where $V_{C,min}$ is the minimum allowed bulk capacitor voltage.

3.1.4.2 DCM operation

Output stage enters to the DCM operation when the current through the secondary winding of the flyback transformer reaches zero before the end of a switching cycle.

This means that equations (3.8) and (3.9) are not valid anymore and voltage over the bulk capacitor has to be determined from a power balance.

Input power can be calculated as before because the input stage operates in the same way as it did earlier. Power is injected from the primary side of BIFRED to the secondary side in two different ways. First one is the power supplied by the bulk capacitor and the other the power supplied by the boost inductor directly to the secondary side. Both of the ways are discussed below.

In DCM operation of the flyback stage the power supplied by the bulk capacitor C_1 from the primary side to the secondary side is as follows

$$P_{\text{out,C}} = V_{\text{C}} I_{\text{M,avg}} = V_{\text{C}} \frac{I_{\text{M,peak}}}{2} D_1 = \frac{V_C^2 D_1^2 T_s}{2L_{\text{M}}} \tag{3.11}$$

This is the energy stored in the magnetic circuit when the switch is conducting and it is released when the switch is turned off.

When the switch is turned off the energized boost inductor begins to de-energize to the bulk capacitor *through* the flyback transformer's primary winding as it was depicted in Fig. 3.4. This causes a current, proportional to the decreasing part of the boost inductor current pulse, to flow in the secondary side. Therefore, the current trough the output diode D_2 is a sum of the reflected boost inductor and the 'normal' transformer current. This is depicted in Fig. 3.6.

Average value of the reflected current, for a current pulse, is as follows

$$I_{\text{refl},n} = \frac{N_1}{N_2} \frac{I_{\text{L,peak},n}}{2} D_{2,n} = \frac{N_1}{N_2} \frac{|v_{\text{in},n}| D_1 T_s}{2L_1} D_{2,n} \tag{3.12}$$

The reflected current carries power, which is delivered directly from the inductor to the output. Average power carried by the reflected boost inductor current pulses is as follows

$$P_{\text{out,L1}} = V_{\text{out}} \sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} I_{\text{refl},n} = \frac{\text{N}_1}{\text{N}_2} \frac{V_{\text{out}} D_1 T_s}{2L_1} \left[\sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} \left(|v_{\text{in},n}| D_{2,n} \right) \right] \times \frac{T_s}{T_{\text{line}}} \tag{3.13}$$

It is delivered straight from the boost inductor to the secondary side during a line cycle.

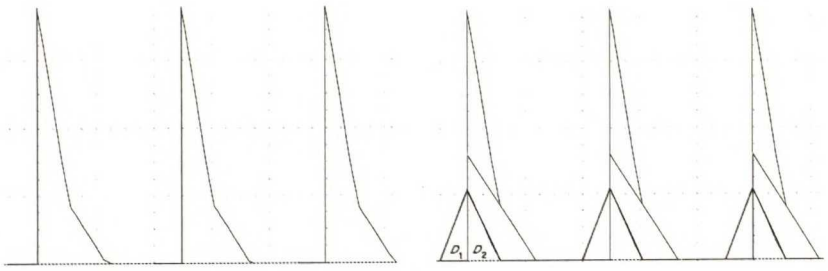

Figure 3.6 Output diode current of BIFRED converter, here in DCM operation. The left picture shows the current and the right picture depicts the same current and its two components: boost inductor current and the de-energizing transformer current. In the figure Boost inductor current is depicted as bolded (almost equilateral) triangle and the normal flyback transformer current is depicted as right-angled triangle. The diode current is sum of the right-angled triangle and right half of the bolded triangle multiplied by the turns ratio. $P_{\text{out,C}}$ in Eq. (3.11) is carried by the right-angled triangles and $P_{\text{out,L1}}$ of Eq. (3.13) is carried by the right halves of the bolded triangles.

Total amount of transferred power from the primary to the secondary is obtained by summing $P_{\text{out,C}}$ and $P_{\text{out,L1}}$. Power balance between the input, Eq. (3.7), and the transferred power is as follows

$$P_{\text{in,avg}} = P_{\text{out,C}} + P_{\text{out,L1}} \tag{3.14}$$

Placing Eqs. (3.7), (3.11) and (3.13) into Eq (3.14) and reorganizing it, an equation for the bulk capacitor voltage during DCM operation of the flyback transformer is obtained. It is as follows

$$\frac{L_1}{L_M} V_C^2 + \left[\frac{N_1}{N_2} V_{\text{out}} \sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} \left(\frac{v_{\text{in},n}^2}{V_C + \frac{N_1}{N_2} V_{\text{out}} - \left| v_{in,n} \right|} \right) - \sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} v_{\text{in},n}^2 \left(1 + \frac{\left| v_{\text{in},n} \right|}{V_C + \frac{N_1}{N_2} V_{\text{out}} - \left| v_{\text{in},n} \right|} \right) \right] \times \frac{T_s}{T_{\text{line}}} = 0 \tag{3.15}$$

Eq. (3.15) indicates that the voltage over the bulk capacitor is only a function of parameters considered here as constants: the circuit parameters, the line voltage and the output voltage. Therefore, the steady state value of V_C is constant in DCM + DCM operation of the converter and the value depends on the load.

Power balance between the power consumed in load and the power transferred to the secondary, for an ideal converter, is as follows

$$\frac{V_{\text{out}}^2}{R_{\text{load}}} = P_{\text{out,C}} + P_{\text{out,L1}} \tag{3.16}$$

Eq. (3.16) gives power balance between consumption and injection. One can set the desired output voltage by calculating R_{load} which gives the desired output voltage

$$R_{load} = \frac{V_{out}^2}{P_{out,C} + P_{out,L1}} \tag{3.17}$$

3.1.4.3 CCM & DCM border

The border between CCM and DCM operation can be defined by comparing the load resistance R_{load} to a resistance called here as resistance R_S. The output stage of BIFRED operates in DCM if the actual load resistance is greater than the R_S. Vice versa, if the load is smaller than R_S the stage operates in CCM. R_S is the value of the load resistance when the output stage of BIFRED operates in the border of CCM and DCM operation. It can be deduced as follows:

$$\begin{aligned} R_S = \frac{V_{out}}{I_{out}} &= \left(\frac{V_{out}}{\frac{N_1}{N_2}\frac{I_{M,peak}}{2}(1-D_1) + \sum_{n=1}^{\frac{T_{line}}{T_S}} I_{refl,n}} \right) = \left(\frac{V_{out}}{\frac{N_1}{N_2}\frac{V_C D_1 T_s}{2L_M}(1-D_1) + \sum_{n=1}^{\frac{T_{line}}{T_S}} I_{refl,n}} \right) \\ &= \left(\frac{V_{out}}{\frac{N_1}{N_2}\left[\frac{N_1}{N_2} V_{out} \frac{(1-D_1)}{D_1}\right]\frac{D_1 T_s}{2L_M}(1-D_1) + \sum_{n=1}^{\frac{T_{line}}{T_S}} I_{refl,n}} \right) = \left(\frac{V_{out}}{\left(\frac{N_1}{N_2}\right)^2 \frac{V_{out} T_s}{2L_M}(1-D_1)^2 + \sum_{n=1}^{\frac{T_{line}}{T_S}} I_{refl,n}} \right) \end{aligned} \tag{3.18}$$

where I_{out} is the average current through the diode D_2 in the border of CCM and DCM operation of the flyback stage and $I_{refl,n}$ is calculated from Eq. (3.12). Eq. (3.18) is based on the fact that in the border of DCM and CCM operation the flyback transformer is completely demagnetized in time duration $(1\text{-}D_1)T_s$.

3.1.5 Calculated results

In Fig. 3.7 calculated results of an example of BIFRED are presented. Following values were used in the calculation of Fig. 3.7 a) and b) : T_{line} = 20 ms, T_s = 10 µs, L_1 = 250 µH, L_M = 450 µH, $V_{in,rms}$ = 260-140 V, $(N_1/N_2)\times V_{out}$ = 150 V and $(D_1 + D_{2,max}) \leq 1$ (Appendix A).

Calculation of Fig. 3.7 c) and d) have been done with the following values:

$D_1 + D_{2,\max} = 1$, $R_{\text{load}} < R_S$ and $V_{\text{in,rms}} = 230$ V.

The change from DCM + CCM operation to DCM + DCM operation can be seen clearly from Fig 3.7 a) and b). In the latter one the rise of the bulk capacitor voltage, DCM + CCM operation, ceases to a constant value when the converter enters to DCM + DCM operation. In the first one curves have a little knee when in the border of the two modes.

The input power curves of Fig. 3.7 clearly show that the available power from the utility grid decreases when the rms value of the line voltage decreases. It happens despite of the fact that the available range of duty ratio of the switch is enlarged at the same time. Consequently, BIFRED cannot be designed for universal input voltage, or it is not practical, if the correct operation mode of the converter is to be retained. Moreover, the bulk capacitor voltage curves show that the with $V_{\text{in,rms}} = 260$ V the voltage is barely below the 450 V limit and with $V_{\text{in,rms}} = 140$ V the bulk capacitor voltage, $V_C = 199.8$ V, is barely above the $V_{\text{in,peak}} = \sqrt{2} \times 140\,\text{V} \approx 197$ V. The 450 V limit is due the the fact that it is hard to find suitable eletrolytic capacitors for higher voltage ratings. Hence, in order to achieve the correct operation mode, it is required that $140\text{ V} < V_{\text{in,rms}} < 260$ V in this example.

In Fig. 3.7 c) and d) it is shown that, as the value of the inductance decreases, the available maximum power and peak current through the inductor increases rapidly. This means that, perhaps, the practical power range of this kind of converter lies somewhere under 500 W input power. Otherwise, even a few percent inaccuracy in value of the inductance increases or decreases the available power remarkably. On the other hand the peak current becomes relatively high for a low power equipment and this could lead to unacceptable losses in the switch, winding (skin and proximity effects) and core.

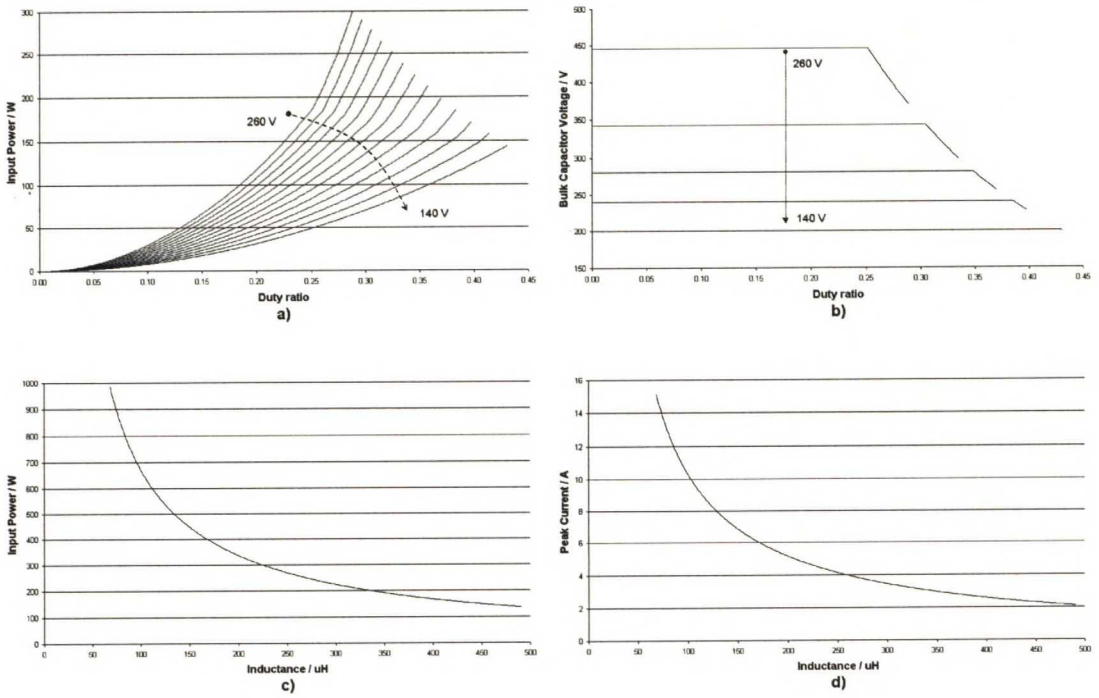

Figure 3.7 a) Calculated input power curves of BIFRED as a function of the duty cycle and line voltage as a parameter, ranging from $V_{in,rms}$ =260 V to 140 V with 10 V steps. b) Corresponding bulk capacitor voltage behavior for voltages $V_{in,rms}$ = 260, 210, 180, 160 and 140 V. c), d) Maximum input power, $V_{in,rms}$ = 230 V, and corresponding peak current as a function of inductance of the DCM-Boost inductor, respectively.

In the calculation of Fig 3.7 all the equations presented in this chapter were used. Bulk capacitor voltage in DCM + DCM operation was solved from Eq. (3.15) by iteration.

3.2 BIBRED

3.2.1 General

BIBRED stands for Boost Integrated with Buck Rectifier/Energy storage/Dc-dc converter /7/. The converter is shown in Fig. 3.8. BIBRED is quite similar to BIFRED. It is a combination of three parts: an EMI-filter, a DCM boost converter and a forward converter. BIBRED has only one switching stage and thus it is a single-stage solution, too. The input stage is almost identical with the one in BIFRED and consequently the analysis of it is very similar. The power factor correction is achieved by allowing the boost converter to operate in DCM. Duty ratio of the switch is used to adjust the output voltage to a desired level.

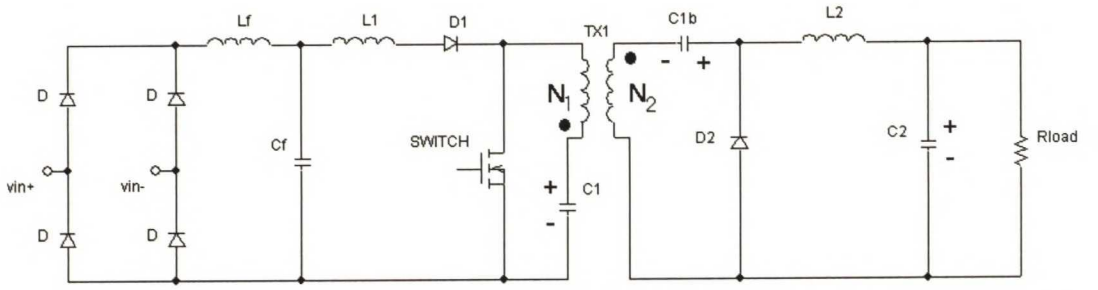

Figure 3.8 BIBRED /7/. L_f and C_f form the EMI-filter, L_1, D_1 and SWITCH form the DCM boost converter and SWITCH, C_1, transformer TX1 and the whole secondary form the forward converter.

The output stage is a little bit modified forward converter. One of the forward converter's output diodes is replaced by the capacitor C_{1b}.

3.2.2 Operation

BIBRED has two operation modes: the switch turned on or off. When the switch is on, the line voltage is applied across the DCM boost inductor. At the same time the bulk capacitor voltage V_C is applied across the primary winding of the transformer. Both the resulting currents, the line current and the transformer current, are circulating through the switch. The transformer current is reflected to the secondary, and the reflected current flows through the capacitor C_{1b}. Capacitors C_1 and C_{1b} are delivering power to the output inductor L_2, capacitor C_2 and the load when the switch is turned on. Voltage across the inductor L_2 during that time is

$$V_{L2} = \frac{N_2}{N_1} V_C + V_{C1b} - V_{out} \tag{3.19}$$

where V_{C1b} is voltage over the capacitor C_{1b}. The two capacitors, C_1 and C_{1b}, are actually in series during this time. This will be discussed later. The current paths when the switch is turned on are depicted in Fig. 3.9.

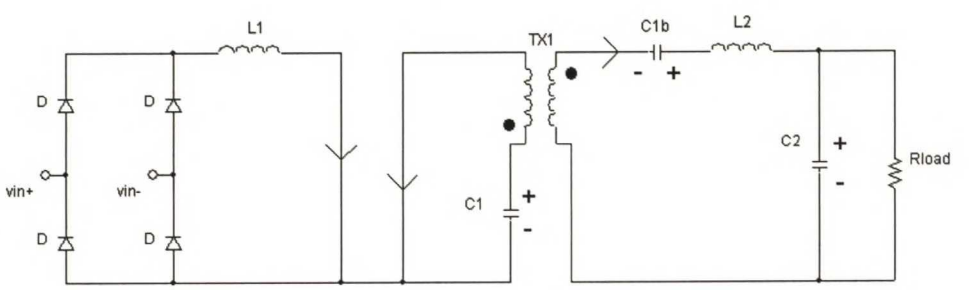

Figure 3.9 BIBRED, switch is turned on, EMI filter is omitted. The transformer current and the line current are both circulating through the switch. The current of the transformer is reflected to the secondary side and the output inductor L_2 is being energized.

When the switch is off the boost inductor L_1 is de-energized to the capacitor C_1 through the primary winding of the transformer. The voltage over the inductor L_2 reverses its polarity and it is fixed to the output voltage V_{out} because the diode D_2 becomes forward biased. The inductor begins to de-energize to the output capacitor C_2 and the load.

BIBRED has a hidden feature compared to a normal forward converter due to the presence of the capacitor C_{1b}. Usually a forward transformer is equipped with a third winding, de-magnetizing winding, which is needed to de-energize the magnetizing inductance of the transformer. In BIBRED application the magnetizing energy can be restored into the capacitor C_{1b} without additional components or a winding. After the switch was been turned off the magnetizing current is able to circulate a path closed by the forward biased diode D_2. Reflected boost inductor current can circulate through the same path as the magnetizing current. The two currents are charging the capacitor C_{1b}. The paths of the currents during the switch-off mode are depicted in Fig. 3.10.

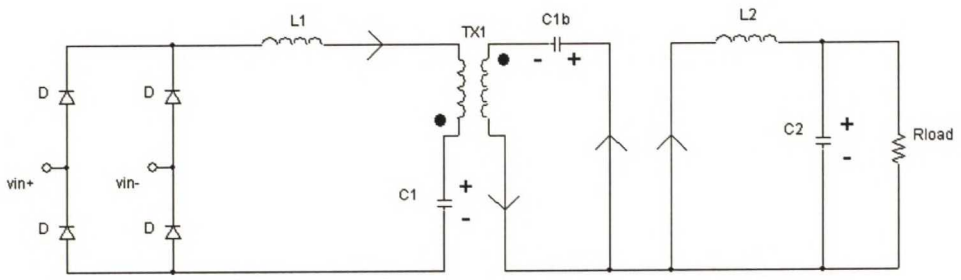

Figure 3.10 BIBRED, switch turned off, EMI filter is omitted. The boost inductor is de-energized completely to the capacitors C_1 and C_{1b}. Transformers magnetizing energy is restored to the capacitor C_{1b} through the diode D_2. The reflected boost inductor current circulates also through the diode D_2.

3.2.3 Input stage

BIBRED has the DCM boost converter as an input converter. DCM operation of the converter is crucial for BIBRED in order to achieve acceptable power factor correction. The operation of the input converter is almost identical with the one in BIFRED. The only difference of the operation of the input stages is in the reverse voltage in which the inductor is fixed right after the switch has been turned off. In BIFRED the voltage $V_{L,n}$ is presented in Eq. (3.4). In BIBRED the voltage $V_{L,n}$ is

$$V_{L,n} = v_{in,n} - \left(V_C + \frac{N_1}{N_2} V_{C1b} \right) \tag{3.20}$$

Careful look at the secondary side of BIBRED reveals that the capacitors C_{1b} and C_2 are the only 'DC components' present at the secondary. In other words, the inductor L_2 or the secondary winding of the transformer cannot store DC voltage in the steady state. Consequently, the capacitors C_2 and C_{1b} must share the same average voltage. The voltage over the capacitor C_2 is the output voltage, which addresses that the average voltage over the capacitor C_{1b} is the output voltage, too. Hence, Eq. (3.20) converts to a form identical with Eq. (3.4). The conclusion is that in the steady state the input stages of BIFRED and BIBRED operate identically. Equations (3.5), (3.6) and (3.7) are applicable for BIFRED as well as for BIBRED.

3.2.4 Output stage

The output stage of BIBRED is a forward type converter. As mentioned earlier, one of the output diodes is replaced by the capacitor C_{1b}. The replacement is done in order to offer a circulation path for the reflected boost inductor current. The capacitor C_{1b} and the diode D_2 form also an appropriate way to de-magnetize the forward transformer. The forward stage can operate either CCM or DCM. Because these two modes of operation differ from each other radically, they are considered separately.

3.2.4.1 CCM operation

In CCM operation the output voltage of the forward stage is strictly defined by the bulk capacitor voltage, turns ratio and duty ratio because the average volt-second balance across the inductor L_2 has to be equal to zero in steady state. The voltage over L_2 during the switch on time is presented in Eq. (3.19). When the switch is off, it equals to the output voltage V_{out}. Equating these two yield (V_{C1b} equals V_{out})

$$\begin{aligned} &\left(\frac{N_2}{N_1}V_C + V_{C1b} - V_{out}\right)D_1T_s = V_{out}(1-D_1)T_s \\ &\Rightarrow V_{out} = V_C\frac{N_2}{N_1}\frac{D_1}{1-D_1} \end{aligned} \qquad \textbf{(3.21)}$$

If the output voltage is regulated to a constant value, V_C has to be

$$V_C = V_{out}\frac{N_1}{N_2}\frac{1-D_1}{D_1} \qquad \textbf{(3.22)}$$

Equations (3.21) and (3.22) are identical with the corresponding ones, (3.8) and (3.9) of BIFRED. Since the input and output stages of the converters operate in an identical manner, the steady state analysis is the same for both the converters in DCM + CCM operation. The circuits look different but the equations ruling their behavior are exactly the same. The voltage over the bulk capacitor in BIBRED has the same pattern as BIFRED, depicted in Fig. 3.7 a).

3.2.4.2 DCM operation

In DCM operation the current through the output inductor L_2 reaches zero before the end of a switching cycle, which means that Equations (3.21) and (3.22) are not valid anymore. Therefore, the bulk capacitor voltage has to be determined from a power balance.

As mentioned earlier, BIFRED has two different ways to deliver power from the primary to the secondary: power supplied by the bulk capacitor C_1 and the power supplied by the boost inductor. BIBRED has three ways to deliver power from the primary to the secondary. The first two ways are the same as in BIFRED. De-magnetizing of the forward transformer can be comprehended as power delivering as well as the two other ones. These three ways to deliver power are discussed below.

The power supplied by the bulk capacitor is as follows

$$P_{\text{out,C}} = V_{\text{C}}\left[\left(\frac{N_2}{N_1}\right)\frac{I_{\text{L2,peak}}}{2}\right]D_1 = V_{\text{C}}\left[\left(\frac{N_2}{N_1}\right)\frac{\left(\left(\frac{N_2}{N_1}\right)V_{\text{C}} + V_{\text{C1b}} - V_{\text{out}}\right)D_1 T_{\text{s}}}{2L_2}\right]D_1 \qquad \textbf{(3.23)}$$

$$= \left(\frac{N_2}{N_1}\right)^2 \frac{V_{\text{C}}^2 D_1^2 T_{\text{s}}}{2L_2}$$

where $I_{\text{L2,peak}}$ is the peak current through the inductor L_2. The reflected transformer current $I_{\text{refl},n}$ calculated in section 3.1.5 can be calculated for BIBRED with same equation, Eq (3.12). The current has the same magnitude and power content in both cases but the circulating route is different. In BIFRED the current is flowing directly into the load and the output capacitor. In BIBRED the current charges the capacitor C_{1b} and the energy is not delivered to the actual output. However, the main point is that

power *is* delivered from the primary side to the secondary side and Eq. (3.13) is applicable in BIBRED to calculation of $P_{\text{out,L1}}$ as well.

Power delivered by the magnetizing inductance of the transformer is as follows

$$P_{\text{M}} = \frac{V_{\text{C}}^2 D_1^2 T_{\text{s}}}{2L_{\text{M}}} \tag{3.24}$$

Notice the similarity of Eq. (3.24) with Eq. (3.11)

Power balance between the input power and the power injected from the primary to the secondary is as follows

$$P_{\text{in,avg}} = P_{\text{out,C}} + P_{\text{out,L1}} + P_{\text{M}} \tag{3.25}$$

where $P_{\text{in,avg}}$ is calculated from Eg. (3.7) and $P_{\text{out,L1}}$ is calculated from Eq (3.13). By placing the variables in Eq. (3.25) and reorganizing it, an equation for the determination of the bulk capacitor voltage in DCM operation of BIBRED's output stage can be obtained. It is as follows:

$$\left[\frac{L_1}{L_{\text{M}}} + \left(\frac{N_2}{N_1}\right)^2 \frac{L_1}{L_2}\right] V_{\text{C}}^2 + \left[\frac{N_1}{N_2} V_{\text{out}} \sum_{n=1}^{\frac{T_{\text{line}}}{T_{\text{s}}}} \left(\frac{v_{\text{in},n}^2}{V_{\text{C}} + \frac{N_1}{N_2} V_{\text{out}} - |v_{\text{in},n}|}\right) - \sum_{n=1}^{\frac{T_{\text{line}}}{T_{\text{s}}}} v_{\text{in},n}^2 \left(1 + \frac{|v_{\text{in},n}|}{V_{\text{C}} + \frac{N_1}{N_2} V_{\text{out}} - |v_{\text{in},n}|}\right)\right] \times \frac{T_{\text{s}}}{T_{\text{line}}} = 0 \tag{3.26}$$

Eq. (3.26) shows clearly that the voltage over the bulk capacitor does not depend on the load or duty cycle but it is defined by the circuit parameters, the line voltage and output voltage. Therefore, the voltage is constant in DCM operation of the output stage of BIBRED.

Power balance between the power consumed in the load and the power injected to the secondary, for an ideal converter, is as follows

$$P_{\text{out,C}} + P_{\text{out,L1}} + P_{\text{M}} = \frac{V_{\text{out}}^2}{R_{\text{load}}} \tag{3.27}$$

Reorganizing Eq. (3.27) it is possible to obtain the value of the load resistance, which corresponds with the desired output voltage

$$R_{\text{load}} = \frac{V_{\text{out}}^2}{P_{C1,\text{out}} + P_{\text{out,L1}} + P_{\text{M}}} \tag{3.28}$$

3.2.4.3 CCM & DCM border

The border between CCM and DCM operation is determined by comparing the actual load resistance R_{load} to the resistance R_{S}. R_{S} is for BIBRED as follows

$$R_{\text{S}} = \frac{V_{\text{out}}}{I_{\text{out}}} = \frac{V_{\text{out}}}{\left(\frac{I_{M,peak}}{2}\right)} = \frac{V_{\text{out}}}{\left(\frac{V_{\text{out}}(1-D_1)T_{\text{s}}}{2L_2}\right)} \frac{2L_2}{(1-D_1)T_{\text{s}}} \tag{3.29}$$

where L_2 is the inductance of the output inductor L_2. The output stage of BIBRED operates in DCM if the load resistance is greater than the R_{S}. Vice versa, if the load resistance is smaller than R_{S} the converter operates in CCM. Eq. (3.29) is based on the fact that the inductor L_2 is completely demagnetized in time duration $(1\text{-}D_1)T_{\text{s}}$.

3.3 Modified Dither

3.3.1 General

Modified dither is an advanced Buck-Boost type single-stage converter, /8/. The schematic of the converter is shown in Fig. 3.11. The converter is clearly a single-stage solution because it has only one switching stage. Its ancestor, the regular dither converter has a problem with excessive voltage rise over the DC-energy storage element C_1 during light loads. Modified dither has, at least, a partial solution for the problem. The converter has a tapped transformer, which is for prevention of the excessive voltage rise over the bulk capacitor. Diodes in the rectifier bridge are able to conduct when the line voltage is larger than a voltage imposed by the bulk capacitor to the lower part of the primary winding (N_{1B}) of the transformer. When the bulk capacitor voltage rises due to a reduced load, the imposed voltage rises, too. Consequently, input power is reduced not only by the reduction of the duty cycle but also by the shortened conduction time of the bridge diodes.

By allowing DCM operation of the inductor L_1 proper power factor correction is attained.

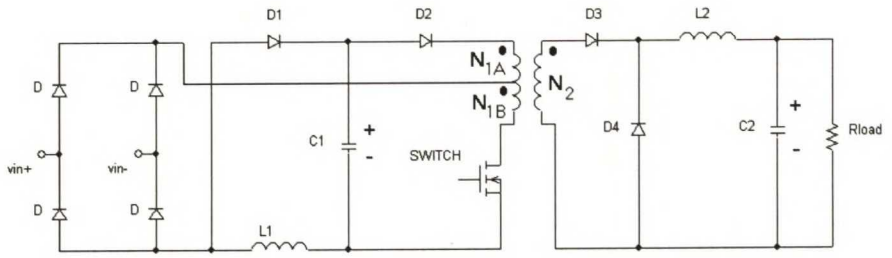

Figure 3.11 Modified dither converter /8/.

In single-stage converters like BIFRED or BIBRED the bulk capacitor voltage cannot fall below the peak line voltage. In Modified dither the diode D_2 prevents the bulk capacitor from becoming automatically charged to the peak line voltage and the voltage can be considerably lower than in BIFRED or BIBRED. The converter suffers from the voltage rise during light loads but due to the low initial value it has 'space' to rise. Therefore, the converter can be designed to operate in DCM + CCM operation over a wide range of loads without exceeding the 450 V limit of the bulk capacitor voltage. Therefore, only the DCM + CCM operation of the converter is included in the analysis.

3.3.2 Operation

The converter has two operation modes: the switch turned or off. When the switch is turned on, the bulk capacitor voltage is applied across the primary winding of the transformer. Since the transformer is tapped, the line voltage confronts an imposed voltage across the lower part of the primary winding N_{1B}. When instantaneous line voltage is below the imposed voltage, the diodes in the bridge are not able to conduct and no power is delivered from the utility grid to the circuit. Paths of the currents during the switch-on mode, when the instantaneous line voltage is less than the voltage across the N_{1B}, are shown in Fig. 3.12.

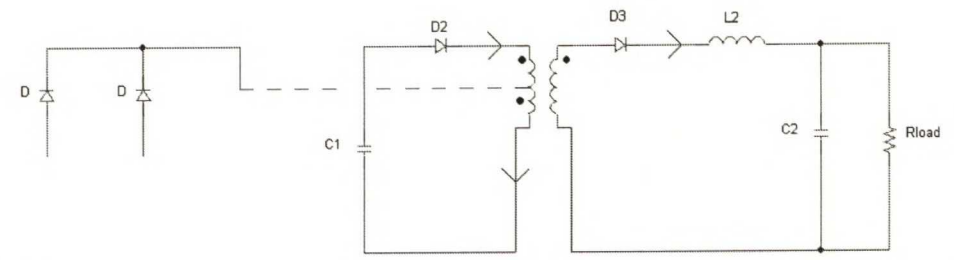

Figure 3.12 Modified dither, the switch is on and the instantaneous line voltage is less than the voltage across the N_{1B}. Diodes in the rectifier bridge are not able to conduct and power flow to the circuit is disabled. The bulk capacitor is supplying power to the secondary.

As the line voltage finally reaches the imposed voltage the diodes in the bridge are able to conduct and power flow from the utility grid to the converter is enabled. Paths of the currents during the mode are shown in Fig. 3.13. Line current energizes the inductor L_1 and the bulk capacitor and a fragment of the line voltage are feeding the secondary. One interesting thing during the operation mode is the current through the forward biased diode D_2. The main portion of the current is the one supplied by the bulk capacitor. However, a look at the transformer and the winding arrangements reveal that the line current causes a reflected current, which flows through the diode to the 'wrong' direction. The current through the diode is the difference between the bulk capacitor current and the reflected current.

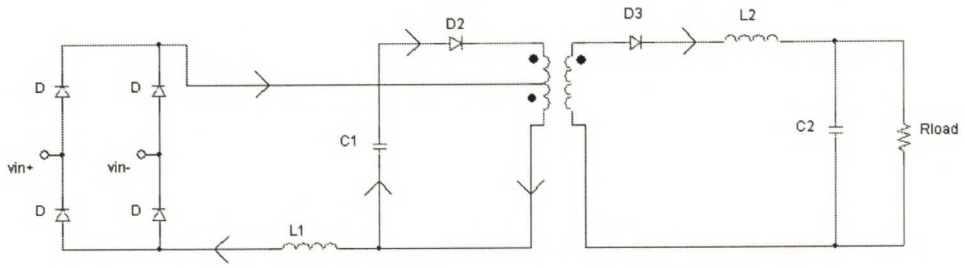

Figure 3.13. Modified dither switch turned on. Instantaneous line voltage is greater than the voltage over N_{1B} and the diodes in the bridge are able to conduct.

When the switch is turned off, the line current and the bulk capacitor current are cut off. Inductors L_1 and L_2 reverse their polarity and they are fixed to voltage level equal to the V_C and V_{out} respectively. L_1 is de-energized to the bulk capacitor completely and L_2 is de-energized partly or completely, depending on the output stage's operation mode (CCM or DCM), to the output capacitor C_2 and the load. Paths of the currents during the switch-off mode are depicted in Fig. 3.14.

Transformer of the converter is forward type. The magnetizing inductance of the transformer has to be de-energized during the switch off time. By adding a third winding to the transformer it is possible to demagnetize the inductance and restore the energy.

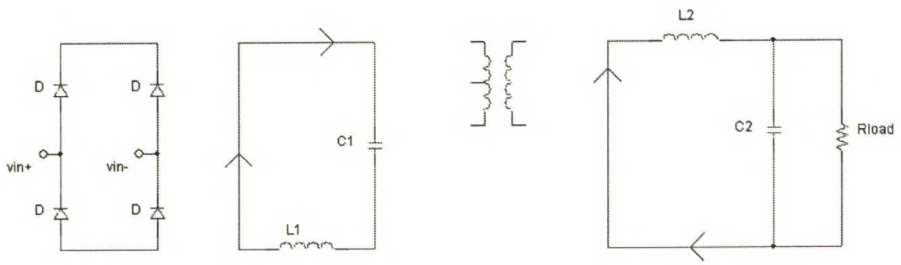

Figure 3.14. Modified dither during the switch-off time. L_1 is completely de-energized to the bulk capacitor. L_2 is partly or completely de-energized to the load and capacitor C_2.

3.3.3 Input stage

Modified Dither has a buck-boost type input stage. The converter has only one degree of freedom due to a single switching device. The degree of freedom has to be used either to adjust the output voltage or to build a proper power factor. Like in BIFRED and BIBRED, the duty ratio of the switch is used to adjust the output voltage and power factor correction is dealt with the DCM operation of the inductor L_1. As mentioned earlier, power flow to the converter is enabled only when the following is true

$$\left|v_{\text{in},n}\right| > V_{\text{C}} \frac{N_{1\text{B}}}{N_{1\text{A}} + N_{1\text{B}}} \tag{3.30}$$

where $N_{1\text{B}}$ and $N_{1\text{A}}$ are the numbers of turns in the lower and upper part of the primary winding respectively. Consequently, $N_1 = N_{1\text{A}} + N_{1\text{B}}$ is the total amount of turns in the whole primary winding.

Line current of Modified Dither consist of a sequence of triangular pulses. The current is depicted in Fig. 3.15. Height of the current pulse can be calculated as follows

$$I_{\text{L,peak},n} = \frac{\left(\left|v_{\text{in},n}\right| - V_{\text{C}} \frac{N_{1\text{B}}}{N_{1\text{A}} + N_{1\text{B}}}\right) D_1 T_{\text{s}}}{L_1} \tag{3.31}$$

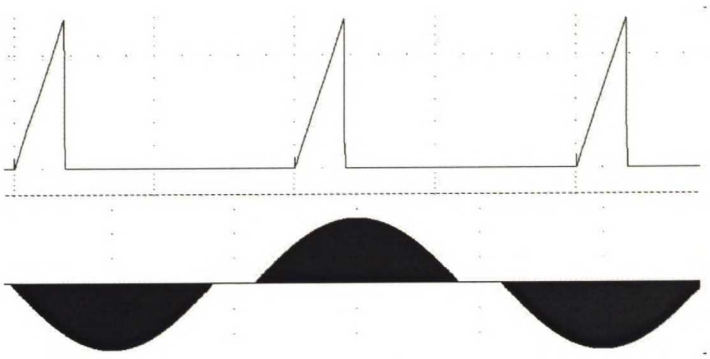

Figure 3.15 Line current of Modified Dither converter. Three single pulses above and the envelope of the current during one and a half line cycle below. Gaps in the envelope waveform is due to the low line voltage and consequent inability to deliver power to the circuit.

The inductor L_1 is energized by a voltage difference between the line voltage and the voltage imposed across the winding N_{1B}. Average power transferred to the circuit by a pulse is as follows

$$P_{\text{pulse},n} = |v_{\text{in},n}| I_{\text{avg},n} = |v_{\text{in},n}| \frac{I_{\text{L,peak},n}}{2} D_1 = \frac{|v_{\text{in},n}| \left(|v_{\text{in},n}| - V \frac{N_{1B}}{N_{1A}+N_{1B}} \right) D_1^2 T_s}{2L_1} \tag{3.32}$$

Notice that $P_{\text{pulse},n}$ is not the average power stored in the inductor L_1 during a switching cycle. It is the average power brought to the circuit during the n:th switching cycle.

More interesting than power carried by a pulse is the average power brought to the circuit during one line cycle. By summing power transferred by the pulses during the line cycle and dividing the sum by the amount of pulses, average input power is obtained. It is as follows

$$P_{\text{in,avg}} = \frac{D_1^2 T_s}{2L_1} \times \left(\sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} v_{\text{in},n}^2 - V_C \frac{N_{1B}}{N_{1A}+N_{1B}} \sum_{n=1}^{\frac{T_{\text{line}}}{T_s}} |v_{\text{in},n}| \right) \times \frac{T_s}{T_{\text{line}}} \tag{3.33}$$

The relative portion of the switching cycle when the inductor current is decreasing to zero is as follows

$$D_{2,n} = \left[\frac{|v_{\text{in},n}|}{V_C} - \frac{N_{1B}}{N_{1A}+N_{1B}} \right] D_1 \tag{3.34}$$

3.3.4 Output stage

The output stage can operate either in CCM or DCM. Resistance R_S determines the border between DCM and CCM operation of the output stage of Modified Dither. It is as follows

$$R_S = \frac{2L_2}{(1-D_1)T_s} \tag{3.35}$$

When the actual load resistance is larger than the R_S, the stage operates in DCM, and on the other hand if it is smaller than the R_S the stage operates in CCM.

In CCM the output voltage of a forward converter is strictly defined by the duty ratio, turns ratio and the input voltage of the forward stage. In CCM operation the output voltage is as follows

$$\begin{aligned} &\left(\frac{N_2}{N_1}V_C - V_{out}\right)D_1T_s = V_{out}(1-D_1)T_s \\ &\Rightarrow V_{out} = V_C\frac{N_2}{N_1}D_1 = V_C\frac{N_2}{N_{1A}+N_{1B}}D_1 \end{aligned} \tag{3.36}$$

Power balance between the power drawn from the utility grid and the power consumed in the load is as follows

$$\frac{D_1^2T_s}{2L_1}\times\left(\sum_{n=1}^{\frac{T_{line}}{T_s}}v_{in,n}^2 - V_C\frac{N_{1B}}{N_1}\sum_{n=1}^{\frac{T_{line}}{T_s}}|v_{in,n}|\right)\times\frac{T_s}{T_{line}} = \frac{\left(V_C\frac{N_2}{N_1}D_1\right)^2}{R_{load}} \tag{3.37}$$

Eq. (3.37) is a second degree function of the bulk capacitor voltage V_C. Reorganizing the equation yields an explicit equation for the bulk capacitor voltage. V_C is as follows

$$V_C = \frac{T_sR_{load}}{4L_1}\frac{N_{1B}N_1}{N_2^2}\sum_{n=1}^{\frac{T_{line}}{T_s}}v_{in,n}\times\frac{T_s}{T_{line}}\left[-1+\sqrt{1+\frac{8L_1}{T_sR_{load}}\left(\frac{N_2}{N_{1B}}\right)^2\frac{\sum_{n=1}^{\frac{T_{line}}{T_s}}v_{in,n}^2}{\sum_{n=1}^{\frac{T_{line}}{T_s}}|v_{in,n}|}\times\frac{T_{line}}{T_s}}\right] \tag{3.38}$$

Eq. (3.38) is only a function of the load resistance and it provides the bulk capacitor voltage in DCM + CCM operation of the converter for any load. Once the value of the

voltage is calculated from the equation one has to adjust the duty ratio D_1 in Eq (3.36) to correspond the desired output voltage, and the steady state operation point has been found for an ideal Modified Dither.

In /8/ it is shown that the bulk capacitor voltage begins to decrease when the output stage of the converter enters to DCM operation.

3.3.5 Calculated and simulated results

Calculated and simulated results of the Modified Dither converter are presented in Fig. 3.16. Following values were used in the calculation of this example:

$$T_{\text{line}} = 20\text{ms}, T_s = 10\mu\text{s}, L_1 = 150\mu\text{H}, L_2 = 1500\mu\text{H}, V_{\text{in,rms}} = 140 - 280\text{V}, V_{\text{out}} = 60\text{V}$$

$$\frac{N_{1A}}{N_{1B}} = 2, \frac{N_2}{N_{1A}} = 2.5, \frac{N_2}{N_{1B}} = 5, D_1 + D_{2,\max} \leq 1 \text{ and } R_{\text{load}} \leq R_S$$

Following values were used in the calculation of Fig. 3.16 c) and d):

$$D_1 + D_{2,\max} = 1,\ R_{\text{load}} < R_S \text{ and } V_{\text{in,rms}} = 230\text{V}$$

The input power curves show that, like in BIFRED, the available input power decreases when the rms value of the line voltage decreases. This means that the Modified Dither converter is not suitable for universal input voltage equipment if the correct operation of the converter is to be retained. The bulk capacitor voltage curve shows that the voltage can have very low values compared to the voltage of BIFRED or BIBRED and this gives the Modified Dither a certain advantage. The output stage can be designed to operate in CCM in a wide range of loads. Consequently, the current stresses and high frequency noise is less in the output stage of the converter than in BIFRED or BIBRED. Simulated points in Fig.3.16 b) verify the calculated results.

Fig. 3.16 c) shows the available power and the peak current through the inductor of Modified Dither as a function of inductance L_1. Clearly, the available power is less than for BIFRED with the same inductance value. Also for the same input power the peak current, Fig. 3.16 d), through the inductor is remarkably higher in Modified Dither than in BIFRED. This indicates that the practical power range, perhaps < 200W, is lower for the Modified Dither than for the BIFRED.

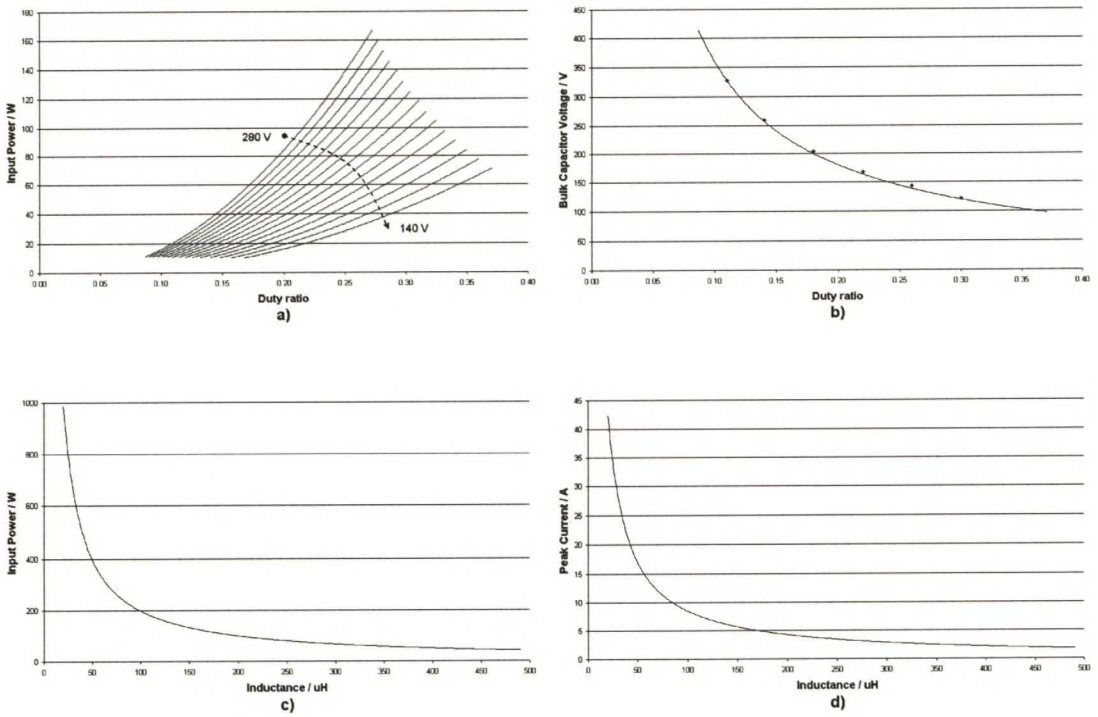

Fig. 3.16. a) Input power in DCM + CCM operation as a function of duty ratio and input voltage as a parameter, ranging from $V_{in,rms}$ = 280 to 140 V with 10 V steps. b) Corresponding calculated behavior of the bulk capacitor voltage and six simulated points. c) and d) Maximum input power and corresponding peak current as a function of inductance of the DCM inductor.

3.4 Brief summary of the topologies

Steady state analysis of the three single-stage converters was presented. BIFRED and BIBRED can be designed for larger power level than Modified Dither with the same peak current rating, Figs. 3.7 and 3.16. However, BIFRED's and BIBRED's output stage have to be designed on the edge of DCM operation in order to avoid excessive voltage rise over the bulk capacitor. On the other hand, Modified Dither's output stage can be designed to operate in CCM over a wide range of loads which is a certain advantage for the topology.

BIFRED has only two large magnetic components: the DCM boost inductor and the flyback transformer. BIBRED and Modified Dither have three: DCM inductor, forward transformer and the output inductor L_2. Therefore, for a 200 W low cost power supply, BIFRED seemed to be to the best choice.

4 Practical design of BIFRED

A prototype of BIFRED was built for the thesis. Necessary design considerations to construct a BIFRED are given in this chapter. The most troublesome parts of the converter were the magnetic components: the DCM boost inductor and the flyback transformer. It was difficult to find suitable magnetic components from the catalogs for this specific application. Consequently, they had to be designed and constructed. In the prototype Philips's ETD-49 3F3 ferrite cores were applied and 100 kHz switching frequency used. The core type and switching frequency mentioned above are used to illustrate the design procedure in the examples of this chapter.

The value of the boost inductance affects the available input power. For a certain power level the estimate of the needed inductance can be read from Fig. 3.7 c) or it can be calculated from Eq. (3.7). The value of the flyback transformer's magnetizing inductance affects to the resistance R_S, Eq. (3.18). The higher the value of the inductance, the longer the DCM + CCM operation of the converter, and the higher the resulting bulk capacitor voltage at light loads. The voltage can be determined from Eq. (3.15).

Design of the DCM boost inductor is discussed in Section 4.1. The design guidelines for the flyback transformer are given in Section 4.2. The effect of the leakage inductance of the transformer is considered in Section 4.3 and a solution is proposed to prevent the imminent problem.

4.1 DCM Boost Inductance

4.1.1 General

The general current waveform through the DCM-Boost inductor of BIFRED is depicted in Fig. 3.5. Due to DCM operation of the inductor, the peak value of a current pulse is substantially higher than the average value of the current ($I_{L,peak,n} \geq 2*I_{L,avg,n}$) and consequently it carries a considerably amount of high frequency current harmonics. The magnetic flux is swinging in the inductor's core from zero value to a substantially high peak value at the switching frequency. Resulting power dissipation and imminent threat

of saturation at the vicinity of peak line voltage may cause problems even at low power levels. The peak value of flux is

$$\Phi_{\text{peak}} = \frac{NI_{\text{L,peak}} A_c \mu}{l_m} \tag{4.1}$$

where μ is permeability of the core, A_c cross sectional area of the core and l_m length of the magnetic path. Core losses and saturation are discussed in sections 4.1.2 and 4.1.3 respectively.

In the winding design, because of the abundant high frequency content of the current, the skin and the proximity effect should be considered. Skin effect and the associated penetration depth describes an ability of a current component to utilize the conductor's cross section area. The proximity effect is a result from multi layer winding construction, in which the adjacent layers disturb conduction in the others. Both of these phenomena increase the *effective resistance* of the conductor and they play a key role in the conductor loss calculations. Winding arrangements are discussed in sections 4.1.4 and 4.1.5.

Losses in the winding and core cause temperature rise in the inductor. The cooling method most often used for SMPS application is free air cooling. In section 4.1.6 the effect of losses in the design procedure of the inductor is discussed.

It is more or less obvious that one has to use gapped ferrite cores to avoid saturation and restrain the loss in the core below a reasonable limit. Introducing an air gap to a magnetic path effectively prevents core saturation and reduces losses in the core due to a reduced value of the magnetic flux.

4.1.2 Losses in the core

Magnetic losses in a core depend on the flux density, switching frequency and material. A loss graph for the 3F3 ferrite material is given in the Philips catalog /9, pp.119/, reprinted in Fig. 4.1. Core loss is reported as a function of peak flux density and switching frequency as a parameter. However, this kind of a graph is difficult to use for exact loss determination when the feeding voltage waveform is not DC and the

consecutive current pulses does not share the same peak value. That is the case with the DCM boost inductor in a BIFRED application, Fig. 3.5.

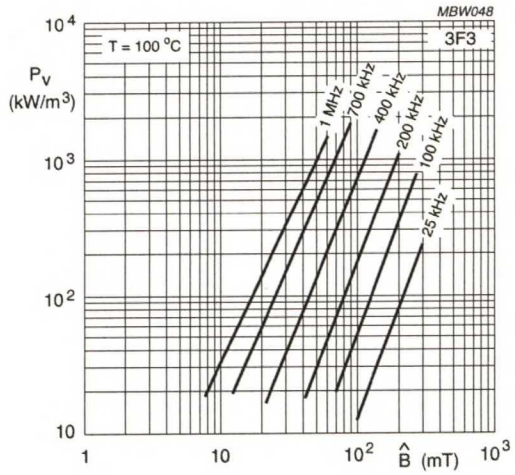

Figure 4.1 Specific power loss density of 3F3 ferrite grade as a function of peak flux density with a frequency as a parameter, /9, pp. 119/.

Loss density in a ferrite, at a constant switching frequency, follows a relationship /10/ presented below

$$\frac{P_h}{V} = a \times B^x \tag{4.2}$$

where a and x are constants, B flux density, V volume of the core and P_h loss in the core material. For example, for a loss density equation at 100 kHz switching frequency two clearly seen points from the 100 kHz curve of Fig 4.1 are needed to solve the a and x. Here points $(B, P_{h/V})$

$$\left(70\text{mT}, 20\frac{\text{kW}}{\text{m}^3}\right) \text{and} \left(90\text{mT}, 40\frac{\text{kW}}{\text{m}^3}\right)$$

are chosen. Resulting loss density equation for the 3F3 material at 100 kHz switching frequency is as follows

$$\frac{P_h}{V} = 163 \times 10^{-6} B^{2,758} \frac{\text{kW}}{\text{m}^3} \tag{4.3}$$

where flux density is in mT.

Next step is to determine the flux and flux density in a gapped core. In Fig. 3.1 it is shown that the current in the DCM-boost inductor rises from zero to the peak value and then back to zero. The loss in the core material is determined by the peak flux density

and therefore the determination of the loss in the DCM boost inductor is a straightforward task. Equation for the peak flux as a function of the peak current in a gapped core /11, pp. 140/ is as follows

$$\Phi_{\text{peak},n} = \frac{\mu_0 N I_{\text{L,peak},n}}{\frac{l_g}{A_g} + \frac{l_e - l_g}{\mu A_e}} = \frac{\mu_0 N}{\frac{l_g}{A_g} + \frac{l_e - l_g}{\mu A_e}} \times \frac{|v_{\text{in},n}| D_1 T_s}{L_1} \tag{4.4}$$

where $I_{\text{L,peak},n}$ is determined by Eq. (3.2), μ_0 is the permeability of air, l_g length of the air gap, l_e effective length of the magnetic path, A_g cross section area of the air gap and A_e effective cross section area of the core.

The peak flux density is obtained by dividing Eq. (4.4) by the cross section area of the core. The worst case is obtained by using the minimum core area A_{min}. Peak flux density is as follows

$$B_{\text{peak},n} = \frac{\mu_0 N}{\frac{l_g}{A_g} + \frac{l_e - l_g}{\mu A_e}} \times \frac{|v_{\text{in},n}| D_1 T_s}{L_1} \times \frac{1}{A_{\text{min}}} \tag{4.5}$$

However, if a relatively large air gap is introduced to a magnetic path, the unavoidable fringing flux will reduce the reluctance of the air gap compared to the ideal situation. The fringing flux expands itself to a larger area than the cross section area of the center limb of the core and the resulting reluctance of the magnetic path is reduced. The fringing flux around an air gap is illustrated in Fig. 4.2, /12/.

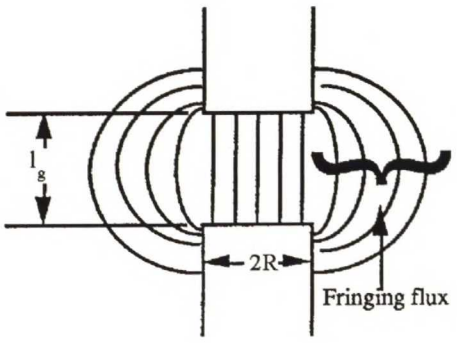

Figure 4.2 Fringing flux around an air gap /12/.

Obviously, with some air gap length, the reduced reluctance of the air gap causes an unacceptable error to the calculation and it should be taken into account. Correction term for the *effective radius* of an air gap is presented in /11, pp. 141/. It is as follows

$$\Delta R = \left(0.241 + \frac{1}{\pi} \log\left(\frac{b_a}{l_g}\right) \right) \times l_g \tag{4.6}$$

where b_a is the total inside length of the limb containing the air gap (e.g. width of the winding space for most of the core types) and ΔR is added to the radius R of the center limb of the core and. Eq. (4.6) should be quite accurate when the ratio b_a/l_g is greater than five and l_g much less than the width of the air gap ($2R$). The effective air gap area is as follows

$$A_{g,e} = \pi(R + \Delta R)^2 \tag{4.7}$$

where R is the radius of the center limb of the core. By replacing A_g in Eq. (4.5) with $A_{g,e}$ it is possible to take the fringing flux into account and achieve a more accurate equation for the peak flux density.

Losses in a gapped 3F3-ferrite core at 100 kHz switching frequency are now determined by Eqs. (4.3) and (4.5). The average loss is obtained by summing the loss generated within every switching cycle during the line cycle and dividing the sum by the number of switching cycles. Average (relative) core loss equation for the 3F3 material is as follows.

$$P_{h/V} = 163 \times 10^{-6} \left(\frac{\mu_0 N}{\frac{l_g}{A_{g,e}} + \frac{l_e - l_g}{\mu A_e}} \times \frac{D_1 T_s}{L_1} \times \frac{1}{A_{min}} \times \sum_{n=1}^{\frac{T_{line}}{T_s}} \left| v_{in,n} \right| \right)^{2.758} \times \frac{T_s}{T_{line}} \frac{kW}{m^3} \tag{4.8}$$

Absolute loss is obtained by multiplying the relative loss by the volume of the core.

4.1.3 Core saturation

Maximum peak flux density is obtained from Eq. (4.5) by placing $v_{in,n} = V_{in,peak}$ and using some maximum value for the duty ratio D_1 (e.g. under worst possible conditions). The $A_{g,e}$ determined in Eq. (4.7) should be used instead of the A_g because the reduced reluctance increases the flux and the flux density. The value of the peak flux density

should be lower than the saturation value read from the manufacturers specific graph, shown for the 3F3 material in Fig. 4.3, /9, pp. 118/.

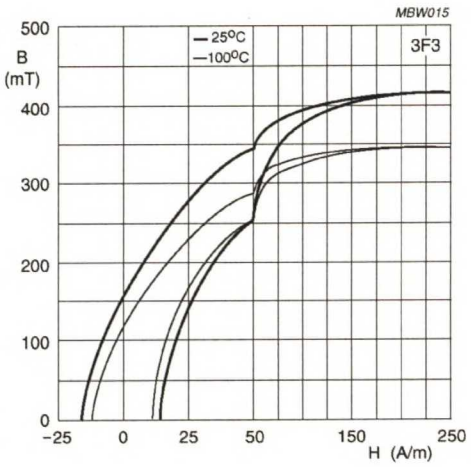

Figure 4.3 Typical B-H loops for 3F3 material, /9, pp. 118/.

4.1.4 Number of turns

Next task is to find out, how many turns are needed for the desired inductance. The link between the inductance and magnetic flux is as follows /11, pp. 139/

$$L = \frac{N\Phi_{\text{peak},n}}{I_{\text{L,peak},n}} \tag{4.9}$$

Substituting $\Phi_{\text{peak},n}$ from Eq (4.4) yields

$$L = \frac{\mu_0 N^2}{\frac{l_g}{A_{g,e}} + \frac{l_e - l_g}{\mu A_e}} \tag{4.10}$$

Since the value of the desired inductance is known, but the number of turns is not, one has to reorganize Eq. (4.10) in order to get an equation for the number of turns.

$$N = \sqrt{L\left(\frac{l_g}{\mu_0 A_{g,e}} + \frac{l_e - l_g}{\mu_0 \mu A_e}\right)} \tag{4.11}$$

4.1.5 Winding

Eq. (4.11) gives the number of turns for the desired inductance. By adjusting the air gap, it is theoretically possible to have as many or as few turns as one may want. Therefore,

it is good practice to calculate the number of turns, average loss in the core and check possible saturation problems for several different air gap lengths. In Fig. 4.4 ETD-49 bobbin, /9, pp. 411/, is reprinted.

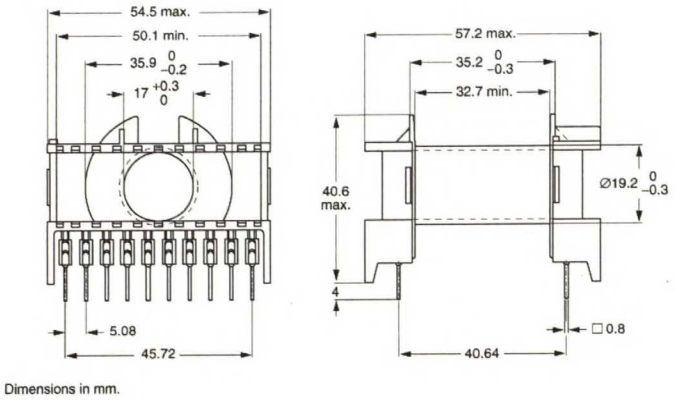

Figure 4.4 ETD-49 core bobbin, /9, pp. 411/.

Once the satisfying l_g, N and core loss combination is found one has to determine the loss in the winding.

By dividing the minimum winding breadth $b_{w,min}$ by the number of the turns N, the maximum wire diameter (with insulation of the wire) for a one layer construction is obtained. In Fig. 4.4 $b_{w,min}$ is 32.7 mm. In a multi-layer case it is good practice to compose the layers with equal (or close to equal) number of turns. Of course it would be more attractive to design a single layer inductor but usually quite a thin wire has to be used. DCM boost inductor carries high rms current compared to the fundamental and one has to check also if the wire with a certain cross section area is capable to carry the needed current.

In a high frequency inductor or transformer the conduction loss in a winding is affected by the skin and proximity effect. In that case the DC-resistance, associated to a conductor, is not enough in the calculation of conduction losses.

The Dowell analysis /11, pp.327 - 330/ is often referred to in the literature in winding loss determination. The analysis returns a resistance factor F_r, which points out how much the DC-resistance of the winding increases due to the skin and proximity effects. The Dowell graph is shown in Fig. 4.5.

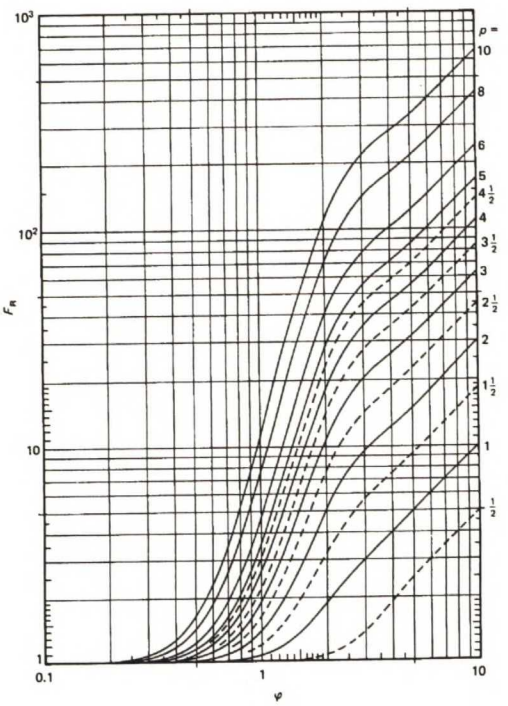

Figure 4.5 The Dowell graph /11, pp. 327 - 330 /.

For the graph, a special parameter φ has to be defined:

$$\varphi = \frac{h\sqrt{F_1}}{\Delta} \tag{4.12}$$

where Δ is the penetration depth, F_1 filling factor and h effective conductor height. The factors are explained below.

Penetration depth:

$$\Delta = \sqrt{\frac{\rho_c}{\pi \mu_0 \mu_c f}} \tag{4.13}$$

where ρ_c is the conductivity of the conductor material. Usually penetration depth is calculated for the maximum temperature condition.

Filling factor:

$$F_1 = \frac{Nb}{b_w} \tag{4.14}$$

Parameters of Eq. (4.14) and h from Eq (4.12) are depicted in Fig. 4.6.

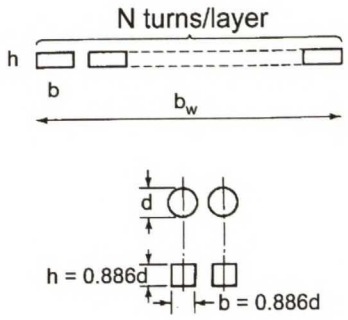

Figure 4.6 h is effective conductor height of a round conductor, b is the breadth of the conductor (without insulation) and b_w is the winding breadth, /11, pp. 327 - 330/.

The resistance factor F_r is determined from the Dowell graph with parameters φ and the number of layers p. By multiplying the DC-resistance of the conductor by the factor F_r, a more accurate and truthful resistance for the conduction loss calculation is attained.

As mentioned in section 4.1.1, the current through the inductor has abundant frequency content. For accurate conduction loss calculation, one should determine the resistance factor for each current component separately and calculate the loss as follows

$$P_h = R_{DC}\left(I_{DC}^2 + F_{r,100Hz} I_{100Hz}^2 + \ldots + F_{r,100kHz} I_{100kHz}^2 + \sum F_{r,f} I_f^2 \right) \qquad \textbf{(4.15)}$$

where R_{DC} is the DC-resistance of the conductor, I_{DC} DC-component of the current and $F_{r,100Hz}$ the resistance factor at 100 Hz. It is not necessarily a difficult task to solve Eq. (4.15) but a frustrating one and therefore it is good to employ some sort of approximation to carry out the calculation. One method is to calculate the loss energy caused by a single triangular current pulse using the corrected DC-resistance. In the method, the resistance factor F_r is calculated for the switching frequency and therefore it is accurate only for that frequency component. However, the current carries prominent DC and 100 Hz components and the corrected DC-resistance naturally gives too high value of the loss for the low frequency components. On the other, hand the current carries components over f_s with noteworthy amplitudes and the loss is naturally low for these. The idea behind the method is that the surplus and the lack of losses compensate each other and the result is a fair and good approximation for the winding loss.

Power loss in the conductor, caused by a triangular current pulse, is approximately as follows

$$P_{\mathrm{h},n} \approx F_{\mathrm{r},fs} R_{DC} \left[\int_0^{D_1 T_s} \left(I_{\mathrm{L,peak},n} \frac{t}{D_1 T_s} \right)^2 dt + \int_{D_1 T_s}^{(D_1 + D_{2,n}) T_s} \left(I_{\mathrm{L,peak},n} \frac{D_{2,n} T_s + D_1 T_s - t}{D_{2,n} T_s} \right) \right] \times \frac{1}{T_s} \tag{4.16}$$

$$= F_{\mathrm{r},fs} R_{\mathrm{DC}} \frac{I_{\mathrm{L,peak},n}^2}{3} \left(D_1 + D_{2,n} \right)$$

Average conduction loss in the DCM-Boost inductor winding is approximately as follows

$$P_{\mathrm{h,avg}} \approx \frac{F_{\mathrm{r},fs} R_{\mathrm{DC}}}{3} \sum_{n=1}^{\frac{T_{\mathrm{line}}}{T_s}} I_{\mathrm{L,peak},n}^2 \left(D_1 + D_{2,n} \right) \times \frac{T_s}{T_{\mathrm{line}}} \tag{4.17}$$

4.1.6 Thermal Conductivity

Losses in the core and winding may cause an excessive temperature rise in the inductor. Usually the temperature in the core is allowed to rise up to 100 °C while the ambient temperature is at maximum 60 °C. Thermal resistance R_{th} of the core describes the thermal conductivity of it. With the knowledge of the temperatures defined above and the thermal resistance, one can calculate how much inductor is allowed to have overall losses.

In other words, overheating of an inductor defines an upper limit for the losses in the inductor. In the following a practical example of maximum allowable power loss in ETD-49 inductor/transformer is calculated. Thermal resistance for different types of cores is presented in /11, pp. 284 - 285/.

$$R_{\mathrm{th,ETD49}} = 12 \frac{^0\mathrm{C}}{\mathrm{W}}$$

$$T_{\mathrm{core}} = 100^0\mathrm{C}$$

$$T_{\mathrm{ambient}} = 60^0\mathrm{C}$$

$$P_{\mathrm{h,max}} = \frac{T_{\mathrm{core}} - T_{\mathrm{ambient}}}{R_{\mathrm{th,ETD49}}} = \frac{100 - 60}{12}\mathrm{W} = 3.33\mathrm{W}$$

where $P_{\mathrm{h,max}}$ is the maximum allowable sum of the winding and core losses, T_{core} is the maximum core temperature and T_{ambient} is the maximum expected ambient temperature.

4.2 Flyback transformer for BIFRED application

4.2.1 General

Flyback transformer is not a usual kind of a transformer. A normal transformer has power balance between the primary and the secondary sides all the time. That means if some power goes in to the primary winding the very same power, except losses, is released by the secondary winding at the very same moment of time. This holds exactly only for an ideal transformer because of the magnetizing current required for a real transformer. In the flyback transformer the power flow from the primary to the secondary is artificially prevented with a secondary side diode (switch-on time). Therefore, only the magnetizing current is able to flow through the primary winding and the transformer is energized. This is illustrated in Fig. 4.7.

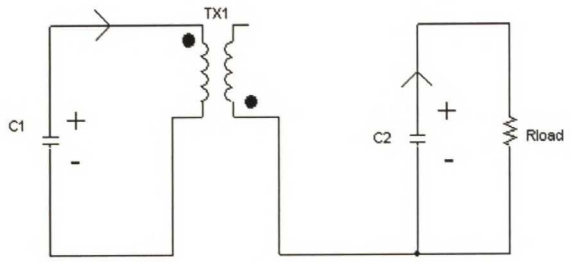

Figure 4.7 Flyback transformer energizing. The current is flowing through the primary winding and current flow through the secondary winding is prevented by the diode. Consequently, the transformer is being energized and no power is delivered from the primary to the secondary while the switch is on.

The stored energy is released to the secondary when the primary side switch is off. The magnetizing inductance of the transformer reverses its polarity, at the moment of the turning off the switch, in order to retain the current flow. The reversed polarity of the inductance forward biases the secondary side diode and the energy flow from the transformer to the load and output capacitor is enabled. No current is flowing through the primary winding while the switch is off. This is illustrated in Fig. 4.8.

Obviously, the flyback transformer utilizes only the magnetizing inductance of the transformer and the power delivered to the secondary depends on the value of the inductance. For example, in DCM operation of the transformer the power delivered from the primary to the secondary does not depend on the secondary side parameters at all, Eq. (3.12).

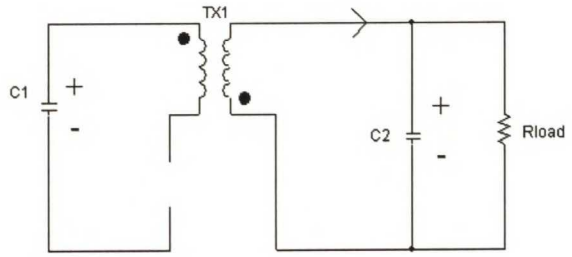

Figure 4.8 Flyback transformer, switch is off. No current is flowing at the primary side and the flyback transformer is de-energizing through the secondary winding to the load and output capacitor.

Since the magnetizing inductance is dictating the operation of the flyback transformer, it has to be designed like an inductor. In that case, one has to use a gapped core, particularly for the DCM flyback transformer, in order to avoid excessive core loss and saturation.

4.2.2 Losses in the core

Power loss in the flyback transformer's core is determined with pretty much the same way than in the DCM boost inductor. Current through the flyback transformer's primary winding consists of a sequence of triangular pulses in DCM operation. In CCM operation the triangular current pulses have a certain offset value I_{M0}. This is illustrated in Fig. 4.9, where the magnetizing current of the flyback transformer is depicted in CCM operation. If the Flyback transformer operates in DCM I_{M0} equals to zero.

The peak value of the transformer current is shown in Eq. (3.3). I_{M0} is as follows

$$I_{M0} = \frac{N_2}{N_1} I_{out} - \frac{V_C D_1 T_S}{2L_M} = \frac{N_2}{N_1} \frac{V_{out}}{R_{load}} - \frac{V_C D_1 T_S}{2L_M} \tag{4.18}$$

where I_{out} is the load current. Placing the Eq. (4.18) to Eq. (3.3) yields

$$I_{M,peak} = I_{M0} + \frac{V_C D_1 T_S}{L_M} = \frac{N_2}{N_1} \frac{V_{out}}{R_{load}} + \frac{V_C D_1 T_S}{2L_M} \tag{4.19}$$

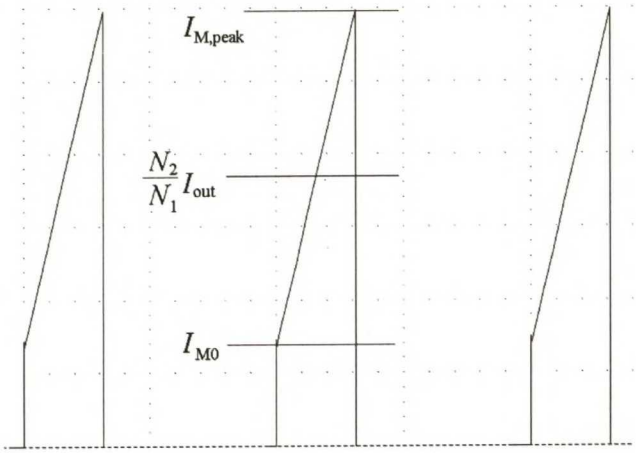

Figure 4.9 Magnetizing current of a flyback transformer, here in CCM operation. The current starts to rise from I_{M0}. In DCM operation I_{M0} equals to zero.

Thus, the relative average loss in the core, for the 3F3 material and 100 kHz switching frequency, is in CCM operation of the flyback stage as follows (Eqs. (4.3) & (4.5))

$$P_{h/V} = 163\times10^{-6}\left(\frac{\mu_0 N_1}{\frac{l_g}{A_{g,e}}+\frac{l_e - l_g}{\mu A_e}}\times\left(\frac{N_2}{N_1}\frac{V_{out}}{R_{load}}+\frac{V_C D_1 T_S}{2L_M}\right)\right)^{2.758} \frac{kW}{m^3} \quad \textbf{(4.20)}$$

where $A_{g,e}$ is calculated from Eq. (4.7).

4.2.3 Core saturation

Core saturation should be avoided in the flyback transformer in the same way as in the DCM boost inductor. The flux density graph for the 3F3 material was already presented in Fig. 4.3.

4.2.4 Number of turns

The needed amount of the wire turns for the primary winding can be determined as described for the DCM boost inductor in section 4.1.4. Equations (4.9), (4.10) and (4.11) are suitable for the determination for the flyback transformer. The number of turns for the secondary winding is obtained by dividing the number of turns of the primary winding by the turns ratio.

4.2.5 Winding and winding losses

A transformer has two purposes in a power supply application. The first thing is to provide an electrical isolation and the other a lower voltage level for the secondary side than the primary side. The latter is achieved by adjusting the turns ratio. Electrical isolation is achieved by a proper insulation between the primary and the secondary windings. However the proper insulation requires a certain creepage distance between the ends of the windings. Therefore, the whole winding breadth of the bobbin presented in Fig 4.4 is not available for the transformer windings. Usually an 8 mm creepage distance is required to assure an adequate insulation. In that case one has to leave a 4 mm strip of empty space for the both ends of the windings. Since the winding breadth for a transformer is even more limited than for a normal inductor, the resulting primary or secondary winding of a transformer tend to be multi layer ones. Winding arrangements for an inductor and also for flyback transformer were already discussed in section 4.1.4 and 4.1.5.

Winding losses should be determined for both windings and all current components. Current through the primary winding of the flyback transformer is depicted in Fig. 4.10.

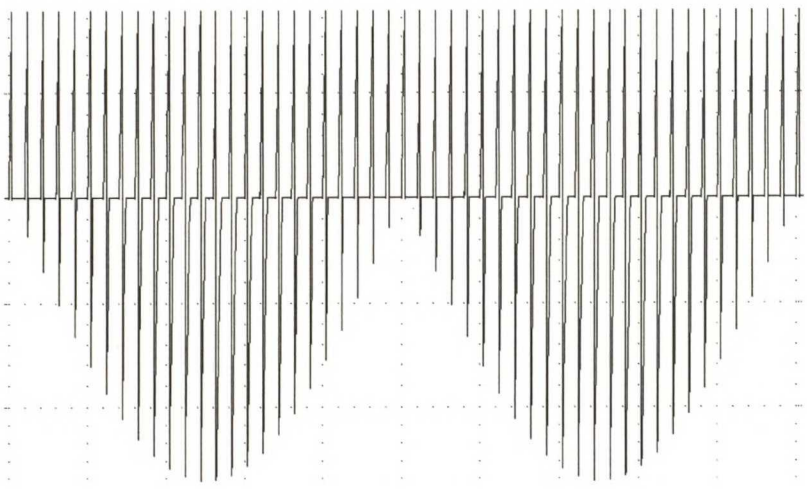

Figure 4.10 Current through the primary winding of Flyback transformer of BIFRED application. The upper sequence of current pulses have a constant peak value and it is considered as the "normal" flyback current. The lower sequence consist of the decreasing part of the DCM boost inductor current pulses and it has clearly a rectified sinusoidal envelope.

As mentioned in section 3.1.5, the decreasing part of a boost inductor current pulse flows through the flyback transformer's primary winding. Therefore, the peak values of the boost inductor current determine also a certain proportion of the winding losses in the flyback transformer of BIFRED. The decreasing part of the boost inductor current

pulse has naturally the same peak value as the boost inductor current, Eq. (3.2). Conduction loss calculation was explained in Section 4.1.5.

4.3 Leakage inductance of the transformer

4.3.1 General

A transformer has always a certain leakage inductance. The leakage inductance is parasitic phenomenon and usually the effects caused by it are harmful. In a normal power supply application the leakage inductance imposes a voltage spike over the switching device. Leakage inductance, like any inductance, tries to retain the current flow after the switch is turned off. Even a negligible leakage inductance can cause a remarkable voltage spike if the switching device is very fast. The voltage spike can be calculated as follows

$$V_{\text{spike}} = L_{\text{sigma}} \frac{\Delta I}{t_{\text{off}}} \tag{4.21}$$

where V_{spike} is the peak value of the voltage spike, L_{sigma} is the leakage inductance, ΔI the change in the current and t_{off} the cut-off time. Eq. (4.21) reveals that if the switching process is ideal e.g. the current flow ceases immediately then even the existence of a small leakage inductance causes an infinite voltage spike over the switch. In a regular power supply application RC-snubber can be used to prevent the voltage spike effectively. The leakage inductance is especially harmful for a single-stage converter like the BIFRED. In section 4.3.2 the effect of the leakage inductance in BIFRED application is briefly described and in section 4.3.3 one solution for the problem is proposed.

4.3.2 Effect of the leakage inductance

In Fig 4.11 the leakage inductance is placed to BIFRED topology in series with the flyback transformer. In Fig. 3.3 the current paths and directions during the switch-on are presented. Inspection of these two figures gives an idea what will happen when the

switch is turned off. The DCM boost inductor L_1 is fully energized at the last moments of the switch-on time and the current through has its peak value, Eq. (3.2). At the same time, the current of the flyback transformer is circulating to the *opposite* direction and the leakage inductance L_{sigma} is consequently fully energized and the current through has its peak value, Eq. (3.3).

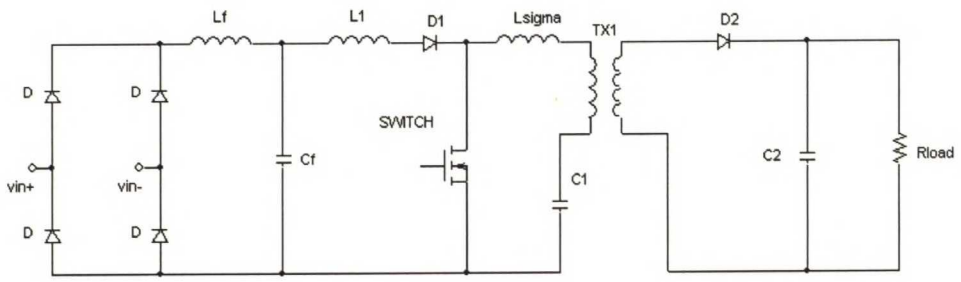

Figure 4.11 BIFRED with leakage inductance L_{sigma} which is placed in series with the flyback transformer.

When the switch is turned off these two currents inevitably collide. Since the leakage inductance is smaller in value than the DCM boost inductance, it loses the battle. However, the change in the current through the leakage inductance is a sum of the peak values of the two currents. The change is as follows

$$\Delta I = I_{\mathrm{L,peak},n} - \left(-I_{\mathrm{M,peak}}\right) = I_{\mathrm{L,peak},n} + I_{\mathrm{M,peak}} \tag{4.22}$$

and the change is due to happen very fast as referred earlier. According to Eq. (4.21), the voltage stress imposed over the leakage inductance and switch may be large since the change in the current is a sum of two large peak currents (DCM operation). Simulation results have indicated that perhaps the normal RC-snubber is not a suitable solution to deal with the voltage spike and that is why some other method has to be used. Simulated switch voltage, without any snubber, is depicted in Fig. 4.12. Spikes in the figure are excessive.

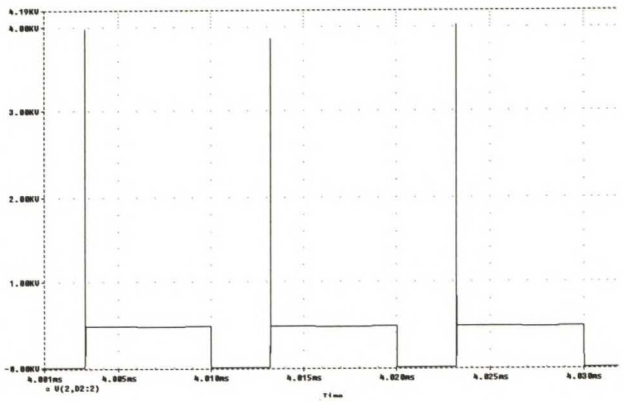

Figure 4.12 Simulated voltage over the switch in BIFRED. The excessive voltage spikes are caused by the leakage inductance. Values used in the simulation: L_1 = 268 µH, L_M = 467 µH, D_1 = 0.31 and L_{sigma} = 5 µH. The switch used in the simulation was ideal one and the turn off time was set to be t_{off} = 100ns.

4.3.3 Proposed solution

An RC-snubber can be designed to prevent the voltage spike problem. The energy content of the spike is quite large and because the snubber cannot restore the energy it absorbs. It is dissipated in the snubber-resistor and in the switch. The effect of it is disastrous for the efficiency of BIFRED. Therefore, it is not an good solution for the problem.

One solution for the voltage spike problem is a loss-less snubber /13/, which is shown in Fig. 4.13. When the spike should appear the capacitors C_{sn} and C_1 absorb it effectively. When the switch is on, the voltage over the capacitor C_{sn} is applied across the filter inductor L_{sn} and consequently the inductor becomes energized. When the switch is off, the inductor transfers energy to the bulk capacitor and the energy of a spike is fully restored.

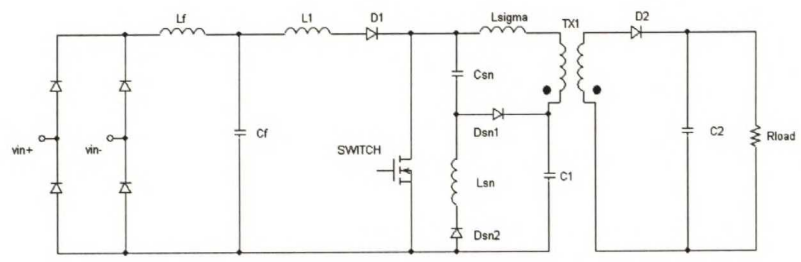

Figure 4.13 BIFRED with a loss-less snubber. When the voltage spike is to turn up, the capacitors C_{sn} and C_1 swallows it. Diode D_{sn1} is forward biased. The energy stored in the C_{sn} is transferred to the inductor L_{sn} and from there it is restored to the bulk capacitor when the switch is turned on.

Simulated voltage over the switch with the proposed snubber is illustrated in Fig. 4.14.

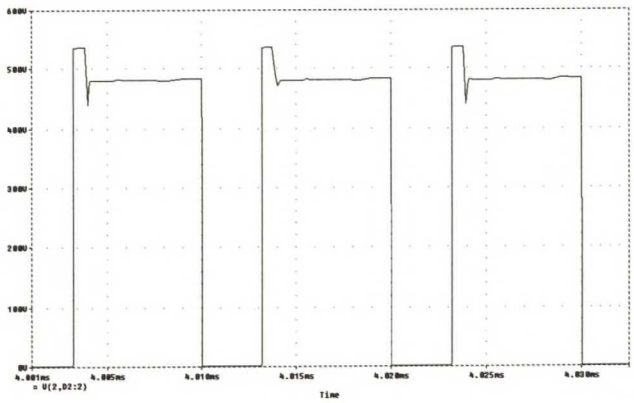

Figure 4.14 Simulated voltage over the switch with the proposed snubber. Values used in the simulation: L_1 = 268 μH, L_M = 467 μH, D_1 = 0.31, L_{sigma} = 5 μH, L_{sn} = 790.6 μH and C_{sn} = 0.94 μF. The switch used in the simulation was ideal one and the turn off time was set to be t_{off} = 100ns.

5 Prototype results

5.1 General

A 200 W BIFRED prototype with output voltage V_{out} = 75 V was built to verify the calculated results. Construction of the prototype and its essential components are presented in this chapter. It was designed to operate in DCM + CCM mode at full load and to enter DCM + DCM operation mode at approximately 75 % load in order to cease the voltage rise over the bulk capacitor. The prototype was designed to operate at a constant duty ratio, which was manually adjusted to correspond the load, so that the converter produced the desired 75 V output voltage. The bulk capacitor voltage and the output voltage carried prominent 100 Hz ripple due to the constant duty ratio. In the bulk capacitor, the 100 Hz peak to peak ripple was approximately 6 V and in the output voltage 1.5 V, both measured at full load.

Construction of the magnetic components of the prototype is presented in Section 5.2. Measured results and essential waveforms are shown in Section 5.3.

5.2 Prototype

The schematic of the prototype is presented in Fig. 4.13. Values of the components and electrical parameters used in the prototype are listed below and in Appendix A.

$L_f = 790.6\,\mu H$	$L_1 = 268.0\mu H$	$C_1 = 330\mu F$	$L_{sn} = 1787.5\mu H$	$T_{line} = 20\,ms$	$V_{in,rms} = 230\,V$
$C_f = 0.94\mu F$	$L_M = 467.3\mu H$	$C_2 = 3000\mu F$	$C_{sn} = 0.94\mu F$	$T_s = 10\,\mu s$	$V_{out} = 75\,V$

The inductor was constructed of 39 turns of 0.71 mm. copper wire. Used ferrite core was Philips ETD-49 3F3 with a 2.2 mm air gap. The measured inductance was 268.0 μH (Appendix B).

The flyback transformer of the prototype has two layers in the primary winding and one layer in the secondary winding. Primary is composed of 36 turns of 1.25 mm copper

wire divided in two layers and secondary winding has 18 turns of 1.25 mm copper wire in a single layer. Measured magnetizing inductance from primary side was 467.3 μH and from the secondary side 118.4 μH. Turns ratio of the transformer, based on the measurements, is as follows

$$\frac{N_1}{N_2} = \sqrt{\frac{L_M}{L_M'}} = \sqrt{\frac{467.3\mu H}{118.4\mu H}} = 1.987 \approx 2 = \frac{36}{18} \tag{5.1}$$

The used ferrite core was Philips ETD-49 3F3 with a 0.8 mm air gap.

The switch of the prototype was APT8056BVR MOSFET /14/. The switch has the following ratings for the maximum drain-source voltage and continuous drain current: V_{DSS} = 800 V and I_D = 16 A. Average conduction loss in the switch during a switching cycle is as follows (see also Eqs. 4.16 and 4.17)

$$\begin{aligned} P_{h,cond,n} &= R_{DS,ON} \times \int_{nT_s}^{nT_s+D_1T_s} \left(I_{M0} + \left(I_{L,peak,n} + I_{sn,peak} + \frac{V_C D_1 T_s}{L_M} \right) \times \frac{t}{D_1 T_s} \right)^2 dt \times \frac{1}{T_s} \\ &= R_{DS,ON} D_1 * \left[I_{M0}^2 + I_{M0} \times \left(I_{L,peak,n} + I_{sn,peak} + \frac{V_C D_1 T_s}{L_M} \right) + \frac{\left(I_{L,peak,n} + I_{sn,peak} + \frac{V_C D_1 T_s}{L_M} \right)^2}{3} \right] \end{aligned} \tag{5.2}$$

where $I_{sn,peak}$ denotes the peak current through the snubber-inductor and $R_{DS,ON}$ is the on-resistance of the switch. APT8056BVR has $R_{DS,ON} \approx 1\ \Omega$ at 100 °C junction temperature.

5.3 Measured results

5.3.1 Boost inductor current

Figure 5.1 shows the two pictures of the measured boost inductor current. The envelope of the current resembles the rectified sinusoidal waveform as was desired.

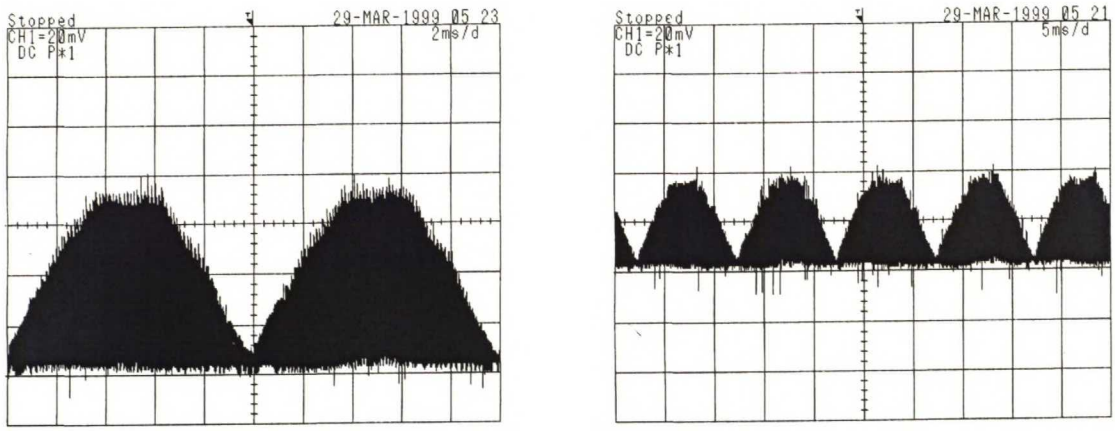

Figure 5.1 Current of the boost inductor of the prototype during one line cycle (scale 1 A/div) and during two and a half line cycles (scale 2 A/div) at full load. The envelope of the waveform resembles rectified sinusoidal waveform as was desired.

In Fig. 5.2 individual current pulses from the boost inductor current are shown. Compare to Fig. 3.1. The current pulses rise nearly linear when the switch is on. The approximation that the voltage during a switching cycle is constant seems to be justified.

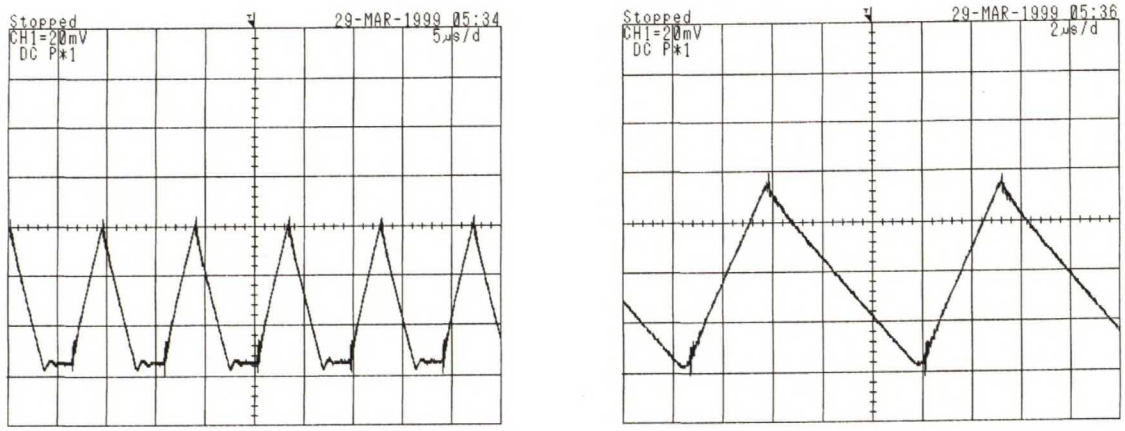

Figure 5.2 Few individual current pulses from the DCM-boost inductor current at full load. Low instantaneous line voltage (left) and vicinity of the peak line voltage (right). Scale is 1 A/div in both pictures.

5.3.2 Input current and compliance with the standard EN 61000-3-2

The measured line current is depicted in Fig. 5.3. The current does not have a perfect sinusoidal waveform. It seems to be acceptable since it is not a single current spike, Fig. (2.2) and Fig. (2.4), but it is spread over the whole half line cycle.

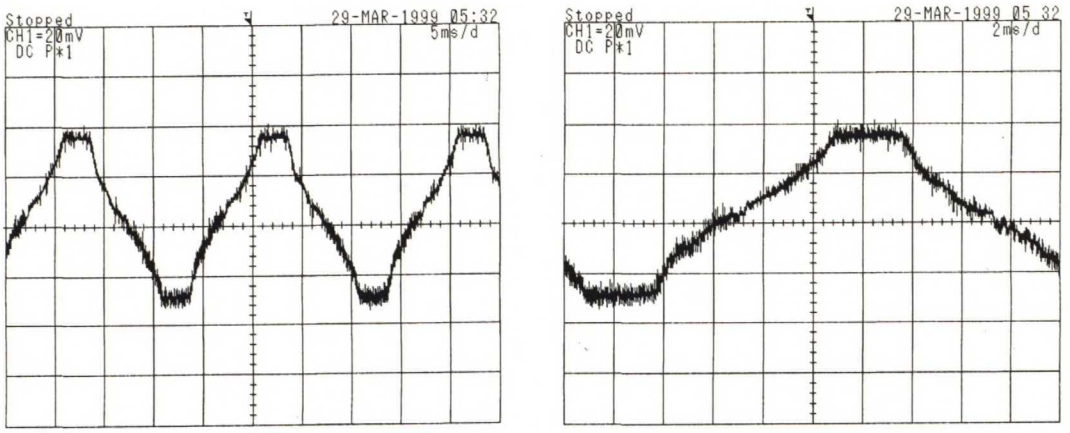

Figure 5.3 Input current of the prototype at full load, 1 A/div.

Fig. 5.4 illustrates the results from the Class D–check /1/ at full load. The waveforms of the line current and voltage are shown with Class D-template in the right side picture. The line current and the template are shown in the picture on the left. Clearly over 5 % of the current waveform lies outside of the template and the equipment does not belong to Class D. Therefore, it belongs to Class A.

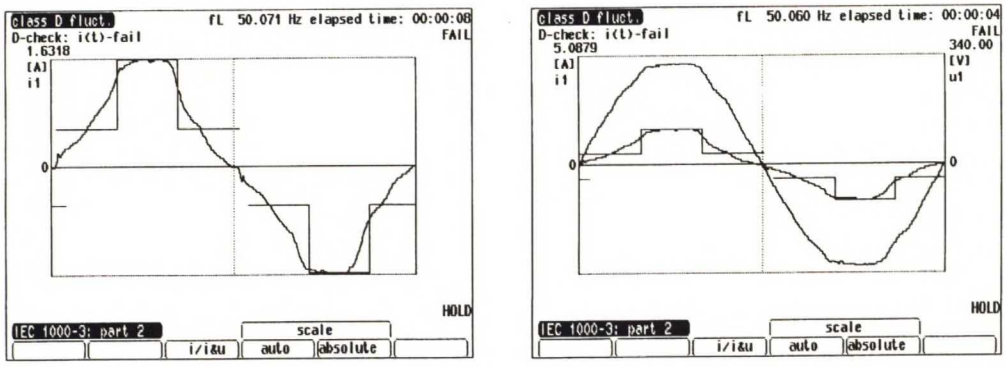

Figure 5.4 Class D-check at full load. The analyzer, NORMA D 6000 with IEC 1000-3 Testing System, concludes that the equipment does not belong to Class D. Therefore, the equipment belongs to Class A. The special template and the current are shown on the left and the template, current and line voltage in picture on the right. Power factor *PF* at full load was approximately 0.98.

The line current at light load, output power is approximately 28 W, is shown in Fig. 5.5 with and without the Class D template. The waveform of the current is not so smooth as it was at full load. However, clearly over 5 % of the waveform lie outside of template and the analyzer concludes that the equipment does not belong to the Class D. Therefore it belongs to Class A and it complies with the standard also at light load.

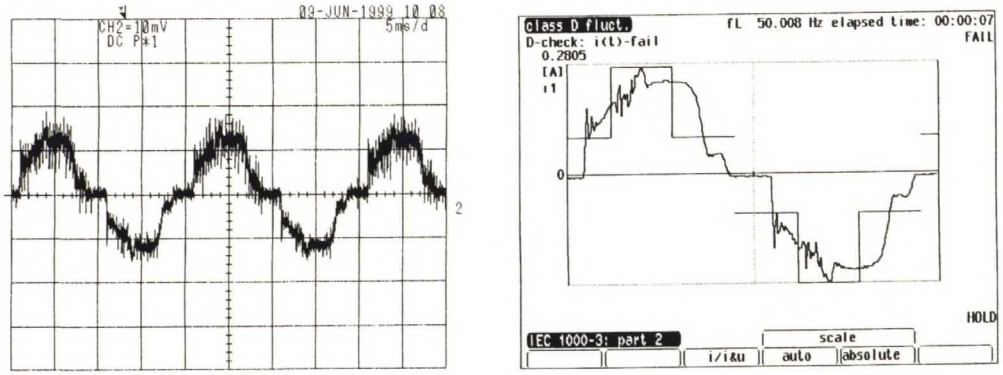

Figure 5.5 Line current at light load, output power is approximately 28 W. Left picture is from an oscilloscope, 200 mA/div, and right picture is from the analyzer. Clearly over 5 % of the current waveform lie outside of the template. The analyzer concludes that the equipment does not belong to Class D and therefore it belongs to Class A. Power factor *PF* at the light load was approximately 0.95.

Fig. 5.6 shows a bar-chart of the measured current harmonics from 3 to 13 and corresponding Class A limits. The harmonics are clearly below the limits.

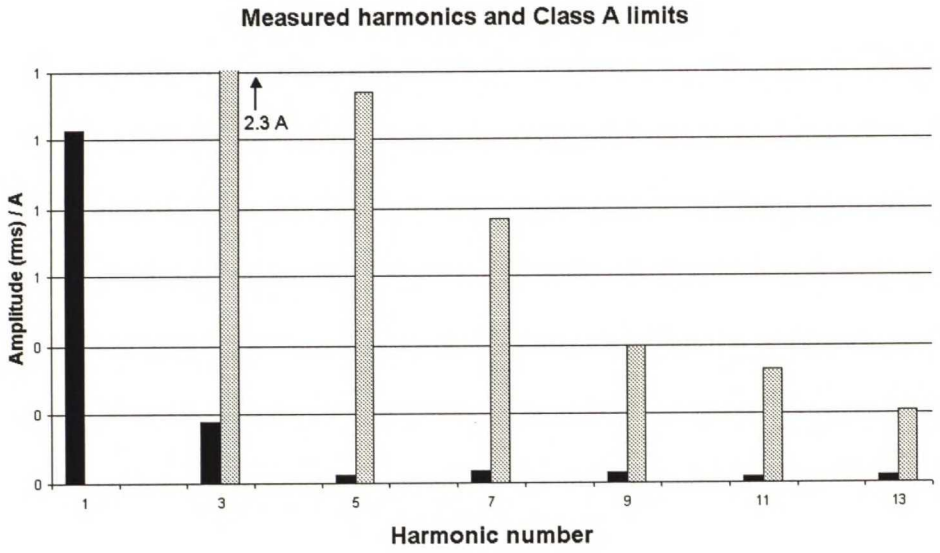

Figure 5.6 Measured current harmonics from 3 to 13 (black bars) of the protype at full load and Class A limits (grey bars). The measured harmonics are clearly below the limits. Power factor *PF* was approximately 0.98 at full load.

5.3.3 Bulk capacitor voltage

The measured bulk capacitor voltage as a function of input power is shown in Fig. 5.7. The calculated ideal curve of the expected behavior of the bulk capacitor voltage is added to the figure. The measured behavior of the bulk capacitor voltage resembles very much the calculated behavior. The converter is obviously in DCM + CCM mode at an

input power range above 150 W and the voltage follows Eq. (3.10). Below 150 W the converter is in DCM + DCM mode and the rise of the voltage is ceased. The voltage in DCM + DCM operation is determined by Eq. (3.16). The errors between the ideal and measured results are only few percents. Since the bulk capacitor voltage is not the voltage, which is regulated and in the ideal calculation losses and other practical phenomena were not considered, the results can be considered to be good.

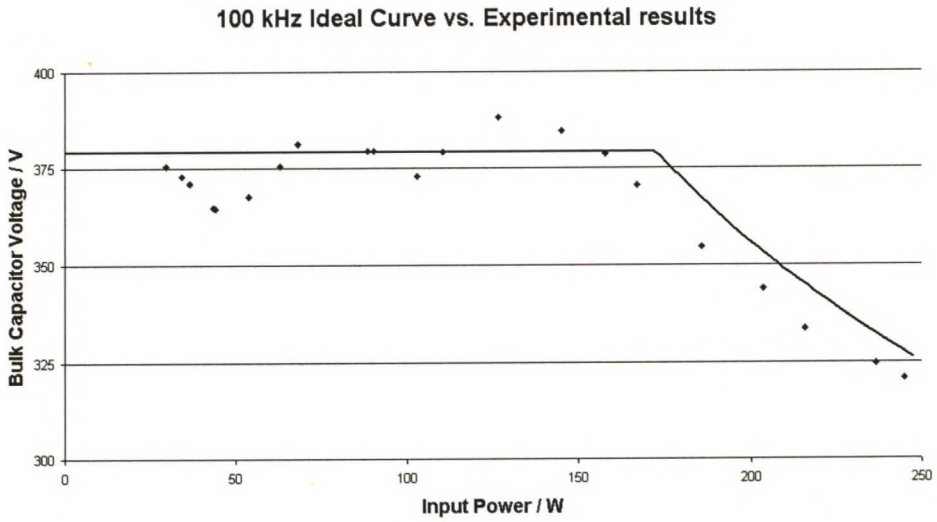

Figure 5.7 The measured and calculated behavior of the bulk capacitor voltage as a function of input power. The measured pattern of the voltage resembles very much the calculated curve.

5.3.4 Efficiency

Efficiency is not an absolute value of a certain topology. It can be improved or degraded by the designer. However, it can be said that the single-stage solution has worse efficiency than the two-stage solution if the same components are used in both topologies. For example, the conduction loss in the two-stage solution's two switches in DCM + DCM operation, with currents I_1 and I_2, is to be calculated from

$$P_{\text{h,cond.,2-stage}} = KR_{\text{DS,ON}}\left(I_1^2 + I_2^2\right) \tag{5.3}$$

while the conduction loss in the single-stage solution's single switch is

$$P_{\text{h,cond.,1-stage}} = KR_{\text{DS,ON}}\left(I_1 + I_2\right)^2 = KR_{\text{DS,ON}}\left(I_1^2 + 2I_1I_2 + I_2^2\right) \tag{5.4}$$

where K is a constant factor for a certain current waveform. The conduction loss is clearly higher in the single-stage case since the loss is proportional to the square of sum rather than the sum of squares.

In BIFRED the flyback transformer and the switch are the most critical components from the efficiency point of view. The current through the switch is composed of three different currents: I_L, I_M and I_{sn} and the conduction loss in the switch is proportional to the squared sum of the peak values of the currents, Eq.(5.2). Due to this fact, the individual currents have to be kept as low as possible and a switch with a low $R_{DS,ON}$ has to be used in order to retain acceptable efficiency. With different kind of winding constructions and by using different kind of switches even a few percent changes in the efficiency were observed. Thus, the efficiency is a result from component choices and designer's skills and experience.

In Fig.5.8 the measured efficiency of the prototype is shown. At full load efficiency is $\eta = 0.861$ and it can be considered to be relatively good.

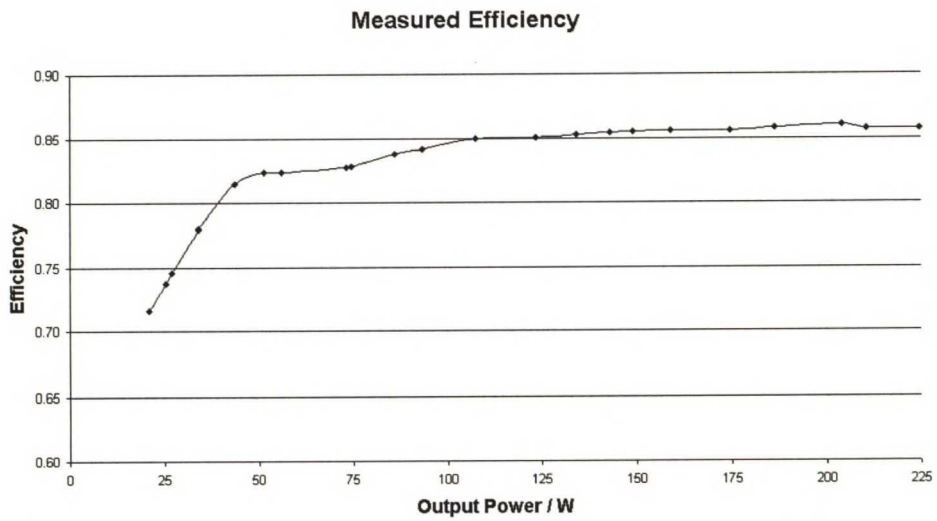

Figure 5.8 Measured efficiency of the prototype as a function of output power.

6 Conclusions

The ideal operation of the three single-stage converter was analyzed and presented. A prototype of BIFRED was built to verify and assess the ideal analysis and the compliance with standard EN 61000-3-2. The prototype behaved as expected: the bulk capacitor voltage rise can be ceased before the 450 V limit by a proper design of the converter and the input current met the requirements of the standard EN 61000-3-2.

However, 200W output power may be too high for the BIFRED topology. This is because the size of the magnetic components were quite large and still the losses, especially in the transformer, were quite high. This was partly due to the 450 V limit, which forced the flyback transformer current to be in the edge of DCM and CCM operation. Therefore, one topic for further research could be the determination of the practical power range of BIFRED. The research includes size and loss optimization of the magnetic components so that the size is reasonable compared to the throughput power and losses are acceptable.

Due to the high peak currents through the switch, the choice of the switching device plays also a key role in BIFRED from the point of view of efficiency. The MOSFET of the prototype was not necessarily as low cost component as it could have been. Requirements for the switch are: $V_{DSS} \geq 800$ V and $R_{DS,ON}$ is ' as low as possible'. However, the cost of a MOSFET is inversely proportional to the value of $R_{DS,ON}$. MOSFET with high $R_{DS,ON}$ costs less but degrades the efficiency and increases the need of heat removal. One alternative for MOSFET is IGBT. State of the art IGBTs have not yet as good performance as MOSFETs for high frequency applications, but in the near future new IGBTs may well offer better efficiency and lower cost than MOSFETs. Use of such IGBT would make BIFRED truly a low cost solution with relatively high efficiency.

Leakage inductance of the transformer is one major problem of BIFRED and therefore the winding of the flyback transformer should be optimized so that the leakage inductance is negligible. Planar transformers or some other solutions may offer lower

leakage inductance than the traditional one. A special loss-less snubber was constructed to prevent the voltage spike problem. The snubber was not optimized but it was designed to keep the current through the switch as low as possible. This was done in order to keep the conduction loss low in the switch and snubber inductor. However, this led the snubber capacitor retain a DC-voltage over itself and thus became an energy storage. Optimization of the snubber from the point of view of effectiveness, efficiency and cost could be a future research topic.

Output voltage of the prototype carried a prominent 100 Hz ripple, which was due to the constant duty ratio of the switch. With closed control-loop the ripple can be removed. However, such a control means that the duty ratio is not constant in steady state operation, which inevitably degrades the power factor correction. One interesting topic for further research is the tradeoff between the reduction of the 100 Hz ripple in the output voltage and the degradation of power factor due to the variable duty cycle.

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/14/ Advanced Power Technology Homepage < http://www.advancedpower.com/ >

Appendix A

Values used in the calculations, simulations and prototype:

BIFRED:

$V_{in,rms} = 230$ V

$T_{line} = 20$ ms

$V_{out} = 75$ V

$T_s = 10$ µs

$L_1 = 250$ µH

$L_M = 450$ µH

$C_1 = 330$ µF

$C_2 = 3000$ µF

$$\frac{N_1}{N_2} = 2$$

Prototype:

$V_{in,rms} = 230$ V

$T_{line} = 20$ ms

$V_{out} = 75$ V

$T_s = 10$ µs

$L_1 = 268.0$ µH

$L_M = 467.3$ µH

$C_1 = 330$ µF

$C_2 = 3000$ µF

$L_f = 790.6$ µH

$C_f = 0.94$ µF

$L_{sn} = 790.6$ µH

$C_{sn} = 0.94$ µF

$$\frac{N_1}{N_2} = 2$$

BIBRED:

$V_{in,rms} = 230$ V

$T_{line} = 20$ ms

$V_{out} = 75$ V

$T_s = 10$ µs

$L_1 = 250$ µH

$L_2 = 75$ µH

$L_M = 10000$ µH

$C_1 = 330$ µF

$C_2 = 3000$ µF

$$\frac{N_1}{N_2} = 2$$

Modified Dither:

$V_{in,rms} = 230$ V

$T_{line} = 20$ ms

$V_{out} = 60$ V

$T_s = 10$ µs

$L_1 = 150$ µH

$L_2 = 1500$ µH

$L_M = 10000$ µH

$C_1 = 330$ µF

$C_2 = 3000$ µF

$$\frac{N_{1A}}{N_{1B}} = 2$$

$$\frac{N_2}{N_{1A}} = 2.5$$

$$\frac{N_2}{N_{1B}} = 5$$

Appendix B

Determination of the effective air gap area and number of turns

In the first column of Table 1 the air gaps l_g (mm) available for the prototype are shown. Measured inductance as a function of air gap for a winding with 28 turns of 1mm wire is shown in the second column. Measured effective air gap area $A_{g,e}$ (mm^2) is obtained by solving it from Eq. (4.10). Calculated value for $A_{g,e}$ is obtained from Eq. (4.7) and from Eq. (4.11). The table shows that with small air gap values the calculation is quite accurate. It is stressed that no exhaustive research were committed to determine $A_{g,e}$ but brief measurements to support the design procedure.

l_g	measured inductance	measured $A_{g,e}$	calculated $A_{g,e}$	calculated number of turns
0.5	461.0	270	263	28.3
0.8	309.7	275	284	27.6
1.0	265.7	292	297	27.8
1.3	211.4	297	316	27.2
1.4	200.1	302	322	27.1
1.6	177.2	303	334	26.7
1.9	157.4	318	351	26.7
2.2	138.7	322	368	26.3
2.8	117.1	345	400	26.0

Table 1 Measured inductance as function of air gap for a winding of 28 turns, measured and calculated effective air gap area and calculated number of turns for the measured inductance.

Based on the above measurement of $A_{g,e}$, the number of turns N for the desired inductance was determined. Here the desired inductance was chosen to be 265 μH, which is required for 240 - 250 W input power. Inductance is shown also for the number of turns: N - 1 and N + 1. Lack or surplus of one turn causes quite remarkable error in the inductance.

l_g	N	inductance $N-1$	inductance N	inductance $N+1$
0.5	21	236	260	284
0.8	26	246	266	287
1.0	28	247	265	285
1.3	31	243	259	276
1.4	32	245	261	278
1.6	34	246	261	277
1.9	36	246	260	275
2.2	39	255	269	283
2.8	42	252	263	277

Table 2 Calculated number of turns for 265 μH inductance. Measured effective air gap area from Table 1 was used in the calculation.

Appendix C

Peak flux densities in the magnetic components of the prototype

Table below shows the calculated peak flux densities in the magnetic components of the prototype at full load. In the calculation following values were used for duty ratio and load resistance:

$D_1 = 0.31$, $R_{load} = 28\ \Omega$

Peak flux density in the boost inductor core	$B_{peak} = 124.1$ mT
Peak flux density in the flyback transformer core:	$B_{peak} = 163.1$ mT

Appendix D

Calculated losses in the prototype

Table below shows a rough estimation of the losses in the main components of the prototype at full power ($D_1 = 0.31$)

Boost inductor	
Core losses, Eq. (4.8)	1.0 W
Winding losses, Eq. (4.17)	0.5 W
Flyback transformer	
Core losses, Eq. (4.20)	5.0 W
Winding losses (primary + secondary), Eq. (4.16)	2.0 W
Switch APT8056BVR	
Conduction loss, Eq. (5.2)	4.0 W
Turn-on loss, $(0.5 \times C_{oss}[V_C + N_1/N_2 V_{out}]^2/T_s)$	1.1 W
Boost diode D_1	
Conduction loss, $(V_D I_{D,avg})$	0.6 W
Output diode D_2	
Conduction loss, $(V_D I_{D,avg})$	2.5 W
Total calculated loss of the prototype	**16.7 W**
Measured loss of the prototype	**33 W**

At least the winding losses are too optimistic. This is because the fringing flux around the air gap increases conduction losses in the winding. There are also turn-off losses in the switch and diodes and minor losses in the filter, snubber and diode bridge.