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A new generation pixel readout ASIC in 65 nm CMOS for HL-LHC experiments

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Summary. — A prototype of a readout ASIC in CMOS 65 nm for a pixel detector at high luminosity LHC is described. The chip has been designed to guarantee high efficiency at extreme data rates for very low signals and with low power consumption. Two different analogue very-front-end designs, one synchronous and one asynchronous, have been implemented. Internal 10-bit DACs are used for biasing, while monitoring is provided by a 12-bit ADC. A novel digital architecture which maintains high efficiency (above 99.5%) at pixel hit rates up to $3\,\mathrm{GHz/cm^2}$, trigger rates up to 1 MHz and trigger latency of $12.5\,\mu$s has been developed. The chip has been designed as part of the Italian INFN CHIPIX65 project and in close synergy with the international CERN RD53 Collaboration on 65 nm CMOS. Test results of the prototype are described.

1. – The CHIPIX65 demonstrator chip

The silicon pixel detectors of the experiments located at the high luminosity Large Hadron Collider will be subject to extreme operating conditions. In particular, the innermost layer will be characterized by a Total Ionizing Dose (TID) of 1 Grad in 10 years and a pixel hit rate equal to $3\,\mathrm{GHz/cm^2}$. The design of a new readout chip is therefore required. For this purpose, the RD53 Collaboration has been established at CERN and INFN contributes to this effort through the CHIPIX65 project. A CMOS 65 nm technology has been chosen since it guarantees an appropriate radiation tolerance and the possibility of introducing more digital logic cells per pixel while keeping the power dissipation under control [1].

The CHIPIX65 demonstrator chip consists of a (64×64) array of $50 \times 50\,\mu\mathrm{m}^2$ pixels. It contains two different analogue very-front-end designs, one synchronous [2] and one asynchronous [3], both occupying an area of $35 \times 35\,\mu\mathrm{m}^2$. The former features a threshold dispersion minimization performed by hardware inside the pixels using capacitors (called "autozeroing"). In the latter the dispersion is instead minimized by means of a 4-bit local DAC. For both designs the Equivalent Noise Charge (ENC) value is below 100 e^- for an

input capacitance of 50 fF and the in-time threshold is below 1000 e^-. The total power consumption is below 5 μW for the two designs. Sensor leakage current compensation up to 50 nA is guaranteed. A Time-over-Threshold (ToT) technique is used to perform charge sampling with 5-bit precision using either a 40 MHz clock or a local fast oscillator (up to few hundred MHz).

The demonstrator features a novel pixel digital architecture based on the concept of pixel region with local trigger matching as in FEI4, but extending the grouping to 4×4 pixels with a centralized latency buffer. This approach allows an optimized sharing of the digital circuitry, maintaining an efficiency above 99.5% at pixel hit rates up to 3 GHz/cm^2, trigger rates up to 1 MHz and trigger latency of 12.5 μs with a power consumption per pixel below 5 μW [4].

The chip periphery contains the building blocks required for the correct operation of the pixel matrix. 10-bits current DACs are used for the analog front-end biasing scheme. It requires a reference current which is provided by a bandgap reference circuit. A 12-bit ADC has been included for monitoring DC voltage levels. In addition, the periphery contains a simple readout architecture in which data are sent via a serializer connected to a CMOS-to-SLVS transmitter working at 320 MHz. All the building blocks and analog front-ends implemented in this chip are silicon proven and tested after high irradiation doses of 500–800 Mrad.

2. – Test results

The chip has been submitted to the foundry for production in July 2016. The prototype performances have been then qualified through an extensive characterization campaign. A dedicated Printed Circuit Board (PCB) has been designed for this purpose. The data taking procedure has been automatized using a FPGA and a LabView data acquisition test interface. First measurements have shown that all the building blocks are fully working.

Concerning the synchronous analog front-end, a ENC equal to 90 e^- has been obtained and it has been successfully operated with thresholds as low as 300 e^-. In addition, the correct operation of the local oscillator for the fast 5-bit ToT counting has been verified at a frequency equal to 320 MHz. Regarding the asynchronous front-end, a ENC of 85 e^- has been obtained, together with a threshold dispersion in untrimmed configuration equal to 450 e^-.

The characterization of the 10-bit DACs has shown a very good linearity in the whole range. In addition, a linear characteristics has been obtained also for the monitoring ADC. Both measurements are compliant with the CAD simulations.

Furthermore, the demonstrator has been irradiated with X-rays up to a TID equal to 600 Mrad. After irradiation the chip is still fully working, with negligible deterioration of the performance in terms of gain, noise and threshold dispersion.

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