IL NUOVO CIMENTO **41 C** (2018) 72
DOI 10.1393/ncc/i2018-18072-1

COLLOQUIA: IFAE 2017

Design and test of a 20 ps TDC for different applications

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received 21 April 2018

Summary. — In this paper we will describe a new type of TDC that has a resolution of 20 ps. This device is realized in SiGe BiCMOS technology 0.13 μm. This technology was chosen since its structure guarantees more radiation hardness, less noise and high speed than silicon technology. A very accurate time resolution may find many applications in the high energy physics field or in medical physics.

1. – Block diagram and functioning, one TDC channel, first prototype

A crucial point of this project is the use of the SiGe technology, which allows the integration, within the same chip, of both analog components (BJT transistor amplifiers) and digital devices like the TDC, that we are presenting [1-3]. The aim is to exploit the advantages of the SiGe technology to improve the front-end performance reducing the power consumption that is a crucial feature to avoid the need for active cooling. The advantages of integrating the TDC in the front-end ASIC with the same technology are numerous: the lower cost of production, better time resolution than a TDC implemented in the FPGA, intrinsic radiation-hardness, and low power consumption. The BiCMOS SiGe technology has a better radiation tolerance than the classic Si BJT [4]. The SiGe HBT technology tolerates a dose of gamma up to 500 kGy and a neutron dose of 10^{13} n/cm, much higher than the 10 kGy and 10^{11} n/cm of the Si BJT technology [4]. In fig. 1, we can see a new prototype of a single channel TDC, that we have created and implemented in a chip. The prototype consists of three function blocks: local oscillator controlled in voltage (VCO), a latch block that receives the command from the outside to save the measurement and finally the Encoder which translates the measurement into a binary code at four bit (A-B-C-D). The results of this prototype are shown in sect. **2**

The VCO is a local oscillator, controlled by the power supply, which operates in a frequency range between 800 MHz and 3 GHz. In each VCO outputs we have the same signal, but with a delay equal to the transit time of the single element, inverter gate. This delay can be controlled by the supply voltage of the device. The short delay time between the several outputs is used by the Lacth block to obtain a very precise

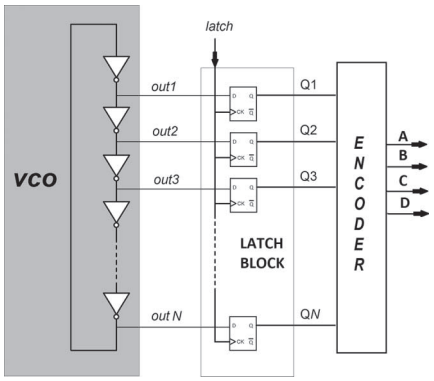

Fig. 1. – Diagrams blocks of the first prototype of the TDC, run in February 2016.

measurement. The VCO is realized by an odd number of inverters for the creation of a ring oscillator. The structure of the ring oscillator allows to divide the period in 14 different intervals. Each interval corresponds to a unique binary combination, which will be read and sampled by the memory block. The power consumption of this block stands between 250 μW and 1500 μW, depending on the frequency of the VCO oscillation.

The Latch block is realized by 7 flip-flops used as a latch. These are employed for reading and storing the temporal intervals of the VCO. The sampling frequency is controlled by an external signal, which is connected to the flip-flops. From the simulations, we found that the maximum sampling frequency is 100 MHz.

The Encoder is a device that translates the 14 intervals of the VCO in a 4 bit binary code.

2. – TDC result

The test on the TDC has been executed by measuring the time between two rise times of a square wave at 100 MHz, generated by a stimulus system, tektronix MFS 9003. The time difference ΔT, measured on a sample of 954 events, is shown in fig. 2 and it exhibits a Gaussian distribution with a rms of 15.2 ps. This rms must be divided by $\sqrt{2}$ since it corresponds to the difference of two values, giving $\frac{\sigma}{\sqrt{2}} = 10.77$ ps which is the TDC jitter.

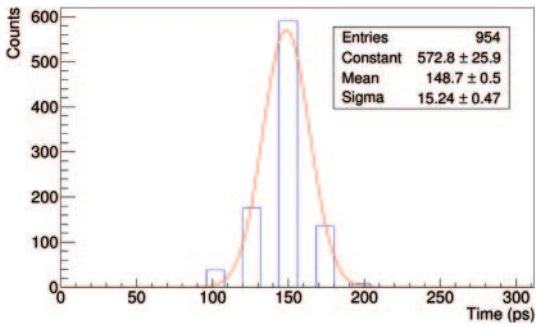

Fig. 2. – TDC, time jitter measurement.

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