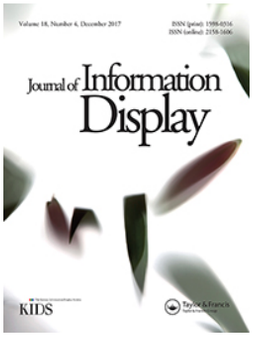

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Appearance of the p-channel performance of poly-Si TFTs with a metal S/D electrode using BLDA aiming for low-cost CMOS

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ABSTRACT

Proposed in this study and fabricated on a glass substrate without adopting impurity doping were p-channel polycrystalline silicon (Si) thin-film transistors (TFTs) with a metal source/drain (S/D) electrode. The amorphous 50-nm-thick Si films deposited on a glass substrate via plasma-enhanced chemical vapor deposition were polycrystallized using blue laser diode annealing. Gold (Au), a high-work-function metal, was evaporated for the S/D electrode directly onto the Si channel layer. As a result of the TFT formation, the typical I_d–V_g characteristics of the p-channel TFT were successfully obtained. In addition, after hydrogenation at 200°C, the drain current drastically increased. The 14 cm^2/Vs effective field effect hole mobility was deduced at the drain voltage of −1 V.

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KEYWORDS
Poly Si; TFT; blue laser diodes annealing; p-channel; metal source and drain

1. Introduction

Low-temperature polysilicon (LTPS) thin-film transistors (TFTs) with high mobility have a number of advantages for the organic light-emitting diode (OLED) pixel and for the liquid crystal display (LCD), such as low power consumption and integration of the functional circuits on a panel [1]. The high mobility of the LTPS TFT compared with the hydrogenated amorphous silicon (a-Si) TFT makes it possible for the former to integrate the peripheral driving circuits through the complementary metal oxide semiconductor (CMOS) constituted on the panel. To fabricate CMOS circuits, a considerable mobility value is required both for the n-channel TFT and the p-channel TFT [2–4].

Excimer laser annealing is effective for crystallizing and/or activating an a-Si film on glass [5], and is commercially used in the LTPS process. On the other hand, blue laser diode annealing (BLDA) for the a-Si film has been reported as a candidate for the next-generation LTPS process [6–8] because the blue diode laser beam can heat up the thin a-Si film uniformly due to its slightly higher penetration depth compared to the ultraviolet (UV) light beam, and is expected to realize a uniform grain size and to be effectively activated with reduced surface roughness [6–10]. The n-channel poly-Si TFT with a Ti metal source/drain (S/D) electrode deposited onto the sputtered poly-Si film after BLDA without using ion implantation has been proposed, and the n-channel transistor characteristic has been reported [11]. The typical transfer curve for a same-structured TFT based on an Si film that underwent plasma-enhanced chemical vapor deposition (PECVD) is shown in Figure 1 [12]. To realize CMOS TFTs on a panel using a low-cost process, a p-channel TFT with a metal S/D electrode is desired, but a p-channel poly-Si TFT with a metal S/D electrode has hardly been reported to date.

In this study, a p-channel poly-Si TFT formed via BLDA with a metal S/D electrode using a high-work-function metal was fabricated and explored.

2. Experiment

Top-gate-structured poly-Si TFTs with a metal S/D electrode were fabricated on glass substrates using BLDA at a low-temperature process. For each fabricated TFT, a 50-nm-thick channel Si layer was deposited via PECVD. After the deposition of the Si films, dehydrogenated annealing was performed at 490°C in the deposition chamber. A 445-nm-wavelength blue laser beam was controlled at 600 × 2.4 μm^2, and the Si films were crystallized by performing BLDA at 6 W with a scanning speed of 300 mm/s. The optical properties and crystallinity of the Si films before and after BLDA were evaluated using spectroscopic ellipsometry (SE).

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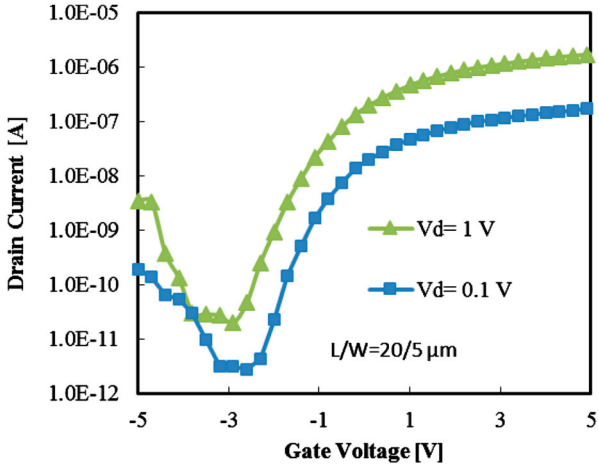

Figure 1. I_d–V_g characteristics of an n-channel TFT with Ti S/D [12].

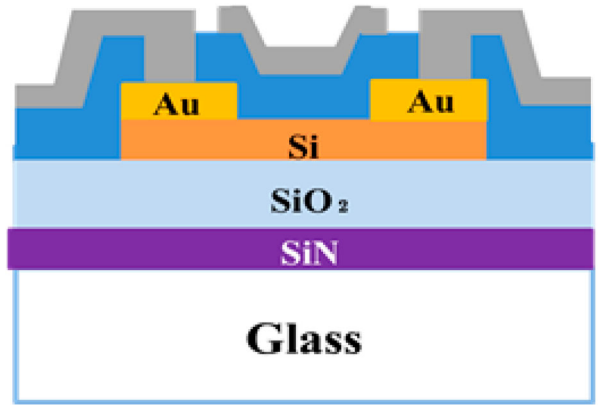

Figure 3. Cross-sectional view of the fabricated TFT.

After patterning the Si film for the channel, the samples were subjected to gas flow for 90min at 400°C, under 4% H_2 in a N_2 ambient atmosphere. After the hydrogenation, gold (Au) was deposited using vacuum evaporation. Figure 2 shows the schematic energy band diagram of the Schottky barrier for the electron between the Au and the single crystalline Si (c-Si). Here, the work function of Au is reported to be 5.1 eV, and the electron affinity of c-Si is 4.05 eV [13, 14]. The resultant barrier becomes higher for the electron while the barrier for the hole becomes lower, making the injection of holes into the Si feasible. The metal S/D electrode for the p-channel layer is expected to be realized by making the Au electrodes contact the polycrystallized Si channel as well. After patterning the Au film, a 100-nm-thick SiO_2 film was deposited at room temperature using RF (radio frequency) sputtering for the gate insulator. In spite of adopting the sputtered deposition of SiO_x, a high-quality insulator can be formed by incorporating a small amount of oxygen [15, 16]. Al electrodes were evaporated on the Au electrodes after patterning the SiO_2 for the contact holes. Figure 3 shows a cross-sectional view of the fabricated TFT.

After the completion of the TFT fabrication, post-hydrogenation was done at between 180°C and 300°C in a 4% $H_2/(H_2 + N_2)$ ambient atmosphere.

All the fabricated TFT processes were limited to below 490°C for the dehydrogenation annealing after the Si deposition.

3. Results and discussion

Figure 4 shows the extinction coefficient (k) deduced from the SE analysis for the Si films before and after BLDA. Considering the extinction coefficient spectrum after BLDA, the peak value is seen at around 280 nm, and a fine shoulder is observed at around 360 nm due to the high absorption probability by the band formation of polycrystalline Si as a result of BLDA [17, 18]. Based on the results of the analysis that was done using SE, the Si film that was formed via BLDA is considered to have been crystallized fairly well.

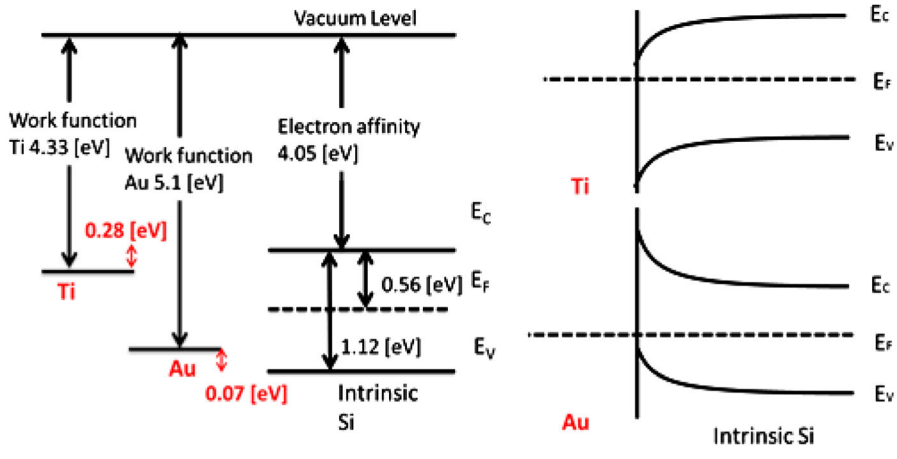

Figure 2. Schematic energy band diagram of the Schottky barrier (or quasi-ohmic barrier) for electrons and for holes.

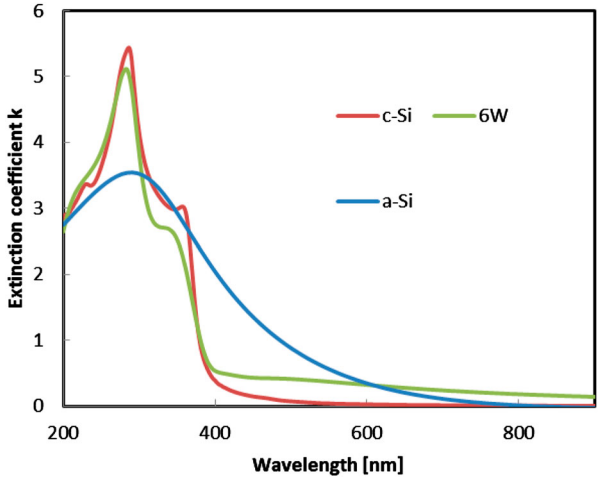

Figure 4. Extinction coefficient of a poly-Si film [20].

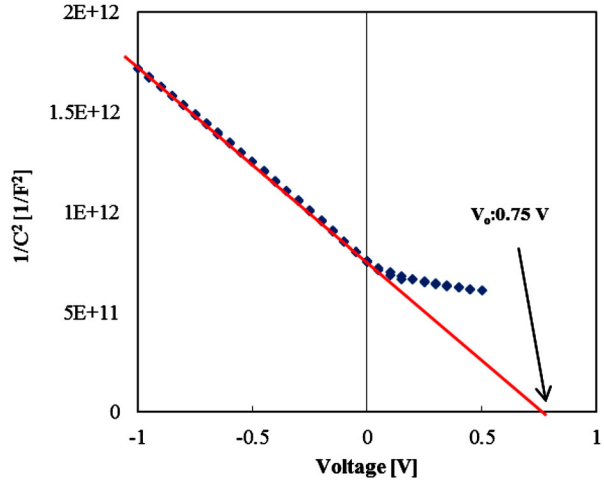

Figure 5. C–V characteristics of the Au/c-Si contact (n-type Si wafer with a (100) face (4–10 ohm cm) was used).

Figure 5 shows the capacitance–voltage (C–V) characteristics of the Au/c-Si contact. From the curve, the deduced barrier height is 0.9 eV [19]. The barrier height is calculated using Equations (1) and (2).

$$\varphi_{bn} = q(V_i + V_n) + kT, \tag{1}$$

$$V_i = V_o + \frac{kT}{q}. \tag{2}$$

Here, V_o is the cut-off voltage, φ_{bn} is the barrier height for the electron at the contact between Si and Au, and V_n is the difference between the bottom of the conduction band and the Fermi level.

Figure 6 shows the I_d–V_g characteristics of the p-channel TFT before hydrogenation [20]. Figure 7 shows the I_d–V_g characteristics of the p-channel TFT (L/W = 20/5 μm) after hydrogenation at 180°C, 200°C, 230°C, 250°C, and 300°C. The drain current increased

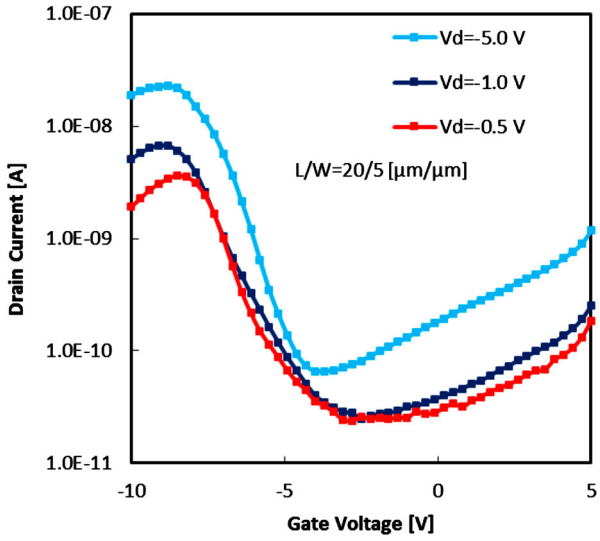

Figure 6. I_d–V_g characteristic before hydrogenation [20].

remarkably, and the typical TFT characteristics were successfully and distinctly obtained. After hydrogenation at 200°C, the highest value of the drain current was observed. The crystal defects, including the grain boundaries in the Si films and at the Si/SiO_2 interface, are considered to have been compensated for by the hydrogen atoms. With hydrogenation at 180°C compared to 200°C, the drain current becomes lower. After hydrogenation at 180°C, it is considered that the improvement of the defects in the Si film and at Si/SiO_2 interface was insufficient. After hydrogenation at 230°C, 250°C, and 300°C compared to 200°C, the S factor was improved, but the drain current and mobility became lower. The improvement of the S factor after annealing at a temperature higher than 200°C implies that the defects at the Si/SiO_2 interface were reduced by the hydrogen atoms. The reduction of the drain current, however, is considered to indicate that the Au was diffused into the Si film, or was alloyed. If the Au was incorporated into the crystallized Si film, energy would be formed near the center of the energy gap. As a result, the holes could not be supplied very efficiently into the channel from the Au electrode. In terms of mobility, a hydrogenation temperature near 200°C seems to be the maximum limit or optimum temperature in the structure or for the process.

The transfer curve shows that a fairly high carrier mobility deduction of 8.1 cm^2/Vs was obtained at the drain voltage of −1 V after hydrogenation at 200°C (Figure 7). Figure 8 shows the I_d–V_d characteristics of the p-channel TFT (L/W = 20/5 μm) after hydrogenation at 200°C for 60 (30 + 30) min [20]. A smooth hole-injected current from the source to the channel can be seen. A drain-induced barrier lowering (DIBL) effect after hydrogenation is speculated to have occurred due

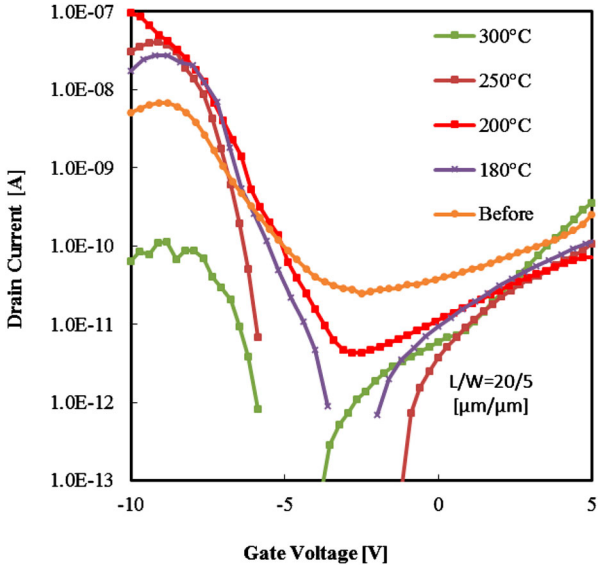

Figure 7. I_d–V_g characteristics before and after hydrogenation at 180°C, 200°C, 250°C, and 300°C ($V_d = -1.0$ V).

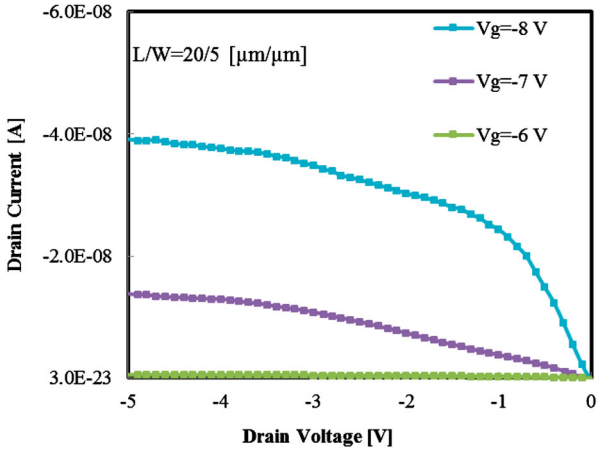

Figure 8. I_d–V_d characteristic after hydrogenation at 200°C [20].

to the improvement of the Si surface (i.e. reduction in the trap state densities at the poly-Si surface as a result of hydrogenation). As the hydrogen atoms are terminated at the defects such as the grain boundaries on the poly-Si surface, the Au/poly-Si Schottky barrier depends more on the higher-work-function Au electrode. The barrier height for the electrons becomes higher while the barrier height for the holes becomes lower. As a result, in this study, the drain current increased remarkably, and the typical TFT I_d–V_d characteristics were observed, as shown in Figure 8. Among the TFT cells on the glass, a maximum effective mobility of 14 cm^2/Vs was deduced at $V_d = -1$ V (L/W = 20/5 μm). The electron mobility for metal S/D TFTs in the previous results for the n-channel was much higher than the value in the current result for the p-channel [12]. Although it is reasonable that the hole mobility as the electron mobility for the polycrystalline Si TFT is not high, by adjusting the structure and optimizing the process, including the improvement of the channel crystallinity, the value can be considerably increased.

4. Conclusion

A new structure of the p-channel polysilicon (poly-Si) TFT) with a metal source/drain (S/D) electrode was fabricated on a glass substrate using BLDA, and the device performance was examined. The injection of holes from the gold (Au) metal source into the poly-Si channel was successfully accomplished, as expected. The typical I_d–V_g and I_d–V_d characteristics of TFTs were observed. After the hydrogen annealing at 200°C, the drain current drastically increased especially for the sample that had been subjected to BLDA at 6 W. The deduced effective hole mobility was 14 cm^2/Vs at the drain voltage of −1 V. By further optimizing the fabrication process, a low-cost TFT with a metal S/D electrode is expected to be realized as a CMOS constituted on a panel.

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Disclosure statement

No potential conflict of interest was reported by the authors.

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References

[1] S.M. Choi, O.K. Kwon, N. Komiya and H.K. Chung, Proc. IDW'03, **AMD/OEL p-4**, 535 (2003).
[2] Y. Miyata, M. Furuta, T. Yoshioka and T. Kawamura, Jap. J. Appl. Phys. **31**, 4559 (1992).
[3] G. Kawachi, Y. Nakazaki, H. Ogawa, M. Jyumonji, N. Akita, M. Hiramatsu, K. Azuma, T. Warabisako and M. Matsumura, Jap. J. Appl. Phys. **46**, 51 (2007).
[4] S-J. Lee, J-H. Park, K-M. Oh, S-W. Lee, K-E. Lee, W-S. Shin, M-C. Jun, Y-S. Yang and Y-K. Hwang, Jap. J. Appl. Phys. **50**, 061401 (2011).
[5] T. Noguchi, Phys. Stat. Sol. **5**, 3259 (2008).
[6] T. Noguchi, Y. Chen, T. Miyahira, J. D. Mugiraneza, Y. Ogino, Y. Iida, E. Sahota and M. Terao, Jap. J. Appl. Phys. **49**, 03CA10-1-3 (2010).
[7] K. Shirai, J. D. Mugiraneza, T. Suzuki, T. Okada, T. Noguchi, H. Matsushima, T. Hashimoto, Y. Ogino and E. Sahota, Jap. J. Appl. Phys. **50**, 021402 (2011).
[8] Y. Ogino, Y. Iida, E. Sahota and M. Terao, Proc. IMID'09 **P1-132**, 945 (2009).
[9] T. Okada, K. Sugihara, S. Chinen and T. Noguchi, J. Korean Phys. Soc. **66** (8), 1265 (2015).
[10] T. Noguchi and T. Okada, J. Inf. Disp **15**, 47 (2014).
[11] K. Sugihara, K. Shimoda, T. Okada and T. Noguchi, J. Inf. Display **18** (4), (2017).
[12] T. Ashitomi, K. Sugihara, K. Shimoda, T. Okada, T. Noguchi, T. Miyashita, Y. Kusuda and S. Motoyama, Proc. iMiD'14 **P1-48**, (2014).
[13] S. M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, 3rd ed. (John Wiley & Sons, Hoboken, NJ, 2007), p. 137.
[14] H. B. Michaelson, *IBM J. Res. Dev.* **22**, 72 (1978).
[15] S. Suyama, A. Okamoto and T. Serikawa, J. Appl. Phys. **65**, 210 (1989).
[16] K. Imura, T. Okada, H. Tamashiro, T. Ashitomi and T. Noguchi, Proc. of Int. Conf. on Intelligent Informatics and BioMedical Sciences (ICIIBMS), Okinawa, Japan, pp. 113–114 (2015).
[17] H. R. Philipp and E. A. Taft, Phys., Rev. **120** (37), (1960).
[18] J. R. Chelikowsky and M. L. Cohen, Phys., Rev. B. **10**, 5095 (1974).
[19] E.V. Kalinina and N.I. Kuznetsov, J. Electron. Mater. **25** (5), 831 (1996).
[20] T. Ashitomi, T. Harada, K. Shimoda, T. Okada, T. Noguchi, O. Nishikata, A. Ota and K. Saito, Proc. IDW 15, **AMD7-4**, 268 (2015).