A solid-state fault current limiting and interrupting device (FCLID) with power factor correction

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***Abstract*— A Solid-State Fault Current Limiter and interrupting device (FCLID) with power factor correction suitable for low-voltage distribution networks employing the Switched Capacitor (SC) Circuit is presented. Some design parameters are investigated and some optimisation is applied. In this application the Switched Capacitor (SC) is inserted in series with the supply line via an isolating transformer, providing both power factor correction and limitation of the current to a pre-set value in the event of a fault. Interruption of the fault is also possible by setting both semiconductor switches in the off state. The voltage across the load is** increased. **Optimisation is applied to correct the power factor to an acceptable value of 0.85 and keep the load voltage within acceptable limits. Losses are estimated and rating of components is discussed.**

Keywords*— *Switched Capacitor, Duty Cycle, Power factor, Current limiter, Distribution network

I. Introduction

Fault current limiting and interrupting can only be achieved by inserting a device in series with the line [1]. In this way the level of the fault current is limited to a safe value for the circuit breakers to perform the interruption much more safely. Thus the rating of the transformers, circuit breaker (CBs), buses and other electric equipment at fault current is lower.

Solid State switches are used together with reactors [2]. LC tuned circuits [3] in Fault Current Limiters. An isolating transformer [4]-[5] option providing flexibility in the choice of the VI ratings of the components used is also an option.

The Switched Capacitor (SC) Circuit, Fig.1 can be set to have either inductive or capacitive impedance at any value by setting the duty cycle of the semiconductor switches, Fig. 2. In the past it was employed for power factor correction [6] and for harmonic current compensation [7]. Fig.3 shows the voltage across the semiconductor switches and passive components of the SC circuit.

In this application, the Switched Capacitor circuit offers the capacitive series impedance during normal operation in order to improve the power (8). The fact that the power factor correction takes place in series gives rise to the load voltage. During a fault the impedance of the SC capacitor circuit can be set at any value in order to limit the current to a safe and predetermined value. Limiting of the Fault current is achieved by setting the duty cycle of the switches S1 and S2.

Compensation of the power factor is done by adjusting the impedance of the SC Circuit to match the impedance of the load. Specifically since most of the loads are inductive, the reactance of the SC circuit is set capacitive at a value to set the power factor at an improved value

In this investigation the circuit is optimized for a power factor of 0.85 and the increase of 5% of the output voltage is allowed. This can be an advantage in areas with low supply voltage.

In this application the switched capacitor circuit is inserted in series with the load Fig. 4, via a transformer providing power factor correction and in the event of a fault it limits the current to a pre-set value. Interruption of the fault is also possible by setting both semiconductor switches S_1, S_2 in the off state. The isolating transformer option has the advantage of taking the capacitor out of the power path. Provision of flexibility in the choice of the VI ratings of the various components will be discussed.

II. The Switched Capacitor Circuit As A Current Limiter And Power Factor Compensator

A. *The switched capacitor circuit*

The operation of the switched capacitor circuit Fig. 1 is explained in [8]. An expression (1) relating the impedance of the circuit to the duty cycle of the switch is derived. The relevant graph is given in Fig. 2.

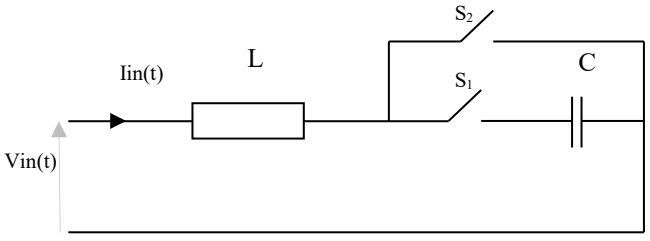

Fig. 1 The switched Capacitor circuit.

$$Z(Ko)=\sqrt{r^2+\left(\omega L-\frac{Ko^2}{wC}\right)^2} \qquad (1)$$

Ko is the duty cycle of S_1, r represents the ohmic resistance of the passive components and semiconductor switches, ω is the mains frequency, L and C are the values of the inductor and the capacitor in the circuit.

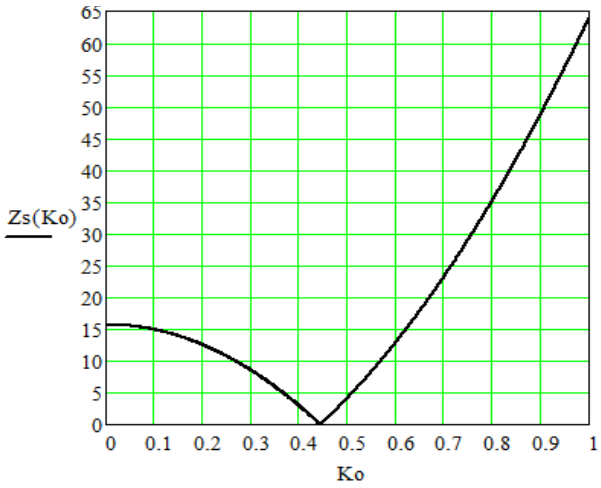

Fig. 2 Impedance of the switched capacitor circuit against Ko-the duty cycle of the switch S_1.

The voltage across the semiconductors and the switches and the passive components is higher than the voltage across the circuit. Expression (2) gives the capacitor voltage which is also the voltage across semiconductor the switches. This is displayed in Fig. 3, against the duty cycle of the switches Ko.

In Fig.3, two sets of values for L and C are displaced. As shown, higher values of C gives lower values of capacitor and switches voltage.

$$V_C(t)=\frac{V}{\sqrt{r^2+\left(wL-\frac{Ko^2}{wC}\right)^2}}\,Ko\,\frac{1}{wC} \qquad (2)$$

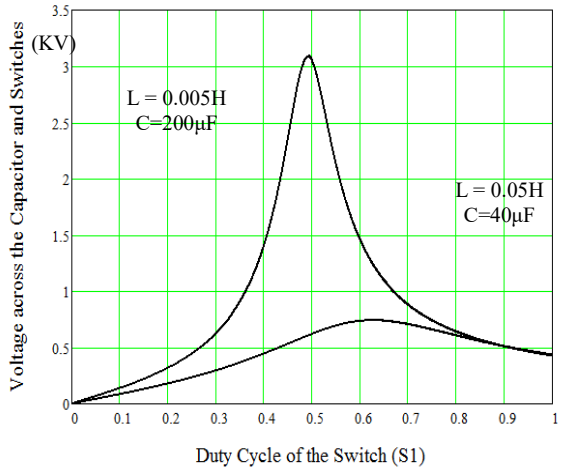

Fig. 3 Voltage across the capacitor (KV) as a function of Ko

In order to take the capacitor away from the main stream of load current, an isolating transformer is used, Fig. 4.

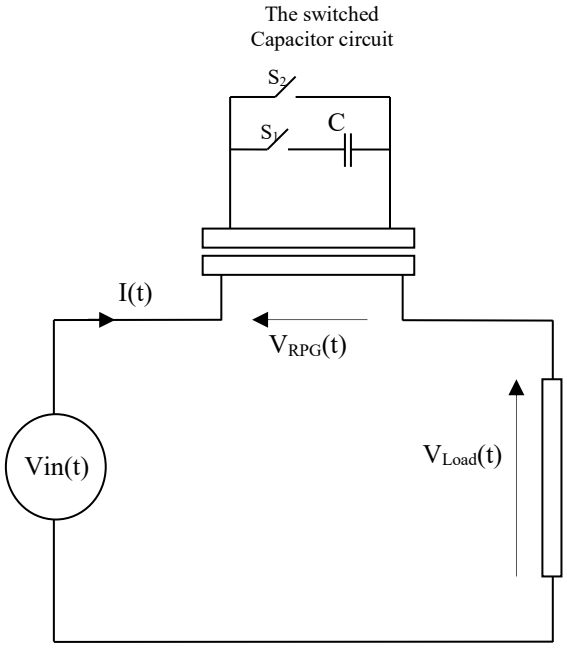

Fig. 4 The power circuit of the SC current limiter and power factor compensator with isolating transformer.

The transformer is connected with the primary to the switched capacitor circuit and the secondary to the power circuit, Fig. 4. The leakage inductance of the transformer is used as the reactance for the SC circuit and it can be complemented by an external inductor if necessary. This is L_{rpg}, Fig.5, giving with Capacitance the reactance X_{rpg} in the SC circuit. By taking into consideration the source impedance, the copper losses in the circuit, the on-losses of the semiconductor switches, the stepping action of transformer and the power circuit takes the form of Fig. 5.

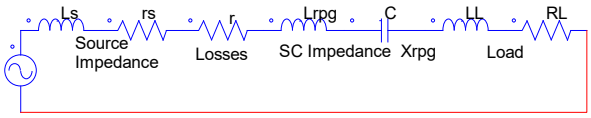

Fig. 5 Equivalent circuit of the Fault Current Limiter without the fault

The total impedance is given by

$$Z_T=\sqrt{(r+r_s+R_L)^2+\left[\omega\cdot(L_L+L_s)+\left[\omega\cdot(L_{rpg})-\frac{Ko^2}{\omega\cdot C}\right]\cdot N^2\right]^2} \qquad (3)$$

N is the turn's ratio of the transformer.

And the power factor at the input of the circuit is given by expression (4)

$$PF_{Circuit} = \cos\left[a\tan\left[\frac{\omega\cdot(L_L + L_s) + \left[\omega\cdot(L_{rpg}) - \frac{Ko^2}{\omega\cdot C}\right]\cdot N^2}{r + r_s + R_L} \right]\right] \quad (4)$$

In order to investigate the effect of the voltage across the load V_{Load}, this voltage is expressed as a ratio to the supply voltage.

$$V_{LoadRatio} = \frac{V_{Load}}{V} \quad (5)$$

Furthermore, in order to investigate the voltages across the semiconductor switches and the passive components of the switched capacitor expression (6) is derived.

$$OVR(Ko) = \frac{V_C(Ko)}{V} \quad (6)$$

These quantities are displayed in Fig. 6 and Fig.7 for two different sets of L_{rpg}, C and N against the duty cycle of the switches Ko. For every value of the power factor there is a corresponding value for the load voltage and the voltage across the semiconductor switches and the passive components of the switched capacitor.

From the graph of Fig. 6, Ko is found for the desired power factor. It is found from this graph that for a power factor corrected to 0.85 lagging, the load voltage is always 5% higher than the supply.

Fig.7 is a similar graph but for different values of L C and N. The low value of C in the circuit allows the bell shape for both the power factor and the voltage across the load. As shown the power factor can be either lagging (LHS slope of the PF curve) or leading (RHS slope of the PF curve)

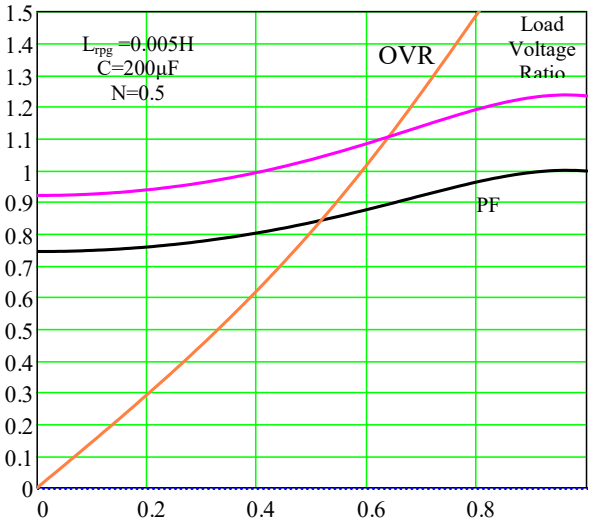

Fig. 6 Power factor and circuit voltages

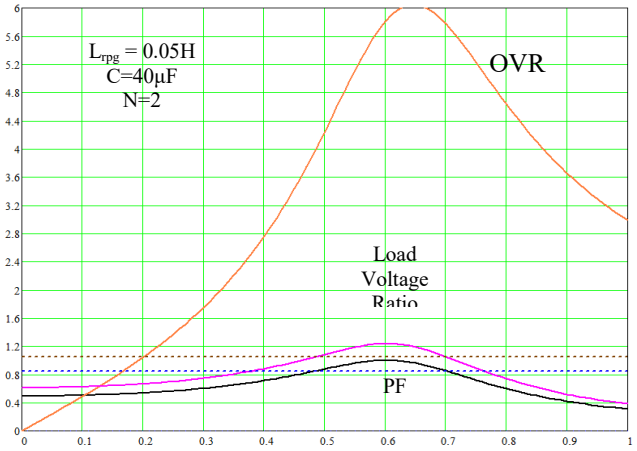

Fig. 7 Power factor and circuit voltages

III. Simulation of the Fault Current Limiter

The Fault current Limiter circuit of Fig. 4, is first simulated in PSIM. The reactance of the switched capacitor circuit is set by Ko to the appropriate value in order to compensate the load as found from the appropriate graph of Fig. 6. A number of choices exist regarding the turn's ratio and the value of C and L_{rpg}. Some of these choices are shown in Table I, II and III. In all three cases the power factor is corrected from 0.786 to 0.85 by setting the corresponding value of Ko.

TABLE I. L_{RPG} =0.05H C=40F N=0.5 Ko=0.465

Table I	V_{pcc} (rms)	V_{rpgp} (peak)	V_{Load} (rms)	V_{sc} (peak)	I (rms)	I_p (rms)
Normal operation	229	70.7	243.4	1300	47.6	23.8
Fault limiting period	230	460	-	810	14.4	7.07

TABLE II. L_{RPG} = 0.005H C=200F N= 2 Ko=0.485

Table II	*V_{pcc} (rms)*	V_{rpgp} (peak)	V_{Load} (rms)	V_{sc} (peak)	I (rms)	I_p (rms)
Normal operation	*228.5*	101	244	1297	47.5	23.8
Fault limiting period	*230*	650	-	811	14.3	7.15

TABLE III. L_{RPG} = 0.005H C= 200F N= 0.5 Ko = 0.535

Table III	V_{pcc} (rms)	V_{rpgp} (peak)	V_{Load} (rms)	V_{sc} (peak)	I (rms)	I_p (rms)
Normal operation	224.5	101	244	287	47.6	23.8
Fault limiting period	230	459	-	724	64.2	32.2

The voltage across the semiconductor switches and the passive components of the switched capacitor (OVR) must be kept as low as possible. The lower values of this quantity are achieved for the larger values of C as dictated by the graph of Fig.3. Furthermore, values of the turn's ratio of the transformer lower than one reduce this voltage dramatically, Table III.

In this investigation a load of a 4Ω resistor and load inductance 0.01H giving a load power factor of 0.786 and a line current of 47.5A is considered. The actual fault current of the circuit is 12.34KA. In normal operation the SC circuit is acting as a power factor corrector. The inductive impedance of the load is matched to the impedance of the SC circuit by choosing the appropriate value of the duty cycle Ko from graph of Fig. 6.

The fault is applied at one second and Interruption takes place two seconds after the occurrence of the fault. These of course can be set to any value. Limiting action is applied by inserting the maximum reactance of the SC circuit by setting the duty cycle to 1 i.e. switch S1 is permanently on. Simulation results

The SC circuit inductance L_{rpg} and capacitance C are set in the first instance at 0.05H and the capacitor is 40μF, Table I. The transformer ratio is 0.5. In order to keep the power factor to 0.85 and the corresponding value of the load voltage to only 5% (241.5V) above supply voltage the duty cycle of the switches is derived from graph of Fig. 7 as 0.485. At this value the voltage across the capacitor and the semiconductor switches is 4 times higher than the supply! This voltage is dramatically reduced when a higher value of capacitance is chosen.

For L_{rpg}=5mH and C=200μF and keeping N=2 the results are shown in Table II. The voltage across the switching transistors is kept to 4 times the supply voltage with the same turn's ratio. When the turns ratio is set to 0.5 the results are better, Table III. From Fig.3, it is evident that lower voltage across the capacitor and the semiconductor switches occurs at higher values of capacitance C and lower turn's ratios of the transformer. If we consider Table III, the case of the transformer with half the turns in the secondary compared to those in the primary (N = 0.5), L_{rpg} = 0.005H and C = 200μF, the voltage across the transistors and the capacitor is only 0.88 p.u. the supply voltage. The current in the SC circuit is naturally half the line current at 23.7A. During the current limiting period the current is limited to 64.2A i.e. 1.35pu. Also the voltage in the SC circuit is raised to 723V only (2.225pu) and the current in the SC capacitor circuit to 35.35A.

Fig. 8, displays the Line current before the fault (power factor correction mode) and during the Fault (Current limiting mode) and the Interruption of the fault (interruption mode). The load current is 47. 5A and in the event of a fault it would have been 12.3KA. The Switched Capacitor limits the current to 64.2A (1.5 pu) one cycle after its occurrence. Eventually the current is interrupted three seconds after its occurrence. Limiting and interruption actions depend on the control circuit and can be set to suit the application. Also the current during the limiting period can be set accordingly. Limiting action is achieved by inserting the maximum reactance of the switched capacitor by setting Ko = 1 i.e. S_1 is permanently on. For the first few cycles of the application of the fault the current exceeds the normal current by about 2.5 times

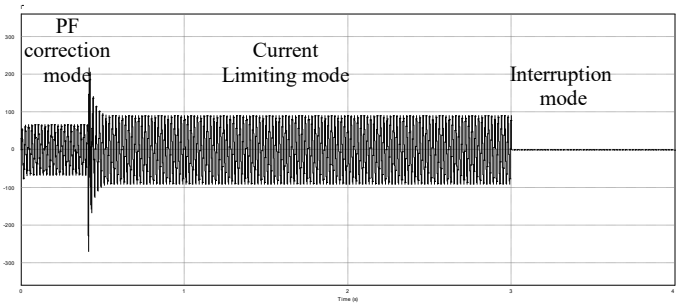

Fig. 8 Line current before and after Fault with Interruption of the fault, Table II

A. *Ratings of components of the Solid State Current Limiting Device*

In this section the voltage current rating of the transformer, Capacitor C and the two semiconductors switches are discussed. The best set of values for L_{rpg}, C and N are in Table III, for the lowest rating of the transistors, and hence suitable transistors are selected.

The maximum voltage across the transistors is 724V (2.23 p.u.) during the current limiting period and the maximum current at the same period is 64.2A, Table III. The transistor IRGPS60B120K is considered as appropriate for this application rated at 1200V and at least 60A (continuous) and is tested for its losses.

The transformer is subjected to 324V rms and 32.2A rms during the fault i.e. 10.4KVA Table III. In normal operation the voltage is 71V and the current 23.8A i.e. 1.7KVA. Therefore the transformer is rated accordingly.

The capacitor used is 200μF and the voltage across it is the same as the one for the transistors. This voltage is less than the supply during the PF Correction mode as shown in Table III but is raised to 724V (2.23pu) during the brief period of the Current limiting. Hence it must be rated accordingly

B. *Losses*

Losses occur in the transformer and the semiconductor switches. In the transformer we have the copper and iron losses. In the semiconductor switches we have the steady state losses and the switching losses. The first are associated to the on resistance R_D for power MOSFETS and the *on* voltage for IGBTs. The switching losses are associated to the switching delays of the transistor and the switching frequency.

Losses for the transistors are estimated in the following way. The transistor IRGPS60B120K) is simulated in Proteus Design Suite. The current and voltages are taken from Table III, for the PF Correction Period. That is 64.4A and 286V the peak value of the line current and voltage. From the simulation the time delays related to the switching are derived and confirmed with the ones in the data sheet.

Expressions (7) to (13) were used in order to calculate the switching losses. Turn-on and turn-off time delays were derived from the simulation graphs shown in Fig. 9 and Fig. 10 and were found to be 26ns and 380ns respectively.

$$W_{on} = \frac{1}{2} V_{CE} \cdot I_C (t_1 - t_0) \quad (7)$$

$$W_{off} = \frac{1}{2} V_{CE} \cdot I_C (t_2 - t_0) \quad (8)$$

$$P_{sw} = \left(W_{on} + W_{off}\right) \cdot f_s \quad (9)$$

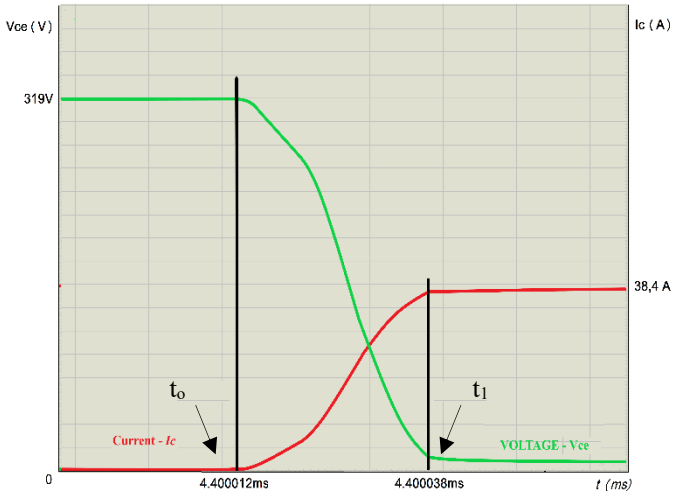

Fig. 9 Turn-on time delay of the IRGPS60B120K IGBT, green line:Vce and red line:Ic current.

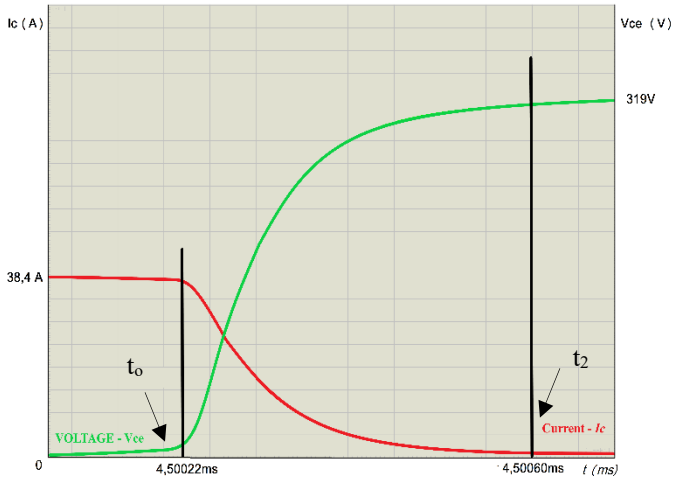

Fig. 10 Turn-off time delay of the IRGPS60B120K IGBT, green line:Vce and red line:Ic current.

Expression (7), (8) and (9) are valid for one switching instance. For the next switching instant, both V_{CE} and I_C will change in a sinusoidal manner. The energy lost in each power cycle for the switching is given by (10) and (11).

$$E_{LossesON} = \sum_{n=1}^{M} \left[\left(t_1 - t_0\right) \cdot \frac{V_{CE} \cdot I_C}{2} \cdot \sin^2 \left(\omega \cdot T \cdot n\right) \right] \quad (10)$$

$$E_{LossesON} = \sum_{n=1}^{M} \left[\left(t_2 - t_0\right) \cdot \frac{V_{CE} \cdot I_C}{2} \cdot \sin^2 \left(\omega \cdot T \cdot n\right) \right] \quad (11)$$

Where V_{CE} and I_C are the peak operating values, T is the period of the switching frequency, M is the number of switching instances in a power cycle

For the on-State the lost power is given by

$$P_{LossesSS} = f \cdot 2 \cdot \sum_{n=1}^{\frac{M}{2}} \left[T_{ON} \cdot V_{CEON} \cdot I_C \cdot \sin\left(\omega \cdot T \cdot n\right) \right] \quad (12)$$

Total losses

$$P_{Losses} = \left(E_{LossesOFF} + E_{LossesON}\right) \cdot f_{sw} + P_{LossesSS} \quad (13)$$

The losses are highly depended on the switching frequency. For 5 KHz the efficiency of the system is 90% and is raised to 99% for a switching frequency of 1 KHz. This is the efficiency by considering the losses in the transistors only.

IV. Discussion

A Fault Current Limiter is presented where the SC Circuit is employed to correct the P.F. and at the same time it is a solid-state fault current limiting and interrupting device (FCLID) for low voltage distribution networks. The component parameters are optimized to improve the power factor from 0.772 to an acceptable limit of 0.85 during normal operation. Also in the event of a fault, the current is limited to 1.35 pu. Eventual interruption is possible.

The appropriate value of the duty cycle of the switches Ko is extracted from the graph, Fig.6 which displays the new pf, the pu values of the voltage across the transistors and the voltage at the load. For a lagging power factor of 0.85 the Load voltage is always 5% above the supply. This can either be tolerated or it is a useful feature in areas where the Grid voltage is low.

The circuit is first simulated in PSIM to derive its functional and operational characteristics. The goal was to improve the power factor to 0.85 and the Load voltage not to exceed by more than 5% the supply. It is tested for various values of its parameters, that is the turns ratio of the transformer and the values of the inductance and capacitance in the switched circuit. The source impedance is fixed giving a fault current of 12.34KA. From Table I, II and III it is concluded that in order to keep the load voltage within limits and the power factor at o.85 larger values of capacitance and lower values of transformer turns ratio keeps the voltage across the transistor low. In one extreme with C=40μF L =0.05H and Transformer turns ratio 2, the voltage across the transistors is raised to 15 times the supply

voltage. On the other end with C=200μF L =0.005H and Transformer turns ratio 0.5, the voltage across the transistors is lowered to 88% of the supply voltage.

The semiconductor switches carry the full load current stepped down by the isolating transformer. Hence we have the question of the rating of the various components and efficiency. The transformer is rated at about 10% of the load, during the power factor mode.

The capacitor value was chosen 200 μF in order to keep the voltage across it and the transistors low. In this case it is 88% during normal operation of the supply and 2.23p.u. during the fault limiting period.

It would appear that a transformer ratio higher than one (with the switched capacitor connected to the primary) would reduce the voltage across the switching transistors. This is not the case because the reflected impedance from the primary to the secondary is multiplied by N^2. Therefore the SC circuit will be forced to produce less reactance by a factor of N^2 in order to reflect the same impedance in the line for power factor correction. Producing less reactance Fig.2 increases dramatically Fig.3 the voltage across the semiconductor switches. Hence a turn's ratio less than one is chosen for this investigation.

The low value of C in the circuit allows the bell shape for both the power factor and the voltage across the load, Fig.7. As shown the power factor can be either lagging (LHS slope of the PF curve) or leading (RHS slope of the PF curve). For a leading power factor the load voltage is closer to the supply voltage than a lagging power factor in this application. The cost is higher voltages across both the switching transistors and the capacitor. This must be investigated further.

The efficiency of the system is considered by taking the losses in the semiconductors only. The losses of one transistor are considered because only one transistor conducts at a time. Losses in the transformer and possibly in one diode in the switching arrangement are not considered. The losses are presented simply to highlight the importance of efficiency and how semiconductors affect it. No optimisation is applied for the losses but it is believed they can be improved.

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