ELECTROLUMINESCENT DEVICES VIA SOFT LITHOGRAPHY

A THESIS

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Abstract

This thesis provides a compendium for the use of microcontact printing in fabricating electrical devices. Work has been undertaken to examine the use of soft lithographic techniques for employment in electronic manufacture. This thesis focusses on the use of high electric field generators as a means to producing electroluminescent devices. These devices provide a quantifiable output in the form of light. Analysis of the electrical performance of electrode structures can be determined by their success at producing light. A prospective reduction in driving voltage would deem these devices more efficient, longer lasting and an improvement on current specification.

The work focussed on the viability of using relatively crude print techniques to create high resolution structures. This was carried out successfully and demonstrated that lighting structures of 75 µm and 25 µm have been produced. Microcontact printing has been established as a method for patterning gold surfaces with a functionalising self-assembled monolayer using alkanethiol molecules. This layer is then utilised as an etch resist layer to expose gold tracks for use as electric field generator electrode arrays.

Through careful analysis of each step of the printing process, techniques were developed and reported to create a robust and repeatable print mechanism for reliability and accuracy. These techniques were employed to optimise the print process culminating in the development of each stage and final electrode structures mounted on a rigid backplate for use as electroluminescent devices for characterisation.

These devices were then modelled for their electrical characteristics and investigated for being used in low voltage application. In this case for the development of electroluminescent applications, a driving voltage of 65 V was achieved and represents a significant advance to the field of printed electronics and Electroluminescence.

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Finally, as a man of faith I do believe that any work or discovery made in this thesis is no accident but the revealing of great mysteries waiting for man to uncover. Belief in a creator has allowed me to approach the subject with humility, not expecting omniscience but expecting understanding.

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Glossary of symbols and units:

E_f	–	Electric field,	V/m
V	–	Voltage,	V
d	–	Spacing,	m
C	–	Capacitance,	F
ε_r	–	Relative Permittivity,	
w	–	Base width of electrode array,	m
l	–	Length,	m
n	–	Number of electrodes,	
E_n	–	Energy dissipated,	J/s
V_0	–	Sinusoidal input voltage,	V
R	–	Resistance,	Ω
W	–	Constant, product of □CR,	
ω	–	Angular frequency,	rad/s
ε_0	–	Permitivity of free space,	
A	–	Area,	m^2
y	–	Factor of linear shrinkage,	%
T	–	Temperature,	˚c
U(y)	–	Uncertainty function of linear shrinkage,	%
α	–	Constant,	
β	–	Constant,	
ρ	–	Resistivity,	Ω/m
Ri	–	Initial resistance	Ω
R(t)	–	Resistance as a function of time	Ω
t	–	Time	s
h	–	Height	m
s	–	Speed	m/s
F_{conc}	–	Factor of concentration	
k	–	Coloumbs constant,	
Q	–	Charge in Coulombs,	C
r	–	Distance,	m
P_i	–	Instantaneous power,	W

V_{max}	–	Peak voltage,	V
I_{max}	–	Peak Current,	A
V_{rms}	–	Root mean square of voltage	V
I_{rms}	–	Root mean square of current	A
θ_v	–	Voltage phase shift,	
θ_i	–	Current phase shift,	
t	–	Time,	s
X_c	–	Capacitive Reactance,	Ω
f	–	Frequency,	Hz
P	–	Power,	W
I	–	Current,	A

Glossary of terms:

ACEL	– Alternating Current ElectroLuminescence.
Alkanethiol	– An saturated organic compound containing a carbon bonded with a sulfhydryl terminating group.
Alkylsulfates	– An organic compound with a core SO_4 sulfate group, with an SO_3 terminating group, and organic residue bonded.
Alkylthiol	– An organic compound containing a carbon-bonded Sulfhydryl terminating group.
Angstrom (Å)	– Unit of length used to define nanometres layers.
Bonding energy	– A measure of bond strength in a chemical bond.
cd/m^2	– Candela per square metre is a measure of luminance from a given unit area.
CLF	– Conductive Lithographic Film.
Confocal microscopy	– Optical imaging technique used to analyse 3-dimensional profiles.
COOH	– Carboxylic Acid group, used to bond to the elastomeric stamps.
EL	– ElectroLuminescence.
Etch gradient	– Used to define the contrast between etched an nonetched regions.
HDT	– HexaDecane Thiol, used as a comparative thiol.
Hybridisation	– Process of stabilisation of charges of a functionalising layer.
Hydrophobic	– Nonpolar regions acting to exclude water.
Instantaneous power	– Power supplied at a given point in time from an alternating source.
Interdigitated	– The finger like structures for a 2-dimensional electrode array, forming a capacitive structure.
TOP 200	– Teloscopic optical probe, equipment used in the measurement of luminance.
ITO	– Indium Tin Oxide, a transparent conductor.

MBA	– MercaptoBenzoic Acid, used as a comparative thiol.
MEMS	– Micro ElectroMechanical Systems.
mMol	– MilliMolar concentration of the Alkanethiol thiol in solution.
MUA	– MercaptoUndecanoic Acid, used as a comparative thiol.
PCB	– Printed Circuit Board.
PDMS	– PolyDiMethyl Siloxane, an elastomeric material used to manufacture ‘soft’ lithographic components.
PEL	– Polyelectrolyte multilayer.
PEG	– Polyethylene Glycol.
Phosphor	– A synthetic substance that has the properties of being able to emit light.
Reactive ion etch	– Process used in the manufacture of silicon wafers.
SAM	– Self-Assembled Monolayer, single chemical layer used for functionalising a surface.
SEM	– Scanning Electron Microscope.
SH	– SulphurHydryl group, the terminating group of thiols that bond to gold.
‘Soft’ Lithography	– The name for a group of patterning techniques employing elastomeric stamps. manufacture ‘soft’ lithographic components.
Sylgard 184	– Commercial name for the PDMS(see above) elastomer.
Tinker toy	– A 3-dimensional integrated electronic device.

Chapter 1
Introduction

1.1 A brief history of electronic manufacture

Electrostatics has undergone huge advances and developments throughout the last 3 centuries, beginning with the initial investigation into electrostatics and magnetism. Many of the advancements owe their success to work carried out in the early 18th century initiated by investigation by Stephen Grey who first identified certain materials as those that carried charge, conductors, and those that did not, insulators, giving rise to the 'flying boy' experiment reported in a 1735 publication by the Royal Society, [1], where charge was carried through silk thread to a suspended boy who in turn acquired a static charge demonstrated by manipulating light materials such as paper or feathers. Despite having observed electrostatic forces and magnetism in nature it was this work that harnessed and substantiated the implications of electrical properties, at last the effects were not just observable but their impact was being quantified. This identification of conductors and insulators gave rise to something of a race to utilise the flow of charge, major participants at the time were Benjamin Franklin's research group based in Philadelphia, and Sir Isaac Newton of the Royal Society, who coincidentally blocked the initial publication of the economically poorer Grey's work due to his close friendship with a rival of Newtons and fellow member of the Royal Society, John Flamsteed. In the meantime Franklin et al made significant progress and commercialisation of the process [2].

Electrical manufacture gathered momentum as the use of conductors gave rise to more elaborate components, methods and machines, during much of the 19th century development primarily continued with manufacturing devices and what could be done with these charge carriers and was expressed in the main through the field of communications, resulting in the telephone in 1870 by Alexander Bell, and followed with the radio by Heaviside and Kenelly at the turn of the century in 1901 [3]. At this point there were no drivers for more efficient fabrication methods, research focussed on the outputs rather than the composition of conductions. It didn't matter about scale or consumption, the focus was that it worked. From this

perspective we see an acceleration in electronic manufacture as technologists began to combine assembly and components to optimise manufacture and increase yield, electronics were still constructed by crude methods in a laboratory. Having constructed useable devices and produced reliable components, what investigators needed most was a standardised method of configuring electrical devices to begin to combine their function into more complex systems. At this point a subtle but important shift in emphasis took place, physicists were now looking to make their devices not just functional but efficient, practical and commercially viable. Over the last century or so this has formed something of a pattern in technological development and still continues today. The subsequent pages tracks the logical progression as development occurred focussing not on the device developments and advances but on the charge carriers themselves and therefore circuitry.

1.1.1 Valve-based 'Chassis' systems

Many avenues were explored as the knowledge base broadened and the rise of electronics gained popularity. Although primitive at first integrated electrical systems were assembled and eventually gave rise to the chassis based construction method [4]. This gained widespread popularity with the development of a valve seal in 1919 by W G Houskeeper [5] who developed a method to isolate components using a technique he developed for sealing thin feathered copper edges to glass that allowed for flexibility with expansion and contraction as heat varied, essentially creating an interface between the component and the charge carriers making them interchangeable.

Fig. 1.1 Valve based amplifier

Combining this with the now commonplace chassis design meant different components could be mounted using valve systems, each valve system was then connected using soldered wires attached to the reverse of the chassis, the main benefit of isolation meant components, which were still temperamental, could just be plugged in and replaced as necessary. This became something of a standard for electronic manufacture as it allowed for small and large scale electronics to be standardised especially with a shift from ebonite to the more versatile steel chassis.

Although revolutionary at the time there were still many drawbacks to this system of integrating electronics, the valve based chassis systems were very heavy and confined to installations. They were material intensive generating huge amounts of waste, valves were still unreliable and the use of a steel chassis all combined to make the process laborious and very expensive. With the relative rapid growth of the industry it was necessary to try and improve the reliability of electronics being

produced, minimising waste, improving quality and reducing size to make them more manageable and potentially portable.

1.1.2 Tinker Toy

With the desire for increased capacity and versatility the valve-based design culminated in modular arrays whereby different components were stacked on top of each other forming a 3 dimensional integrated system connected using wires soldered into notches up and down the array. One of the most advanced of these was the tinker toy array developed by the US Navy in 1951 [6]. The tinker toy was developed to reduce size, weight and waste. Modular arrays that still utilised the valve-based system were made. By layering the components it was possible to introduce another degree of complexity to the circuitry, and by using ceramic wafers that were vertically soldered through notches in the wafers, vast increases were made in the usable surface area of the wafers.

Tinker toy had the possibility of including more complex electronics into what had previously been a planar array. This massively reduced the planar design of chassis-based circuit design, which was already being reduced in size to optimise efficiency and maximise the potential of the material. Tinker toy had the possibility to improve the quality and usability of devices drastically. Also the development of modular electronics made it now possible to optimise the valve-based 'chassis' system, and this did happen throughout the 1950's however towards the end of the decade, the modular arrays were being eclipsed by some more exciting technology that was being developed and with the dawn of the transistor that would render the use of vacuum tubes obsolete, component manufacture was taking another turn.

1.1.3 Transistors and semiconductors

With the advances in component technology and construction arrays it had also become apparent that steel 'chassis' construction was a laborious and inefficient process giving rise to the development of the Printed Circuit Board (PCB) which by the 1950's was becoming common place and still forms the basis of our electronic circuitry today. With the reduction of size PCB's became a standard template for

circuit design, this was even more realised as semiconductor materials gave rise to transistors and the advent of microelectronics. At this juncture using semiconductors led to devices being developed on single crystal arrays of germanium and later silicon, the birth of 'chips' integrated circuits (IC) designs with multifunctional devices in one, eliminating the need for vacuum tubes or valves, it was a race throughout the ensuing decades to develop higher and higher functionality using IC design.

With this advancement in technology much attention was now focussed on chip arrays and their capabilities, interest in the basic carrier circuitry had wained leaving much of the electronics we know today limited to the use of PCB's. In the manufacture of electronics it has been largely untapped as the PCB has not until now proved a limiting factor except for novel device fabrication. The limiting factors centre around the physical dimensions of the conductors, certain sensor and capacitive structures could utilise smaller track and gap widths to generate proportionally higher electric fields and increased sensitivity for measurement. A relatively small, lightweight, functional mounting board used in almost all electronics from simple radios to the highest specification supercomputers. However with the need to improve the functionality of even the circuitry and charge carriers, questions around flexibility, transparency, yield and cost are pushing the need for a broader range of fabrication techniques. The author was not ignorant of the use or capabilities of semiconductors but much of the passive component technology can be incorporated into more economical, cheaper and expedient circuit design and research began on manufacturing techniques to reduce cost, improve quality and optimise functionality.

To produce low-cost, high yield and effective electronics, it has been a natural progression to examine the use of print technologies to attempt to achieve this. Frequently this included combining print techniques but more recently has been inspired to attempt printing conductors in an additive process, making the process less wasteful and more effective leading to higher yield and better, more consistent results. Section 1.1.4 and 1.2 detail the unfolding of print technologies to try and optimise the circuitry properties since an initial publication in 1956 [7], success and limitations of the respective processes are identified and discussed below.

1.1.4 Current circuit boards

The concept of circuit boards dates back to the turn of the 20th century as electronics gained popularity and commercial appeal. The earliest constructions although crude and often unsightly were effective, utilising a carrier material that could range from ceramics to wood. Brass wire was then riveted to holes drilled through the material, the system of holes then acted as holders for components that were then mounted using valve systems to make electrical connection between component and wiring. Later the method was adapted to take advantage of the double sided nature of the mounting boards, components on one side and increasingly complex wiring on the reverse. A method that would eventually give rise to the concept of embedded electronics, circuitry in a multilayer array providing a huge surface area for a small volume of material, some of this progression is discussed by Kirstie Petheridge et al. [8].

A breakthrough came in 1956 when the US Patent Office granted a patent to a small group of scientists titled 'Process of Assembling Electrical Circuits' [7]. The description of which involved photographing a circuit design onto a Zinc plate for use in Offset Lithography. The Offset lithographic process was then used to print an acid resistant masking layer onto copper foil mounted on a rigid substrate. An acid etch removed the unmasked copper foil giving rise to conductive tracks of copper layered on a rigid backplate. This process has been refined and redefined but essentially this process still makes up the vast majority of circuit fabrication available today. Methods beyond Offset Lithography have been developed for the deposition of the masking layer however much of the focus has been on removing the masking and etching process altogether and to leap directly to printing conductive inks, and for the most part successfully.

The most prevalent method using copper foil and chemical etching is a subtractive process and inherently wasteful, despite the several manufacturing steps to arrive at a finished product, including a final processing step to cap the copper tracks to prevent them oxidising. This well documented process has a common flaw and that is given the chemical etching process the track and gap spacing achievable is limited to approximately 100 µm for optimal performance. Widths below this run into trouble

with bridging due to the isotropic nature of chemical etching leading to under etching, also a common problem at these dimensions is the tin coating applied to the copper, a process which itself can lead to the joining of tracks and bridging. A method that has arisen to eliminate these issues is the use of Photolithography, providing a higher resolution due to use of UV light to cure a photoresist deposited on the surface.

1.1.5 Research question

Given the limitations of current manufacturing techniques, it was suggested that a novel fabrication of conductive material can accomplish several goals. Electrical design is constantly evolving, a significant driver has been the desire for smaller packaged circuitry. As the circuit architecture becomes increasingly small, we encounter several problems with many of the current novel methods for printing conductive material. There are electrical complications as fabrication moves towards this goal. The most significant issue is conductivity, as conductive deposits reduce in volume their conductivity diminishes. Section 1.2 explores the diversity of manufacturing techniques as they pertain to smaller circuit geometry.

1.2 Diversification of manufacturing methods

1.2.1 Photolithography

This method of printing electronics utilises a UV curable photosensitive layer to pattern the circuit design. The earliest systems were essentially comprised of a polymer backplate, overlaid with a conductive layer finished with a photoresist. Beyond these elements increasingly complex manufacture has been used to aid the physical properties. The circuit design is typically masked whilst the resist is cured by exposure to a UV source and then all waste is stripped away using an etch solution, the final product is then reacted with tin to cap copper tracks providing good conductivity, whilst minimising the effects of oxidation.

This process is highly successful and constitutes a significant portion of the circuit fabrication market. Photolithography has been established as a reliable method for printing circuits however there are occasions at which photolithography cannot

sustain the demands required. The most apparent limitation with regard to this thesis is that conductivity diminishes with track and gap spacings below 80 µm.

The resolution of the process is currently a limiting factor. Light modelled as a wave undergoes diffraction as it passes through narrow gaps, the UV light used to cure the photosensitive layer is no different. Where diffraction occurs and light scatters beneath the mask, a portion of the masked track is rendered useless due to under etching.

Using the process described a level of success was achieved at a track and gap of 80 µm as illustrated below but this is still not the resolution desired and at present there is no suggestion of progress from this point. Oxidation is also a problem with the process, once printing at higher resolutions the volume to oxidation ratio is much higher so the tracks oxide rapidly with little opportunity to coat them with Tin, this can be overcome using a vacuum chamber but this is expensive and time consuming, and still doesn't solve the track and gap spacing problem.

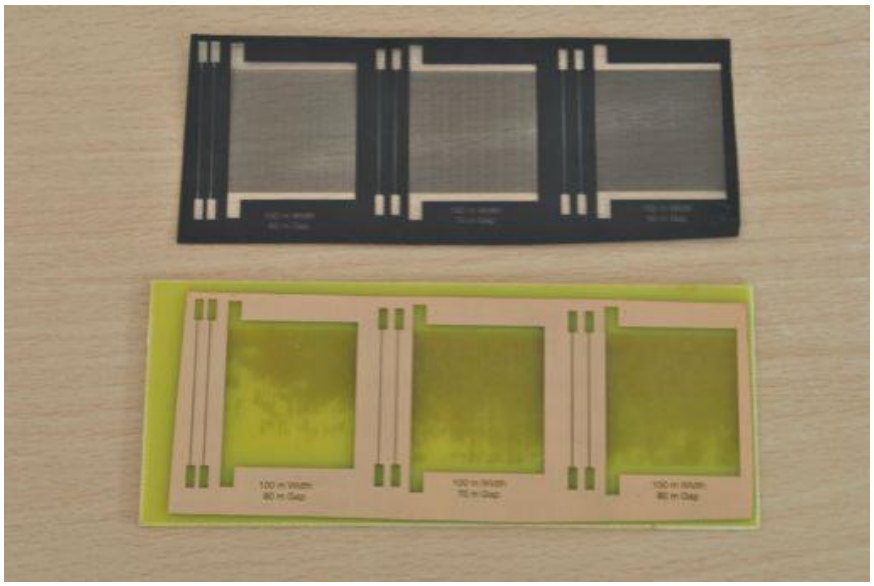

Fig. 1.2 Various arrays fabricated by Photolithography. All arrays with 100 µm tracks but 60 µm (left), 70 µm (centre) and 80 µm (right) gaps.

As reported in by P. Mendes et al. [9] hypothesised a method for depositing gold nano particles utilising a combination of photolithography and alkylthiols. An alkylthiol is deposited over the surface of a substrate before UV light is irradiates the

molecules through a mask. The UV light oxidises the alkylthiolates to form alkylsulfates. This leads to depassivation and coagulation of the gold particles. Finally the surface can be rinsed of excess stabilised molecules to reveal coagulated gold nano particles.

Nanopatterning, as demonstrated by P. Mendes et al. [9], combines photolithographic techniques with alkylthiols to produce, gold features of the order of 60 nm. These features are believed to be porous and problematic for conductivity [9]. They do however demonstrate that with subsequent processes, these gold features could be used for a variety of applications, including as seeding layers on which to lay further conductors.

1.2.2 Screen printing

The process of screen printing has also been developed for use with primarily conductive inks. The screen printing process has long been established as a tried and tested process for printing especially graphics but also text and more recently electronics [10]. The method uses a woven mesh with a photo emulsion cured over the surface, the desired print is masked and left uncured, the excess photo emulsion is washed from the surface leaving an exposed mesh through which an ink is passed.

The process is additive unlike PCB manufacture, meaning only the necessary ink is laid down creating minimal waste. A variable that determines the success of the process is the particulate size, this is crucial for printing conductive matter as the ink must contain a certain critical solid particulate to enable conductive properties. For this reason the mesh count must be sufficiently low enough to allow relatively large particulates to pass through, this however introduces a fundamental problem of dot gain, this is caused by a wider gap between the mesh threads allowing too much material to pass through and widening the track resolution. Given that this is a random process dependent on impurities on the substrate, it is hard to predict and therefore unreliable to introduce as a tolerance to the process. The most significant advantage of screen printing is the ability to take an array of materials and manufacture inks to print different conductors for different functions. However even

with the developments there still is the issue of resolution being limited to about 100 µm track and gap for an electrode array. Screen printing is also a slow process allowing only a single pass at a time. Methods for increasing print area combat the yield however they do not maintain the reliability required.

1.2.3 Offset lithography

The printing process of offset lithography has been developed over decades of careful research to mechanise a process that is repeatedly accurate and reliable. It has the capacity to print at high volumes, whilst trying to print at smaller volumes is uneconomic with many offset lithographic presses. The process has been used for the reproduction of literature and graphics with the capability to lay colours down in stages, larger presses use 4 or more print stages to lay colour down.

Until the early 90's the process was written off as a method for printing electronics due to the large shear forces introduced with the use of mechanised rollers. The rollers rotate at different speeds, and are designed to shear the ink to lower its viscosity when passing through to the substrate. The offset lithographic process utilises a printing plate comprised of hydrophobic and hydrophilic regions, the ink is solvent based and therefore adheres to the hydrophobic areas and is repelled from the hydrophilic areas that are coated with water due to a water bath passed through a separate set of rollers to the plate. Again this process is additive in that only ink transferred to the plate is laid over the substrate, this improves the efficiency of the process and reduces the waste, however due to the use of substantial equipment the waste is scalable, so the larger the print run the inversely proportionally small the waste will be.

This work is significantly contributed to by research that has been carried out over the previous 15 years by The Cleaner Electronics Research Group, the drive behind this work is to develop new and novel techniques for printing, this has been most notably advanced through the development of conductive inks for use with an Offset Lithographic Press [11]. The group have a Heidleberg GT46 press that has been used primarily for this work and continues to be used as the development of printed electronics advances, the major achievement of this group has not stopped at

printed circuitry that can rival current Printed Circuit Board (PCB) manufacture, but also has developed printing techniques for a range of components including, resistors, capacitors. Flexible microwave applications were also reported in [12] and [13], despite the performance their flexibility offers a range of possibility not previously achieved. Integrating the manufacture of CLFs has even resulted in a fully functional printed thermometer.

One recent conductive offset lithographic printing advancement was the capability to print electroluminescent displays for the use in advertising [14]. Previous electroluminescent displays consisted of a five stage layered approach, using Conductive Lithographic Film (CLF) it is possible to reduce this to a two layer structure [14]. First a capacitive electrode array structure is deposited and then a phosphor luminescent ink layer is coated over the surface. Due to the fragile ink layers it is difficult to build up to three dimensional structures on such a small scale.

1.2.4 Inkjet

The most successful consumer electrical product with regard to printing is the inkjet printer, for many it brought the reality of home printing to a competitive level with industry. The technology itself is relatively simple in principle, much like a pen, there is a head or nib, through which the ink is passed to direct the pattern being created, there is a reservoir where ink is stored until it is ejected onto the substrate. Most homes have access to an inkjet printer demonstrating their success. However to print conductive material introduces complications that industry are only just getting to grips with.

In order to print conductive material it is required to print particulates that can carry charge. Inkjet printing at present relies on a liquid ink however to print conductive material. Capabilities must be improved to print solid particles in a liquid carrier, this has been achieved primarily through widening the print head [15]. This provides the diameter for the flow of particulates through the head onto the substrate. Increasing the exit on the print head increases the flow onto the substrate and therefore the rate of dot gain increases, and when considered for track and gap spacings, widens the track.

1.2.5 Flexography

Flexography utilises a flexible relief plate when printing, it is effectively a more advanced letterpress process, inking the printing plate to then transfer ink to the substrate. Key stages are the feed section, often reel to reel, providing tension in the substrate as it passes through the press, and slightly more critical is the plate manufacture that has attracted much attention to improve on current limitations [16]. Also the print section is ideal for printing large block regions of colour making it ideal for packaging, using an arrangement of different print plates it is possible to build up a pattern in one pass. Finally the rewind at the end of the process also helps maintain tension in the process but also must allow for sufficient air flow to dry the ink.

Given that the process is a block printing method on a large scale, resolution is a problem especially given the flexible nature of the plate meaning impurities can affect the pressure and distort an image which on a scale of 10 µm can destroy print quality. It is rarely used to print detail patterning given the resolution problems. This problem doesn't include the difficulty of photolithography resolution to print the plates in the first place. Although extremely effective at printing unfortunately the resolution remains a problem limiting effectiveness to about 100 µm track and gap even when a press is optimised to the highest specification.

1.2.6 Gravure printing

Gravure printing is an established technique and utilises the recess structure of a patterned printing plate to hold ink before the plate and substrate are brought into contact. Pressure between the plate and substrate allows high control over the ink deposited providing very accurate resolution and print capabilities, due to the ink being held in the recess of the plate it requires only small amounts and therefore is ideal for fine resolution printing [17].

The main drawback with gravure printing is the small volume of liquid needed to print, this balance is very hard to perfect and often leads to track breakages, due to

small volumes of ink, or dot gain where the track expands, due to the volume of liquid expelled being too large.

1.2.7 The benefits of smaller geometry

The variety of methods explored for manufacturing circuitry all run into difficulty when they are applied to real world applications. Whether it be physical capacity of the machinery, or conductive properties of the deposit. Frequently, research attempts to take an existing process, which is already operating at capacity, and extend the reach of the process into ever shrinking results. Whilst this can and has yielded results, the manufacturing processes are already then operating at or near their capacity. This proved a costly and slow process. Could novel manufacturing provide a cheap reliable method for fabricating circuitry? Using a process that is known to perform at sizes well below the required geometry, is it possible to transfer that knowledge to printing conductors?

The benefit of producing conductive feature sizes below what's currently possible are useful in many areas, not just research. For electronic devices, a reduced circuitry could lead to more inclusive circuit design. Instead of having to load a circuit board with additional components, feature size could be used to print a range of components from resistors to capacitors. Further to this goal, circuitry could be designed to integrate with more complex components, but providing battery electrodes or LEDs. This integration of circuitry could lead to designs interacting with their environment, for applications such as sensors.

For many sensor devices, feature size can be directly correlated to sensitivity. An example of this is in the use of thermistors. According to the second law of thermodynamics, 'the passage of heat', heat 'flows' from a hotter to a colder body. A thermistor device, a temperature sensitive resistor, responds to heat in its environment. The smaller and more localised the environment the more sensitive the device can be to heat disturbances. Heat will also dissipate to the environment surrounding it and therefore a smaller device can provide closer proximity to the heat source to respond accordingly.

Smaller feature size can also be utilised for micro battery production. At present electrochemical cells rely on the interaction between terminals and the interface they create with an electrolyte. Conventional batteries employ two large electrode terminals wound round one another using a porous insulating membrane to create a large surface area interface. Using reduced electrode geometry those terminals could be printed with a narrow gap leading to a large interface region, the substrate used for mounting could provide the structure without the use of complex separators, allowing electrolytic chemicals to make direct contact with the electrodes.

These are just two examples of how reduced feature size could improve the performance of devices.
Exploration for an accessible process with potential for manufacturing feature sizes at the sub-micrometer scale was the next endeavour.

1.3 Novel fabrication employing soft lithography

Soft lithography is a category of print techniques that emerged in the early '90's and is continuing to emerge with new techniques being added [18]. The field was largely developed in response to the growing demand for high resolution features that is limited at present by standard industrial methods. It is lithographic in the sense that regions on a plate face are inked respective of the desired print finish, the 'soft' refers to the elastomeric material frequently used as an ink carrier. Due to the high resolution and surface chemistry these techniques have found great success in the area of signalling proteins and the development of immunoassays, DNA fingerprinting and other biosensor applications [19].

Soft lithography is unlike other methods of printing in that it generally operates on the micron and sub-micron scale. There are several established techniques with more evolving all the time. They can broadly be categorised into three groups: moulding, embossing and printing [18].

A few research groups have begun development in the area of harnessing 'Soft Lithography' for use in electronics. There is more on this topic in section 2.2 however, suffice to say Microcontact Printing is the most successful for this purpose.

Due to its relative success in this area when trying to print conductors attention will focus on an analysis of Microcontact Printing as a suitable method for printing electrical components. Given the title it is self evident that prints occur on a micro scale. The methods were developed to overcome the limitations of other print methods at that scale. The method is subtractive similar to Photolithography meaning the print components don't carry metallic particulates, which can be difficult to manipulate. Instead the print plate is an elastomeric polymer and the ink a single molecular compound. Due to surface chemistry a single monolayer of an alkane-thiol can be deposited to act as an etch resist layer and pattern a metallic substrate. Etching reveals the conductive pattern allowing for accurate, high resolution features at the micro scale that conduct electricity.

1.4 Specifying EL displays for quantifiable outcomes

The objectives of this thesis are to demonstrate the potential use of microcontact printing in printed electronics. This will be achieved in part by demonstration of microcontact printing as a means to produce electronic circuitry and components. This will be observed most notably by development in the area of electroluminescent displays. Electroluminescent displays have not previously been manufactured by the use of microcontact printing. This will contribute novel development in the printed electronics field. A two-stage manufacturing process for producing electroluminescent displays was developed by The Cleaner Electronics Research group using an interdigitated electrode structure as outlined by Kilhan kim et al [20]. This was accomplished using offset lithography as reported in [10] and overcame the need for the industry standard five-stage manufacturing process. Incorporating the advantages of this technology. This research aimed to produce a functional electroluminescent display via microcontact printing. The device will overcome a common problem with electroluminescent displays which is the relatively large field, around $1x10^6$ V/m, that needs to be supplied in order to stimulate phosphor particulates to emit light.

From prior research, offset lithography is a technique that can be used for printing functional electronics on flexible media. Dependent on the surface roughness and porosity of the substrate multiple passes are often used to build up an ink layer. By

using less porous and reduced surface roughness, the number of passes required can be reduced and in certain circumstances only one pass is necessary to ensure a conductive layer is deposited.

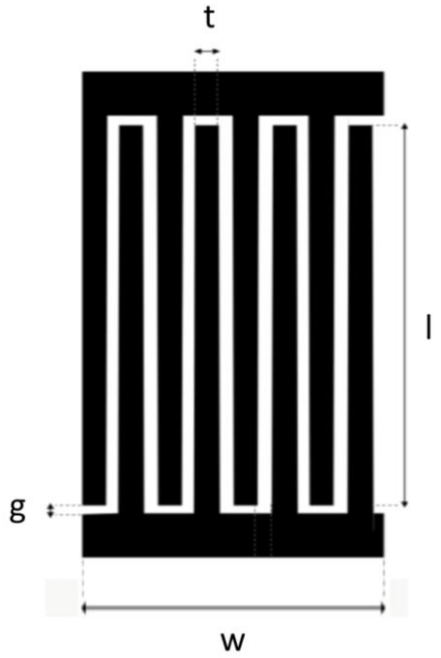

Fig. 1.3 Geometry of an interdigitated electrode array displaying the various dimensions: t = conductive track width, g = nonconductive gap spacing, l = length of electrode producing electric field and w = the width of the base of the structure.

This layer can be used to print the desired electrode structure array for generating a high electric field. Using offset lithography, reliable feature sizes of 100 µm track and gap have been produced. Conventional calculations for the electric field suggest using a stimulating voltage where V_{rms} = 110 V coupled with a spacing of d = 100 µm produces the following theory:

$E_f = V/d$ (Eq. 1)

$E_f = 110/100x10^{-6} = 1.1x10^6$ V/m

A field of around $1x10^6$ V/m is required to stimulate phosphor inks [21]. The model above runs into limitations as we try to decrease the driving voltage. The only other solution is to scale down the geometry of the structure. Given the direct proportion relationship between the voltage and distance, by reducing the electrode spacing

then the driving voltage should similarly be lowered. It can be seen that to produce a field as before of $1.1x10^6$ V/m, and therefore calculated:

$E_f = V/d \Rightarrow V = E_f d$

$V = 1.1x10^6 \times 10x10^{-6} = 11$ V

With previously discussed methods at this scale conductivity issues present themselves using current print technologies. Whether they be introduced by the surface roughness, oxidation of metallic tracks or limitations of the print techniques. Furthermore, as the scale of the electrode structure decreases another limitation presents itself. Uncoated phosphor particulates used for the emission of light are limited to a size around 7 µm in diameter. Uncoated phosphors have significantly reduced lifespan and 'off-the-shelf' coated phosphor particulates are currently optimised at approximately 25 µm. This field is constantly evolving with new products being developed. Hence, with the track and gap spacing being reduced to 10 µm structures can be manufactured to utilise the optimal properties of current phosphor powders.

Fig. 1.4 Offset lithographically printed electroluminescent display. The array has 100 µm track and gap spacings producing a field of $2x10^6$ V/m^2 at an operating voltage of 200 V [21].

The display illustrated in Fig. 1.4 was fabricated using Offset Lithography. The panel display is composed of an interdigitated (see section 1.4.2) electrode array overlaid with a Cu doped ZnS phosphor ink. The theories of Phosphor ink and interdigitated electrode manufacture underpin this construction. Soft lithography will look to replicate the electrode structure, whilst the phosphor ink formulation is adapted from the offset lithographic process [21].

1.4.1 Phosphor theory and ink formulation

Phosphorescent materials can be used to emit light. Electrons can 'fall' from the conductive band to the valence band within the electron configuration and in so doing, energy is emitted as light. A common semiconductor material used for this application is ZnS which typically has a band gap dependent on the particular bonding structure. Cubic forms have lower band gaps around 3.54 eV, whilst hexagonal structures have greater band gaps in the region of 3.91 eV.

ZnS can be doped with a metal to introduce intermediary energy levels that aid the movement of electrons, the release of energy and therefore photon emission. ZnS:Cu produces a blue/green hue and is commonly used in Electroluminescent displays as in Fig. 1.3. According to M. Warkentin et al, 'it is understood that ZnS:Cu relies on Cu precipitating at thin needlelike Cu_xS defects' forming a reliable p-type semiconductor, [22]. As a p-type semiconductor the holes provide the majority charge carriers. An applied electric field is thought to be concentrated at the tips of the Cu_xS defects, injecting holes and electrons into the host lattice from each end of the defect. It is suggested that the electrons are captured leaving holes trapped at the opposite end of the defect. Critically, when the ac voltage changes, the internal field reverses and so to does the injection. When electrons recombine with trapped holes luminance is produced.

Given the nature of the injection at either end of the defects a charge build up is observed. This gives rise to the formation of distinct electron-hole regions, which alternate with the cyclical nature of an ac voltage. When the voltage is delivered and the electron-hole arrangement formed, the Cu_xS defect can be thought of as

responding to the field produced by opposing electrodes, and thereby thought of as responding to a capacitive device.

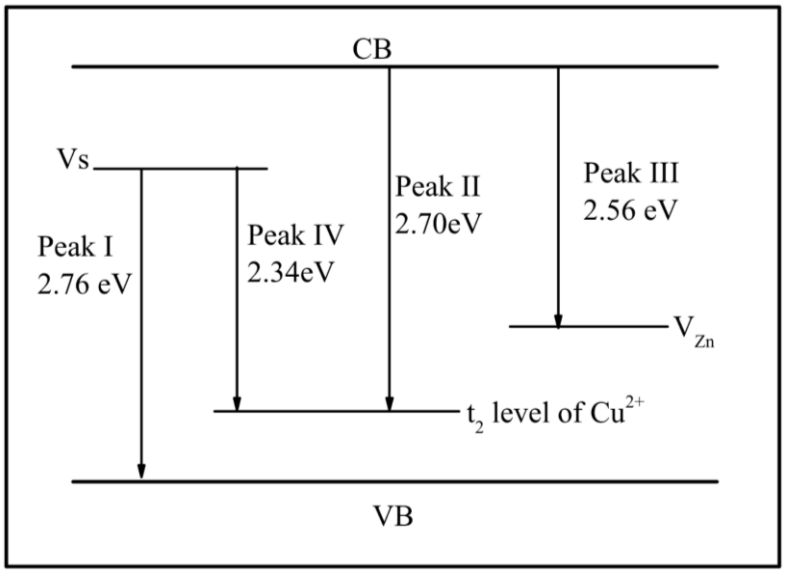

Fig. 1.5 Schematic energy level diagram showing the emission mechanism in ZnS:Cu nanoparticles, by J. Hasanzadeh et al. [23]

An example of ZnS:Cu energy levels is reported in [23] and detailed in Fig. 1.5. From the energy level diagram it's observed that electrons can fall between a combination of energy levels. Each movement electrons make towards the valence band emits energy. Introduction of intermediary energy levels means electrons are required to emit less energy to 'fall' to a lower energy state.

The Phosphor material is often turned into an ink using a resin binder mixed with a solvent. As the solvent dries the phosphor ink is deposited over a substrate and when an alternating current is supplied the particulates emit light. The quantity of ink is significant. Too many particulates will obscure some of the glowing material underneath, whilst too few particulates will not optimise the field produced leading to potential holes. Ink formulation was carried out by Brunel university when producing electroluminescent displays by Offset Lithography, this work is detailed in the paper by R. Withnall et al., titled 'Low Cost, Flexible Electroluminescent displays with a Novel Electrode Architecture Printed by Offset Lithography'[21]. The ink formulation was translated to the work contained in this thesis. It was known as a reliable method for aligning phosphor material in the space between interdigitated electrodes. As a solvent evaporated from the resin bound ink a phosphor particulate

layer is left across the surface of the structures, leaving a phosphor layer of around 100 µm. Screen printing was employed after the Offset lithographic process was used to lay down the initial electrode structure with relative success. The method of deposition over the surface of a micro electrode structure employed a mask. The frame would suffice for an initial deposition of between 30 µm - 50 µm and investigation of such a small area of examination.

1.4.2 Interdigitated theory

The second theory underpinning this experimentation is that of the interdigitated electrode array. Interdigitated electrodes are capable of providing the required electric field to stimulate the Cu_xS defects to enable them to emit light. The field produced can be related to the voltage and spacing between electrodes as defined in Eq. 1, by reducing the spacing an increased field across the phosphor material increased the localised field within the defects. By reducing the size of the electrode architecture a reduced voltage can be used to produce the stimulating field.

Capacitive structures typically are composed of two parallel plates spaced evenly apart with a dielectric separating layer that acts to insulate and ‘carry’ field between electrodes. For interdigitated arrangements, a planar array is created with electrodes positioned side by side. There are three main concerns relating to traditional capacitive structures: the location of the field is hidden, the electrodes are typically constructed of non transparent material and there is an increase to the stages of processing.

For many applications to have the field concealed between parallel plates does not pose a problem, but this is not true for sensors and indeed Electroluminescent displays. In these devices the field’s interaction with it’s environment is often the effect needed and for Electroluminescent displays the fields effect on the phosphor ink is the effect to be observed. This leads onto our second issue with parallel plate capacitors, the fact that conductors are typically not transparent and therefore will not allow light emitted by the phosphor particulates to pass through. The common solution to this problem is to use Indium Tin Oxide (ITO), a transparent conductor. Given its unique qualities, ITO is expensive and for larger arrays this makes them

inefficient. Lastly, when constructing parallel plate capacitors there are several stages to manufacture: two plate layers, dielectric, separators and mounting, as well as registration complications. Depending on the applications interdigitated arrays can use the same stage for both electrodes and separator applications, especially when printed directly onto a rigid substrate. This makes the process cheaper and more efficient.

It was considered that a parallel plate capacitive device would provide sufficient theory for adaptation into a interdigitated array. Opposing plates could be thought of as spaced into linear conductive features, as the spacing between the linear features of a plate increased the distance between the plates becomes less critical. This however did not suffice for two reasons: adjacent electrodes and therefore field produced acted to superimpose on one another and given the nature of thin film plates the field produced originated from the edge of the electrodes rather than across the whole surface of the plate. Field can no longer be thought of as vertically uniform between two parallel plates and therefore across the whole area. Now according to the architecture described in Fig. 1.3 the field produced occurs horizontally between electrodes. A different model was required for interdigitated electrode arrays based on the alternative geometry.

Interdigitated arrays have been explored fairly comprehensively with a standard equation to work out the capacitance of structures using an equation based on the area of the array, number of fingers and track and gap width. As published by J. Hector through RF wireless circuits [24] the formula for measuring interdigitated capacitance is detailed as:

$$C = [(\varepsilon_r + 1)/w] \times l \times \{[(n - 3) \times 0.089] + 0.1\} \qquad \text{(Eq. 2)}$$

Where: ε_r = Relative permittivity, w = base width of electrode, l = length, and n = number for interdigitated electrodes.

Using this equation to measure capacitance, theoretical calculations can be made as to the expected capacitance for various dimensions and therefore a range of

structures suggested that would meet this criteria. Eq. 2 was employed for a range of structures as detailed in Table 1, 2 and 3.

This formula is largely trusted and employed by Rui Igreja et al in their paper 'Analytical evaluation of the interdigital electrodes capacitance for a multi-layered structure' [25] to characterise their own interdigitated structures before characterising a variety of sensor materials deposited over the electrode structure.

1.5 Alternating Current Electroluminescent Displays (ACEL)

Electroluminescent (EL) displays rely on the supply of an alternating current (AC) to provide a constant field within electrode spacings. Work on alternating current electroluminescence (ACEL) displays has been explored to try and understand the relationship between, voltage, frequency, capacitance and how this affects the energy dissipated in EL displays. This work has focused on a more traditional layered structure approach using a parallel plate capacitor, spaced at 30 µm. Coated ZnS:Cu at a size of roughly 25 µm were arranged over the surface of a bottom electrode forming a single particulate layer. Chris Winscom has published several papers on the matter and has built a model for determining the energy dissipated when the phosphor particulates are stimulated to emit light. The following formulae was reported in 'Equivalent Circuits and Efficacy of Single-layer ACPEL Devices' by C. J. Winscom et al. [26]

$E_n = ½ \times (V_0^2/R) \times W^2/(1+W^2)$ (Eq. 3) And: $W = \omega CR$ (Eq. 4)

Combined suggests:

$E_n = ½ \times (V_0^2/R) \times (\omega CR)^2/(1+ (\omega CR)^2)$ (Eq. 5)

This work provides helpful background but also a useful comparison. The layered approach is limited by the particulate size and has direct consequence on the geometry of the final EL display. By using an interdigitated array with a high

resolution process, it is possible to reduce the feature sizes to a few microns and even sub-micron.

By using theoretical values for capacitance, and energy dissipated, work was conducted to measure the performance against current Electroluminescent displays. This combined background work provides a solid basis for investigation into the use of alternative manufacturing techniques, most notably in the area of reducing electrode geometry. With the many fabrication processes discussed in this chapter resolution becomes a problem when looking to construct conductive electrode arrays below 100 µm. For those techniques that can achieve very fine feature sizes, due to the precision and low yield, cost becomes a deterring factor.

1.6 Plan of work

Work commenced by identifying the use of soft lithographic techniques as a possible source for printing high resolution electrode structures for a range of applications. Similar structures have been used to fabricate electroluminescent display [21]. Identification of the preferred method for printing was first established. This was investigated by evaluating the range of soft lithographic techniques available and their strengths and limitations with respect to printing conductor materials. This work continues in Chapter 2.

1.7 Chapter Summary

Given the initial study and analysis it has been observed that the most appropriate method for printing high resolution conductive features at a scale of 10 µm is to use the soft lithographic processes. This study will be pursued in chapter 2, the various processes will be looked at in further detail and conclusions made on the present uses, limitations and optimisation of the capabilities for industry.

This work will also begin to focus on an application for which higher resolution features are directly beneficial and that being an area of research that has long been established, and that is Electroluminescent displays [14] [21]. The most significant benefit of higher resolution features is their sensitivity. Where two tracks interact, the

smaller the gap and the greater the proportional differences between them will be. Soft lithography has the potential to print fine lines to a resolution even on the sub-micron level increasing the potential for incredibly sensitive devices.

Chapter 2
Literature review

2.1 Established limitations

It was established in the preceding chapter that current electronic manufacturing techniques, whilst widely employed, have limitations. These include:

1. Relatively low resolution for an electrode array, with a reliable track and gap spacing of around 100 µm, best case 75 µm.
2. Problematic conductivity, due to pinholes and surface roughness dependent on process and geometry.
3. Several passes frequently required, introducing multiple steps and leading to registration problems and track widening.

Having previously reviewed circuit fabrication strategies and identified certain limitations, it was necessary to consider alternative methods that deviated from conventional methods but did not introduce further difficulties in processing. A common thread through recent developments in circuit fabrication has been the use of printing to pattern substrates (e.g. with an electrical conductor) before it then undergoes subsequent processing to lay down other electronic components.

As discussed in section 1.3, one possible solution to some of the present limitations of circuit fabrication is the use of soft lithography, an emerging field focusing on the use the polymer elastomers for different print applications. Much of the success of soft lithography is in the application for MicroElectroMechanical Systems (MEMS) technology for biosensor arrays especially where there is a need for high resolution features. Soft lithography was established in the mid 1990's by G. M. Whitesides et al [18]. Currently within the field of soft lithography there are several main processes that have emerged and are most commonly used for micro/nano fabrication depending on the applications required. These utilise the expertise from three fields: moulding, embossing and printing. Given their characteristics, not all of these can be used for electronic application. With most of these applications there are still

problems with resultant charge carriers even once an initial relief or patterning has occurred.

Soft lithographic processes largely use the same basic components in various configurations to achieve specific but varying results. Of these processes microcontact printing is the most efficient process at forming conductive tracks on the surface of a substrate. Below is an introduction to the main processes and their drawbacks with respect to patterning conductors.

2.2 Soft lithographic techniques for moulding

In replica moulding, a substrate is patterned using the physical properties to form structures of varying size, shape and functionality [27]. Sections 2.2.1 and 2.2.2 outline the most commonly found forms of moulding in soft lithography. There is much potential to use moulding as a form of fabrication technique that could produce high definition, well structured relief profiles in a substrate.

2.2.1 Micromoulding in capillaries

This process uses the action of capillary flow of fluids through a capillary section. An elastomeric stamp is brought into conformal contact across the surface of a polyelectrolyte (PEL) substrate creating capillary tubes due to a profile structured on the stamp [28]. The contact is critical to ensure appropriate pressure for capillary action. A UV curable solution of polyethylene glycol (PEG) is then deposited and works its way through the voids until all capillaries are filled and the structure is exposed to a UV source for curing. The stamp provides a transparent relief carrier to allow light to pass through and cure the material. The stamp can then be removed to expose a relief pattern across the surface of a substrate. This process is best used in cathode electrode separator applications in devices like diode arrays [29].

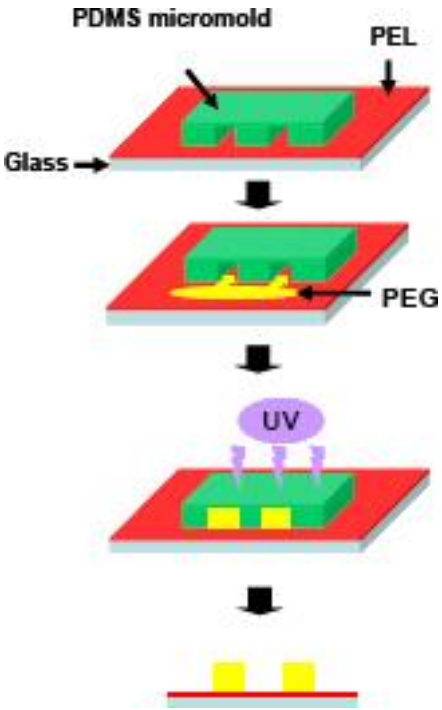

Fig 2.1 Demonstration of micromoulding in capillaries, by Chang-Soo Lee et al. [29] Capillaries formed by an Polydimethylsiloxane (PDMS) elastomeric micromould are used to align Polyethylglycol (PEG) on a polyelectrolyte (PEL) substrate before being UV cured.

2.2.2 Solvent assisted micromoulding

Solvent assisted micromoulding uses a PDMS stamp to create an impression in a resin solution based substrate that can then be cured by evaporating the solvent [30]. As the solvent from the resin is evaporated, the precursor reduces to a cured resin structure mounted on a back plate.

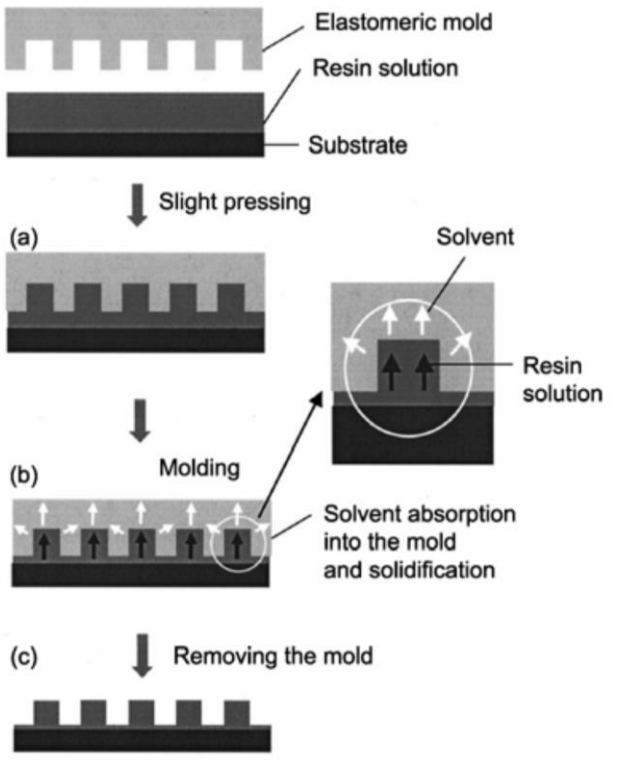

Fig. 2.2 An example of replica moulding and solvent assisted micromoulding combined by Han LuLu et al. [31] An Elastomeric stamp, typically PDMS, is used to mold a resin solution. The solvent in the resin is then absorbed to cure and solidify the resin to create the micromolded features.

2.2.3 Limitations of moulding techniques

Moulding is a very precise and robust fabrication technique with a significant drawback. To lay down conductive tracks with either method above requires a further manufacturing step or significant manipulation of the process itself. The methods are improving constantly and making advances. However, the use of conductive material is imperative to certain applications as discussed later. There is no doubt that a wide range of feature sizes can be fabricated leading to significant applications but they are characteristically physical applications rather than electronic [31].

2.3 Soft lithographic techniques for embossing

Embossing is the process where contours are established across the surface of a substrate and this physical relief can then be utilised to differentiate various functional regions. The biggest drawback with this process is then deposition of conductive material as described by M. Heckele et al.[32]. Application of a conductor preprocessing presents two significant problems, the oxidation of metals and structural properties of suitable metallic substrates. Oxidation or chemical reaction with air to form sulphites or carbonates typically hinder conductivity. With various metallic substrates, such as, with gold are largely ductile and readily drawn into wires and therefore malleable enough not to be fractured when embossing, leaving a conductive film over the surface. Application of a conductor after the relief has been formed also poses challenges. Highly specialised mechanisation is often required, coupled with the relatively low surface roughness making the deposition process very delicate. The most established of these techniques is soft embossing, for which a brief introduction is given below.

2.3.1 Soft embossing

In soft embossing a substrate is coated with a material susceptible to manipulation, usually in the form of heat. An elastomeric stamp is brought into contact and pressure applied while the deposited material is manipulated to fill the areas of relief on the stamp [33]. The final step involves cooling the system, whilst pressure is continually applied. In doing this the structure 'freezes' into its new position. As a result soft embossing can create micron sized features, however the primary drawback with this process is that material remains in the troughs even where the stamp has depressed the initial surface. This leaves conductive material across the entire surface not clearly defining regions of conductivity and non-conductivity. The nature of the embossing process also suggested that the deformation is not linear across the surface as pressure is applied to the reverse of the elastomeric stamp [33].

2.3.2 Limitations of embossing techniques

Given the nature of embossing and its performance at forming a contoured relief pattern across the surface of a material it poses several issues when it comes to laying down conductive tracks. The relief itself does not deposit conductive matter unless the substrate used is conductive, but even in this instance there is a continuous conductive film without a defined track and gap electrode spacing. This is due to the relief structure not expelling material from certain regions. One solution to this is to cap a nonconductive contoured relief pattern with a conductive material through adhesion or another deposition method. The fundamental problem with this is the scale, at a track and gap profile below 100 μm it is hard to maintain reliability with deposition of conductive material, except for the use of high resolution, low pressure systems to maintain accuracy and not deform the contoured pattern in the process [34].

2.4 Soft lithographic techniques for printing

Printing has a variegated and established methodology, involving the patterning of a substrate. This subcategory of soft lithography is no different, involving the standard components of print face, substrate and ink. Soft lithographic printing relies critically on chemical interaction rather than physical properties for pick up and put down, such as those frequently found in use for typography.

2.4.1 Microtransfer printing

With microtransfer printing a master structure is relocated from a native to a target substrate [35]. This employs differing bonding energies to transfer ink, bonding first to a stamp and then utilising a higher bonding energy with a substrate for deposition. This process can transfer conductive materials from one location to another, however conductivity is difficult to maintain as it is transferred. Also for the purpose of fabricating conductive tracks, transfer is also necessary. Research has been reported into the use of microtransfer printing for display applications, and the process involves layering *n*-GaN and *p*-GaN on a silicon wafer before gold is used to form a bridge with the *n*-GaN layer through the *p*-GaN layer before a final gold layer

is masked and the desired pattern anisotropically etched on the silicon. PDMS can then be used to bond with the gold and transfer the pattern to a flexible substrate in this case, before being configured into GaN LED array [36].

2.4.2 Microcontact printing

Microcontact printing is almost a step back from microtransfer printing in that the facilitator is not looking to relocate any deposited material but to establish an initial conductive pattern on the substrate. Microcontact printing utilises an alkanethiol ink that is deposited using a PDMS stamp onto a conductive substrate. This monolayer undergoes hybridisation forming a self assembled monolayer (SAM) which can be used to functionalise regions for further experimentation [37]. The alkanethiol terminates with a COOH (carboxyl group) and can therefore be used as bonding agents for certain organic material. The process is illustrated in Fig. 2.5.

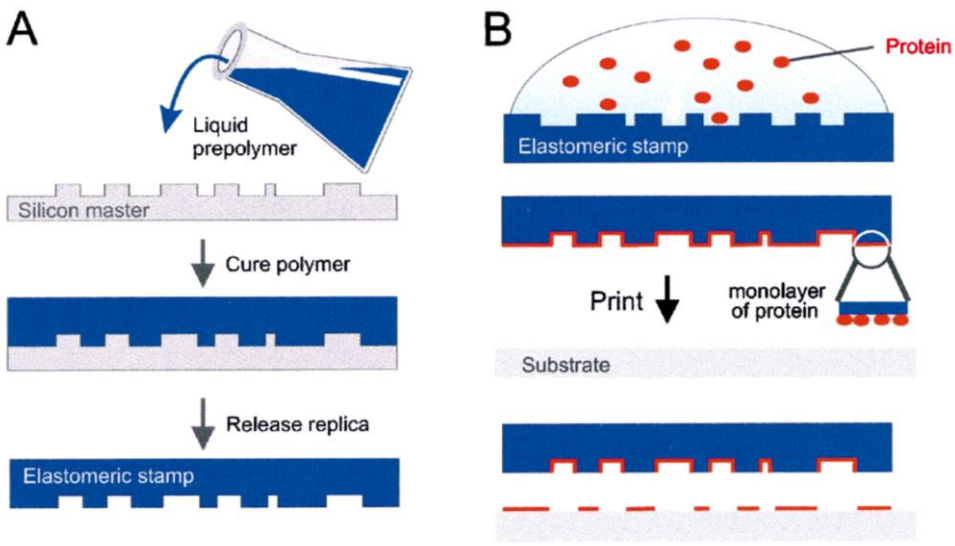

Fig. 2.6 A) Manufacture of Elastomeric stamp, B) Subsequent print of molecular compound, in this case Proteins, by Andre Bernard et al. [38]

2.5 Suitability of soft lithographic methods for micro conductors

Soft lithography is a set of printing techniques designed and developed to overcome limitations faced by conventional printing, most significantly the resolution of any patterned or defined features. These functionalised surfaces are frequently

incorporated into a range of applications such as biosensor protein triggers and MEMS. As applications constantly emerge, the benefit of these soft lithographic processes is the ability to fabricate micro and nano structures with relatively crude and simple print techniques.

Microcontact printing has been developed largely out of Harvard by Prof. G. M. Whitesides and has been taken up by further research outfits using the functionalised surfaces for largely biomedical purposes [38]. The main application of microcontact printing is to produce biosensor arrays, a method of printing protein arrays onto substrates that act as targets for specific protein pairings. This application has potential in numerous forms from DNA profiling to immunoassays. However, rarely is it used as a means for fabricating functional electronic devices. With the development of a field of this nature and magnitude it is invariable that a diverse range of applications will emerge and the process suggested in this thesis may not form the complete solution.

It is worth bearing in mind that in context the primary limiting factor of conventional print technologies has been the resolution of the process, currently at best a reliable 100 µm track and gap electrode spacing array. Soft lithography has the capacity to print resolutions on a sub-micron scale which provides a vastly improved and developed print system [39]. With regard to printing conductors there are several key factors that must be considered including: the volume of deposition, the rate of oxidation and the surface chemistry. The volume of deposition must be significant to pattern a charge carrying substrate, this means having a significant enough deposit to overcome resistive factors most likely in the form of a metallic substrate. Oxidation is also critical especially when working with metals. Given the volume to surface area ratio of the conductive tracks it is likely that oxidation will occur rapidly, it is critical at this point to select a conductor that oxidises relatively slowly, or not at all. Leading into our third critical factor which is the chemistry of the process to ensure bonding of the alkanethiol, and the critical nature of a subsequent etch process to reveal a patterned surface in the conductor.

Microcontact printing will be used to functionalise a conductive substrate surface and by introduction of a subsequent etch process the conductive tracks will be revealed

for use in functional electronic devices. This methodology has attracted interest but to varying degrees of success, due to it frequently being hard to quantify the performance of electronic devices produced to date. What follows is an introduction to some of those processes and developments.

2.6 Current developments with microcontact printing.

2.6.1 Whiteside's Research group

The Whiteside's research group has developed microcontact printing for a variety of applications. One such application that has gained real momentum is the functionalising of gold surfaces for use in biosensors [37]. The group have had a continued presence in the field, particularly in biomedical applications, and much of their early work still forms the basis for many current applications and derivatives in the field.

A significant publication for functional devices is 'Patterning self-assembled monolayers using microcontact printing: a new technology for biosensors?' [41], but a more extensive back catalogue can be found at gmwgroup.harvard.edu. These publications chart the progression of microcontact printing and the success, particularly pertaining to biomedical applications.

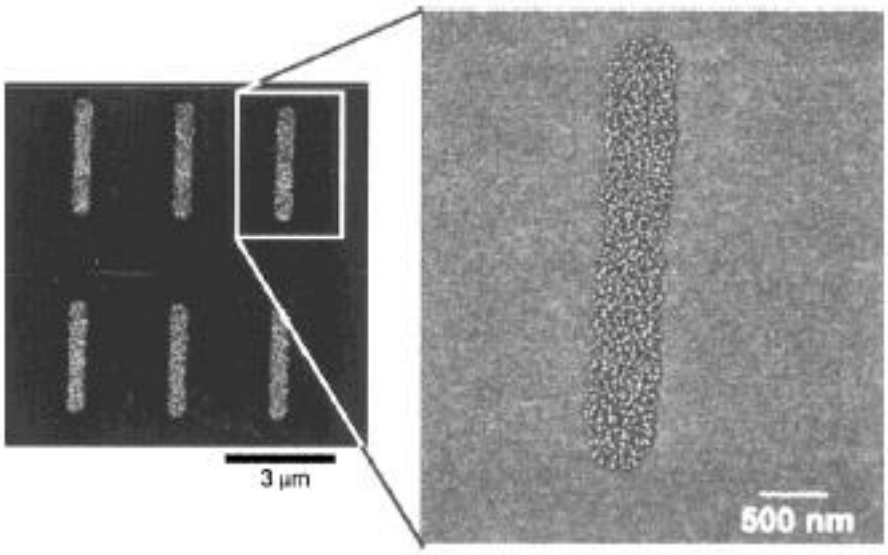

Fig. 2.4 Microcontact printing of immunoglobulins G on a Si wafer, by Andre Bernard et al. [38] The array demonstrates the resolution of the process, linear arrays represented are 3 µm x 500 nm.

The group's efforts have progressively focussed more on simplifying diagnostic techniques and increasingly lab-on-a-chip developments [42]. The Whiteside's research group does acknowledge the use of microcontact printing and its applications for electronics but, at the time of carrying out the research in this thesis, had not progressed significantly into the field and whilst collaborating with electronic and engineering departments alike had not successfully developed the technology in the electronic fabrication direction. The group has been a significant contributor and developer of the field and still holds a majority of the patents [43]. Due to the emphasis on diagnositic and biomedical applications there is little beyond initial trial and investigation into the use of microcontact printing to develop functional electronic devices. This has however been picked up by electronic research outfits.

2.6.2 IBM Research

Individuals at IBM Research have published numerous papers on the subject, their most significant being 'Printing meets lithography: Soft approaches to high-resolution patterning' [44]. Their work has progressed over the last 10 years and has been developed as advanced microcontact printing, looking to pattern gold with an etch resist and increase the yield of successful gold patterned substrates. IBM research has managed to successfully print gold wires of 125 nm. The fundamental problem with this level of resolution is that conductivity poses a problem, with a resistivity reported of 31.7 Ω/μm [44], this is an order of around ten times great than that required for electroluminescent electrodes. Increasing the cross-sectional area of the gold would improve the performance, alternatively a coating process could be explored to coat the gold. However, this could potentially lead to bridging between wires and other issues.

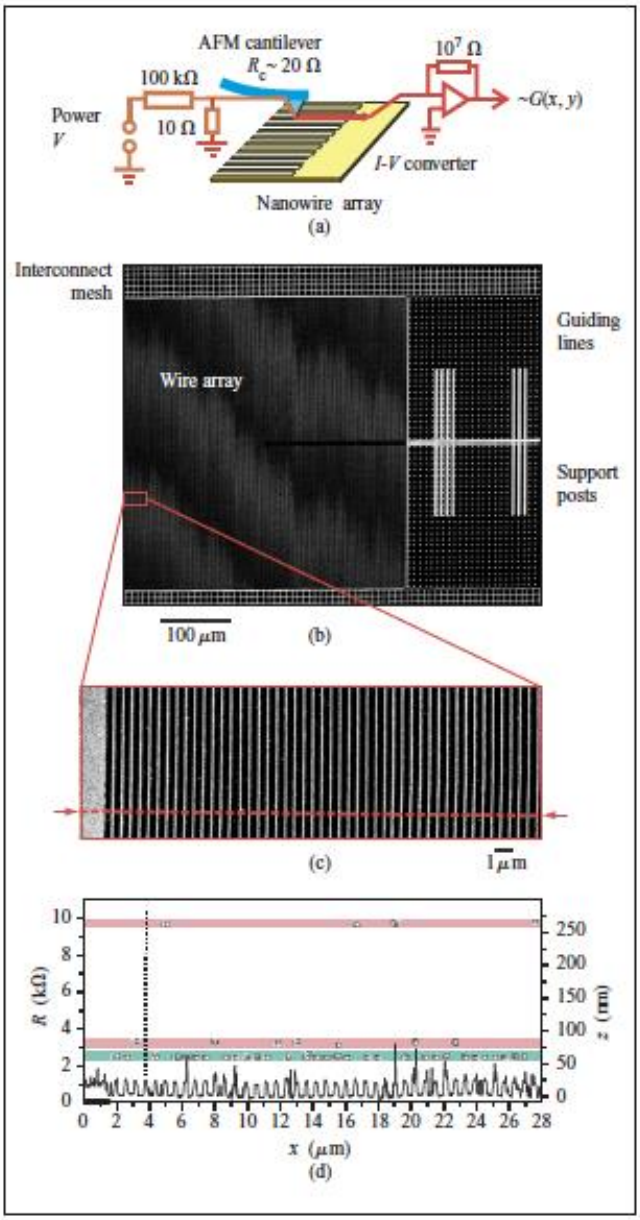

Fig. 2.5 Characterisation of Microcontact printed wires. a) Scheme of conductivity measurements. b) Image of 125 nm wide Au wires on SiO_2. c) Inset image of probing path. d) Results of wire probing showing resistance and topography. Work completed by B. Michel et al, [44]

2.6.3 Philips Research

Philips Research also explored the possibilities of using microcontact printing to pattern localised surfaces be they curved or flexible substrates. They have had moderate success and developed a process called wave printing, whereby a minimal part of the stamp is brought into contact with the substrate narrowing the margin for

error over a larger print area. If a small proportion of the stamp is in contact with the substrate at any given point it vastly increases the tolerance of the process and improves the chance of a more widespread and successful process [45]. Philips' most developed use of microcontact printing has been to functionalise a surface for use in heterogeneous catalysis [46]. This allowed a functionalised surface to be deposited on an oxide layer creating hydrophobic regions for model catalysts.

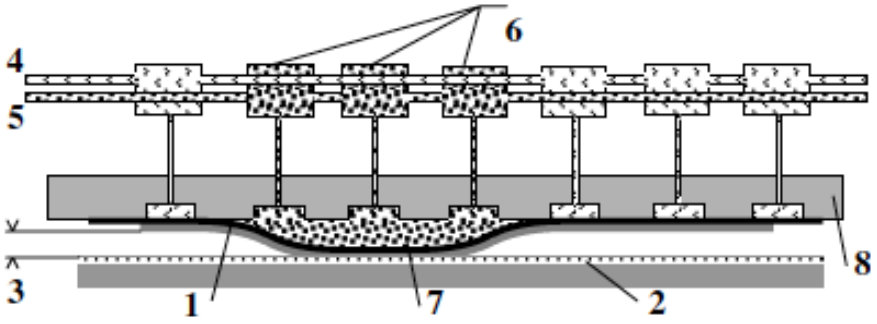

Fig. 2.6 Cross-section of the wave printing prototype: 1) Stamp backplate assembly. 2) Substrate. 3) Working gap (100 µm). 4) Vacuum supply. 5) Pressure Supply (2 kPa). 6) Valves switched to pressure supply, thereby creating waves. 7) Wave. 8) Grooves-plate. Diagram illustrating the wave propagation method by M.M.J. Decre et al. [45]

2.6.4 Centre Suisse d'Electronique et de Microtechnique

Centre Suisse d'Electronique et de Microtechnique (CSEM) has an impressive track record in MEMS technology and an ongoing interest in micro and nano fabrication techniques for plasmonics including significant publications [47]. Their interest has been mainly in the microsystems network and they have ongoing research into functional devices, such as sensors and actuators, amongst other components that form a wide knowledge base from which microcontact printing, and nanoimprint technology would enhance their expertise. In their technology report of 2009 [48], it expanded upon the usage of microcontact printing including the functionalisation of substrates for use in bioreactive receptors. Using photocatalysis cellular repellent molecules are oxidised and removed using a mask. These regions are then filled with cellular adherent molecules to then align cells creating bioactive layers. The

functionalised surfaces for electronics has been explored at CSEM, but not in great depth beyond the initial fabrication process.

2.6.5 Massachusetts Institute of Technology

Massachusetts Institute of Technology (MIT) have developed a method for printing batteries through employing microcontact printing methods. The batteries are one step towards micro power generation and can be printed on a range of surfaces for use, [49]. The batteries utilised a solid state electrolyte deposited over the surface of the electrodes. However there was a slight drawback with producing the opposite electrode to allow the ion exchange needed for power generation, and so the battery architecture was still being configured when reported in [49]. However, they made significant progress given that the process allowed the possibility of harvesting power on the micro scale and had huge potential for powering MEMS technology and other microsystems.

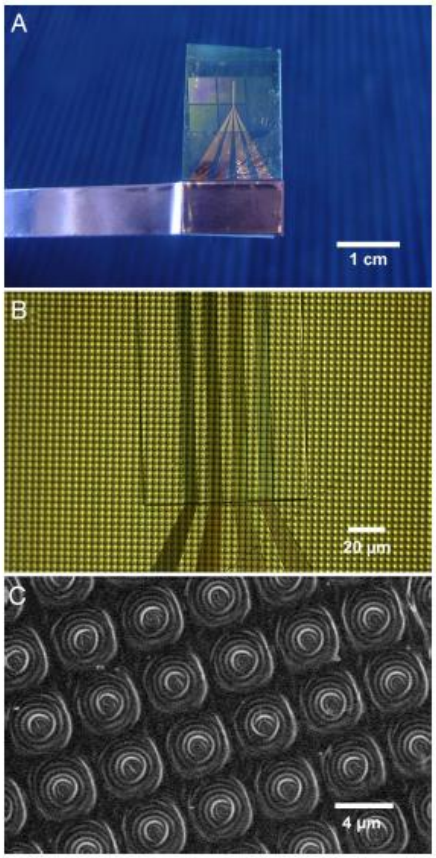

Fig. 2.7 Microcontact printed microbatteries, by Ki Tae Nam et al. [49]. A) Microbatteries on a Pt current collector. B) Optical microscopy image for the micro battery electrode. C) SEM image of the 4 µm diameter electrode.

2.6.6 Microcontact printing for electronic applications to date

It is possible to see the capabilities of the process from section 2.6, both in terms of the geometric possibilities but also the range of applications for microcontact printing. Many of the advances centre around biomedical applications. However, IBM's printed nanowires helpfully demonstrate that the process can produce conductive deposits to a very high resolution. The balance in this instance was between structural integrity of the materials used, PDMS is elastomeric and the smaller the feature size the more critical that becomes to maintaining linear features for deposition without bridging or collapse. As reported by B.Michel et al [44] conductivity of the nanowires was such that they were unsuitable for carrying sufficient load.

MIT's progress when looking at micro-batteries was promising looking to print electrode configuration for use as terminals for a solid electrolyte. The success at printing terminals with 4 μm dimensions demonstrates the reliability and repeatability of the process over a larger area. At present the material deposited is to form the anode, within their paper [49] Ki Tae Nam et al discuss the potential use of interdigitated devices to form the cathode adjacent to the anode. This has not been achieved due to the resolution problems when patterning multiple conductive materials and providing track and gap spacing geometries as illustrated in Fig. 1.3.

2.7 Identification of the knowledge gap

To bring clarity and direction to this thesis, there is a natural progression between standard industry methods of printing that demonstrate a drive to recognise increasingly more functional electronic devices coupled with the emergence of soft lithography as an increasingly more established method for patterning, in particular, gold surfaces. The use of gold is deliberate to eradicate the influences of oxidation, and it would therefore be wise to continue using gold as the primary substrate.

This thesis has been focussed on manufacturing electrode structures on a rigid backplate with an output that is easily quantifiable. For this reason it was suggested to advance some of the work previously completed by Brunel University and the

manufacture of interdigitated electrode arrays by offset lithography for use in electroluminescent devices, with the aim to reduce the track and gap spacing to an order of 10's of microns. The size of 10 µm is limited due to the use of phosphor particulates employed in electroluminescent displays. In order to improve the particulate lifespan they are encapsulated to protect them. Uncoated phosphor material has a size of 7 µm. The encapsulation of phosphor particulates by SiO_2 does increase their size to a minimum of around 25 µm [50]. This thesis will therefore explore the opportunity to produce electroluminescent devices with geometrically optimised track and gap spacings. A direct consequence of this will be reducing the driving voltage of the devices to below current operating voltages of using an AC supply at 110 V_{rms}. Section 2.8 details an introduction to electroluminescent technology that has been established and researched extensively over the last century and has gained fresh interest as new manufacturing and technology has emerged, including wearable technology [51].

2.8 Electroluminescent displays and phosphor particulates.

Electroluminescent (EL) displays have found widespread use in their functionality as backlighting for a range of applications. More recently EL displays have been used for advertising hoardings, the phosphor particulates providing a soft blue-green hue against a contrasting background. EL devices utilise a capacitive structure producing a high electric field with a dielectric layer of phosphor material that is placed within the electric field.

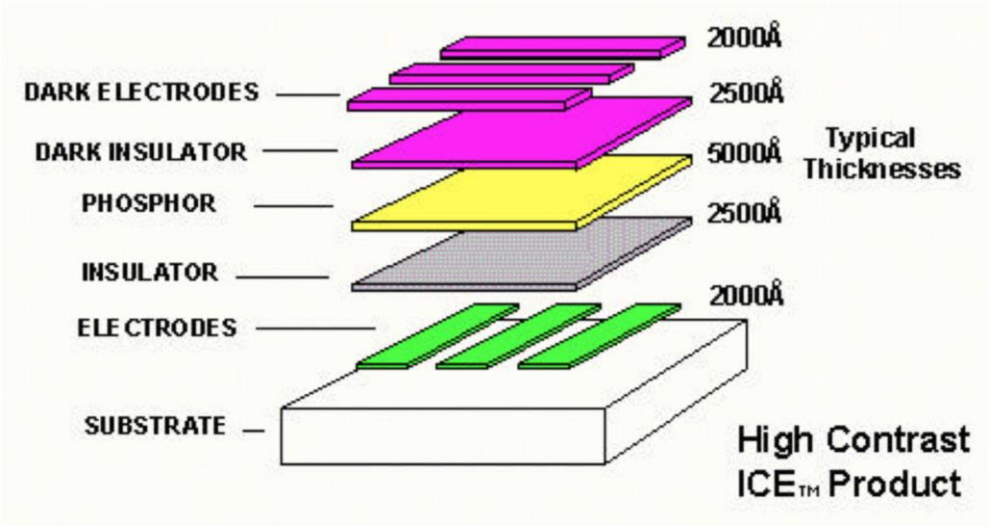

Fig. 2.8 Structure of a traditional Monochrome EL structure by J. A. Hart et al. [52]

Using an alternating current changes the direction of the field between electrodes and as this process occurs the direction of the current being supplied to the electrodes switches, this in turn generates an alternating field that continuously excites the phosphor particulates, which gives rise to the emission of light. Discussion has arisen over the manner in which phosphor particulates become excited, much of the discussion centres on the electronic configuration of the atoms involved, [53]. That being said it is acknowledged that the phosphor inks undergo excitation due to charge transfer and periodically return to a more stable state. Encapsulating the phosphor particulates makes them more robust and preserves their functionality making them last longer, [54]. The light emission can be controlled by electrical variables such as the frequency of the alternating current and the magnitude of the voltage, and physical variables such as the dielectric material used and the spacing of the electrodes. The spacing of the electrodes is the variable critical to this thesis as the dimensions are explored with a view to reducing the driving voltage.

EL theory was introduced in Chapter 1 but here we can identify microcontact printing as a method for producing micro conductors. By reducing the track and gap spacing of the relative capacitive devices, the field can be increased to a point beyond the threshold required for stimulating phosphor particulates.

2.8.1 Refined objectives

The objective of this thesis is to demonstrate the potential use of microcontact printing in printed electronics. This will be achieved in part by demonstration of microcontact printing as a means to produce electronic circuitry and components. This will be observed most notably by development in the area of electroluminescent displays, as electroluminescent displays have not previously been manufactured by the use of microcontact printing, and thus will contribute a novel development in the printed electronics field. A two stage manufacturing process for producing electroluminescent displays was developed by The Cleaner Electronics Research group, this overcame the need for the conventional five stage layered manufacturing process [14]. An interdigitated arrangement was fabricated, using the geometry

described in Fig 1.3, with a 100 µm track and 100 µm gap (100 µm track and gap). Fig 1.4 illustrates this result, silver loaded ink was printed using a Heidleberg GT46 offset lithographic press. The group used a range of polymer substrates to print an interdigitated array, with dimensions 10 cm x 5 cm. A resin bound phosphor was then screen printed onto the surface, as a solvent carrier evaporated from the surface the particulates we deposited over the electrode array. Incorporating this technology, this thesis aims to produce a functional electroluminescent display via microcontact printing, the two-stage device will aim to overcome a common problem with electroluminescent displays and that is the relatively large voltage (around 100 V_{rms}) that needs to be supplied in order to stimulate phosphor particulates to emit light.

2.8.2 Identification of investigative procedure

Work commenced by optimising each of the printing process steps in turn. They were then combined to print a range of features from 100 µm to 10 µm track and gap spacing as illustrated in Fig 1.3, which were used for electroluminescent displays. Once the tracks were printed and the displays produced, they were characterised by measuring the luminance of the structures. This gave indication of the progress and relative success of the research work.

Work started with analysis of the master fabrication, looking at the possibilities for use as a mould or forming process for the stamp production. The selected option for fabricating a master depended on certain properties desired for the stamp, and certain capabilities of different processes.

It was then necessary to work on developing stamps for use in microcontact printing. The artwork needed to be such that it was relatively simple to replicate and scale down. We used an interdigitated structure with a spacing that runs back and forth between the electrodes. Also it was necessary to look at the effects of mould release agents on the surface chemistry of the stamps.

The method and process of deposition of gold for use as the substrate also had to be understood. The best method was determined for manufacturing the substrates

based on the properties required. Substrates were then produced by different deposition methods, these included sputtering and vapour deposition.

Different thiol compounds were examined for their suitability to the etching process. This helped determine the progress achieved by using an alternative thiol. The thiols considered had varying carbon chain lengths in order to observe whether altering the chain length affected the resist properties. 11-Mercaptoundecanoic acid if often for used to functionalise surfaces leading to a hydrophobic COOH terminating group being exposed. There are however various other compound molecules that can be used to functionalise gold surfaces. A small selection of molecules were chosen for examination and comparison.

In order to ink the stamp it was necessary to leave it in a solution of thiol and solvent, the thiol was left in a solution of 1 mMol in an ethanol carrier, the ethanol is a solvent but is not aggressive towards the thiol molecules or the stamp. Research was carried out into the development of whether alternative solvent carriers could be used to substitute for the ethanol.

Once the stamp was inked it was necessary to analyse the best and most appropriate method for printing. It was noted that certain parameters restricted the method of printing. Any deformation to the stamp has a negative impact on the stamp face and warped the stamp surface. Conformal contact between the stamp and the substrate must be maintained to avoid any registration problems. The fact that the stamps were elastomeric meant they were flexible and could accommodate tiny imperfections in the movement of a hand when printing. It also meant that flexibility was an issue when horizontal forces were introduced.

The etching process used to remove gold from the non thiolated areas was critical to the final conductive tracks. The exact process by which etching could take place needed to be determined. What concentration of etch solution allowed sufficient control over the process and yet still produced a steep etch gradient between the gold tracks and etched areas also needed to be established. It was considered to use alternative etch solutions but this was decided against on the grounds that there were too many variables even using a potassium iodide (PI) etch. Also the

suggested alternatives were either cyanide based etches, or aqua regia, both of which are hazardous.

This work was then combined and print results were compared to the early stages of development in determining the best course of action and improvements to be made during progression of the printing process.

Theoretical values of capacitance and field for interdigitated arrays have been calculated and reported on in Chapter 3. These values can be used to estimate the energy dissipated and instantaneous power for an Electroluminescent display. This theory can be reconciled with the energy dissipated from the phosphor band gap as electrons lose energy ‘falling’ from the conductive band to the valance band. Functional electroluminescent displays were produced and quantifying these values can also be reconciled with the relevant theory to further understand their nature.

Chapter 3
Methods and materials

3.1 Further investigation of the microcontact printing process

A study of soft lithography was undertaken to improve upon low cost, large scale manufacture using relatively crude printing techniques applicable to printed electronic circuit fabrication. The area of microcontact printing, a soft lithographic method was identified for deposition of organic and inorganic material leading to the functionalisation of surfaces.

This research is a continuation of work completed by The Cleaner Electronics Research Group of Brunel University in lithographically printed conductive inks [14]. From this work they managed to print several different passive components with measured performance comparable to traditional circuits, making it possible to print lithographically an entire circuit board rivalling standard PCB techniques and potentially rendering certain electronic fabrication approaches redundant [55]. One application of their printed circuits was to manufacture electroluminescent displays, printing an interdigitated electrode array structure to create a high electric field needed to stimulate a phosphor ink deposited over the surface and more critically in the gaps created. It was found in 2001 that with offset lithographic techniques there were limitations on the process created by the registration of the rollers and dot gain in the process meaning the highest electric field created was limited by the track and gap spacing of around 100 μm [56]. As described in section 1.4 an inverse proportionality relationship between track spacing and electric field would suggest decreasing the track and gap spacing to increase the electric field created, a task that if achieved would lower the voltage used to power the device. Microcontact printing provides a manufacturing technique to print conductive tracks to much finer resolution and reduce the gap spacing between the tracks and therefore the voltage needed to drive the device.

The process of microcontact printing has not been a well known or established technique for electronic manufacture and without the form of microcontact printing

being widespread, definition must be given to the parameters of the process. It was noted that microcontact printing methods used primarily in the deposition of a single layer of an alkanethiol to create a functionalised surface for use in biochemical applications and not for electronic purposes. There were principles from the application of Self Assembled Monolayers (SAMs) to a substrate that could be applied to help create a printing process but given the nature of the specification for microcontact printing, first investigation turned to the analysis of each step of the printing process and it's suitability to be used as a print technique for electrical conductors. It was noted that whilst investigation continued by various research outfits the process remains low yield and therefore costly. All results point to the potential for microelectronics with many impressive developments from the microcontact battery, for harvesting micro-power generation, to the wave method, for large scale arrays, employed by Philips Research.

To begin with a stamp that was manufactured to a certain relief specification is thiolated by immersion in a thiol solution, a common chemistry of MUA (Mercaptoundecanoic acid) and a solvent vehicle was employed. The inked stamps align the MUA molecules in such a way that they bond to the PDMS stamp by a carboxylic acid terminating group [57]. The stamp was then brought into contact with the gold substrate and bound to the gold via a sulphur group that is at the opposing end of the chain. This transfer occurred due to the difference in bonding energies, a higher bonding energy between the sulphur and gold effected a release from the stamp. After the thiol ink was printed onto the gold substrate it was then left to undergo hybridization. This is a process that when the SAM aligns itself according to charge, it effectively formed a protective shell that acts as a resist layer to the etching process [58]. The etching solution was then used to remove the unprotected gold substrate to reveal the printed gold conductive tracks.

3.2 Use of a commercially supplied microcontact printing kit

To begin with a commercially available microcontact printing kit for patterning gold substrates was supplied by Platypus technologies, this allowed for initial experimentation and investigation of each step to be done quickly. The kit included: substrates, stamps and a thiol [59]. The kit did not include an etch solution and

certain sources recommended a cyanide based etch when using a functionalised surface [60]. Due to the corrosive nature and environmental consequences of using cyanides, attempt was made to bypass the use of cyanides and find an alternative etch. The details of the kit are recorded below and their main observations and progressions detailed.

A substrate of gold was sputtered onto the surface of a glass slide, with a thickness of 500 Å, using a titanium (Ti) adhesive layer. The glass acted as a mount for the gold substrate to provide a back plate that supported the layers placed over it and eventually a backing for printed tracks. Due to the characteristics of the glass it was ideal to reduce bend and other mechanical forces placed on the tracks during the contact printing process to help ensure equal pressure across the area of contact. To prepare the glass for contact there was a need to clean the substrate surface due to any impurities on the printing surface that would hinder transfer of the thiol from the stamp to the substrate. It was advised that this should be done using ethanol to rinse the surface followed by a stream of nitrogen to dry it.

A stamp was also prepared for the experiment using an elastomer, Polydimethylsiloxane (PDMS) to fabricate a 100 µm track and gap; this was done using a master copy as a mould with the desired pattern inverted to create the PDMS stamp. The stamp fabrication for 100 µm track and gap is a relatively simple process and was used to transfer a thiol of 11-Mercaptoundecanoic acid to the gold substrate, the particles being bonded first to the stamps relatively low energy surface (PDMS) and then transferred to the relatively high energy surface (gold substrate). The stamp needed to be prepared for printing to allow the MUA particles to bond with the surface of the stamp. This was done by immersion in a prepared solution of ethanol containing 1 mMol of the thiol for 2 hours in a capped and airtight container.

Once in contact with the substrate the MUA formed a self assembled monolayer (SAM) over the surface that acts as a resist layer to a subsequent wet chemical etch. It is important to note that the SAM was only a resist layer and not an inhibitor, meaning etching still occurred, but at a slower rate.

To bypass the use of cyanides an alternative etching solution was required for the gold except for where the MUA acts as an etch resist to create the desired gold lines of 100 µm track and gap. A wet chemical etching process involving Potassium Iodide (KI), Iodine (I_2) and distilled water (H_2O) in the quantities 4g KI: 1g I_2: 40ml H_2O was used with successful results [61]. A 100% etching solution etches gold at a rate of approx 1 µm/min; given that at present there is 500 Å of gold over the glass slide which equates to 50 nm, it was necessary to leave the substrate in the etchant for 3 seconds to remove the gold from the surface. It was desirable to slow the etching process by diluting the etchant solution. Due to the aggressive nature of the etch there was a strong possibility that it would remove the gold protected by the MUA mask as well, but slowing the process down would allow more control over the etching process by monitoring the substrate's progress.

3.2.1 Autonomous print development

In order to optimise the process it was important to develop the printing procedure to become independent of the commercially available kit and therefore gain a greater degree of control over the print techniques. In order to do this it was necessary to explore alternative manufacturing methods of individual stages of the print process. The pre-fabricated kit supplied by Platypus technologies was limited by various constraints: the stamp dimensions, the yield of gold substrates, the quantity of an appropriate thiol and use of an additional etch solution [59]. The key areas for development were: a suitable master manufacture, successful stamp fabrication, selection of an optimal thiol, a method for producing a high yield of appropriate substrates and the development of a suitable etch solution. This followed the consecutive stages to the print process. Initial success was difficult to quantify. To determine a useful adaptation it must be used in the context of the process as a whole. For this reason early prints were looking to establish certain successes relevant to the necessary print stage, rather than leap to the final stages. It was necessary to optimise each stage before the process was collated and underwent further improvement to increase accuracy of the final results.

3.2.2 Master manufacture

Two methods for constructing a reliable master were identified: a diffraction grating master and a reactive ion etched silicon wafer.

The issue that was discovered when considering the use of a diffraction grating master was that the relief across the face of the grating is typically either triangular or circular to utilise the angles needed for diffraction as light passes through the grating, meaning the desired square profile of the stamp relief were not readily achievable with a diffraction grating as demonstrated below:

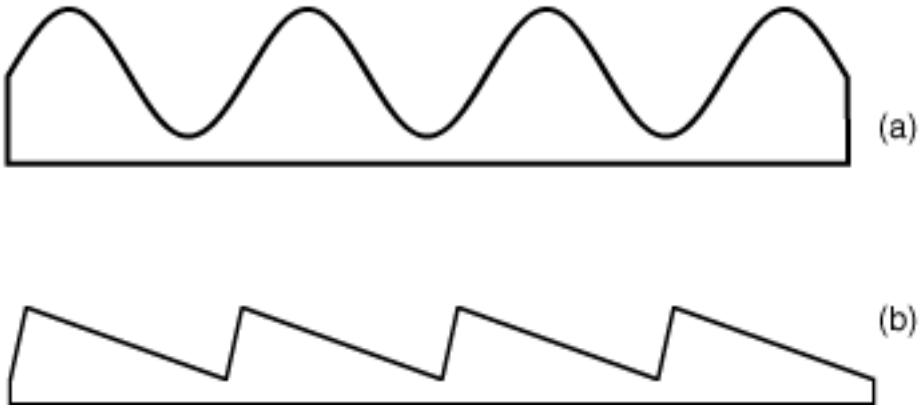

Fig. 3.1 Common diffraction grating profiles, cross-section of a) Sinusoidal, b) triangular, by C. Palmer et al. [62]

From Fig. 3.1, it should be noted that conformal contact across the topography means minimal areas of contact and therefore only partial transfer of thiol ink reducing reliability of the track width. The PDMS stamps were elastomeric so there would be some elasticity broadening the tracks but to depend on the elastic properties of the stamps on a micron scale does not produce the reliability necessary when using manual application which is then subject to inconsistencies from the human printer [63]. Another problem that arose from using a diffraction grating master was the delicate nature of them. They are mostly made by mechanically scoring metal and therefore have very delicate features that can fracture or crack very easily, making them hard to store as wear and tear can damage micro features

beyond repair, they are also expensive due to the high precision of mechanical scoring.

Another manufacturing solution for the master was to dry etch a silicon wafer, this could involve a number of processes including physical sputtering and reactive ion etching. The benefit of these techniques is that they produce an anisotropic etch, meaning the etch rate vertically differs to the etch rate horizontally as displayed in the figure below [64].

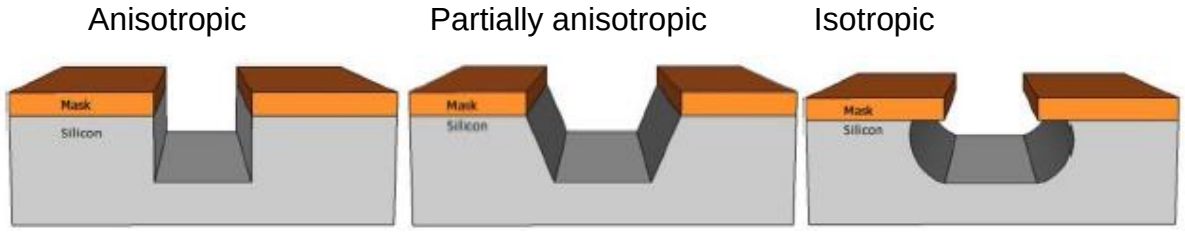

Fig. 3.2 Fully anisotropic through to isotropic etching, as described by Avinash P. Nayak et al. [64]

From Fig. 3.2, a clearly defined and high resolution channel is produced by an anisotropic etch. Due to the control of the etching in a single linear direction anisotropic etches are typically employed in the manufacture of MEMS technology and microfluidics. This process reduces the effect of underetching or track gain, leading to very high resolution features with a tolerance of potentially nanometres [65].

For several reasons, it was decided that using a silicon wafer would be a more preferable master. Firstly, due to the high level of detail it was relatively simple to transfer a design to the wafer. Secondly, although still fragile, the wafer was also less fragile than a diffraction grating master. Thirdly, it was also possible to have a range of stamps varying in size on a single wafer. Lastly, there was control over the depth of the dry etch, which has consequences for the feature size and forces introduced across the surface of the stamp.

It was determined that a silicon wafer was the preferable media for using as a stamp master. Using the standard formula developed for measuring capacitance of an

interdigitated electrode array a range of structures was manufactured. When designing the structures there were two goals in mind: to demonstrate the resolution of microcontact printing and the reliability for printing over increasing areas. Firstly, the resolution from previous structures was limited to approximately 100 µm. Soft lithography has the potential to reliably print functional electrodes on a nanometre scale. Secondly, the dimensions of the tracks potentially hamper conductivity affecting performance. As the interdigitated array increases in area the more likely it is that electrodes are fractured reducing the amount of light emitted.

3.2.2.1 Capacitance calculations

Tables 1, 2 and 3 detail the theoretical capacitance for multiple structures. The dimensions for length and width are taken from Fig. 1.3. From this table it can be observed which structures produce an optimal electric field. Using capacitor theory we can equate Capacitance to Field as a direct relationship.

$C = (\varepsilon_r \varepsilon_0 A)/d$ (Eq. 6) and, $E_f = V/d$ (Eq. 1)

Combining these two suggests:

$C = (\varepsilon_r \varepsilon_0 A E_f)/V$ (Eq. 7)

The Tables represented in Table 1, 2 and 3 were produced using Eq. 2 to establish the theoretical capacitance values for various track and gap geometries. By representing these values and comparing them with Eq. 7 it could be determined how the theoretical values for capacitance tabulated (Table 1, 2 and 3) performed against a parallel plate capacitor.

Modelled capacitance of interdigitated structures (pF/m)				
		Dimensions w x l (mm) (Area)		
		3 x 1	3 x 3	3 x 5
Track and Gap (µm)	No. of digits	(3 mm^2)	(9 mm^2)	(15 mm^2)
100	15	0.0385	0.1156	0.1927
75	20	0.0532	0.1597	0.2661
50	30	0.0826	0.2478	0.4130
25	60	0.1707	0.5121	0.8535
15	100	0.2882	0.8646	1.4409
10	150	0.4350	1.3051	2.1752

Table 1. Theoretical capacitance of structures with a width of 3 mm.

Modelled capacitance of interdigitated structures (pF/m)				
		Dimensions w x l (mm) (Area)		
		5 x 1	5 x 3	5 x 5
Track and Gap (µm)	No. of digits	(5 mm^2)	(15 mm^2)	(25 mm^2)
100	25	0.0407	0.1222	0.2037
75	33	0.0548	0.1645	0.2742
50	50	0.0848	0.2544	0.4240
25	100	0.1729	0.5187	0.8646
15	166	0.2892	0.8677	1.4461
10	250	0.4372	1.3117	2.1862

Table 2. Theoretical capacitance of structures with a width of 5 mm.

Modelled capacitance of interdigitated structures (pF/m)				
		Dimensions w x l (mm) (Area)		
		10 x 1	10 x 3	10 x 5
Track and Gap (µm)	No. of digits	(10 mm^2)	(30 mm^2)	(50 mm^2)
100	50	0.0424	0.1272	0.2120
75	66	0.0574	0.1721	0.2869
50	100	0.0865	0.2594	0.4323
25	200	0.1746	0.5237	0.8728
15	333	0.2918	0.8753	1.4588
10	500	0.4389	1.3167	2.1945

Table 3. Theoretical capacitance of structures with a width of 10 mm.

The equation $C = (\varepsilon_r\varepsilon_0 AE_f)/V$ suggests a direct correlation between capacitance and electric field strength. Based on this relationship we can determine a minimum value for capacitance at each structure size. Simulating a standard capacitive device, as defined in section 1.4, operating at 100V and producing an electric field of 1×10^6 V/m, and by using the extremes for the electrode areas in our model above, at a minimum area of 0.75 mm^2. Each of the area calculations must be divided by four to accommodate track and gap spacing, and then the remaining electrode material is then split evenly between the positive and negative terminal. We can calculate:

$C = (\varepsilon_r\varepsilon_0 AE_f)/V$ (Eq. 7)

$C > (8.9)(8.854 \times 10^{-12})(0.75 \times 10^{-6})(1000000)/100$

$C > 5.91 \times 10^{-13}$ F/m
C > 0.00591 (pF/cm)

Taking the largest area from the set of data, we can determine:

$C = (\varepsilon_r\varepsilon_0 AE_f)/V$ (Eq. 7)

$C > (8.9)(8.854 \times 10^{-12})(1.25 \times 10^{-5})(1000000)/100$

$C > 9.85 \times 10^{-12}$ F/m
C > 0.0985 (pF/m)

Both these calculations demonstrate that the dimensions described throughout the model fall in the range of being able to stimulate phosphor particulates by comparison with the equivalent theory for parallel plate capacitors. Selection on a range of structures must demonstrate a diversity of track and gap widths and areas. For this reason a silicon wafer was fabricated by the Scottish Microelectronics centre at Edinburgh University facilitated by Peter Lomax.

3.2.3 Stamp fabrication

To manufacture the stamp, the silicone based elastomer Polydimethylsiloxane (PDMS) supplied by Dow Corning, commercially known as Sylgard 184 [66], is poured over the master and allowed to cure, one part curing agent is added to 10 parts PDMS. This is then degassed in a vacuum chamber to remove all air, that could affect the elastomeric properties. During degassing the pressure in the chamber is dropped causing all the air pockets to expand and burst. Once brought back to atmospheric pressure nearly all the air pockets are removed except for very tiny defects, hardly visible to the naked eye, having negligible effect upon printing.

Three problems were encountered when fabricating the stamps. Firstly, a parallel plane had to be maintained when curing to avoid misalignment with any mounting surfaces. Secondly, removing of the stamp from the mould was a highly precise process and frequently sheered structures on the surface of the stamp. Finally, heat curing potentially introduces losses to the surface area, this effect can be minimised by curing at different temperatures.

Firstly it is important to maintain a parallel cure to ensure that the stamp is structurally consistent across the surface. This is important not just for the cured reverse of the stamp but also for the wafer to be horizontal to allow the stamp face to be parallel to the stamp reverse [67]. One technique to overcome this was to use a spirit level to measure a flat surface on which to cure the stamps, the wafer was then immersed in the PDMS, this allowed for the weight of the wafer, although not very much but for the liquid elastomer significant, to settle the master horizontally on the bottom, so that when cured a thin layer of PDMS would be found underneath the wafer which also led to easier extraction of the stamps after curing.

Secondly the release techniques of the stamps from the wafer were a challenge, an array of structures were printed ranging in size and feature size across the surface of the wafer. The smaller the feature size led to a more delicate stamp surface, when removing the stamps from the master there was frequent tearing of the PDMS features as stresses were introduced, below is an image demonstrating the tearing that occurred during release, in this case left to right:

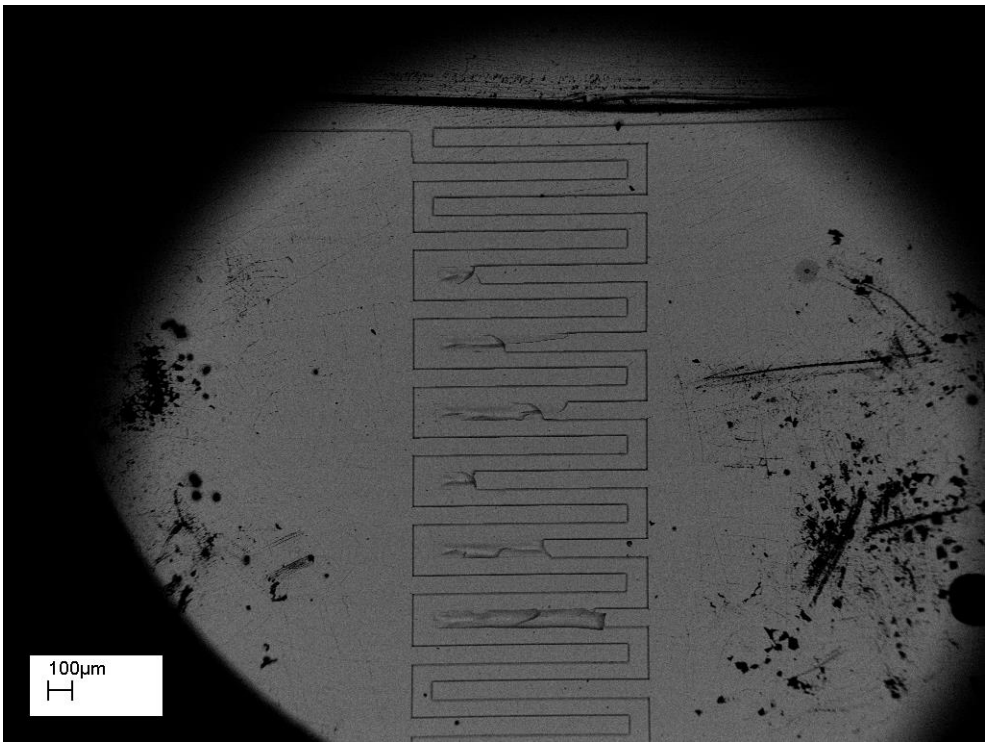

Fig. 3.3 Tearing of track profile during release from master

Mould release agents were explored to aid the release of the stamp that would line the master with a thin film to prevent any bonding between the cured stamp and the master. The mould release agents used however are polysiloxane based, meaning that when in contact with PDMS they alter the surface chemistry which prevents subsequent adhesion of the thiol to the stamp [68]. One solution to overcome this problem is to use a dry etch technique to remove the top few microns on the stamp surface. Although this will remove the contaminant, it is costly.

Thirdly, it is preferable to cure PDMS at 60 ˚c for 24 hours, it is possible to heat cure PDMS at up to 130 ˚c for 90 minutes, this was initially attempted with the silicon wafer master, however the PDMS shrank snapping the wafer. An experiment was then conducted to understand this phenomenon. It was discovered that a total loss of about 3% occurred across the stamp surface when cured at 130 ˚c. A non-precious rigid test sample was used to manufacture sample stamps. The width of the sample measured was 21.37 mm, and after the heat cure at 130 ˚c it measured 20.72 mm, a 3.04% loss. A reduction at this rate across the whole 120 mm wafer means a reduction of 3.6 mm in diameter. When inflicted on the 100 µm features on the wafer

surface, this leads to the features putting high stresses on the PDMS features. This problem is minimised using a low temperature cure method.

3.2.3.1 Linear shrinkage of PDMS elastomer

Linear shrinkage is not a new concern when using PDMS. With several publications substantiating the effect, a room temperature cure takes in the region of 48 hours. A heat cure can reduce this to under an hour. At a temperature of 120 ˚c this was specified at 40 mins, [69]. In this paper a theoretical model is devolved for the ongoing reduction in feature size during heat curing. This heat shrinkage appears to be a common issue and has been reported in [70], [71] and [72]

The results obtained above, regarding heat curing at 130 ˚c noted a reduction in feature size from 21.37 mm to 20.72 mm. This indicates a loss of 3.04% across the surface. The theoretical values proposed by [69] explore a heat cure between 8-120 ˚c. A proposition is made for a least squares linear model for the linear expansion of PDMS as below:

At 130 ˚c:
$y = 0.0180 \times T + 0.46$ (Eq. 8)
$y = 2.80$

An uncertainty factor is proposed using [73], and defined as below:

$U(y)^2 = (T \times u(\alpha))^2 + (\alpha \times u(T))^2 + (u(\beta))^2$ (Eq. 9)
$U(y) = \pm 0.23438$

This suggests $y = 2.80 \pm 0.23438$, therefore an estimated solution is between 2.56562% and 3.03438%

When the measured experimental value or 3.04% shrinkage is compared with the theoretical range of values we can see this value sits at the extremities of the model.

It can be viewed as a reasonable value for the linear reduction of PDMS undergoing heat curing at 130 ˚c.

Settling on a heat cure of 60 ˚c applied with the same model detailed below:

At 60 ˚c:

$y = 0.0180 \times T + 0.46$ (Eq. 8)

$y = 1.54$

Gives:

$U(y)^2 = (T \times u(a))^2 + (\alpha \times u(T))^2 + (u(\beta))^2$ (Eq. 9)

$U(y) = \pm 0.15823$

This suggests $y = 1.54 \pm 0.15823$, therefore an estimated percentage reduction is between 1.38177% and 1.69823%

At room temperature of 20 ˚c, the model suggests $y = 0.82 \pm 0.13355$. This theory doesn't hold as explained by Morten et al. Shrinkage occurs during the cooling period subsequent to heat curing.

Table 3.1 and Fig. 3.4 Reports the findings by Madsen et al. [69] as PDMS undergoes heat curing.

Curing temperature (˚c)	Linear % shrinkage, Madsen et al. (PDMS 1:10)
40	1.07 ± 0.05
60	1.67 ± 0.06
80	1.92 ± 0.03
100	2.28 ± 0.04
120	2.70 ± 0.05

Table 4 Experimental results for linear shrinkage as recorded by Madsen et al. [69]

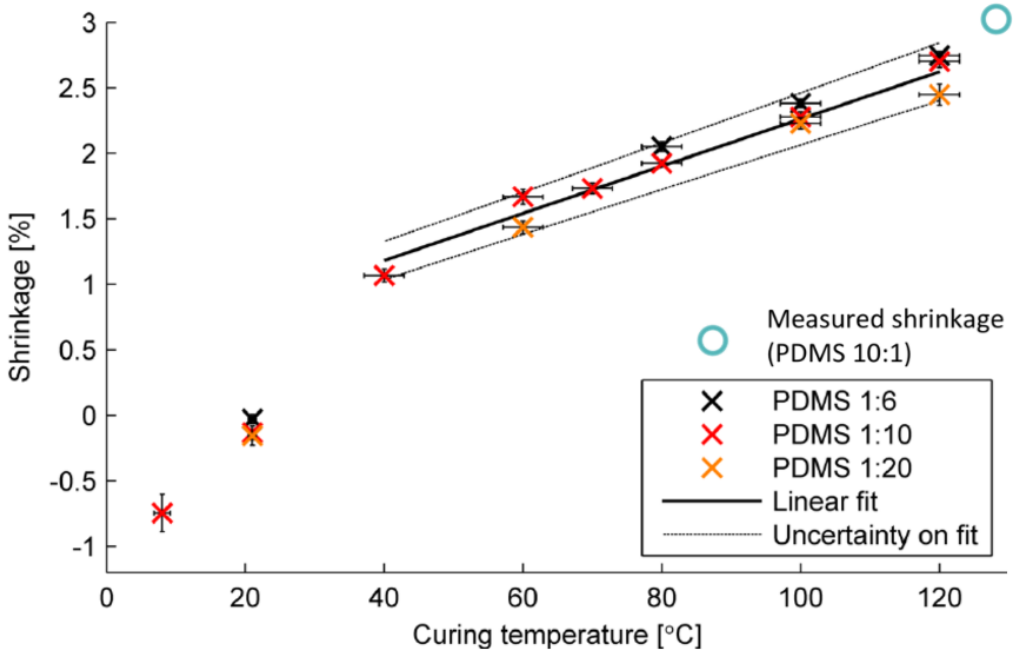

Fig. 3.4 Result for linear shrinkage, of PDMS (mixed at 1:10), superimposed on the model for linear shrinkage of PDMS, by Madsen et al. [69]

From Fig. 3.4 it was also noted that extrapolation of the results implies that at 130 ˚c, the result was slightly above those recorded by Madsen et al. [69] in their paper. This is mostly caused by an inconsistency when heating in an oven using a dial rather than a more precise digital oven. The result, however, maintained consistency with the linear relationship, which is in keeping with other results recorded by Madsen et al.[69].

3.2.4 Substrate production

The substrates being produced were gold, this is largely due to the chemical structure of the thiol being used, with a SH (sulphydryl) end group it readily bonds to the gold. Gold is also recorded as inert, so when the slides were supplied with the initial kit the effects of oxidation were lessened. Other metallic films of silver and copper were considered, but already having a chemistry for the thiol and etch solution it was decided to continue to use gold.

It was decided to use glass microscope slides as a back plate to deposit the thin gold films on, this was done for several reasons, firstly the glass back plate provided structural support for the initial films and also for the micron sized features attempting to be printed. Secondly glass acts as an insulator adding to the build up of field between the two electrode. Finally the glass is inert, reducing the interference with the detailed surface chemistry being explored. To produce the gold coated glass slides two methods were considered due to them being readily available; vapour deposition and sputtering, it was decided that sputtering was the preferred option but a brief explanation follows of both processes and the reasons for the decision to sputter.

Vapour deposition is performed in a near vacuum and relies on the boiling of a gold deposit placed in a tungsten deposition boat. A large current is passed through the tungsten boat which is narrowed towards the deposit allowing for a concentration of the current flow which heats and boils the gold powder. The current used is variable as the conditions dictate; an incremental increase allows the vacuum chamber to stabilise throughout the process.

Sputtering consists of firing particles at a sample target; ions from the target are then ejected from the surface, ionised and propelled through an argon plasma region towards the substrate. Sputtering is performed under a vacuum with argon gas leaked into the chamber to create the plasma.

There are advantages to both methods, vapour deposition seemingly produces a smoother film as the gold is first vaporised, it is also a simpler process as there is no need for an argon cylinder. Sputtering however is much quicker to perform and takes an hour rather than a day; sputtering can be performed at high pressures, whereas Vapour deposition requires very low pressures. The electrical performance of substrates from each process is indistinguishable. Once etched, the performance may vary due to the method of deposition employed. For interdigitated electrode structures at nanometre thicknesses, it was anticipated that the nature of how the film performed was dependant on the method. In light of this, sputtering was the preferred method due to the yield rate once it was established to perform as well as the vapour deposited films. Were conductivity to pose a problem, then it was

considered that a further avenue of investigation might be to explore vapour deposition as a method.

Both methods produced electrically very similar results. Fig. 3.5 demonstrates the performance of various thin film thicknesses and their resistance. Theoretically a model was developed for the resistance as film thickness varies. This could then be used to identify an optimal film thickness for electric field generators. It could also be used to characterise the structures being produced. If the resistance along each track can be quantified, then the film thickness can be measured. The model that governs the graph in Fig 3.5 was established from:

$R = (\rho L)/A$ (Eq. 10)

Where R = resistance, ρ = resistivity, L = length, and A = cross-sectional area (defined as width and film thickness). Using a glass microscope slide that measures 0.075 m in length and 0.025 m in width, we can define resistance as a function of thickness (h):

$R = (2.44 \times 10^{-8} \times 0.075) / (0.025 \times h)$,

$R = 7.32 \times 10^{-8} / h$

This function defines for the graph illustrated in Fig. 3.5

This graph demonstrates that substrates at 40 nm thicknesses proved to reduce the resistance to below 2 Ω, an acceptable level for electrode performance. This was however under idealised conditions, and doesn't consider surface roughness of the glass mounting slides. It was determined that a thickness of 50 nm (500 Å) be used to account for approximately 10nm surface roughness. At this point they are very sensitive to impurities and fractures. These results were later examined once substrates were manufactured and had undergone the etch process to better interpret their characteristics, in section 4.2.5.

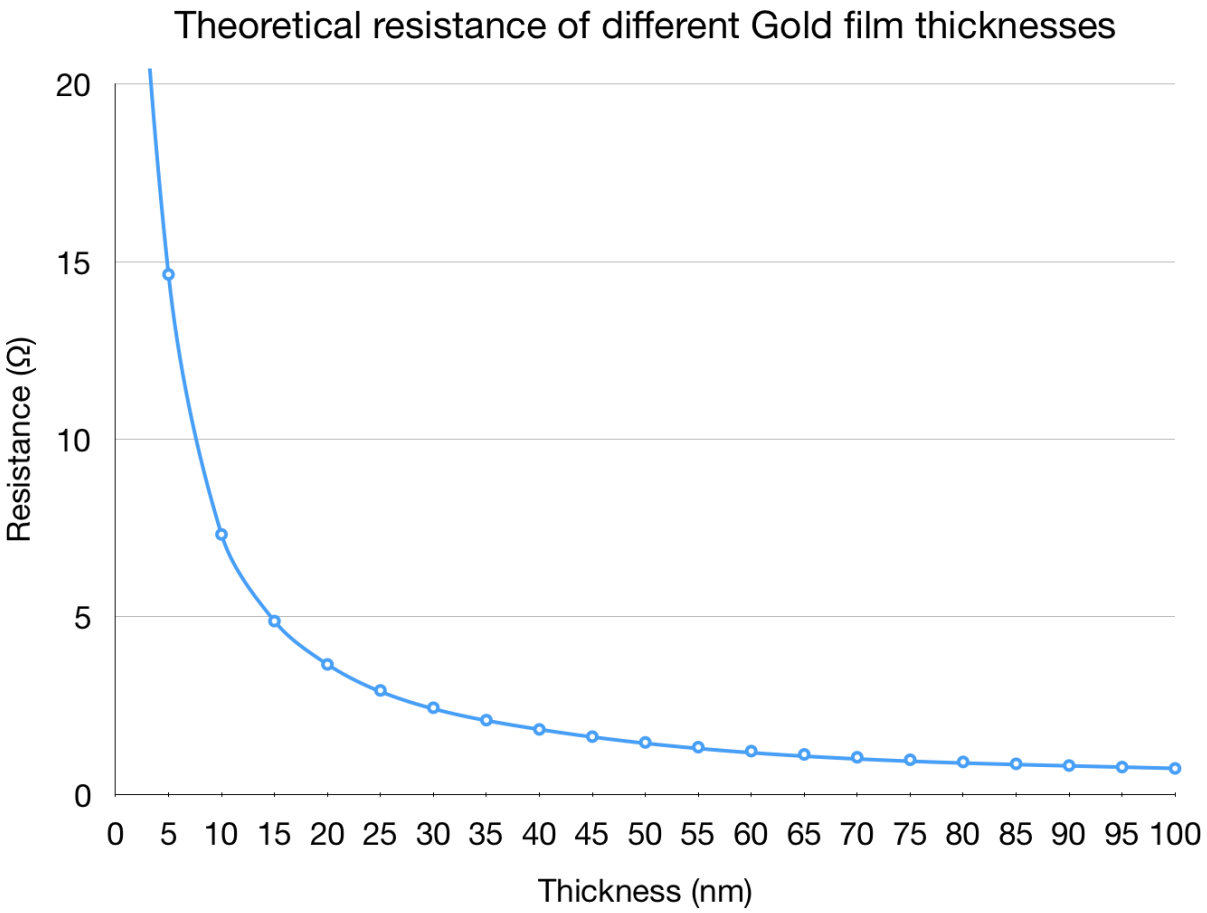

Fig. 3.5 Theoretical resistance of thin gold films.

3.2.5 Thiol Selection

Many thiol compounds are used for the functionalisation of gold surfaces, Mercaptoundecanoic Acid (MUA) was supplied with the original microcontact printing kit supplied by Platypus technologies. MUA is an 11 carbon chain molecule, with a carboxyl (COOH) group at one end and a sulphydryl (SH) group at the other, this molecule is essential to the nature of the self assembled monolayer (SAM) produced and ultimately provides the functionalising surface for the gold.

The thiol is critical to the microcontact printing process, and it wasn't satisfactory to assume that MUA would give the optimal properties to use as an etch resist layer. For this reason work was done to compare MUA against other thiols and measure the resist layers performance under an etching process [74]. Investigation used thiol molecules of varying carbon chain lengths as this plays a role in the characteristics of the thiol layer [75]. Two alternative thiols chosen to be used for the funtionalisation

of a gold film were Mercaptobenzoic Acid (MBA) and Hexadecane Thiol (HDT). In Fig. 3.6 we can see the structure of each of the molecules.

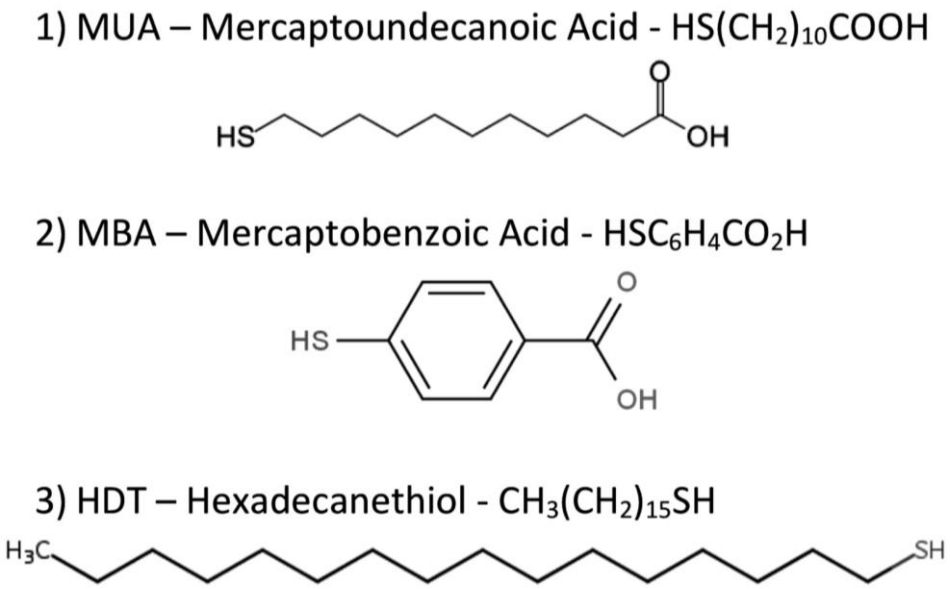

Fig. 3.6 Representation of thiol molecular structures. 1) Mercaptoundecanoic acid (MUA), 2) Mercaptobenzoic acid (MBA), 3) Hexadecanethiol (HDT)

MBA is a shorter molecule the chemical formula is, $HSC_6H_4CO_2H$, with a total of 7 carbons, there is a carbon ring of 6 carbon atoms and a total length of 4 carbons. Fig. 3.6 demonstrates that the molecule although shorter still has a relatively high mass giving rise to a potentially denser resist layer. It is supposed that this relatively high mass will prolong the etching time forming a thinner but stronger self assembled monolayer (SAM).

HDT was also used for comparison, the chemical formula is $CH_3(CH_2)_{15}SH$, this gives rise to an 16 chained molecule. The characteristics of this molecule is different in that one end has a SH terminating group as with previous molecules, however at the other end is a CH_3 group. This gives rise to an intensely hydrophobic group and makes etching with an aqueous etch very difficult. We can see in Fig. 3.6 a long carbon chain characterises the structure of HDT. Given the length of this molecule a larger mass was deposited on the surface giving rise to a thicker thiol layer and therefore better resistive properties. HDT is frequently used to functionalise a surface with an intensely hydrophobic layer, this is demonstrated Fig. 3.7 where a ball of water consisting of a few ml of water sits on the surface.

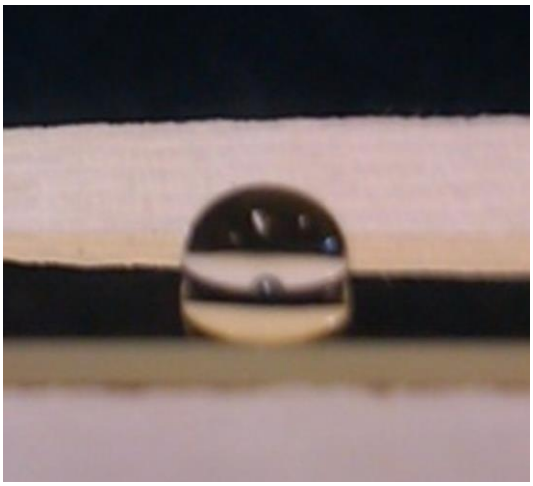

Fig. 3.7 Ball of water placed on a hydrophobic surface. The intensely hydrophobic nature is caused by an HDT functionalising SAM.

In order to consider resistance as a function of time it was evaluated from Fig. 3.12 that for a 20% etch concentration an etch rate of 0.457 nm/s. We deduce this from a height of 50 nm taking 109.33 seconds to etch completely. Applying this to a resistive property of gold a model was developed based on the initial resistance of the 50nm layer plus an additional resistance factor as a function of time that the etch is in contact with the substrate.

$R = R_i + R(t)$ (Eq. 11)

Where R = Final resistance, R_i = Initial resistance, and R(t) = Resistance as a function of time. Expanding the above and considering Eq. 10 whereby resistance is calculated, we can rearrange to form an equation for the height (h) in terms of time (t).

$R = (\rho L)/A$ (Eq. 10)

So:

$R = (\rho L)/(wh)$

Where L = length of gold region, w = width of gold region and h = height of the gold region

$R = 7.32x10^{-8} / h$

Solving for height (h) as an inverse function of time (t) due to the removal of material, then:

$h = (0.45x10^{-9} t)$,
becomes:
$R = (\rho L)/((w\ 0.45x10^{-9}\ t))$

Which simplifies to provide a function of R(t):
$R(t) = 73.2x10^{-9} / 0.45x10^{-9}t$
Therefore height can be defined in terms of speed and time, the speed being a constant dependent on the constant for a 20% etch solution of $0.45x10^{-9}$ m/s, this was established from etching 50 nm of gold in 109.33s in Fig. 3.12. Combining this function of R(t) with a function for the initial resistance we can establish:

$R = R_i + R(t)$ (Eq. 11)
$R = 1.37\text{^}((t - 60)/10) + 73.2 \times 10^{-9} /(0.457x10^{-9} \times (t – 60))$

Although the model produced the same shape as the measured values, it was noted that it required a translation to the right, hence the factor of (t – 60).

In order to test the performance of various thiols, 75 mm x 25 mm glass slides were coated with 100 nm of gold, each slide was then coated with a different thiol except for the control. The slides were left in solution for 10 minutes to allow adhesion of the thiol molecules via their SH terminating groups. The slides were rinsed of excess thiol solution before being left for a further 5 minutes to allow hybridisation to take place. Contact was made at the ends of each sample slide and then resistance measured every 20 seconds as the slide was immersed in 20% etch solution.

It was discovered that MUA and MBA provided the best results for SAM structure to use as resist layers. Hybridisation occurs as the molecular forces stabilise the self assembled monolayer to produce a more resilient layer. There is however a ratio

between mass and force even at this molecular scale, with more massive particles, greater forces are needed to stabilise the layer [58]. HDT has a long carbon chain in its structure terminating with a hydrophobic group this leads to a greater surface energy and when brought into contact with water a volatile response from the gold layer. From the results MUA remained the designated thiol of choice.

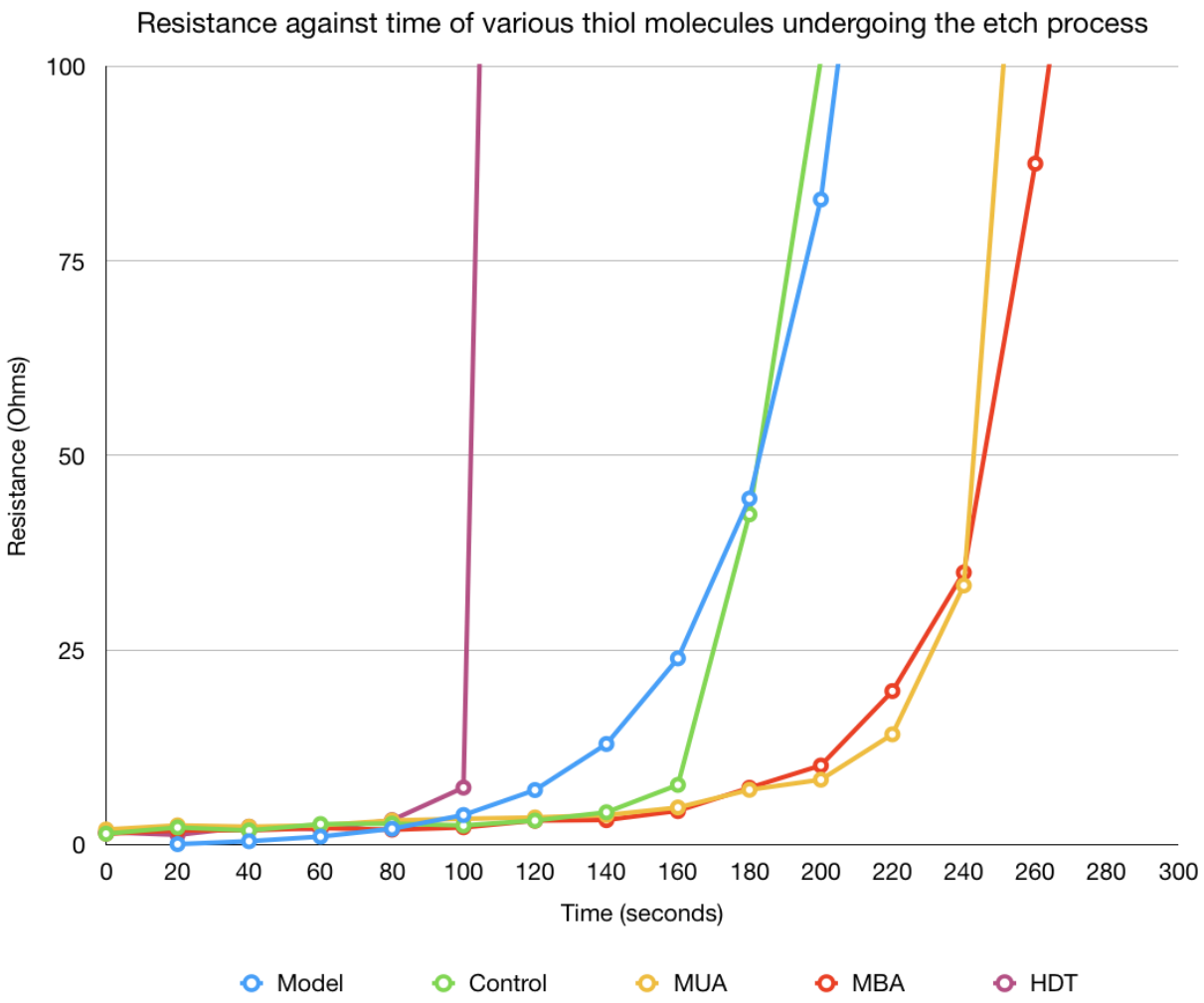

Fig. 3.8 Graph of thiol masking properties. Resistance plotted against time as thiols underwent a potassium iodide etch at a concentration of 20% in aqueous solution.

From Fig. 3.8 it can be determined that an optimum etch time for MUA is between 140 and 180 seconds. This is shown as the control (no thiol) graph curves between 140 and 180 seconds. This timing is based on a 20% etch solution. This timing is critical to maintaining a consistent etch gradient across the surface and clearly defining regions between the conductive electrodes and the non conductive spacings. The timings can be amended by increasing or reducing the concentration.

3.2.6 Thiol inking of stamp

In any printing process, ink is the fundamental ingredient to creating an image, and Microcontact Printing is no different, in this case it was a thiol used to ink a PDMS stamp for printing. A thiol is a molecular compound with a COOH (Carboxyl) terminating group that was used to bond to the PDMS stamp. This was aided via the bonding energy between the stamp and thiol. Upon completion of the inking of the stamp, the molecule exposed a SH (Sulphydryl) terminating group that was bonded to the gold substrate via a higher bonding energy.

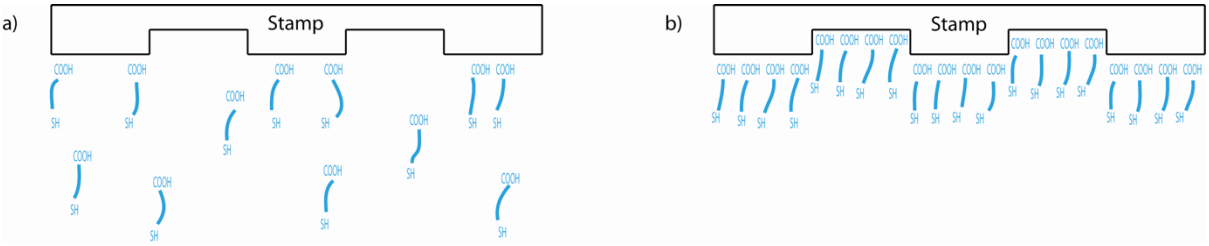

Fig. 3.9 Stamp immersion in alkanethiol. a) The PDMS elastomeric stamp was immersed in 1 mMol solution for 2 hours, b) Thiol molecules were bonded across the surface of the PDMS stamp via the carboxyl terminating groups.

When inking the stamp it was necessary to have the right concentration of thiol in a solvent, it was recommended to use 1 mMol in ethanol. A range of solvents were tried, but ethanol provided the best results, due to its rapid evaporation time on the stamp and also its relatively unaggressive nature compared to other solvents, methanol was successful as a thiol carrier but acetone, butanol and isopropanol proved to be too aggressive, breaking down the molecules and hindering transfer. Ethanol was therefore preferred given the recommended chemistry on provision of the kit [59].

Timing is also critical to allowing the molecules to adhere to the stamps, so the stamps were left in the solution for a period of 2 hours. This time allowed molecules to align themselves and bond, via their COOH group, to the stamp in preparation for printing. After this 2 hour period the stamps were removed and washed with ethanol to remove any excess thiol still left on the surface, the solvent is then evaporated before being used to print.

3.2.7 Printing of thiol

The thiol was printed directly onto the gold substrates to produce the resist layer, the stamp must therefore make conformal contact with the substrate to ensure clean transfer of the thiol to the substrate. The PDMS stamp has an elastomeric nature that allows for some flexibility across the surface when brought into contact.

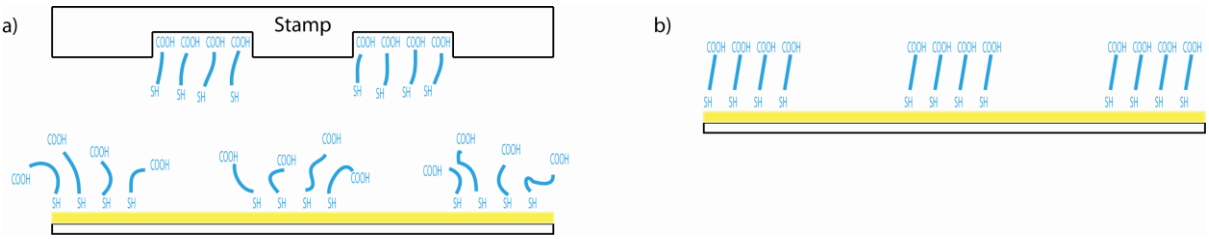

Fig. 3.10 Thiol transfer from the stamp to substrate. a) The stamp is brought into conformal contact with a gold substrate layer mounted on a rigid glass backplate, b) the deposited thiol monolayer undergoes hybridisation.

The chemistry of the thiols are such that they bond to the stamps using a COOH group, this was then brought into contact with the substrate and due to a higher bonding energy between the SH group and the gold, the COOH group was released from the stamp surface. The molecules, when deposited on the gold surface and released from the stamp, underwent hybridisation, a stabilising of forces as the molecules interact and align with one another. The result of this process was a more stable and resistive Self-Assembled Monolayer (SAM). The layer also has a small hydrophobic nature to it which can be used for further, alternative application.

3.2.8 Etching process

Careful attention needs to be focused on the etching process to ensure successful etching of the gold with high resolution and efficient removal of the unresisted gold. An etch solution at 100% has an etch time of 1 µm/min, which results in a very quick etch of around 3 seconds [61]; this could lead to hastening the experiment increasing the margin for error. Dilution of this solution would result in a longer etch time and therefore more control over the process itself. There were also fears for the SAM

being removed if the etchant was too aggressive, whereas even if the etchant performs a longer etching process on the MUA coated gold lines this process also would be slowed and could be monitored to find the optimum time for etching. Fig. 3.11 details the process of wet chemical etching exposing the desired conductive tracks.

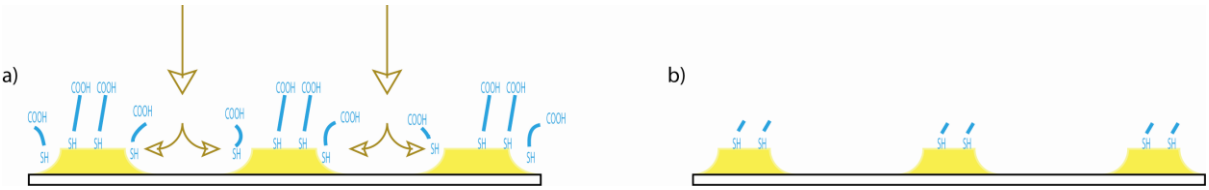

Fig. 3.11 Masking SAM layer undergoing wet chemical etching. a) Wet chemical etching exposes tracks under the SAM resist layer, and b) tracks with depleted thiol resist molecules left on the surface.

The initial investigation began with a crude etch of an Intel 486 computer chip, nonetheless the etch appeared successful and appeared to remove the gold coating on the pins. This provoked thought and discussion into the etching process and work began by using a step etch process, whereby a glass microscope slide coated with 100 nm of gold is etched in this solution to test the etching rate. The slide will be placed with about 10 mm in the solution and at various points lowered further in roughly 10 mm increments into the solution by using a suitable time frame and by building up an etching profile there is a possibility to work out the etch rate. If this rate is not satisfactory and appears too rapid an attempt to dilute the solution will hopefully slow the rate to control the etch.

A potassium iodide based etch mixed in solution at a ratio of 4g: 2g: 10ml is then diluted in deionised water which slows the etch rate significantly. To maintain consistency heat can be used to improve the performance of the etchant if the performance is slowed too much, along with this agitation also increases the performance of the etch. Experimentation will look to find a concentration that slows the etch to a rate that is not so aggressive and more easily manageable. In doing this discovery of the optimum concentration for the etch to be carried out at room temperature will be investigated, coupled with this, if the concentration of the etch

was lessened then it minimises the use of chemicals and proved both cleaner and cheaper.

Concentrations were made using the 4g KI: 2g I_2: 40ml H_2O solution described above diluted with H_20 to make various concentrations of solution; 10%, 20%, 30%, 40% and 50% which was followed by a step etch process, to try and build a profile for the best etching concentration. After the step etch process use was made of the opposite end of the slide to time how long a complete etch of the slide will take, with results demonstrated in Fig. 3.12.

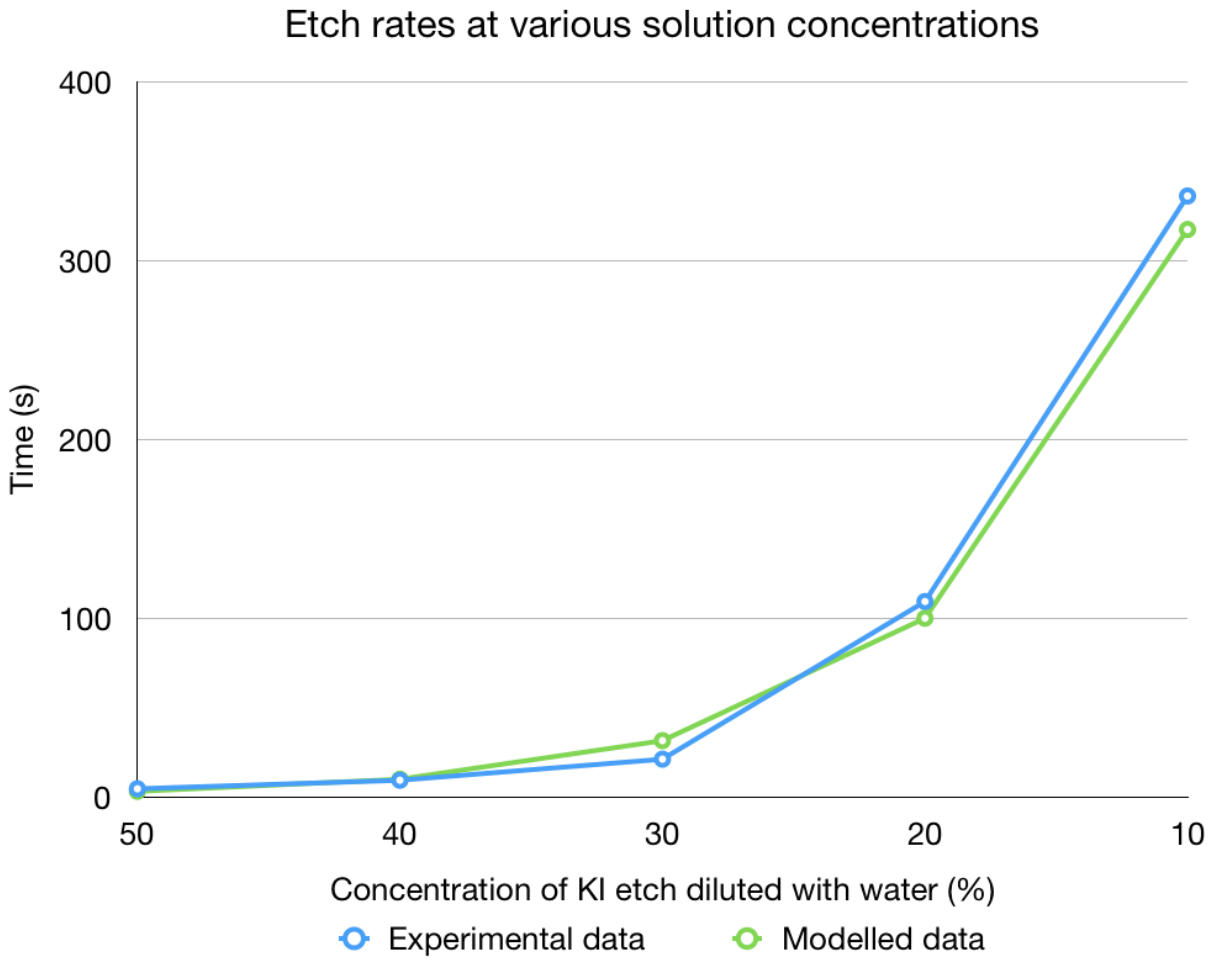

Fig. 3.12 Etch rates at various etch concentrations.

The model identified in Fig. 3.12 indicates a strong correlation with the measured results. The time taken for the gold substrate to completely etch increases with increasing dilution. The model developed is given by the formula below and is considered to be a factor of the etch rate for 100% concentration, which is 1 µm/min. The formula is derived below:

$T = (h/s)F_{conc}$ (Eq. 12)

Where h = height, s = speed, and F_{conc} = the factor of concentration. The height is 50nm or 5 $x10^{-8}$ m, and the speed of 1 µm/min or 1.667$x10^{-8}$ m/s, and the factor of F_{conc} is $2^{((50-conc)/6)}$.

Therefore:
$T = (5x10^{-8}/1.667x10^{-8}) \times 2^{((50-conc)/6)}$

Several interesting observations were made regarding the performance of the etchant solutions. When diluted and the activity of the solution inhibited, a non-uniform patch etch was found across the substrate surface. Dilution appears to be a problem that when H_2O diluted the solution the etching is slowed and more manageable but to the detriment of the etch uniformity. A process that initially took 1.67 seconds, when diluted then took 336 seconds, which is a remarkable increase and a partial success. However, concentration will need to be increased to balance the quality of the etch with the speed of the process.

Given the non-uniformity of the step etch process initially carried out, not all the samples gave the desired effect of a visibly progressive etch. It was noted in the first two concentrations; 10% and 20%, that significant amounts of substrate are still left on the slide despite being left in solution for over 5 minutes.

Another observation is that deposits were found on the reverse side of the slides, this is thought to be residue from the solution being deposited over clean areas of the slide, interestingly the deposits found decrease as the solution concentration increase. It was also noted that in the solutions of 10% and 20% debris was found in solution as the waste substrate was etched into the solution. However for higher concentrations no such particles were seen but the solution remained apparently clean. Etchant solutions can become ‘dirty’ and need to be disposed of, this has been observed with the 10% etch and is due to saturation of the solution, leading to the etching solution not being able to remove any more gold from the substrate. For the complete etch of the substrate it was observed that apparent saturation points

were reached for two of the solutions, 10% and 20%, leaving a display of partially etched slides.

The timings of the etch process were measured to the point of saturation or until the gold substrate was completely removed. Small deposits on the slides of 10% and 20%, the size of the deposits decrease as the concentrations increase. Optimal concentration from Fig. 3.12 suggests 30% as best for achieving the most expedient etch, at 21.13 s.

3.3 Progress and experimental procedure

Experimentation will continue by looking at combining the above patterning components. Microcontact printing kit for functionalising a gold substrate, made available from Platypus technologies, will now be used to investigate the previously discussed and established techniques. Independence from the kit will be of first priority before results are then evaluated and the performance of any conductive tracks or devices can be quantified and concluded. Certainties for the process at this stage are listed below:

1. A solution of 1 mMol was used to ink the stamp.
2. The PDMS stamps were to be left in solution for 2 hours.
3. The PDMS stamps were then air dried.
4. A potassium Iodide etch solution at 30% concentration was used to etch the substrates.
5. Deionised water was used to remove excess etch solution from the stamp.

Chapter 4
Print development

4.1 Investigation with kit

Using the microcontact printing kit good initial results gave rise to more flexibility to develop the necessary procedures of inking, stamping and etching to improve the printing techniques. The kit supplied was an off the shelf kit designed for those interested in the functionalising of gold layers, at the time of purchase, the kit cost $495, for 3 gold slides and a sample of MUA. It was not designed for etch purposes, but for manipulating surface chemistry for depositing organic material. During the process, areas that need some vast improvement to generate a working demonstrator were uncovered. As work continued a log was compiled of significant progress with certain print trials providing milestones as well as new issues to tackle. This chapter provides successive print conclusions showing the stages of progression. These print results begin with detailing the use of the commercial available microcontact printing kit supplied by Platypus Technologies. The next chapter moves towards autonomy from commercially available components, utilising the manufactured slides and stamps. The print trials described here and in the next chapter are not exhaustive but demonstrate key stages of moving towards independence of the kit and then work towards conductive structures. For this reason each print illustrates a significant step in progressing the techniques, the observations and conclusions of significant print trials are discussed.

4.2 Print runs with kit

4.2.1 First print trials, track splitting

Initially a PDMS stamp was immersed for 2 hours in a 1 mMol concentration of MUA ink held in solution/suspension by an ethanol carrier. This allowed the carboxyl groups of the thiol molecules to bond to the stamp. Given that the ethanol carrier evaporated at room temperature, it must be kept in a sealed container. As the process for inking the stamps neared an end the substrates, 50 nm (500 Angstrom (Å)) gold films deposited over a microscope slide with a titanium adhesion layer,

were prepared by washing them with ethanol to remove any additional thiol molecules.

The stamps were then removed from the thiol solution and once the excess solution was rinsed from the stamp surface, this was then allowed to dry in ambient air. A nitrogen supply could have been used to speed the process, but ambient evaporation for 30s proved satisfactory, using a microscope it was clear to see when all the solvent had evaporated. The stamp was then brought into uniform contact with the substrate and gentle pressure applied to the reverse of the stamp to ensure contact. The stamp was then left for a period of 10 seconds to allow time for the thiol to bond to the substrate by the free SH end group. The stamp was then peeled from the surface by a simple lift off technique by hand and as it was removed, a SAM (self-assembled monolayer) was transferred to the surface of the stamp. The substrate was left for a further minute to enable the SAM to undergo the process of hybridisation, a stabilising of the monolayer as the molecular forces balanced the free chains.

Once the substrate had been left for a period of 1 minute, the substrate was then subjected to an etching process, the etch was the Potassium Iodide (KI) aqueous etch as described in Section 3.2.8. A dilute etch at 30% concentration was made. As discussed in the last chapter a 30% concentration of etch solution was found to be optimum giving an etch time of approximately 21.13 s. The reduced speed of the etch will aid contrast between the masked layer and the area to be etched.

Results and observations

During this print trial linear structures were formed on the glass slide, which demonstrated early success of the Microcontact printing process. The initial and most visible problem that occurred whilst printing is that of no thiol transfer to the substrate in certain areas. The tracks were not continuous and therefore not conductive. This resulted in partially printed tracks and track splitting. Confocal microscopy was used to determine the structures that had been printed and Fig. 4.1 illustrates the results of the cross section of a track that had seemingly no thiol deposit down the centre of the track.

Given the observations made of the results the most notable concern is the quality of the structures produced. It would appear that there are no continuous lines across the substrate of length 10 mm (the length of the linear stamp structures supplied by platypus), but there were clearly defined linear features. A conductive linear pattern was not successfully printed across the entire slide.

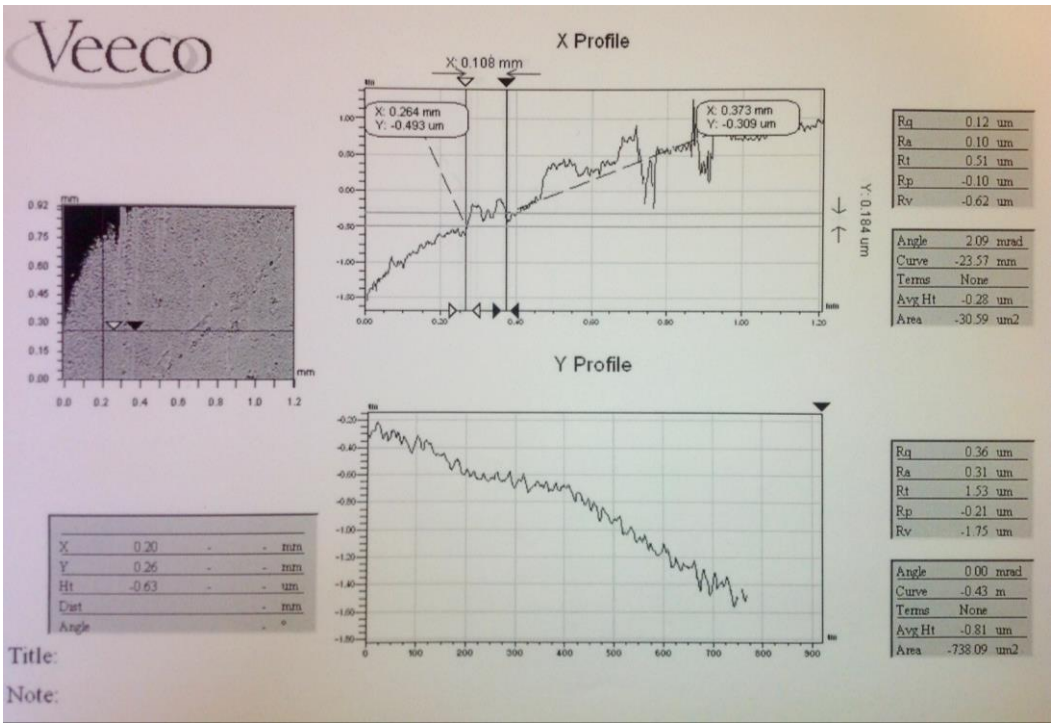

Fig. 4.1 Confocal microscopic cross-section of a printed track. A measured width of 108 µm on the X Profile (top), also shown in the profile is the height dropping in the centre due to ‘track splitting’.

Firstly, the lack of equal pressure across the whole stamp could lead to incomplete transfer. Given that the thiol solution is transferred to the substrate and this transfer relies on the contact between the stamp and substrate to deposit a monolayer onto the surface. If pressure was not consistent across the stamp surface then only parts of the linear structure would be deposited and an inconsistent line seen. A solution to this problem was suggested that the stamp be left in contact with the substrate for a longer period of time, allowing a greater amount of thiol to be transferred and a more consistent SAM produced.

Secondly there was an area imprinted around the pattern in question where it appeared etching occurred faster than across the rest of the slide. The cause of this

is not entirely known and speculation would say that where the stamp was removed a part of the gold substrate was also lifted from the surface of the glass. It is also hypothesised that when the PDMS stamp was rinsed off with ethanol, it was not dried correctly and deposits were left on the edge of the stamp and acted to increase the etch rate. This is not entirely satisfactory as the thiol solution is ethanol based and therefore the problem should have occurred across the printed area not just at the sides. Another explanation could be that where the stamp is in contact with the substrate and pressure is applied to attempt an equal stamping, most of the force is applied in the PDMS stamp to the peripheral parts of the stamp which alters the substrate on the surface allowing a faster etch.

Thirdly and perhaps most importantly, it was observed that the formation of the SAM over the surface of the substrate appears inconsistent. It would appear that at the end of the linear patterns there was bridging between track boundaries suggesting that the entire line had not been printed and actually the structures were very thin lines joined at either end with voids running down the middle of each track; this would undoubtedly increase the resistance of the tracks and reduce performance. It was also noted that there was bridging at midpoints on the tracks indicating that the SAM had not been correctly assembled. The thiol may deposit from the outside of the lines towards the centre in which case a longer transfer time would combat this to allow maximum transfer completely along the printed lines. Time is needed for the monolayer to bond to the substrate allowing it to act as a sufficient resist layer. Having looked at the structures under a microscope it was possible to see that certain lines have partially printed successfully while others experience this problem of track splitting.

Conclusion

There were immediately identifiable areas for improvement, the transfer between the stamp and the substrate, including the pressure used to maintain this contact. Given the prescriptive nature of inking the stamp it is assumed that at this stage the stamp is fully inked and the poor quality print is as a result of the printer’s inexperience rather than the incomplete inking of the stamp.

The initial test for printing 100 µm track and gap lines was successful and produced mixed results, there were definite linear structures formed on the gold substrate as seen on the confocal microscopy image analysis in Fig. 4.1. When these substrates were etched clear, although incomplete, gold tracks were visible. The lines were inconsistent across the surface in terms of quality and further tests need to be performed to try and perfect the printing technique. Increased contact time between the stamp and substrate was used. Also, the addition of a standard weight to help aid uniform and complete contact was introduced to subsequent print trials.

4.2.2 Improving the print techniques

The aim of this print was to produce linear gold tracks of width 100 µm track and gap without track splitting and maintaining a consistent print across the entire print surface. The issues raised in the previous print were modified to consider the dwell time of the stamp. Attention focused on creating uniform pressure across the interface of the stamp and substrate and thereby a comprehensive deposition of the monolayer for etching.

Method

The stamp was immersed in the thiol solution for a period of two hours as described previously, knowing that the time provided satisfactory adhesion of the thiol ink. Whilst the stamp was inking the etch solution was prepared and the substrates manufactured by the process of sputtering and then were rinsed to remove surface impurities.

When the stamp was brought into contact with the substrate, a weight of 95g was immediately placed on the reverse for a period of 1 minute. The weight was then removed and the stamp left for a further 2 minutes to allow bonding of the molecules to the gold substrate. The stamp was then removed and the thiol left to undergo hybridisation for a further 2 minutes, after this time the inked substrate underwent the etching process to expose the linear structures.

Results

Observations appear to have solved the issue of track splitting with the addition of weight and longer contact between the stamp and the substrate. It would appear that some faint lines with regular linearity were produced; this occurred only over a portion of the stamp surface showing that the weight used to apply pressure to the stamp may have been unevenly weighted.

Conclusion

This print stage was successful at producing linear tracks that appeared to solve the issue of track splitting. There remains several concerns about the quality of the printed region. Linear tracks appeared to be incomplete. However, the linear structures produced did appear to have over come the problem of track splitting. Two main variables were explored for the incomplete print: an uneven distribution of weight, and a lack of transfer of thiol ink either between the solution and stamp or between stamp and substrate.

It was also noted at this stage that the slides produced by sputtering performed as well as the slides provided by Platypus technologies. There appeared to be a greater structural integrity with the slides provided by Platypus this was due to the inclusion of a titanium adhesion layer that gave structural support to the gold, which is very ductile at low thicknesses. The titanium layer was primarily introduced to support the gold during carriage. Good quality prints were being produced at this scale without a titanium layer and therefore work continued without an adhesion layer.

4.2.3 Improvement of the etch solution

Whilst worked had focused on the transfer of thiol ink, little attention had been paid to the etch solution. In this print trial a solution was sought over the control and timing for the etching process. It was hoped that a standardised etch process can be confirmed for future print trials. An etch solution of 30% was established from experimentation in Section 3.2.8. Issues surrounding immersion and timing still remained unanswered.

Method

Various methods of exposure of the substrate to the etch solution were explored. These included immersion, spraying, dripping and beading over the print area. The best results were found by simple immersion, if the concentration was reduced sufficiently, the etch gradients caused by introduction of the substrate to the solution were seemingly insignificant.

A stamp with linear structures 50 µm track and gap and 10 mm in length was immersed in a thiol solution to ink the stamp in preparation for thiol transfer onto the gold substrates. Whilst this was carried out an etch solution of 30% strength was made for use in the subsequent etching process. In preparation the gold substrates were prepared by rinsing with a solvent wash.

Once the stamp had been inked, a weight was then placed on the reverse of the stamp to aid conformal contact between stamp and substrate. The same process of 2 minutes with the stamp in contact, and 2 more minutes for the thiol to undergo hybridisation, was applied. At this point the substrate would be exposed to the etching solution for a period of 20 seconds, at an etch strength of 30%. Preliminary trials indicated that this time proved to be optimal for the etch to take effect.

Results and observations

Concerning the etching of the gold substrate it appeared to have been successful. There was a vastly improved etch gradient across the surface of the print leading to a better contrast of the linear structures which can even be seen with the naked eye. It was noticed that these structures were still not conductive. Given that more comprehensive print trials were being produced, they were placed under a Scanning Electron Microscope (SEM) for analysis.

One observation was that the etch appeared to have penetrated the thiol resist layer and etched part of the track that was previously masked by the SAM. In Fig. 4.2 a clearly defined track can be observed.

Conclusions

The sufficiency of the etch solution at 30% etch strength gave a clear etch gradient. The high resolution, contrasting etch gradient between the glass slide and the gold tracks, led to good edge definition. The etch appears to have etched the gold tracks, albeit to a lesser degree leaving a clear track without a continuous conductive film of gold. There are several explanations for this phenomenon: pinholes, underetching, and overexposure to the etch solution. This serves to reaffirm how critical the timings for the etching process were, for 30% etch solution, 20 seconds proved to be optimal.

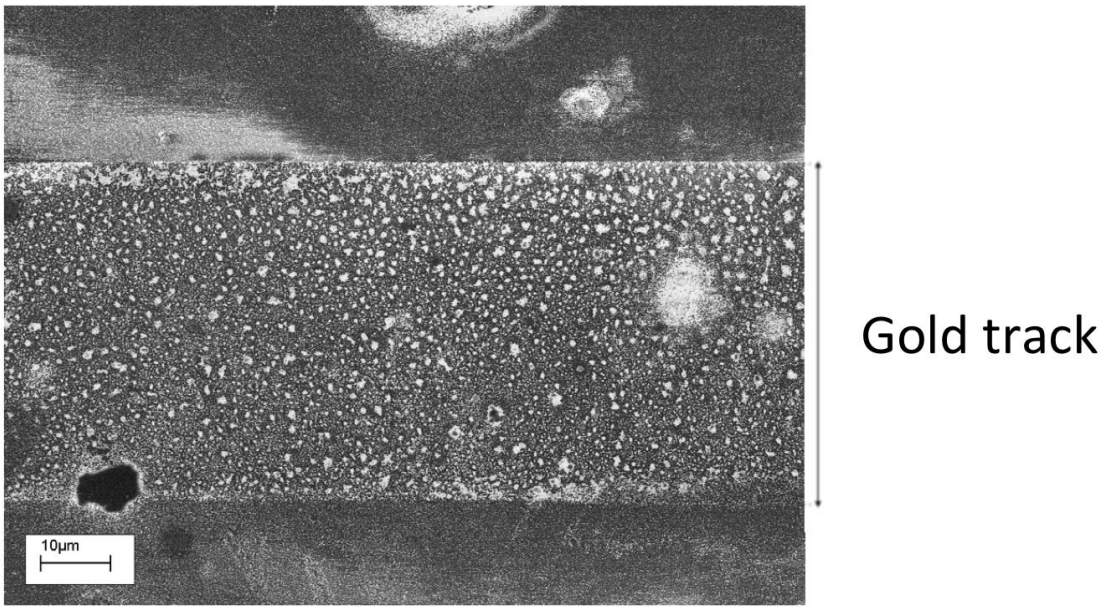

Fig. 4.2 A 50 µm non-conductive track. An island formation previously masked by the thiol resist layer.

4.2.4 Confirming the substrates

This trial aimed to understand the comparative effect of using vapour deposited substrates instead of using sputter coated substrates. To this point substrates were manufactured using sputter coating. Given that partial etching of the track occurred, a 50 nm layer etched to around 20 nm, the method of manufacture for the substrate could have caused a difference in conductivity. It was anticipated that vapour deposition would reduce the speckled gold effect on the glass slides that appeared as islands, possibly produced by the sputter process characteristics.

Method

Sputter coating uses a gold target and an electron source. The electron source ‘fires’ electrons at a target and effectively chips gold ions out of the target. The ions are then ionised in an argon rich plasma environment and are propelled towards the microscope slide. The benefits of sputtering are that it is a relatively fast process, as the vacuum required to sputter is typically 10 Pa rather than $0.1x10^{-3}$ Pa for vapour deposition. Vapour deposition uses a very high resistance to generate heat for boiling the substrate, meaning Sputtering is lower cost and quicker.

During this print the stamp was left in solution for exactly 2 hours, a 30% etching solution was made up ready for the process. After preparation of the 500Å gold coated slide by rinsing with ethanol, the stamp was left in contact with the substrate with a 95 g weight placed on the reverse to aid contact across the entire surface of the stamp. The stamp was weighted for 1 minute before being unloaded and left in contact for a further 2 minutes to aid transfer. After being left for a further 2 minutes to allow for hybridisation to occur, the substrate was then immersed in the etching solution to reveal patterned gold tracks on the glass microscope slide.

Results and observations

Fig. 4.3 is a micrograph comparison showing an etched sample of a vapour deposited sample (left) alongside a sputtered sample (right). We can see that similar features are observed, using vapour deposition did not alter the final pattern of the gold substrate. There was still an island formation with no conductivity. However it is also important to note that there was a higher concentration of gold deposit where the tracks should have been which indicated similar results as when sputter coated samples were used.

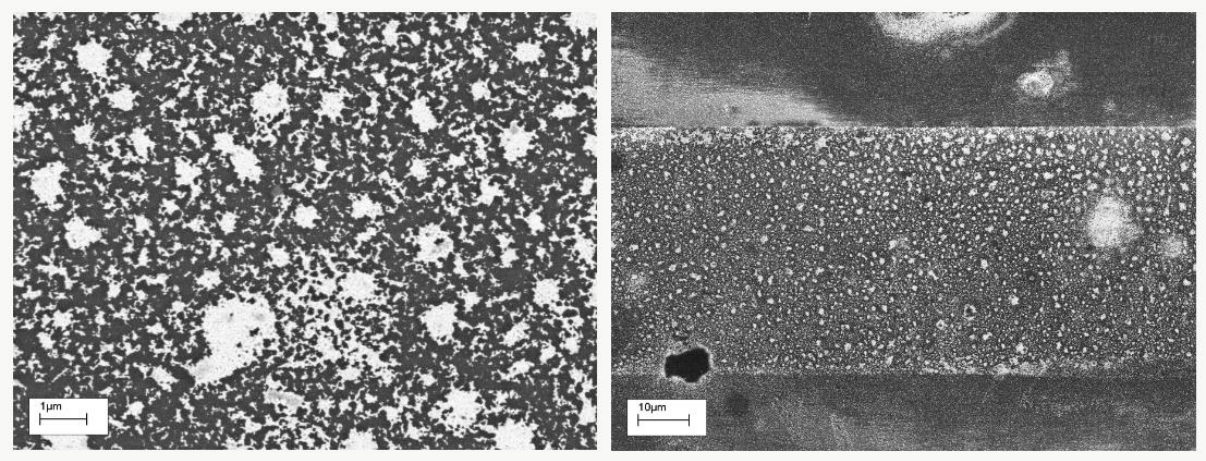

Fig. 4.3 Vapour deposited and sputtered gold layer comparison. Non-conductive islands, vapour deposited (left) and sputter coated (right) on a glass mounting slide. Although different scales we can see a clear isolated conductive regions in both micro graphs.

Conclusion

This print demonstrated that there is little difference between sputter coating and vapour deposition when manufacturing the gold substrates. We find that the samples still produced a speckled island effect to the gold substrate. The spread of conductive regions suggested that the lack of conductivity was probably caused by pinholes in the surface of the thiols SAM resist. Were the pattern caused by underetching of the tracks we would expect a gradient of density from the boundaries to the centre of the tracks. What was observed in both trials was a fairly even degradation of the tracks, and in some cases, a higher density at the boundaries.

Sputter coating was continued to be used based on the speed and performance of the results produced. Attention was then shifted onto the thickness of the gold substrate and whether an increased thickness will increase the etch gradient over the gold substrate.

4.2.5 Substrate thickness

Substrate thickness was then explored that could potentially help increase the etch gradient across the stamp. Given the previous success it was suggested that by

increasing the thickness of the gold layer it would be able to produce a greater contrast between tracks and gaps. The etch process appeared to be slowed, not prevented, by the existence of a thiol resist layer. Would starting with a thicker gold layer emphasise this effect? or do we find that all thiol has been removed from the surface and the substrate undergoes the standard linear etch as experienced in other print trials?

Method

By this stage an established method for printing had been developed and was used again here to print a SAM. The stamps were immersed in a thiol solution for 2 hours, during this time the gold coated slides were prepared by washing them in an acetone bath. The stamps were removed from the solution and any excess rinsed off using ethanol. Once in contact with the substrate a 95 g weight was applied to the reverse of the stamp to aid uniform contact across the substrate. This was left for a period of 1 minute, before the weight was removed and the stamp left for 2 more minutes to aid thiol transfer. The stamp was then removed from the surface of the substrate and left for a further 2 minutes to allow the SAM resist layer to undergo hybridisation. A pre-prepared etch solution was made at 30% etch strength as previously done. The substrate was then immersed into the etch bath, the etching process time varied depending on the thickness of the layer.

Initially, the results from Fig. 4.4 were achieved using a microscope slide coated with various thicknesses of Gold. Microscope slides with dimensions 75 mm x 25 mm were sputter coated using a Cressington 306r vacuum chamber device. They were coated with gold using an Argon plasma to varying thicknesses. Samples were manufactured at 10 nm, 25 nm, 50 nm, 75 nm and 100 nm. The surface roughness of the slides was specified as ±10 nm. Once coated, contact was made using a conductive epoxy adhesive, the same adhesive was used on all samples. The epoxy was delivered 5 mm from both ends of each slide before contact was made using crocodile clips. Once constructed the resistance of each sample was measured using a Fluke 787 multimeter. The experiment was repeated with 3 slides in each thickness category and averages taken to ensure accuracy.

The graph demonstrates that at thicknesses below 50 nm the resistance of the gold slides increases significantly. Once the gold slides have undergone the etching, the affected resistance is only increased suggesting the slides should start with enough gold mass to lower the resistance to a reasonable value, before being etched. From the graph it is noticeable to see that gold film thickness between 50 nm - 100 nm gives preferable conductivity as the larger amount of gold allows for better conductivity.

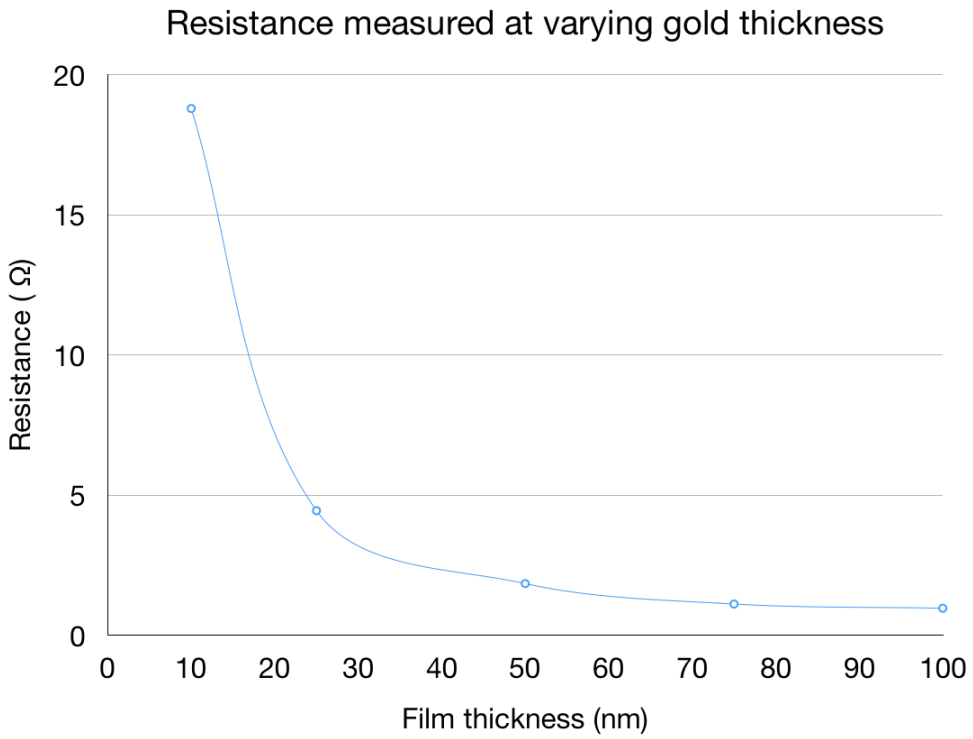

Fig. 4.4 Sheet resistance of varying gold film thickness.

Until this print the substrates were manufactured to a thickness of 50 nm so for comparative purposes, the print that comprises this section was manufactured to a thickness of 100 nm. The critical aim for printing was that resistance remains low along the tracks, whilst in the spacings between electrodes the resistance significantly increases. The sharp rise in resistance with lower thicknesses as detailed in the graph meant the timing would be critical to drawing the distinction between conductive and non-conductive regions. Individual electrodes were not measured due to the resolution of the features, given this limitation the effects of temperature on the conductive layers was not fully explored in the context of interdigitated electrode arrays. Work was completed in section 6.2.2 to find the

reactance of the devices to model instantaneous Power (P_i). These results are consistent with the model for resistance developed in section 3.2.4, these results were then compared and comments made in section 6.1.2.

Results and observations

It is interesting to note that the slides manufactured with a thicker deposit of gold appear to have produced clearly defined regions. Although an inverse print appears to have occurred. This observation can be see in the micrograph Fig. 4.5. The exact same process was used to print and Fig. 4.5 details an example of a repeated pattern seen where the tracks appear to have been etched more than usual. Gold deposit remained where the electrode regions should be, this result was not a one-off event.

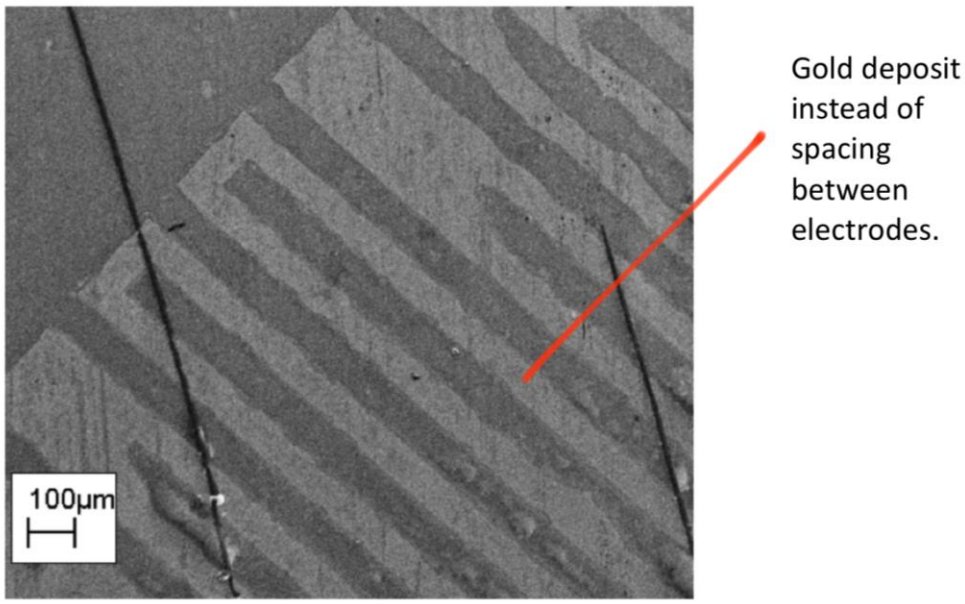

Fig. 4.5 Micrograph of inverse results with 75 µm track and gap.

The gold regions, albeit reversed, were still not conductive across the surface. However we were continuing to see clearly defined tracks formed on the substrates.

Conclusions

Drawing on the results produced by using 100 nm thick gold film deposits it is noticed that increasing the thickness of the gold film did not result in producing better

results. The critical etch point appeared harder to distinguish at greater thicknesses. As the stamp was brought into contact with the very fragile layer, the gold collapsed creating regions of more gold per unit area on the surface and therefore regions that took longer to etch. Given the progress so far it was decided to continue using 50 nm gold film deposit for future prints.

4.2.6 Manufactured stamps

Until this set of prints most work had been carried out with stamps supplied by platypus technologies. The stamps supplied by platypus technologies are a silicone elastomer called PDMS (PolyDimethyl Siloxane) and have feature sizes of 100 µm track and gap spacing and total length of 10 mm. The platypus stamps were designed to print simple linear tracks, not interdigitated arrays. Stamps have been manufactured independently with a desired pattern for printing an interdigitated electrode array as described in section 3.2.3. For this a silicon wafer master produced by Peter Lomax of The Scottish Microelectonics Centre (SMC) was used. A range of 15 stamp geometries was designed using Adobe Illustrator. This artwork was sent to the SMC, subsequently the template was used to mask a 3 in wafer. Three silicon wafers were produced by reactive ion etching to a depth of 10 µm, at a cost of £1,500. To mould the stamps and they were then removed by hand using a peeling process. Interdigitated features of varying sizes have been manufactured from 10 µm to 100 µm, and were substituted directly into the printing process to replace the Platypus stamps.

Method

The manufactured stamps had significantly more defects due to the shape and manufacturing process. The stamps supplied by Platypus technologies were a linear design and therefore easier to remove form a mould, it was also thought that the stamps were reactive ion etched after manufacture to remove impurities. This would allow for the use of mould release agents in manufacture and dramatically change the surface finish to the stamps. Using mould release agents, most likely a polysiloxane would lead to possible crosslinking with the PDMS and significantly impair the surface chemistry of the stamps destroying their capabilities to then bond to a COOH group at the end of the alkanethiol.

The standard technique developed was used for printing. The platypus stamps were substituted for the manufactured stamps. The manufactured stamps could begin print development towards functional devices. High electric field generators were the target component with application initially towards EL displays.

Results and observations

The use of manufactured stamps with the desired pattern in relief was successful. A structure of 50 µm track and gap was produced, suggesting very promising results. At this 50 µm scale the tracks were visible to the naked eye which show signs of promise. Even though they did not appear to be conductive, much higher gold deposits were left in the track regions of the glass slide after printing. Conductivity was measured across the contact regions at either end of the electrode array. If the structure showed promise of conductivity, a conductive epoxy resin was used to measure resistance across the structure as demonstrated in Fig. 4.6.

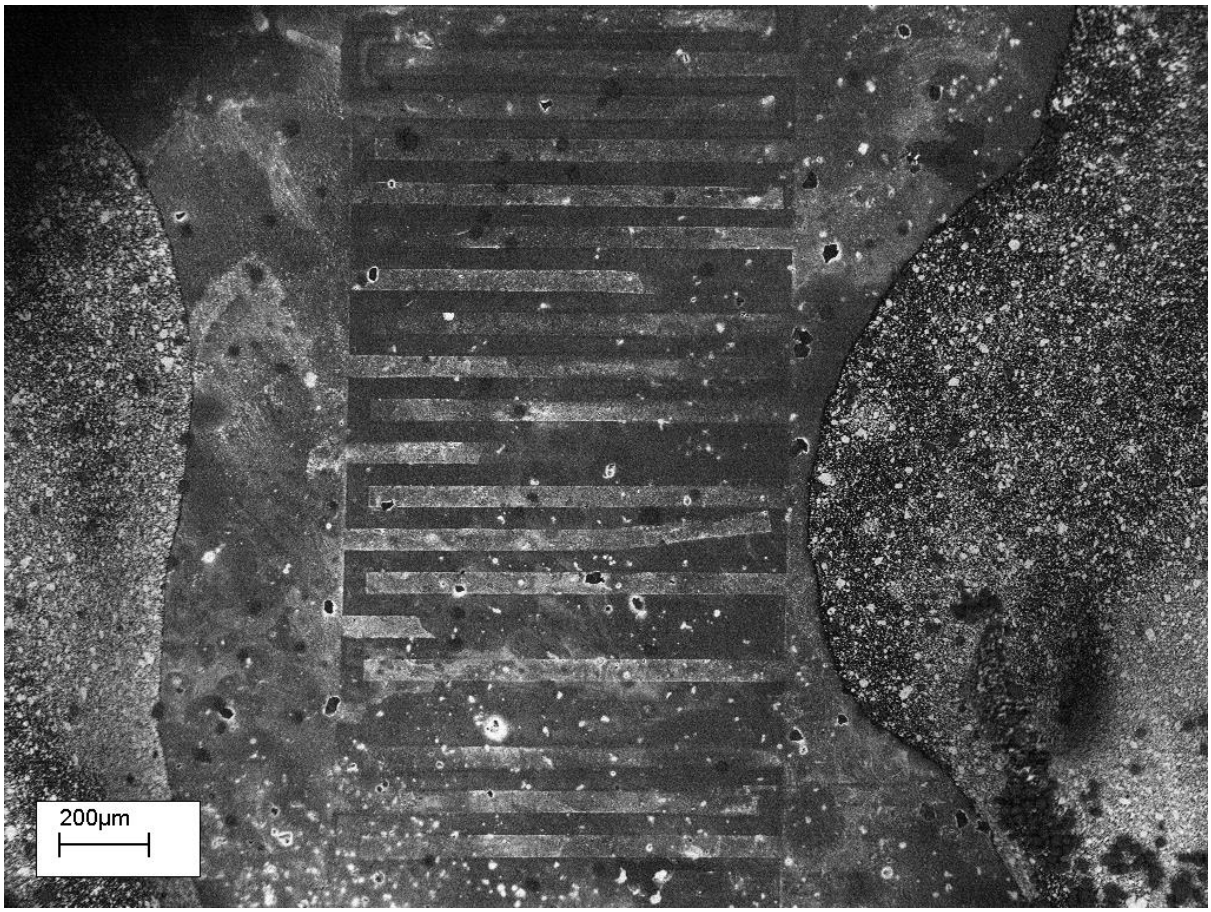

Fig. 4.6 Non-conductive 50 µm track and gap patterning, this geometry is a 90 rotation from Fig. 1.3 and illustrates horizontal electrode structures with a gap

running back and forth between them. Conductive epoxy resin used to make contact with the electrode array, and visible to the left and right of the micrograph.

From the above image it is possible to see clearly defined tracks, it is noted that the use of contact pads at either end of the design appears to have increased the transfer of the thiol resist to the substrate providing a more comprehensive resist layer.

Conclusion

It was discovered that the stamps produced using a silicon wafer master have produced successful prints and demonstrated early signs of conductive tracks for use in electroluminescent displays. The use of contact pads on the design of the stamps had led to a more stable print surface allowing better transfer of the thiol to the stamp. Work then commenced on improving the print quality at this scale of 75 µm before attempting to print finer track and gap thicknesses.

4.3 Finalised print process as independent of the kit

To summarise this chapter a brief overview of the print process used is documented below, this constitutes the optimal properties for printing conductive tracks. Whilst there were variations to the process for other applications it was discovered that the steps below proved most reliable to producing robust conductive patterned structures:

6. Prepare a 1mM thiol solution in an ethanol carrier.
7. Prepare etch solution at 30% concentration for use in the etch process subsequent to printing.
8. Clean the stamp using an acetone bath, do not over expose as acetone can cause swelling of the PDMS stamp due to porosity.
9. Place the stamp in the prepared thiol solution for a period of 2 hours, to allow bonding between the COOH group and the stamp.
10. Clean substrate with a solvent bath and evaporate any excess left on the surface using a gentle stream of air.

11. Remove the stamp from solution and wash the surplus solution off using ethanol and a gentle stream of air to evaporate excess ethanol.
12. Bring the stamp into conformal contact with the gold substrate and apply gentle pressure to ensure uniform contact, 10 mm height on the stamp should provide ample gravitational force to make uniform contact. A weight of 95g can be placed on the reverse of the stamp to aid conformal contact.
13. Leave for 2 minutes to allow chemical transfer of molecules from the stamp to the substrate.
14. Remove stamp and leave for a further 2 minutes for the functionalising layer to undergo hybridisation and stabilise.
15. Immerse the substrate in the 30% etch solution for 20 seconds whilst gently agitating.
16. Clean the excess etch solution from the surface of the substrate.

4.4 Outstanding objectives

With problems having arisen from the resistivity of the tracks and the inherent relationship that has with conductivity, attention on conductivity could be quantified based on the reciprocal results for resistivity. Whilst successful printing of a thiol resist layer had been achieved, there was no conductivity recorded along the tracks. Attention then focussed on taking the techniques and experience developed previously and building towards printing viable conductive samples for characterisation. Work from here commenced with the 75 µm track and gap structure to produce a functional device. Once achieved attention can then focus on reduced the feature sizes and increased yield.

Chapter 5
Print resolution

5.1 Independent print experimentation

Given the progress made with the microcontact printing kit and preliminary development of the techniques used as independent print runs, attention then turned to the development of the quality of the prints.

Having analysed each stage of microcontact printing to understand and develop each stage of the process, attention turned to employing the combined stages to form viable print runs to produce gold conductive tracks. Microcontact printing when used to functionalise gold surfaces is a relatively common practice in the development of biosensors, hence particular attention must be focussed on combining this with the etch process, and the interaction with the functionalised substrate to generate conductive tracks. The work must now evaluate the success of the established process at printing gold electrodes for use in a variety of components, but at this stage limited to electroluminescent displays. This is an order of complexity greater than functionalised surfaces as the attention switches from the surface chemical properties, well known and documented, to the physical conductive potential of the system. For this reason analysis of the subsequent print trials will focus on the structural and electrical reliability of the gold tracks as revealed during the process, quality in this context is defined as the potential for the tracks to conduct along their entire length whilst maximising durability of the tracks.

It is acknowledged that due to the design specified, partial conductivity will also produce positive results of high electric field generators, and therefore electroluminescent displays. For the best results conductivity needs to be maintained along the entire length of the tracks however even partial prints will be evaluated for their efficiency and success.

In section 5.2 a set pattern of apparatus was used to print and quantify results. In addition to the process developed in section 4.3, a selection of PDMS elastomeric

stamps proved successful at patterning gold for conductive purposes. These stamps included: a 75 µm track and gap with dimensions 1 mm x 3 mm, a 50 µm track and gap with dimensions 1 mm x 5 mm and a 25 µm track and gap with dimensions 3 mm x 3 mm. MUA was used for patterning throughout section 5.2, and substrates were produced with 50 nm gold layers. 30% etch solution was used throughout and never reused.

The Cressington 306r vacuum deposition instrument was used to manufacture all substrates through sputter coating in an argon plasma as described in 3.2.4. Stamps were all produced through the moulding techniques developed in section 3.2.2. A Fluke 787 multimeter was used for the initial characterisation of conductivity, and MG chemicals silver conductive adhesive epoxy was employed to fix wires in contact with devices in the contact regions. A Power supply ran through a handheld SparkFun inverter battery pack. A telescopic optical probe (TOP) 200 was used to measure the luminance emitted by supplying varied voltages and frequencies.

5.2 Further print investigation

5.2.1 Optimising print conductivity at 75 µm track & gap

The desired electrode array is a capacitive structure and therefore not directly conductive. The devices were theoretically quantified in Farads previously in section 3.2.2.1. Contrast between regions on the glass substrate were critical to providing a robust electrode array structure. A common issue that occurred was short circuiting.

Method

The standard print technique as discribed in section 4.3 was used for inking, printing and etching. However, since there was little possibility of testing success by making contact with the individual interdigitated electrodes, light output from successfully printed devices offered a quantifiable measure of success. A simple step by step test for measuring the quality of the prints was developed. Initially, the conductivity of the contact pads were tested. If conductive, then a conductive epoxy resin was deposited to attach the contact pad to a current carrying wire that could be used to supply an alternating current, and measure reactance. Finally a phosphor ink was then deposited across the surface using a simple mask to deposit a phosphor layer

of around 50-100 µm. An alternating current was supplied, if an electric field was produced the particles were excited and emitted light.

The structures require a high field strength to be stimulated. If a single track was not conductive on the 75 µm device, the next opposing electrode is 375 µm away, at which point the voltage supplied would have needed to be considerably higher. If one track was not conductive it would be unlikely to produce any light, but if light were produced along an electrode it was evidence that adjacent electrodes were conductive.

Results and observations

From this set of print trials, many structures failed to conduct in the contact region. Of the structures that did conduct, few demonstrated a significantly high enough resistance for use as high electric field generators. Fig. 5.1 shows a micrograph of the 75 µm track and gap electrode array before phosphor ink was deposited over the surface.

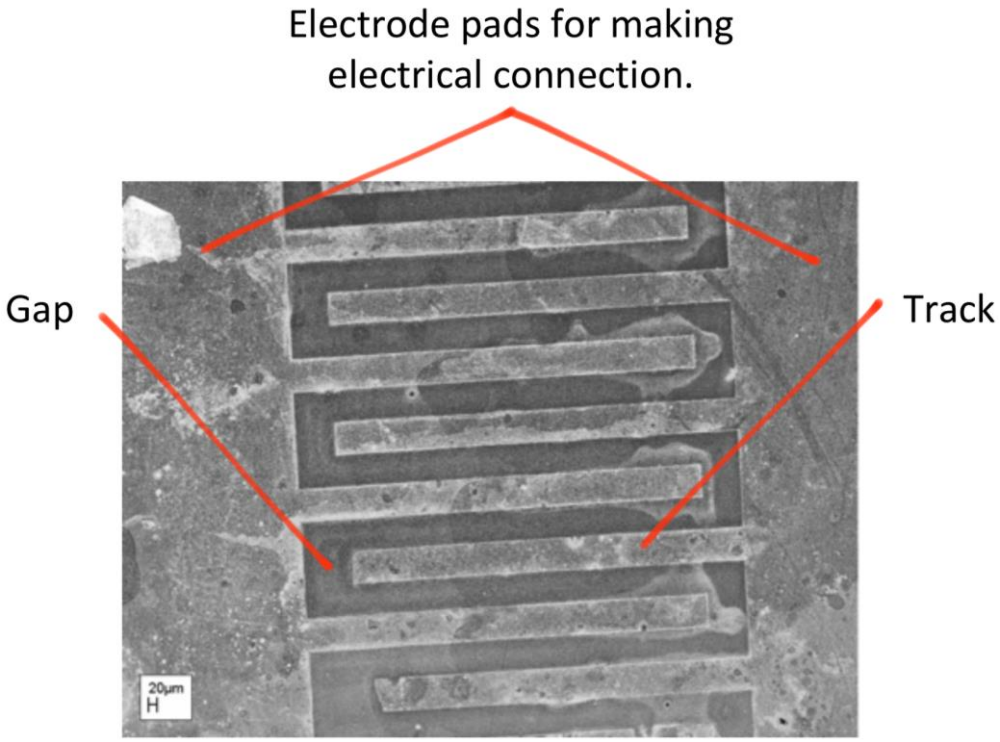

Fig. 5.1 Scanning electron micrograph (SEM) of 75 µm track and gap structure with clearly defined regions.

It can be seen from Fig. 5.1 clearly defined regions of gold left after the substrate had been etched. A sharp contrast between tracks and spacings indicate a successful print. One observation was that there appeared to be clouding around electrodes, particularly at the tips of the electrodes. A closer inspection in Fig. 5.2 shows this effect occurring around two electrodes.

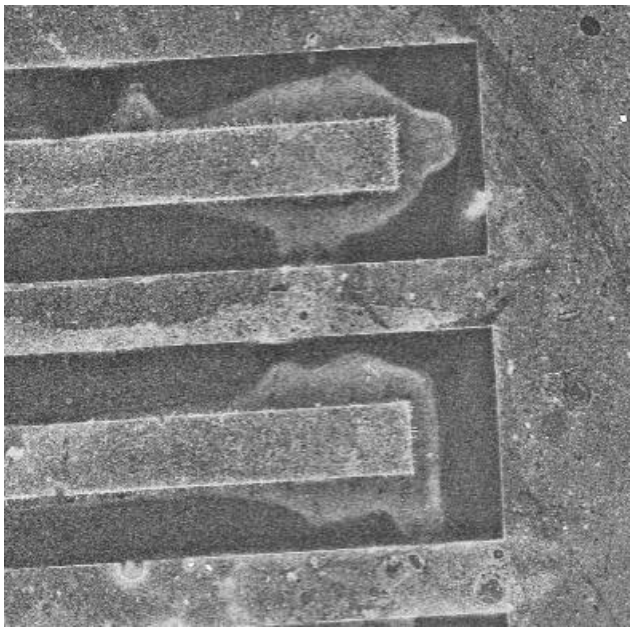

Fig. 5.2 Enlarged clouding region of 75 µm track and gap device.

It was unclear what caused this additional deposit. The most likely cause of this was the nature of the wet chemical etch. The etch being anisotropic means that etching occurs in all directions and therefore any variation to the etch process could have produced the clouding effect.

In certain circumstances this clouding effect around the electrodes enlarged the conductive regions and reduced the spacing. Where the spacings were reduced, frequently bridging between tracks occurred which led to shorting. Destruction of the print happened in two locations repeatedly, either around the epoxy resin or between the interdigitated electrodes. A surge in charge can ionise the particles in the spacings this frequently caused a spark at either boundary and destroyed contact. When this occurred around the conductive epoxy, it was difficult to reapply the epoxy around the existing contact and on occasion when this was accomplished the build

up of charge was still a problem and then went on and shorted the capacitive structure.

Conclusion

Incremental improvements were made throughout this set of print results. The testing of structures indicates significant progress, beyond print techniques and device architecture to electrical functionality. As the processes and techniques continued to be honed it was imperative to try and move towards manufacturing conductive devices.

5.2.2 Functional 75 µm track and gap device emitting light

The electrode array at a track and gap of 75 µm with an electrode length of 1 mm consistently produced the best results from manufacture of the stamps through to reliable prints. Work continued to improve the print quality of the 75 µm track and gap structure before transferring to stamp trials with reduced feature sizes.

Method

The print method established in section 4.3 was used, and work maintained its focus on producing 75 µm track and gap structures, printed for use in an electrode array. The instruments described in section 5.1 were configured for use with the device. Since the initial tentative conductivity of prints the yield of successful prints increased and began to produce some promising results.

For structures that proved conductive, phosphor ink was deposited over the surface at a thickness of between 50 - 100 µm, measured using a micrometer. Fig. 5.3 showed the 75 µm track and gap structure emitting light at different frequencies along certain track spacings, evidence that the electrodes adjacent to one another were conductive. From the images it was possible to notice that the light emitted was not even across the entire electrode array, this was caused by breakdown along some of the tracks, leading to the electric field falling below the threshold strength for stimulating the phosphor particulates held in the resin bound ink. A TOP 200 was used to characterise the structures. Typically to measure the luminance of structures is preferable to have an area that emits light of at least 5 mm^2 evenly across the

array. Focussing the probe is difficult below these areas, a resolution of approximately 1 mm^2 means any dark fringes will impinge the final measurements. Because the conductivity of the tracks was not consistent, this wasn't possible from this structure. The light output was, however, still measured at 3 different frequencies: 400 Hz, 1 KHz and 2 KHz, the voltage was varied and a relationship plotted in Fig. 5.4. These frequencies were chosen as they represent a broad range of existing performances. At the lower end of the range of frequencies was 400 Hz, and whilst 2 KHz is not the maximum frequency to test for, at higher frequencies degradation of the phosphor particulates happens faster and therefore lowers the lifespan of the display. It was also considered during measurement that the area at which the structure did emit light was estimated to be function at approximately 30% of the potential luminance output

A) B)

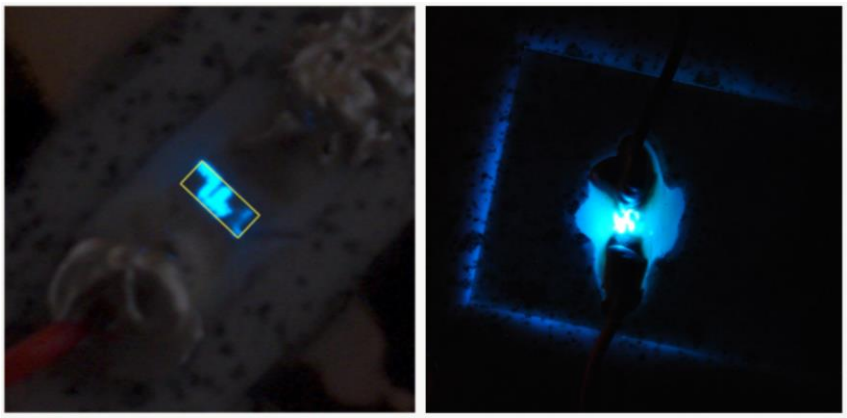

Fig. 5.3 Illuminated structure of 75 µm track and gap structure. An area of 1 mm by 5 mm (defined by the yellow box in A), with varying frequency at A) 400 Hz, and B) 2 kHz with a ZnS phosphor ink.

Characterising this structure, and measuring data collected from the emitting device is detailed below in Fig. 5.4

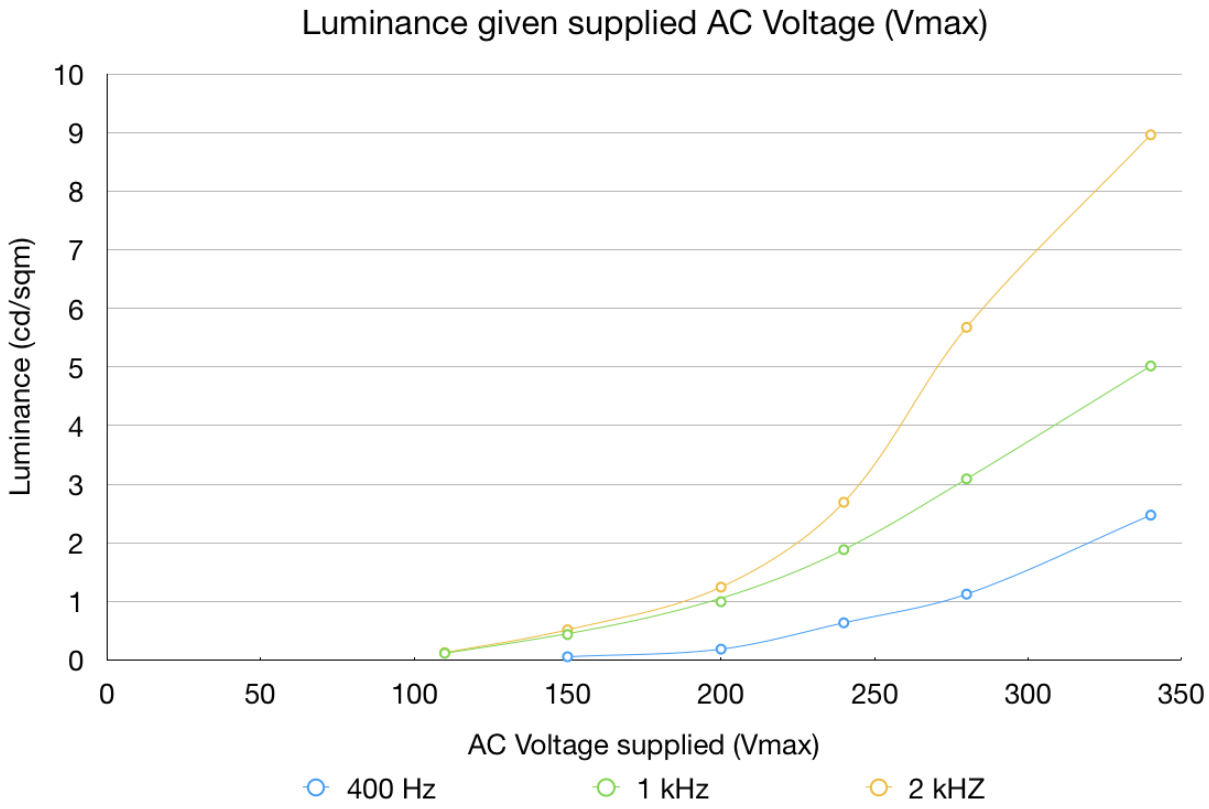

Fig. 5.4 Luminance results of the 75 µm track and gap structure [76]. The graph demonstrates an initial luminance for a supply of 1 kHz and 2kHz at 110 V, but for 400 Hz at 150 V.

In Fig. 5.4 it was noticeable that for the field strength to begin emitting light from the phosphor a threshold voltage of 110 V_{max} was required. This was significant as commercially available electroluminescent devices operate at a voltage of around 130 V_{rms}. Therefore demonstrating that the stimulating voltage for the microcontact printed electroluminescent display was not too distant from current industry performance. For comparison, Display Innovations supply EL displays, that operate at 220 V_{rms}, and 3 kHz, producing a luminance of 200 cd/m^2. Given the relative areas although Fig. 5.4 represents a poorer performance, there are far less inefficiencies and a longer lifespan as a result.

From Fig. 5.4 it was also observed that frequency impacts the final luminance, as the frequency is increased the luminance also increased. It was also noted that at 1 kHz and 2 kHz, the voltage value for which initial luminance occurred was the same, this

implies a typical threshold for luminance at approximately 110 V_{max}. This provided a helpful insight for the device as it allowed calculations to begin determining where the losses occurred. Theoretically it was also determined the theoretical luminance threshold voltage in section 6.2.5. The light output measured was 0.075 cd/m^2 which may seem poor by comparison, except limitations of the device must be considered. The 75 µm device operates at only 30% capacity, the TOP 200 will collect all light produced over a given area and this will include dark regions both across the structure and around the perimeter. In order to produce more substantial results a structure that emits light across the entire area is required. Some mobile phone technologies use displays that operate at approximately 11 cd/m^2 demonstrating the usability of the light produced. Ideally the light produced would be operated by as low a frequency as possible. Fig. 5.4 shows that at a frequency of 400 Hz the devices produce a luminance of about a 1/4 that of 2 kHz. The results show that even at 400 Hz the threshold voltage was currently at 150 V_{max}.

Conclusion

Providing a light emitting device was significant progress to the work, with the proof that microcontact printing could be used in the manufacture of novel electronics. Work was conducted to improve the reliability of electrode conductivity. The percentage of working structures compared to the number of prints undertaken was very small and work tried to increase the yield of working structures to demonstrate the suitability of the process for printing electroluminescent displays.

It has been possible to identify the threshold voltages for a structure of 75 µm track and gap. Also demonstrated was the reliability of the stamp manufacture and reproduction of the stamp features in the thiol deposit on the gold substrate. From the graph in Fig. 5.4 it can be determined that the operating voltages for producing useful light have fallen in line with expected values. Furthermore, given the partial lighting of the structure once the printing techniques have been perfected it should be possible to measure 100% of the light output. Despite this structure being successful it was still only operating at about 30% of the potential light output. Whilst print techniques and quality improve, attention must be turned to reducing the track and gap spacing down from 75 µm.

5.2.3 Reducing the track and gap spacing

The developed print process was employed for this set of prints. The next step in progression was to print devices at 25 µm track and gap spacings. This would decrease the driving voltage and it was hoped that the device could run at 400 Hz.

Method

Stamps, with the interdigitated pattern were produced, the varying sizes of track and gap spacing manufactured were: 10 µm, 15 µm, 25 µm, 50 µm, 75 µm and 100 µm. The electrode array structures were produced at varying electrode lengths of 1 mm, 3 mm, 5 mm with contact pads at either end of the electrodes with length 5 mm and width dependent on the number of electrodes present in the structure. Occasionally at the smaller track and gap spacings the stamp's patterned electrodes would shear and frequently elastomeric tracks would tangle with the other track features and directly interfere with the print quality. Without the use of mould release agents this appeared to be a consistent problem. The silicon wafers can be cleaned with sulphuric acid to dissolve any PDMS deposit on the surface and used again. The simple peel process continued to produce torn stamp surfaces and limited success. Stamps were produced with relative degrees of success with feature sizes: 15 µm, 25 µm, 50 µm and 75 µm. The use of mould release agents was avoided due to the fact that they alter the surface chemistry by bonding to expose alternative functional groups. Usually the print surfaces then require reactive ion etching to remove the top few microns of the contaminated stamps. Without access to this equipment any contamination would alter the surface chemistry of the stamps and prevent inking of the stamps with the thiol.

The range of stamps produced were then used in this set of prints, selection had to be made due to the tearing and stress forces involved with manufacturing the stamps. The stamps were subjected to the aforementioned printing process, given the track record of the process and the constant improving of the quality of the prints, it was settled to continue using the same method.

Results and observations

Conductivity proved to be an issue, below is displayed a structure with feature sizes of 15 µm track and gap, this was successfully manufactured; it shows the potential possibilities with this process. The track and gap can be produced much finer and

research has even been developed on the nanoscale [43]. The limiting factor for our application was the use of phosphor particulates for EL devices, limited to around 7 µm.

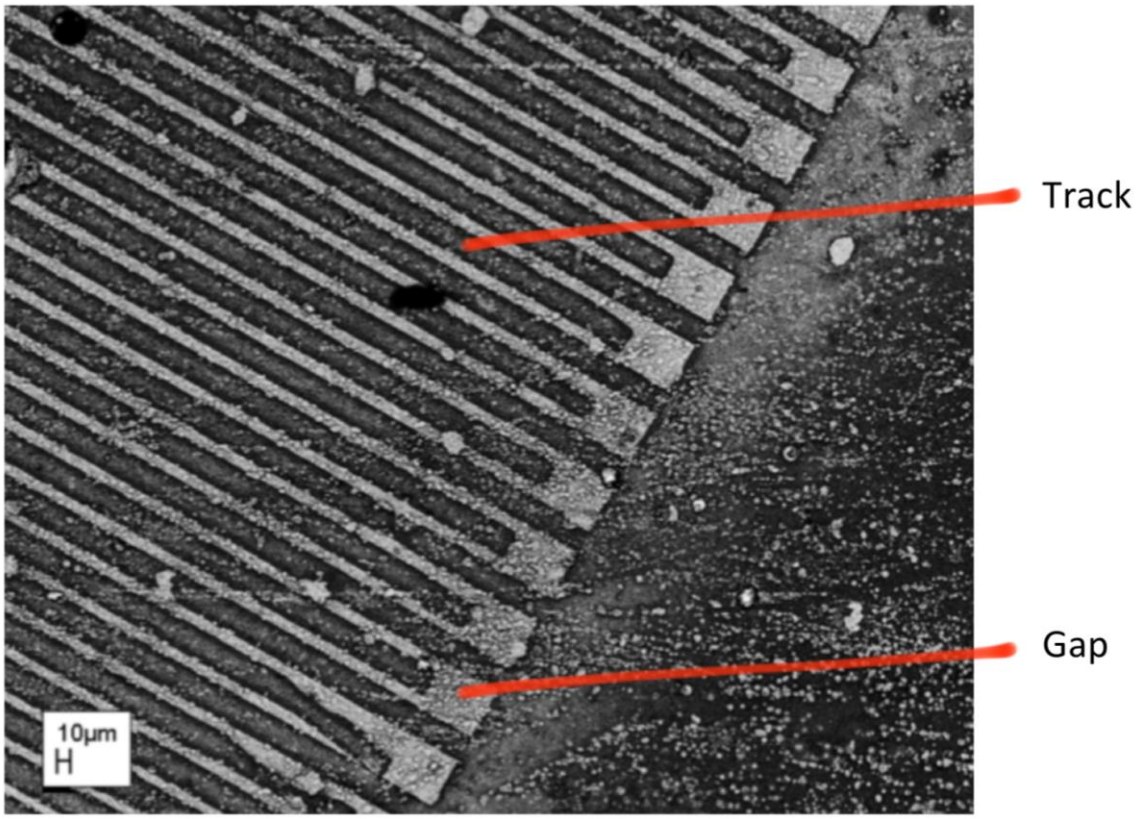

Fig. 5.5 Potential for 15 µm track and gap features.

Unfortunately these structures did not conduct electricity due to some stray tracks from the stamp that tore during peeling from the mound. The length of the electrodes increases the room for error, here an interdigitated electrode structure array with 6 mm long electrodes was used. With a track and gap of 15 µm even a tiny fracture at any point on the surface would destroy conductivity. Another reason for a lack of conductivity was that of pinholes in the resist layer partially etching the tracks, we know this to have been an issue previously and interferes with performance due track degradation.

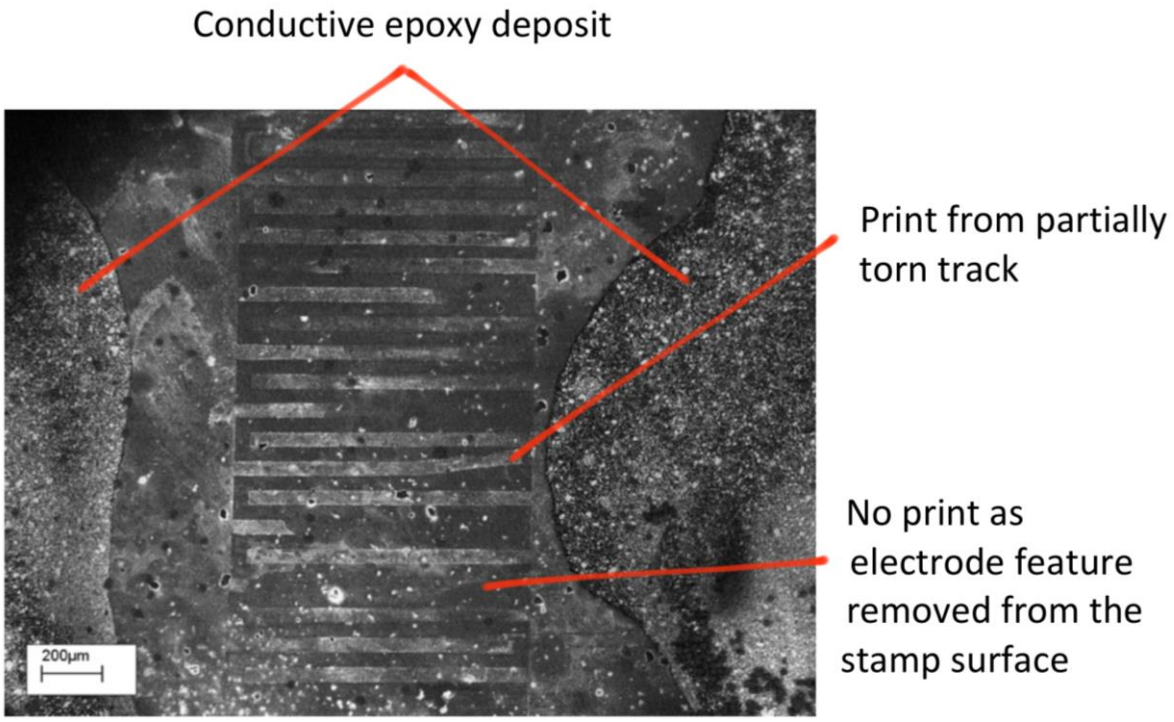

Fig. 5.6 50 µm track and gap structure with poor conductivity. Cured by over exposure to the etch solution and track tearing.

Conclusion

From Fig. 5.5 and Fig. 5.6 it was possible to see the capabilities of the process, improvement to the scale of the structures being produced was impressive. Smaller track and gap features were being manufactured, and each time taking a step closer to the goal of producing a functional EL device with lower driving voltages. Printing continued in this vein to print a conductive track and gap structure at a smaller scale.

5.2.4 Conductive 25 µm device with low driving voltage

Using stamps of 25 µm features it was investigated whether conductive tracks could be produced at the desired scale to stimulate phosphor particles at lower driving voltages. The 25 µm structures were selected as they were producing the most consistent results for clear prints with clean definition and minimal impurities. These features were 3 mm long and therefore much more delicate than the previously successful stamps.

Method

With regard to the print method, the process developed in section 4.3 was again employed during this set of prints. Characterisation of the device to identify the luminance also required the use of a TOP 200 and other apparatus from section 5.1. This time only 2 frequencies were measured 400 Hz and 2 KHz, this was due to lower luminance emissions. Fig. 5.8 plots these results and compares them with the previous set of luminance results.

Results and observations

This set of prints led to a successful print with a stamp of 25 µm track and gap spacing, although by comparison with the 75 µm track and gap spacing structure the light appeared to be much dimmer, most likely caused by the more fragile electrode array. It also showed that fewer tracks were conductive along their length, previously adjacent tracks would have led to a superimposing of the field and would boost the strength and cause the phosphor to emit more light. It is also noticed that the tracks are 3 mm long, and 25 µm wide. This leads to a much higher resistance along the tracks by nearly an order of magnitude, even with this would disrupt conductivity which given the film thickness was already very delicate.

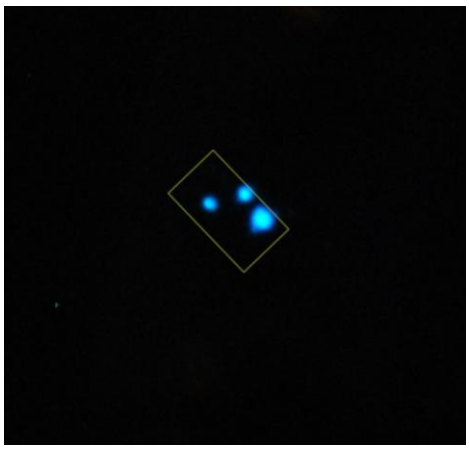

Fig. 5.7 25 µm track and gap structure illuminated.

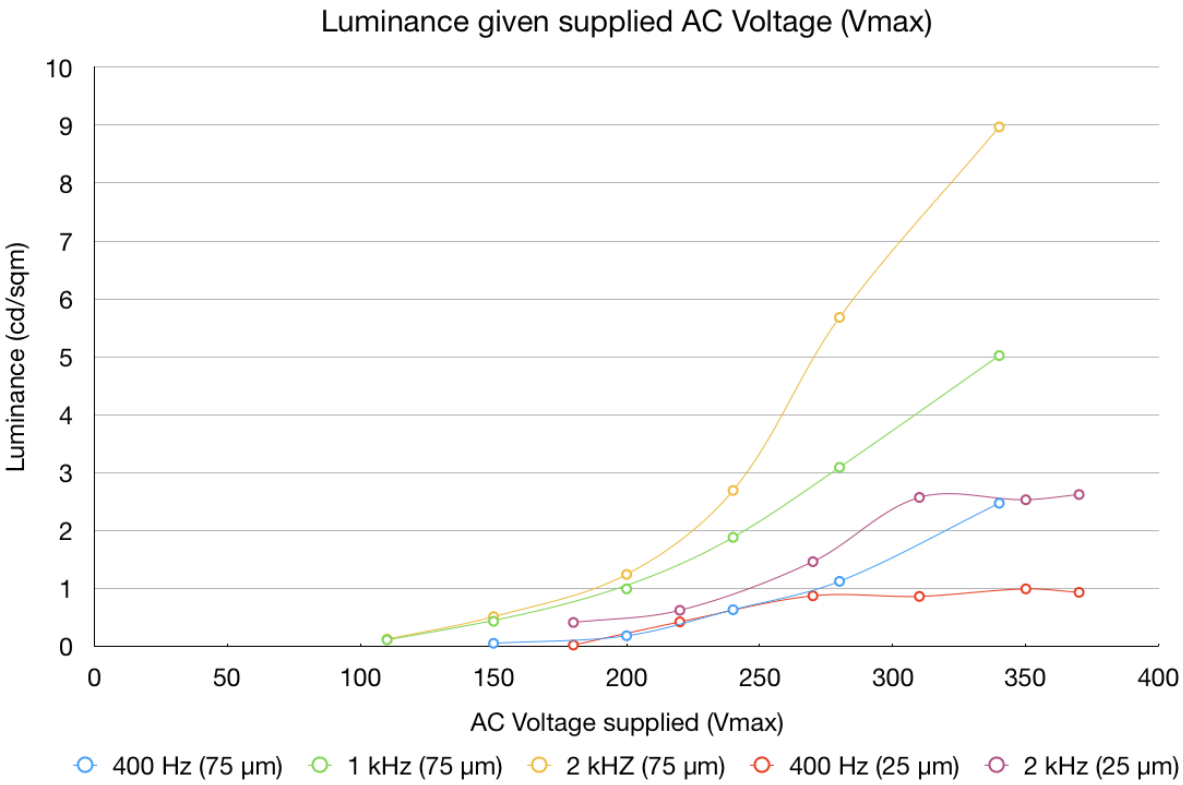

Fig. 5.8 Luminance results of a 75 µm and 25 µm track and gap spacing device superimposed for comparison. The lowest driving voltage was 110 V for the 75 µm structure, and 180 V for the 25 µm structure.

Conclusions

Printing a structure of 25 µm track and gap spacing was successful when used to fabricate an EL device, however due to physical constraints resulting in an increased resistance the structure by did not produce light uniformly across its surface. This lack of light output means that when measured using the interferometer the luminance generated could not be accurately recorded. Voltage measurements showed that the stimulating voltage for this structure actually dropped to about 65 V_{max}. Standard phosphor materials suggest that light is not emitted below 100 V_{rms} however this structure has proven the benefit of using microcontact printing as a method for printing functional EL devices to reduce the required driving voltages.

5.3 Experimentation summary

It can be identified that interdigitated electrode arrays can be used as viable high electric field generators in EL applications. It was also noted that although devices appeared to show a threshold voltage, explored more in Chapter 6, the voltages are comparable to other EL configurations. The threshold voltage exists due to emission of non visible electromagnetic waves. The devices are on but this emission is undetectable. Understanding the power delivered to the device and therefore how much of that is undetected would help better understand the losses and performance of the EL devices.

Given the low, albeit, increased yield of devices produced for electroluminescence, a complete electrical characterisation of the electrode arrays would be premature. Without improved print yields and full illumination of the devices, theoretical modelling provides the best analysis for the structures and performance against which manufactured electrode arrays seek to perform. The work focussed on the capacitive properties of the devices, however impedance calculations would be the next step towards building a complete model for EL devices.

Whilst the print trials were many and varied the above documents incremental successes. This success proved that microcontact printing can be used for the fabrication of high electric field generators with applications in electroluminescent displays and other devices. Alternative applications were not explored in this thesis, but interest has already been shown in various sensor applications.

There were many more print trials that were undertaken and many of these encountered difficulty, mostly these were rectified through the work in this thesis. The print process as established in section 4.3 improved the quantity of functional devices being fabricated and gave greater reliability to the outcome of each print trial.

Chapter 6
Summary of results

6.1 Results for print components

6.1.1 Stamps

The stamps were manufactured to varying sizes using moulding techniques over a silicon wafer, the structures ranged from 100 µm to 10 µm with the smaller sizes becoming increasingly susceptible to shearing stresses upon release from the moulds. Fig. 6.1 below demonstrates both the high quality stamp surface and the problem that occurred due to tearing of the features:

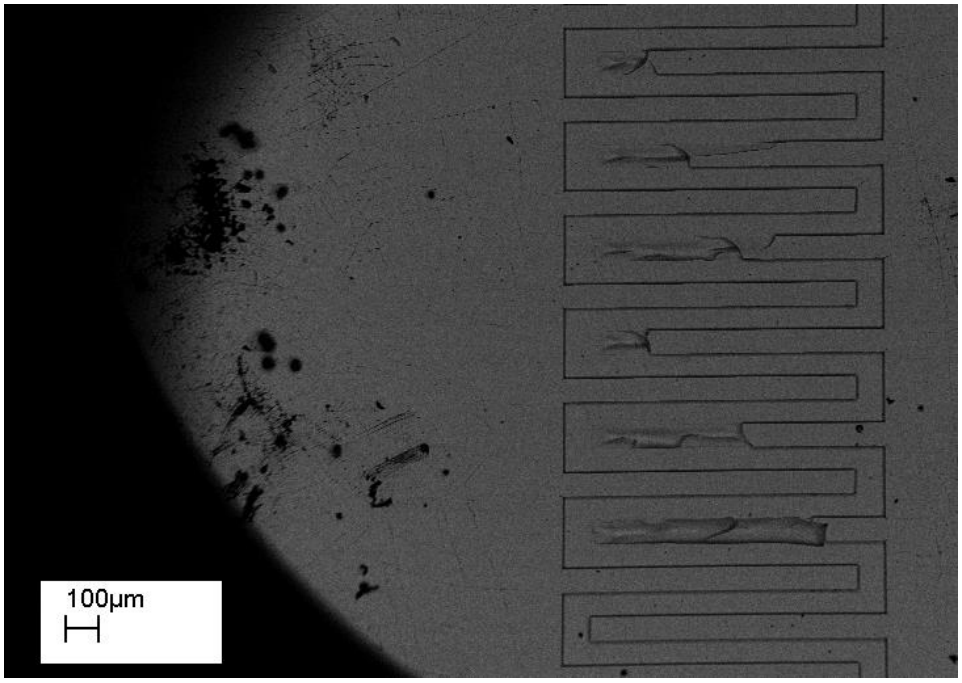

Fig. 6.1 Effects of stress on the PDMS stamp causing tearing.

From Fig. 6.1, it is possible to see tracks left to right very clearly defined stamp features with sharp edges and good resolution. When compared to tracks from right to left, there were torn tracks as the stamp was removed from the mould, placing large shear forces on the elastomeric stamps. A solution to the shear force interference would be to employ mould release agents to prime the surface of the silicon wafer for ease of release. Release agents for the PDMS used are

polysiloxane based and therefore would interfere with the surface chemistry of the stamps and interrupt the bonding required between the alkanethiol ink and stamps. The polysiloxane mould release agents act to spread across the surface providing a thin film over the surface to prevent bonding between the PDMS stamp and the silicon wafer master. This in turn leaves a polysiloxane based deposit over the surface of the stamp altering the chemical surface. With only known solution for clearing the residue problem was to use a reactive ion etch to remove any surface impurities and reveal the desired chemistry of the PDMS stamp. Given the rectangular profile of the stamps this is achievable providing the alignment is correct as a reactive ion etch occurs as an anisotropic etch in a single linear direction. This however is expensive and time consuming.

A range of stamps have been manufactured utilising an optimised curing temperature of 60 ˚c. Whilst some of these stamps still exhibit shearing across their profile the yield of usable stamps improved through the research.

6.1.2 Gold Substrates

Work was carried out to determine the optimal thickness of gold to be deposited for use as the printable substrate. This was performed with a view to measuring the resistance across the film and how that would relate to the structure after etching had occurred. It was discovered that etching occurred across the whole slide in masked and unmasked regions alike. However it was thought that perhaps the increase in film thickness would increase the gradient across the slide to create greater extremes between gold tracks and the spacings between. If the ratio of etch rates between the SAM protected gold and the unprotected gold was different, which previous research suggests, then it was assumed that a thicker layer of gold would only exaggerate the effect.

The etch process undermined the SAM layer through the exploitation of pinholes in the surface of the SAM and in so doing undermined the chemical bond of the thiol SAM to the gold substrate. To minimise the effect this had on the gold tracks exposure time was critical to the process in conjunction with the etch concentration. Firstly the gold substrate thickness was identified, before examining the role of

various thiols on the surface followed by its use in conjunction with the desired etch solution.

To begin, the resistance of the gold slides was measured at varying thicknesses and the graph below shows the results, from this the sheet resistance of the gold layers were calculated to find an optimal thickness for the gold layer before analysis with the etching process.

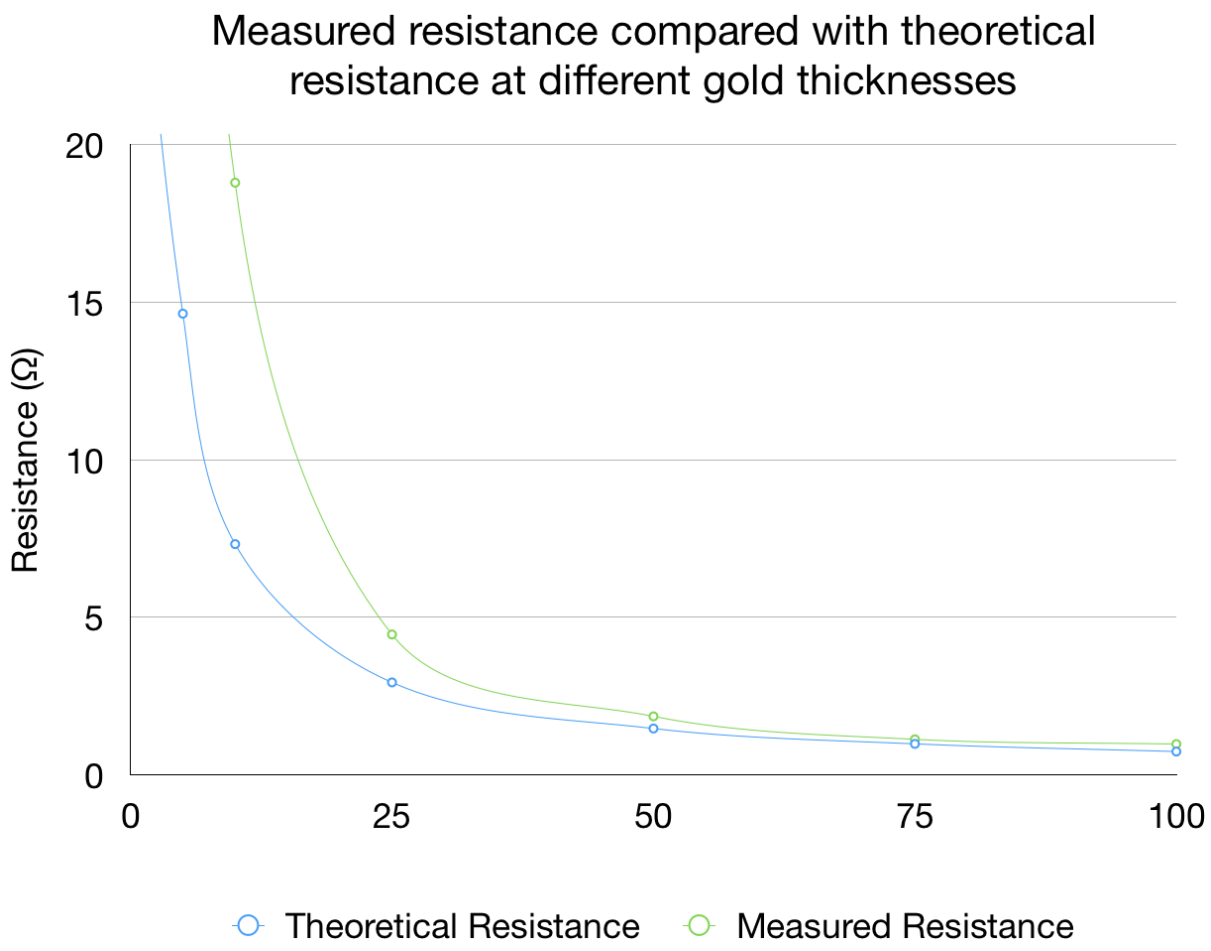

Fig. 6.2 Resistance of gold thin films compared with theory. The graph demonstrates that performance of gold films mounted on glass substrates have similar performance to theoretical values below 50 nm.

Fig. 6.2 shows that conductance increased with gold film thickness suggesting it is significantly better to begin by laying down a thicker layer of gold. Comparative resistance calculations suggest that at film thicknesses of 50 nm the samples are

fairly closely aligned with theoretical calculations for thin films. The model was based on the established formula for Resistance as detailed below:

$R = (\rho L)/A$ (Eq. 10)

Where: R is the resistance calculated, *p* is the resistivity of gold (2.44×10^{-8} Ωm), L is the length of the sample and A is the cross-sectional area of the thin film.

In conjunction with the etch solution and Thiol conclusions it was identified that 50 nm provided the best thickness for experimentation as it limited the possibility of under etching and damage to the conductive tracks. See 6.1.4 for further details of performance when used in conjunction with the etch solution.

6.1.3 Thiol

Alkane-thiol materials are compound molecules with a sulphurhydryl (SH) terminating group at one end and a carboxyl group (COOH) at the other. The COOH group is used to bond to the stamp, whilst the SH group is used to bond to the gold substrates. This allows for thiol pick up and put down according to the bond strength between surfaces.

Work was undertaken to compare the MBA, HDT and MUA molecules for use as a resist layer during the etch process. All three thiols are used to form functionalising layers over the surface of a variety of substrates depending on chemistry and desired effects for end use.

The density of MBA provides structural support for carrying additional molecules bonded to the free COOH group, once bonded to the gold. HDT has two SH terminating groups at either end of the molecule. This allows for both ends to be attached to the substrate exposing the carbon chain along the length of the molecule, this creates an intensely hydrophobic region, demonstrated by water balling on the surface. MUA is a linear molecule, with COOH and SH groups at opposing ends. This structure makes it ideal for use as a comprehensive

functionalising layer, the process of hybridisation is easier to carry out, free from carbon chains that would hinder compatibility along the length of the molecule.

During investigation with MUA, MBA and HDT, it was established that MUA and MBA both performed with similar performance to be used as resist layers and therefore the decision was made to continue with the use of MUA due to its prior recommendation and chemical structure. It was noted that MBA has a higher density due to a carbon ring although this didn't improve comparative performance. It was also considered that a more complex molecule may take longer to undergo hybridisation and therefore may be less reliable in practice. MUA is a linear molecule and formed a uniform layer under the process of hybridisation.

6.1.4 Etch process

For use with gold substrates, there were two common etch solutions identified as being in widespread use, aqua regia and a potassium Iodide etch. Aqua regia is a hydrochloric acid based etch and particularly aggressive, not just for the gold substrates, for this reason potassium iodide provided a more suitable alternative.

There were complicated effects to be discussed, such as to determine the nature of the etching process. Does the etch resist layer prevent or hinder the etching solution? If the etching process was prevented by the SAM resist layer then the thickness of the gold film would be less critical because the etch is chemical and therefore isotropic. The process occurs both vertically and horizontally, so the desired gold tracks would in turn be etched, but only once the unprotected gold films have been removed causing under etching of the resistive SAM layer. Given that the etch rate of the etching solution is approximately 1 µm/min and the tracks are at least 10 µm wide, there is significant difference at etching horizontally across the slide to be able to determine the optimum etch time with enough tolerance not to affect the results of the printed gold tracks.

For this reason, it was preferred to use 50 nm layers of gold across the substrate surface. This in turn meant the dimensions of any under etching would be limited to the rate at which the 50 nm etches. Use of a 30% etch solution reduced the etch rate

to allow greater control over the process. This led to a more distinguishable point at which etching of the good film had completed.

If, however, the etch resist layer only hindered the etch process and the gold tracks still underwent etching then exposure time to the etching solution was critical to the results. There were two main solutions to why the SAM resist layer would only hinder and not prevent the etch: either the thiol used to form the SAM chemically reacted with the etch solution or there were pinholes that exist in the resist layer where the etching solution still made contact with the gold allowing etching to occur, or both these circumstances existed simultaneously. It was more probable that the etch resist layer only hindered and did not prevent the etching process leading to a critical thickness of gold to be deposited. This was due to the fact that if there was pinholes in the SAM resist layer. Exposure of a thicker gold film layer would exaggerate this effect and under etching would still occur again, only this time across the surface of our gold tracks instead of at the edge boundaries.

There was a significant trade off observed between depositing enough gold to conduct and act as a charge carrier for the interdigitated electrode structures, coupled with a thin enough layer for the etching process to distinguish a satisfactory etch gradient across the surface to fabricate prominent gold features. It was imperative to look at the characteristics of the varying thicknesses of gold film to be used in experimentation and the relative conductance and sheet resistive properties of the films, as discussed in section 6.1.2.

The etch solution was composed of a ratio of 4g (PI):1g (I_2):40ml (H_2O) this provided a sufficient etch with an approximate etch rate of 1 µm/min, or 16 nm/s. With the thickness of the gold substrate layer determined at 50 nm this meant an etch time of approximately 3-4 seconds. In order to control the etch process, dilution provided a manageable and reasonable way to monitor the progress of the etch and identify the optimal point of etching. Within the parameters an etch concentration of 30% led to a sufficient etch gradient across the profile of the substrates.

A 30% etch solution gave control over the rate, extending the etch time from 3-4 s to 21 s, demonstrating a non-linear relationship, which is usual for dilution processes.

Due to the additional time used to etch the unprotected gold substrates it gave greater precision of the process and therefore made it easier to carry out.

6.2 Results for characterising printed functional devices

Given the success of the previous printing processes using the microcontact printing kit, techniques to incorporate comparable substrates, stamps and thus conductive structures were developed. Given the success of preliminary stamping, some basic sample analysis was performed to establish the quality being produced.

It began with surface characterization of the gold lines being produced using a confocal scanning optical microscope; this generated images and values for the dimensions of lines being produced shown in Fig. 6.3 and 6.4.

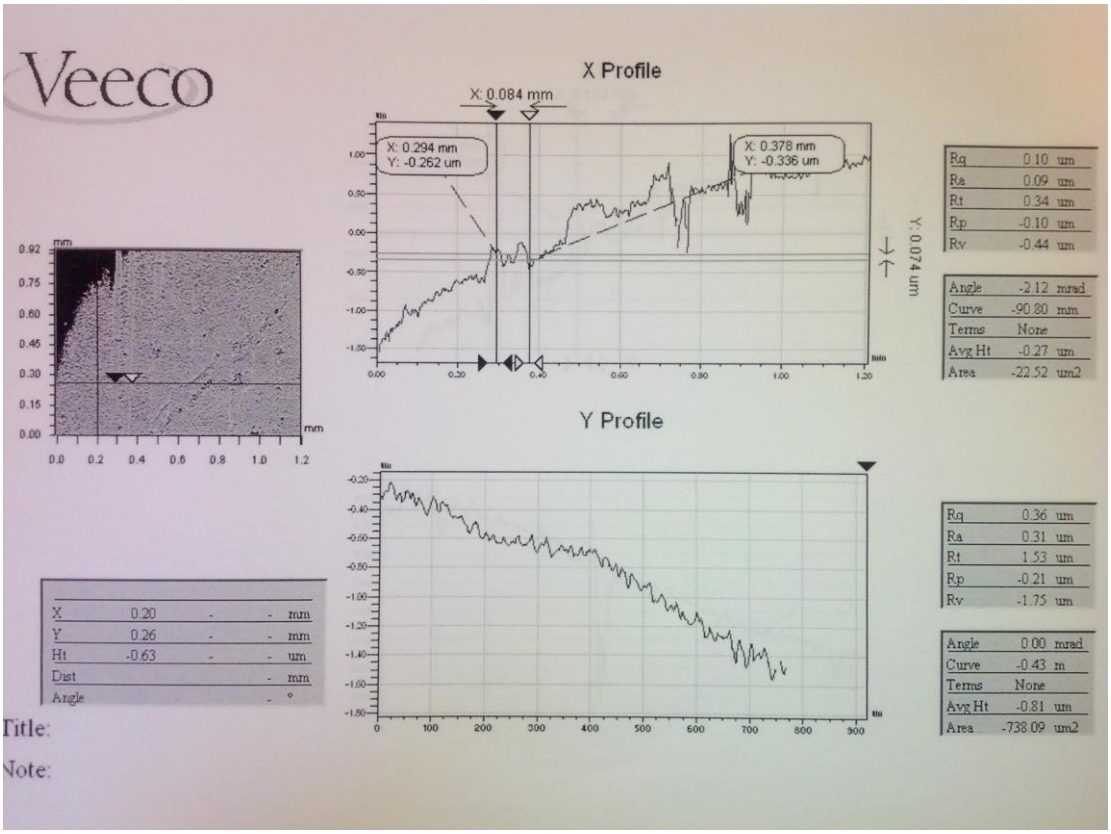

Fig. 6.3 Confocal microscopy illustrating a line height of 74 nm.

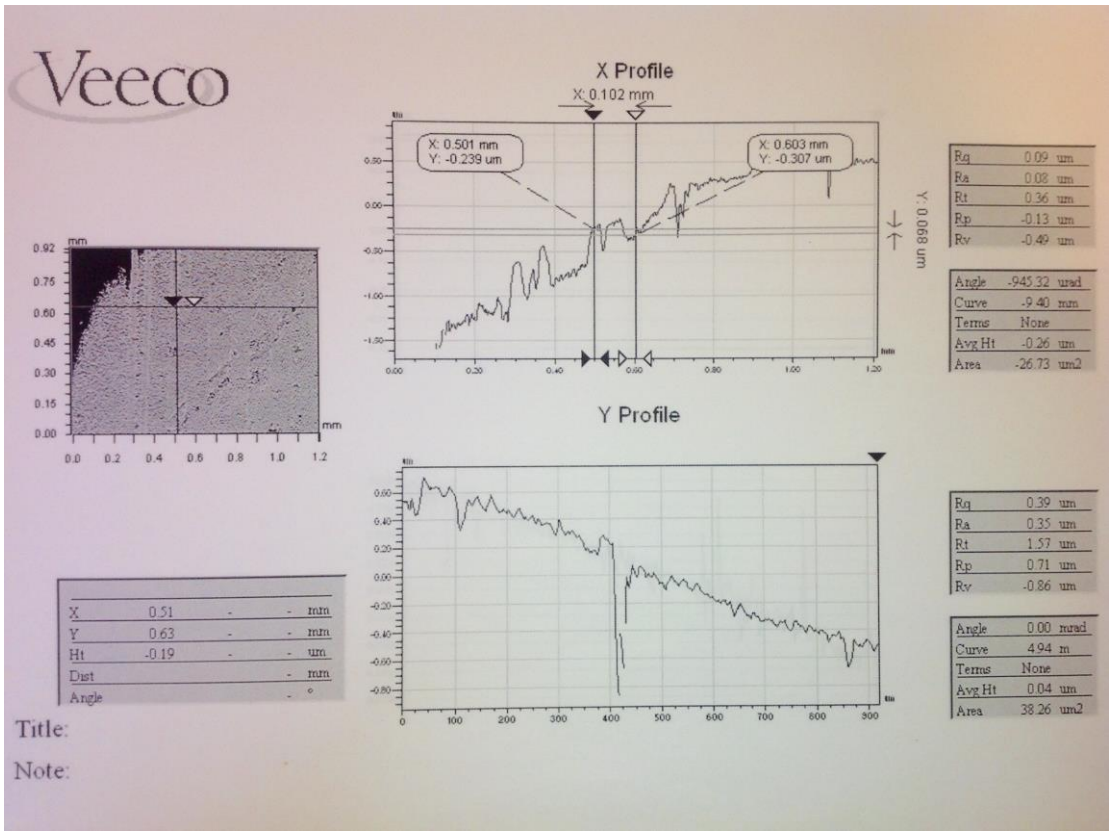

Fig. 6.4 Confocal microscopy illustrating a line height of 68 nm.

In summary the initial width of the gold lines are an average of 105 µm demonstrating a minor track growth, and there is also an average height value of 71 nm where the original value of the substrate layer thickness was 50 nm gold. The further 20 nm was due to the introduction of a titanium adhesion layer. The layer was employed by Platypus technologies to aid transportation of the gold substrates. Once substrates were developed independently of the platypus kit, this layer was removed. The layer provided not only adhesion but also a mounting layer adding structural support to the gold film. A layer of between 20 and 30 nanometres is a reasonable tolerance for the adhesion layer.

Although good results were produced with the substrates there were problems encountered with the conductivity of the gold tracks, upon closer examination with Scanning Electron Microscopy (SEM) it was found there was no continuous gold contact for conductivity along the length of the track.

From these initial findings, work began to establish a reliable and repeatable process for printing high electric field generators, as discussed previously in this thesis. This work culminated in printing a range of high electric field generators for use in electroluminescent displays. Fig. 5.8 is the graph characterising the luminance output of various structures.

Certain factors must be considered, namely: supply voltage, frequency and geometry. Apparent from the graph above this combination of variables affect the luminance based on the track size, the voltage supplied and the frequency at which the inverter is set. The track size is determined by the stamp fabrication and print performance, prints at 75 µm and 25 µm have been successful as represented by the above graph. It is apparent that track and gap spacing provided an inverse relationship whilst the voltage and frequency provided a positive correlation.

Electric field as defined by $E_f = (kQ)/r^2$ (Eq. 13) demonstrates an inverse square relationship with the distance between adjacent electrodes. The constant, k, is determined in this case as coulombs constant and defined by the equation $k = 1/(4\pi\varepsilon_0)$ (Eq. 14), where the parameter of epsilon zero (ε_0) is the permittivity of free space. In this instance a resin based ink is used as a dielectric carrier for the phosphor particulates. This changes the permittivity of the material and therefore the constant used. The relationship still demonstrates an inverse square relationship even when using a different relative permittivity (ε_r). The relative permittivity for the ZnS phosphor particulates is 8.9.

6.2.1 Energy dissipated from structures

The voltage supplied shows a positive correlation with the high electric field generated. $E_f = V/d$ (Eq. 1) governs this relationship, where d is the spacing between adjacent electrodes, E_f is the field and V is the Voltage. We can therefore see that an increase in voltage increases the field strength and therefore increases the luminosity of the phosphor particles.

By increasing the frequency, it is also possible to increase the luminosity of the structures as evidenced by the graph above. Due to the atomic structure of the particulates we find that applying a current to them excites the atoms causing an unbalanced state to occur. When the atom returns to a stable state energy is released as light, this is a momentary effect and why an alternating current is required. As the frequency of an alternating current driving the device increases this happens at a faster rate causing more excitation and greater intensity of light emitted. It is largely thought that the optimum operating frequency for phosphor particulates is around 400 Hz, but they can be driven by frequencies up to 3 kHz [49]. At 3 kHz, inefficiencies dictate that the particulates breakdown fairly rapidly lowering lifespan. For commercial applications, frequency is often increased in the short term to boost their performance.

A range of structures were manufactured to varying degrees of success. Light was produced using structures at 75 µm and 25 µm. The 75 µm structures appeared to produce the stronger output however this is due to the physical dimensions of the structure. However using the 25 µm structure it was observed, not quantified in the results, that an operating voltage of 65 V would light the structure, represented in Fig. 6.5. This demonstrates that although 25 µm produced a lower performing structure it does have a greater capacity of operating at lower voltages.

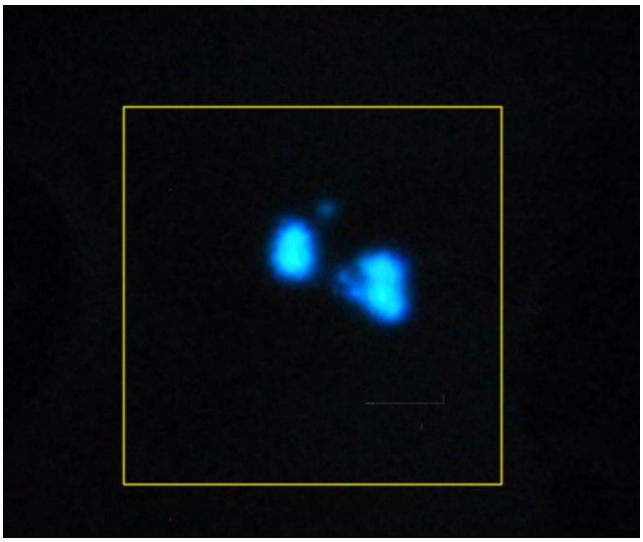

Fig. 6.5 A structure of 25 µm track and gap stimulated with a driving voltage of 65 V. The total device area of 3 mm x 3 mm is bound by the yellow box.

6.2.2 Determining instantaneous power (P_i) of the devices

As the results suggest from observing light emitted, it is important to interpret the results and mathematically confirm the observations. When characterising an AC (alternating current) supply to the structure, standard DC (direct current) equations are insufficient. The principles are maintained but due to the reversing of directions, typically a sinusoidal wave signal is generated. The phase diagram for a purely capacitive load stipulates that current leads voltage and is given in Fig. 6.6 [77]

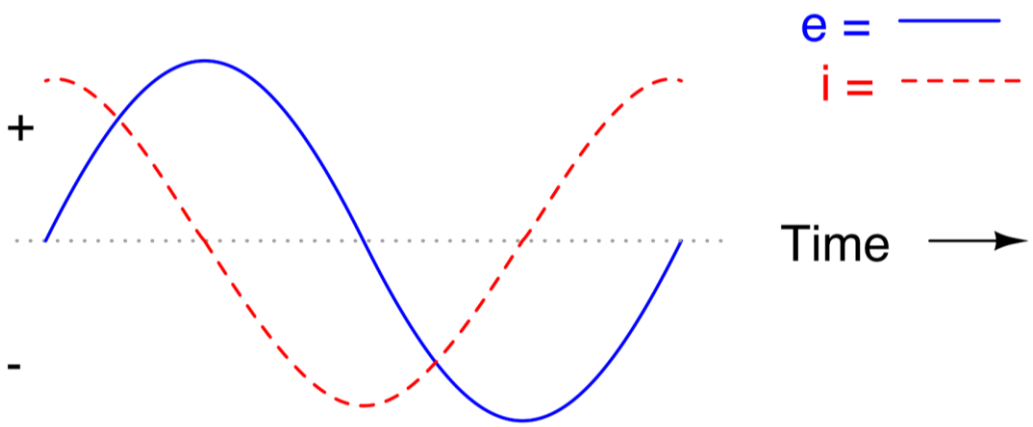

Fig. 6.6 Phase diagram for a purely capacitive load, e = emf (electromotive force), i = current [76].

Power supplied can be derived from the frequency, current and voltage supplied. Using the standard equation for instantaneous power given as (Eq. 15):

$$P_i = (V_{max}I_{max}/2)\text{Cos}(\theta_v - \theta_i) + (V_{max}I_{max}/2)\text{Cos}(\theta_v - \theta_i)\text{Cos}2\omega t - (V_{max}I_{max}/2)\text{Sin}(\theta_v - \theta_i)\text{Sin}2\omega t \qquad \text{(Eq. 15)}$$

By modelling the structure, albeit imperfectly, as purely a capacitive load, we know that current 'leads' voltage by 90˚, and can therefore derive (Eq. 16):

$$\theta_i = \theta_v + 90^\circ, \text{ so } \theta_v - \theta_i = -90^\circ \qquad \text{(Eq. 16)}$$

Substitution of (Eq. 16) into (Eq. 15) reduces the equation for instantaneous power of a purely capacitive load to (Eq.17), recognising that cos(-90˚) = 0, sin(-90˚) = -1, and ω = angular frequency:

$P_i = (V_{max}I_{max}/2)Sin2\omega t$ (Eq. 17)

This equation provided instantaneous power as a function of time. In order to calculate the current (I_{max}) drawn by the capacitive structure using an AC supply, the capacitive reactance (X_c) can be calculated using (Eq. 18), before substituting this into a rearranged Ohms law (Eq. 19), as a replacement for the resistance.

$X_c = 1/(2\pi fC)$ (Eq. 18)

$I_{max} = V_{max}/X_c$ (Eq. 19)

By using this process it is possible to derive the instantaneous power as a function of time before then plotting the results. Table 5 details these variables and the final equations to derive power for each set of parameters.

Structure	Theoretical Capactiance (pF)	Frequency (rad/s)	Voltage (Vmax) (V)	Current (Imax) (pA)
75 µm	0.01596	2513.27	110	4.412
75 µm	0.01596	6283.19	110	11.03
75 µm	0.01596	12566.37	110	22.06
25µm	0.15363	2513.27	110	42.47
25µm	0.15363	6283.19	110	106.2
25µm	0.15363	12566.37	110	212.4
25µm	0.15363	18849.56	110	318.5
25µm	0.15363	2513.27	65	25.10
25µm	0.15363	6283.19	65	62.74
25µm	0.15363	12566.37	65	125.5
25µm	0.15363	18849.56	65	188.2

Table 5 The variables and constants for the derivation of the instantaneous power variables.

6.2.3 Comparison of how frequency affects P_i across the devices

Interpreting the results began by comparing the varying frequency results for the two devices as represented in Fig. 6.7 using the function Eq. 17 and inputting the variables from Table 5.

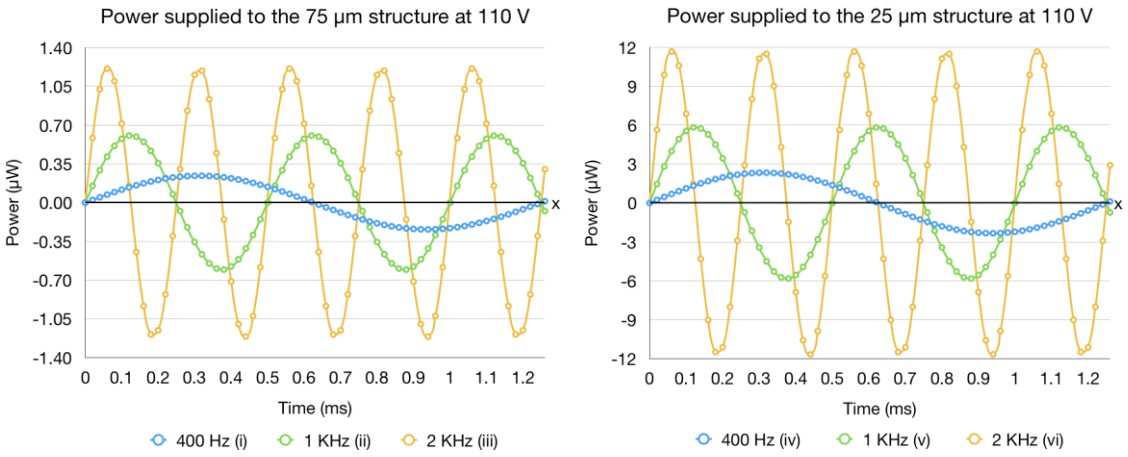

Fig. 6.7 Theoretical calculations for the effects of frequency on instantaneous power. Frequency was varied and the instantaneous power measured. A 75µm (left) device and 25µm (right) device. Both structures were supplied with 110 Volts.

From Fig. 6.7 the pattern of power supplied varies in a similar ratio irrespective of device architecture. Despite the feature size of the 25 µm structure being one third of the 75 µm structure, the power supplied appears to have increased by nearly a factor of 10. Evidently the device architecture is critical to the performance of the electroluminescent displays and therefore lowering the required driving voltage of the devices.

6.2.4 Establishing a model for reducing the driving voltage

Having determined the impact of reducing the feature size of the structures, attention can be turned to the driving voltages required to stimulate the phosphor particulate and illuminate the electroluminescent lamps. Table 5 illustrates the P_i of the 25 µm device as this device demonstrated a luminance at 65 V_{max} from the Fig. 6.5

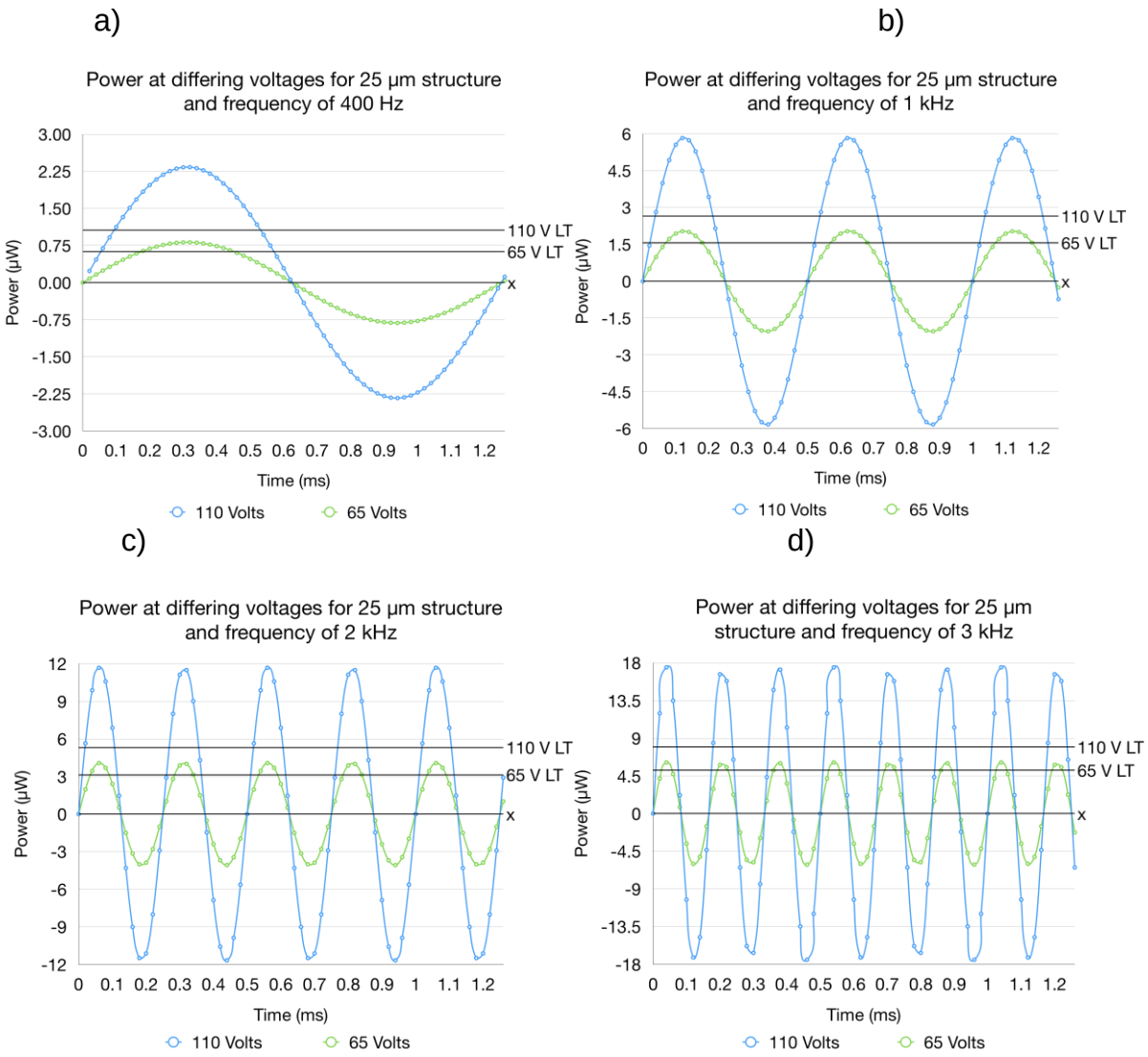

Fig. 6.8 Modelled representation of instantaneous power against time for 25µm structure, including Luminance threshold (LT). This shows a comparison of instantaneous power against time for the 25µm structure at a range of frequencies, a) 400 Hz, b) 1 kHz, c) 2 kHz and d) 3 kHz. Also included is the various luminance thresholds (LT) for power at each voltage supply. In each case demonstrating the possibility of the device emitting light.

By observing Fig. 6.8, it can be seen the instantaneous power for the 25µm device at two comparative supply voltages. It would appear the relationship is not linear. The ratio of the voltages, 65:110 (0.59), is not the ratio of the power values, ~0.8:~2.26 (~0.35), from c) in Fig. 6.8. The ratio for the instantaneous power values do appear to be consistent across each of the frequency ranges.

6.2.5 Defining luminance threshold

Also included in Fig. 6.8 is the different luminance thresholds (LT) for each set of variables. Given the field required to stimulate the phosphor particulates the power required to cause initial luminance to occur was calculated. This was defined as the luminance threshold. The LT can be derived by application of the power law and electric field equation in a capacitive structure:

$P = I \times V$ (Eq. 20),

and rearranging (Eq. 1):

$E_f = V/d$ (Eq. 1) gives: $V = E_f \times d$

Substitution of rearranged (Eq. 1) into (Eq. 20) gives (Eq. 21):

$P = I \times E_f \times d$ (Eq. 21)

The required field was defined as a constant value of 1 $x10^6$ V/m in section 1.4, the field strength required to stimulate the phosphor particulates. The spacing was also constant based on the 25 µm structure geometry. The current however varied in each case depending on frequency and could be extracted from Table 5. Table 6 is a table illustrating the different LT for the 25 µm device at 110 V_{max} and 65 V_{max} as shown in Fig. 6.8.

Spacing (µm)	Voltage (V_{max})	Current (Imax) (pA)	Electric field (E) (MV/m)	Power threshold (µW)
25	110	42.47	1.1	1.06
25	110	106.2	1.1	2.65
25	110	212.4	1.1	5.31
25	110	318.5	1.1	7.96
25	65	25.10	1.1	0.627
25	65	62.74	1.1	1.57
25	65	125.5	1.1	3.14
25	65	188.2	1.1	5.18

Table 6 A table modelling the minimum power luminance thresholds for the characterised structures that are graphed in Fig. 6.8.

For each for the LT there was a portion of the power function that exceeded this threshold value and proved that driving voltages below current operating voltages of 110 - 130 V are possible. The areas between the LT and the x-Axis graphed in Fig. 6.8 is equivalent to energy losses, either as heat or radiation at non-luminous frequencies.

6.2.6 Comparison with band gap energies

From evaluation of the instantaneous power calculations it can be determined that there is sufficient energy being supplied to the devices in order to stimulate the phosphor particulates. There are however other sources of power dissipation whereby energy is emitted at alternative non-luminous frequencies. From section 1.4.1 it was determined from [22] that the band gap required for emission of photons was 3.54 eV. Electrons 'falling' at 3.54 eV is equivalent to 5.672×10^{-19} Joules. The total power dissipated by the structures can be defined by the area below the curve in Fig. 6.8. By integrating the function of P_i given in Table 5, the total energy of the system can be determined. The efficiency of the phosphors can also be determined, the amount of useful energy for producing light as a fraction of the total energy dissipated by the system.

The instantaneous power calculations can be converted into energy calculations by multiplying by the time. Energy dissipated by the 25 µm structure operating at 400 Hz and stimulated by 65 V_{max}, suggests that estimated total energy supplied to the phosphor particulates is 252 pJ. Sufficient energy is therefore supplied to stimulate the ZnS particulates.

When the efficiency of the system is investigated, the area between the Luminance threshold and the maximum of the function is considered. Crude estimates for the energy dissipated suggest that operating at 110 V_{max} the devices are approximately 40% efficient, but when operating at 65 V_{max} this efficiency drops to approximately 10%. This demonstrates that driving voltages can be significantly reduced, the impact this has on the particles themselves is not fully understood, but provides scope for further research.

6.2.7 The effects of Phase shift

The electrode arrays were modelled as pure capacitors, that is to say that current leads voltage by a phase shift of $\pi/2$, as demonstrated in Fig. 6.6. This implies an idealised resistance load within the sinusoidal period. As evidenced by the images, we can see disruptive ohmic resistance and reactance, leading us to conclude that the impedance of the device is not perfect. Fig 6.2 demonstrated that the measured resistance of the gold films were higher that those calculated theoretically. This evidence led to the conclusion that the phase shift cannot be a perfect fit for a purely capacitive device. Phase shift leads to an interference between the resultant phase diagrams and inefficiencies for the device. The fragile nature of the device architecture within this work did not allow for investigation of the phase shift relationship.

6.3 Characterising a model for luminance

Luminance was measured and graphed in Fig. 5.8. The emission of the electrode arrays vary as supply voltage and frequency are manipulated. This manipulation leads to varying electric field properties. Knowing the relationship between variables, such as, the area and voltage are both directly related to the field, and knowing that the reactance is inversely related, we can set up the following

$$E_f = (AV)/X_c \qquad \text{(Eq. 22)}$$

Then substituting our reactance formula $X_c = 1/(2\pi fC)$ (Eq. 18), we can derive:

$$E_f = A \times V \times 2\pi fC \qquad \text{(Eq. 23)}$$

This provides a close model to the luminance output if we treat the emission as an exponential raised to the 6.3 degree, the model is applied to the graph for 75 µm track and gap taken from Fig. 5.4. In Fig. 6.9, the results are plotted.

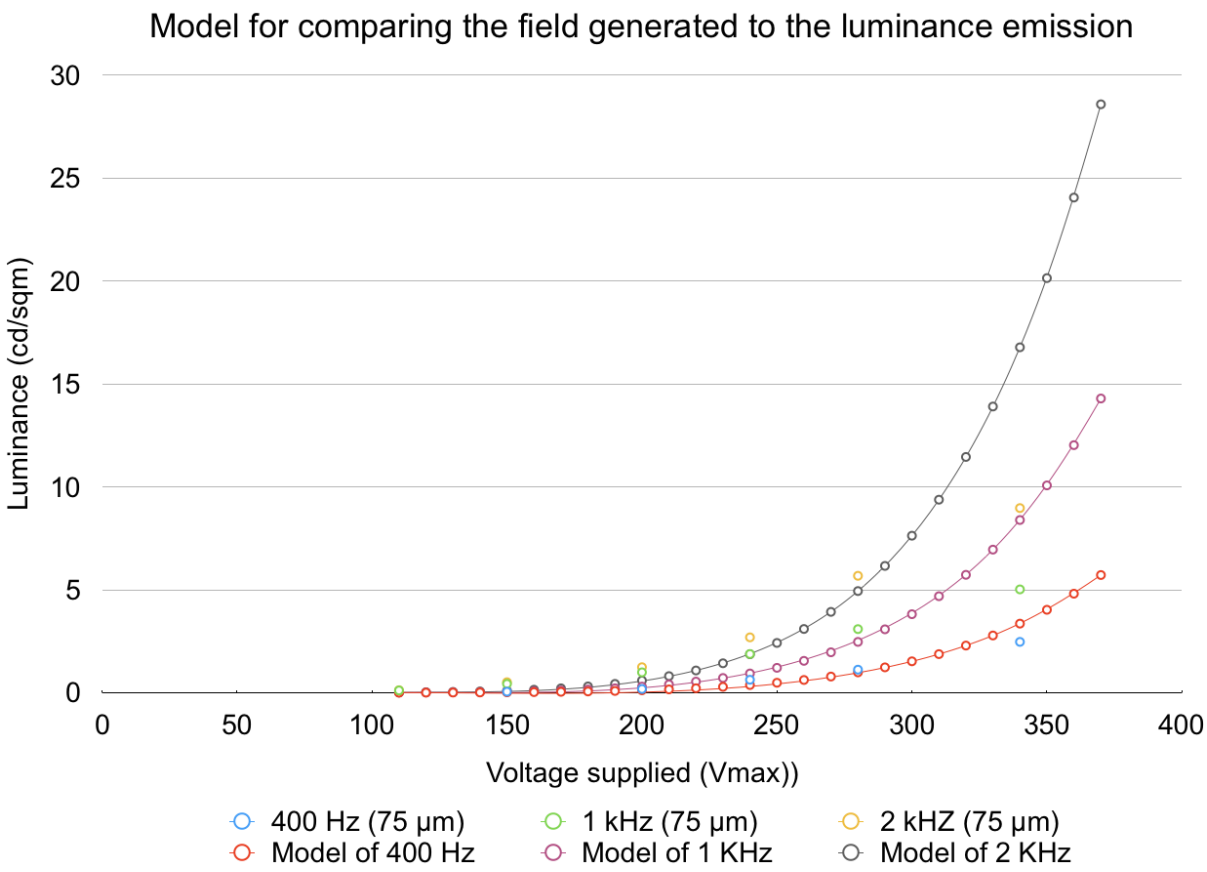

Fig. 6.9 A model to begin comparison between Electric field and luminance emission. The graph shows a strong trend up to a value of 280 V_{max}, beyond this point it appeared the device failed to support the model.

For an ac supply, as both the voltage and frequency are increased the energy delivered to each Cu_xS defect increased creating a more vigorous and therefore inefficient process. Were the device architecture robust enough it is hypothesised that greater Energy could be delivered by the improved quality of the print process.

Chapter 7
Conclusions and further work

7.1 Summary of conclusions

In conclusion, high electric field generators have been manufactured for a variety of applications. In this work particular attention has been paid to electroluminescent displays. Throughout the research it has been determined that gold provides the best conductor at micrometer size features. Paired with a chemistry of the alkane-thiol MUA and an iodine based etch solution, a range of structures were manufactured and characterised for their suitability for use in diagnostic luminance testing. The smallest feature size characterised was 25 µm. Although not tested due to a lack of conductivity, feature sizes of 10 µm track and gap were produced during several print trials. The devices were characterised for their luminance and power dissipation. Most notable was the production of an electroluminescent lamp with a 25 µm track and gap with an operating voltage of 65 V_{max}, nearly half commercial driving voltages. For electroluminescent displays, this has the potential to increase lifespan and reduce power consumption. For other applications of high electric field generators, much greater sensitivity can be achieved with various sensor applications.

The goal of this thesis was to explore the use of novel fabrication techniques for use in electronics. Much of the work centred on the fabrication techniques and limitations of microcontact printing. Although interest has begun to draw researchers, it has still remained an elusive task to pattern reliable charge carriers for us in electronics. Microcontact printing was explored throughout this thesis as a process for manufacturing novel circuit architecture and to a degree of success. Application of the designs centred on EL displays building on a wealth of knowledge available, but depending on the properties and characterisation these devices can be applicable to a variety of structures.

7.2 Contribution to knowledge

The contribution to knowledge as described in this thesis is the production of electroluminescent displays by means of microcontact printing methods utilising lower driving voltages using a novel architecture. Devices with a 25 µm track and gap interdigitated electrode array were produced and characterised to demonstrate that the driving voltages can be significantly reduced, consuming less power making them more economical. Electroluminescent displays are already hailed as ‘cold’ light due to current rates of efficiency, with the work of this thesis greater efficiency and reduced impact from decreased driving voltages was achieved.

7.3 Further work

7.3.1 Energy calculations

Much of the work in this thesis was centred on power. It was considered that from the power calculations completed to characterise the structures, energy consumption and efficiency could be established. This research understood power as a function of time, and using the formula: $P = E_n/t$ (Eq. 24), the amount of energy dissipated from the structures could be calculated. Integration of the function could define the quantity of energy in the area that was observed to emit light, using these values work could move towards how much of the energy supplied is attributed to the luminance of the structures.

The benefit to understanding the results in terms of energy would be to better understand where inherent losses in the process occur. It was observed that with an AC supply, producing a sinusoidal input signal incurs losses as current switches back and forth. Given that electroluminescent displays have a minimum threshold for producing light, it would be beneficial to better understand how the energy is converted to radiating forms that were not detected as light. Alternative devices that might make use of some of those outputs would help establish the best functionality of the devices, and potentially multiple uses of the same device.

7.3.2 Exploration of the energy losses of imperfect capacitive devices

The model developed for determining the luminance of the 25 µm structure has been based on the fact that the structures operate as purely capacitive load. In real world applications no device is considered ideal, therefore this theory, despite being true, doesn't represent the full picture. With regard to the instantaneous power calculations, there are multiple loads, inductive, resistive and capacitive, that skew the final power results. Although research has begun on these effects, there are by no means conclusive results. The analysis of interdigitated electrode arrays only increase the number of variables that affect the final power calculations.

7.3.3 Improvement to the printing process

The printing process itself has been well established and documented in this thesis. Despite there being significant improvement to the process functional devices were still proportionally low. Many solutions could help rectify this, automation was suggested to increase the reliability and precision of each step in the process.

Further investigation could have been done with the alkanethiol resist layers. They are usually used as seeding layers on which to mount biological material, potential exists to improve upon the resist layers by adding further steps to bolster the monolayer against the effects of the etching process.

7.4 Closing statements

This thesis has discussed the potential for using microcontact printing as a method for fabricating high electric field generators. The direct application of this body of work is in the area of electroluminescent displays but high electric field generators find widespread application in industry and microcontact printing has been demonstrated to provide high resolution conductive features. Taking one application of high electric field generators it has been demonstrated that these devices can be improved upon and run from lower voltages making them more environmentally friendly, longer lasting and more efficient.

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R.J.H. Young, P.S.A. Evans, G.I. Hay, D.J. Southee & D.J. Harrison, 'Electroluminescent Light Sources via Soft Lithography', Circuit World, Vol. 34 No. 3, 2008.

Poster Presentations:

R. Young, P.S.A. Evans & D.J. Harrison, 'Manufacturing Electronic Devices Using Embossing & Microcontact Printing', IeMRC Conference, Loughborough University, September 2007.

R. Young, P.S.A. Evans & D.J. Harrison, 'Manufacturing Electronic Devices Using Soft Lithography', IeMRC Reveiw, Loughborough University, March 2008.

R. Young, P.S.A. Evans & D.J. Harrison, 'Electric Field Generators', 3D-Mintigration, Greenwich University, September 2008.

R. Young, P.S.A. Evans & D.J. Harrison, 'Microcontact Printing for the Fabrication of Electrical Components', IeMRC Conference, Henry Ford College, September 2009.

Conference Presenations:

R. Young, P.S.A. Evans & D.J. Harrison, 'Manufacturing Electronic Devices via Soft Lithography', UK - Displays & Lighting KTN, Newtown, Wales. April 2008.

R. Young, P.S.A. Evans & D.J. Harrison, 'Manufacturing Electronic Devices Using Microcontact Printing, Research Student Conference, Brunel University, June 2008.

R. Young, P.S.A. Evans & D.J. Harrison, 'Microcontact Printed Electroluminescent displays', Plastic Electronics: the challenges of low temperature manufacturing, Cambridge University, March 2011.