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Pipelined photonic analog-to-digital converter

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Abstract

Electronic analog to digital converters (EADCs) face serious challenges when the root mean square timing jitter of the sampling pulse is less than a femtosecond. This restriction limits the maximum allowable sampling frequency of an EADC. In photonic analog-to-digital conversion (PADC), using a mode locked laser as a sampling source limits the sampling frequency timing jitter only at sub-femtosecond levels. The current architectures for PADC use photonic techniques either for sampling or for quantization. Consequently, current PADC architectures are not suitable for higher frequency applications because of the limitations of their electronic components. In this paper, the feasibility of implementing concept architecture for a fully photonic pipelined ADC is analyzed and evaluated to provide a design for an 8-bit pipelined PADC, the performance of which is investigated through modeling and simulation. The 8-bit pipelined PADC's effective number of bits is shown to be 4.34 bits at 200 gigasample per second.

Keywords: analog to digital converter (ADC), photonic analog-to-digital converter (PADC), data conversion

(Some figures may appear in colour only in the online journal)

1. Introduction

Digital systems achieve a better dynamic range than analog systems, and more appropriately interface with other systems [1], are flexible, more reliable and robust against additive noise. Data converters such as analog-to-digital converters (ADCs) and digital-to-analog-converters (DACs) are the interfaces between the analog and the digital worlds of signal processing. In general, there are the following known architectures for electronic ADCs (EADCs): (1) Sigma-Delta, (2) successive approximation register (SAR), (3) pipelined, (4) flash, and, (5) folding [2, 3].

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Sigma-Delta EADCs have the highest resolution with sampling rates from k-sample(s) to megasample(s). In the SAR EADC scheme, the sampling rate must be lower than the internal clock frequency, which is the key disadvantage of the SAR EADC architecture. While SAR EADCs are not the fastest, because of a favorable cost-benefit, the SAR EADC architecture is common. When latency requirements are relaxed the pipelined architecture is useful. The pipelined architecture has the best overall performance and is an appropriate choice when high performance is required. Flash EADCs are the fastest single-standing EADC topology, the operation of which relies on the parallel decision of a number of comparators, but N-bit conversion needs $2\hat{}N-1$ comparators. This increase in the number of comparators as N increases linearly puts an upper limit on resolution and results in increasingly high power dissipation and input capacitance. However, a flash EADC is suitable when low resolution is acceptable and low latency is required. Folding is a technique where the quantization decision is divided into parts with

flash sub-ADCs each quantizing a part of the full resolution [4].

The effective number of bits (ENOB) of the EADCs based on speed, resolution, and the impact of timing jitter on the EADC's performance highlight the technical challenges facing EADCs such as reducing aperture uncertainty to below 0.1 ps and increasing sampling frequencies beyond 10 GHz while providing an ENOB of about 6. A photonic ADC (PADC) is a system that uses photonic technology to digitize an analog radio frequency (RF) electronic signal, to address the challenges faced by EADCs, by using mode locked laser (MLL) pulses with femtosecond timing jitter. PADCs are promising candidates for realizing over ten Gsample(s) ADCs with an ENOB about 7 bits [5]. There are four known architectures for PADC: (1) photonic assisted ADC, (2) photonic sampling and electronic quantization (PSEQ) ADC, (3) electronic sampling and photonic quantization (ESPQ) ADC, and (4) photonic sampling and quantization (PSPQ) ADCs [6].

In photonic assisted ADC architecture, an RF signal is modulated onto an optical carrier; an ultra-stable MLL source switches an electronic track and hold circuit. The advantages of these systems are: (a) reduced aperture time, (b) high clock isolation, (c) low clock jitter, (d) optical clock distribution, [7–13].

In PSEQ techniques, an MLL may be used to sample an electronic representation of an RF signal and quantization is performed using a single high rate EADC, [14–16], however, this system is a photonic assisted EADC. Two major sources of error in PSEQ ADCs are pulse-to-pulse amplitude fluctuation and timing jitter. This architecture requires that the modulator response is linear, one way to obtain a linear response is to use a low modulation index but this often increases the optical power requirements. Another solution is to digitize both outputs of a Mach–Zehnder modulator (MZM) and invert the nonlinear transfer function of the modulator by post processing, [17–20]. Other key requirements are linearity of the photo diode and high-speed EADC to perform the quantization of the sampled values in the electrical domain at the same rate as the MLL pulse rate. Path matching, cross talk, and calibration are also important issues. In [21], a PSEQ ADC is presented that exploits optical comb generation for sampling.

In ESPQ techniques, an electronic sample and hold circuit produces a staircase voltage waveform that is used to vary the wavelength of a semiconductor laser, then different optical filters and electronic detectors are used to quantize the sampled signal, [6]. The main weakness of this technique is sampling is in the electronic domain so suffers significant timing jitter. In [22, 23], a cascaded phase modulator system for high-speed PADCs is reported that utilizes distributed phase modulation to quantize the signals in the optical domain based on the architecture in [24]. The spatially distributed successive approximation register ADC scheme in [5] is an architecture integrating those of [22–24] to encode an input analog voltage into the carrier signal phase. This cascaded photonic signal processing departs from previous photonic architectures by dramatically reducing the electronic ADC hardware complexity, analog signal channel timing, and synchronization. However, photonic and electronic matching delays are required to synchronize successive stages in this feed-forward approach.

In [6], PSPQ techniques are classified into optically sampled and intensity modulation (OSIM), optically sampled and angle modulation (OSAM) and optical sigma-delta modulator techniques. The OSIM and OSAM techniques are based on PSEQ. The sigma-delta modulator technique tolerates low sampling rates but also mixes optical and electronic techniques.

In this paper, the implementation of a fully photonic pipelined ADC concept architecture is analyzed and evaluated to provide a design for a PADC, the performance of which is investigated through modeling and simulation using Optiwave-optisystem and the MATLAB tools environment. The concept architecture of pipelined ADC is discussed in section 2. In section 3, an architecture is proposed for a pipelined PADC and analyzed based on a 2-bit pipelined PADC design. In section 4, an 8-bit pipelined fully photonic ADC is presented and its simulated performance compared with that of state-of-the-art PADCs reported in the literature. The conclusions are presented in section 5.

2. All-photonic pipelined ADC concept architecture

Wideband analog to digital conversion is a critical problem encountered in broadband communication and radar systems. Pipelined architecture ADCs are popular for such applications due to their sustained high sampling rates, low power consumption, and the linear scaling of their complexity. The term 'pipelined' refers to the stage-by-stage processing of an analog input signal. Pipelined architecture consists of several cascaded stages and timing circuits, it offers a good trade-off between conversion rate, resolution and power consumption. The concurrent operation of all pipelined stages makes this architecture suitable to achieve very high conversion rates. The overall speed is determined by the speed of a single stage [25].

In figure 1(a), for an M bit output, after the analog input signal enters the ADC, each subsequent pipelined stage of the ADC resolves the $(M-(J-1))$th bit, $1 \leqslant J \leqslant M$, to be contributed to the final conversion output. Simultaneously, after each stage has finished quantizing its input sample, it outputs an analog residue signal that serves as the input to the next stage. Each stage's digital decision is then passed to a digital block that properly retimes the output bits then the final digital decision is produced.

The block diagram of the pipelined ADC's Jth stage is shown in figure 1(b). The input signal is sampled in each stage. Subsequently, a k-bit flash ADC quantizes the analog signal and produces a digital decision of k bits. The digital decision is then fed through a k-bit flash DAC to be re-converted into an analog signal. The summation node takes the input signal and subtracts the DAC output signal from it. This difference signal is then fed through a gain stage with gain G to produce the residue voltage the output of this stage [26, 27]. This means that all the stages can be implemented

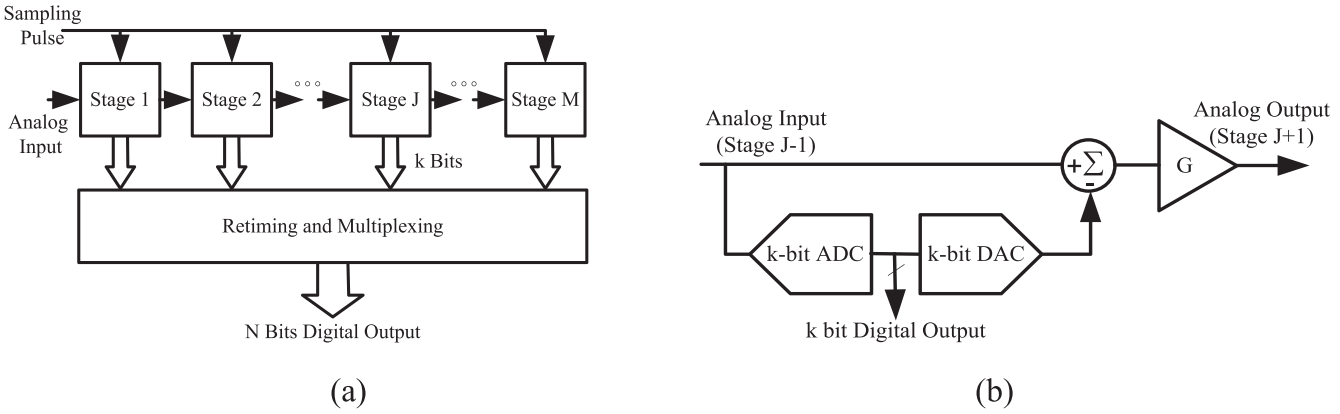


Figure 1. (a) A basic block diagram of a pipelined ADC, (b) pipelined ADC Stage J's block diagram.

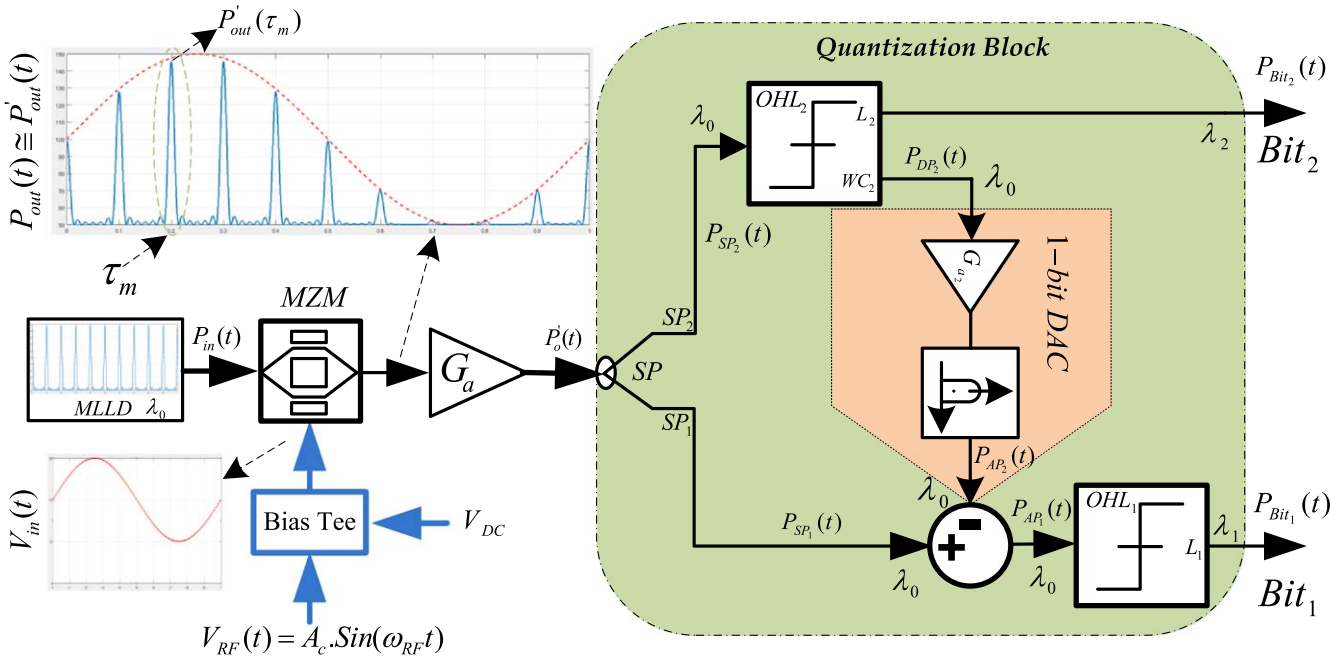


Figure 2. The proposed architecture of a 2-bit PADC.

identically and there is a linear relationship between the resolution and the required hardware.

However, recent EADC systems still experience problems such as jitter in the sampling clock, the settling time of the sample and hold circuit, the speed of the comparator, mismatches in the transistor thresholds and passive component values. The limitations imposed on EADCs by these factors become more severe at higher frequencies, which is why pipelined PADCs involving electronic components have not been proposed. In the next section, a novel architecture for an all-photonic pipelined ADC is proposed which is shown to have the potential to overcome the limitations of pipelined EDAC at higher frequencies.

3. The proposed pipelined PADC architecture

The proposed architecture of a pipelined PADC is depicted in figure 2. To discuss and analyze the proposed architecture in detail and evaluate its implementation, the feasibility a 2-bit pipelined PADC architecture is first considered. At the end of this section the generic mechanism for the quantization of a sampled signal at the output of the optical amplifier Ga into *N*-bits is presented based on the proposed architecture. As shown in figure 2, an RF signal, $V_{\mathrm{RF}}(t)$ is sampled by a sampling pulse train $P_{\mathrm{in}}(t)$. The sampled signal $P_{\mathrm{out}}(t)$ is connected to the input of a 1-bit ADC and the positive input of a subtractor. The 1-bit ADC quantizes the sampled signal, which generates the most significant bit (MSB) B_2 at the output. Based on pipelined architecture, the MSB output signal is converted back to analog form using a 1-bit DAC, the input of which is connected to the output of the 1-bit ADC. The generated signal at the output of the 1-bit DAC, $P_{AP_2}(t)$, is subtracted from the input sampled signal $P_{SP_1}(t)$. The resulting signal, $P_{AP_1}(t)$, is given by:

$$P_{AP_1}(t) = P_{SP_1}(t) - P_{AP_2}(t). \tag{1}$$

The output signal of the subtractor, $P_{AP_1}(t)$, is fed to the second 1-bit ADC, to be quantized as the least significant bit (LSB), B_1.

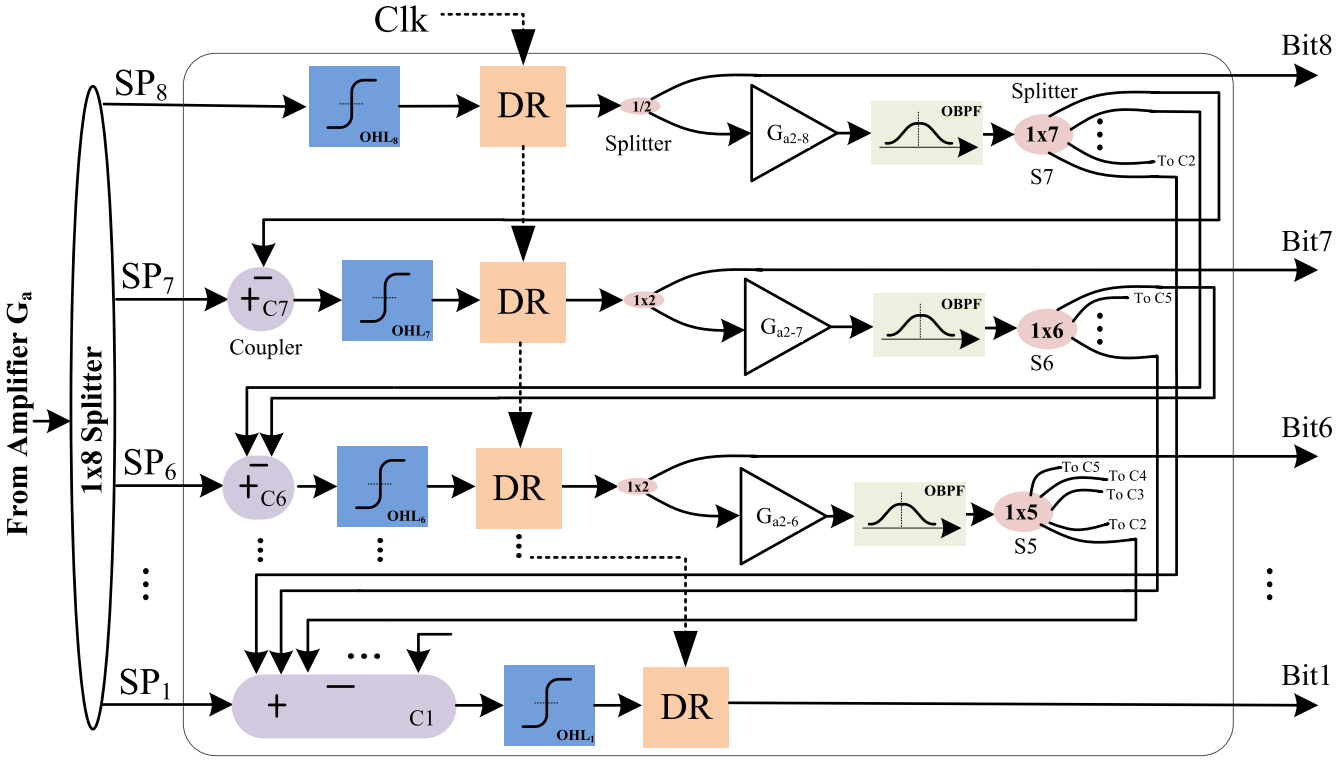


Figure 3. Photonic signal quantization block for the 8-Bit PADC deployment.

To consider the impact of physical impairments very close to those of a practical realization of the system, a physical model of the 2-bit PADC system in the optical domain is shown in figure 2. In the model, the optical pulse is generated based on the model of a mode locked laser diode (MLLD) [27], which is fed to a dual drive MZM. In the proposed system, an MZM is used as a modulator and a sampling component, the transfer function of which is given by:

$$P_{\text{out}}(t) = \frac{\alpha P_{\text{in}}(t)}{2}\left[1 + \cos\left(\frac{V_{\text{in}}(t)\pi}{V_{\pi}}\right)\right], \tag{2}$$

where α is the insertion loss of the modulator, $P_{\text{out}}(t)$ is the output optical power of $E_{\text{out}}(t)$, which is the modulated electrical field at the output of the MZM and $E_{\text{in}}(t)$ is the input optical power of $P_{\text{in}}(t)$, which is the amplitude of the electrical field of the input optical carrier that is generated by the modelled MLLD and is launched into the MZM input [27], where $V_{\text{in}}(t)$ is the voltage of an applied RF and DC bias signal and V_{π} is a half-phase voltage [14].

It is assumed in that the electrical field $E_{\text{in}}(t)$ at the input of the MZM, which is launched by the MLL laser diode, can be represented by:

$$\begin{aligned} E_{\text{in}}(t) &= \sum_{q=-n}^{n} E_q \exp[i(\omega_0 + q\Delta\omega)t] \\ &= e^{i\omega_0 t}\sum_{q=-n}^{n} E_q \exp[i(q\Delta\omega)t], \end{aligned} \tag{3}$$

where $(2n + 1)$ is the number of longitudinal modes oscillating with the qth electrical field amplitude E_q and ω_0 denotes the angular frequency of the electrical field of the optical carrier, respectively, and $\Delta\omega$ is the frequency difference between two consecutive modes. In equation (3), the electrical field spectral envelope of the qth mode can be approximated by a Gaussian distribution

$$E_q^2 = E_0^2 \exp\left[-\left(\frac{2q\Delta\omega}{\Delta\omega_L}\right)^2 \ln 2\right], \tag{4}$$

where $\Delta\omega_L$ represents the full wave half maximum (FWHM) bandwidth. If the number of modes $(2n + 1)$ increases without limit, the series of equation (3) can be approximated by an integral:

$$E_A(t) = \lim_{n\to\infty}\sum_{q=-n}^{n} E_q \exp[i(q\Delta\omega)t] \cong \int_{-\infty}^{+\infty} E_q e^{iq\Delta\omega t} dq. \tag{5}$$

The field amplitude $E_A(t)$ is seen to be proportional to the Fourier transform of the spectral amplitude E_q. $E_A^2(t)$ and correspondingly the optical pulse power can be approximated by a Gaussian function of time which can be written as

$$P_{\text{in}}(t) \propto E_A^2(t) \cong P_0 \exp\left(-\frac{t^2}{\tau^2}\right), \tag{6}$$

where $\tau = 2\sqrt{\ln(2)}/\Delta\omega$ and p_0 is the optical pulse peak power. Note that $\Delta\tau_p = 2\sqrt{2\ln(2)}\tau$ is the FWHM time duration of the MLL pulse.

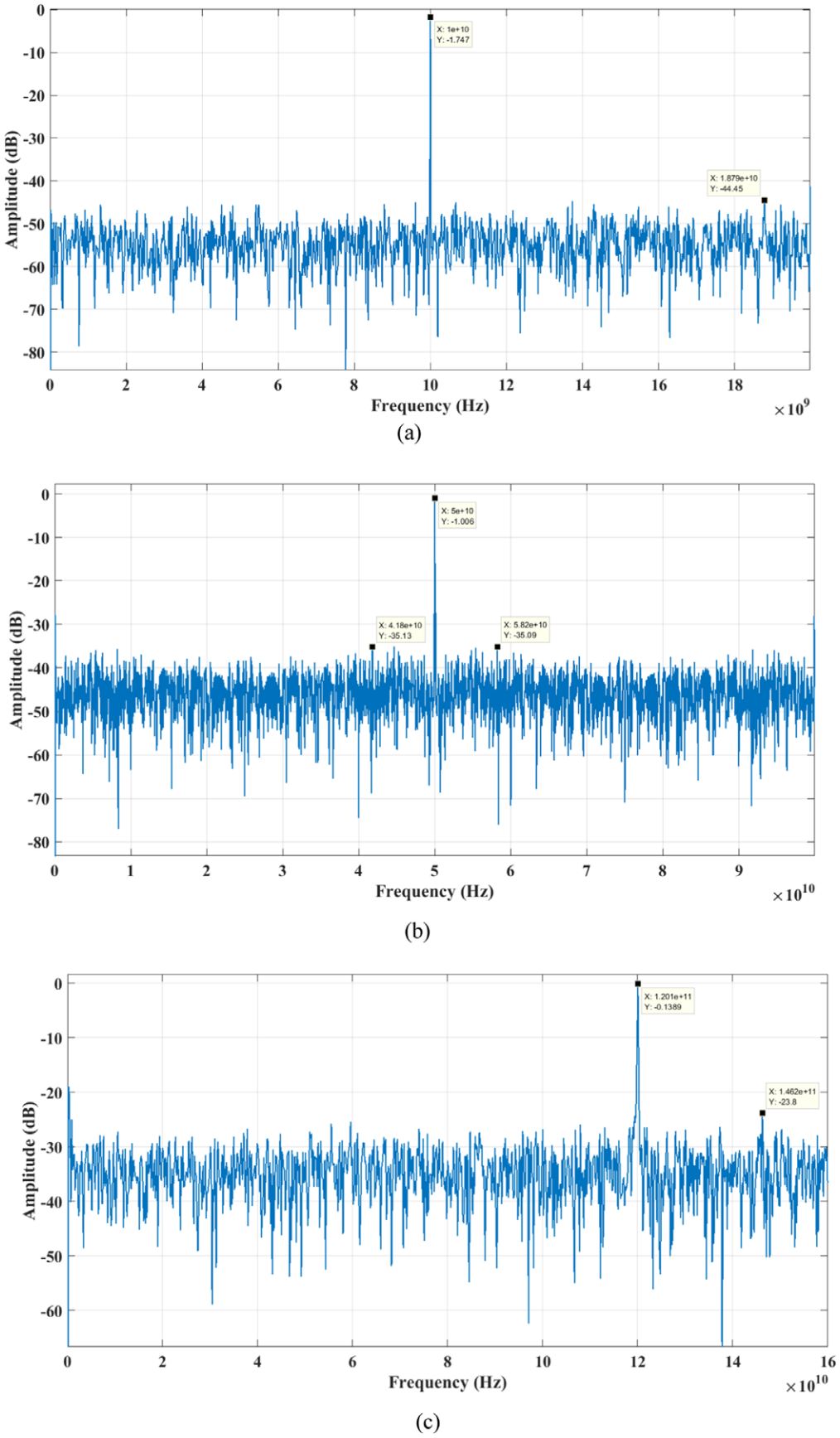


Figure 4. FFT of the 8-Bit ADC output of a single tone input sampled: (a) at 40 GHz of sampling frequency for a 10 GHz input RF signal. (b) At 200 GHz of sampling frequency for a 50 GHz input RF signal. (c) at 320 GHz of sampling frequency for a 120 GHz input RF signal.

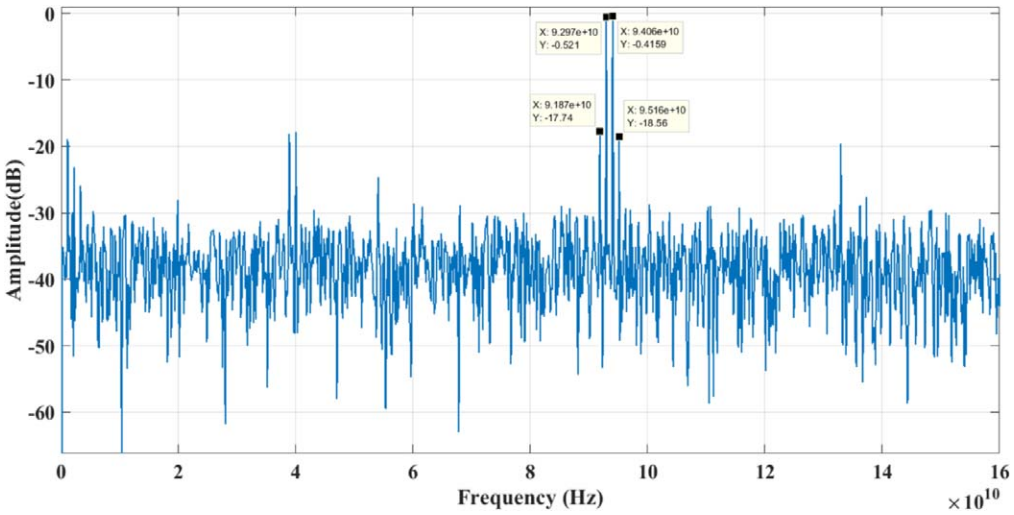
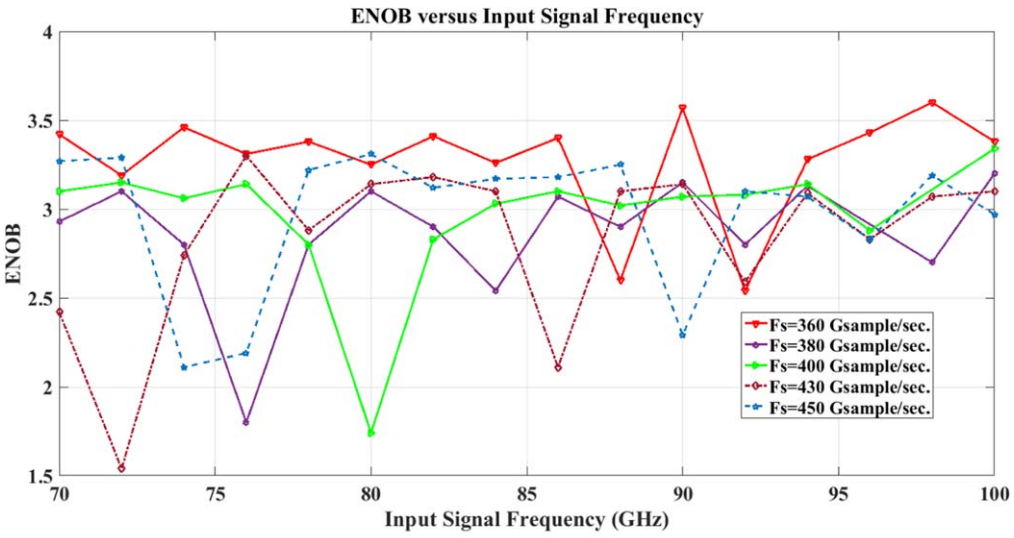
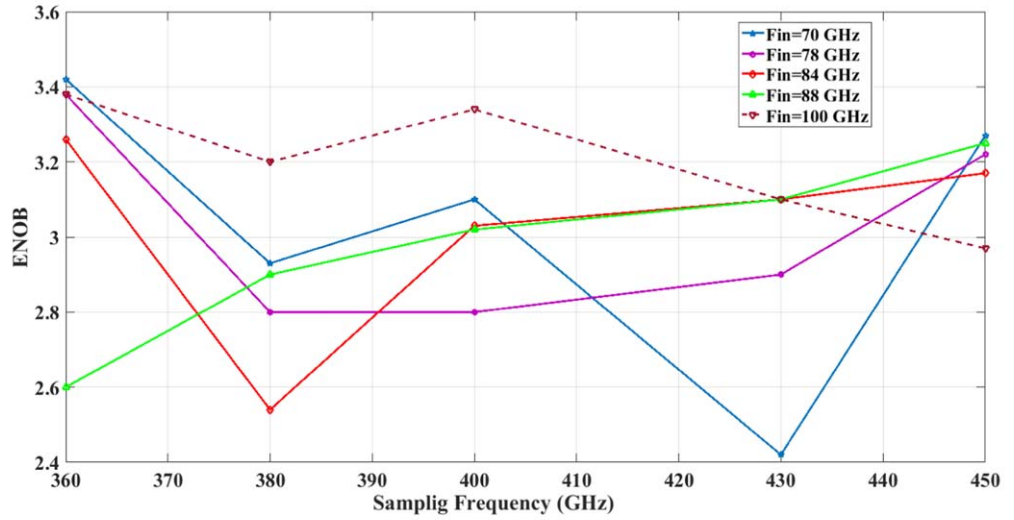


Figure 5. FFT of the 8-Bit ADC output of two-tone inter-modulation at 93 and 94 GHz for a 320 GHz sampling frequency.



(a)



(b)

Figure 6. ENOB versus: (a) input signal frequency for different sampling frequencies, (Fs). (b) Sampling frequency for different input signal frequencies (Fin).

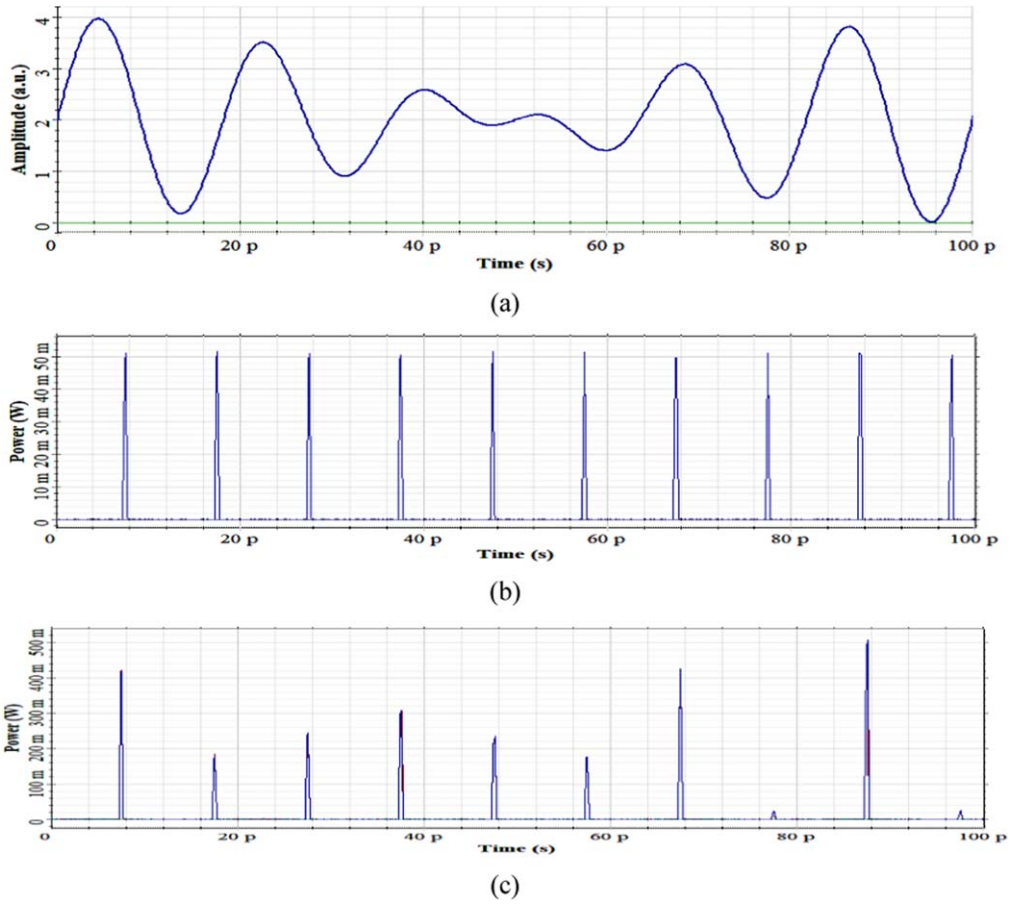


Figure 7. PADC waveforms: (a) the analog input signal, (b) the MLLD generated pulse train, (c) the sampled signal at the MZM output.

It is assumed a sample single tone RF carrier $V_{RF}(t)$ can be given by:

$$V_{RF}(t) = A_c.\sin(\omega_c t) \tag{7}$$

and

$$V_{in}(t) = V_{DC} + V_{RF}(t), \tag{8}$$

where A_c and ω_c are the amplitude and the frequency values of the RF carrier, and V_{DC} is the bias voltage of the MZM, respectively, and all parameters are constant.

The MZM in the concept architecture of figure 2 samples the input electrical RF signal $V_{RF}(t)$ and modulates it onto the optical carrier. Substituting equations (6) and (8) in (2), the optical power at the output of the MZM can be expressed by:

$$P_{out}(t) = \frac{\alpha P_{in}(t)}{2}\{1 + \cos[V + U\sin(\omega_c t)]\}, \tag{9}$$

where V is $\frac{V_{DC}\pi}{V_\pi}$ and U is the modulation index equal to $\frac{A_c\pi}{V_\pi}$. Regardless of the magnitude of $V_{RF}(t)$, the lowest harmonic distortion is achieved at the quadrature operating point of the MZM transfer function at $V_{DC} = \frac{V_\pi}{2}$. Therefore, $V = \frac{\pi}{2}$ and equation (9) can be rewritten:

$$P_{out}(t) = \frac{\alpha P_{in}(t)}{2}[1 - \sin\{U\sin(\omega_c t)\}]. \tag{10}$$

By using the Bessel function [7], to expand the element inside of the brackets of equation (10), the output optical power can be expressed as:

$$P_{out}(t) = \frac{\alpha}{2}P_{in}(t)\left[1 - 2\sum_{k=1}^{\infty}\{J_{2k-1}(U).\sin[(2k-1)\omega_c t]\}\right], \tag{11}$$

where $J_k(U)$ denotes the first kind Bessel function for any integer k.

$$J_k(U) = \frac{1}{\pi}\int_0^{\pi}\cos(U\sin\theta - k\theta)d\theta. \tag{12}$$

As the higher order first kind Bessel functions can be ignored, equation (9) can be approximated by

$$P_{out}(t) \cong \frac{\alpha}{2}[1 - 2J_1(U)\sin(\omega_c t)]P_{in}(t). \tag{13}$$

By selecting a proper modulation index (U), equation (13) can clearly express intensity modulation and the optical pulse envelope of the RF signal modulated onto the MLL optical carrier. Equation (13) can be expressed as

$$P_{out}(t) \cong K_1 P_{in}(t) + K_2\sin(\omega_c t)P_{in}(t), \tag{14}$$

where $K_1 = \frac{\alpha}{2}$ and $K_2 = -\alpha J_1(U)$.

As the amplitude of the optical Gaussian sampling pulse train p_0 is constant, considering the width of the MLL optical pulse ($\Delta\tau_p$) in comparison with the period of the sample RF signal ($\tau_c = 2\pi/\omega_c$) when $\Delta\tau_p \ll \tau_c$, the optical pulse can be

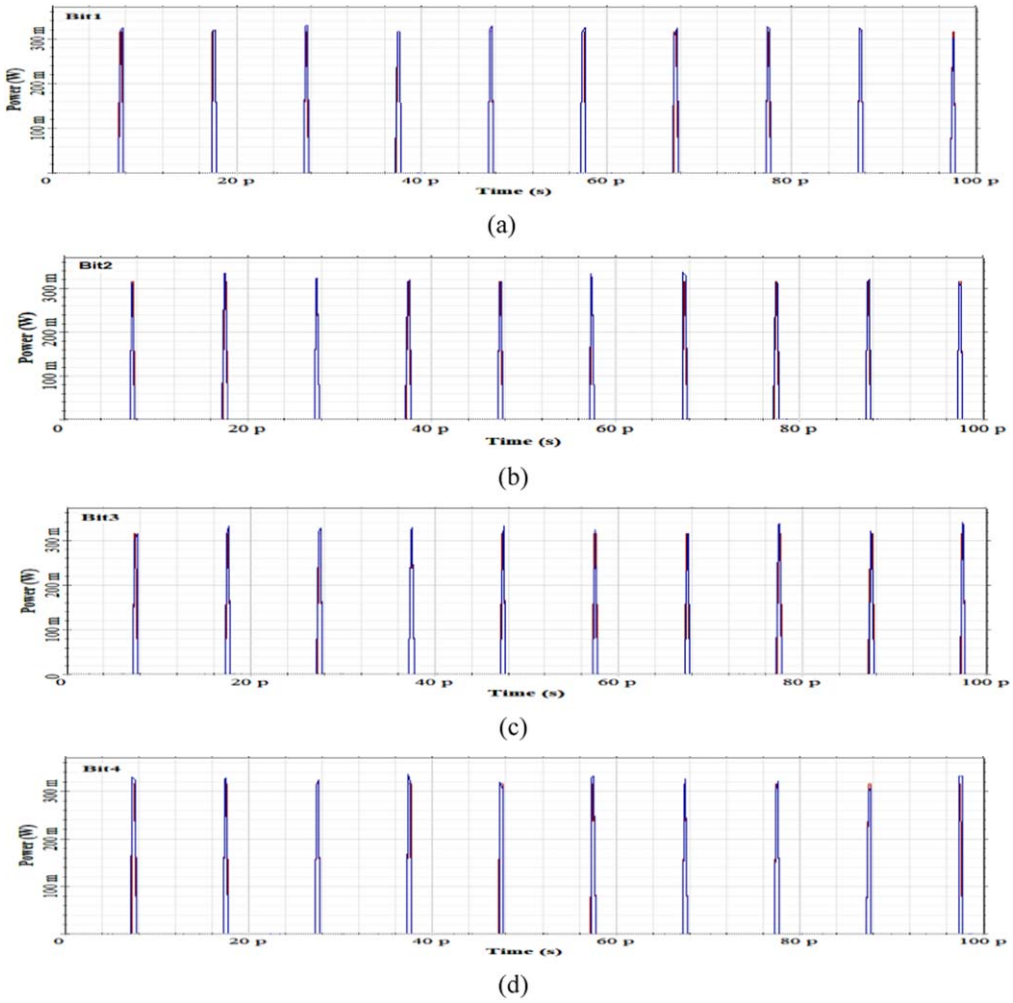


Figure 8. The digital data generated at the PADC's output by sampling a 55 GHz RF signal at 200 GHz: (a)–(h) Bit_8-Bit_1.

approximated as an impulse sampling train. Therefore, the first term of equation (13) is approximately constant over time $\Delta\tau_p$. Therefore, the first term of equation (14) is constant. By considering the second term of equation (14), at the mth sampling instant τ_m, the peak of the output optical power of the MZM $P'_{\text{out}}(\tau_m)$ can be approximated by

$$P'_{\text{out}}(\tau_m) \cong K_2 P_0 \sin(\omega_c \tau_m). \tag{15}$$

The amplified sample sequence is split into two parts SP_1 and SP_2. The amplifier with gain G_{a1} is used to compensate the power division proportion rate of the splitter and the insertion losses of the splitter and the MZM by pre-amplifying the samples at the output of the MZM. The symmetrically split power of the splitter outputs can be given by:

$$P'_o(\tau_m) = G_a.P'_{\text{out}}(\tau_m), \tag{16}$$

$$P_{SP_2}(\tau_m) = P_{SP_1}(\tau_m) = \frac{P'_o(\tau_m)}{2}. \tag{17}$$

As shown in figure 2, the output signals of the splitter are fed to a fully optical pipelined quantization block. The quantization block has the following sub-blocks: optical hard limiters (OHLs), [28], a 1-Bit PDAC and an optical subtractor, which are discussed in [29, 30]. The two splitter outputs correspond to the number of quantization bits. The SP_2 power, $P_{SP_2}(\tau_m)$, is fed to the input of OHL_2 to perform the quantization of the MSB Bit_2. The OHL_2 threshold level has been setup based on the half-magnitude of the full-scale amplitude of the corresponding electrical field at the output of the splitter, which is proportional to the corresponding input electrical signal amplitude. Comparing the input signal power $P_{SP_2}(\tau_m)$ with the threshold level power $P_{\text{th-Bit}_2}$, the corresponding optical power of the MSB, can be expressed as:

$$P_{\text{Bit}_2}(\tau_m) = \begin{cases} P_h & P_{SP_2}(\tau_m) \geqslant P_{\text{th-Bit}_2} \\ P_l & \text{Otherwise} \end{cases}. \tag{18}$$

If the input signal power $P_{SP_2}(\tau_m)$ was greater than $P_{\text{th-Bit}_2}$, then the corresponding output bit $P_{\text{Bit}_2}(\tau_m)$ is 'one $= P_h$', otherwise it is equal to 'zero $= P_l$'. OHL_2 has two possible outputs L_2 and WC_2. The wavelength of output WC_2 is identical to the input wavelength λ_0 and WC_2 is used for the quantization process. However, the output WC_2 passes through a 1-bit DAC. The 1-bit DAC is a key component of the proposed PADC. This architecture includes an optical amplifier and a Gaussian filter. The combination of these two components performs the 1-Bit DAC task. In this model, the amplifier gain G_{a2} is setup based on the quantization threshold of the predecessor quantized bit, Bit_2. The gain G_{a2} of the

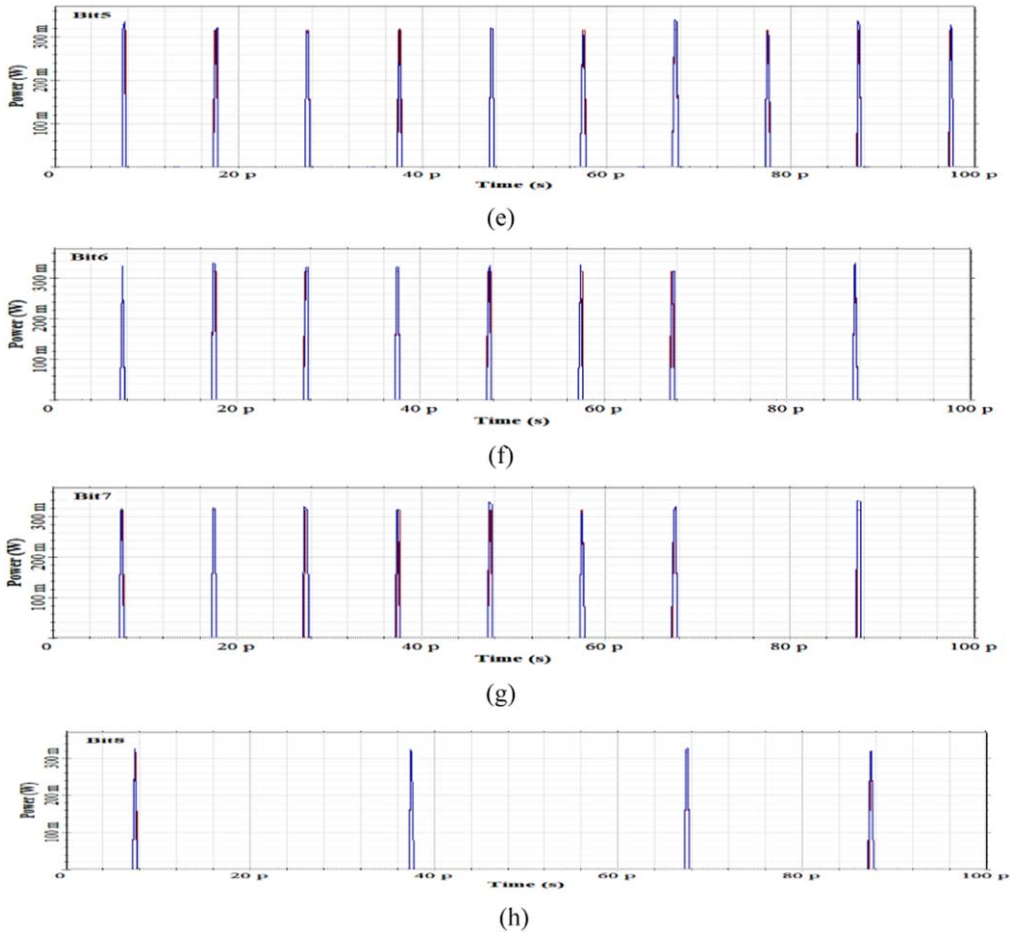


Figure 8. (Continued.)

amplifier is close to the ratio of P_h and $P_{\text{th-Bit}_2}$, in dB so G_{a2} can be given as:

$$G_{a_2}(dB) = P_h(dB) - P_{\text{th-Bit}_2}(dB). \tag{19}$$

The 1-Bit PDAC is a tuneable block that depends on the sampling rate of the PADC and its parameters, such as its amplifier gain, and on the optical bandpass filter (OBPF) bandwidth having been setup properly; for each sampling frequency region there is a suitable set point at which the PADC gives its best achievable performance.

To quantize the LSB of the PADC, Bit_1, the output power of the 1-bit PDAC is subtracted from $P_{SP_1}(t)$. The power magnitude of the output of the WC_2 of the OHL_2, $P_{DP_2}(\tau_m)$, is approximately equal to $P_{\text{Bit}_2}(\tau_m)$ but their wavelengths are different. Therefore, the powers at the outputs of the 1-Bit PDAC can be given by

$$P_{AP_2}(\tau_m) = G_{a_2}.|P_{\text{Bit}_2}(\tau_m)|, \tag{20}$$

$$P_{AP_1}(\tau_m) = P_{SP_1}(\tau_m) - P_{AP_2}(\tau_m). \tag{21}$$

The output of the subtractor is fed into OHL_1 to quantize the amplitude of the pulse representation of Bit_1. The output L_1 represents Bit_1 at the wavelength λ_1. Therefore, comparing the input signal power $P_{AP_1}(\tau_m)$ with the threshold level power $P_{\text{th-Bit}_1}(\tau_m)$, the corresponding optical power of the LSB, can be expressed as:

$$P_{\text{Bit}_1}(\tau_m) = \begin{cases} P_h & P_{AP_1}(\tau_m) \geqslant P_{\text{th-Bit}_1} \\ P_l & \text{Otherwise} \end{cases}. \tag{22}$$

If the input signal power to OHL_1, $P_{AP_1}(\tau_m)$, was greater than $P_{\text{th-Bit}_1}(\tau_m)$, then the corresponding output bit $P_{\text{Bit}_1}(\tau_m)$ is 'one $= P_h$', otherwise it is equal to 'zero $= P_1$'.

Based on the above analysis a concept of an all-photonic architecture for pipelined PSPQ ADC for N-Bit quantization can be proposed. As shown in figure 2, in the concept architecture an MZM electro-optical modulator (EOM) samples an input RF signal using an MLLD generated pulse train. The optical power of the sampled pulses is split into N levels using a symmetrical optical splitter, where N denotes the number of quantization bits instead of the two levels of figure 2, the split signals are then fed to a photonic signal-processing subsystem for quantization and wavelength conversion operations. A flowchart of the quantization process was presented in [30]. At the first stage of the quantization process, in which the number of the stages is equal to the number of quantization bits N, the stage number S is equal to '1'. For quantization of the MSB the received signal from output number 'N' of a symmetrical splitter SP_out(M) is identified by the generic number 'M' which is equal to 'N' at this stage. This output optical signal is compared with a reference quantization level equal to '$2(M-S)$ $^*A$', where A'

Table 1. A comparison of PADCs.

References	Type of results	Year	ENOB	Sampling frequency (GHz)	Input frequency (GHz)	Architecture
[9]	Experimental	2003	3.5	40	—	Photonic assisted
[32]	Experimental	2008	7	40	—	PSEQ
[33]	Experimental	2009	10.2	25	—	Photonic assisted
[34]	Experimental	2006	<4	—	—	PSEQ
[35]	Experimental	2009	7	41	—	PSEQ
[36]	Experimental	2012	3.5	—	10	PSEQ
[22]	Experimental	2007	4.1	—	2.2	PSEQ
[23]	Experimental	2008	4.3	—	2.5	PSEQ
[5]	Simulated	2012	3.45	40	2.5	PSEQ
[37]	Simulated	2009	8	40	—	PSEQ
[21]	Experimental	2016	3.4	20	—	PSEQ
This work	Simulated	2018	4.34	200	50	All-photonic pipelined

is a constant parameter. If the signal power square is greater than or equal to '$2(M-S)$ $^{*}A$', the output quantization bit is '1', otherwise, it is '0'. This process would be performed using an OHL block. As in the pipelined architecture the quantized bits must be converted back into the analog domain, in stage number '$(M-S)$' the converted back analog signals from stages 'N' to '$(M-S+1)$' of the process are subtracted from the input of the split output signal SP_out $(M-S)$, then the given signal is compared with '$2(M-S)$ $^{*}A$'. The quantization process is repeated in parallel 'N' times to quantize each sampled optical signal into 'N' bits.

4. Discussion of the PADC functionality and performance

In this section, an 8-bit PADC is based on the concept architecture that was discussed in section 2 is evaluated. Using optiwave-optisystem and MATLAB simulation tools, the proposed PADC architecture is modelled and simulated, its functionality is demonstrated, and its performance is investigated. With respect to figure 2, for changing the 2-bit PADC architecture to an 8-bit PADC, the digitized optical signal's power at the output of optical amplifier G_{a1} is split into 8 channels by replacing the 1×2 splitter with a 1×8 splitter. Each output of the splitters, SP_{i} (where $i = 1, 2\ldots, 8.$) is fed to a photonic signal quantization block as shown in figure 3. In this system, a data recovery (DR) block is used to synchronize all functions with the MLLD sampling pulses. The DR block is discussed in detail in [31]. One output of each 1×2 splitter is a digitized output of the PADC and the other output is connected at each stage to the input of a 1-bit PDAC. To obtain each bit of lower significance, it is necessary to subtract all bits of higher significance converted back to analog values from the corresponding sampled signal, the output of each 1-bit PDAC is split into $(i-1)$ outputs, where i indicates the significance of each bit. For example, for the bit3 quantization stage, the coupler number 3, (C3), needs to subtract SP_3 from the output signals of S_7 to S_4. The sampling pulse is generated using a modeled MLLD and sampling, the EOM is a dual driven MZM with splitting ratio 1.3, bias voltage 1 –2.8 V and bias voltage 2 1.1 V. The sampled optical signal at the output of the MZM is amplified using an optical amplifier with gain $G_{\mathrm{a}} = 6$ dB and noise figure of 4 dB, the bandwidth of the OBPF of the 1-bit PDAC is 4 nm at 1545 nm. Furthermore, the gain of $G_{\mathrm{a2}\text{-}i}$ (where $i = 2, 3, \ldots, 8$) is based on the significance of the corresponding bit. In the simulated model, $G_{\mathrm{a2}\text{-}8} = 22$ dB, $G_{\mathrm{a2}\text{-}7} = 10$ dB, $G_{\mathrm{a2}\text{-}6} = 4$ dB, $G_{\mathrm{a2}\text{-}5} = 1.8$ dB, $G_{\mathrm{a2}\text{-}4} = -2.3$ dB, $G_{\mathrm{a2}\text{-}3} = -10$ dB, and $G_{\mathrm{a2}\text{-}2} = -19$ dB.

Figure 4 shows the simulated output spectrum of the proposed 8-Bit PADC in the presence of MLLD timing jitter and optical amplifiers' amplified spontaneous emission noise, which is discussed in [29]. The performance of the 8-Bit PADC is evaluated at a 200 GHz sampling frequency for single tone RF inputs at different frequencies. As shown in figure 4(a), the amplitude of the output sampled single tone RF input at 10 GHz is about −1.7 dB and the maximum spur signal magnitude is about −44 dB, therefore, the SFDR is 42.3 dBc and the SNDR about 29.18 dB. According to this SNDR, the ENOB of the 8-bit PADC is 4.55. As shown in figure 4(b), the amplitude of the output sampled single tone RF input at 50 GHz is about −1 dB and the maximum spur signal magnitude is about −35 dB, therefore, the SFDR is 34 dBc and the SNDR about 27.94 dB. According to this SNDR, the ENOB of the 8-bit PADC is 4.34. Furthermore, for a 120 GHz single tone RF input at a 320 GHz sampling frequency, as shown in figure 4(c), the fundamental signal amplitude is −0.1 dB and the strongest spur signal magnitude is about −23.8 dB which gives a SFDR of about 23.7 dBc and a SNDR of about 18.3 dB and an ENOB of about 2.74.

Figure 5 enables the impact of two-tone inter-modulation distortion on the performance of the proposed 8-bit PADC to be assessed. It is investigated by considering two individual single tone RF signals with a very small frequency difference and examining the FFT amplitude of the inter-modulation distortion at the output of the PDAC. In this assessment, two single tones at frequencies 93 and 94 GHz are sampled at 320 GHz. The FFT amplitude of the output gives the magnitude of the fundamental signals and the harmonics distortion. The signal amplitude at 93 GHz is about −0.5 and −0.4 dB at 94 GHz, whereas the distortion spurs signal amplitude is about −17.74 dB. That shows the inter-modulation distortion (IM3) is about 17.24 dB.

To access the performance of the PADC, the ENOB of the PADC is considered for different sampling frequencies and different input RF signals. The tuning of the PADC is performed by tuning the bandwidth of the OBPF of the 1-Bit PDAC block and its amplifier gain, $G_{a2\text{-}j,}$ where $j = 1, 2, \ldots, 8$. Figure 6(a) shows the variation in the ENOB for a single tone input RF signal at different sampling frequencies (Fs). This figure demonstrates that the PADC's performance is better than for other sampling frequencies over the frequency range of interest around a sampling frequency of 360 GHz.

To demonstrate the physical functionality of the 8-bit PADC, a sample waveform is generated. Figure 7(a) shows a sample RF signal with 55 GHz fundamental frequency that is sampled with MLLD generated pulses with 200 GHz repetition rate. The MLLD pulses train is given in figure 7(b) and the sampled signal in figure 7(c).

The quantized output bits of the PADC shown in figures 8(a)–(h), respectively, correspond to Bit_8 to Bit_1 of the PADC. As shown in this figure, each sample of the optical signal of figure 7(c) is quantized into 8 bits that correspond to the time of sampling of the original signal. Therefore, corresponding to the 10 sampling times that are shown in figure 7(b), the following digitized data is generated at the output of the PADC, the first to tenth samples are quantized to '11111111', '01111111', '01111111', '11111111', '01111111', '01111111', '11111111', '00011111', '11111111' and '00011111', respectively.

The amplitude fluctuation of the digital output is related to the flatness of the OHL's transfer function for high values of frequency, [30]. Table 1 compares the performance of different reported architectures with that of the proposed PADC showing it to be much faster while providing an acceptable ENOB. Some of the source works reported the sampling frequency, whereas the others reported the analog input signal frequency. Unlike previously reported architectures the proposed architecture is fully optical in so far as the input optical signal is not converted to an electrical signal at any point in its processing, furthermore, the output of the proposed architecture is binary with no need to post process in the electronic domain.

5. Conclusions

In this paper, the feasibility of implementing concept architecture for a fully photonic pipelined ADC (PADC) has been analyzed and evaluated to provide a design for an 8-bit PADC, which is fully optical in both signal sampling and quantization, the output of which is binary with no need for post processing in the electronic domain.

The system simulation results show the proposed PADC's performance over a sampling frequency bandwidth of about 90 GHz. For a sampling frequency of around 400 GHz, the ENOB is approximately flat for an RF input of 78 GHz, the performance in terms of the ENOB provided at a 200 GHz sampling frequency is about 4.34 bits. Based on the ongoing development in photonic integrated circuit technology, the proposed architecture could be a suitable and cost-effective candidate for a high performance PADC for applications such as radio over fiber in the near future. The main barriers to the implementation of this scheme are the implementation of a suitable OHL and optical mathematical components such as subtractors and adders, architectures for which have been proposed [28, 30].

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