An Investigation of the Switched-Capacitor Circuit as a Solid-State Fault Current Limiting and Interrupting Device (FCLID) with Power Factor Correction Suitable for Low-Voltage Distribution Networks

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***Abstract*— The Switched Capacitor (SC) Circuit is investigated in this paper as a Solid-State Fault Current Limiter and interrupting device (FCLID) with power factor correction suitable for low-voltage distribution networks. It was applied so far successfully as a power factor and harmonic current compensator and as a Switched Capacitor Circuit inverter. In this application it is inserted in series with the supply line, providing both power factor correction and limitation of the current to a pre-set value in the event of a fault. Interruption of the fault is also possible by setting both semiconductor switches in the off state. Overvoltage is present in SC Circuits and they appear across both the passive and active components. The problem can be alleviated by optimising the system operation and system components.**

***Index Terms*— Switched Capacitor, Duty Cycle, Power factor, Current limiter, Distribution network**

I. INTRODUCTION

Fault current limiting and interrupting can only be achieved by inserting a device in series with the line [1]. In this way the level of the fault current is limited to a safe value for the circuit breakers to perform the interruption. Thus the rating of the transformers, circuit breaker s (CBs), buses and other electric equipment at fault current is lower.

Solid State switches are used together with reactors [2]. LC tuned circuits [3] in Fault Current Limiters. An isolating transformer [4]-[5] option providing flexibility in the choice of the VI ratings of the components used is also an option, Fig. 4.

The impedance of the Switched Capacitor (SC) Circuit can be set either inductive or capacitive at any value by setting the duty cycle of the semiconductor switches, Fig. 2. In the past it was employed for power factor correction [6] and for harmonic current compensation [7].

In this application, the Switched Capacitor circuit offers the capacitive series impedance during normal operation in order to either make the power factor unity or just improve it. The fact that the power factor correction takes place in series Fig. 3, gives rise to the load voltage, Fig. 5. During a fault the impedance of the SC capacitor circuit can be set at any value in order to limit the current to a safe and predetermined value.

Compensation of the power factor is done by adjusting the impedance of the SC Circuit to match the impedance of the load. Specifically since most of the loads are inductive, the reactance of the SC circuit is set capacitive at a value to set the power factor at any value including unity.

The entire load current flows through the passive and any active components of the Fault Current Limiter. In the case of the SC Circuit, the full load current flows through the semiconductor switches, the capacitor and the inductor giving rise to a high voltage across the capacitor and losses. The various results for all cases were obtained through PSIM simulations.

II. THE SWITCHED CAPACITOR CIRCUIT AS A CURRENT LIMITER AND POWER FACTOR COMPENSATOR

A. *The switched capacitor circuit*

The semiconductor switches in a switched capacitor circuit are working in antiparallel Fig. 1. The current is diverted from S_2 to S_1 and through the capacitor. In this way the total impedance of the switched capacitor circuit can be set either zero, capacitive or inductive and anything in between by setting the duty cycle of the switch S_1, Fig. 2.

The impedance of the circuit as a function of the duty cycle of the semiconductor switch S_1 is derived according to [6] and [8] as

$$Z(K_o) = \sqrt{r^2 + \left(\omega L - \frac{K_o^2}{\omega C}\right)^2} \qquad (1)$$

Where K_o is the duty cycle of S_1, r represents the ohmic resistance of the passive components and semiconductor switches, ω is the mains frequency, L and C are the values of the inductor and the capacitor in Fig. 1.

The impedance Z of Fig. 1, is set according to (1) by the values of L, C and K_o. For L = 0.05 and H =40μF, it is inductive for values of K_o less than 0.444 and capacitive for values

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of K_o above 0.444 as shown in Fig. 2. Resonance is also possible at K_o = 0.444 where the impedance of the circuit is reduced to the small ohmic resistance *r*.

An obvious application of this circuit is as a power factor compensator [6].

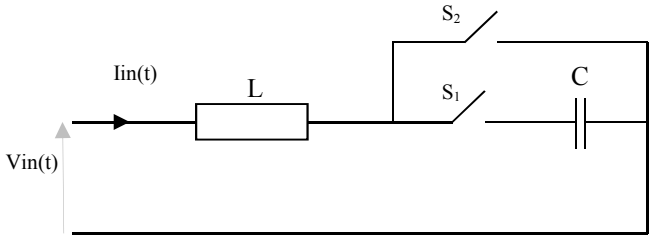

Fig.1. The switched Capacitor circuit.

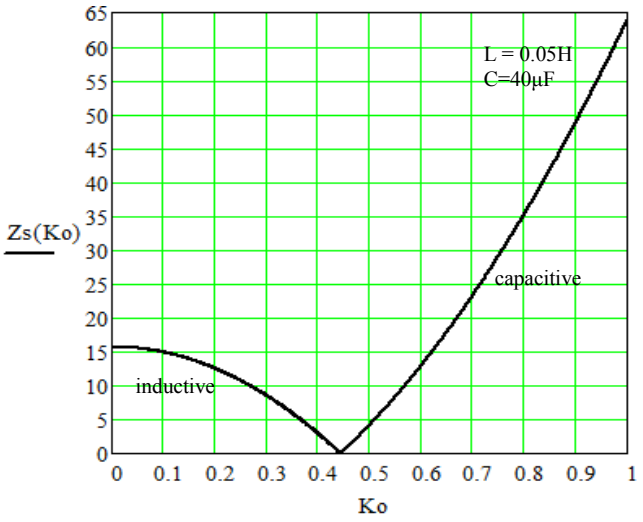

Fig. 2. Impedance of the switched capacitor circuit against K_o, the duty cycle of the switch S_1.

B. The switched capacitor circuit as a current limiter and power factor compensator

In this application the switched capacitor circuit is inserted in series with the load Fig. 3, providing power factor correction and in the event of a fault it limits the current to a preset value. Interruption of the fault is also possible by setting both semiconductor switches S_1, S_2 in the off state. An isolating transformer [5]-[7] option providing flexibility in the choice of the VI ratings of the components used is also an option, Fig. 4.

The load consists of a 4Ω resistor and 0.01H giving a load power factor of 0.786 and a line current of 56A. The SC Circuit inductance and capacitance are set in the first instance at 0.05H and the capacitor is 40μF. Later on, another set of L and C values is employed in order to control the voltage across the capacitor and the switches.

In normal operation the SC circuit is acting as a power factor corrector. The inductive impedance of the load is matched to the impedance of the SC circuit by choosing the appropriate value of the duty cycle K_o.

Specifically, the load reactance is 3.142Ω. In order to make the power factor unity the SC circuit must provide 3.142Ω capacitive reactance. This is done by setting the duty cycle of the switch S_1 in Fig. 3, to 0.4867 according to (1). Alternatively it can be read from Fig. 2. The general vector diagram is shown in Fig. 5. Fig. 6a, displays the current uncompensated at a power factor of 0.786 and in Fig. 6b, compensated at unity power factor. As expected the voltage across the load will rise with the power factor correction.

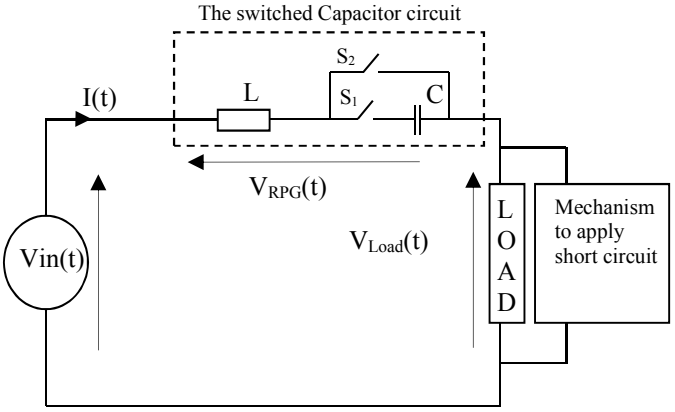

Fig. 3. The power circuit of the SC current limiter and power factor compensator.

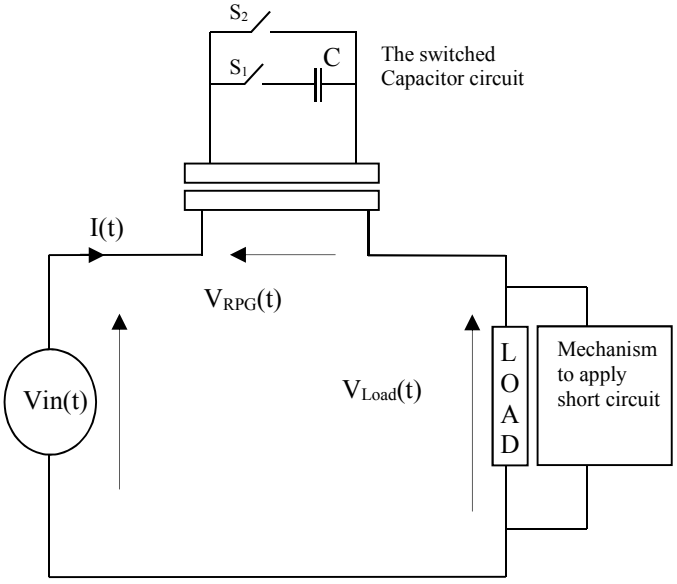

Fig. 4. The power circuit of the SC current limiter and power factor compensator with isolating transformer.

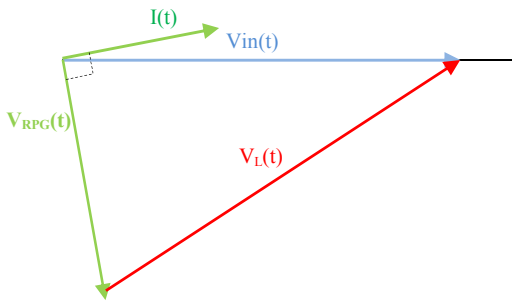

Fig. 5. Vector diagram for setting the power factor.

In the event of a fault there is the impedance of the SC Circuit of 3.142Ω (Case A) to limit the current, Fig. 7a. As shown at the beginning of the fault (t =1s) the current increases from 50A to 125A but it decays quickly to 45A in less than a second. The final value of the current will be set by the SC Circuit 3.142Ω impedance. The presence of the fault can be sensed by observing the frequency spectrum of the fault current, Fig. 7b. A strong 59Hz harmonic appears during the fault.

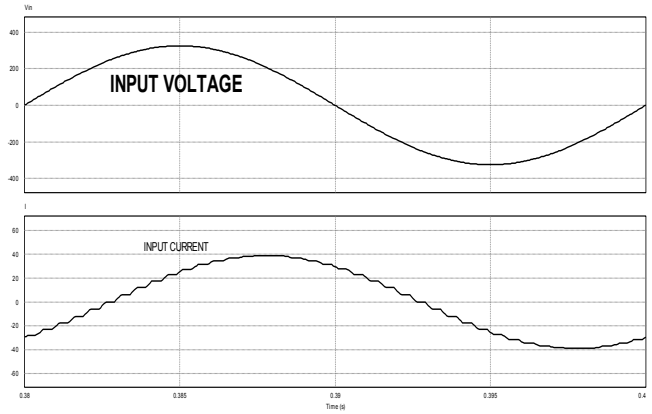

Fig. 6a. The line current uncompensated pf=0.623.

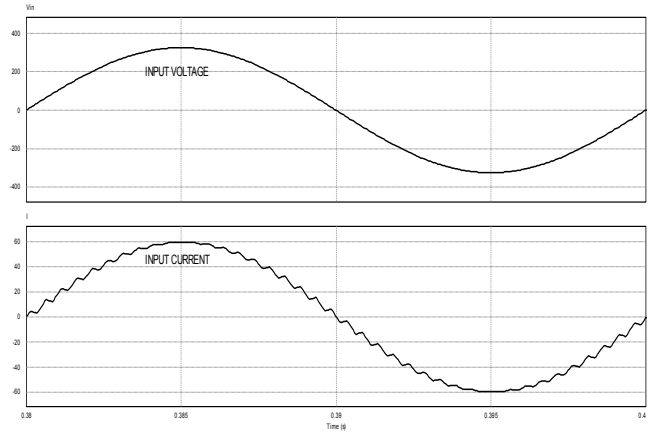

Fig. 6b. The line current compensated pf= 1.

The reaction of the circuit to a fault is tested further by inserting the full capacitive reactance of the SC Circuit (Case B) one cycle after the occurrence of the fault. This is the reactance of the 40μF capacitor, 79.6Ω. Fig. 8a, displays the current before and during the fault with its maximum value rising to 118A. The insertion of the 79.6Ω reactance is achieved by setting the duty cycle K_o of the semiconductor switch S_1 to one as dictated from (1) and Fig. 2. The fault current eventually decays to a value dictated by the 79.6Ω reactance i.e. 4A. A strong presence of a 112Hz harmonic Fig. 8b, is observed during the fault.

Finally the circuit is tested by inserting the full inductive reactance 22Ω of the circuit (Case C) one cycle after the occurrence of the fault, Fig. 9a. It is raising the current to 142A with a strong decaying dc component, Fig. 9b. The fault current eventually decays to a value dictated by the 22Ω reactance i.e. 14.8A. The insertion of the 22Ω reactance is accommodated by setting the duty cycle of the switch K_o to zero as dictated by (1).

Furthermore, interruption of the fault is possible at any point by switching off both switches S_1, S_2. Of course the fault current can be set to any value by adjusting K_o accordingly.

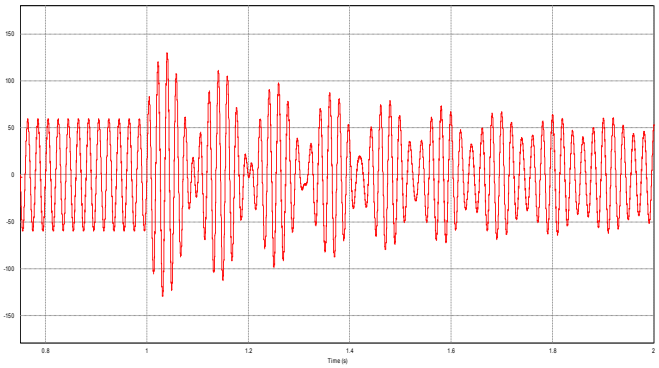

Fig. 7a. Current during fault conditions Case A: No action. L = 0.05 C = 40μF

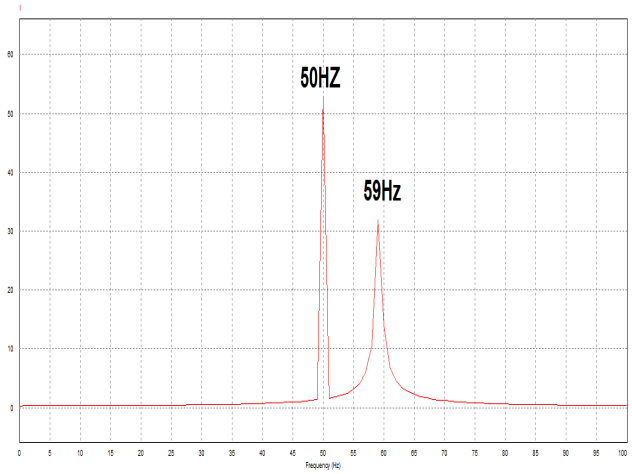

Fig. 7b. Frequency Spectrum of the current during fault conditions Case A: No action. L = 0.05 C = 40μF

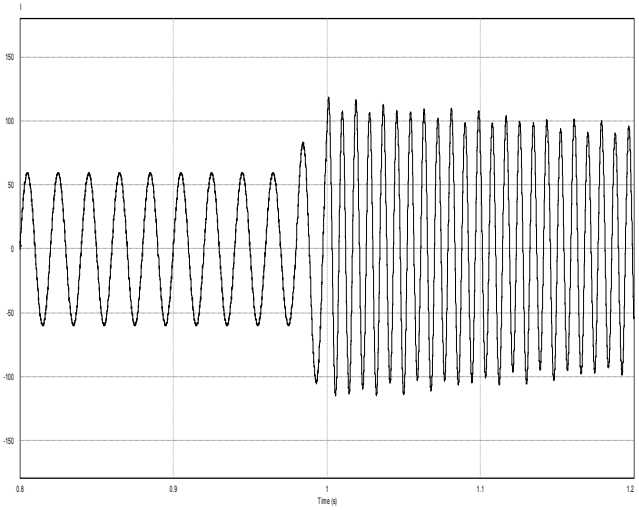

Fig. 8a. The current during fault conditions Case B: Maximum impedance-capacitive. L = 0.05 C = 40μF

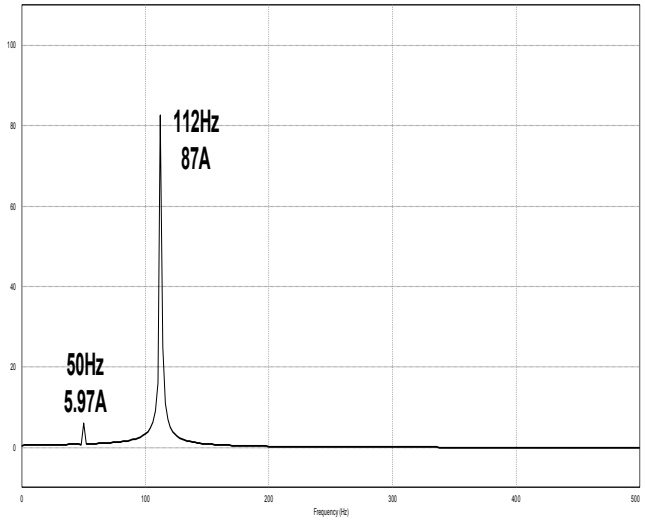

Fig. 8b. Frequency Spectrum of the current during fault conditions Case B: Maximum impedance-capacitive. L = 0.05 C = 40μF

C. Ratings of components of the switched capacitor and optimization.

The SC circuit is characterized by overvoltage phenomena across both the passive and active components, Fig. 10. The voltage across the capacitor and hence the semiconductor switches is easily derived for the fundamental component by considering the current entering the switched capacitor as the ratio of the supply voltage V to the impedance and the fact that the current (2) entering the capacitor is determined by the duty cycle K_o of S_1 [8]. Hence the voltage across the capacitor and the switches is given by (3)

The current entering the capacitor is

$$I_C(t) = \frac{V}{\sqrt{r^2 + \left(\omega L - \frac{K_o^{\,2}}{\omega C}\right)^2}} K_o \qquad (2)$$

The voltage across the capacitor is

$$V_C(t) = \frac{V}{\sqrt{r^2 + \left(\omega L - \frac{K_o^{\,2}}{\omega C}\right)^2}} K_o \frac{1}{\omega C} \qquad (3)$$

During normal operation when the SC Circuit is performing only power factor correction the voltage across the capacitor and hence the semiconductor switches can be much higher than the supply voltage, Fig. 10. This is basically determined by the L/C ratio. As shown in Fig. 10, there is a dramatic reduction of this voltage for lower ratios. For a 56A load and power factor at 0.786, if unity pf correction is needed, utilizing high L/C ratio where, L=0.05H and C=40μF, the voltage across the capacitor is raised to 2920V given by (3), a voltage which is very high. This is decreased to 686V by a lower L/C ratio where, L = 0.005H and C=200μF. The voltage across the capacitor and switches can be reduced further if a power factor less than unity is acceptable, Fig. 5. The capacitor voltage can be reduced by 30% and still retain a pf of 0.9 leading.

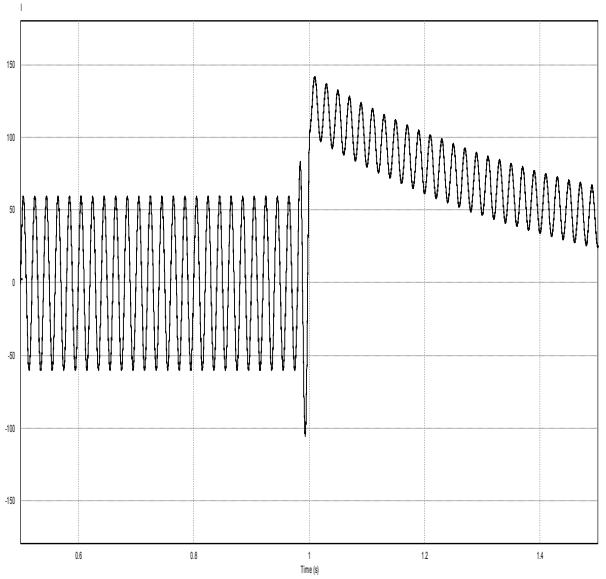

Fig. 9a. The current during fault conditions Case C: Maximum impedance-inductive. L = 0.05 C = 40μF

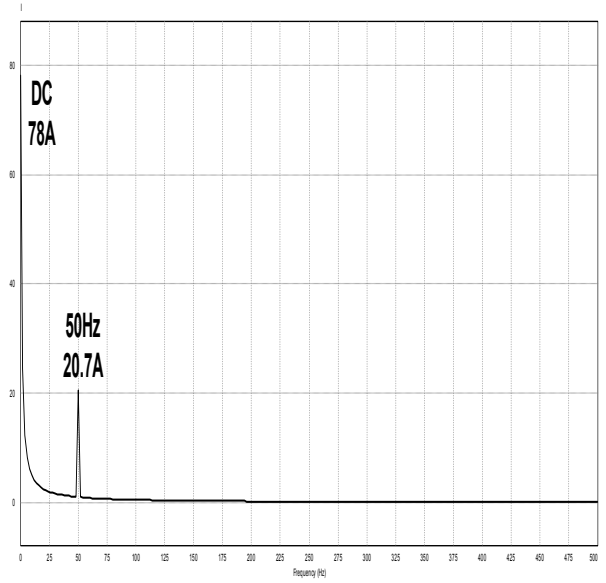

Fig. 9b. Frequency Spectrum of the current during fault conditions Case C: Maximum impedance-inductive. L = 0.05 C = 40μF

From the load side, the output voltage is increased because the power factor is compensated in series, Fig. 5. Specifically, with the high ratio of LC (L = 0.05H C=40μF) the output voltage is raised to 274V but reduced to 248V by setting the lower L/C ratio with power factor of 0.9 leading. Therefore with proper optimisation the output voltage is expected to be within acceptable limits. Under these conditions with leading power factor the SC Circuit is also providing leading KVA to the grid. Further optimization is possible.

More options to the designer are offered by employing the circuit of Fig. 4, where a transformer is used to connect the SC circuit to the network. The leakage inductance of the transformer can be utilized to replace the inductor L in the power circuit of Fig. 3. Its turn ratio can be arranged to accommodate the voltage ratings of the capacitor and the semiconductor switches.

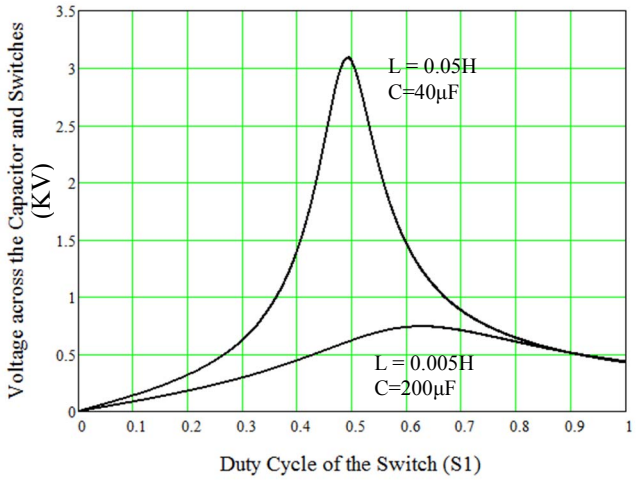

Fig. 10. Voltage across the capacitor (KV) as a function of K_o.

III. DISCUSSION

The SC Circuit is employed in a new application to correct both the pf and at the same time it is a solid-state fault current limiting and interrupting device (FCLID) for low voltage distribution networks. The SC circuit is inserted in series with the power line and its current limiting ability lies in the fact that its impedance is smoothly controlled by the duty cycle of its switches, K_o. For power factor correction the reactive impedance of the load is compensated by the impedance of the SC circuit.

The ability of the circuit to control the fault lies in the fact that there is always the reactive impedance of the SC Circuit in series with the line at the connection point. While this circuit can be used in low-voltage (LV) systems as well, at this stage no consideration has been taken to costs.

Since, this limiter is not in practical use yet the circuit is tested through PSIM simulation under three conditions. In the first case in the event of the fault no action is taken and the current first rises from 50A to 125A and quickly decays to 45A within one second. In the second case the full impedance of the SC circuit 79.6Ω is inserted with the current first rising from 50A to 118A and quickly decays towards 4A. In a final test the full inductive 22Ω reactance of the SC circuit is inserted and the current first rises from 50A to 142A and quickly decays towards 14.8A. In all three cases the value of the duty cycle K_o of the switch S_1 is set accordingly. Actually the series impedance of the SC circuit can be set to any value in order to keep the current with any preset limits value by selecting the appropriate value of K_o. The presence of a fault can be detected from the strong 59Hz harmonic in the fault current. Of course the frequency and magnitude of the harmonic depends on the values of LC.

A drawback of this preposition is the fact that both the semiconductor switch and the capacitor can be subjected to a voltage higher than the supply. It was shown though that this becomes manageable by selecting a lower L/C ratio and further reduction is possible by adopting a lower but leading power factor than unity. Further optimization is possible by employing a transformer to connect SC to the line.

Another disadvantage is the increase of the load voltage when the SC is performing power factor correction. It might be an advantage in areas where the grid voltage is low but this does not happen always. Adopting a leading power factor less than unity (0.9) can reduce it by 35%.

The switching frequency of the semiconductor switches S_1 and S_2 sets the voltage harmonics across the load. For this reason the switching frequency must be optimized with the size of the passive filter against the switching losses.

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