A New Switched DC –Link Capacitor Based Multilevel Converter (SDC^{2}MLC)

Abstract

At present, one of the most common techniques for high power conversion in medium voltage applications is the use of cascaded multilevel converters. In this article, a new Switched DC-Link Capacitor Multilevel converter (SDC^{2}MLC) with considerably few numbers of power electronics switches (IGBTs) is proposed, where keeping the total harmonic distortion (THD) of the output voltage waveforms as low as possible is desired. The proposed topology is configured using two separate basic units. Each unit consists of four switches with a series-parallel combination of isolated DC sources. The performance of the presented topology for both configurations is described. The required number of switches, power diodes, gate driver circuits and voltage stresses across the switches are compared with those of other recent published techniques. Furthermore, operation and performance of the proposed SDC^{2}MLC are illustrated with the aid of experimental results of a single-phase 11-level converter to clarify the viability of the proposed topology.

Keywords: Harmonic distortion, multilevel converters, power quality, power switches, symmetric and asymmetric design.

I. Introduction

One of the high-power conversion devices that are widely used in medium voltage applications is the cascaded multilevel converters, because of their low switching frequency, low electromagnetic emissions; thus, complying with Electromagnetic Interference standards, low *dv/dt* stress, and low total harmonic distortion (THD) of the output voltage without the need of a high rating passive LC filter [1]-[2]. The conventional multilevel converter topologies using medium-voltage devices are the Neutral- Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) topologies [3]. The NPC and FC converters can be scaled up to produce a high number of levels by partitioning the DC link voltage using some capacitors. However, voltage balancing circuits are necessary for this kind of multilevel converters. On the other side, CHB converters require more isolated DC sources to generate multiple stepped output voltage waveforms. These isolated DC sources can be fed from a multi-winding transformer or a photovoltaic (PV) panel. Accordingly, this kind of

converters suffers from the high additional cost [4]. Practically, these topologies are successfully implemented for various power ranges in megawatts [5]. However, these topologies suffered from the use of a vast number of power electronic components such as clamped diodes, clamped capacitors and power switches (IGBTs), which increase the complexity of the modulation techniques, beside the concern for the increased number of gates-driver circuits, and large installation areas that may be needed with additional supporting components. Unfortunately, the high cost of these topologies has been sensed in the power electronic based markets, delaying their widespread deployment in a broad sense. Consequentially, the development of new cascaded multilevel topologies is necessary, and the issues of higher power quality that should meet the grid code specifications, with reduced complexity, and lower cost are vital necessities that should be addressed.

In the literature, solutions that consider balancing of the DC capacitor voltages is widely presented [6]-[11], reducing complexity of the modulation techniques by the development of novel control methods is introduced [12]-[15], and some modulation techniques that enhance the voltage quality with reduced number of components, are presented in [16]-[20]. Additionally, many novel multilevel converter topologies are recently presented [21]-[27]. Despite the valuable development added by such novel algorithms, they are mainly composed of two units: (i) multi-stepped DC/DC converter (a switch reduction unit), and (ii) full-bridge converter unit (multi-stepped DC/AC). However, switches of the full-bridge converter unit should endure the sum of all the DC source voltages that are presented in the switch reduction unit. Accordingly, high voltage rating switches with complex high-voltage protection circuits are needed, which will reflect on the multilevel converter investment cost. This is a remarkable disadvantage of this type of converters. In [28], a series connection of a new basic unit is introduced, including various algorithms to find the proper magnitudes of the DC source voltages, for both symmetric and asymmetric design methods. Fig. 1(a) demonstrates the construction of this basic unit with the aid of unidirectional switches. In [29], another topology that has separate basic units for symmetric and asymmetric methods is presented. Each unit consists of two isolated DC sources and a series-parallel connection of unidirectional switches, as shown in Fig. 1(b). Both symmetric and asymmetric methods include cascaded basic units which generate a high number of levels of voltage with reduced number of switches. The combination of both unidirectional and bidirectional switches based sub-

multilevel converter is presented in [30]. The bidirectional switches are configured with two series connected switches. The main advantage of bidirectional switches is the need of one driver circuit for the two switches with a high reverse blocking voltage capability. Furthermore, this topology is presented for both symmetric and asymmetric methods and can easily be optimized for different goals. However, all the former topologies are configured with connections to single full bridge converters and use isolated DC sources. However, there are other topologies recently introduced without using a full bridge converter presented in [31] - [36].

II. Structure of the Basic Unit

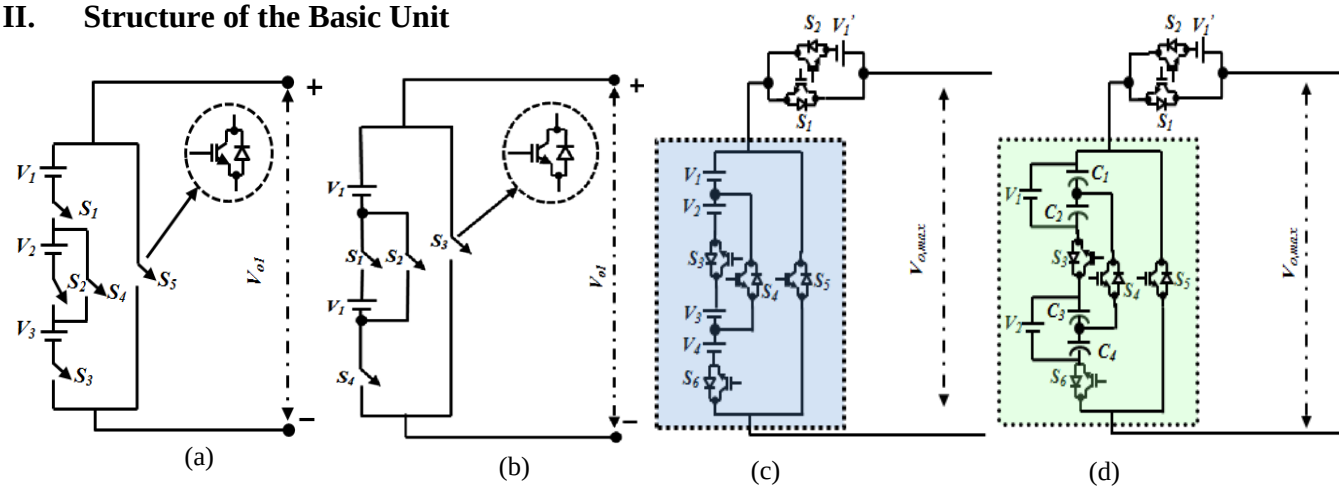


Fig. 1. Different basic unit structures (a) The structure presented in [28], (b) The structure presented in [29], (c) The proposed basic unit configurations using 4 isolated DC sources and (d) Using 2 isolated DC sources with capacitors.

In this work, a proposed multilevel converter topology with reduced number of IGBTs is presented, where maintaining the THD of the output voltage waveforms as low as possible to comply with the typical requirements of the conventional multilevel converter, is desired. The proposed topology has different basic unit configurations. Various algorithms to find the magnitudes of the DC source voltages are presented. Terms describe the numbers of levels (N_{Level}), driver circuits (N_{Driver}), sources (N_{Source}), variety of sources ($N_{Variety}$), switches (N_{Switch}), and the total standing voltage of switches (V_{TSV}) are used for the comparisons purpose between the suggested topology and other recently published topologies. Moreover, operation and performance of the proposed SDC^{2}MLC are illustrated with the aid of experimental results of a single-phase 11-level converter to clarify the viability of the proposed topology.

III. The Proposed Topology

Fig. 1 demonstrates the structure of the presented basic unit configurations. The first unit configuration illustrated in Fig. 1(c), uses four isolated DC voltage sources. The second one which is illustrated in Fig. 1(d) uses two separate DC voltage sources that are divided by two DC-link capacitors, respectively. As obvious, the first configuration has an advantage of the absence of any DC link capacitor balancing circuits, which may decrease the total cost. However, compared to the second configuration, more isolated DC sources are used. Accordingly, the second configuration is more suitable for the applications using renewable resources.

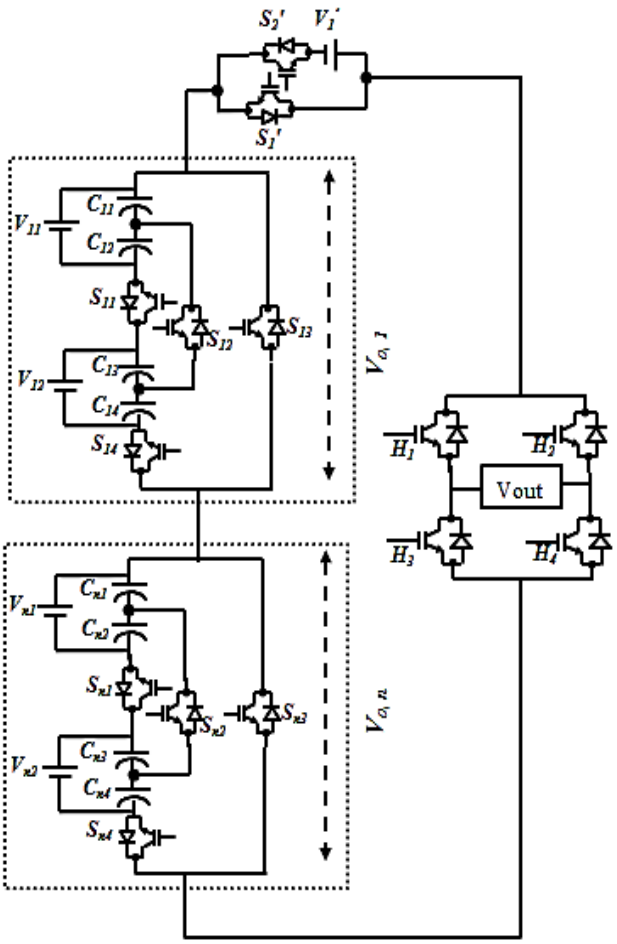


Fig. 2. A generalized structure of the new cascaded multilevel converter

Regarding the proposed structure and number of electronic components, a brief comparison between the basic units presented in [28], [29] and the proposed basic unit configurations are clarified in **Table 1**. It is obvious that required number of switches, driver circuits, isolated DC sources, and the total standing voltage (voltage stresses across the switches) are different from such structures. From the overall standing voltage

viewpoint, a higher standing voltage of the proposed basic unit configurations might be observed compared to the corresponding values of [28] and [29]. However, for the proposed topology, it should be mentioned that for a higher number of levels, the total standing voltage values will decrease. More details about this point will be illustrated in the next section.

TABLE 1 Comparison between the new proposed basic unit configurations and the basic unit configurations presented in [28], [29]

Description	Presented in [28]	Presented in [29]	Proposed (a)	Proposed (b)
Number of main switches	5	4	4	4
Number of anti-parallel diodes	5	4	4	4
Number of gates-driver circuits	5	4	4	4
Number of isolated DC sources	3	2	4	2
Total standing voltage	8 V_{DC}	6.5 V_{DC}	10 V_{DC}	10 V_{DC}

The maximum possible value of the output voltage ($V_{o,max}$) and the corresponding switching patterns of the suggested basic unit for both configurations are shown in **Table 2**. They are common for both configurations.

TABLE 2 Switching patterns of the proposed basic unit

Number	Switches				Voltage level
	S_1	S_2	S_3	S_4	$V_{o,\,max}$
0	0	0	1	0	0
1	0	1	0	1	V_1+V_4
2	1	0	0	1	$V_1+V_2+V_3+V_4$

The switches S_1 and S_2 are turned on to get the output voltage (V_1+V_4), S_1 and S_4 are turned on to get the maximum output value of voltage which is the sum of ($V_1+V_2+V_3+V_4$). S_3 is turned on to bypass the DC sources presented in the basic unit. It should be mentioned that the switches (S_1, S_2, S_3) and (S_3, S_4) are parallel switches; thus, they must not be turned on at the same time to keep away from short-circuiting of the DC sources. The switches S_1, S_2, S_3, and S_4 generate even output voltage levels ($2V_{DC}$, $4V_{DC}$…). Moreover, producing odd output voltage levels ($3V_{DC}$, $5V_{DC}$…) might be achieved using a series connection of the single-source unit presented in [37] and the proposed basic unit, as illustrated in Fig. 2. However, this arrangement

may suffer from additional costs because of the high voltage rating switches of the full bridge converter as mentioned before. Numbers of DC voltage sources (N_{Source}), capacitors ($N_{Capacitor}$), switches (N_{Switch}), and the maximum magnitude of the generated output voltages ($V_{o,\ max}$) can be calculated for the circuit configuration shown in Fig. 2, respectively, as follows:

For the first circuit configuration (shown in Fig. 1 (c)):

$$N_{Source} = 4n + 1 \qquad (1)$$

where *n* represents the number of series connected basic units.

For the second circuit configuration (shown in Fig. 1 (d)):

$$N_{Source} = 2n + 1 \qquad (2)$$
$$N_{Capacitor} = 4n \qquad (3)$$

On the other side, the numbers of main switches and a maximum magnitude of the generated output voltages are equal for both configurations. They could be given, respectively, as follows:

$$N_{Switch} = 4n + 6 \qquad (4)$$
$$V_{o,max} = v'_{o,1} + v_{o,1} + v_{o,2} + ...v_{o,n} \qquad (5)$$

Each basic unit generates the maximum magnitude of the output voltage ($v_{o,\ 1}$, $v_{o,\ 2}\ldots\ v_{o,\ n}$), and the single source unit generates $v'_{o,1}$. So that;

$$v'_{o,1} = v'_1, v_{o,1} = v_{11} + v_{12} + v_{13} + v_{14},$$
$$v_{o,n} = v_{n1} + v_{n2} + v_{n3} + +v_{n4}.$$

The generated output voltage levels of the presented topology are based on the on-off states of the different switching combinations. Accordingly, a generalized switching pattern of the cascaded multilevel converter is given in Table 3. For simplicity, only the on-state switches are presented. Recalling Fig. 2, the full-bridge converter switches (H_1, H_4) and (H_2, H_3) should be turned on and off, alternatively, in order to produce either

positive or negative output voltage levels at the load side (V_L) and allow the flow of current in both directions. So that;

$$V_L = \pm V_{o,max} \quad (6)$$

Recalling [28], the maximum blocking voltage or the standing voltage by the power switches is an important factor that affects the total cost of the converter. For the switches' current rating the case is different since the required current rating of each switch is equal and depends on the load value.

TABLE 3 A generalized switching pattern of the proposed cascaded multilevel converter

State	On-states switches						$V_{o,\,max}$
0	S_1'	S_{13}	-	-	$S_{n-1,3}$	S_{n3}	0
1	S_2'	S_{13}	S_{23}	…..	$S_{n-1,3}$	S_{n3}	V_1'
2	S_1'	S_{14}	S_{12}	…..	$S_{n-1,3}$	S_{n3}	$V_{11} + V_{14}$
3	S_2'	S_{14}	S_{12}	…..	$S_{n-1,3}$	S_{n3}	$V_{11} + V_{14} + V_1$'
4	S_1'	S_{11}	S_{14}	…..	$S_{n-1,3}$	S_{n3}	$V_{11} + V_{12} + V_{13} + V_{14}$
5	S_2'	S_{11}	S_{14}	…..	$S_{n-1,3}$	S_{n3}	$V_{11}+V_{12}+V_{13}+V_{14}+V_1$'
…..	…..	…..	…..	…..	…..	…..	…..
*(n-1)*th	S_1'	S_{11}	S_{14}	…..	S_{n4}	S_{n1}	$\sum_{j=1}^{4} V_{1j}+V_{2j}+...V_{nj}$
*n*th	S_2'	S_{11}	S_{14}	…..	S_{n4}	S_{n1}	$V_1'+\sum_{j=1}^{4} V_{1j}+V_{2j}+...V_{nj}$

However, the voltage rating of the switches varies according to the total standing voltage of the power switches. According to Fig. 2, the standing voltage of each switch for the *n*th unit is calculated as follows;

$$V_{Sn1} = V_{Sn2} = V_{n2} + V_{n3} \quad (7)$$
$$V_{Sn4} = V_{n4} + V_{n3} \quad (8)$$
$$V_{Sn3} = V_{n1} + V_{n2} + V_{n3} + V_{n4} \quad (9)$$

where V_{Snj} (j=1, 2.. 4) is the blocked voltage by the switch S_j.

Additionally, the standing voltage of the single-source unit and the full bridge are given as;

$$V_{S1}^{'} = V_{S2}^{'} = V_1^{'} \quad (10)$$
$$V_{H1} = V_{H2} = V_{H3} = V_{H4} = V_{o,max} \quad (11)$$

Thus, the total standing voltage (V_{TS}) across the switches in the single-source unit, the n^{th} basic unit and the full bridge unit can be given as follows:

$$V_{TS} = V_{S1}' + V_{S2}' + \left\{ \sum_{j=1}^{4} V_{S1j} + V_{S2j} ..... + V_{Snj} \right\} + V_H \qquad (12)$$

Since the standing voltage of the full bridge converter is always higher than the standing voltage of the basic unit switches; thus they will need an extra protection circuit (snubber-circuit) in addition to special cooling arrangements. Accordingly, the total cost of the multilevel converter will increase. This may limit usage of the suggested topology in high voltage applications. **Table 4** shows four algorithms to select the DC source voltages regarding generation of all voltage levels and operation for both symmetric and asymmetric methods. Asymmetric methods produce the maximum output voltage level compared to the symmetric one using an equal number of DC sources and switches. However, the variety of magnitudes of the DC sources will considerably increase. The isolated DC sources are used as inputs for the converter. They can be provided through a multi-winding transformer integrated with rectifier circuits or renewable energy resources such as photovoltaic and fuel cells, or energy storage elements such as batteries.

IV. Comparison with Recent Topologies

A detailed comparison of the SDC^{2}MLC with other current topologies is provided taking into account the required number of power switches, DC sources, gates driver circuits, output levels, and the total standing voltage of the multilevel converters. In these aspects of assessment, V_{DC} was assumed to be the base value. Seeking a clear demonstration of the proposed topology; the following algorithms are compared with the proposed algorithms (P_1–P_4) that are clarified in **Table 4**.

(i) The algorithm of the conventional asymmetric cascaded multilevel converter CHB (trinary) that was presented in [38], [39].

(ii) The four algorithms that have been presented in [28], they will be indicated in the comparison as R_{11}–R_{14}, respectively.

(iii) In [29], a different topology of an advanced cascaded multilevel converter with various structures for the symmetric and asymmetric methods was presented. Hence, the two algorithms that have been shown there will be compared to the previous algorithms; they will be indicated in the comparison as R_{21}–R_{22}, respectively. Readers could refer to [28] and [29] for more details about these different algorithms. Fig. 3(a) demonstrates a comparison of the various topologies versus the suggested topologies for different voltage level and the number of switches. It is evident that the proposed topology requires a lower number of switches to produce the maximum output voltage levels compared to the other topologies. Additionally, it should be noted that the fourth algorithm (P_4) has the best performance, as it achieves the maximum output voltage levels with a low number of switches (or anti-parallel diodes) compared to the other algorithms. Since the modern switches are often integrated with anti-parallel connected diodes in their fabrication, the number of power switches is equal to the number of power diodes. Hence, a reduction in the number of the power switches means a reduction of the number of the diodes. Regarding the symmetric algorithm, Fig. 3(b) demonstrates a comparison of the number of output levels versus variation of the number of the power switches for the proposed and conventional topologies. The magnitudes of the DC source voltages of the basic units are considered as equal (V_{DC}). It is notable the reduction of the total number of the switches in the proposed topology compared to the conventional CHB and other topologies. Since all the presented topologies use unidirectional power switches, therefore, each switch will need an individual gate driver circuit. Also, the converters that use a low number of gate driver circuits are considerably more reliable.

TABLE 4 Magnitudes of the DC source voltages for the proposed cascaded multilevel converter

Algorithm (P)	Determination of the DC source voltage values	N_{Level}	$V_{o,\,max}$	$N_{Variety}$	V_{TS}
P_1	$V_1' = V_{DC}$ $V_{1j} = V_{2j} = \cdots = V_{nj} = V_{DC}$	$8n+3$	$(4n+1)\,V_{DC}$	1	$(26n+6)\,V_{DC}$
P_2	$V_1' = V_{1j} = V_{DC}$ $V_{2j} = 2\,V_{DC}$ $\vdots$ $V_{nj} = 2^{i-1}\,V_{DC}$, i = 1, 2⋯n	$2^{n+3}-5$	$\left(4*(2^n-1)+1\right)V_{DC}$	n	$\left(26*(2^n\text{-}1)+6\right)\,V_{DC}$
P_3	$V_1' = V_{1j} = V_{DC}$ $V_{2j} = \cdots = V_{nj} = 2\,V_{DC}$	16*n-5	$(8n\text{-}3)\,V_{DC}$	2	$(26*(2n\text{-}1)+6)\,V_{DC}$
P_4	$V_1' = V_{1j} = V_{DC}$ $V_{2j} = 3\,V_{DC}$ $\vdots$ $V_{nj} = 3^{i-1}\,V_{DC}$, i = 1, 2⋯n	$(4*3^n)\text{-}1$	$\left((2*3^n)-1\right)V_{DC}$	n	$\left[26*\left[\sum_{k=1}^{n}3^{k-1}\right]+6\right]V_{DC}$, k = 1, 2...n

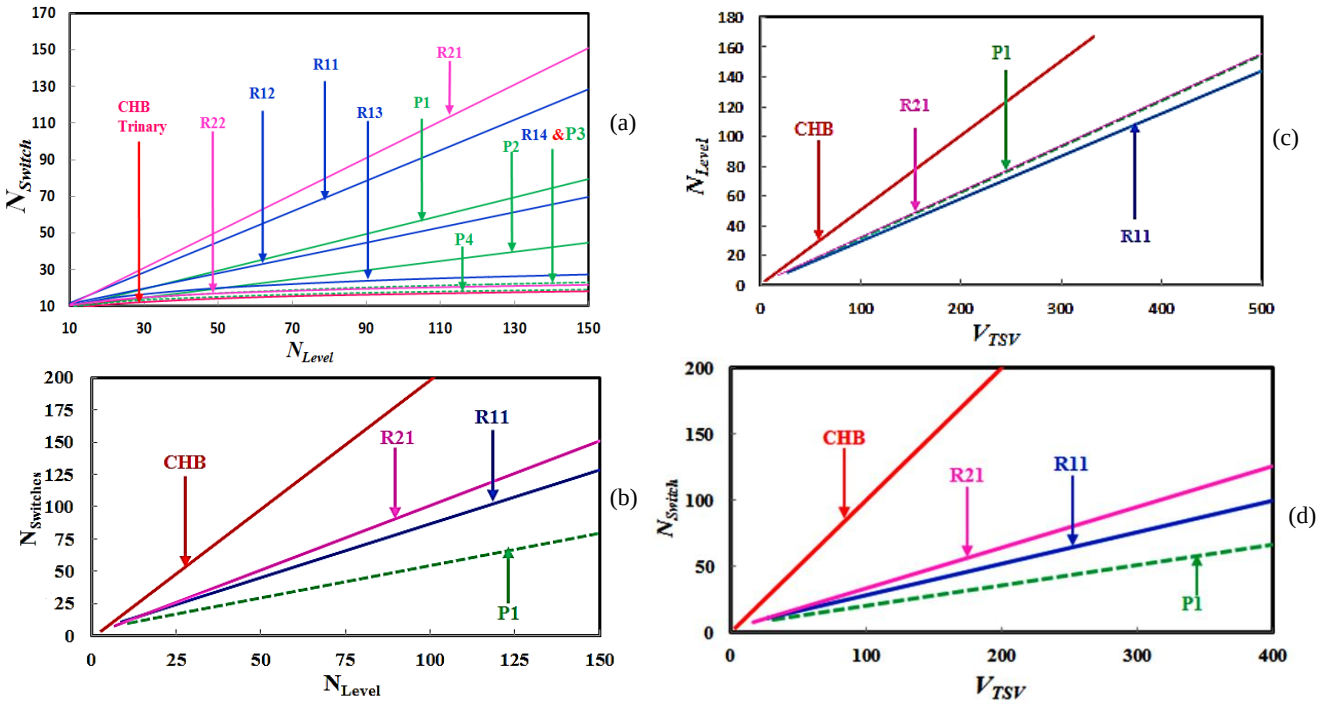


Fig. 3. Comparison of the number of levels versus the number of switches and the total standing voltage of the proposed and other topologies (a) The four algorithms presented in the proposed topology and the configurations introduced in [28], [29] and the conventional CHB Trinary configuration, (b) Symmetric N_{Level} versus $N_{Switches,}$ (c) N_{Level} versus V_{TSV} and (d) N_{Switch} versus $V_{TSV.}$

Recalling that the proposed topology utilizes a low number of switches, accordingly, the proposed topology will use a low number of gate driver circuits compared to the other topologies. However, the conventional CHB symmetric configuration practices lower value of the total blocking voltage relative to the SDC^{2}MLI topology and the other topologies. From another point of view, reduced number of the switches may lead to an increase of the standing voltage of the individual switches as given in Fig. 3(c). As presented in [40], the cascaded connection of the SDC^{2}MLI topology may reduce the blocking voltage of the full bridge switches and increase the number of levels using a lower number of switches. On the other hand, a high total standing voltage of the proposed basic unit was noticeable in Table 1 compared to the other units. Accordingly, Figs. 3(c) and 3(d) show the variation of the required number of switches and the number of levels versus the total standing voltage for the proposed and the conventional multilevel converter topologies, respectively. It is noticed that the total standing voltage of the cascaded multilevel converter based on the proposed basic unit, for the structure given in Fig. 2, is lower than the corresponding values of the other converters. Additionally, for a given value of the total standing voltage; the planned configuration guarantees a higher output voltage level with a lower number of switches compared to the other topologies.

Finally, conduction losses ($P_{Conduction\ loss}$) and switching losses ($P_{Switching\ loss}$) are calculated based on different parameters such as switching frequency, active switches, block voltage of the individual switches, and time switches gets on-off during 0-π/2. The proposed topology uses less number of switches and guarantees low switching loss. The fundamental switching scheme is implemented for the proposed topology which leads to the reduction of the number of switches' on and off. The switching loss of each topology is shown in Fig. 4(a) for the symmetric method. In this paper, the t_{on} and t_{off} are considered as 2μs and the switching frequency is 50 Hz. The corresponding blocking voltage of each switch is taken into account. Reasonably, a high number of on-state switches produce more switching and conduction losses. The on-state switches for a different number of levels are illustrated in Fig. 4(b). Figs. 4(a) and 4(b) validate that the proposed topology produce low switching loss compared to the other topologies.

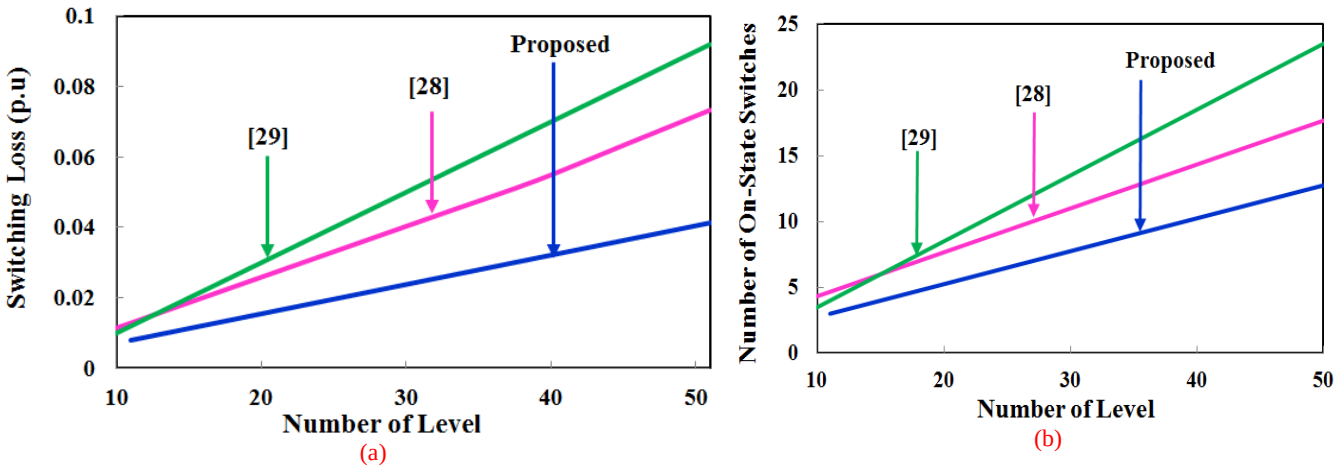


Fig. 4. Comparison of the switching loss and number of on-state switches versus the number of level of the proposed and other topologies (a) Switching loss versus N_{Level}, (b) On-state switches versus N_{Level}

Table 5 shows a summary of the total power loss (T_{Loss}) of the different topologies versus the number of levels, where the total losses can be calculated as given in Equation (13). Additionally, a transistor voltage drop (V_T) is assumed to be 2.5V, and a diode voltage drop (V_d) is assumed to be 1.5V, where, the transistor resistance R_T and the diode resistance are given respectively in ohms as R_T=0.15 and R_d=0.1. Transistor specification β=1 and the fundamental switching frequency=50Hz.

$$T_{Loss} = P_{Conduction\ Loss} + P_{Switching\ Loss} \qquad (13)$$

On the other side, asymmetric methods use different magnitudes of the sources compared to the symmetric methods. The asymmetric method can produce the highest number of output voltage level with reduced number of switches.

TABLE 5 Total losses calculation for the different topologies

Presented in [29]			Presented in [28]			Proposed Topology		
Number of Conduction Switches	Level	T_{Loss} (pu)	Number of Conduction Switches	Level	T_{Loss} (pu)	Number of Conduction Switches	Level	T_{Loss} (pu)
5	9	0.2	6	9	0.98	5	11	0.82
6	11	0.84	9	15	1.47	7	19	1.14
7	13	1.14	12	21	1.96	9	27	1.47
8	15	1.31	15	27	2.46	11	35	1.80
9	17	1.47	18	33	2.95	13	43	2.13
10	19	1.64	21	39	3.44	15	51	2.46
11	21	1.80	24	45	3.93	17	59	2.78
12	23	1.96	27	51	4.28	19	67	3.16
13	25	2.13	30	57	4.92	21	75	3.44
14	27	2.29	33	63	5.41	23	83	3.72
15	29	2.46	36	69	5.90	25	91	4.10
16	31	2.62	39	75	6.39	27	99	4.42
17	33	2.78	42	81	6.88	29	107	4.75
18	35	2.95	45	87	7.38	31	115	5.08
19	37	3.11	48	93	7.87	33	123	5.41
20	39	3.28	51	99	8.36	35	131	5.74

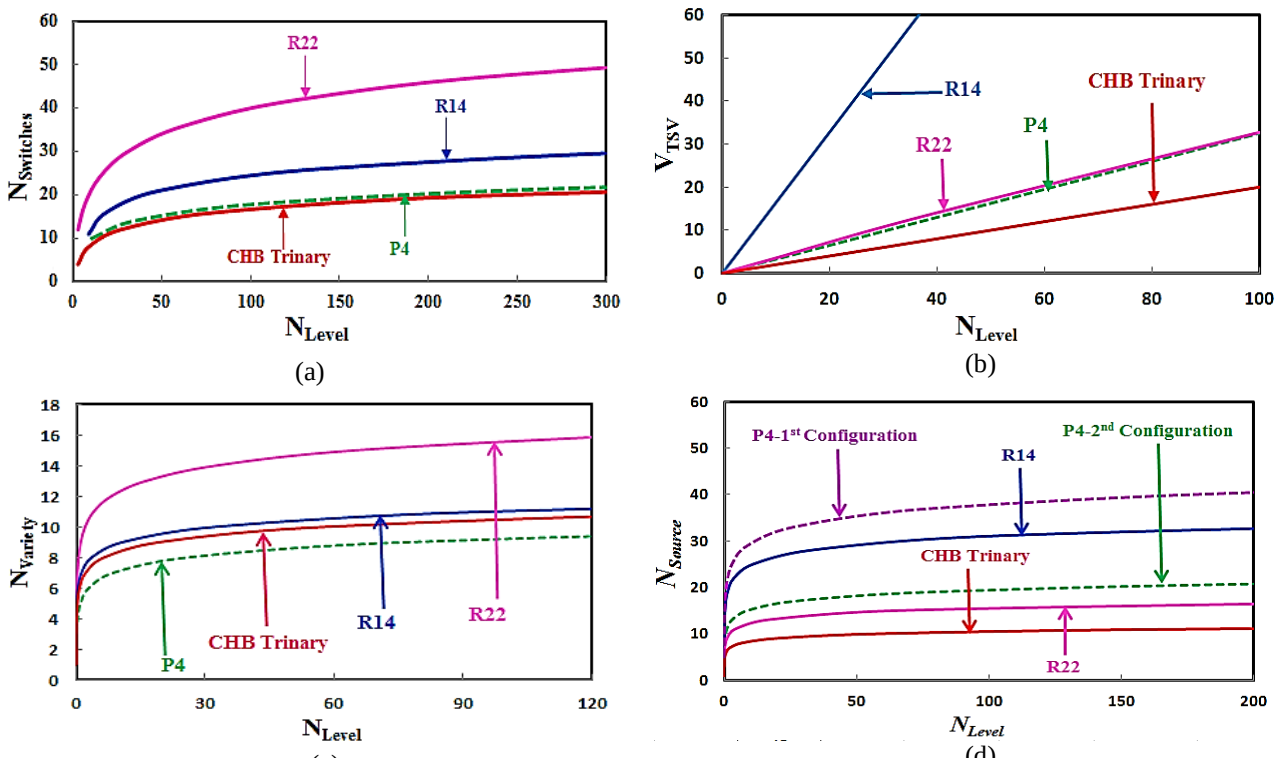


Fig. 5. Comparison of asymmetric methods (a) N_{Level} versus $N_{Switches}$ (b) N_{Level} versus V_{TSV}, (c) N_{Switch} versus $N_{Variety}$ and (d) N_{Level} versus N_{Source}

Fig. 5(a) shows a comparison of the number of the switches versus the number of levels for the algorithms P_4, R_{14}, R_{22} and CHB Trinary configuration. It is clear that proposed algorithm and the CHB trinary configuration produce a higher number of levels compared to other two topologies. In the asymmetric method, the various voltage ratings of switches are required, and the total standing voltage by switches is increasing whenever the number of level increases. The conventional CHB trinary configuration requires lower standing voltage of switches compared to the proposed asymmetric topology. The total standing voltage is lower than other two topologies presented in [28] and [29] for the same output voltage level, as revealed in Fig. 5(b). Moreover, the proposed topology offers a fewer number of DC sources with less variety as illustrated in Figs. 5(c) and 5(d). Briefly, the proposed topology requires a lower number of switches, gate driver circuits, and relatively fewer varieties of the magnitudes of the DC sources to generate the same number of output voltage levels compared to those values of [28] and [29].

The aim of this paper is to reduce the number of switches in the high voltage levels and also to reduce the blocking voltage of switches. **Table 6** presents a comparison of the proposed topology and the topologies presented in [28] and [29]. It validates that the proposed topology requires a lower number of switches compared to other topologies. Besides, the total blocking voltage is also lower than that presented in [28] and approximately equal to that presented in [29]. In addition, the proposed topology has a low lower number of DC sources.

TABLE 6 Comparison of the proposed topology and the topologies presented in [28] and [29]

Description	Number of level	Number of switches	Number of gate-driver circuits	Number of DC sources	Maximum blocking voltage (V)	Total blocking voltage (V)	Switch reduction ratio (%)	Total blocking voltage reduction ratio (%)
Proposed topology	51	30	30	13	25	162	-	-
	75	42	42	19	37	240	-	-
	99	54	54	25	49	318	-	-
[28]	51	46	46	25	25	174	35.00	7.00
	75	66	66	37	37	258	36.50	8.00
	99	86	86	49	49	342	38.00	9.00
[29]	51	52	52	25	25	160	42.31	-1.23
	75	76	76	37	37	238	44.74	-0.83
	99	100	100	49	49	316	46.00	-0.63

On the other side, although the proposed topology requires a minimum number of components, it requires additional voltage balancing circuits. Accordingly, a comparison between the total number of components for a particular level , with and without balancing circuits, is given in **Table 7**, where all the topologies require the same number of DC-link capacitors to maintain the DC voltage but with additional six capacitors for the voltage balancing circuits in the proposed topology. It is obvious that the proposed topology still require less number of components.

TABLE 7 The required components for a 27- level inverter

Description	Proposed	[28]	[28]
Power switches (IGBT)	18	26	28
Gate-drivers	18	26	28
Optocouplers	18	26	28
Heat sinks	18	26	28
DC sources	7	13	13
DC-link capacitors	13	13	13
Total number of components without voltage balancing circuit	91	117	138
Power diodes	24	-	-
Auxiliary capacitor	6	-	-
Total number of components with voltage balancing circuit	122	130	138

V. Simulation and Experimental Results

The scheme of the proposed topology is given in Fig. 6. The nearest level control method is used to construct the appropriate gate pulses for the switches. To validate the functional usage of the proposed multilevel converter; an experimental prototype based on the basic unit configuration given in Fig. 1(c), is developed for a resistive-inductive (RL) load with R=70 ohms and L=50 mH.

The simulated voltage and current waveform are shown in Figs. 7(a) and 7(b), and the voltage across the DC-link capacitor waveforms, with and without the voltage balancing circuits, are shown in Figs. 7(c) and 7(d), respectively. Determination of the magnitude of the voltage sources for the experimental 11-level multilevel converter is configured on the basis of the second algorithm (P_2). Moreover, the conventional nearest-voltage level modulation technique, presented in [40], is embedded in the FPGA Spartan XE3S250E controller (that

generates the trigger pulses to the appropriate switches) with a fundamental frequency of 50 Hz. Three DC voltage sources V_1=44V (C_1=C_2=22V), V_2=44V (C_3=C_4=22V) and V_1'=22 V, Ten IGBTs (BUP400D), and eight IGBT drivers (HCPL316j) are employed to generate the 11-level output voltage at the load side with a maximum output voltage of 110 V and RMS value of 74.08 V.

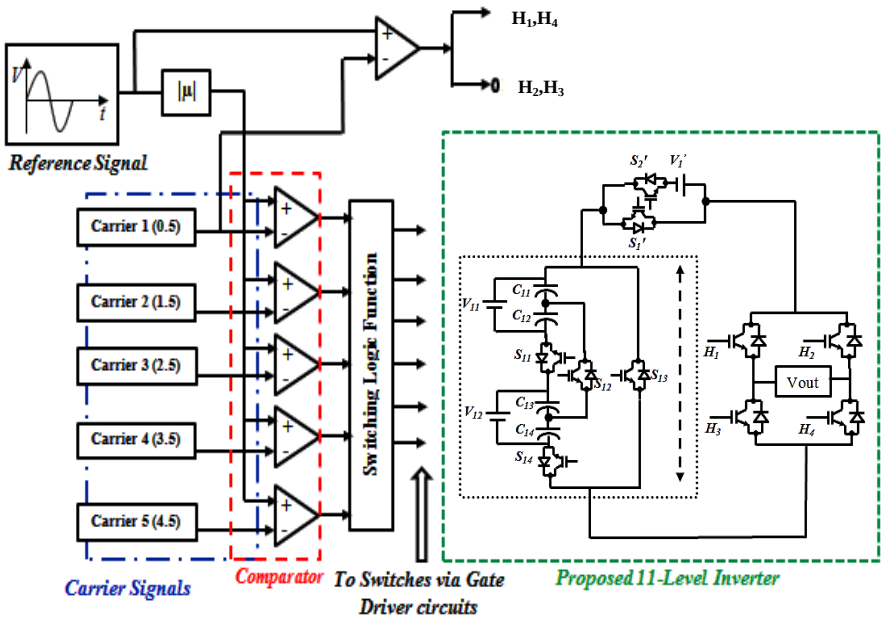
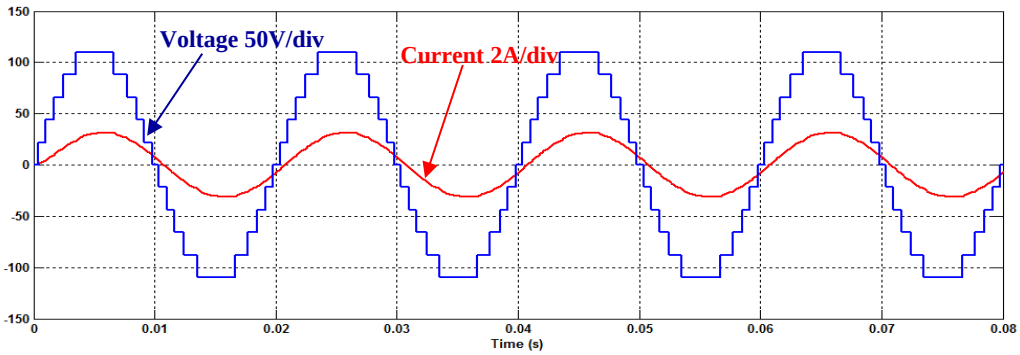


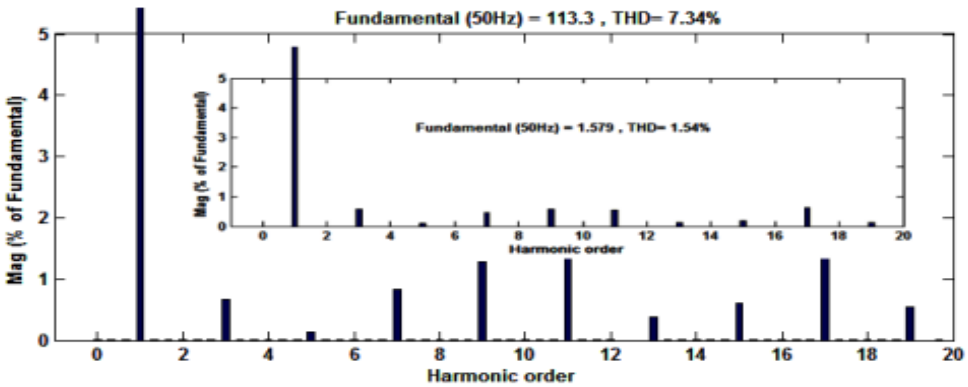
Fig. 6. Schematic diagram of a proposed 11-level inverter

The experimental output voltage and current waveforms are shown in Fig. 8(a). The current waveform is almost sinusoidal as the inductive load acts as a low-pass filter at the load terminals. Based on the experimental results, total harmonic distortion percentages of the load voltage and load current are demonstrated in Figs.8 (b) and 8(c), and their values are given as 8.0% and 2.9%, respectively, which indicate an adequate agreement of both experimental and simulation results. A photograph of the prototype model is shown in Fig. 8(d).

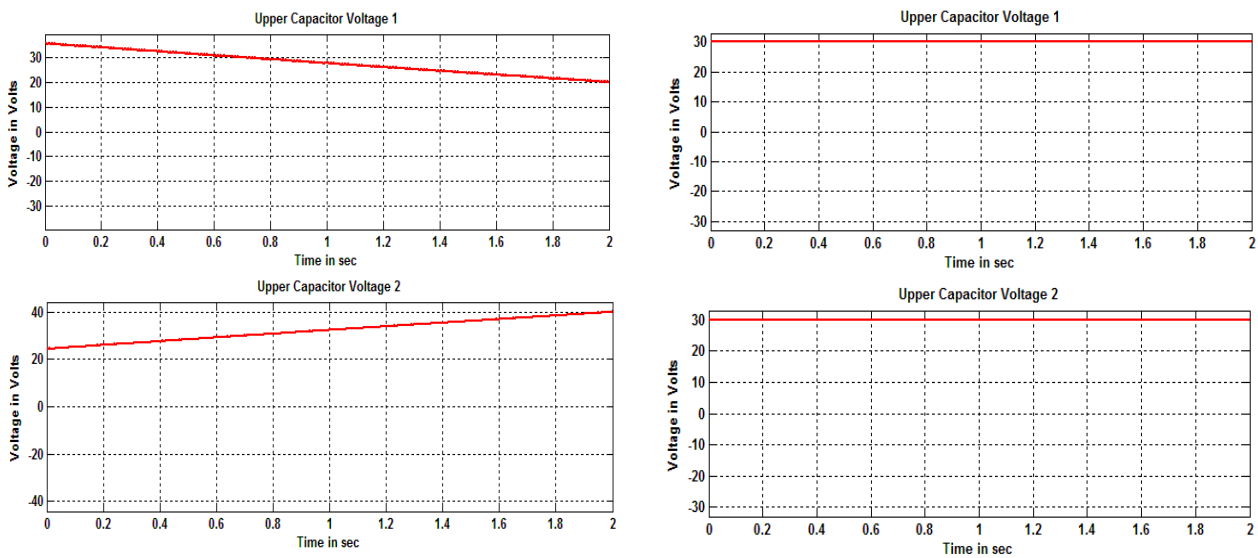
Since balancing voltage across the series connected DC-link capacitor is another important issue in the multilevel inverter designs; two different voltage balancing circuits are presented for both regulated and unregulated DC sources, as shown in Fig. 9. In Fig. 9(a), four power diodes with one auxiliary capacitor (C_a) is presented, while Fig. 9(b) shows that the unregulated DC source can be regulated by a boost converter [43], [44].



(a)

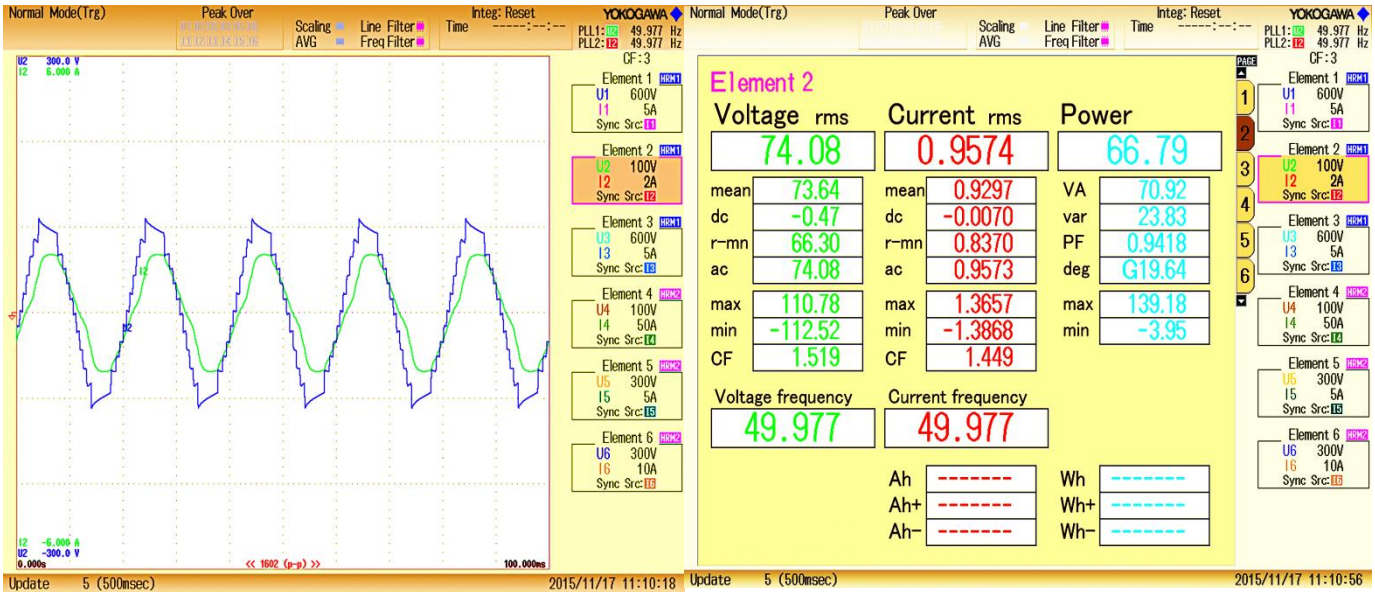


(b)

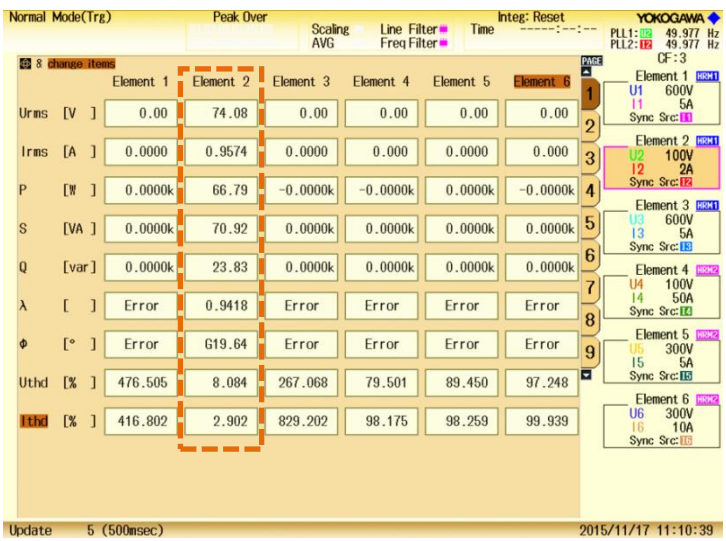


(c) (d)

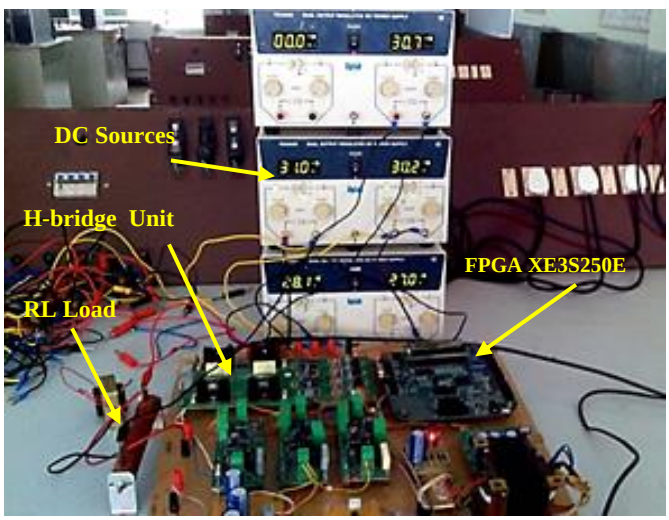
Fig. 7. Simulation results (a) Simulated output voltage and current waveforms, (b) THD and harmonic spectra of the voltage and current, (c) Unbalanced capacitor voltages for the second configuration, and (d) Balanced capacitor voltages for the second configuration



(a) (b)



(c)



(d)

Fig. 8. Experimental setup of the proposed multilevel inverter, (a) The experimental output voltage and current waveform of the proposed multilevel inverter, (b) The power quality analyzer outputs, (c) The THD of proposed multilevel inverter, and (d) Hardware photograph.

The voltage reference signal generated for an amplitude of 5V with the fundamental frequency of 50Hz. This reference signal is compared with various dc offset value ranges from 0.5 to 4.5V. The logical comparator produces the corresponding pulses for various levels. As per the switching tables, the comparator output signal is manipulated with help of the logic gates to generate the pulses for each switch by using MATLAB/Simulink, as shown in Fig.10(a).

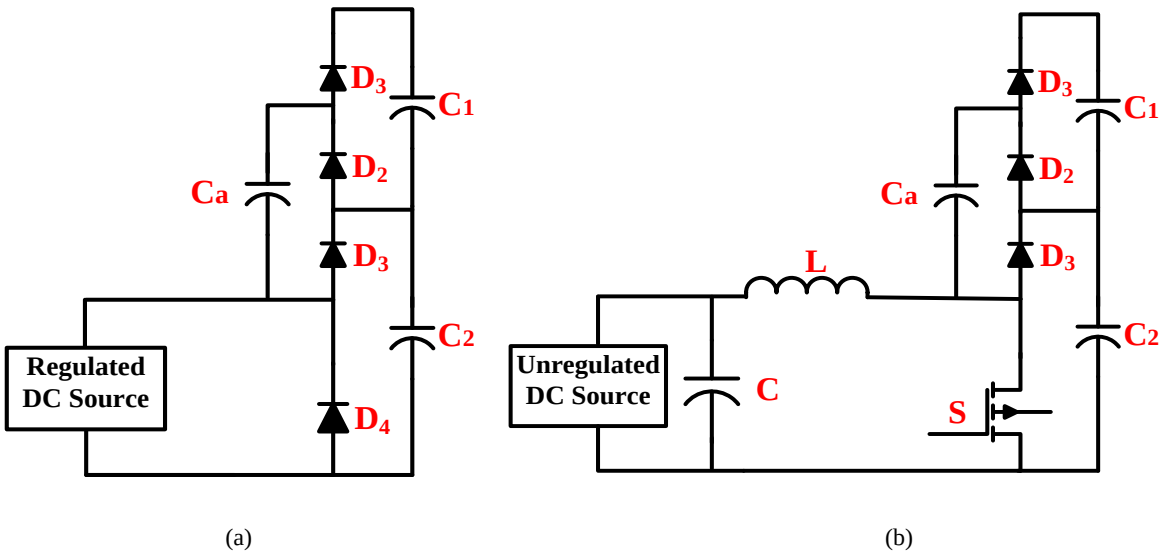
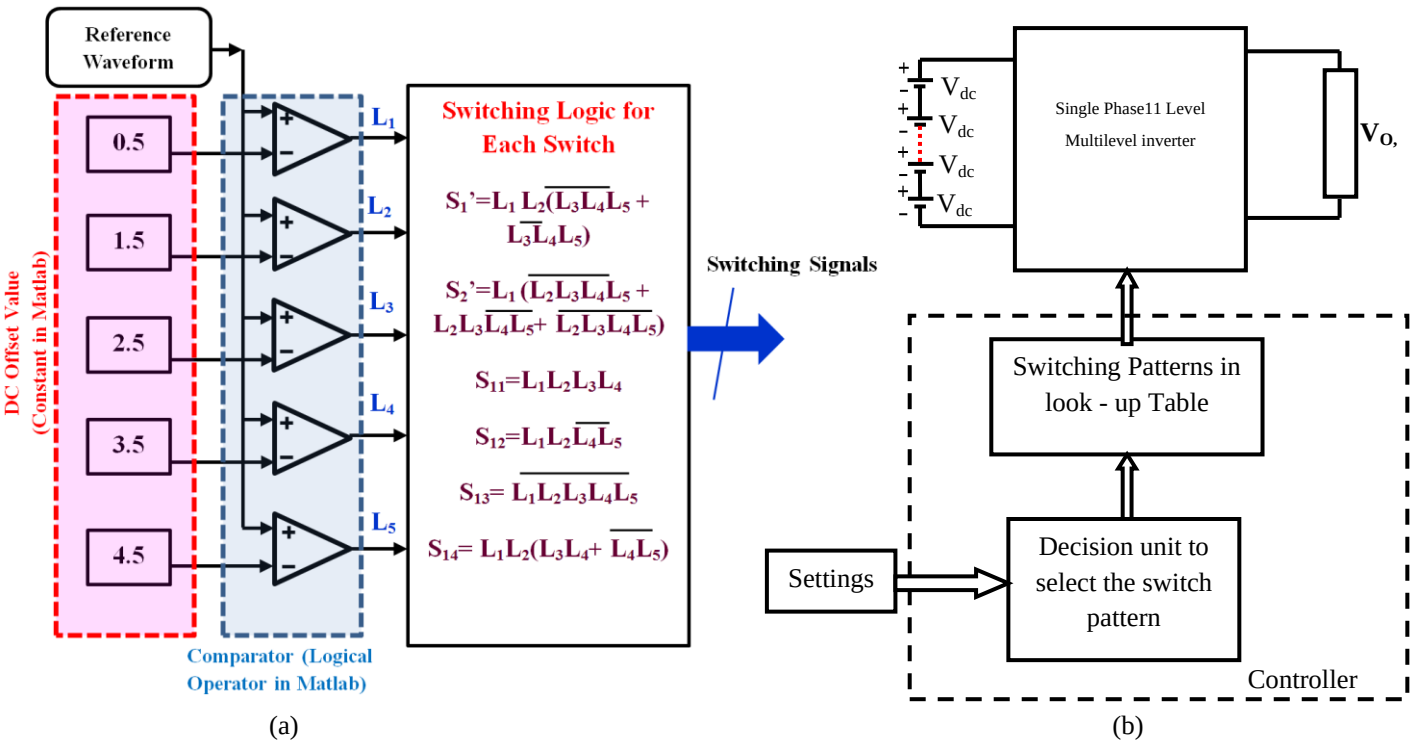


Fig. 9. The voltage balancing circuits for series connected DC-link capciotrs (a) For regulated DC sources (b) Unregulated DC sources

In the experimental study, the DC signal ranges between the minimum and maximum voltages wave of the sine waveform. When the sinusoidal waveform voltage is greater than the DC level, the output of the op-amp swings high, and when it is low, the output swings low. An array of integer range from '-256 to 256' is generated in FPGA coding and these values are stored in the look-up table as shown in Fig. 10(b). The sinusoidal reference signal is sampled from ‘0, 8, 16,…, 256’ for the positive signal, and ‘0,-8,-16, …..,-256’ for the negative signal. The pulses generated by the FPGA controller are shown in Fig. 10(c). These sampled signals are compared with the DC Offset level to generate the switching pulses. By using logical operators such as the AND, OR gates, the corresponding switching pulses for each switch is generated and addressed to the particular output port number. The output port signals are directly given to the switches through optocoupler and gate driver circuits. The gate driver circuit consists of optocoupler, Schmitt trigger circuits, and buffer as shown in Fig. 11. The optocoupler provides better isolation between the controller and the switch. The output of the optocoupler is not constant but can be regulated by the Schmitt trigger circuit to produce the appropriate pulse with the required amplitude. The buffer provides a storage and delay of the input signal. The dead time for each signal is considered in software coding. The gate driver circuit consists of optocoupler, Schmitt trigger circuits, and buffer as shown in Fig. 11. The optocoupler provides better isolation between the controller and the switch. The output of the optocoupler is not constant but can be regulated by the Schmitt trigger circuit to

produce the appropriate pulse with the required amplitude. The buffer provides a storage and delay of the input signal. The dead time for each signal is considered in software coding. The gate pulses for the individual switches are illustrated in Fig. 12.



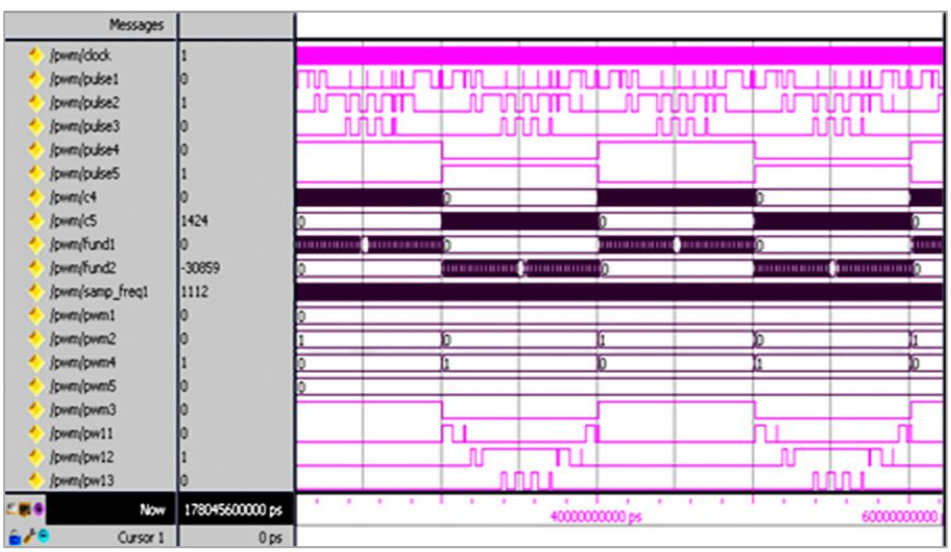


Fig. 10. Control Block Diagram for proposed method (a) For Simulation and (b) For Experimental (c) Pulse waveform generated by FPGA Controller

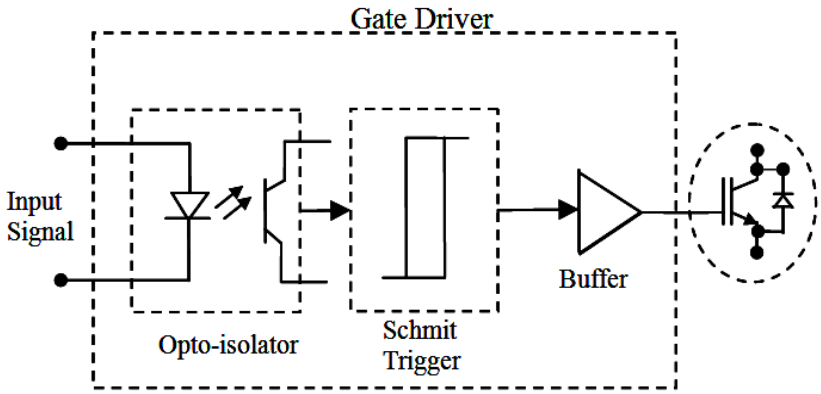


Fig. 11. Gate driver circuit and switching mechanism for the switch

The efficiency (η) is an important index to assess the proposed converter. Hence, the calculated efficiency of the converter is presented in **Table 8**. The total input power, given in Table 8, is the sum of the power delivered by each DC source. Also, **Table 9** illustrates a cost comparison, based on the cost of the switches, of the proposed symmetric configuration with a corresponding CHB based converter with the same number of levels. It is obvious that the total cost of the symmetric configuration of the considered topology is lower than the corresponding total cost of the other CHB converter.

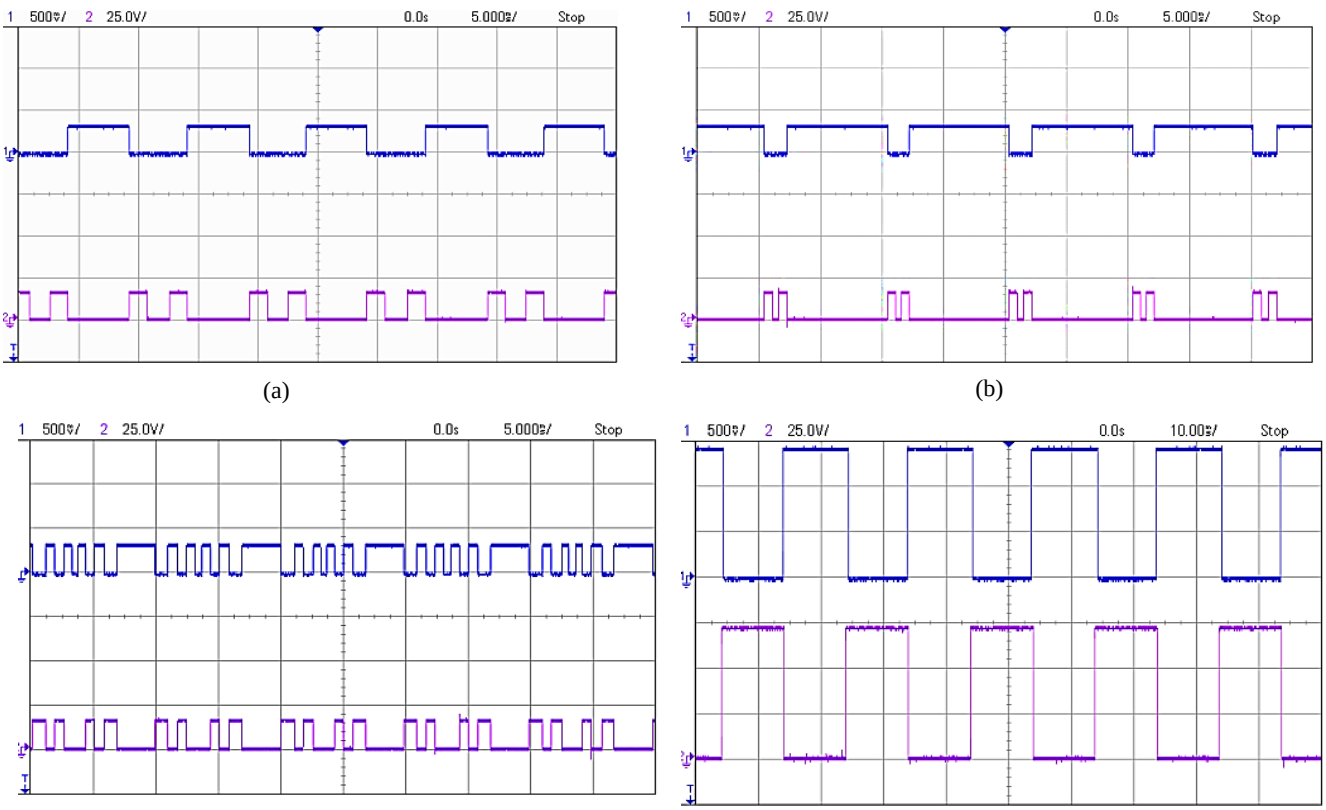


Fig. 12. Gating Signals to the IGBT in the proposed multilevel inverter (in CH2 1:10 Probe with 5V/div), (a) S_6,S_4, (b) S_4,S_5, (c) S_2,S_1 and (d) H_1 & H_2

TABLE 8 Power and efficiency calculations of the proposed converter based on simulations

Input power			Output Power	Efficiency
V_1'=22V	C_{11}= C_{13}=44V	C_{12}= C_{14}=44V		
8.04 W	39.28 W	41.72 W	82.1 W	92.7 %

TABLE 9 Cost comparison of the proposed symmetric configuration with other CHB converter, with equal number of levels

Courtesy	Part Number	Voltage rating	Quantity	Unit price* ($)	Cost ($)	
					Proposed 35-level	CHB 35-level
www.galco.com [41]	Item#CM400DU-5F (Dual Pack)	250V	1	254.91	509.82	8666.94
	Item#CM400DU-12F (Dual Pack)	600V	6	217.21	1303.26	-
www.theelectrostore.com [42]	Item#FF400R12KE3 (Dual Pack)	1200V	2	183.24	366.48	-
	Item#CM400HB-90H (Single HV-IGBT)	4500V	4	995	3980	-
Total Cost ($)					6159.56	8666.94

* *The prices may vary based on market growth*

The proposed configuration, with 35 levels, needs 22 switches with a total cost of $6,159.56, while a conventional CHB converter needs 68 switches with a total cost of $8,666.94 to practice the same number of levels. Furthermore, one can note that both configurations use the same number of switches for equal numbers of output voltage levels. However, for the symmetric topology, only the first configuration can be used, while the second configuration cannot be used. Regarding the asymmetric topology, both configurations can be used to generate a high number of output voltage level with the same number of switches, but with a different number of DC sources.

Regarding the total harmonic distortion (THD) percentage, **Table 10** presents a comparison between the proposed topology and the topologies presented in [28] and [29]. The proposed topology produces the maximum number of levels with reduced voltage harmonic profile. The summary of the proposed topology for the 11-level inverter with both simulation and experimental results are given in **Table 11**.

TABLE 10 Comparison of the proposed topology and the topologies presented in [28] and [29] with the same number of switches

Topologies	Proposed	[28]	[29]
Switch (IGBT)	26	26	26
Number of level	43	27	25
Voltage total harmonics distortion (%)	1.7	2.6	2.8

TABLE 11. Experimental versus simulation values

Parameter		**Simulation**	**Experimental**
Input voltage (V)		110	
Load resistance (Ω)		70	
Load inductance (mH)		50	
%THD	Voltage	7.34	8.0
	Current	1.54	2.09
V_{rms} (V)		77.54	74.08
I_{rms} (A)		1.00	0.95
Output power (W)		77.54	66.79

VI. Conclusion and Future Work

A new single-phase cascaded multilevel converter based on a new basic unit is proposed, where the unit is configured into two different structures. The performance of the proposed topology for both configurations is illustrated and compared. Four different algorithms are introduced to find the magnitudes of the DC voltage sources for the proposed topology. Among these algorithms, the fourth one can be used to obtain the maximum output voltage level with a lower number of switches (or anti-parallel diodes) and with different DC sources' magnitudes. Moreover, the performance and effectiveness of the proposed converter were verified by the experimental results achieved by a single-phase 11-level converter.

For the asymmetric configuration, the cost of the converter depends on the number of DC sources. Hence, in order not to lose generality, all the equations in this work are derived based on the first configuration,

as it can operate in symmetric and asymmetric topologies alike. However, for the asymmetric topology, the second configuration is practiced using two DC sources with four capacitors instead of using four DC sources.

The main advantage of the proposed converter is increasing the number of output voltage levels through reducing the number of switches, power diodes, driver circuit and DC voltage sources, with less or equal amount of the blocked voltage by the switches compared with other published schemes. However, the full bridge converter should withstand the maximum blocking voltage; hence, the stress across the switches will increase, as well as the cost. Accordingly, high-voltage applications may be restricted.

On the other side, the considered topology is suitable for medium-voltage applications, such as grid-connected PV system ranging from 2.3 kV up to 6 kV with a reasonable cost. To overcome the high-voltage applications restriction; much attention should be paid to enhancing the performance of the proposed topology with a cascaded hybrid topology to generate a high number of output voltage levels with a considerable reduction of the voltage stress of the full bridge of the converter. Hence, reduced cost of the converter may be achieved in high-voltage applications. The findings of this point will be presented in future work.

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